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LCL filter based UPQC configuration for power quality improvement

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LCL Filter Based UPQC Configuration for Power Quality Improvement

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***Abstract*—This paper proposes a unified power quality conditioner (UPQC) configuration employing an LCL filter at front of shunt voltage source inverter (VSI). As compared to conventional UPQC with L filter at the front of the shunt VSI, the proposed UPQC provides improved compensation while using much smaller value of filter inductance. With the smaller filter inductance, voltage requirement of common dc link also gets reduced. It results in reduced switching losses in the series and shunt VSIs. Therefore, proposed UPQC achieves reduction in weight, cost, size, and losses while providing improved current compensation capability. Simulation results are presented to verify all the features.**

Index Terms: Power factor, harmonics, voltage regulation

I. Introduction

Major power quality (PQ) issues in the power distribution system are unbalanced distorted source current, poor power factor, voltage sag, swell and unbalance, flicker, transients, etc. The unified power quality conditioner (UPQC) has been proposed for simultaneously eliminating these PQ problems with extensive focus on reference generation technique and optimal utilization [1]–[3]. However, the compensation performance of the UPQC largely depends upon the passive filters. These passive filters condition the polluted output of VSI containing higher frequency components, and ensure filtered voltage or current at the PCC.

Presently, almost all UPQC topologies use an L type filter at front of shunt VSI to shape injected currents [1], [2], [4]. The L filter uses a bulky inductor, has a low slew rate for reference tracking, and produces large voltage drop which results in need for higher value of dc link voltage for proper compensation. Another issue with UPQC operation is common dc link voltage requirement. When series and shunt active power filters (APFs) operate separately, both require different voltages at the dc bus [5]. When series and shunt APFs are combined to form UPQC, dc bus voltage is chosen based on requirement of overall performance which uses higher dc voltage rating required by shunt APF. But, higher dc bus voltage increases voltage and power rating of series VSI, increases stress on the VSI switches which in turn increases switching losses, and requires bigger inductor to limit the maximum switching frequency.

Recently, LCL filter has been used at front end of VSI instead of L filter [6]–[8]. This scheme provides better reference tracking performance while using much lower value of passive components. Also, lower value of passive components ensures that the voltage drop across them is much less. Consequently, the dc link voltage requirement for the LCL filter based shunt VSI will be lesser compared to the L filter based shunt VSI.

Unfortunately, there is lack of literature dealing with the application of LCL filter in the UPQC operation. To fill this gap, this paper proposes a new UPQC configuration integrating an LCL passive filter at the front end of shunt VSI. As compared to conventional UPQC topologies, proposed configuration provides better compensation capability while using smaller value of filter inductance. Therefore, source current quality is improved while reducing the size, weight, and cost of the passive filter. Also, due to requirement of lower dc voltage by LCL filter, losses in both VSIs will decrease. Moreover, performance of the series VSI will also improve while using a smaller inductor.

II. Proposed and Conventional UPQC Configuration

Equivalent circuit diagram of proposed UPQC configuration is shown in Fig. 1. This consists of two VSIs with a common neutral point clamped dc-link between them. An LCL filter is connected at the front end of shunt VSI. The components R_1 and L_1 are resistance and inductance, respectively at the filter side, R_2 and L_2 are resistance and inductance, respectively at the grid side, and C is the filter capacitance forming LCL filter part in all three phases. A damping resistance R_d is used in series with C to provide passive damping to the overall system. The elements L_{se}, C_{se}, and R_{se} together form the ripple filter in all three phases which filters out the switching frequency components of the VSI. C_{dc} is capacitance of both dc link capacitors, whereas a voltage of V_{dc} is maintained across each of them.

Conventional UPQC topology connects an L filter at the front end of shunt VSI. Filter inductance and resistance of shunt VSI in each phase are given by L_f and R_f, respectively.

III. Control of the UPQC

A. Derivation of Reference Currents of Shunt APF

In this paper, instantaneous symmetrical component theory based control algorithm is used to compute reference filter currents (i^*_{f2j} where j = a, b, c) [9] as follows:

$$i^*_{f2j} = i_{lj} - i^*_{sj} = i_{lj} - \frac{v^+_{lj1}}{\Delta^+_1}(P_{lavg} + P_{loss}) \qquad (1)$$

where $\Delta^+_1 = (v^+_{la1})^2 + (v^+_{lb1})^2 + (v^+_{lc1})^2$. Voltages v^+_{la1}, v^+_{lb1}, and v^+_{lc1} are fundamental positive sequence voltages at phases

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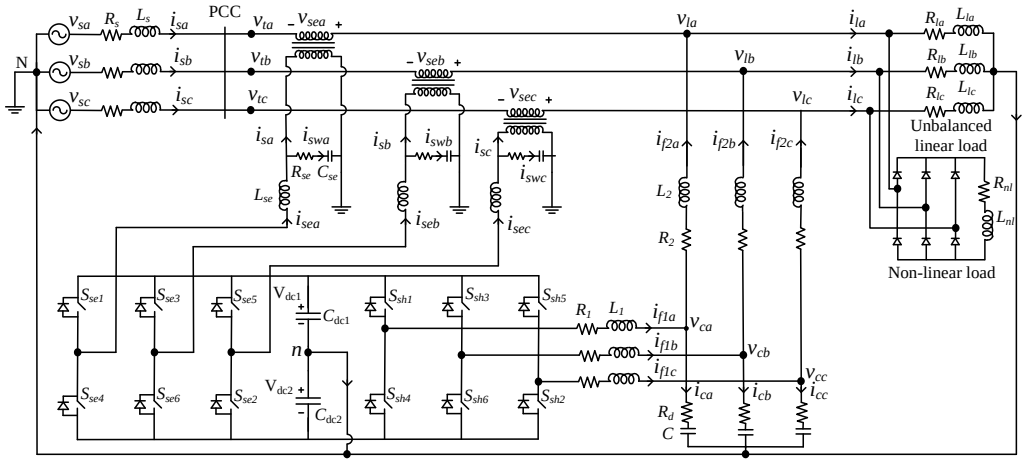

Fig. 1. Proposed UPQC configuration in a distribution system.

a, b, and c, respectively. The terms P_{lavg} and P_{loss} are average load power and total losses in the VSI, respectively. P_{lavg} is calculated using a moving average filter as following:

$$P_{lavg} = \frac{1}{T}\int_{t_1}^{t_1+T} (v_{la}i_{la} + v_{lb}i_{lb} + v_{lc}i_{lc})\, dt \qquad (2)$$

where t_1 and T are any time instant and source time period, respectively. P_{loss} is computed using a proportional-integral (PI) controller given as follows:

$$P_{loss} = K_p\, e_{vdc} + K_i \int e_{vdc}\, dt \qquad (3)$$

where K_p, K_i, and e_{vdc} = $2\,V_{dcref}$ - $(v_{dc1} + v_{dc2})$ are proportional gain, integral gain, and voltage error of the PI controller, respectively.

B. Derivation of Reference Voltages of Series APF

Series VSI in UPQC applications maintains load voltages balanced and sinusoidal during normal supply voltage as well as during voltage disturbances like sag, swell, unbalances, etc. Let three phase instantaneous balanced and sinusoidal reference voltages that need to be maintained at the load terminal are

$$\begin{aligned} v_{la}^* &= \sqrt{2}\, V_l^*\, \sin(2\pi f t - \theta_{vla1}^+) \\ v_{lb}^* &= \sqrt{2}\, V_l^*\, \sin(2\pi f t - 2\pi/3 - \theta_{vla1}^+). \\ v_{lc}^* &= \sqrt{2}\, V_l^*\, \sin(2\pi f t + 2\pi/3 - \theta_{vla1}^+) \end{aligned} \qquad (4)$$

In (4), V_l^* is reference load voltage magnitude (it is taken as nominal voltage i.e., 1.0 pu in this paper). The angle θ_{vla1}^+ is angle of the fundamental positive sequence of actual load voltages. The instantaneous reference voltages injected by the series APF (v_{sea}^*, v_{seb}^*, and v_{sec}^*) will be difference between the instantaneous reference load voltages and corresponding actual PCC voltages.

Complete block diagram of the UPQC controller is shown in Fig. 2. The hysteresis control action is used for controlling the VSI switches [9].

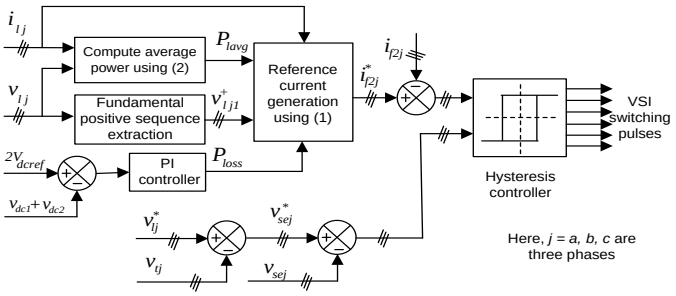

Fig. 2. Control block diagram of the UPQC.

IV. UPQC Parameters Design

A. Design of Parameters of dc Link

1) Reference dc Link Voltage (V_{dcref}): Application of LCL filter at the shunt VSI results in significant reduction in filter inductance as compared to conventional UPQC scheme. Consequently, voltage drop across filter inductor reduces and enables proposed scheme to operate satisfactorily with a reduced dc link voltage. In present case, a dc link voltage of 400 V is chosen which provides satisfactory tracking performance.

2) Storage Capacitance (C_{dc}): It is chosen based on its ability to regulate voltage during transients. With S_x as real power supplied by capacitor during transients, T as system time period, and n as number of cycles of transient, the maximum possible energy that capacitor can exchange with the load during transient will be $n\,S_x\,T$. This energy will be equal to change in stored energy of the capacitor. Hence,

$$\frac{1}{2}C_{dc}\left({V_{dcref}}^2 - V_{dc}^2\right) = n\,S_x\,T \qquad (5)$$

where V_{dc} is maximum allowed voltage variation from V_{dcref} during transients. Here, S_x = 25% of total load power (15 kVA), V_{dcref} = 400 V, n = 0.5, T = 0.02 s, and maximum change in dc link voltage during transient is $\pm 10\%$ of V_{dcref}.

B. Design of Parameters of Shunt APF

Values of LCL filter components should be chosen considering the several constraints such as cost of inductor, ripple in

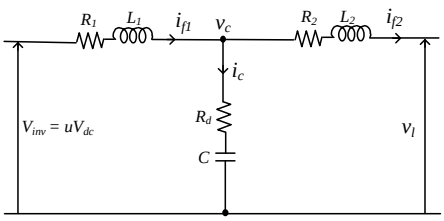

Fig. 3. Single phase circuit diagram of shunt VSI passive filter.

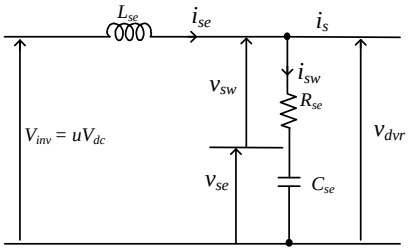

Fig. 4. Single phase equivalent circuit of series VSI passive filter.

current, resonance frequency (f_{res}), choice of damping resistor (R_d), and attenuation at switching frequency (f_{sw}) [6], [7], [10]. Fig. 3 shows the single phase equivalent circuit of shunt VSI passive filter. Here, inductor L_1 is chosen for attenuation of lower order harmonics. Considering that only L_1 of LCL filter is used, its dynamics is given as

$$L_1 \frac{di_{fl}}{dt} = -v_l - R_1 i_{fl} + V_{inv}. \tag{6}$$

The value of inductance L_1 is chosen from a trade-off, which provides reasonably high switching frequency and sufficient rate of change of filter current, such that the VSI currents follow the reference currents. The inductor is designed to provide good tracking performance at maximum switching frequency which is achieved at the zero of the supply voltage in hysteresis current control (HCC) scheme [11]. Therefore, inductance L_1 is given by

$$L_1 = \frac{V_{dcref}}{(2\,h_c)\,(2\,f_{max})} = \frac{V_{dcref}}{4\,h_c\,f_{max}} \tag{7}$$

where $2h_c$ is allowable ripple in the current and f_{max} is maximum switching frequency achieved by HCC.

Here, a current ripple of 20% is taken while compromising ripple and inductor size [10]. Substituting values of ripple current and reference dc link voltage V_{dcref} in (7) while keeping maximum switching frequency (f_{max}) at 10 kHz, value of L_1 will be 4.54 mH.

L_2 and C are designed for elimination of higher order harmonics. Without damping resistor while neglecting R_1 and R_2, expression for the resonance frequency is given as follows:

$$f_{res} = \frac{1}{2\,\pi}\sqrt{\frac{1+k}{k\,L_1 C}} \tag{8}$$

where $k = L_2/L_1$. Resonance frequency must be greater than the highest order of harmonics current to be compensated. If highest harmonics order to be compensated is 30 and taking a variation of 20%, f_{res} turns out to be 1800 Hz for a 50 Hz system. For ensuring low loss and high efficiency, a lower value of k is selected (k<1) [8]. A higher C will provide a low impedance path for harmonics, but will draw more reactive current from VSI which further increases loss in L_1 and IGBT switch. However, a smaller capacitance will not provide sufficient attenuation which in turn is compensated by selecting larger inductor. As a trade-off between these requirements, C = 10 μF is chosen. The value of k is found to be 0.438 using (8). With this value of k, L_2 will be 2 mH.

Equivalent impedance of the LCL filter approaches to zero at the resonance frequency (f_{res}) and system may become unstable. However, system can be made stable by inserting a resistance (R_d) in series with the capacitor. Usually, it is chosen more than the capacitive reactance at f_{res} (X_{cres}) such that the damping losses are minimum while assuring that the sufficient resonance damping is provided to the system [12].

C. Design of Parameters of Series APF

Single phase circuit diagram of passive filter of series APF is given in Fig. 4. A detailed design procedure has been presented in following section [13].

1) Design of Inductor (L_{se}): At any point of time, inductor dynamics is represented by following equation:

$$L_{se} \frac{di_{se}}{dt} = -v_{dvr} + V_{dcref} \tag{9}$$

where $i_{se} = i_s + i_{sw}$. Practically, source current variations are much slower as compared to the capacitor current. Therefore, $\frac{di_{se}}{dt} = \frac{d(i_{sw}+i_s)}{dt} \approx \frac{di_{sw}}{dt}$. Replacing this expression in (9)

$$L_{se} \frac{di_{sw}}{t_{on}} = V_{dcref} - v_{dvr}. \tag{10}$$

Assuming that the rate of change of capacitor current is same in both ON as well as OFF switching state, switching frequency f_{sw} can be given as follows:

$$f_{sw} = \frac{V_{dcref} - v_{dvr}}{2\,L_{se}\,di_{se}}. \tag{11}$$

From Fig. 4, voltage across the DVR is given as

$$v_{dvr} = R_{se} i_{sw} + \frac{1}{C_{se}} \int i_{sw}\,dt \tag{12}$$

Differentiating above equation with respect to time

$$\frac{dv_{dvr}}{dt} = R_{se} \frac{di_{sw}}{dt} + \frac{1}{C_{se}} i_{sw}. \tag{13}$$

The capacitor will draw negligible current at lower order harmonics, and will provide a low impedance path at higher order harmonics. Thus, voltage drop across the capacitor will be negligible at the higher order harmonics. Moreover, drop across resistor will be predominant at higher order frequencies and will be nearly equal to $2\,h_v$. Hence, (13) becomes

$$di_{sw} = \frac{2\,h_v}{R_{se}}. \tag{14}$$

Substituting (14) into (11)

$$f_{sw} = \frac{R_{se}}{4\,L_{se}\,h_v}\,[V_{dcref} - v_{dvr}]\,. \tag{15}$$

TABLE I
SIMULATION PARAMETERS

System quantities	Values
Source voltage	230 V rms line to neutral, 50 Hz
Feeder parameters	R_s = 0.5 Ω, L_s = 0.5 mH
Linear load	Z_{la} = 20 + j94.2 Ω, Z_{lb} = 40 + j62.8 Ω, Z_{lc} = 50 + j94.2 Ω
Nonlinear load	R_{nl} = 50 Ω, L_{nl} = 300 mH
UPQC parameters (conventional scheme)	V_{dcref} = 520 V, C_{dc} = 2500 μF, L_f = 23.6 mH, R_f = 0.5 Ω L_{se} = 6.93 mH, C_{se} = 30 μF, R_{se} = 3.68 Ω
UPQC parameters (proposed topology)	V_{dcref} = 400 V, C_{dc} = 2500 μF, L_1 = 4.5 mH, L_2 = 2 mH, R_d = 25 Ω, $R_1 = R_2$ = 0.5 Ω, C = 10 μF, L_{se} = 5.5 mH, C_{se} = 30 μF, R_{se} = 3.68 Ω

In above equation, maximum switching frequency can be achieved for $v_{dvr} = 0$. Hence, filter inductance to limit maximum VSI frequency is given as following:

$$L_{se} = \frac{V_{dcref}\, R_{se}}{4\, h_v\, f_{max}}. \tag{16}$$

2) Design of Capacitor and Resistor (C_{se} and R_{se}): As already mentioned, the values of capacitor and resistor are chosen such that the voltage drop across the resistor will be much more than that the voltage across capacitor at the higher order frequency component. Therefore, series filter circuit acts as a first order circuit and makes voltage-current relation linear.

With UPQC in operation, source will supply only fundamental positive component of load currents. Consider I_s and I_{se} as rated currents to be drawn from source and current rating of the series VSI, respectively. Therefore, maximum current that can flow through the series capacitor C_{se} will be $I_{sw} = \sqrt{I_{se}^2 - I_s^2}$. At fundamental frequency, the voltage drop across resistor is negligible as compared to the capacitor, whereas at higher frequencies the voltage drop across capacitor is negligible compared to resistor. Therefore, I_{sw} can be divided into parts 1) fundamental current corresponding to voltage across capacitor (I_{sw1}); and 2) switching frequency current (I_{swh}). Therefore, $I_{sw} = \sqrt{I_{sw1}^2 + I_{swh}^2}$.

Neglecting voltage drop across resistor at fundamental frequency, voltage across capacitor is given as

$$V_{se} = V_{dvr} = I_{sw1}\, X_{se1} = \frac{I_{sw1}}{2\,\pi\, f_1\, C_{se}}. \tag{17}$$

Restricting total reactive current drawn by the capacitor to 5% of the rated load current, capacitor value will be

$$C_{se} = \frac{I_{se}}{40\,\pi\, f_1\, V_{ref1}}. \tag{18}$$

Further, neglecting capacitor voltage drop at higher frequency component, voltage across resistor is given as:

$$V_{sw} = I_{seh}\, R_{sw}. \tag{19}$$

At the switching frequency, the rms value of V_{sw} will be $h_v/\sqrt{3}$. Restricting total current drawn by the resistor to 5% of the rated current, the value of resistor is given as

$$R_{sw} = \frac{20\, h_v}{\sqrt{3}\, I_{se}}. \tag{20}$$

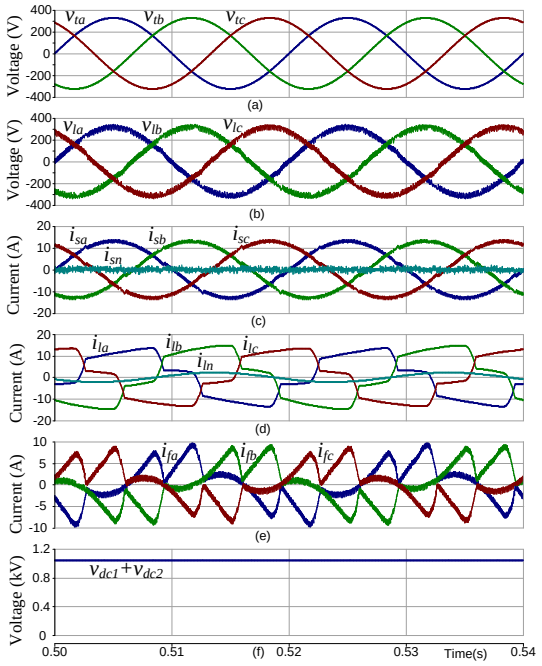

Fig. 5. Compensation performance of conventional UPQC. (a) PCC voltages. (b) Load voltages. (c) Source currents. (d) Load currents. (e) Shunt VSI currents. (f) Voltage at dc link. (L_f = 23.6 mH and L_{se} = 6.93 mH).

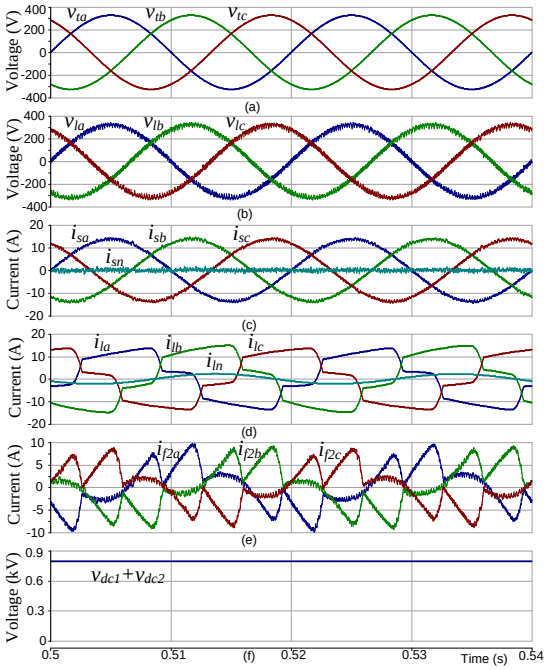

Fig. 6. Compensation performance of proposed UPQC. (a) PCC voltages. (b) Load voltages. (c) Source currents. (d) Load currents. (e) Shunt VSI currents. (f) Voltage at dc link. (L_1 = 4.5 mH, L_2 = 2 mH, C = 10 μF, L_{se} = 5.5 mH).

V. SIMULATION RESULTS

Firstly, steady state compensation performance of conventional scheme is shown in Fig. 5. As can be seen from the figure that the load voltages and source currents are balanced, sinusoidal, and in phase with the respective phases. However, these waveforms contain switching harmonic ripple

TABLE II
PERCENTAGE THDS IN SOURCE CURRENTS AND LOAD VOLTAGES

System configuration	i_{sa}	i_{sb}	i_{sc}	v_{la}	v_{lb}	v_{lc}
Without compensation	20.69	18.41	20.1	1.05	1.04	1.03
Compensation with conventional topology	2.3	2.2	2.05	1.13	1.11	1.05
Compensation with proposed topology	1.12	1.1	1.08	0.8	0.75	0.72

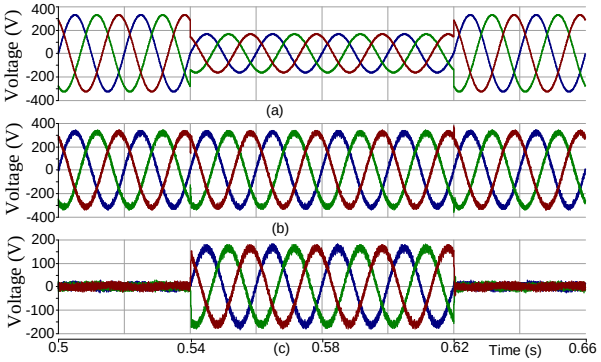

Fig. 7. Compensation performance of proposed UPQC during voltage sag. (a) PCC voltages. (b) Load voltages. (c) DVR injected voltages.

TABLE III
COMPARISON OF UPQC PARAMETERS

UPQC topology	Shunt VSI inductor	Series VSI inductor	Voltage at dc link
Conventional	23.6 mH	6.93 mH	1040 V
Proposed	6.5 mH	5.5 mH	800 V

component. Moreover, total dc link voltage is maintained at the reference value of 1040 V to achieve this compensation.

Fig. 6 illustrates the steady state simulation waveforms for the proposed UPQC configuration. The waveforms of three phase source voltages, load voltages, source currents, load currents, shunt VSI currents, and voltage at dc link are shown in Figs. 6(a)-(f), respectively. The load voltages and source currents are balanced, sinusoidal, and in phase with respective phases. Moreover, these waveforms have reduced switching ripple components as compared to the waveforms of conventional scheme as shown in Fig. 5. Consequently, the filter currents injected at the load point have reduced harmonic ripple component in the proposed scheme. A total voltage of 800 V (400 V across each capacitor) is maintained at the common dc link of the VSIs, and it is sufficient to achieve improved compensation performance. For the comparison purpose, the percentage total harmonic distortion (THDs) level of source currents and load voltages in conventional and proposed UPQC schemes are given in Table II. It can be observed that the percentage THDs of source currents have been decreased in the proposed scheme. Further, Table III summarizes the details of filter inductances of passive filter components and total dc link voltage in both the schemes.

Proposed UPQC configuration is subjected to three phase voltage sag of 50% as shown in Fig. 7. Compensated load voltages maintained at the reference voltage are given in 7(b), whereas voltages injected by the series transformer are shown in 7(c). These results show the capability of proposed scheme to effectively compensate for voltage disturbances.

VI. CONCLUSIONS

This paper proposes a UPQC configuration employing an LCL input filter at the front end of shunt VSI to mitigate voltage and current related PQ problems. Proposed UPQC has provided better current and voltage compensation with improved ripple attenuation capability while using reduced passive components. Moreover, appropriate reduction in common dc link voltage is also achieved. With the simulation results, it is verified that the proposed UPQC configuration is able to provide improved compensation while utilizing reduced size passive components and dc link voltage as compared with the conventional UPQC.

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