Integrated Circuit Blocks for a DCSK Chaos Radio

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Abstract **- A proposal for an integrated digital communication system using a DCSK chaotic modulation scheme is presented. It is a point-to-point wireless system capable of supporting half-duplex real-time voice and low data rate communication (following ISDN standards) in a noisy indoor environment. Design strategies for the integrated realization of the most relevant building blocks of the chaotic modem are also included.**

I. INTRODUCTION

In the last years, there has been an increasing interest on the application of chaos for communication purposes [1]. Chaotic basis functions used as information carriers exhibit some distinctive features, which differentiate from the more conventional modulation approaches based on sinusoids. Since chaotic signals are aperiodic and wideband signals, they provide simultaneous *coding* and *spreading* of the information. Thus, chaotic modulation can be seen as a *spread spectrum* (SS) technique, for which the transmission band is larger than the minimum required to send the information [2]. Note however that spreading is not achieved by convolution with a pseudorandom sequence as in conventional SS approaches, but simply by taking advantage of the broadband spectrum of chaotic signals.

Different modulation schemes have been proposed for the exploitation of chaos to convey information [3]. Some of them are based on the ability to synthesize copies of the chaotic carrier signal at the receiver, by means of synchronization among chaotic oscillators. These modulation schemes are said to employ *coherent* detection to recover the information. In other cases, signal recovery is achieved by estimating one of the statistical attributes of the incoming chaotic signal previously encoded at the transmitter. Then, the demodulation process is said to rely on *noncoherent* signal detection.

Up to date, most of the experimental demonstrations of communications with chaos reported so far have employed wired links as transmission channel. Remarkably, some of these experiments (based on coherent detection techniques) have used monolithic realizations for the chaotic generators, thus confirming the possibility of engineering with chaos in a fully integrated manner [4][5]. However, few results have been reported on the application of chaos for wireless communications. Since this is the scenario where the spreading capability of chaotic modulation schemes can be fully exploited, the design of a chaos radio is largely suggested. This interest is also justified by the excellent performance predicted from some preliminary studies on chaotic radio transmission [3]. Exhaustive simulations including all the major nonideal effects of the RF link (floor noise, time-varying multipath channels and selective fading, among others) have shown that chaotic communications by Differential Chaos Shift Keying (DCSK) modulation (scheme proposed in [6] based on noncoherent detection for signal recovery) are able to guarantee signal transmission under very poor propagation conditions. Namely, it was found that the DCSK system is able to achieve a Bit Error Rate (BER) of 10^{-3} with only -3dB of Signal-to-Noise Ratio (SNR), and an efficiency (E_b/N_0 = 12.5dB) comparable with that exhibited by conventional sinusoid-based modulation schemes [3]. The purpose of this paper is to define the architecture of an integrated wireless transceiver using the DCSK modulation scheme, which serves as a proof-of-concept and allows to characterize the system performance under real-world conditions.

The paper is organized as follows. Section II presents the architecture of the DCSK chaos radio system, designed to provide point-to-point digital transmission of speech signals in a wireless indoor propagation channel. Section III gives a brief overview of the DCSK chaotic modulation scheme. Section IV shows a generic architecture for the monolithic realization of the DCSK modem, and identifies their basic building blocks. Sections V and VI deal with the electronic implementation of two essential blocks of the DCSK modem; the chaos generator and the delay block, respectively. Finally, Section VII gives some conclusions.

II. CHAOS-BASED RF TRANSCEIVER

Fig.1 shows the conceptual diagram of the proposed chaos-based RF transceiver. The prototype is a point-to-point wireless system capable of supporting half-duplex real-time voice and low data rate transmission (following ISDB standards) in a noisy indoor environment. One intended application domain for this proof-of concept system is a large manufacturing facility with roaming employees who must communicate intermittently for inventory or command purposes. A second application is for remote control of machines which represent

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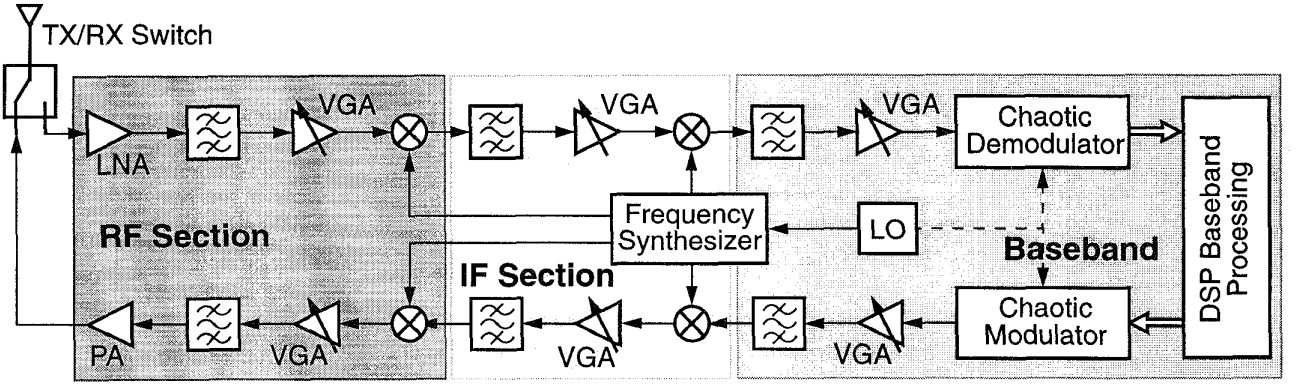

Fig. 1. Conceptual Diagram of a chaos-based transceiver system.

a strong source of interference for conventional narrowband wireless controllers (such as inductive welding equipment).

The system in Fig.1 uses a conventional heterodyne topology. The DSP baseband processing block performs the source and channel encoder/decoder operations, where the information signal is compressed, encrypted, and provided with error-correction capability by introducing algorithmic redundancy. This digital information is mapped to/from a set of analog chaotic basis function at the modulation/demodulation blocks, by means of the DCSK technique. At the RF section, the chaotic carriers are linearly translated in frequency to/from the RF transmission band. Finally, a TX/RX switch selects the transmission/reception mode of operation to allow bidirectional communication by time-division duplexing.

The transceiver is intended to conform the IEEE 802.11 standard "Direct Sequence Physical Layer". The ISM (Industrial, Scientific and Medical) transmission band of 2400MHz to 2483.5MHz has been selected because of its almost universal availability. Block requirements for the different blocks of the transceiver as been derived as to satisfy a maximum range of about 50m in a metalworking building. Target performances of the RF/IF sections are -102dBm of receiver sensitivity, maximum output power of +20dBm, and a spurious free dynamic range of 80dB. On the other hand, a data rate R of 64×10^3 bps (bits per second) is specified, which is the standard speed of transmission through 'B' channels assigned to ISDN end-users for voice or data communication.

Clearly, the major difference of the architecture in Fig.1 as compared to more conventional digital communication setups, comes from the chaotic modulation/demodulation block. In the following sections, its functional description, as well as a proposed integrated solution, will be given.

III. DIFFERENTIAL CHAOS SHIFT KEYING

Fig.2 shows the conceptual diagram of the binary DCSK chaotic modulation/demodulation scheme used in the transceiver of Fig.1. At the modulator (Fig.2(a)) every incoming binary information signal from the DSP baseband block is mapped into two sample functions of duration $T = (2R)^{-1}$, which are transmitted one after the other. The first sample function, provided by a chaos generator, acts as a reference signal while

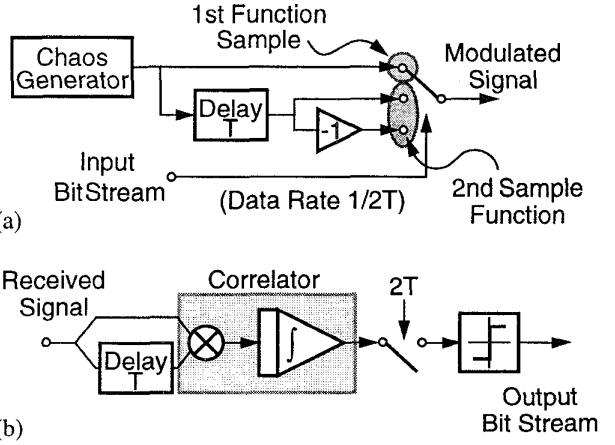

Fig. 2. Conceptual Diagram of the DCSK modulation scheme: (a) Modulator; (b) Demodulator.

the second one conveys the information. Depending on whether the information symbol is '0' or '1', the second sample function is an inverted or non-inverted replica of the reference signal.

At the demodulator (Fig.2(b)), the information is recovered by noncoherent detection, through the estimation of the crosscorrelation value of the incoming signal with a delayed by T version of itself. This estimation is realized on a finite temporal basis of duration T. The output of the correlator is sampled at decision instants separated by $2T$. Such instants are chosen so that, on the temporal basis of the correlator just before sampling, the received signal corresponds to the second sample function of the transmitted signal, and the delayed copy corresponds to the associated reference. According to the sign of the sampled output of the correlator, a level comparator decides the information symbol that was transmitted. A large positive (negative) autocorrelation indicates that a symbol '1' (symbol '0') has been received.

IV. BASEBAND DCSK MODEM

Fig.3 shows the block diagram associated to the DCSK concept of Fig.2. At the modulator, a band limited continuous-time chaos generator is used to provide the reference chaotic

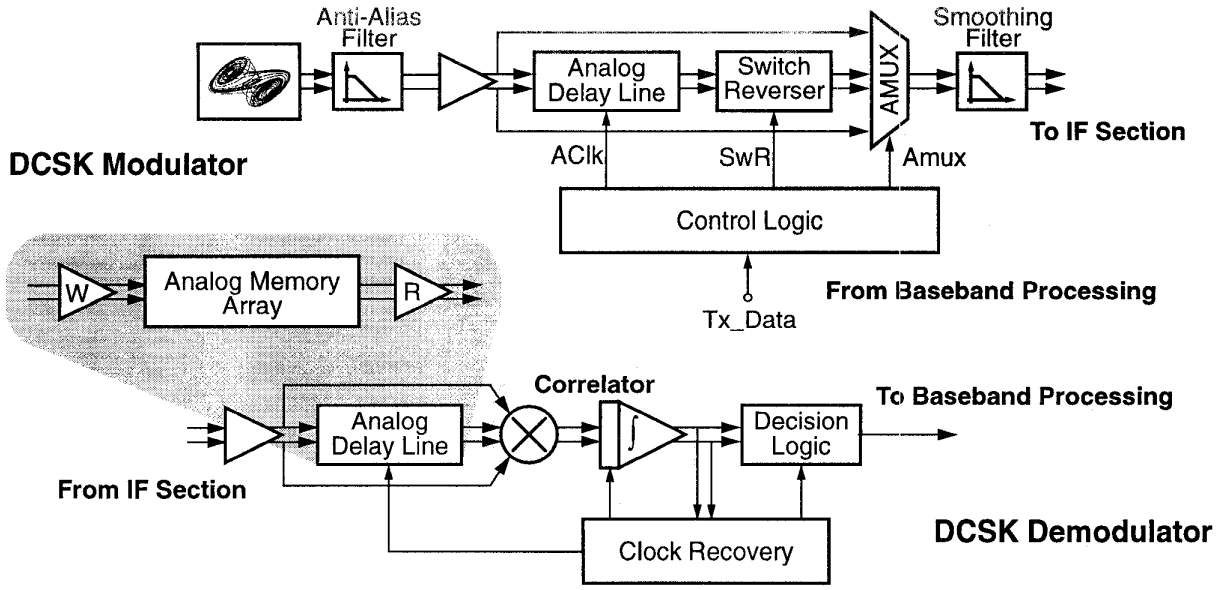

Fig. 3. Block Diagram of the DCSK modulation scheme.

sample function of the DCSK scheme. A sampled-data analog memory array solution is used to implement the delay block of Fig.2. This block, driven by a sample and hold amplifier, operates alternatively in read/write mode, each phase with T seconds of duration. Internal processing of this analog delay line is fully differential to increase the dynamic range of the circuit. At the same time, this allows to synthesize both the inverted or non-inverted replica of the reference signal (according to the information symbol) by a simple switch reverser arrangement at the output. The modulated signal is obtained by multiplexing (and then filtering) the signals coming from the switch reverser and the sample and hold amplifier at the input of the analog delay line.

An important consideration of the design is the number N of memory cells included in the analog delay line. Bearing in mind, that signal recovery at the receiver is achieved by estimating the autocorrelation value of the incoming signal during a time interval T (defined by the data transmission rate), the larger the number of memory cells, the lower the variance of the symbol estimation, and hence, the lower the BER of the digital transmission. However, as the number of memory cells grows the speed requirements on the internal circuitry of the delay block, which operates at a sampling frequency of $1/(NT)$, become more severe. Preliminary simulations have shown that an acceptable trade-off value for N is 200 which, assuming a data rate of 64kbps, gives a sampling frequency of the analog delay line of 25.6MHz.

The DCSK demodulator shown in Fig.3 is also based on the analog delay line previously described. In this case, the read and write phases of each memory cell occur consecutively, so that the inputs to the correlator (consisting of a multiplier cell and discrete-time analog integrator) correspond to samples of the signal from the IF section separated exactly by T seconds. According to the sign of the integrator output at the correlator, a decision logic unit recovers the transmitted information symbol.

An essential element of the demodulator is the clock recovery circuitry, which must determine the precise sampling time instants of the decision unit, as well as the timing diagram of the analog delay line and the integrator. Clearly, the proper time to sample the output of the correlator and decide the transmitted symbol is at the peak of the autocorrelation function, which corresponds to the end of the time interval of duration T where the transmitted sample functions (reference and delayed copy) completely overlap. However, in the presence of noise, the identification of the peak value of the integrator output is difficult, and an early-late gate symbol synchronization approach must be considered [7]. Additionally, special preamble sequences should be transmitted, previous to sending the information content, in order to speed up the time synchronization of the demodulator. A convenient preamble consists on an alternating sequence of '0' and '1'.

Critical blocks for the implementation of the DCSK modem are the chaos generator and the analog delay line. In the following, considerations for the IC design of such blocks are briefly reviwed.

V. CHAOS GENERATOR

The monolithic design of the DCSK modem in Fig.3 largely relies on the availability of robust chaotic oscillators with reproducible and easily controllable behavior. [8] gives a systematic procedure for the design of continuous-time chaos generators following a top-down approach. It starts from a general topology able to synthesize an infinite number of chaotic attractors (the Lur'e form depicted in Fig.4) and, given a particular target behavior, identifies which architecture provides the best trade-off between complexity and performance from an IC perspective. The resulting mathematical model is then mapped onto a circuit schematic and the influence of the hardware non-idealities are analyzed. Then, the different block requirements are extracted, and an integrated solution

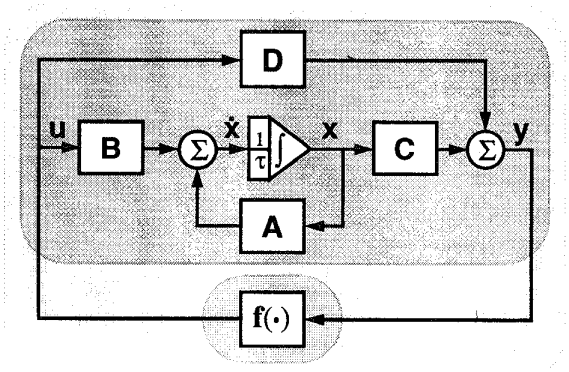

Fig. 4. Multidimensional Luré form.

obtained, taking into account the desired operating frequency and the required tunability range of the chaotic oscillator. Following this approach, authors in [8] have developed a CMOS prototype for a chaos generator with low-pass spectrum characteristics and proved the suitability of the chip to implement chaotic modulation schemes by coherent detection [5].

VI. ANALOG DELAY LINE

As shown in Fig.3, it comprises two OTA's (labeled 'W' and 'R' in Fig.3) and a fully-differential storage capacitor array [9]. The write 'W' OTA is used to transfer the charge from a sampling capacitor at the input of the delay line to the selected memory cell of the array; while the read 'R' OTA is used to retrieve the charge stored from the selected memory location and convert it to a voltage proportional to the read out charge. The analog memory array consists of N storage locations, whose selection is accomplished by closing the appropriate MOS switches. Since the estimated value for N is 200, a linear-type structure of the capacitor array would result in a large parasitic capacitance from the unselected storage locations, thus placing stringent demands on the OTA's to achieve fast access time (bear in mind that the sampling frequency of the analog delay line is 25.6MHz for $N = 200$). A better strategy is to adopt a matrix-type arquitecture, as shown in Fig.5. The storage cells are broken into sub-arrays, so that only the active sub-array is connected to the OTA at any one time. Then, the parasitics seen by the OTA can be substantially reduced. Besides the storage cells (their schematic is shown at the inset of Fig.5) the analog memory array also requires read and write row multiplexers and address generators for cell access.

VII. CONCLUSIONS

A proposal for an integrated digital communication system using a DCSK chaotic modulation scheme has been presented. The design of the baseband DCSK modem is currently ongoing.

Acknowledgments

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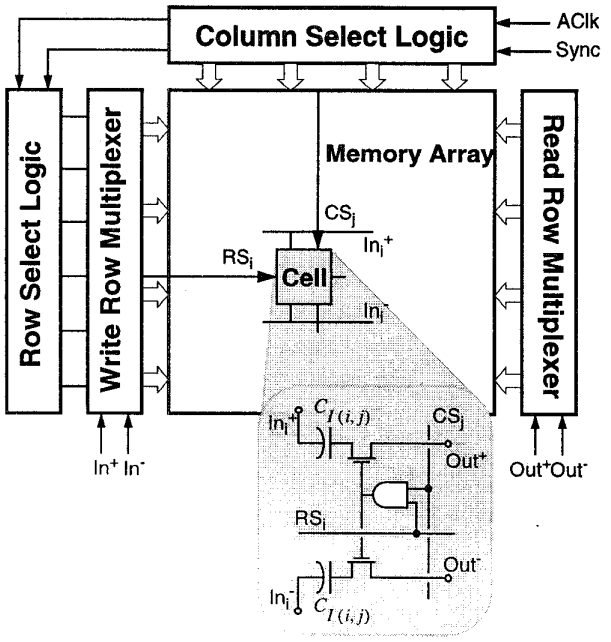

Fig. 5. Block diagram of the analog memory array.

References

[1] M. Hasler, "Engineering Chaos for Encryption and Broadband Communication". *Phil. Trans. R. Soc. Lond.*, series A, Vol. 353, pp. 115-126, Oct. 1995.

[2] R. C. Dixon, "*Spread Spectrum Systems with Commercial Applications*". John Wiley, New York, 1994.

[3] G. Kolumbán, M. P. Kennedy and L. O. Chua, "The Role of Synchronization in Digital Communication Using Chaos. Part II: Coherent and Noncoherent Chaos Modulation Schemes", to appear in *IEEE Trans. on Circuits and Systems.*

[4] M. Delgado-Restituto, R. López-Ahumada and A. Rodríguez-Vázquez, "Secure Communications using CMOS Current-Mode Sampled-Data Circuits", in *Proc. 3rd Int. Workshop on Nonlinear Dynamics of Electronic Systems*, pp. 241-244, Jul.1995.

[5] M. Delgado-Restituto, M. Liñán, J. Ceballos and A. Rodríguez-Vázquez, "Bifurcations and Synchronization using an Integrated Programmable Chaotic Circuit", *Int. Jour. Bifurcations and Chaos*, Vol. 7, No. 4, Oct. 1997.

[6] G. Kolumbán, B. Vizvári, W. Schwarz and A. Abel, "Differential Chaos Shift Keying: A Robust Coding for Chaotic Communication", in *Proc. 4th Int. Workshop on Nonlinear Dynamics of Electronic Systems*, pp. 87-92, Jun.1996.

[7] J. G. Proakis and M. Salehi, "*Communication Systems Engineering*". Prentice Hall, Englewood Cliffs (NJ), 1994.

[8] M. Delgado-Restituto and A. Rodríguez-Vázquez, "Design Considerations for Integrated Continuous-Time Chaotic Oscillators", accepted for publication in *IEEE Trans. on Circuits and Systems.*

[9] K. A. Nishimura and P. R. Gray, "A Monolithic Analog Video Comb Filter in 1.2-μm CMOS". *IEEE J. of Solid-State Circuits*, Vol. 28, No. 12, pp. 1331-1339, Dec. 1993.