In vivo measurements with a 64-channel extracellular neural recording integrated circuit

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***Abstract*—This paper presents *in vivo* measurements obtained from an implantable 64-channel neural recording Application Specific Integrated Circuit (ASIC) developed at IMSE and gives details of the computer interface used for real-time data acquisition. This interface connects the ASIC to a conventional 2.0 USB port by means of a Field Programmable Gate Array (FPGA). Communications are bidirectional and employ custom protocols both for delivering commands to the ASIC and for recording neural information under different channel selection and operation modes. The link is controlled by a user-friendly programming interface written in C++ which includes a built-in routine to efficiently index and store the captured data. Mesurements demonstrate the suitability of the ASIC for capturing local field and action potentials with two different microelectrode array platforms.**

I. Introduction

In recent years, advances in technology have made it possible to monitor bioelectric brain activity using devices physically implanted in the patient [1]–[3]. Thanks to the use of electrode arrays with inter-electrode separation in the order of tens of microns and bandwidths in the kH range, such devices offer much higher levels of spatio-temporal detail than those achievable with electroencephalography (EEG). This increase in resolution is allowing specialists to prescribe more area-specific treatment and even develop new therapeutic procedures. Implanted closed loop neuromodulation systems, for example, can alleviate the adverse effects of certain illnesses, such as the motor dysfunction caused by Parkinson's disease, or predict and counteract epileptic seizures [4]. Further, efficient monitoring of brain signals from implanted devices is a key factor in the development of brain-machine interfaces in which appropriately instrumented objects can be controlled exclusively by a person's thoughts, thus improving the quality of life of patients with severe mobility impairments [5].

In this paper, *in vivo* measurements obtained from an implantable 64-channel neural recording system prototype developed at IMSE are presented. The most salient features of this prototype, as well as its implementation details, were briefly described in [6]. Herein, attention is paid on the bidirectional wire line interface used to communicate the prototype with a computer in order to configure the recording system and store the acquired neural information. Although the prototype also includes modules for wireless data and power transfer,

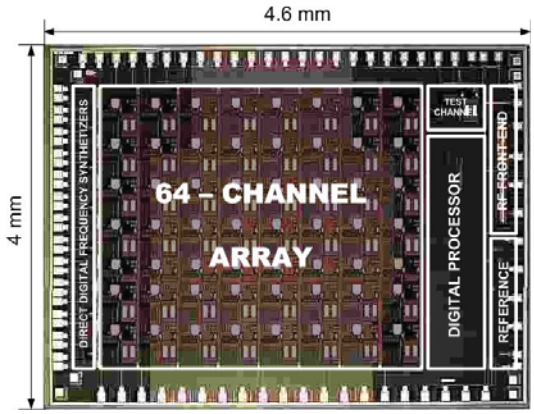

Figure 1. Microphotograph of the multichannel neural recording array prototype.

in the presented experiments, we have considered a wireline approach as a first step towards assessing the full functionality of the prototype. Such wireline interface has been implemented by means of a Field Programmable Gate Array (FPGA) and uses a conventional 2.0 USB port to communicate with the host computer.

For the sake of completeness, a short review of the fabricated 64-channel neural recording system is presented in Section II and, afterward, a description of the experimental setup for the *in vivo* measurements is given in Section III. Then, the FPGA-based interface is described in Section IV including details of the ASIC programming hardware and the data recording module. Section V presents some of the *in vivo* neural recording measurements using animal models obtained in the Institute of Bioengineering in Elche (Spain). They consist of local field potentials (LFPs) captured with a sub-dural microelectrode array and action potentials (APs) recorded with an intracortical Utah array. Finally, Section VI ends the paper with some conclusions.

II. Neural Recording System

Fig. 1 shows a microphotograph of the 64-channel neural recording system, fabricated in a 1.2-V 130nm (6M2P) standard CMOS technology. Each channel comprises an analog front-end with programmable gain and tunable bandpass characteristics for the acquisition and conditioning of neural signals; a local SAR-based analog-to-digital converter (ADC);

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a digital module for the detection and compression of action potentials; and means for temporarily storing the aforementioned information. All these in-channel functions, together with an internal pad for flip-chip connection, are integrated in an area of $0.16mm^2$. A dedicated digital processor collects and classifies the information gathered by the channels before sending it out either through an inductive link or by means of a wireline connection, as presented in this paper. Additionally, the processor transfers parameters to the channels, checks for digital consistency and provides internal timing references from a single 4MHz master clock. This clock can be extracted from the carrier of the inductive link or, as done in the presented experiments, introduced through a dedicated pin.

Besides a configuration phase in which the different channels are parametrized, the recording system offers three operation modes. In one case, denoted as calibration mode, the system self-calibrates so that the recording bandwidth of every selected channel is tuned to the desired frequency range and the gain of their front-ends is adjusted to maximally cover the input dynamic range of the local ADC. The second operation mode, denoted as signal tracking mode, is intended to stream out uncompressed raw data from the selected channels. Finally, in the last mode, denoted as feature extraction mode, the digital compression modules of the selected channels are activated and the detected APs are on-the-fly approximated by piecewise-linear (PWL) representations. For each selected channel, the AP detection threshold is adaptively updated according to the noise floor of the captured signal. In this mode, a channel remains idle and, hence, it does not transmit any information, as long as no action potential is detected. Therefore, activity in this mode is event-driven thus favoring the reduction of the system power consumption.

The input/output data frames used for the configuration of the channels and the recording of information for the different operation modes were presented in [6].

In this paper, we have focused on the signal tracking mode, under two possible recording configurations:

1) Tracking of the whole array (64 channels) at a throughput rate per channel of 4kS/s. Although this configuration can be also used to detect the presence of spikes, it is mainly used for the recording of LFPs at which the high-pass and low-pass corners of the bandpass characteristic in every channel are set to the lowest frequencies possible (15Hz and 5.2kHz, respectively, in this prototype). If required, the low-pass corner of the bandpass characteristics can be digitally move off-chip to lower frequencies after downsampling and FIR filtering the recorded streams. In the reported experiments, no extra filtering is applied.
2) Tracking per row/column (8 channels) at a throughput rate per channel of 30kS/s. This is the default sampling rate in the AP feature extraction mode (bandpass characteristics set between 200Hz and 7kHz), but it can also be used in tracking mode to fully appreciate the waveform details of the recorded signals. No additional off-chip filtering is required.

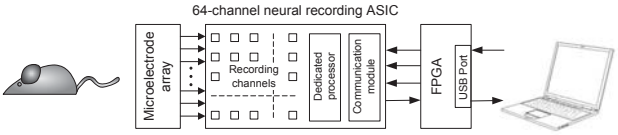

Figure 2. Measurement setup

III. Measurement Setup

Fig. 2 shows the schematic diagram of the measurement setup used for *in vivo* neural recording. Two different types of microelectrode arrays (MEAs) for neural recording were used. In one case, a flexible sub-dural microelectrode array (Multi Channel Systems MCS GmbH) with TiN electrodes separated by 300μm (diameter 30μm) placed on a polymide substrate was used. The signals captured by the microelectrodes were transferred to the 64-channel neural recording system by means of flat ribbon cables connected between the MEA adapter (ADPT-FM-36, MCS GmbH) and the ASIC through row precision sockets from Samtec. In the second case, the MEA was a Utah array with an ICS-96 connector (Blackrock Microsystems LLC). A custom adapter was designed for arranging the pin distributions of the ICS-96 connector (only, banks A and C) so that the same connection strategy employed with the flexible MEA could be reused.

A Field Programmable Gate Array (Nexys™2 Spartan-3E FPGA Board by Digilent) was used to communicate the 64-channel neural recording ASIC with a host computer through a conventional 2.0 USB port. A user interface developed in C++ was designed to control the whole measurement setup. This interface compiles the Digilent DEPP Dynamic Link Library [7] to access the USB driver. The communications between the ASIC and the FPGA only need two downward connections, for the command line and write enable signals, and one upward connection, for the transfer of the neural information recorded and processed by the ASIC. Additionally, a 4MHz master clock is transferred for timing purposes.

All experimental procedures were performed in conformance to the directive 2010/63/EU of the European Parliament and of the Council, and the RD 53/2013 Spanish regulation on the protection of animals use for scientific purposes and approved by the Miguel Hernandez University Committee for Animal use in Laboratory. Animal models were adult male Long Evans rats.

IV. FPGA Interface

The purpose of the FPGA board is to control and transfer the data acquired by the 64-channel neural recording ASIC. The FPGA board, programmed with the Xilinx ISE Design Suite, implements two major blocks: (i) a control module in charge of sending configuration commands to the selected channels of the ASIC and (ii) a data recording module which temporarily stores in internal RAMs the data received from the ASIC and, afterward, delivers the information through the USB port. Both modules make use of a USB interface which implements the bidirectional communication between the FPGA board and the USB port. This interface consists of a state machine with 8-

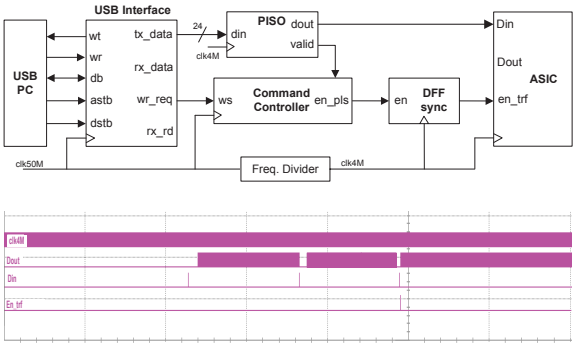

Figure 3. Block and timing of the proposed controller unit.

bits bidirectional data bus, five control signals and one clock signal (40MHz).

A. Logic Control Module

The logic control module, shown at the top of Fig. 3, enables the external operator to configure the channels of the ASIC, through the Din serial port, at instances of the control signal en_trf. As described in [6], all configuration commands start with a 5-bits preamble, followed by a payload of 14-bits and a 5-bits of Cyclic Redundancy Check (CRC).

Every time the USB interface detects a write request (wr_req is active) from the host computer it begins packing bits in word frames. These frames are then fed into a synchronous parallel-input serial-output (PISO) register for serialization. Signals inside the FPGA have to be carefully synchronized in order to avoid time out errors and/or incomplete command transfers. To overcome these issues, an internal controller, clocked at 40MHz, triggers the control signal en_trf only when the data stored in the PISO register is valid. This control signal en_trf, which defines the data transfer window to the ASIC, remains active as long as the content of the PISO resister is being dumped to the ASIC. The 4MHz master clock of the ASIC is derived by dividing the 50MHz FPGA clock. The output stream of the PISO register and the control signal en_trf are aligned to the master clock of the ASIC.

The start-up of the recording system involves three commands, as illustrated in the bottom plot of Fig. 3. The first command is intended to define the bandpass of the 64 channels included in the ASIC. Depending on the logic value of a flag comprissed in the command stream, this can be done either by directly defining the programming words of the highpass and lowpass corners of the channel' filters or by running a self-calibration process over the whole array. In this latter case, aimed to counteract on-chip PVT variations, a tuning mechanism based on digital frequency synthesis is enabled to automatically adjusting the aforementioned programming words to the desired filter pole values. The second command is intended to calibrate the voltage gain of the channels to the largest value possible, avoiding the saturation of the embedded data converter. Once completed this operation, a third command selects the channels to be recorded and the acquisition commences.

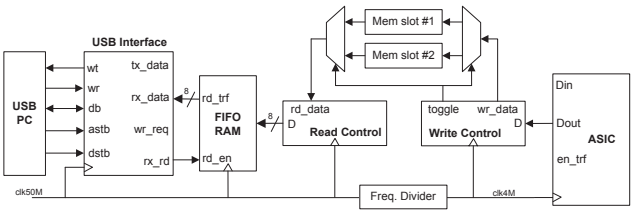

Figure 4. Block diagram of the data recording module.

B. Data Recording Module

The data recording module, shown in Fig. 4, enables to transfer the information provided by the selected channels of the ASIC to a host computer. For the two experiments under signal tracking mode described in Sec. II, output data frames coming from the ASIC have 85-bits length. They consist of an 8-bits preamble, a 72-bits information packet, and a 5-bits CRC checksum. Besides a code for the operation mode (2-bits), the information packet contains an identifier (6-bits) of the column/row in the ASIC which is currently transmitting information and the digitized sampled data sent out by the corresponding channels (8-bits per channel streamed from MSB to LSB). Depending on whether the identifier remains static or runs cyclically over the 8 columns/rows of the array, the ASIC delivers the recordings from 8 cells at a throughput rate per channel of 30kS/s or sweeps the whole array at a throughput rate per channel of 4kS/s.

A write control unit, synchronized to the 4MHz master clock, identifies and alternatively dumps the serial output frames of the ASIC into two memory slots which temporarily store the neural information. Every time a new frame is read and stored, the write control unit changes the state of the control signal, toggle. This same signal is used by a read control unit, clocked at 50MHz, to retrieve the stored information from that memory slot which is not under read operation. Hence, while one of the memories is being written the other is being read, and vice versa. Because of the different clocks used by the read and write units, no information is lost. Additionally, the read control unit transfers the retrieved information to a first-input first-output (FIFO) memory in parallel slots of 8-bits. Data are transferred from this memory to the USB port during the time intervals allowed by the protocol.

V. In vivo results

Fig. 5 shows 16 of the recordings captured by the ASIC when operated in signal tracking mode with the column scanning option enabled (64 channels tracked at a throughput rate per channel of 4kS/s). The flexible sub-dural microelectrode array described in Sec. III was used in this experiment. Although the experiment lasted for several hours, only a 10s interval is shown in Fig. 5; no substantial differences were appreciated in the course of the measurement, not among the channels. The average power consumption of the ASIC was 241μW which, according to post-layout simulations, splits into some 194μW for the recording channels and about 47μW for the embedded digital processor and the communication module together (see Fig. 2).

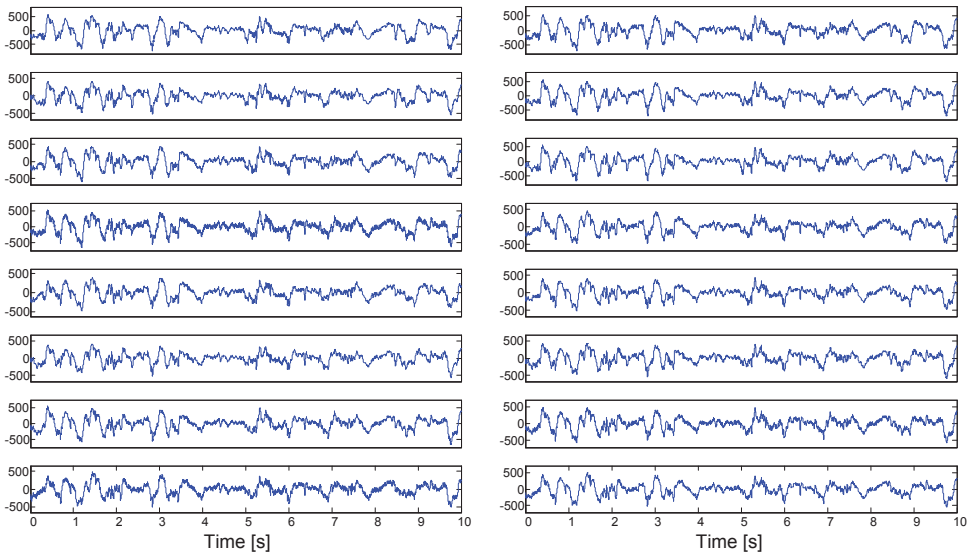

Figure 5. LFP activity recorded from 16 channels in the *in-vivo* test performed with the neural recording array attached to a flexible array of MultiChannel Systems (vertical axis in μV).

Fig. 6 shows the 8 recordings captured by the ASIC when operated in signal tracking mode from a single column of the channel array (8 channels tracked at a throughput rate per channel of 30kS/s). In this case, the Utah array was employed in the *in vivo* measurement. As can be observed in Fig. 6, isolated action potentials and bursts of spikes are clearly noticeable in the 30ms recording. As in the previous case, no substantial difference from the shown performance was observed along the experiment. In this case, the average power consumption of the ASIC was 69μW which splits into some 24μW for the recording channels and about 45μW for the digital periphery. It is worth observing no major difference on the power consumption of the digital circuitry was detected as compared to the previous experiment. This is because the lower number of channels is counterbalanced by the higher data rate.

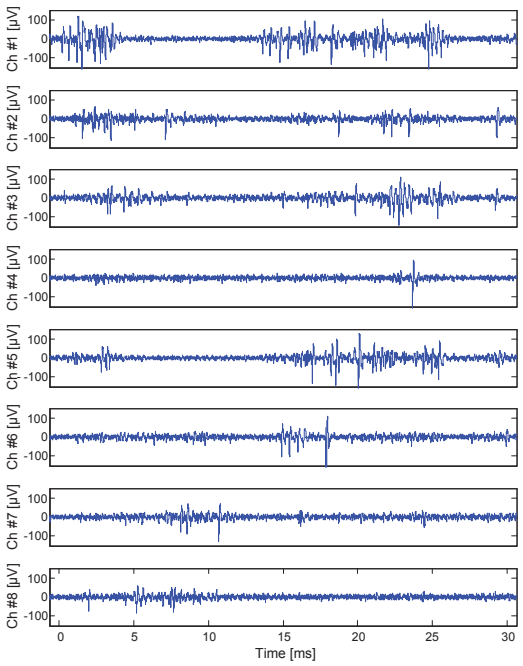

Figure 6. Neural spike activity recorded from 8 channels in the *in-vivo* test performed with the neural recording array attached to a Utah array (vertical axis in μV).

VI. Conclusions

This paper presents *in vivo* measurements obtained from an implantable 64-channel neural recording system prototype developed at IMSE. Details are given on the FPGA interface used to communicate the ASIC to a host computer. The implemented system is capable of acquiring online data from various channels for unlimited amount of time and it is found suitable both for sub-dural and intracortical recordings.

Acknowledgments

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