# Mixed-signal quadratic operators for the feature extraction of neural signals

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***Abstract*—This paper presents design principles for reusing charge-redistribution SAR ADCs as digital multipliers. This is illustrated with an 8-b fully-differential rail-to-rail SAR ADC/multiplier, designed in a 180 nm HV CMOS technology. This reconfigurability property can be exploited for the extraction of product-related features in neural signals, such as energy content, or for the discrimination of spikes using the Teager operator.**

## I. Introduction

Closed-loop neural implants are a promising solution for the treatment of neurological diseases [1], [2], as well as for the implementation of sensori-motor brain-machine interfaces [3]. Neural signals captured by the implant are internally processed and, based on the analysis, stimulation patterns are triggered either for ameliorating the impact of the disease (e.g., by stopping uncontrolled epileptic seizures [4]) or for restoring lost senses after a neural injury. Signal processing in neural implants should, on the one hand, reduce dimensionality and extract features able to provide clinically relevant information [5], [6] and, on the other, exhibit low power consumptions to not exhaust the presumably short energy resources available.

Quadratic operators are often used in the calculation of neural features. For instance, the accumulated energy in spectral bands, the variance of amplitude distributions, the auto- or cross-correlation of neural recordings or the calculation of nonlinear interdependences are measures typically used for the univariate or multivariate analysis of local field potentials and EEGs [7]. Similarly, the Teager operator, also called Nonlinear Energy Operator (NEO), which also relies on the multiplication of neural samples, is an effective procedure for the detection of neural spikes [8]. These quadratic operators can be implemented in analogue domain by exploiting translinear principles [9], or in digital domain at the price of an increased computation complexity due to the use of digital multipliers [10]. Indeed, the use of look-up tables after data rounding has been proposed to alleviate the computational burden of binary multiplications [11].

Herein we propose an alternative mixed-signal approach for the multiplication of digitized neural samples. The design principle is based on reusing the analog-to-digital conversion process (assuming charge-redistribution SAR ADCs) to also compute quadratic terms. In doing so, the presented approach requires little extra hardware thus leading to area-efficient solutions. The paper is organized as follows. Section II describes the operations of voltage loading and voltage scaling in capacitor arrays which are behind the mixed-signal multiplication concept. Then, Section III presents an 8-b differential SAR ADC/multiplier based on those operations. Section IV shows two examples of quadratic operator implementations using the described circuit. After illustrating in Section V the simulated performance of the ADC/multiplier, Section VI concludes the paper.

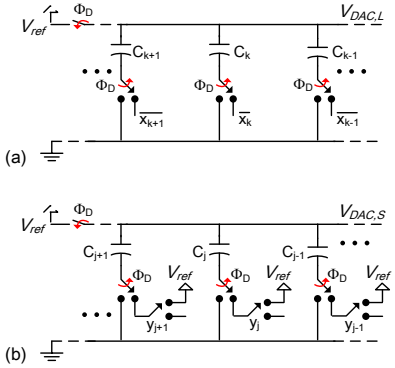


Figure 1. Voltage loading (a) and voltage scaling (b) processes.

## II. Operations in capacitor arrays

Mixed-signal multiplication of two digital vectors with a charge-redistribution ADC can be accomplished by generating a voltage proportional to the product of the two multiplicands in the capacitor array of the ADC and then converting that voltage with a conventional binary search algorithm. The synthesis of the product voltage can be easily implemented, without relying to any external block, by means of two simple digital-to-analog operations in the capacitor array. Such operations, denoted as voltage loading and voltage scaling, are applied sequentially and require one single clock cycle each.

Voltage loading consists on programming the switching nodes of the capacitor array according to the bits of a digital word $\mathbf{X} = \{x_k\}$. The operation is illustrated in Fig. 1(a), where bottom-plate programming is assumed (of course, other configurations are also possible). When $\Phi_D = 1$, the top plates of the capacitors in the array are all connected to $V_{ref}$, whereas the bottom plates are connected to ground or $V_{ref}$, depending on the $x_k$ values. Afterwards, in the holding phase ($\Phi_D = 0$), the top plates of the capacitors are disconnected from $V_{ref}$, the bottom plates are connected to ground, and the charge is redistributed in the array to

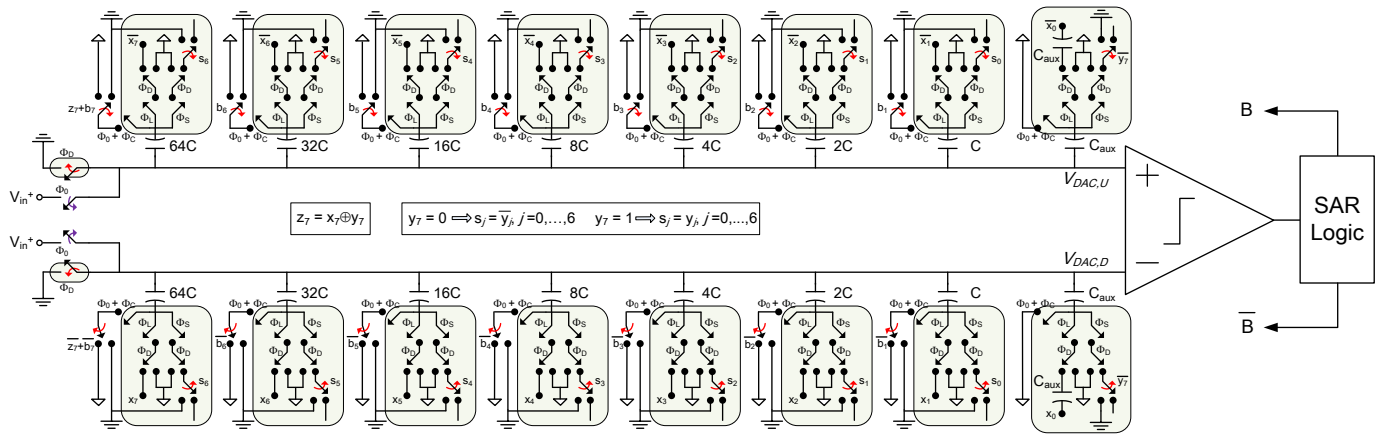


Figure 2. SAR ADC multiplier architecture.

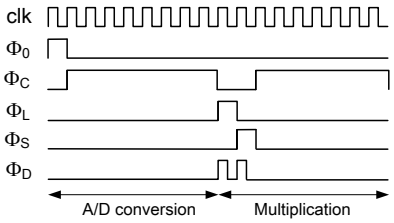


Figure 3. Timing diagram.

generate $V_{DAC,L} = V_{ref} \cdot \sum x_k \cdot C_k/C_T$, where $C_T$ is the total capacitance of the array.

Once the voltage $V_{DAC,L}$ has been stored in the capacitor array, the next operation is to scale that voltage according to a second digital word $\mathbf{Y} = \{y_j\}$. This is done by selectively discharging part of the capacitors in the array. Fig. 1(b) illustrates the procedure. When $\Phi_D = 1$, the top plates of the capacitors are all connected to $V_{ref}$. Contrarily, the bottom plates are only connected to $V_{ref}$ if the associated bit $y_j = 0$ (capacitor $C_j$ discharges), otherwise the bottom plate is left open (capacitor $C_j$ preserves the previously stored charge). In the holding phase ($\Phi_D = 0$), all the bottom plates are connected to ground, the top plates are disconnected from $V_{ref}$, and again the charge is redistributed through the array. This gives rise to a voltage $V_{DAC,S} = V_{DAC,L} \cdot \sum y_j \cdot C_j/C_T$ which, assuming the capacitors of the array are binary weighted, represents an analogue version of the dot product $\mathbf{Z} = \mathbf{X} \cdot \mathbf{Y}$ normalized between ground and $V_{ref}$. As metioned, the actual vector $\mathbf{Z}$ can be obtained after a conventional A/D conversion process.

It is worth observing the above operations follow similar principles as the Multiplying SAR ADC proposed in [12]. However in this case, both multiplicands are binary words what open vistas for the implementation of quadratic operators with digital vectors, as will be shown in Section IV.

## III. SAR ADC MULTIPLIER

Figure 2 shows a possible implementation of the mixed-signal domain multiplier concept presented in Sec. II. The architecture is based on the monotonic capacitor switching procedure described in [13], although the strategy could be likewise applied to other switching schemes. The multiplier is built upon an 8-b fully-differential SAR ADC with two binary weighted arrays of capacitors which are constructed by shunting replicas of a unit instance with capacitance $C$. In total there are $2^8 + 2$ unit capacitors, including the four auxiliary capacitors ($C_{aux} = C$) employed for loading the first multiplicand. The shaded switch arrangements in Fig. 2 and the associated driving circuitry constitute the extra hardware required for adding multiplication functionality to the ADC. The circuit has three input ports: one analog, for data conversion; and two digital, for multiplication. Fig. 3 shows the timing diagram of the circuit when both operations are chained.

The analog port is used for sampling the differential input voltage $V_{in}$ in the capacitor arrays. During phase $\Phi_0$, the top plates of the capacitors arrays are connected to terminals $V_{in}^+$ and $V_{in}^-$, respectively, while the bottom plates of all capacitors, no matter the array, are connected to $V_{ref}$. After sampling, the conversion process starts ($\Phi_C = 1$) and the comparator decides the most significant bit, $b_7$, without switching any capacitor. At the next clock cycle, the largest capacitor of the array with higher potential (upper array if $b_7 = 1$; bottom array, otherwise) is switched to ground while the equivalent capacitor in the other array remains connected to $V_{ref}$. After a new comparison, bit $b_6$ is decided. This process repeats until the LSB is obtained. Including the sampling phase, the overall procedure requires 9 clock cycles.

Digital ports are used for parallel uploading the words $\mathbf{X}$ and $\mathbf{Y}$ to be multiplied. Following, the concepts presented in Sec. II, this is done in two steps, one for loading $\mathbf{X}$ and the other for scaling the charge stored in the capacitor arrays according to the bits of $\mathbf{Y}$. Once the proper $V_{DAC}$ value is generated, a conversion process finally obtains $\mathbf{Z} = \mathbf{X} \cdot \mathbf{Y}$. The loading and scaling procedures are illustrated in Fig. 4.

During the first half ($\Phi_D = 1$) of the $\mathbf{X}$ loading phase ($\Phi_L = 1$), the top plates of the capacitors in both arrays are shorted to ground and the bottom plates are connected to the bits of $\overline{\mathbf{X}}$ (top array) or the bits of $\mathbf{X}$ (bottom array), as illustrated in Fig. 4(a). Note that the auxiliary capacitors in both arrays are arranged so as to provide an equivalent capacitance $C/2$. Afterwards, when $\Phi_D = 0$ [see Fig. 4(b)], all the bottom plates are connected to $V_{ref}$, the top plate switches are open, and charge is redistributed.

Taking advantage of the differential circuit structure and

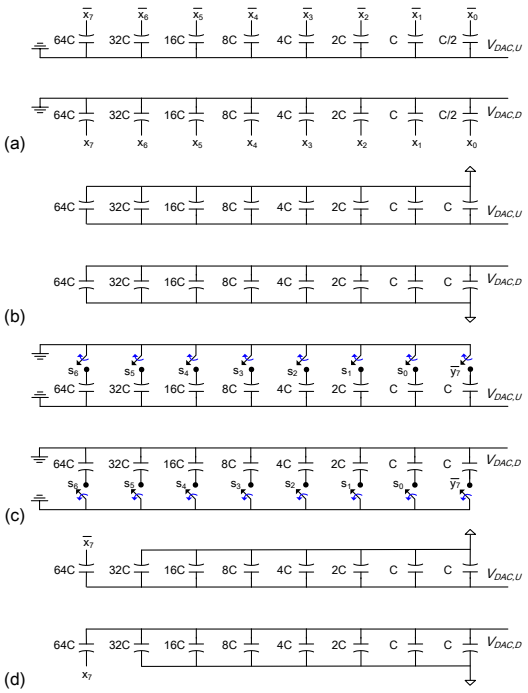


Figure 4. Specific steps for the multiplication process.

the fact that the MSB of $\mathbf{Z}$ can be easily derived beforehand as $z_7 = x_7 \oplus y_7$, the scaling by $\mathbf{Y}$ phase ($\Phi_S = 1$) is accomplished in such a way that only the remaining bits of $\mathbf{Z}$ are resolved, thus saving a conversion step. To that end, the MSB and the remaining bits of $\mathbf{Y}$ are handled differently. As shown in Fig. 4(c), when $\Phi_D = 1$, the top plates of the capacitors are shorted to ground and the charge stored in the auxiliary capacitors are either discharged (case $y_7 = 1$) or preserved (case $y_7 = 0$). Similarly, bits $y_j,\ j = 0, ..., 6$, are used to cancel or retain the voltages stored in the capacitors of the binary weighted arrays. For $y_7 = 1$, the charge in capacitor $C_j = 2^j C$ is preserved if the associated bit $y_j = 1$; otherwise, if $y_j = 0$, capacitor $C_j$ is discharged. For $y_7 = 0$, the opposite occurs, i.e., $y_j = 1$ implies discharging and $y_j = 0$ implies preserving. At the next step, when $\Phi_D = 0$, the charge is redistributed again by restoring the same configuration in Fig. 4(b). Afterwards, a conversion process begins assuming that the MSB is already known. This is illustrated in Fig. 4(d) in which the largest capacitors of the top and bottom arrays are connected to $\overline{x_7}$ or $x_7$, respectively. After 7 conversion steps, the remaining 7 LSBs of vector $\mathbf{Z}$ are obtained as follows: if $y_7 = 1$, then $z_j = b_j,\ j = 0, ..., 6$; otherwise $z_j = \overline{b_j}$.

## IV. Quadratic Operators

### A. Running average energy operator

The running average energy of a time series $\{s(n)\}$ is obtained by cumulatively summing the instantaneous energy of that signal according to [7]

$$E_D(k) = \frac{1}{N} \cdot U_D(k) = \frac{1}{N} \sum_{n=1+(k-1)(N-D)}^{k(N-D)+D} s^2(n) \qquad (1)$$

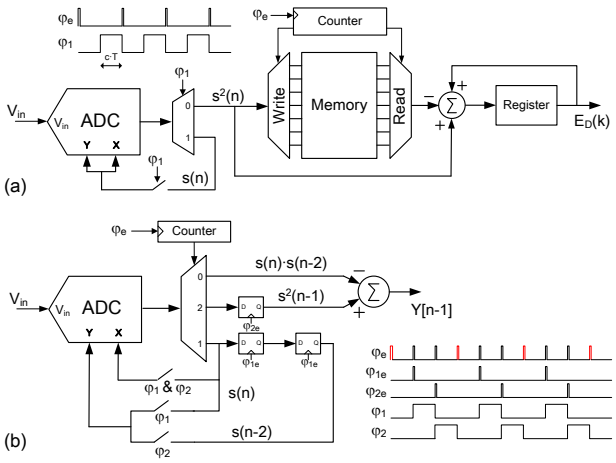


Figure 5. Implementation of (a) running average energy and (b) nonlinear energy operators.

where $N$ is the length of the observation window (for simplicity, $N = 2^m$ where $m$ is a positive integer), $D$ is the amount of overlap between consecutive windows, $n$ is an integer indicating the time index of $\{s(n)\}$, and $k$ is the feature time index. Note that for $k > 1$, $E_D(k)$ updates every $N - D$ samples of $\{s(n)\}$. Fig. 5(a) shows an implementation of this operator based on the proposed SAR ADC/multiplier. The circuit has two operation modes: analog signal conversion (phase $\varphi_1 = 0$) and digital squaring of the previously quantized signal $s(n)$ (phase $\varphi_1 = 1$). This latter operation is carried out by feeding back $s(n)$ to both digital input ports of the ADC.

The squared values $s^2(n)$ are cyclically stored in an $N$-sample memory at instances of the pulse train $\varphi_e$. This is done by first retrieving and then replacing the memory positions previously occupied by the instances $s^2(n - N)$. A counter, running at the same rate as $\varphi_e$, addresses the read/write positions. The samples stored in the memory are accumulated in an output register to provide the $E_D(k)$ values. Two cases can be distinguished. For $k = 1$, the samples $s^2(n)$, $n = 1, ..., N$, are summed in the accumulator as soon as they are stored in the memory. For $k > 1$, the digital word in the register is updated by solely adding the difference $s^2(n) - s^2(n - N)$. The values of the running average energy $E_D(k)$ are obtained by shifting right by $m$ bits the values stored in the register.

### B. Nonlinear energy operator

The nonlinear energy operator of a time series $\{s(n)\}$ is defined as [8], [10]

$$\Psi(n-1) = s^2(n-1) - s(n) \cdot s(n-2) \qquad (2)$$

which can be easily implemented by the circuit of Fig. 5(b). In this case, the SAR ADC/multiplier has three operation modes, one for converting the input signal into the vector $s(n)$, another for calculating the square term in (2) (phase $\varphi_1 = 1$), and a third term for calculating the last product in (2) (phase $\varphi_2 = 1$). As long as different samples of the input signal are involved in the NEO operator, digital registers are used to store $s^2(n-1)$

and $s(n-2)$. When both terms in (2) are available, a simple substractor obtains the operator value.

## V. Simulation Results

The SAR ADC/multiplier described in Sec III has been sized in a 0.18 $\mu$m HV CMOS technology. Transistor-level simulations of the circuit performing as ADC preliminary show 7.8-b ENOB at 4 kS/s and consumes about 10nW. Fig. 6 illustrates the performance of the circuit as multiplier, running at the same sampling frequency of 4 kS/s. All possible $\mathbf{X}$ and $\mathbf{Y}$ combinations have been formed and the product deviations from the ideal $\mathbf{Z}$ value have been computed. As can be seen, errors remain below $\pm 1$ bit and, most often, no errors occur.

The SAR ADC/multiplier has been also evaluated when embedded in the running average energy operator decribed in Sec. IV.A. The digital circuitry around the multiplier has been modeled in VHDL. The sampling frequency of the SAR ADC/multiplier has been scaled down to 512 S/s, the observation window is $N = 128$ samples and the average energy updates with every new sample, i.e., $D = N-1$. Fig. 7 (top) show the signal used as testbench. It is a scalp EEG signal sampled at 256 S/s available in the CHB-MIT Scalp EEG Database [14]. Concretely, the signal is a 70 seconds beta-band filtered sequence recorded from channel 9 (FP2-F4) of a patient (11 years, female). This time interval includes an epilepsy episode that according to annotations happens during the interval [1467, 1494] seconds. Fig. 7 (bottom) compares the theoretical and simulated results obtained in the calculations. The maximum deviation between both plots only amounts 1 LSBs and, hence, the proposed circuit could be suitably used in the detection of epileptic seizures. Proper operation with similar error levels were also observed in the electrical simulation of the NEO operator of Fig. 5(b).

## VI. Conclusions

This paper has presented the design principles of a non-coventional approach for the multiplication of digital vectors by reusing charge-redistribution SAR ADCs. The concept has been illustrated and verified with electrical simulations of a 8-b fully-differential rail-to-rail SAR ADC/multiplier, sized in a 180 nm HV CMOS technology. Preliminary results indicate that the proposed approach may represent a promising low-area low-power alternative for the feature extraction of neural signals when quadratic operators are involved.

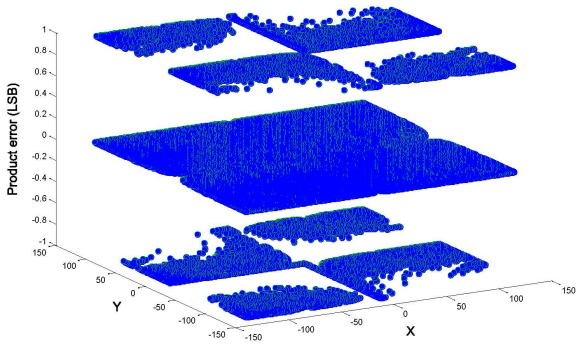


Figure 6. Errors in the multiplication of X and Y.


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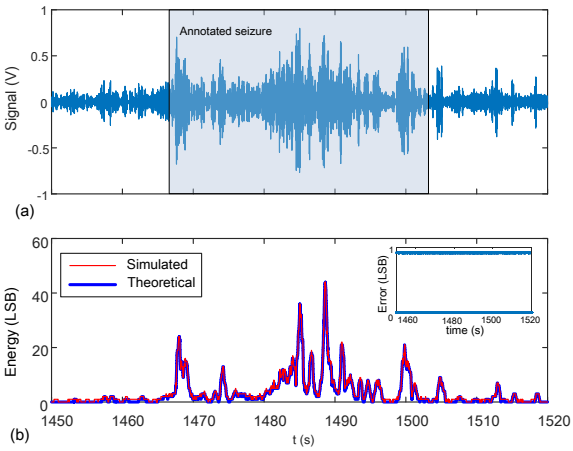


Figure 7. (a) Scalp EEG signal and (b) running average energy from circuit simulation and theoretical calculation (the inset shows the difference between them).