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Issues on Analysis and Design of Single-Phase Grid-Connected Photovoltaic Inverters

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ABSTRACT

This thesis provides a comprehensive study of the problems in single-phase grid-connected photovoltaic (PV) systems. The main objective is to provide an explicit formulation of the dynamic properties of the power-electronic-based PV inverter in the frequency domain. Such a model is used as the main tool to trace the origins of the observed problems that cannot be studied with the conventional time-domain analyses. The dynamic model also provides the tool for deterministic control-system design.

Grid-connected PV inverters have been reported to reduce damping in the grid, excite harmonic resonances and cause harmonic distortion. These phenomena can lead to instability or production outages and are expected to increase in the future, because the installed capacity of the grid-connected PV energy is rapidly growing. A PV generator (PVG) itself is a peculiar source affecting the inverter dynamic behavior. The PVG is internally a current-source with limited output voltage and power. The nonlinear behavior yields distinguishable operating regions: the constant-current region at the voltages lower than the maximum-power-point (MPP) voltage and constant-voltage region at the voltages higher than the MPP voltage. Such a behavior is quite well known but not really understood to need special attention. Vast majority of the photovoltaic inverters originate from the voltage-source inverter (VSI) with a capacitor connected at the input terminal for power-decoupling purposes. It is convenient to assume that the inverter is supplied by a voltage source and perform the analyses based on the existing modeling and design teqhniques of the voltage-fed (VF) VSI. However, the input voltage of a PV inverter must be controlled for MPP-tracking purposes, which implies that the inverter has to be analyzed as a current-fed (CF) inverter. Such analysis reveals that the CF VSI has second-order dynamics compared to the first-order dynamics of the VF VSI. The control dynamics of the CF VSI is also shown to incorporate right-half-plane zero and pole introducing control-system-design constraints.

This thesis presents the dynamic modeling procedure of PV inverter both at open and closed loop taking into account the type of the input source. The dynamic behavior of the PVG is modeled as an operating-point-dependent dynamic resistance, which is shown to shift the operating point dependent zero and pole in the inverter control dynamics between the right and left halves of the complex plane. It is also shown that the negative-incremental-resistance behavior of the inverter output impedance makes the inverter prone to instability and the grid to harmonic resonance problems, and that such a behavior can originate e.g. from the grid synchronization and the cascaded control scheme. It is important to recognize such a behavior in order to enable reliable large-scale utilization of the PV energy.

PREFACE

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SYMBOLS AND ABBREVIATIONS

ABBREVIATIONS

A	Ampere
AC, ac	Alternative current
CC	Constant current
cc	Current controller
CCR	Constant current region (of a photovoltaic generator)
CF	Current-fed (i.e. supplied by a current source)
CFSQBB	Current-fed semi-quadratic buck-boost
CSI	Current source inverter
CV	Constant voltage
CVR	Constant voltage region (of a photovoltaic generator)
DC, dc	Direct current
dB	Decibel
dBA	Decibel-ampere
dBS	Decibel-siemens
dBV	Decibel-volt
dBΩ	Decibel-ohm
G	G-parameter model (i.e. voltage-to-voltage)
H	H-parameter model (i.e. current-to-current)
Hz	Hertz
L	Load subsystem
LHP	Left half of the complex plane
MPP	Maximum power point
MPPT	Maximum power point tracking
NPC	Neutral-point clamped
OC	Open circuit
p.u.	Per unit value
PV	Photovoltaic
PVG	Photovoltaic generator
RHP	Right half of the complex plane
S	Source subsystem
SC	Short circuit
SSA	State space averaging
V	Volt
vc	Voltage controller
VF	Voltage-fed (i.e. supplied by a voltage source)
VSI	Voltage source inverter

Y	Y-parameter model (i.e. voltage-to-current)
Z	Z-parameter model (i.e. current-to-voltage)

GREEK CHARACTERS

Δ	Characteristic equation of a transfer function (determinant)
ω_{grid}	Grid frequency (rad/s)
ω_{loop}	Control-loop crossover frequency (rad/s)

LATIN CHARACTERS

a	Diode ideality factor
$\mathbf{A}$	State coefficient matrix A
$\mathbf{B}$	State coefficient matrix B
$\hat{c}$	Perturbed general control variable
C	Capacitor or capacitance
$\mathbf{C}$	State coefficient matrix C
c_{pv}	Internal capacitance of a photovoltaic generator
d	Duty ratio
$\hat{d}$	Pertured duty ratio
D	Steady-state value of the duty ratio
$\mathbf{D}$	State coefficient matrix D
d'	Compelement of the duty ratio
D'	Compelement of the duty ratio in steady state
$\mathbf{f}$	General function in time domain
$f_{\text{-3dB}}$	Cut-off frequency of PV impedance magnitude curve
f_{sw}	Switching frequency
G_{a}	Modulator gain
G_{cc}	Current controller transfer function
G_{ci}	Control-to-input transfer function
G_{co}	Control-to-output transfer function
G_{io}	Forward (input-to-output) transfer function
G_{se}	Voltage sensing gain
G_{vc}	Voltage controller transfer function
i_0	Diode reverse saturation current
i_{C}	Capacitor current
i_{cpv}	Current through the capacitance c_{pv}
i_{d}	Diode current
i_{g}	Grid current
i_{in}	Input current
$\hat{i}_{\text{in}}$	Perturbed input current
$\hat{i}_{\text{inS}}$	Perturbed source subsystem input current

i_{inv}	Inverter input current
i_{L}	Inductor current
$\hat{i}_{\mathrm{L}}$	Perturbed inductor current
i_{o}	Output current
$\hat{i}_{\mathrm{o}}$	Pertured output current
$\hat{i}_{\mathrm{oL}}$	Pertured load subsystem output current
i_{ph}	Photocurrent, i.e. current generated via photovoltaic effect
i_{pv}	Terminal (output) current of a photovoltaic generator
I_{pv}	Photovoltaic generator operating-point current
i_{rsh}	Current through the resistance r_{sh}
I_{in}	Steady-state input current
I_{L}	Steady-state inductor current
I_{o}	Steady-state output current
$\mathbf{I}$	Identity matrix
k	Boltzmann constant
k_{grid}	Coefficient regarding the input-voltage-control bandwidth
k_{i}	Coefficient regarding the short-circuit current of a PVG
k_{RHP}	Coefficient regarding RHP pole in the input voltage loop
L	Inductor or inductance
L_{in}	Loop gain for input-voltage control loop
L_{in}	Loop gain for intermediate-voltage control loop
L_{out}	Loop gain for output-current control loop
N_{s}	Number of series-connected cells in a photovoltaic generator
p_{pv}	Power of a photovoltaic generator
q	Electron charge
r_{C}	Equivalent series resistance of a capacitor
r_{d}	Diode resistance (non-linear)
r_{ds}	Drain-to-source resistance of a switch
r_{L}	Equivalent series resistance of an inductor
r_{pv}	Internal resistance of a photovoltaic generator
r_{s}	Internal series resistance of a photovoltaic generator
r_{sh}	Internal shunt resistance of a photovoltaic generator
R_{eq}	Equivalent current-sensing resistor
s	Laplace variable
S	Switch component
t	Time
T	Temperature
T_{oi}	Reverse (output-to-input) transfer function
$\mathbf{u}(t)$	Input variable vector in time domain
$\hat{\mathbf{u}}(t)$	Perturbed input variable vector in time domain

u_{d}	Diode voltage
u_{g}	Grid voltage
u_{in}	Input voltage
$\hat{u}_{\mathrm{in}}$	Perturbed input voltage
$\hat{u}_{\mathrm{inS}}$	Perturbed source subsystem input voltage
u_{inv}	Inverter input voltage
u_{C}	Capacitor voltage
u_{L}	Inductor voltage
u_{o}	Output voltage
$\hat{u}_{\mathrm{o}}$	Pertured output voltage
$\hat{u}_{\mathrm{oL}}$	Pertured load subsystem output voltage
u_{pv}	Terminal (output) voltage of a photovoltaic generator
U_{pv}	Photovoltaic generator operating-point voltage
u_{ref}	Reference voltage
U_{C}	Steady-state capacitor voltage
U_{in}	Steady-state input voltage
U_{o}	Steady-state output voltage
$U(s)$	Input variable vector in laplace domain
$\hat{x}_{\mathrm{in}}$	Perturbed input variable of interconnected system
$\mathbf{x}(t)$	State variable vector in time domain
$\hat{\mathbf{x}}(t)$	Perturbed state variable vector in time domain
$\mathbf{X}(s)$	State variable vector in laplace domain
$\mathbf{y}(t)$	Output variable vector in time domain
$\hat{\mathbf{y}}(t)$	Perturbed output variable vector in time domain
Y_{ff}	Feedforward admittance
$\mathbf{Y}(s)$	Output variable vector in laplace domain
Y_{in}	Input admittance
$\hat{y}_{\mathrm{o}}$	Perturbed output variable of interconnected system
Y_{o}	Output admittance
Y_{S}	Source admittance
Z_{in}	Input impedance
Z_{L}	Load impedance
Z_{o}	Output impedance
Z_{S}	Source impedance

SUBSCRIPTS

-∞	Ideal transfer function
1,2...	Indexing numbers
-c	Closed loop
grid	Utility grid

loop	Control loop
max	Maximum
min	Minimum
-o	Open loop
-oco	Open-circuited output
p	pole (root of transfer function denominator)
pv	Photovoltaic generator
RHP	Right half of the complex plane
SA	Source affected
-sci	Short-circuited input
z	Zero (root of transfer function nominator)

SUPERSCRIPTS

-1	Matrix inverse
G	G-parameter model (i.e. voltage-to-voltage)
H	H-parameter model (i.e. current-to-current)
im	Intermediate or intermediate-voltage-control loop is closed
in	Input or input-voltage-control loop is closed
io	Output current
L	Load subsystem transfer function
out	Output current control loop is closed
out-in	Output current and input voltage control loops are closed
S	Source subsystem transfer function
SA	Source-affected transfer function
uim	Intermediate voltage
uin	Input voltage
Y	Y-parameter model (i.e. voltage-to-current)
Z	Z-parameter model (i.e. current-to-voltage)

1 INTRODUCTION

This chapter introduces the background of the research, clarifies the motivation for the conducted research and reviews the existing knowledge related to the topic of the thesis and the ideas presented in it. In addition, the structure, objectives and main scientific contributions of the thesis are introduced.

1.1 Photovoltaic energy

Majority of global energy consumption is covered by non-renewable fuels, such as coal, peat, oil, natural gas and nuclear. In 2009, 86.7 % of primary energy consumption and 80.5 % of electrical energy production was covered by the non-renewable fuels. The share of hydropower in electrical energy production was 16.2 % while other renewable energy sources covered only 3.3 % (IEA, 9.3. 2012).

The depletion of the non-renewable fuel supplies is a serious threat in the relatively near future. Abbott (2010) estimates that at the current rate of consumption reasonably recoverable coal reserves will run out in 130 years, natural gas in 60 years, oil in 40 years and uranium resources used in the nuclear energy production in 80 years. In addition, Abbott reminds that oil, coal and gas are precious resources used in numerous crucial industrial applications and physical products and thus should be conserved and not burned.

The burning of the fossil fuels generates emissions that cause environmental pollution and global warming, which is considered as one of the main issues of modern society. The mitigation of the global warming problem, energy independency and securing the availability of energy also in the future require the promotion of energy consumption in electrical form, energy conservation and harnessing renewable energy resources such as solar and wind (Barroso et al., 2010; Bose, 2010; Razykov et al., 2011).

Solar energy has enormous potential. Kroposki et al. (2009) estimate that the annual global energy consumption of mankind is less than the energy the earth receives from the sun in one hour. Solar radiation can be exploited as heat or converted directly into electrical energy by means of photovoltaic (PV) conversion (Parida et al., 2011). A PV cell is the basic building block of a PV generator (PVG). The low-voltage PV cells are typically connected in series to form higher-voltage units known as modules, enabling practical harvesting of the PV energy. The modules may be further connected in series

and parallel to form strings and arrays for utility-scale PV energy harvesting (Rahman, 2003).

Most of the commercial PV technology is based on silicon, which is the basic material of modern electronics. Therefore, the manufactoring process of silicon is well-known and the existing facilities enable large-scale commercial production of the silicon-based PV cells. The efficiency of the silicon-based PV cells can be over 20 %, although higher efficiencies have been achieved utilizing materials such as gallium and arsenic (Green et al., 2012). Because the efficiency of the PVG is low, the interfacing-converter efficiency is a vital aspect in the PV system design.

The first large-scale interest in the silicon-based PV technology since its invention in 1955 emerged in the mid 1970s. The oil crisis and the increasing demand to use PV technology in large telecommunication systems stimulated rapid development of the module technology, resulting in the first modern PV modules (Green, 2005). The current interest is to use the PV technology in grid-connected applications driven by the urge to minimize environmental pollution and dependency on oil, positive price development of renewable energy technologies and their public subventions (Rahman, 2003; Watt et al., 2011).

The solar PV electricity has had the highest growth rate of all electrical energy production with the annual increase of 33 % in production capacity. It has been estimated that solar PV will be the second largest source of renewable electrical energy generation after wind power around 2020, excluding hydropower, and the largest source around 2050 (Valkealahti, 2011). Valkealahti forecasts that the solar PV will be competitive without subventions by mid 2030's with an uncertainity margin of 10 years depending on the geographical solar radiation conditions.

1.2 Photovoltaic generator as an input source

Simplified electrical equivalent circuit of a PV cell can be represented by a parallel connection of a photocurrent i_{ph}, which is linearly proportional to the irradiation, and a diode depicting the properties of the semiconductor junction as shown in Fig. 1.1. In addition, the practical single-diode model of a PV generator includes shunt resistace r_{sh} and series resistance r_{s} depicting losses in the cell (Liu and Dougal, 2002; Villanueva et al., 2009). In Fig. 1.1, i_{pv} is the PV cell terminal current, u_{pv} is the terminal voltage, i_{rsh} is the current through the shunt resistance and i_{d} is the diode current.

The single-diode model can also be used to model the operation of a PV module, i.e. a series connection of PV cells, by scaling the module parameters as presented by Villanueva et al. (2009). According to Villanueva et al., the static terminal characteristics

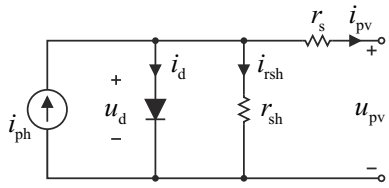


Fig. 1.1: Simplified electrical equivalent circuit of a PV cell.

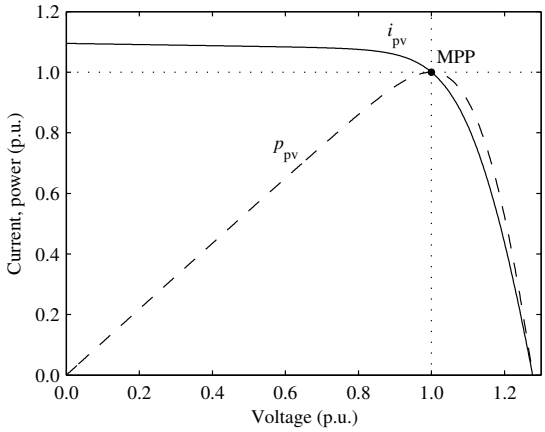


Fig. 1.2: Static terminal behavior of a PVG.

of a PV module can be given by

$$i_{\mathrm{pv}} = i_{\mathrm{ph}} - i_0 \left[\exp\left(\frac{u_{\mathrm{pv}} + r_{\mathrm{s}} i_{\mathrm{pv}}}{N_{\mathrm{s}} a k T / q} \right) - 1 \right] - \frac{u_{\mathrm{pv}} + r_{\mathrm{s}} i_{\mathrm{pv}}}{r_{\mathrm{sh}}}, \tag{1.1}$$

where i_{ph} is the photocurrent generated by the irradiation, i_0 is the diode reverse saturation current, T is the temperature of the p-n junction in Kelvin, k is the Bolzmann constant, a is the diode ideality factor, q is the electron charge and N_{s} is the number of series-connected PV cells.

The static terminal characteristics are shown in Fig. 1.2 as a current-voltage (IV) and power-voltage curves presented in normalized (p.u.) values. Fig. 1.2 shows that the PVG is a power and voltage-limited current source. At voltages lower than the MPP, the internal current-source property determines the terminal characteristics, i.e. the PVG current i_{pv} stays relatively constant despite changes in the operating point. At voltages higher than the MPP, the PVG voltage (and thus also power) is limited due to the forward biasing of the diode in Fig. 1.1 and the PVG has the properties resembling a voltage source, i.e. the PVG voltage stays relatively constant despite the changes in the operating point.

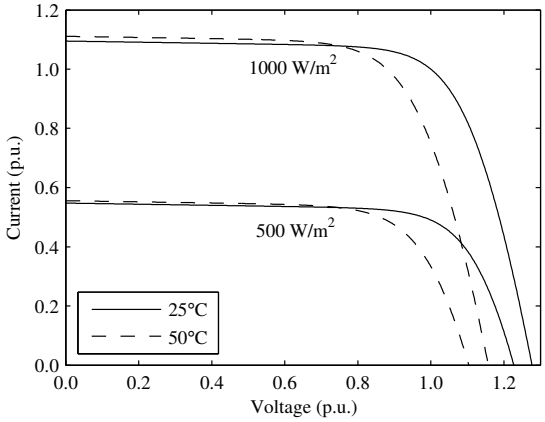


Fig. 1.3: Static terminal behavior of a PVG at varying irradiance and temperature.

In order to maximally utilize the energy of solar radiation by using a PVG, its operating point should constantly be kept at the maximum power point (MPP, Fig. 1.2), in which

$$\frac{\mathrm{d}p_{\mathrm{pv}}}{\mathrm{d}u_{\mathrm{pv}}} = \frac{\mathrm{d}(u_{\mathrm{pv}} i_{\mathrm{pv}})}{\mathrm{d}u_{\mathrm{pv}}} = I_{\mathrm{pv}} + U_{\mathrm{pv}} \frac{\mathrm{d}i_{\mathrm{pv}}}{\mathrm{d}u_{\mathrm{pv}}} = 0, \tag{1.2}$$

where I_{pv} and U_{pv} are the MPP current and voltage. Esram and Chapman (2007) have reviewed various algorithms used for MPP-tracking (MPPT) that has to be implemented in order to locate the MPP along the PVG IV-curve.

In Eq. (1.1), the p-n junction temperature is in the denominator of the power of the exponential function, which can be used to determine the open-circuit voltage. Accordingly, a PVG provides more power at lower temperatures. The temperature and irradiance dependency of a PVG is depicted in Fig. 1.3. The open-circuit voltage is mostly determined by the temperature and the short-circuit current by the solar radiation.

1.3 Grid-connected photovoltaic systems

The grid-integration of a PVG requires a power electronic interface, an inverter. Power electronics is a key technology in a sustainable energy future by enabling efficient energy conversion and grid integration of renewable energy sources (Blaabjerg et al., 2004; Carrasco et al., 2006; Popovic-Gerber et al., 2011). Popovic-Gerber et al. have studied the energy payback times of power electronic systems and conclude that power electronics does not only enable the grid-integration of renewable energy sources but also offers vast energy saving potential e.g. in motor drives and lighting. Harnessing such a potential is crucial in achieving sustainable energy future.

According to Blaabjerg et al., the way to fully exploit the renewable energy sources is the grid connection, where the power electronics plays a vital role in matching the grid-connection requirements and the intermittent nature of the renewables. The basic rule in the power grid is that the consumption and production of electrical energy match all the time. The output power of the renewables, on the other hand, is determined e.g. by environmental conditions. Carrasco et al. discuss the future urge to utilize energy storing technologies in order to store excess renewable energy and utilize it during the low-production conditions. Kakimoto et al. (2009) have proposed a ramp-rate-control scheme utilizing stored energy in order to level out the varying PV inverter output due to moving clouds.

Each grid-connected PV conversion system composes of at least the inverter, but may also contain an additional dc-dc converter used as an upstream converter between the PVG and the inverter forming a two-stage conversion scheme. The use of the additional dc-dc stage enables the use of PV string composed of less series-conncted PV modules compared to single-stage conversion scheme, which may be beneficial in case of partial shading conditions (Mäki and Valkealahti, 2012). The dc-dc stage can also regulate its input voltage to practically pure dc (i.e., it provides perfect power decoupling), which according to Wu et al. (2011) can compensate the energy losses caused by single-phase power fluctuation affecting especially the single-stage single-phase inverters. The grid-connected PV inverters are subjected to high expectations and requirements. According to Araneo et al. (2009); Eltawil and Zhao (2010), the PV inverters should have

- high conversion efficiency,
- high-accuracy MPP-tracking facility,
- long life span,
- high quality of injected power,
- reduced cost, size and weight
- and comply with all the required standards for the grid interfacing.

1.3.1 Photovoltaic inverter concepts

The most common concepts of interfacing PVG to the utility grid are shown in Fig. 1.4. In the modular concept shown in Fig. 1.4a, each PV module is interfaced to the grid with a dedicated micro inverter. Typically the micro inverter adopts the two-stage conversion scheme since the input-voltage requirement of a typical single-phase inverter is at least the peak grid voltage with a sufficient margin, and the MPP voltage of a typical module is in the order of a few tens of volts. Matching such a high voltage difference requires

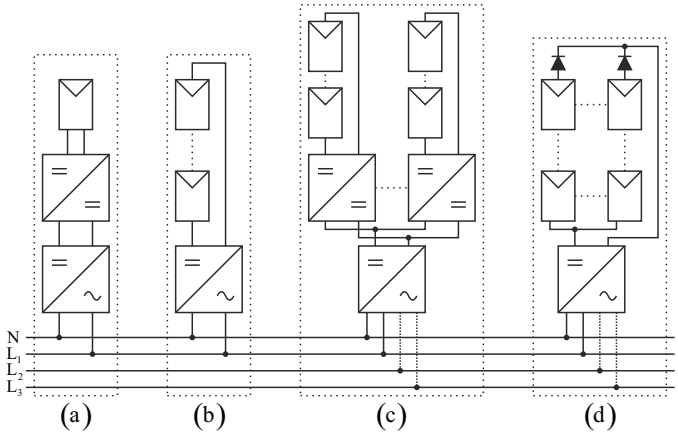


Fig. 1.4: a) Module-integrated, b) string, c) multistring and d) central inverter concepts.

the use of converter topologies with high conversion ratio (Kjaer et al., 2005; Li and He, 2011). The modular concept has good expandability and high MPP tracking efficiency due to dedicated MPP-trackers for each module (Liu et al., 2011; Roman et al., 2006). The disadvantage of the modular concept is the high conversion ratio requirement, which has a negative effect on the conversion efficiency.

The relatively high PV voltage required for the single-stage inverter can be achieved by connecting PV modules in series, forming the PV string. The string-inverter concept is shown in Fig. 1.4b. The string inverters are characterized by simplicity and high efficiency. The string inverter is one of the most interesting concepts in small-scale PV power production such as residential rooftop applications (Araujo et al., 2010; Liu et al., 2011; Myrzik and Calais, 2003; Schönberger, 2009). The disadvantage of the string inverter concept is the increased propability of partial shading of the long PV string, especially in the built environment, which may significantly reduce the energy production.

The multistring-inverter concept using the additional dc-dc stages is shown in Fig. 1.4c. Each of the dc-dc stages fed by individual PV strings are connected to the inverter input terminals in a parallel configuration. The combined power of the multiple short strings may require the use of a three-phase inverter topology (Araujo et al., 2010). A modular dc-dc conversion scheme can be derived from the multistring-inverter concept, where each of the short strings is replaced by a single PV module (Zhang et al., 2011).

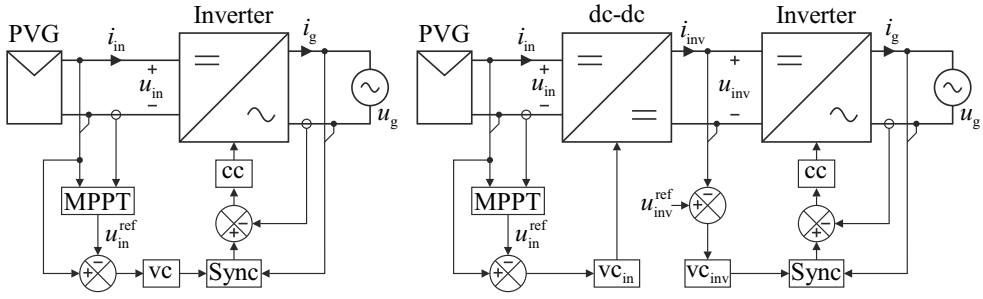
In the central-inverter concept shown in Fig. 1.4d, the inverter is fed by a parallel connection of long PV strings forming a high-power PV array. The central inverter concept was popular in the early grid-connected PV systems and is still typically used in dedicated high-power PV plants. The strings are typically equipped with series-connected

diodes in order to prevent negative power flow in the strings, because in partial shading conditions the non-shaded strings could inject power to a shaded string possibly damaging it. Most of the central inverters are three-phase inverters, although some single-phase products exist in the PV market according to Araujo et al. (2010). Araujo et al. also mention a minicentral concept, which is based on three single-phase string inverters forming a three-phase system. Its main advantage is that the input-voltage requirement of a single-phase inverter is reduced compared to three-phase topologies, allowing the use of higher efficiency topologies and shorter PV strings.

Most of the PV inverters are based on the voltage-source-inverter (VSI) topology, although the use of current-source-inverter (CSI) topology is proposed e.g. by Sahan et al. (2011). The VSI-based multilevel inverter is also an emerging application, whose main advantages, according to Calais et al. (1999), are low grid-current ripple and the ability to use lower-voltage-rating components. However, this thesis mainly studies the VSI-based inverter. A review of various topologies for single-phase grid interfacing of renewable resources can be found e.g. in (Lai, 2009).

1.3.2 Single- and two-stage conversion schemes

A single-stage grid-connected PV conversion scheme is shown in Fig 1.5a. The single-stage PV inverter employs a cascaded control scheme, where an inner grid-current-feedback loop controls the grid current and an outer input-voltage-feedback loop controls the input voltage by generating the grid-current reference (Yazdani and Dash, 2009). The grid-current reference must be synchronized with the grid voltage (Sync.) utilizing some of the various existing grid synchronization methods (Teodorescu et al., 2011). The current controller is denoted by cc and voltage controller by vc in Fig 1.5a. The input-voltage reference is generated by the MPPT facility. The grid-current control is a must in grid-connected applications in order to inject high quality power to the grid.



(a) Single-stage. **(b)** Two-stage.

Fig. 1.5: Single and two-stage PV conversion schemes.

A two-stage grid-connected PV conversion scheme is shown in Fig 1.5b. In the two-stage conversion scheme, the inverter again controls its input voltage by means of the cascaded control scheme. The input-voltage controller of the inverter is denoted by vc_{inv} and the input-voltage controller of the dc-dc stage by vc_{in} in Fig 1.5b. The inverter input-voltage reference in the two-stage conversion scheme is constant (i.e., proportional to the grid voltage) compared to the varied input-voltage reference of the single-stage scheme. The dc-dc converter in the two-stage scheme is responsible for the MPPT function, either by controlling its input voltage or current, or by operating at open loop (Khalifa and El-Saadany, 2011; Masoum et al., 2002).

In PV applications, the input-current control is prone to saturation, since the MPP current is close to the short-circuit current that is dependent on the irradiation level with relatively fast dynamics. The open-circuit voltage, on the other hand, is dependent mostly on the temperature with negligibly slow dynamics, thus input-voltage control can be realized in a reliable manner (Xiao et al., 2007). It has been studied by Messo et al. (2012) that the input-voltage control of the dc-dc pre-regulator transforms its output into a constant-power-type source, which is beneficial for the inverter. Therefore, the input-voltage control is also recommended over the open-loop-based MPPT.

Some authors claim that the dc-dc converter in the two-stage conversion scheme could be used to control the dc-link voltage (Kwon et al., 2006; Liao and Lai, 2011; Vighetti et al., 2012). However, it has been proven e.g. by Leppäaho et al. (2010); Nousiainen et al. (2011b); Puukko et al. (2012), that an output-side control, be it output current or voltage, cannot draw maximum power out of a PVG without compromising the stability, as will also be shown in this thesis. Thus, input-voltage control should always be used. This implies that the PVG-interfacing converters are current-fed converters instead of traditional voltage-fed converters (Capel et al., 1983). The correct identification of the controlled variables in a PV converter is of utmost importance, because the dynamic formulation of a converter is based on the selection of controlled variables (system outputs) and uncontrollable variables (system inputs), where the transfer-function set of the converter describes the relation between the system inputs and outputs (Suntio, 2012). The dynamic formulation of a PV converter is discussed in detail later in this thesis.

1.4 Issues on single-phase photovoltaic systems

Electricity generation has been centralized in large power plants until the recent development towards distributed energy generation. The rapidly increasing penetration level of the dispersed power generation, such as relatively small-power PV plants, has increased concerns about the reliability and quality of the electricity supply (Bletterie and Brunner, 2006; Braun et al., 2011). Bletterie and Brunner define reliability by the number and duration of power interruptions and power quality by the distortions, such as harmon-

ics, voltage dips or flicker. According to Braun et al., the PV inverters have adopted a passive approach in the grid connection, but in the future should actively participate in grid control in order to maintain reliable and high-quality electricity supply without the need for excess grid reinforcements, and to keep the costs of PV grid integration low.

In the passive grid-connection approach, PV inverters are required to inject high quality active power and disconnect from the grid upon detection of e.g. over- or undervoltage, excess grid frequency deviation or detection of an islanding situation in the grid (Ciobotaru et al., 2010). When the number of PV systems in the grid is high, such voltage and frequency deviations might disconnect a large portion of power production off the grid leading to an unrecoverable violation of the power balance and total loss of electricity supply. The energy stored in the inertia of traditional spinning generators has maintained grid integrity during the violations of the power balance, which is reflected as small deviations of the grid frequency that can be fixed by adjusting the amount of power production (Bebic et al., 2009).

In the active approach, the PV inverter's ability to supply real and reactive power is utilized in order to provide grid voltage and frequency supporting functions (Braun et al., 2011; Carnieletto et al., 2011). Carnieletto et al. have reviewed control methods to realize such functions in a single-phase photovoltaic inverter. It might not be feasible to disconnect a large PV plant from the grid in case of an islanding situation but let the PV plant maintain the grid by itself. Methods to cope with intended islanding have been studied e.g. by Nian and Zeng (2011); Vasquez et al. (2009); Yao et al. (2010). The dynamic formulation of the PV inverter presented in this thesis can be helpful in order to study the dynamic properties of the supporting functions or the islanding situation, although the developement of such a functionality is out of the scope of this thesis.

Chicco et al. (2009) has observed that harmonic distortion in the grid voltage excites harmonic-current pollution in a PV inverter. They have reported linear increase in the harmonic current as a function of grid harmonic voltages. This implies that PV inverters have finite output impedances at the relevant harmonic frequencies. In order to study such interactions, a dynamic model of the output impedance is required, because the time-domain analyses cannot explain such a behavior. This emphasizes the importance of the PV-inverter modeling in the frequency domain. Chicco et al. have also observed that the highest current distortion occurs in low-power conditions, i.e. in cloudy weather or at sunrise and sunset. Simmons and Infield (2000) assume that this is caused by the limited resolution of the grid-current measurement and control. Bhowmik et al. (2003) have studied the maximum allowable penetration of the distributed-generation-related inverters in the grid based on the harmonic pollution limits.

The efficiency of a PV inverter system is not merely determined by the inverter efficiency, but also by the MPP efficiency (Bletterie et al., 2011). The MPP efficiency is

defined as a fluctuation of the operating point around the MPP that is caused by the inverter input-voltage ripple or inaccuracy of the MPP-tracking facility. The voltage ripple is caused either by the converter switching actions or the inherent power fluctuation at twice the grid frequency in single-phase power grid (Benavides and Chapman, 2008; Sullivan et al., 2011). The voltage ripple at twice the grid frequency may be mitigated by connecting a large capacitor at the input terminal of the inverter (Liserre et al., 2004; Prapanavarat et al., 2002) and by applying passive (Nonaka, 1994) or active power decoupling techniques (Hu et al., 2010; Shimizu et al., 2006; Tan et al., 2007; Vitorino and de Rossiter Correa, 2011). Input-voltage can be also controlled practically to dc by a pre-regulator, which provides perfect power decoupling as discussed earlier.

The most unreliable part of a PV system has been observed to be the inverter (Chan and Calleja, 2011; Petrone et al., 2008), and the most unreliable component in the inverter is the large electrolytic power decoupling capacitor (Bower et al., 2006; Kotsopoulos et al., 2001; Ninad and Lopes, 2007; Rodriguez and Amaratunga, 2008). The possibility to use a small capacitor would allow the use of other types of capacitors than electrolytics, which would increase inverter reliability. However, the issues related to the small energy-storage capacitors need to be solved (Chen et al., 2009; Chen, Wu, Chen, Lee and Shyu, 2010; Fratta et al., 2002). According to Fratta et al. (2002), the minimization of the input capacitor can lead to sub-harmonic oscillations in the inverter or even instability. In this thesis, the minimum allowed input capacitance for the single-phase PV inverter is derived based on the input-voltage-control stability.

1.4.1 Grid interactions

The inverters related to distributed generation have been observed to generate harmonic current pollution, excite harmonic resonances in the grid or even cause instability, especially, in weak grid conditions (Cespedes and Sun, 2009, 2011; Chen and Sun, 2011; Enslin and Heskes, 2004; Heskes et al., 2010; Liserre et al., 2006; Mohamed, 2011; Sun, 2008; Wang et al., 2011). Such issues can be most conviniently studied based on inverter and grid impedances. It is well known that the stability of an interconnected voltage-fed system can be assessed by applying the Nyquist stability criterion to the impedance ratio of the load and source subsystems known as minor-loop gain ($Z_{\mathrm{o}}/Z_{\mathrm{in}}$), where Z_{o} is the output impedance of the source subsystem and Z_{in} is the input impedance of the load subsystem (Middlebrook, 1976). The stability of a current-fed system can be assessed by the inversion of the minor-loop gain ($Z_{\mathrm{in}}/Z_{\mathrm{o}}$) (Leppäaho et al., 2011; Sun, 2011). Typically the stability criterion is used to study the stability of the inverter/grid interface, but it naturally also applies to the PVG/inverter interface.

If the impedance ratio of an interconnected system consisting of independently stable source and load subsystems does not satisfy the Nyquist stability criterion, the inter-

connected system is unstable. It can be deduced that the impedance-based stability criterion will be violated in a PV system if $|Z_{\text{in}}/Z_{\text{o}}| \geq 1$ while the phase difference of the impedances exceed 180 degrees. Therefore, it is obvious that problems can be expected when the grid impedance is high (weak grid conditions), as reported e.g. by Liserre et al. (2006). Likewise, Caamano-Martin et al. (2008) reports that PV inverters do not contribute to the harmonic current pollution in strong networks (i.e. the grid impedance is low). The concept of minor-loop gain can be used to determine the stability of the interface between the inverter and the utility grid (Cespedes and Sun, 2009; Sun, 2011), but it can also be used to study the harmonic resonance problem (Chen and Sun, 2011; Wang et al., 2011). Wang et al. propose that the standards regarding distributed generation inverters should include limits for the minimum inverter output impedance.

If the source and load subsystem impedances show passive-circuit-like behaviour, i.e. the impedance phase lies between $\pm 90°$, the violation of the stability criterion requires undamped circuits. Accordingly, the passive-circuit-like behavior can excite harmonic resonances, but a complete loss of stability requires active-circuit-like behaviour in the inverter output impedance. Therefore, it is obvious that negative-resistor-like behavior (phase is $-180°$) in the inverter output impedance exposes the inverter/grid interface to instability (Heskes et al., 2010). One of the origins of the negative-resistor-like behavior is the grid synchronization (Cespedes and Sun, 2011; Enslin, 2005). Enslin implicitly concludes that grid-synchronization where the shape of the grid voltage is used to shape the grid current reference results in negative-resistor-like behavior. In this thesis, such a multiplier-based synchronization is analyzed and an additional negative-output-impedance term caused by the synchronization is explicitly formulated.

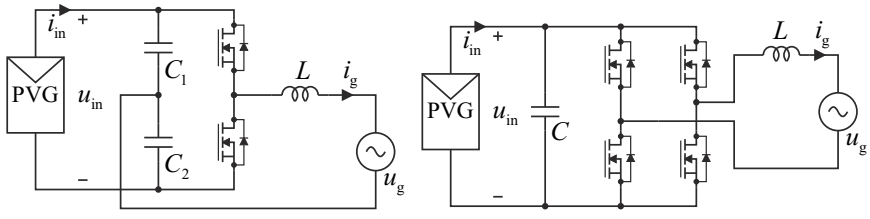
1.4.2 Ground-leakage current

The PV modules have a high surface area forming relatively high parasitic capacitance between the module and its framing. According to Calais et al. (1999), the parasitic capacitance might be up to several nanofarads per module. The PV module installation is typically connected to the system ground. Therefore, a path between the dc-side and the neutral conductor exists allowing possible ground-leakage current to flow (also known as common-mode current). The ground-leakage current is owing to a high rate-of-change of voltage ($\mathrm{d}u/\mathrm{d}t$), known as common-mode voltage, induced accross the ground capacitance by the inverter switching actions, which creates the ground-leakage current according to $i_{\text{C}} = C \cdot \mathrm{d}u_{\text{C}}/\mathrm{d}t$. The ground current is limited by standards and may decrease the lifetime of the PV module and the inverter efficiency as well as distort grid current and cause electromagnetic interference (Gubia et al., 2007; Lopez et al., 2010; Xiao and Xie, 2010). According to Bower and Wiles (2000), the ground-leakage current may become large enough to indicate a ground fault and cause unwanted tripping of

safety equipment. Such false indications of ground faults can have a significant effect on the system down time (Caamano-Martin et al., 2008).

Three possible methods exist to mitigating the ground-leakage current. The first method is not to ground the PV module framing. However, in case of common mode voltage generated by the inverter between the PVG terminals and the power system grounding, a person touching a PV module is exposed to an electric hazard. Such safety concerns can be eliminated by grounding the module installation. Accoding to Lopez et al. grounding of the PVG installation is mandatory in the U.S. and in some countries in Europe. Secondly, the galvanic path could be disconnected using a transformer. A low-frequency transformer connected between the inverter and the grid is large, expensive, heavy and has low efficiency. Therefore, it is not a desired method to solve the ground-current problem, although it also blocks the dc-current that increases the risk of saturation in distribution transformers and is limited by standards (Bründlinger et al., 2009; Salas et al., 2008). A small and cheap transformer can be used integrated into a transformer-isolated dc-dc converter used as the pre-regulator (Kjaer et al., 2005). The third method is to use a topology or modulation method that excites minimal ground current to flow. Transformerless inverters are stated to be the key technology for simple, efficient and low-cost grid integration of a PVG. A lot of research effort has been devoted to the development of the transformerless inverters (Barater et al., 2009; Gonzalez et al., 2008, 2007; Kerekes et al., 2011; Xiao et al., 2011; Xue et al., 2004; Yang et al., 2012; Yu et al., 2011).

The transformerless inverter topologies are typically based either on the conventional half-bridge (Fig. 1.6a) or full-bridge inverter (Fig. 1.6b) that are also referred to as VSI-type topologies. In the half-bridge inverter, the neutral conductor is connected between two capacitors dividing the input-side voltage. Thus, the voltage accross the parasitic ground capacitance is determined by the voltages of capacitors C_1 and C_2 in Fig. 1.6a. The capacitor voltages, and therefore the ground voltage, are ideally dc and practically no ground current flows (Kerekes et al., 2007). However, the input or



(a) Half-bridge. **(b)** Full-bridge.

Fig. 1.6: Typical VSI-type single-phase PV inverters.

dc-link voltage requirement is twice the requirement of the full-bridge inverter. The half-bridge is also a 'two-level' topology, i.e. the voltage between the switches can be either negative or positive dc-voltage, which increases the output-current ripple and decreases the efficiency. A variation of the half-bridge, known as neutral-point-clamped inverter (NPC), is proposed that employs 'three-level' switching (negative, positive and zero) (Calais et al., 1999). However, the NPC suffers from the high input-voltage requirement and voltage balancing of the capacitors complicates the control-system design (Celanovic and Boroyevich, 2000).

The full-bridge inverter enables both three-level and two-level switching. Even though the two-level switching mitigates the ground-leakage current, it requires large grid-side inductor L and lowers the inverter efficiency. The three-level switching, however, is not suited for a transformerless inverter due to pulsating common-mode voltage at the switching frequency (Kerekes et al., 2007). A feasible concept that can be used to build a 'three-level' transformerless PV inverter is the concept based on unfolding inverter switching at the grid frequency as shown in Fig. 1.7 (Chiang et al., 2009; Erickson and Rogers, 2009; Kang et al., 2005; Li and Wolfs, 2008; Park et al., 2006; Prapanavarat et al., 2002; Rodriguez and Amaratunga, 2008; Tofoli et al., 2009). The unfolder is operated in such a manner that the control signal c_p is high and c_n is low during positive grid cycle and vice versa during negative grid cycle. In addition, the inverter in Fig. 1.7 composes of an additional dc-dc converter whose output current i_o is controlled according to full-wave rectified grid voltage, which is 'unfolded' into sinusoidal grid current i_g. Because of its low switching frequency, the unfolder basically only exhibits conduction losses yielding low total losses in the unfolder. The inverters analyzed in this thesis are based on the unfolding-inverter concept. A review of various transformerless PV inverters can be found e.g. in (Teodorescu et al., 2011).

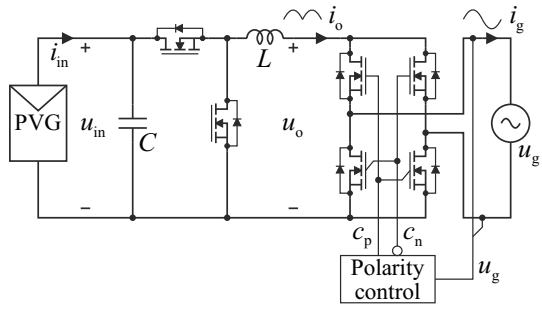


Fig. 1.7: VSI-type PV inverter based on unfolding inverter.

1.4.3 Partial shading of photovoltaic generator

As discussed earlier, the string inverters are characterized by high efficiency enabled by the development of various transformerless topologies, while micro inverters slightly lack efficiency due to wide current and voltage-conversion-ratio requirement and multiple power-conversion stages. However, the proper operation of a PV string requires uniform operating conditions. In a long string, mismatch losses in the modules increase and partial shading compromises the energy yield, especially in the built environment (Garcia et al., 2008; Mäki et al., 2011; Ramabadran and Mathur, 2009).

Partial shading generates multiple local maximum power points (MPP) to the power-voltage curve of the string as shown in Fig. 1.8, where one third of a PV module with three bypass diodes is shaded. When the shading intensity is low, the global maximum power is found at higher voltages, but when the shading intensity increases, the global MPP is found at low voltages, which might be outside the VSI-type inverter input-voltage range, and therefore, impossible to obtain. It is a demanding task for a tracking algorithm to locate a global MPP among the local maxima (Esram and Chapman, 2007; Kobayashi et al., 2006; Patel and Agarwal, 2008). In general, algorithms without special intelligence track the first maximum they find, whether it is local or global. This has been measured to cause significant energy losses in a string inverter system in addition to the decreased irradiance (Bründlinger et al., 2006).

The number of the local maxima in the power-voltage curve is defined by the bypass-diode configuration: the number of possible MPP's is the number of bypass-diodes in a

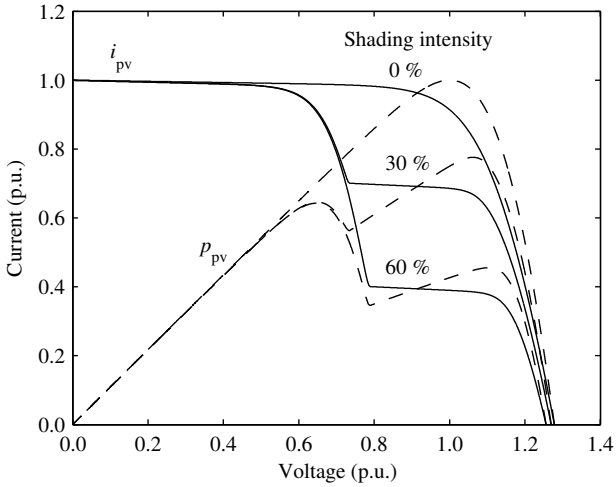


Fig. 1.8: Static terminal characteristics of a partially shaded PVG.

module multiplied by the number of modules in series, making the proper exploitation of a string in case of partial shading difficult (Silvestre et al., 2009). The issue of partial shading is an important topic that has been researched e.g. by (Deline, 2009; Mäki and Valkealahti, 2012; Wang and Hsu, 2010; Woyte et al., 2003).

In a modular system, MPP-tracking is performed on a module level, which minimizes the effect of non-uniform operating conditions of the modules. It has been shown that individual modules in parallel can outperform the series-connected string (Oldenkamp et al., 2004). The modularity can be realized in a dc-dc system (Liu et al., 2011) or by directly connecting each module to the ac grid by the micro-inverters. It has been shown that a micro-inverter system can outperform conventional string-inverter system despite lower efficiency, especially in the shaded conditions (Mohd, 2011). The potential energy yield increase is the single most important reason for modular power electronics applied in PV systems (Bründlinger et al., 2011).

Another advantage of a micro-inverter system is the modularity itself. The inverters have been observed to be one of the most unreliable parts of a PV energy system as discussed. In case of micro inverter failure, other modules in the system still provide power to the grid while failure of a string inverter seizes energy production of the string completely. The modular architecture provides straightforward expandability and reduces cost of initial investment. The micro inverter system is also free of high voltage dc wiring, switch boxes and protection devices, which substantially lowers the installation cost (Mohd, 2011). Various micro-inverter concepts has been studied e.g. by (Choi and Lee, 2012; Kwon et al., 2009; Li and Oruganti, 2012; Rodriguez and Amaratunga, 2008; Shimizu et al., 2006; Xue et al., 2004; Yu et al., 2011).

In this thesis, a new semi-quadratic buck-boost-type (CFSQBB) converter is proposed that can be used as such in a dc-dc system or used to realize a transformerless micro inverter utilizing the unfolder concept.

1.5 Structure of the thesis

In Chapter 2, the dynamic formulation of switching converters and dynamic modeling of PV systems is presented and the effect of nonideal source and load on a PV converter dynamics is formulated. Chapter 2 also presents dynamic models for the VSI- and CFSQBB-type inverters in addition to the dynamic model of a PVG.

Chapter 3 formulates the closed-loop dynamics of PV converters and the control-system designs of VSI- and CFSQBB-type inverters are presented. The closed-loop analysis reveals the property of negative-resistor-like output impedance caused by the cascaded control scheme, which is amplified by the multiplier-based grid synchronization. The design of the input-voltage control in the cascaded control scheme is derived based on the observed right-half-plane pole (RHP) in the control loop. The frequency of

the RHP pole is further used to formulate the design rule for minimum input capacitance in a single-phase single-stage PV inverter.

Chapter 4 presents experimental results and Chapter 5 summarizes the thesis and proposes important future research topics in PV inverters.

1.6 Objectives and scientific contribution

The objective of this thesis is to provide a dynamic formulation for the single-phase PV inverter and reveal the origin of some of the problems discussed. The dynamic modeling provides a powerful tool for deterministic control-system design and system-interaction and stability analyses of the interconnected systems. The basic principles presented in this thesis can be used to analyze various control practices emerging in the field of PV inverters and other renewable energy technologies based on power electronics. The scientific contribution of this thesis can be summarized as

- Explicit formulation of photovoltaic inverter modeling.
- Effect of photovoltaic generator on a single-phase VSI-type inverter dynamics.
- Design rule for the minimum input capacitance of a VSI-type photovoltaic inverter based on input-voltage-control stability.
- Explicit formulation of the effect of multiplier-based grid synchronization causing negative output impedance.
- Invention and development of a current-fed semi-quadratic buck-boost-type converter topology suited for transformerless modular photovoltaic applications.

1.7 Related papers and authors contribution

The ideas presented in this thesis are published in the following scientific publications.

[P1] T. Suntio, J. Leppäaho, J. Huusari, L. Nousiainen, "Issues on solar-generator interfacing with current-fed MPP-tracking converters," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2409-2419, Sept. 2010.

[P2] J. Leppäaho, J. Huusari, L. Nousiainen, J. Puukko, T. Suntio, "Dynamic properties and stability assessment of current-fed converters in photovoltaic applications," *IEEJ Trans. Ind. Appl.*, vol. 131, no. 8, pp. 976-984, 2011.

[P3] L. Nousiainen, T. Suntio, "Current-fed converter with quadratic conversion ratio," Patent Application, US2012007576, EP2408096, CN102332821, 2012.

[P4] L. Nousiainen, T. Suntio, "Current-fed converter," Patent Application, US2012008356, EP2408097, CN102332840, 2012.

[P5] L. Nousiainen, T. Suntio, "Dual-mode current-fed semi-quadratic buck-boost converter for transformerless modular photovoltaic applications," *14th European Conf. on Power Electronics and Applications (EPE)*, Birmingham, U.K., Aug./Sept. 2011, pp. 1-10.

[P6] L. Nousiainen, T. Suntio, "Dynamic characteristics of current-fed semi-quadratic buck-boost converter in photovoltaic applications," *3rd IEEE Energy Conversion Congr. and Expo. (ECCE)*, Phoenix, Arizona, U.S., Sept. 2011, pp. 1031-1038.

[P7] L. Nousiainen, T. Suntio, "Simple VSI-based single-phase inverter: dynamical effect of photovoltaic generator and multiplier-based grid synchronization," *IET Renewable Power Generation Conf. (RPG)*, Edinburgh, U.K., Sept. 2011, pp. 1-6.

[P8] L. Nousiainen, T. Suntio, "DC-link voltage control of a single-phase photovoltaic inverter," *IET Power Electronics, Machines and Drives Conf. (PEMD)*, Bristol, U.K., March 2012, pp. 1-6.

[P9] L. Nousiainen, J. Puukko, T. Suntio, "Appearance of a RHP-zero in VSI-based photovoltaic converter control dynamics," *33rd Int. Telecommunications Energy Conf. (INTELEC)*, Amsterdam, Netherlands, Oct. 2011, pp. 1-8.

[P10] J. Puukko, L. Nousiainen, T. Suntio, "Effect of minimizing input capacitance in VSI-based renewable energy converters," *33rd Int. Telecommunications Energy Conf. (INTELEC)*, Amsterdam, Netherlands, Oct. 2011, pp. 1-9.

[P11] J. Puukko, L. Nousiainen, A. Mäki, J. Huusari, T. Messo, T. Suntio, "Photovoltaic generator as an input source for power electronic converters," *15th Int. Power Electronics and Motion Control Conf. and Expo. (EPE-PEMC)*, Novi Sad, Serbia, Sept. 2012.

[P12] L. Nousiainen, J. Puukko, A. Mäki, T. Messo, J. Huusari, J. Jokipii, J. Viinamäki, D. Torres Lobera, S. Valkealahti, T. Suntio, "Photovoltaic generator as an input source for power electronic converters," accepted for publication in *IEEE Trans. Power Electron.*, DOI: 10.1109/TPEL.2012.2209899.

In publications [P1]-[P2], the author helped with experiments and analyses. The patent applications [P3]-[P4] are based on the new converter topologies by the author, where the second author and the supervisor of this thesis, Professor Suntio, helped in writing the patent proposals. Professor Suntio also gave useful comments and insight regarding the theoretical and experimental findings in the publications [P5]-[P6], analyzing the converter in [P4] and analyzing the dynamic properties of the VSI-type PV inverter in the publications [P7]-[P8]. The ideas behind publications [P9]-[P10] are a

collaboration with M.Sc. Puukko, who was responsible for the writing of [P10] and the author was responsible for the writing of [P9]. The author had significant contribution in the measurements and writing of [P11] and wrote the additional part of [P12] compared to [P11].

2 DYNAMIC MODELING OF PHOTOVOLTAIC CONVERTERS

In order to overcome the issues discussed earlier, a frequency-domain model of a PV converter is of great advantage. The frequency-domain (i.e. small-signal) model describes the relation between the converter input and output variables, also known as system inputs and outputs. Such models describe e.g. the relation between the control (i.e. duty ratio) and system outputs, which is needed in the control-system design, or the impedance behavior of the converter, which is important in order to study the grid interactions as discussed earlier.

2.1 State-space averaging

A conventional method to model a power electronic converter is the state-space averaging method (Middlebrook and Cuk, 1977; Suntio, 2009). In the state-space averaging, the converter operation is first averaged over a switching cycle with common average integral. The averaged derivatives of state variables $\langle \boldsymbol{x}(t) \rangle$ and system outputs $\langle \boldsymbol{y}(t) \rangle$ are represented as a function of the state variables and system inputs $\langle \boldsymbol{u}(t) \rangle$ as shown in (2.1), where the variables in angle brackets denote the average values and bold italics mean vectors. The state variables are conveniently the capacitor voltages and inductor currents. The system inputs and outputs are voltages and currents either at the load or source side. Also a control variable is a system input.

$$\begin{aligned} \frac{\mathrm{d}\langle \boldsymbol{x}(t) \rangle}{\mathrm{d}(t)} &= \boldsymbol{f}_1\left(\langle \boldsymbol{x}(t) \rangle, \langle \boldsymbol{u}(t) \rangle\right) \\ \langle \boldsymbol{y}(t) \rangle &= \boldsymbol{f}_2\left(\langle \boldsymbol{x}(t) \rangle, \langle \boldsymbol{u}(t) \rangle\right) \end{aligned} \tag{2.1}$$

In case of switching converters, the average-valued equations are non-linear and have to be linearized at a steady-state operating point. The standard linearized state-space representation is shown in (2.2) in the time domain and in (2.3) in the frequency domain. The hat over the variables denote small-signal deviation around the steady-state value

and the bold letters mean matrices.

$$\begin{aligned} \frac{\mathrm{d}\hat{\boldsymbol{x}}(t)}{\mathrm{d}\,(t)} &= \mathbf{A}\hat{\boldsymbol{x}}(t) + \mathbf{B}\hat{\boldsymbol{u}}\,(t) \\ \hat{\boldsymbol{y}}\,(t) &= \mathbf{C}\hat{\boldsymbol{x}}(t) + \mathbf{D}\hat{\boldsymbol{u}}\,(t) \end{aligned} \tag{2.2}$$

$$\begin{aligned} s\boldsymbol{X}(s) &= \mathbf{A}\,\boldsymbol{X}(s) + \mathbf{B}\,\boldsymbol{U}(s) \\ \boldsymbol{Y}(s) &= \mathbf{C}\boldsymbol{X}(s) + \mathbf{D}\,\boldsymbol{U}(s) \end{aligned} \tag{2.3}$$

The relation between the controllable output variables and uncontrollable input variables in the frequency domain can be solved using (2.3) applying basic matrix algebra as given in (2.4).

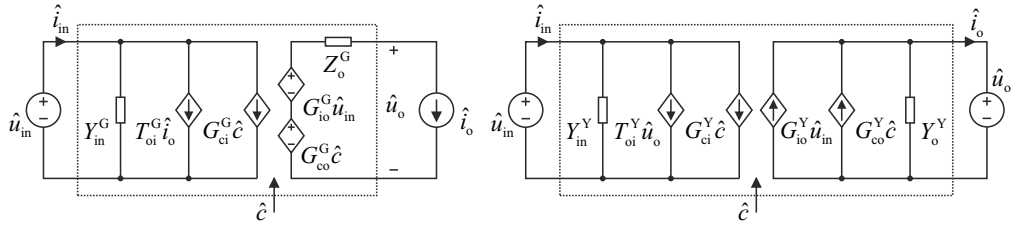
$$\boldsymbol{Y}(s) = \left(\mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B} + \mathbf{D}\right)\,\boldsymbol{U}(s) = \mathbf{G}\,\boldsymbol{U}(s) \tag{2.4}$$

The contents of the tranfer-function matrix $\mathbf{G}$ in (2.4) depend on the selection of the input and output variables. According to Suntio et al. (2011), two basic converter structures can be formed depending on the characteristics of the input power supply. If the converter is fed from a stiff current source or the input voltage is controlled, the source-side system input is the input current. If the converter is fed from a stiff voltage source or the input current is controlled, the source-side system input is the input voltage. Accordingly, Suntio et al. categorize converters into current-fed (CF) and voltage-fed (VF) converters.

2.2 Two-port network representation

The CF and VF converters can be further divided according to their load mode, be it voltage-type load or a current sink. Consequently, four possible conversion structures exist that can be represented by the transfer function set given in (2.4). The transfer function sets can be equally represented by linear two-port network models, which is a common practice in circuit theory (Tse, 1998). According to Tse, the transfer-function sets of the four conversion structures are known as G-, Y-, Z- and H-parameters. All of the parameters consist of a set of transfer functions between system inputs and outputs that represent the impedance behavior of the converter, ratios between input and output currents and voltages, or the converter behavior related to control inputs. The meaning of a specific transfer function can be easily deduced from the corresponding input and output variables.

The linear network models of the VF converters are shown in Fig. 2.1. A voltage-



(a) Voltage-to-voltage converter. **(b)** Voltage-to-current converter.

Fig. 2.1: Linear network models of VF converters.

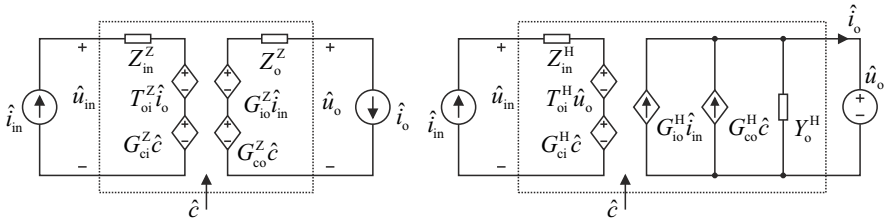
to-voltage converter represents a VF converter loaded with a current sink. The transfer function set of the voltage-to-voltage converter, known by the G-parameters, is given in (2.5) and its equal network model in Fig. 2.1a. The superscript 'G' denotes the G-parameter transfer function. The general control variable $\hat{c}$ represents the duty ratio at open loop and current or voltage reference at closed loop. A vast majority of commercial power supplies are typically fed from a voltage source such as the utility grid or a battery bank and control the converter output voltage. Therefore, they can be represented by the G-parameters.

$$\begin{bmatrix} \hat{i}_{\mathrm{in}} \\ \hat{u}_{\mathrm{o}} \end{bmatrix} = \begin{bmatrix} Y_{\mathrm{in}}^{\mathrm{G}} & T_{\mathrm{oi}}^{\mathrm{G}} & G_{\mathrm{ci}}^{\mathrm{G}} \\ G_{\mathrm{io}}^{\mathrm{G}} & -Z_{\mathrm{o}}^{\mathrm{G}} & G_{\mathrm{co}}^{\mathrm{G}} \end{bmatrix} \begin{bmatrix} \hat{u}_{\mathrm{in}} \\ \hat{i}_{\mathrm{o}} \\ \hat{c} \end{bmatrix} \tag{2.5}$$

A VF converter loaded by a voltage-type load, i.e. a voltage-to-current converter, is represented by the Y-parameters. The Y-parameter transfer-function set is given in (2.6), where the superscript 'Y' denotes the Y-parameter transfer function. The network model of the voltage-to-current converter is shown in Fig. 2.1b. The Y-parameters can be used to describe e.g. the dynamics of a VF battery-charging converter or a grid-connected inverter fed from a voltage source. Castilla et al. (2008, 2009) have used the Y-parameters to represent a grid-connected PV inverter.

$$\begin{bmatrix} \hat{i}_{\mathrm{in}} \\ \hat{i}_{\mathrm{o}} \end{bmatrix} = \begin{bmatrix} Y_{\mathrm{in}}^{\mathrm{Y}} & T_{\mathrm{oi}}^{\mathrm{Y}} & G_{\mathrm{ci}}^{\mathrm{Y}} \\ G_{\mathrm{io}}^{\mathrm{Y}} & -Y_{\mathrm{o}}^{\mathrm{Y}} & G_{\mathrm{co}}^{\mathrm{Y}} \end{bmatrix} \begin{bmatrix} \hat{u}_{\mathrm{in}} \\ \hat{u}_{\mathrm{o}} \\ \hat{c} \end{bmatrix} \tag{2.6}$$

The linear network models of the CF converters are shown in Fig. 2.2. The input-



(a) Current-to-voltage converter. **(b)** Current-to-current converter.

Fig. 2.2: Linear network models of CF converters.

voltage control is the recommended practice in PV applications as discussed earlier, which implies that the models of CF converters have to be used (Leppäaho and Suntio, 2011). The transfer-function set of a current-to-voltage converter represented by the Z-parameters is given in (2.7), where the superscript 'Z' denotes the Z-parameter transfer function. The linear network model of the current-to-voltage converter is shown in Fig. 2.2a. The Z-parameters can be used to describe e.g. the dynamics of a battery-charging PV converter under output-voltage-limiting control (Leppäaho et al., 2010).

$$\begin{bmatrix} \hat{u}_{\mathrm{in}} \\ \hat{u}_{\mathrm{o}} \end{bmatrix} = \begin{bmatrix} Z_{\mathrm{in}}^{\mathrm{Z}} & T_{\mathrm{oi}}^{\mathrm{Z}} & G_{\mathrm{ci}}^{\mathrm{Z}} \\ G_{\mathrm{io}}^{\mathrm{Z}} & -Z_{\mathrm{o}}^{\mathrm{Z}} & G_{\mathrm{co}}^{\mathrm{Z}} \end{bmatrix} \begin{bmatrix} \hat{i}_{\mathrm{in}} \\ \hat{i}_{\mathrm{o}} \\ \hat{c} \end{bmatrix} \tag{2.7}$$

The transfer-function set of a current-to-current converter, represented by the H-parameters, is given in (2.8), where the superscript 'H' denotes the H-parameter transfer function. The network model of the current-to-current converter is given in Fig. 2.2b. The H-parameters can be used to represent a CF converter connected to a voltage-type load, such as the utility grid or a battery bank.

$$\begin{bmatrix} \hat{u}_{\mathrm{in}} \\ \hat{i}_{\mathrm{o}} \end{bmatrix} = \begin{bmatrix} Z_{\mathrm{in}}^{\mathrm{H}} & T_{\mathrm{oi}}^{\mathrm{H}} & G_{\mathrm{ci}}^{\mathrm{H}} \\ G_{\mathrm{io}}^{\mathrm{H}} & -Y_{\mathrm{o}}^{\mathrm{H}} & G_{\mathrm{co}}^{\mathrm{H}} \end{bmatrix} \begin{bmatrix} \hat{i}_{\mathrm{in}} \\ \hat{u}_{\mathrm{o}} \\ \hat{c} \end{bmatrix} \tag{2.8}$$

The H-parametes explicitly describe the dynamic properties of an output-current and input-voltage-controlled grid-connected inverter, and therefore, the transfer functions analyzed later in this thesis are the H-parameters if not otherwise stated. The transfer

functions in (2.8) can be divided into input dynamics composing of

- Z_{in} Input impedance,
- T_{oi} Reverse voltage transfer ratio,
- G_{ci} Control-to-input-voltage transfer function

and output dynamics composing of

- G_{io} Forward current gain,
- Y_{o} Output admittance and
- G_{co} Control-to-output-current transfer function.

The sign in front of the output admittance Y_{o} in (2.8) reflects the adopted direction of the output current $\hat{i}_{\mathrm{o}}$ correcting the phase behavior of the output admittance.

2.2.1 Effect of non-ideal source

The transfer-function sets presented in the previous section describe only the internal dynamics of a converter with an ideal source and load. The effect of a practical source on the converter dynamics can be solved by representing the source subsystem with a similar transfer-function set. An interconnected system composed of the source subsystem 'S' and the converter 'H' representing the load subsystem is shown in Fig. 2.3. The source subsystem could represent e.g. an additional CL-filter connected at the converter input or the PVG. The transfer-function set of the load subsystem is given in (2.9) and the transfer functions of the source subsystem are given in (2.10), respectively.

$$\begin{bmatrix} \hat{u}_{\mathrm{in}} \\ \hat{i}_{\mathrm{o}} \end{bmatrix} = \begin{bmatrix} Z_{\mathrm{in}} & T_{\mathrm{oi}} & G_{\mathrm{ci}} \\ G_{\mathrm{io}} & -Y_{\mathrm{o}} & G_{\mathrm{co}} \end{bmatrix} \begin{bmatrix} \hat{i}_{\mathrm{in}} \\ \hat{u}_{\mathrm{o}} \\ \hat{c} \end{bmatrix} \tag{2.9}$$

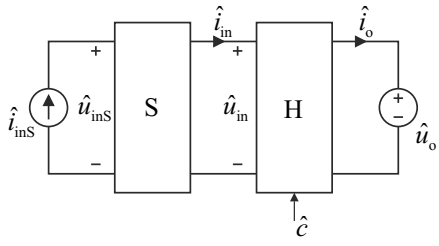


Fig. 2.3: Conversion system consisting of the converter and the source subsystem.

$$\begin{bmatrix} \hat{u}_{\mathrm{inS}} \\ \hat{i}_{\mathrm{in}} \end{bmatrix} = \begin{bmatrix} Z_{\mathrm{in}}^{\mathrm{S}} & T_{\mathrm{oi}}^{\mathrm{S}} \\ G_{\mathrm{io}}^{\mathrm{S}} & -Y_{\mathrm{o}}^{\mathrm{S}} \end{bmatrix} \begin{bmatrix} \hat{i}_{\mathrm{inS}} \\ \hat{u}_{\mathrm{in}} \end{bmatrix} \tag{2.10}$$

Next, the outputs of the interconnected system ($\hat{u}_{\mathrm{in}}$, $\hat{u}_{\mathrm{inS}}$, $\hat{i}_{\mathrm{in}}$ and $\hat{i}_{\mathrm{o}}$) are solved as a function of the inputs of the interconnected system ($\hat{u}_{\mathrm{o}}$, $\hat{i}_{\mathrm{inS}}$ and $\hat{c}$). The converter input voltage $\hat{u}_{\mathrm{in}}$ at the presence of the source subsystem can be solved by substituting $\hat{i}_{\mathrm{in}}$ given in (2.10) into $\hat{u}_{\mathrm{in}}$ given in (2.9) yielding

$$\begin{aligned} \hat{u}_{\mathrm{in}} &= Z_{\mathrm{in}} \left(G_{\mathrm{io}}^{\mathrm{S}} \hat{i}_{\mathrm{inS}} - Y_{\mathrm{o}}^{\mathrm{S}} \hat{u}_{\mathrm{in}} \right) + T_{\mathrm{oi}} \hat{u}_{\mathrm{o}} + G_{\mathrm{ci}} \hat{c} \\ &= \frac{Z_{\mathrm{in}} G_{\mathrm{io}}^{\mathrm{S}}}{1 + Z_{\mathrm{in}} Y_{\mathrm{o}}^{\mathrm{S}}} \hat{i}_{\mathrm{inS}} + \frac{T_{\mathrm{oi}}}{1 + Z_{\mathrm{in}} Y_{\mathrm{o}}^{\mathrm{S}}} \hat{u}_{\mathrm{o}} + \frac{G_{\mathrm{ci}}}{1 + Z_{\mathrm{in}} Y_{\mathrm{o}}^{\mathrm{S}}} \hat{c}. \end{aligned} \tag{2.11}$$

The input voltage of the source subsystem $\hat{u}_{\mathrm{inS}}$ can be solved by substituting $\hat{u}_{\mathrm{in}}$ in (2.11) into $\hat{u}_{\mathrm{inS}}$ given in (2.10) yielding

$$\begin{aligned} \hat{u}_{\mathrm{inS}} &= Z_{\mathrm{in}}^{\mathrm{S}} \hat{i}_{\mathrm{inS}} + T_{\mathrm{oi}}^{\mathrm{S}} \left(\frac{Z_{\mathrm{in}} G_{\mathrm{io}}^{\mathrm{S}}}{1 + Z_{\mathrm{in}} Y_{\mathrm{o}}^{\mathrm{S}}} \hat{i}_{\mathrm{inS}} + \frac{T_{\mathrm{oi}}}{1 + Z_{\mathrm{in}} Y_{\mathrm{o}}^{\mathrm{S}}} \hat{u}_{\mathrm{o}} \frac{G_{\mathrm{ci}}}{1 + Z_{\mathrm{in}} Y_{\mathrm{o}}^{\mathrm{S}}} \hat{c} \right) \\ &= \frac{1 + Z_{\mathrm{in}} Y_{\mathrm{o\text{-}sci}}^{\mathrm{S}}}{1 + Y_{\mathrm{o}}^{\mathrm{S}} Z_{\mathrm{in}}} Z_{\mathrm{in}}^{\mathrm{S}} \hat{i}_{\mathrm{inS}} + \frac{T_{\mathrm{oi}}^{\mathrm{S}}}{1 + Y_{\mathrm{o}}^{\mathrm{S}} Z_{\mathrm{in}}} T_{\mathrm{oi}} \hat{u}_{\mathrm{o}} + \frac{T_{\mathrm{oi}}^{\mathrm{S}}}{1 + Y_{\mathrm{o}}^{\mathrm{S}} Z_{\mathrm{in}}} G_{\mathrm{ci}} \hat{c}, \end{aligned} \tag{2.12}$$

where

$$Y_{\mathrm{o\text{-}sci}}^{\mathrm{S}} = Y_{\mathrm{o}}^{\mathrm{S}} + \frac{G_{\mathrm{io}}^{\mathrm{S}} T_{\mathrm{oi}}^{\mathrm{S}}}{Z_{\mathrm{in}}^{\mathrm{S}}}, \tag{2.13}$$

which denotes the admittance characteristics of the source subsystem output port when its input port is short-circuited. The output current of the source subsystem, i.e. the converter input current, $\hat{i}_{\mathrm{in}}$ can be solved by substituting $\hat{u}_{\mathrm{in}}$ in (2.11) into $\hat{i}_{\mathrm{in}}$ given in (2.10) yielding

$$\begin{aligned} \hat{i}_{\mathrm{in}} &= G_{\mathrm{io}}^{\mathrm{S}} \hat{i}_{\mathrm{inS}} - Y_{\mathrm{o}}^{\mathrm{S}} \left(\frac{Z_{\mathrm{in}} G_{\mathrm{io}}^{\mathrm{S}}}{1 + Z_{\mathrm{in}} Y_{\mathrm{o}}^{\mathrm{S}}} \hat{i}_{\mathrm{inS}} + \frac{T_{\mathrm{oi}}}{1 + Z_{\mathrm{in}} Y_{\mathrm{o}}^{\mathrm{S}}} \hat{u}_{\mathrm{o}} + \frac{G_{\mathrm{ci}}}{1 + Z_{\mathrm{in}} Y_{\mathrm{o}}^{\mathrm{S}}} \hat{c} \right) \\ &= \frac{1}{1 + Y_{\mathrm{o}}^{\mathrm{S}} Z_{\mathrm{in}}} G_{\mathrm{io}}^{\mathrm{S}} \hat{i}_{\mathrm{inS}} - \frac{Y_{\mathrm{o}}^{\mathrm{S}}}{1 + Y_{\mathrm{o}}^{\mathrm{S}} Z_{\mathrm{in}}} T_{\mathrm{oi}} \hat{u}_{\mathrm{o}} - \frac{Y_{\mathrm{o}}^{\mathrm{S}}}{1 + Y_{\mathrm{o}}^{\mathrm{S}} Z_{\mathrm{in}}} G_{\mathrm{ci}} \hat{c}. \end{aligned} \tag{2.14}$$

The converter output current $\hat{i}_{\mathrm{o}}$ at the presence of the source subsystem can be solved

by substituting the converter input current $\hat{i}_{\mathrm{in}}$ in (2.14) into $\hat{i}_{\mathrm{o}}$ given in (2.9) yielding

$$\begin{aligned}\hat{i}_{\mathrm{o}} =& G_{\mathrm{io}}\left(\frac{1}{1+Y_{\mathrm{o}}^{\mathrm{S}}Z_{\mathrm{in}}}G_{\mathrm{io}}^{\mathrm{S}}\hat{i}_{\mathrm{inS}} - \frac{Y_{\mathrm{o}}^{\mathrm{S}}}{1+Y_{\mathrm{o}}^{\mathrm{S}}Z_{\mathrm{in}}}T_{\mathrm{oi}}\hat{u}_{\mathrm{o}} - \frac{Y_{\mathrm{o}}^{\mathrm{S}}}{1+Y_{\mathrm{o}}^{\mathrm{S}}Z_{\mathrm{in}}}G_{\mathrm{ci}}\hat{c}\right)\\ &- Y_{\mathrm{o}}\hat{u}_{\mathrm{o}} + G_{\mathrm{co}}\hat{c} \\ =& \frac{G_{\mathrm{io}}^{\mathrm{S}}}{1+Y_{\mathrm{o}}^{\mathrm{S}}Z_{\mathrm{in}}}G_{\mathrm{io}}\hat{i}_{\mathrm{inS}} - \frac{1+Y_{\mathrm{o}}^{\mathrm{S}}Z_{\text{in-oco}}}{1+Y_{\mathrm{o}}^{\mathrm{S}}Z_{\mathrm{in}}}Y_{\mathrm{o}}\hat{u}_{\mathrm{o}} + \frac{1+Y_{\mathrm{o}}^{\mathrm{S}}Z_{\text{in-}\infty}}{1+Y_{\mathrm{o}}^{\mathrm{S}}Z_{\mathrm{in}}}G_{\mathrm{co}}\hat{c},\end{aligned} \tag{2.15}$$

where

$$Z_{\text{in-oco}} = Z_{\mathrm{in}} + \frac{T_{\mathrm{oi}}G_{\mathrm{io}}}{Y_{\mathrm{o}}}, \tag{2.16}$$

$$Z_{\text{in-}\infty} = Z_{\mathrm{in}} - \frac{G_{\mathrm{io}}G_{\mathrm{ci}}}{G_{\mathrm{co}}}. \tag{2.17}$$

The impedance $Z_{\text{in-oco}}$ in (2.16) denotes the impedance characteristics of the converter input port when the output port of the converter is open-circuited. The impedance $Z_{\text{in-}\infty}$ in (2.17) denotes certain ideal input impedance.

The source-affected transfer functions given in (2.11)-(2.17) are best suited to model the effect of a source that has series-impedance terms in addition to parallel impedances (i.e. $\hat{u}_{\mathrm{inS}} \neq \hat{u}_{\mathrm{in}}$) and the input voltage of the source subsystem ($\hat{u}_{\mathrm{inS}}$) is available as a feedback variable, e.g. if the input voltage of an additional CL-type filter connected at the converter input terminals is controlled. Typically, only the output port of the source subsystem can be measured. In such a case, the source subsystem is best represented as a Norton equivalent circuit composed of the current source $\hat{i}_{\mathrm{inS}}$ and its internal admittance Y_{S} as shown in Fig. 2.4. The input current $\hat{i}_{\mathrm{in}}$ can be solved from Fig. 2.4 as

$$\hat{i}_{\mathrm{in}} = \hat{i}_{\mathrm{inS}} - Y_{\mathrm{S}}\hat{u}_{\mathrm{in}}, \tag{2.18}$$

which substituted into the nominal converter dynamics given in (2.9) yields the source-affected H-parameters given in (2.19), when the source is assumed to consist of the Norton

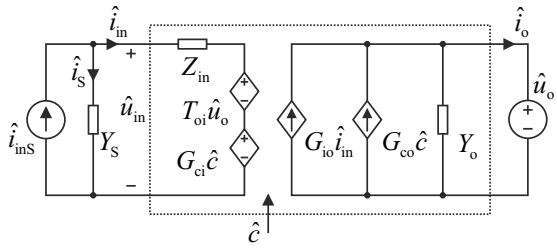


Fig. 2.4: H-parameter network with nonideal source admittance.

equivalent circuit.

$$\begin{bmatrix} \hat{u}_{\mathrm{in}} \\ \hat{i}_{\mathrm{o}} \end{bmatrix} = \begin{bmatrix} \dfrac{Z_{\mathrm{in}}}{1+Y_{\mathrm{S}}Z_{\mathrm{in}}} & \dfrac{T_{\mathrm{oi}}}{1+Y_{\mathrm{S}}Z_{\mathrm{in}}} & \dfrac{G_{\mathrm{ci}}}{1+Y_{\mathrm{S}}Z_{\mathrm{in}}} \\ \dfrac{G_{\mathrm{io}}}{1+Y_{\mathrm{S}}Z_{\mathrm{in}}} & -\dfrac{1+Y_{\mathrm{S}}Z_{\mathrm{in\text{-}oco}}}{1+Y_{\mathrm{S}}Z_{\mathrm{in}}}Y_{\mathrm{o}} & \dfrac{1+Y_{\mathrm{S}}Z_{\mathrm{in\text{-}}\infty}}{1+Y_{\mathrm{S}}Z_{\mathrm{in}}}G_{\mathrm{co}} \end{bmatrix} \begin{bmatrix} \hat{i}_{\mathrm{inS}} \\ \hat{u}_{\mathrm{o}} \\ \hat{c} \end{bmatrix} \tag{2.19}$$

2.2.2 Effect of non-ideal load

The effect of a nonideal load on the converter dynamics is solved similarly to the effect of the nonideal source. The interconnected system consisting of the converter 'H' and the load subsystem 'L' is shown in Fig. 2.5. The load subsystem could represent e.g. a CL-type output filter or the utility grid. The transfer functions of the load subsystem are given in (2.20) and the transfer functions of the converter are the same transfer functions as given earlier in (2.9).

$$\begin{bmatrix} \hat{u}_{\mathrm{o}} \\ \hat{i}_{\mathrm{oL}} \end{bmatrix} = \begin{bmatrix} Z_{\mathrm{in}}^{\mathrm{L}} & T_{\mathrm{oi}}^{\mathrm{L}} \\ G_{\mathrm{io}}^{\mathrm{L}} & -Y_{\mathrm{o}}^{\mathrm{L}} \end{bmatrix} \begin{bmatrix} \hat{i}_{\mathrm{o}} \\ \hat{u}_{\mathrm{oL}} \end{bmatrix} \tag{2.20}$$

Next, the outputs of the interconnected system ($\hat{u}_{\mathrm{in}}$, $\hat{u}_{\mathrm{o}}$, $\hat{i}_{\mathrm{o}}$ and $\hat{i}_{\mathrm{oL}}$) are solved as a function of the inputs of the interconnected system ($\hat{u}_{\mathrm{oL}}$, $\hat{i}_{\mathrm{in}}$ and $\hat{c}$). First, the input voltage of the load subsystem, i.e. the output voltage of the converter, $\hat{u}_{\mathrm{o}}$ given in (2.20), is substituted into the converter output current $\hat{i}_{\mathrm{o}}$ given in (2.9) yielding

$$\begin{aligned} \hat{i}_{\mathrm{o}} &= G_{\mathrm{io}}\hat{i}_{\mathrm{in}} - Y_{\mathrm{o}}\left(Z_{\mathrm{in}}^{\mathrm{L}}\hat{i}_{\mathrm{o}} + T_{\mathrm{oi}}^{\mathrm{L}}\hat{u}_{\mathrm{o}}\right) + G_{\mathrm{co}}\hat{c} \\ &= \frac{G_{\mathrm{io}}}{1+Z_{\mathrm{in}}^{\mathrm{L}}Y_{\mathrm{o}}}\hat{i}_{\mathrm{in}} - \frac{T_{\mathrm{oi}}^{\mathrm{L}}Y_{\mathrm{o}}}{1+Z_{\mathrm{in}}^{\mathrm{L}}Y_{\mathrm{o}}}\hat{u}_{\mathrm{oL}} + \frac{G_{\mathrm{co}}}{1+Z_{\mathrm{in}}^{\mathrm{L}}Y_{\mathrm{o}}}\hat{c}. \end{aligned} \tag{2.21}$$

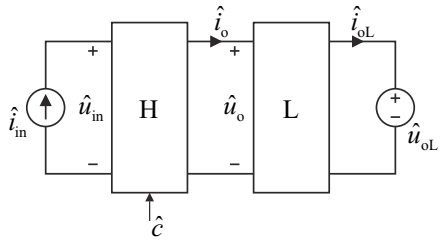


Fig. 2.5: Conversion system consisting of source and load subsystems.

The converter output current $\hat{i}_{\mathrm{o}}$ in (2.21) is then substituted into $\hat{u}_{\mathrm{o}}$ given in (2.20) yielding

$$\begin{aligned}\hat{u}_{\mathrm{o}} &= Z_{\mathrm{in}}^{\mathrm{L}}\left(\frac{G_{\mathrm{io}}}{1+Z_{\mathrm{in}}^{\mathrm{L}}Y_{\mathrm{o}}}\hat{i}_{\mathrm{in}} - \frac{T_{\mathrm{oi}}^{\mathrm{L}}Y_{\mathrm{o}}}{1+Z_{\mathrm{in}}^{\mathrm{L}}Y_{\mathrm{o}}}\hat{u}_{\mathrm{oL}} + \frac{G_{\mathrm{co}}}{1+Z_{\mathrm{in}}^{\mathrm{L}}Y_{\mathrm{o}}}\hat{c}\right) + T_{\mathrm{oi}}^{\mathrm{L}}\hat{u}_{\mathrm{oL}} \\ &= \frac{Z_{\mathrm{in}}^{\mathrm{L}}G_{\mathrm{io}}}{1+Z_{\mathrm{in}}^{\mathrm{L}}Y_{\mathrm{o}}}\hat{i}_{\mathrm{in}} + \frac{T_{\mathrm{oi}}^{\mathrm{L}}}{1+Z_{\mathrm{in}}^{\mathrm{L}}Y_{\mathrm{o}}}\hat{u}_{\mathrm{oL}} + \frac{Z_{\mathrm{in}}^{\mathrm{L}}G_{\mathrm{co}}}{1+Z_{\mathrm{in}}^{\mathrm{L}}Y_{\mathrm{o}}}\hat{c}.\end{aligned} \tag{2.22}$$

The converter input voltage $\hat{u}_{\mathrm{in}}$ at the presence of the load subsystem can be solved by substituting $\hat{u}_{\mathrm{o}}$ in (2.22) into $\hat{u}_{\mathrm{in}}$ given in (2.9) yielding

$$\begin{aligned}\hat{u}_{\mathrm{in}} &= Z_{\mathrm{in}}\hat{i}_{\mathrm{in}} + T_{\mathrm{oi}}\left(\frac{Z_{\mathrm{in}}^{\mathrm{L}}G_{\mathrm{io}}}{1+Z_{\mathrm{in}}^{\mathrm{L}}Y_{\mathrm{o}}}\hat{i}_{\mathrm{in}} + \frac{T_{\mathrm{oi}}^{\mathrm{L}}}{1+Z_{\mathrm{in}}^{\mathrm{L}}Y_{\mathrm{o}}}\hat{u}_{\mathrm{oL}} + \frac{Z_{\mathrm{in}}^{\mathrm{L}}G_{\mathrm{co}}}{1+Z_{\mathrm{in}}^{\mathrm{L}}Y_{\mathrm{o}}}\hat{c}\right) + G_{\mathrm{ci}}\hat{c} \\ &= \frac{1+Z_{\mathrm{in}}^{\mathrm{L}}Y_{\text{o-sci}}}{1+Z_{\mathrm{in}}^{\mathrm{L}}Y_{\mathrm{o}}}Z_{\mathrm{in}}\hat{i}_{\mathrm{in}} + \frac{T_{\mathrm{oi}}^{\mathrm{L}}T_{\mathrm{oi}}}{1+Z_{\mathrm{in}}^{\mathrm{L}}Y_{\mathrm{o}}}\hat{u}_{\mathrm{oL}} + \frac{1+Z_{\mathrm{in}}^{\mathrm{L}}Y_{\text{o-}\infty}}{1+Z_{\mathrm{in}}^{\mathrm{L}}Y_{\mathrm{o}}}G_{\mathrm{ci}}\hat{c},\end{aligned} \tag{2.23}$$

where

$$Y_{\text{o-sci}} = Y_{\mathrm{o}} + \frac{T_{\mathrm{oi}}G_{\mathrm{io}}}{Z_{\mathrm{in}}}, \tag{2.24}$$

$$Y_{\text{o-}\infty} = Y_{\mathrm{o}} + \frac{T_{\mathrm{oi}}G_{\mathrm{co}}}{G_{\mathrm{ci}}}. \tag{2.25}$$

The admittance $Y_{\text{o-sci}}$ in (2.24) denotes the admittance characteristics of the converter output port when the input port of the converter is short-circuited and the admittance $Y_{\text{o-}\infty}$ in (2.25) denotes ideal output admittance. The output current of the load subsystem is solved by substituting $\hat{i}_{\mathrm{o}}$ in (2.21) into $\hat{i}_{\mathrm{oL}}$ given in (2.20) yielding

$$\begin{aligned}\hat{i}_{\mathrm{oL}} &= G_{\mathrm{io}}^{\mathrm{L}}\left(\frac{G_{\mathrm{io}}}{1+Z_{\mathrm{in}}^{\mathrm{L}}Y_{\mathrm{o}}}\hat{i}_{\mathrm{in}} - \frac{T_{\mathrm{oi}}^{\mathrm{L}}Y_{\mathrm{o}}}{1+Z_{\mathrm{in}}^{\mathrm{L}}Y_{\mathrm{o}}}\hat{u}_{\mathrm{oL}} + \frac{G_{\mathrm{co}}}{1+Z_{\mathrm{in}}^{\mathrm{L}}Y_{\mathrm{o}}}\hat{c}\right) - Y_{\mathrm{o}}^{\mathrm{L}}\hat{u}_{\mathrm{oL}} \\ &= \frac{G_{\mathrm{io}}^{\mathrm{L}}G_{\mathrm{io}}}{1+Z_{\mathrm{in}}^{\mathrm{L}}Y_{\mathrm{o}}}\hat{i}_{\mathrm{in}} - \frac{1+Y_{\mathrm{o}}Z_{\text{in-oco}}^{\mathrm{L}}}{1+Z_{\mathrm{in}}^{\mathrm{L}}Y_{\mathrm{o}}}Y_{\mathrm{o}}^{\mathrm{L}}\hat{u}_{\mathrm{oL}} + \frac{G_{\mathrm{io}}^{\mathrm{L}}G_{\mathrm{co}}}{1+Z_{\mathrm{in}}^{\mathrm{L}}Y_{\mathrm{o}}}\hat{c},\end{aligned} \tag{2.26}$$

where

$$Z_{\text{in-oco}}^{\mathrm{L}} = Z_{\mathrm{in}}^{\mathrm{L}} + \frac{G_{\mathrm{io}}^{\mathrm{L}}T_{\mathrm{oi}}^{\mathrm{L}}}{Y_{\mathrm{o}}^{\mathrm{L}}}, \tag{2.27}$$

which denotes the impedance characteristics of the load subsystem input port when its output port is open-circuited.

The load-affected transfer functions given in (2.21)-(2.27) are best suited to describe a situation where the load subsystem consists of parallel-impedance terms in addition to series impedances (i.e. $\hat{i}_{\mathrm{oL}} \neq \hat{i}_{\mathrm{o}}$) and the output current of the load subsystem is available

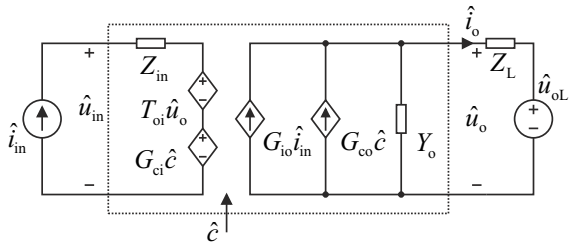


Fig. 2.6: H-parameter network with nonideal load impedance.

as a feedback variable. Such a case could be e.g. a CL-type filter connected at the output terminals of a VSI-type inverter forming a typical LCL configuration, where the grid-side current is used as a feedback variable. However, typically only the input terminals of the load subsystem are available for measurements. In such a case, a Thevenin equivalent circuit composed of the load voltage $\hat{u}_{\mathrm{oL}}$ and a series load impedance Z_{L} as shown in Fig. 2.6 is best suited to model the load effect. The output voltage $\hat{u}_{\mathrm{o}}$ can be solved from Fig. 2.6 by

$$\hat{u}_{\mathrm{o}} = Z_{\mathrm{L}}\hat{i}_{\mathrm{o}} + \hat{u}_{\mathrm{oL}}, \tag{2.28}$$

which substituted into the nominal converter dynamics in (2.9) yields the load-affected H-parameters given in (2.29), when the load is assumed to be the Thevenin equivalent circuit.

$$\begin{bmatrix} \hat{u}_{\mathrm{in}} \\ \hat{i}_{\mathrm{o}} \end{bmatrix} = \begin{bmatrix} \dfrac{1+Z_{\mathrm{L}}Y_{\mathrm{o\text{-}sci}}}{1+Z_{\mathrm{L}}Y_{\mathrm{o}}}Z_{\mathrm{in}} & \dfrac{T_{\mathrm{oi}}}{1+Z_{\mathrm{L}}Y_{\mathrm{o}}} & \dfrac{1+Z_{\mathrm{L}}Y_{\mathrm{o\text{-}\infty}}}{1+Z_{\mathrm{L}}Y_{\mathrm{o}}}G_{\mathrm{ci}} \\ \dfrac{G_{\mathrm{io}}}{1+Z_{\mathrm{L}}Y_{\mathrm{o}}} & -\dfrac{Y_{\mathrm{o}}}{1+Z_{\mathrm{L}}Y_{\mathrm{o}}} & \dfrac{G_{\mathrm{co}}}{1+Z_{\mathrm{L}}Y_{\mathrm{o}}} \end{bmatrix} \begin{bmatrix} \hat{i}_{\mathrm{in}} \\ \hat{u}_{\mathrm{oL}} \\ \hat{c} \end{bmatrix} \tag{2.29}$$

2.3 Stability assessment of interconnected electrical systems

It is known that the stability of an interconnected electrical system can be determined by applying the Nyquist stability criterion to the impedance ratio of the load and source subsystems (Middlebrook, 1976; Suntio, 2009). Such an interconnected system composed of the source subsystem S and the load subsystem L is shown in Fig. 2.7. The subsystems may be arbitrary electrical systems in such a way that the output port of the source subsystem and the input port of the load subsystem are duals of each other, i.e. either current/voltage or voltage/current, because the parallel connection of voltage sources or the series connection of current sources are not allowed according to the circuit theory.

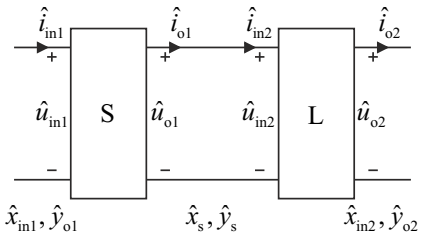


Fig. 2.7: An interconnected electrical system.

The input variables of the interconnected system are denoted by $\hat{x}_{\text{in1}}$ and $\hat{x}_{\text{in2}}$, the output variables are denoted by $\hat{y}_{\text{o1}}$ and $\hat{y}_{\text{o2}}$ and the intermediate variables are denoted by $\hat{x}_{\text{s}}$ and $\hat{y}_{\text{s}}$. The intermediate variables are chosen in such a way that $\hat{x}_{\text{s}}$ is an output variable of the load subsystem at the source side and an input variable of the source subsystem at the load side and $\hat{y}_{\text{s}}$ is an output variable of the source subsystem at the load side and an input variable of the load subsystem at the source side. According to the selection of the system variables, the source subsystem can be presented as defined in (2.30) and the load subsystem as defined in (2.31).

$$\begin{bmatrix} \hat{y}_{\text{o1}} \\ \hat{y}_{\text{s}} \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & -S_{22} \end{bmatrix} \begin{bmatrix} \hat{x}_{\text{in1}} \\ \hat{x}_{\text{s}} \end{bmatrix} \tag{2.30}$$

$$\begin{bmatrix} \hat{x}_{\text{s}} \\ \hat{y}_{\text{o2}} \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} \\ L_{21} & -L_{22} \end{bmatrix} \begin{bmatrix} \hat{y}_{\text{s}} \\ \hat{x}_{\text{in2}} \end{bmatrix} \tag{2.31}$$

The internal and input-output stabilities can be studied by constructing the mappings from the system input variables to the intermediate variables and to the system output variables. First, $\hat{y}_{\text{s}}$ given in (2.30) is substituted into $\hat{x}_{\text{s}}$ given in (2.31) and then $\hat{x}_{\text{s}}$ is substituted into $\hat{y}_{\text{s}}$ yielding the mapping between the system inputs and the intermediate variables as given in (2.32). The mapping between the system inputs and outputs can be calculated by substituting $\hat{x}_{\text{s}}$ given in (2.32) into $\hat{y}_{\text{o1}}$ given in (2.30) and by substituting $\hat{y}_{\text{s}}$ given in (2.32) into $\hat{y}_{\text{o2}}$ given in (2.31) yielding (2.33).

$$\begin{bmatrix} \hat{x}_{\text{s}} \\ \hat{y}_{\text{s}} \end{bmatrix} = \begin{bmatrix} \dfrac{S_{21}L_{11}}{1+S_{22}L_{11}} & \dfrac{L_{12}}{1+S_{22}L_{11}} \\ \dfrac{S_{21}}{1+S_{22}L_{11}} & -\dfrac{S_{22}L_{12}}{1+S_{22}L_{11}} \end{bmatrix} \begin{bmatrix} \hat{x}_{\text{in1}} \\ \hat{x}_{\text{in2}} \end{bmatrix} \tag{2.32}$$

$$\begin{bmatrix} \hat{y}_{o1} \\ \hat{y}_{o2} \end{bmatrix} = \begin{bmatrix} \dfrac{1+L_{11}\left(S_{22}+\dfrac{S_{12}S_{21}}{S_{11}}\right)}{1+S_{22}L_{11}}S_{11} & \dfrac{S_{12}L_{12}}{1+S_{22}L_{11}} \\ \dfrac{S_{21}L_{21}}{1+S_{22}L_{11}} & -\dfrac{1+S_{22}\left(L_{11}+\dfrac{L_{12}L_{21}}{L_{22}}\right)}{1+S_{22}L_{11}}L_{22} \end{bmatrix} \begin{bmatrix} \hat{x}_{in1} \\ \hat{x}_{in2} \end{bmatrix} \quad (2.33)$$

For stability to exist, all the transfer functions have to be stable, i.e. their poles must be located on the left half of the complex plane. Assuming that the original subsystems S and L as independent stand-alone subsystems are stable, the stability of the interconnected system is dependent according to (2.32) and (2.33) on the stability of $1/(1+S_{22}L_{11})$, which can be verified by applying the Nyquist stability criterion to $S_{22}L_{11}$. According to Section 2.2, in case of VF interfacing $S_{22}L_{11}$ equals to Z_{o}^{S}/Z_{in}^{L}, which is the famous minor-loop gain (Middlebrook, 1976), where Z_{o}^{S} is the output impedance of the source subsystem and Z_{in}^{L} is the input impedance of the load subsystem. In case of CF interfacing, $S_{22}L_{11}$ equals to Z_{in}^{L}/Z_{o}^{S}, which is the inverse of the minor-loop gain (Leppäaho et al., 2011).

The boundary for instability is the condition in which the impedances of the load and source subsystems are equal with 180° phase difference, i.e. $S_{22}L_{11} = -1$, where the system poles are located at the imaginary axis of the complex plane and the system may oscillate at the frequency where the boundary condition is valid. If both the source and load subsystems have passive-circuit-like behavior, the violation of the stability criterion needs undamped source and load subsystems which do not exist in practice. Therefore, the stability of an interface is compromised if one of the subsystems has the property of negative incremental resistance, which is a possible property of a switching converter operated under feedback control (Suntio, 2009).

2.4 Dynamic model of a photovoltaic generator

The static characteristics of a PVG were represented in Section 1.2. The dynamic behavior of a PVG is determined by non-linear dynamic resistance r_{pv} and capacitance c_{pv} (Kumar et al., 2006; Mäki et al., 2010; Recart and Cuevas, 2006; Thongrpon et al., 2006). Fig. 2.8 shows a single-diode model of a PVG incorporating the additional dynamic capacitance compared to the single-diode model in Fig. 1.1. The relation between diode current i_d and voltage u_d can be modeled with an exponential equation, yielding a non-linear resistance r_d that can be used instead of the diode-symbol in Fig. 2.8 (Chenvidhya et al., 2005; Liu and Dougal, 2002). The measured static and dynamic characteristics of a PV module are shown in Fig. 2.9 as normalized (p.u.) values. The measurement setup

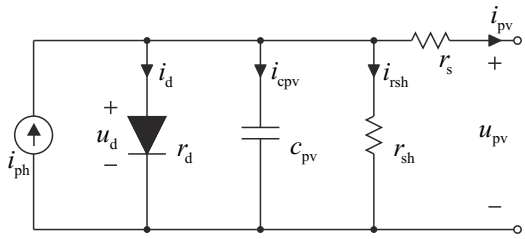


Fig. 2.8: Simplified electrical equivalent model of a photovoltaic cell.

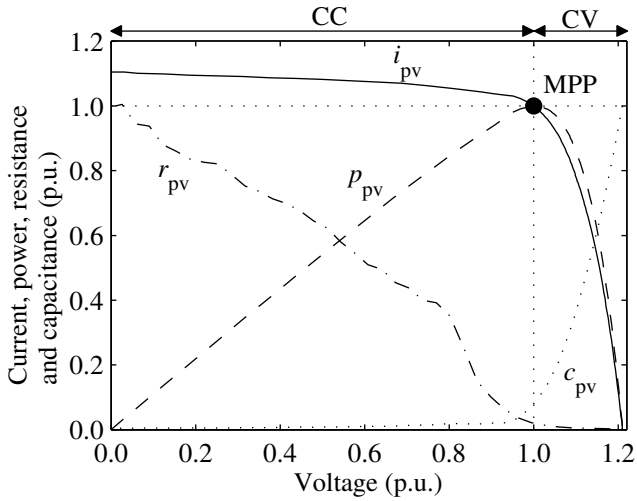


Fig. 2.9: Static and dynamic terminal behavior of a PVG.

has been reported earlier in detail in (Mäki et al., 2010).

The dynamic behavior of the PVG is shown in Fig. 2.9 in terms of its dynamic resistance $r_{\mathrm{pv}} = r_{\mathrm{d}} || r_{\mathrm{sh}} + r_{\mathrm{s}}$ and capacitance c_{pv}, which are non-linear and dependent on the operating point. The dynamic resistance represents the low-frequency value of the PVG impedance and is the single most important variable that has effect on the interfacing converter dynamics. The magnitude of the dynamic resistance supports the fact that the PVG has the characteristics of a current source at voltages lower than the MPP, i.e. in the constant current (CC) region (CCR). In the CCR, the internal impedance of the PVG is high, whereas the internal impedance of an ideal current source is infinite. On the other hand, the PVG impedance is low at voltages higher than the MPP voltage, i.e. in the constant voltage (CV) region (CVR), whereas the internal impedance of an ideal voltage source is zero.

The voltage derivative of the PVG power at an arbitrary operating point can be given

by

$$\frac{\mathrm{d}p_{\mathrm{pv}}}{\mathrm{d}u_{\mathrm{pv}}} = \frac{\mathrm{d}(u_{\mathrm{pv}}i_{\mathrm{pv}})}{\mathrm{d}u_{\mathrm{pv}}} = I_{\mathrm{pv}} + U_{\mathrm{pv}}\frac{\mathrm{d}i_{\mathrm{pv}}}{\mathrm{d}u_{\mathrm{pv}}} \approx I_{\mathrm{pv}} + U_{\mathrm{pv}}\frac{\Delta i_{\mathrm{pv}}}{\Delta u_{\mathrm{pv}}}, \tag{2.34}$$

where I_{pv} and U_{pv} are the PVG-operating-point current and voltage. The maximum power of a PVG is obtained when the power derivative is zero, and therefore the static PVG resistance denoted by $R_{\mathrm{pv}} = U_{\mathrm{pv}}/I_{\mathrm{pv}}$ and the dynamic resistance $r_{\mathrm{pv}} = -\Delta i_{\mathrm{pv}}/\Delta u_{\mathrm{pv}}$ coincide at the MPP as implied also by the maximum power transfer theorem (Wyatt and Chua, 1983). According to Kirchhoff's laws, the analyzed or measured output impedance of a device is $-Z_{\mathrm{o}}$, if the direction of the positive current flow is defined out of the device as in Figs. 2.8 and 2.9. Thus, the dynamic resistance r_{pv} (or the incremental resistance as named by Thongrpon et al.) is in fact positive since $\Delta u_{\mathrm{pv}}/\Delta i_{\mathrm{pv}}$ in Fig. 2.9 is negative and has to be multiplied by '-1' to obtain the correct impedance.

The operating-point-dependent dynamic effect of a PVG can be taken into account by considering the source as a parallel connection of a current source i_{inS} and source admittance Y_{S} as in Section 2.2.1. According to Fig. 2.8, PVG impedance behaves as an RC-circuit, which is true if the self-inductance of the current path is neglected. This is justified because the system is modeled only up to half the switching frequency of the converter and the interconnection wires used are relatively short. The source impedance Z_{S} can be given according to Fig. 2.8 by

$$Z_{\mathrm{S}} = r_{\mathrm{s}} + r_{\mathrm{d}}||r_{\mathrm{sh}}||\frac{1}{sc_{\mathrm{pv}}} = \frac{\overbrace{r_{\mathrm{s}} + r_{\mathrm{d}}||r_{\mathrm{sh}}}^{r_{\mathrm{pv}}} + sc_{\mathrm{pv}}r_{\mathrm{s}}\left(r_{\mathrm{d}}||r_{\mathrm{sh}}\right)}{1 + sc_{\mathrm{pv}}r_{\mathrm{s}}\left(r_{\mathrm{d}}||r_{\mathrm{sh}}\right)}, \tag{2.35}$$

which can be approximated by considering $r_{\mathrm{s}} = 0$ and $r_{\mathrm{pv}} = r_{\mathrm{d}}||r_{\mathrm{sh}} + r_{\mathrm{s}}$ as

$$Z_{\mathrm{S}} \approx r_{\mathrm{d}}||r_{\mathrm{sh}}||\frac{1}{sc_{\mathrm{pv}}} \approx r_{\mathrm{pv}}||\frac{1}{sc_{\mathrm{pv}}}, \tag{2.36}$$

and further at low frequencies by

$$Z_{\mathrm{S}} \approx r_{\mathrm{pv}}. \tag{2.37}$$

The use of (2.37) instead of (2.36) is justified if the interfacing-converter input capacitance $C >> c_{\mathrm{pv}}$, which applies in a single-phase inverter due to the need for the large power decoupling capacitor. If the converter input capacitance and the dynamic capacitance of the PVG are in the same order of magnitude, the dynamic capacitance can influence the converter dynamics. According to Mäki et al. (2010), the dynamic capacitance of a single PV module can be in the order of a few microfarads and is highest at

the open circuit as shown in Fig. 2.9.

It can be deduced from (2.35) that the PVG impedance has passive-circuit-like characteristics, i.e., its phase lies between $\pm 90°$. Therefore, according to Section 2.3, instability of the PVG/converter interface requires that the input-port of the interfacing converter has the properties of the negative incremental resistance (i.e., its phase $> 90°$).

2.5 Dynamic model of a current-fed VSI-type converter

The VSI-type inverter also presented earlier is shown in Fig. 2.10 with relevant parasitic resistances of the power-stage components. The converter is operated in such a way that the switch S_1 conducts during the on-time and the switch S_2 is off. The on-time subcircuit of the VSI-type converter is shown in Fig. 2.11a. During the off-time the switch S_1 is off and the switch S_2 is conducting as shown in Fig. 2.11b. The VSI-type converter is derived from a buck converter with an additional input capacitor (Leppäaho et al., 2010).

The average state-space of the converter can be obtained by solving the derivatives of the inductor current and capacitor voltage as well as the input voltage and output current during the on- and off-times according to Kirchhoffs' laws and applying averaging over one switching cycle. Denoting the duty ratio by d and the complement of the duty ratio by $d' = 1 - d$ and carrying out the aforementioned procedures yields the average

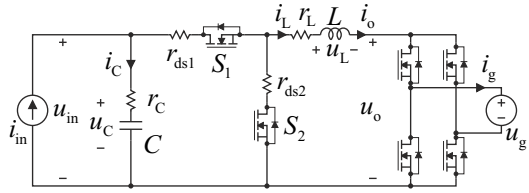
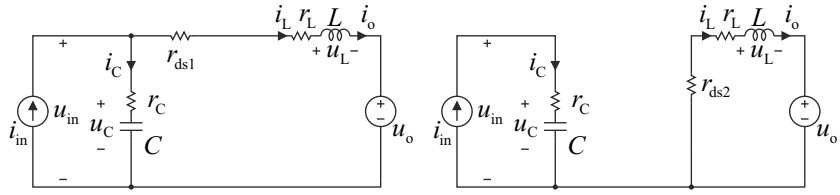


Fig. 2.10: VSI-type CF inverter.



(a) On-time. **(b)** Off-time.

Fig. 2.11: VSI-type converter during on- and off-times.

state-space of the VSI-type converter as given in (2.38).

$$\begin{aligned}
\frac{\mathrm{d}\langle i_\mathrm{L}\rangle}{\mathrm{d}t} &= \frac{\langle d\rangle}{L}\langle u_\mathrm{C}\rangle - \frac{r_\mathrm{L}+\langle d\rangle(r_\mathrm{C}+r_\mathrm{ds1})+d'r_\mathrm{ds2}}{L}\langle i_\mathrm{L}\rangle + \frac{dr_\mathrm{C}}{L}\langle i_\mathrm{in}\rangle - \frac{1}{L}\langle u_\mathrm{o}\rangle \\
\frac{\mathrm{d}\langle u_\mathrm{C}\rangle}{\mathrm{d}t} &= -\frac{\langle d\rangle}{C}\langle i_\mathrm{L}\rangle + \frac{1}{C}\langle i_\mathrm{in}\rangle \\
\langle u_\mathrm{in}\rangle &= \langle u_\mathrm{C}\rangle - \langle d\rangle r_\mathrm{C}\langle i_\mathrm{L}\rangle + r_\mathrm{C}\langle i_\mathrm{in}\rangle = \left(1+r_\mathrm{C}C\frac{\mathrm{d}}{\mathrm{d}t}\right)\langle u_\mathrm{C}\rangle \\
\langle i_\mathrm{o}\rangle &= \langle i_\mathrm{L}\rangle
\end{aligned} \tag{2.38}$$

In order to maintain flux linkage and charge balances, the average voltages accross the inductors and the average currents through the capacitors have to be zero. Accordingly, the steady-state operating point of the converter can be obtained from (2.38) by letting the derivatives be zero yielding

$$\begin{aligned}
I_\mathrm{in} &= DI_\mathrm{L}, \\
I_\mathrm{o} &= I_\mathrm{L} = \frac{I_\mathrm{in}}{D}, \\
U_\mathrm{in} &= U_\mathrm{C} = \frac{U_\mathrm{o}}{D} + \frac{DD'r_\mathrm{C}+r_\mathrm{L}+Dr_\mathrm{ds1}+D'r_\mathrm{ds2}}{D}I_\mathrm{L},
\end{aligned} \tag{2.39}$$

where the capital letters denote the steady-state values. Eq. (2.39) implies that the converter has step-up-converter-like properties because the system outputs are greater in magnitude than the corresponding system inputs, i.e. $I_\mathrm{o} > I_\mathrm{in}$ and $U_\mathrm{in} > U_\mathrm{o}$.

The small-signal state space can be obtained by linerizing the average state space in (2.38), i.e. by developing the proper partial derivatives. The small-signal state-space model of the VSI-type converter is given in (2.40).

$$\begin{aligned}
\frac{\mathrm{d}\hat{i}_\mathrm{L}}{\mathrm{d}t} &= \frac{D}{L}\hat{u}_\mathrm{C} - \frac{r_\mathrm{L}+D(r_\mathrm{C}+r_\mathrm{ds1})+D'r_\mathrm{ds2}}{L}\hat{i}_\mathrm{L} + \frac{Dr_\mathrm{C}}{L}\hat{i}_\mathrm{in} - \frac{1}{L}\hat{u}_\mathrm{o} \\
&\quad - \frac{(D'r_\mathrm{C}+r_\mathrm{ds1}-r_\mathrm{ds2})I_\mathrm{L}-U_\mathrm{C}}{L}\hat{d} \\
\frac{\mathrm{d}\hat{u}_\mathrm{C}}{\mathrm{d}t} &= -\frac{D}{C}\hat{i}_\mathrm{L} + \frac{1}{C}\hat{i}_\mathrm{in} - \frac{I_\mathrm{L}}{C}\hat{d} \\
\hat{u}_\mathrm{in} &= \hat{u}_\mathrm{C} - Dr_\mathrm{C}\hat{i}_\mathrm{L} + r_\mathrm{C}\hat{i}_\mathrm{in} - r_\mathrm{C}I_\mathrm{L}\hat{d} = \left(1+r_\mathrm{C}C\frac{\mathrm{d}}{\mathrm{d}t}\right)\hat{u}_\mathrm{C} \\
\hat{i}_\mathrm{o} &= \hat{i}_\mathrm{L}
\end{aligned} \tag{2.40}$$

Applying the matrix manipulation methods resulting in (2.4), the H-parameters of the converter can be solved. The symbolic transfer functions of the VSI-type converter input

dynamics can be given by

$$Z_{\text{in-o}} = \frac{\hat{u}_{\text{in}}}{\hat{i}_{\text{in}}} = \left(\frac{s}{C} + \frac{DD'r_{\text{C}} + Dr_{\text{ds1}} + D'r_{\text{ds2}} + r_{\text{L}}}{LC} \right) (1 + sr_{\text{C}}C) \frac{1}{\Delta}, \tag{2.41}$$

$$T_{\text{oi-o}} = \frac{\hat{u}_{\text{in}}}{\hat{u}_{\text{o}}} = \frac{D}{LC} (1 + sr_{\text{C}}C) \frac{1}{\Delta}, \tag{2.42}$$

$$G_{\text{ci-o}} = \frac{\hat{u}_{\text{in}}}{\hat{d}} = -\left(s\frac{I_{\text{L}}}{C} + \frac{\left(D^2 r_{\text{C}} + r_{\text{ds2}} + r_{\text{L}}\right) I_{\text{L}} + DU_{\text{C}}}{LC} \right) (1 + sr_{\text{C}}C) \frac{1}{\Delta}, \tag{2.43}$$

and the output dynamics by

$$G_{\text{io-o}} = \frac{\hat{i}_{\text{o}}}{\hat{i}_{\text{in}}} = \frac{D}{LC} (1 + sr_{\text{C}}C) \frac{1}{\Delta}, \tag{2.44}$$

$$Y_{\text{o-o}} = \frac{\hat{i}_{\text{o}}}{\hat{u}_{\text{o}}} = \frac{s}{L} \frac{1}{\Delta}, \tag{2.45}$$

$$G_{\text{co-o}} = \frac{\hat{i}_{\text{o}}}{\hat{d}} = -\left(s\frac{(r_{\text{ds1}} - r_{\text{ds2}} + D'r_{\text{C}}) I_{\text{L}} - U_{\text{C}}}{L} + \frac{DI_{\text{L}}}{LC} \right) \frac{1}{\Delta}, \tag{2.46}$$

where subscript extension '-o' denotes the open-loop transfer function and the determinant of the transfer functions denoted by Δ is

$$\Delta = s^2 + s\frac{D\left(r_{\text{C}} + r_{\text{ds1}}\right) + D'r_{\text{ds2}} + r_{\text{L}}}{L} + \frac{D^2}{LC}. \tag{2.47}$$

A Matlab script calculating the transfer functions in (2.41)-(2.47) can be found from Appendix A.

According to (2.41)-(2.47) the CF VSI-type converter has second order dynamics and a duty-ratio dependent resonance at an angular frequency of $D/\sqrt{LC}$. The control-to-output-current transfer fuction in (2.46) also incorporates a right-half-plane zero (RHP) approximately at an angular frequency given in (2.48). The approximation is done by neglecting the parasitic resistances in (2.46), which have a minor effect on the frequency of the zero.

$$\omega_{\text{z-RHP}} = \frac{I_{\text{in}}}{CU_{\text{in}}} \tag{2.48}$$

A RHP zero in the control loop limits the upper control bandwidth to the frequency of the RHP zero (Skogestad and Postlethwaite, 1998). Both the RHP zero and the duty-ratio dependent resonance are known properties of a VF boost converter (Suntio, 2009). Therefore, in addition to the evidence provided by the steady-state operating point in (2.39), a VSI-type inverter fed from a current source is a current step-up inverter.

The steady-state operating point in (2.39) implies that the duty ratio D has to be

decreased in order to increase the output current or the input voltage. The frequency-domain evidence of this phenomenon is the minus sign in front of the control-related transfer functions in (2.43) and (2.46), which effectively means that their low-frequency phase is 180°. Therefore, if direct-duty-ratio-type control of the output current or the input voltage is to be implemented, the reference has to be subtracted from the feedback signal, which is an inversion of the typical practice in control engineering (Dorf and Bishop, 2001).

2.5.1 Effect of photovoltaic generator

The source-affected H-parameters of the VSI-type converter are given in this section. The symbolic transfer functions are calculated based on Fig. 2.4 and (2.19), the nominal transfer functions given in (2.41)-(2.47) and the source admittance of the PVG ($Y_\mathrm{S} = 1/r_\mathrm{pv}$). The effect of the parasitic resistances of the power-stage components is omitted in order to emphasize the effect of the dynamic resistance of the PVG. A Matlab script containing the calculation of the source-affected transfer functions also including the parasitic resistances can be found in Appendix A. The resulting input dynamics can be given by

$$Z_\mathrm{in\text{-}o}^\mathrm{SA} = \frac{\hat{u}_\mathrm{in}}{\hat{i}_\mathrm{inS}} = \frac{s}{C}\frac{1}{\Delta_\mathrm{SA}}, \tag{2.49}$$

$$T_\mathrm{oi\text{-}o}^\mathrm{SA} = \frac{\hat{u}_\mathrm{in}}{\hat{u}_\mathrm{o}} = \frac{D}{LC}\frac{1}{\Delta_\mathrm{SA}}, \tag{2.50}$$

$$G_\mathrm{ci\text{-}o}^\mathrm{SA} = \frac{\hat{u}_\mathrm{in}}{\hat{d}} = -\frac{I_\mathrm{o}}{LC}\left(\frac{U_\mathrm{o}}{I_\mathrm{o}} + sL\right)\frac{1}{\Delta_\mathrm{SA}}, \tag{2.51}$$

and the output dynamics by

$$G_\mathrm{io\text{-}o}^\mathrm{SA} = \frac{\hat{i}_\mathrm{o}}{\hat{i}_\mathrm{inS}} = \frac{D}{LC}\frac{1}{\Delta_\mathrm{SA}}, \tag{2.52}$$

$$Y_\mathrm{o\text{-}o}^\mathrm{SA} = \frac{\hat{i}_\mathrm{o}}{\hat{u}_\mathrm{o}} = \frac{1}{L}\left(s + \frac{Y_\mathrm{S}}{C}\right)\frac{1}{\Delta_\mathrm{SA}} = \frac{1}{L}\left(s + \frac{1}{r_\mathrm{pv}C}\right)\frac{1}{\Delta_\mathrm{SA}}, \tag{2.53}$$

$$G_\mathrm{co\text{-}o}^\mathrm{SA} = \frac{\hat{i}_\mathrm{o}}{\hat{d}} = \frac{U_\mathrm{in}}{L}\left[s - \frac{1}{C}\left(\frac{I_\mathrm{in}}{U_\mathrm{in}} - Y_\mathrm{S}\right)\right]\frac{1}{\Delta_\mathrm{SA}} \tag{2.54}$$

$$= \frac{U_\mathrm{in}}{L}\left[s - \frac{1}{C}\left(\frac{1}{R_\mathrm{pv}} - \frac{1}{r_\mathrm{pv}}\right)\right]\frac{1}{\Delta_\mathrm{SA}}, \tag{2.55}$$

where the superscript 'SA' denotes the source-affected transfer function, $R_{\mathrm{pv}} = U_{\mathrm{pv}}/I_{\mathrm{pv}} = U_{\mathrm{in}}/I_{\mathrm{in}}$ and the determinant of the source-affected transfer functions Δ_{SA} is given by

$$\Delta_{\mathrm{SA}} = s^2 + s\frac{Y_{\mathrm{S}}}{C} + \frac{D^2}{LC} \approx s^2 + s\frac{1}{r_{\mathrm{pv}}C} + \frac{D^2}{LC}. \tag{2.56}$$

According to the source-affected determinant in (2.56), the dynamic resistance of the PVG (r_{pv}) will attenuate the internal resonant behavior of the converter. Damping factor of the transfer functions (2.49)-(2.56) is low when r_{pv} is high, i.e. in the constant current region (CCR), and the PVG has little or practically no effect on the nominal transfer functions. On the other hand, in the constant voltage region (CVR), r_{pv} is low and it effectively shunts the converter input capacitor and the transfer functions will show the properties of the first order dynamics of a VF VSI (Nousiainen et al., 2011a).

The dynamic resistance of the PVG has significant effect on the nominal control-to-output-current transfer function $G_{\text{co-o}}$ given in (2.46). The source-affected $G_{\text{co-o}}$ given in (2.55) has an operating-point-dependent zero at an angular frequency given by

$$\omega_{\text{z-SA}} = \frac{1}{C}\left(\frac{I_{\mathrm{in}}}{U_{\mathrm{in}}} - Y_{\mathrm{S}}\right) = \frac{1}{C}\left(\frac{1}{R_{\mathrm{pv}}} - \frac{1}{r_{\mathrm{pv}}}\right). \tag{2.57}$$

Because the dynamic resistance r_{pv} is high in the CCR, it has practically no effect on (2.57) compared to the nominal zero in (2.48). At the MPP, r_{pv} coincides with the static resistance R_{pv} as discussed in Section 2.4, and therefore the zero in (2.57) is located at the origin of the complex plane. In the CVR, the dynamic resistance is low compared to the static resistance, and consequently the zero in (2.57) lies on the left half of the complex plane (LHP). Accordingly, the zero in the source-affected control-to-output-current transfer function $G_{\mathrm{co}}^{\mathrm{SA}}$ shifts from the RHP to the LHP when the operating point moves from the CCR to the CVR as shown in (2.58).

$$\begin{aligned}
&\text{CVR:} \quad r_{\mathrm{pv}} < R_{\mathrm{pv}} \Rightarrow \omega_{\mathrm{z}} < 0 \quad \text{LHP-zero} \\
&\text{MPP:} \quad r_{\mathrm{pv}} = R_{\mathrm{pv}} \Rightarrow \omega_{\mathrm{z}} = 0 \quad \text{Origin} \\
&\text{CCR:} \quad r_{\mathrm{pv}} > R_{\mathrm{pv}} \Rightarrow \omega_{\mathrm{z}} > 0 \quad \text{RHP-zero}
\end{aligned} \tag{2.58}$$

The operating points and the main parameters of a low-power VSI-type PV inverter are defined in Table 2.1. Fig. 2.12 shows its soure-affected control-to-output current transfer function at three operating points: one of the operating points lies in the CCR, one in the CVR and one is at the MPP. The low-frequency phase in Fig. 2.12 confirms the movement of the zero in (2.57) along the complex plane as defined in (2.58). It can be deduced that high-bandwidth current controller is easy to be implemented in the CVR applying conventional feedback control. However, when the operating moves to the MPP,

Table 2.1: Main parameters of the VSI-type converter and the PVG used as a source.

	I_{in} (A)	U_{in} (V)	U_{o} (V)	r_{pv} (Ω)	L	C	f_{sw}
CCR	1.01	12.2	8.0	360.0			
MPP	0.95	15.6	8.0	16.4	220 μH	2.2 mF	100 kHz
CVR	0.71	17.4	8.0	4.0			

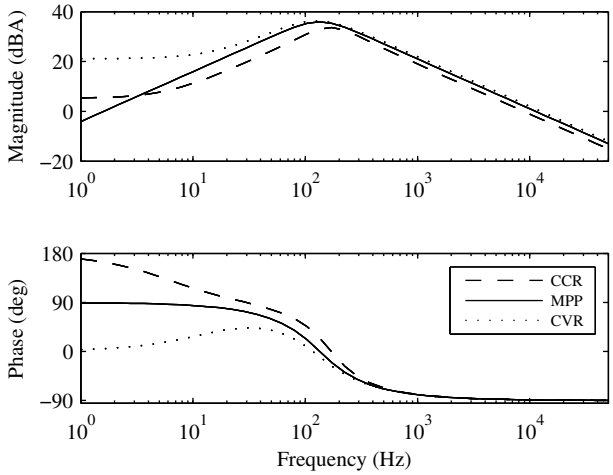


Fig. 2.12: Control-to-output-current transfer function $G_{\mathrm{co\text{-}o}}^{\mathrm{SA}}$.

such an output-current-control loop becomes marginally stable and instability occurs when the operating point is in the CCR. An unstable current loop can be stabilized in the CCR with the cascaded control scheme, where an input-voltage controller determines the output-current reference. This means that input-side control has to be implemented in order to transfer maximum power. The cascaded control scheme is a standard in photovoltaic inverters, however, the origin of why it is needed is explicitly explained only recently (Nousiainen et al., 2011b; Puukko et al., 2011). The stabilizing effect of the input-voltage control will be discussed in detail later in this thesis.

The source-affected control-to-input-voltage transfer function $G_{\mathrm{ci\text{-}o}}^{\mathrm{SA}}$ at the three operating points is shown in Fig. 2.13. The phase behavior of $G_{\mathrm{ci\text{-}o}}^{\mathrm{SA}}$ does not show similar operating-point-dependent characteristics as $G_{\mathrm{co\text{-}o}}^{\mathrm{SA}}$. According to Fig. 2.13, direct-duty-ratio control of the VSI-type converter would be easy to implement, however, the output-current loop is a must in grid-connected inverters in order to guarantee high-quality output current. The source-affected output admittance $Y_{\mathrm{o\text{-}o}}^{\mathrm{SA}}$ in Fig. 2.14 shows operating-point-dependent behavior. At high frequencies, the inductor L dominates the output admittance. In the CCR, when r_{pv} is high, the low-frequency behavior is de-

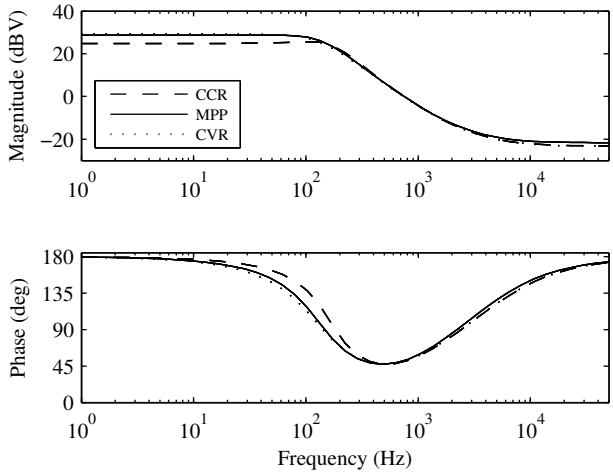


Fig. 2.13: Control-to-input-voltage transfer function $G_{\text{ci-o}}^{\text{SA}}$.

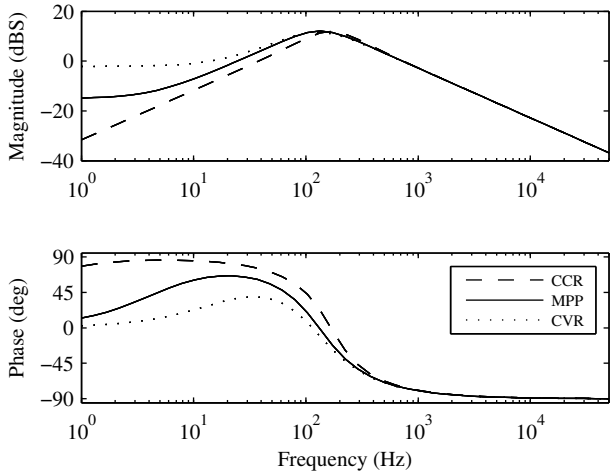


Fig. 2.14: Output admittance $Y_{\text{o-o}}^{\text{SA}}$.

termined by the input capacitor, whereas in the CV region, low r_{pv} shunts the input capacitor. When the impedance of a certain circuit is determined, voltage sources are considered as short circuits and current sources as open circuits. Therefore, when the output impedance of the VSI-type inverter is observed, the inverter input terminals consist of the parallel connection of the input capacitor C and r_{pv}. Therefore, when $r_{\text{pv}} = 0$, the input capacitor is shorted and it does not contribute to the output impedance.

It is not meaningful to plot the source-affected input impedance $Z_{\text{in-o}}^{\text{SA}}$ or the source-

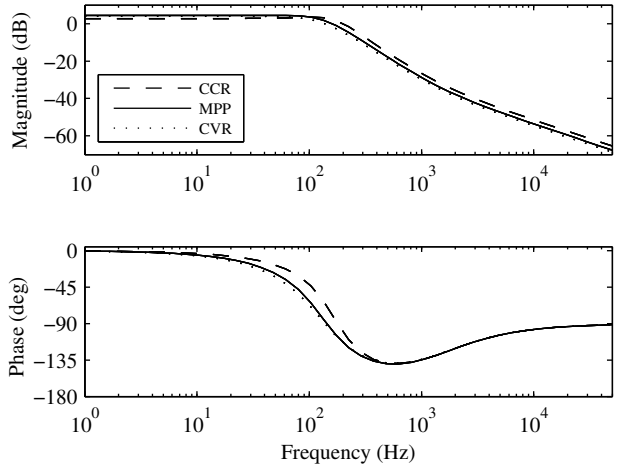


Fig. 2.15: Reverse voltage transfer ratio $T^{\mathrm{SA}}_{\mathrm{oi\text{-}o}}$.

affected forward current gain $G^{\mathrm{SA}}_{\mathrm{io\text{-}o}}$ because the measurement of these transfer functions would require summing of excitation current to the PVG photocurrent, which is not explicitly available for such a use. The input impedance is, however, an important transfer function, because it can be used to determine the stability of the PVG/inverter interface based on the inverse minor-loop gain concept presented in Section 2.3. The closed-loop input impedance will be inspected considering the stability criterion later in this thesis. Fig. 2.15 shows the source-affected reverse voltage transfer ratio $T^{\mathrm{SA}}_{\mathrm{oi\text{-}o}}$. It can be used to study the effect of grid voltage fluctuations, such as voltage spikes or dips, to the inverter input voltage. Fig. 2.15 can also be used to depict the behavior of the forward current gain $G_{\mathrm{io\text{-}o}}$ because according to (2.42) and (2.44) $T_{\mathrm{oi\text{-}o}} = G_{\mathrm{io\text{-}o}}$ and according to (2.50) and (2.52) $T^{\mathrm{SA}}_{\mathrm{oi\text{-}o}} = G^{\mathrm{SA}}_{\mathrm{io\text{-}o}}$.

2.5.2 Comparison of current-fed and voltage-fed VSI

As has been discussed earlier, the PVG has the properties of both current and voltage sources. Therefore it might occur to a reader that a model of a VF converter could be applicable. In this section, the transfer functions of a VF VSI are compared with the transfer functions of the CF VSI derived in the previous section. A VF VSI-type inverter is shown in Fig. 2.16. The power-stage in Fig. 2.16 is exactly the same as the power-stage of the CF VSI-type inverter shown in Fig. 2.10, only the type of the input source is changed. The Y-parameters in (2.6) are used to represent the converter in Fig. 2.16. The Y-parameters can be derived based on the H-parameters by solving the input current $\hat{i}_{\mathrm{in}}$ from the input dynamics in (2.8) yielding

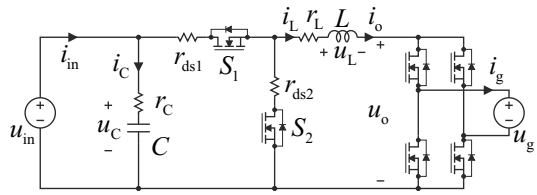


Fig. 2.16: VSI-type VF inverter.

$$\hat{i}_{\mathrm{in}} = \frac{1}{Z^{\mathrm{H}}_{\mathrm{in}}}\hat{u}_{\mathrm{in}} - \frac{T^{\mathrm{H}}_{\mathrm{oi}}}{Z^{\mathrm{H}}_{\mathrm{in}}}\hat{u}_{\mathrm{o}} - \frac{G^{\mathrm{H}}_{\mathrm{ci}}}{Z^{\mathrm{H}}_{\mathrm{in}}}\hat{c}, \tag{2.59}$$

which substituted into the output dynamics in (2.8) yields

$$\begin{aligned}\hat{i}_{\mathrm{o}} &= G^{\mathrm{H}}_{\mathrm{io}}\left(\frac{1}{Z^{\mathrm{H}}_{\mathrm{in}}}\hat{u}_{\mathrm{in}} - \frac{T^{\mathrm{H}}_{\mathrm{oi}}}{Z^{\mathrm{H}}_{\mathrm{in}}}\hat{u}_{\mathrm{o}} - \frac{G^{\mathrm{H}}_{\mathrm{ci}}}{Z^{\mathrm{H}}_{\mathrm{in}}}\hat{c}\right) - Y^{\mathrm{H}}_{\mathrm{o}}\hat{u}_{\mathrm{o}} + G^{\mathrm{H}}_{\mathrm{co}}\hat{c} \\ &= \frac{G^{\mathrm{H}}_{\mathrm{io}}}{Z^{\mathrm{H}}_{\mathrm{in}}}\hat{u}_{\mathrm{in}} - \left(Y^{\mathrm{H}}_{\mathrm{o}} + \frac{G^{\mathrm{H}}_{\mathrm{io}}T^{\mathrm{H}}_{\mathrm{oi}}}{Z^{\mathrm{H}}_{\mathrm{in}}}\right)\hat{u}_{\mathrm{o}} + \left(G^{\mathrm{H}}_{\mathrm{co}} - \frac{G^{\mathrm{H}}_{\mathrm{io}}G^{\mathrm{H}}_{\mathrm{ci}}}{Z^{\mathrm{H}}_{\mathrm{in}}}\right)\hat{c}.\end{aligned} \tag{2.60}$$

The transfer-functions of the VF VSI based on the CF VSI transfer functions can be given according to (2.59) and (2.41)-(2.43) by

$$Y^{\mathrm{Y}}_{\text{in-o}} = \frac{\hat{i}_{\mathrm{in}}}{\hat{u}_{\mathrm{in}}} = \frac{1}{Z_{\text{in-o}}} = C\left(s^2 + \frac{D^2}{LC}\right)\frac{1}{s}, \tag{2.61}$$

$$T^{\mathrm{Y}}_{\text{oi-o}} = \frac{\hat{i}_{\mathrm{in}}}{\hat{u}_0} = -\frac{T_{\text{oi-o}}}{Z_{\text{in-o}}} = -\frac{D}{L}\frac{1}{s}, \tag{2.62}$$

$$G^{\mathrm{Y}}_{\text{ci-o}} = \frac{\hat{i}_{\mathrm{in}}}{\hat{d}} = -\frac{G_{\text{ci-o}}}{Z_{\text{in-o}}} = I_{\mathrm{o}}\left(s + \frac{U_{\mathrm{o}}}{LI_{\mathrm{o}}}\right)\frac{1}{s}, \tag{2.63}$$

and according to (2.60) and (2.44)-(2.46) by

$$G^{\mathrm{Y}}_{\text{io-o}} = \frac{\hat{i}_{\mathrm{o}}}{\hat{u}_{\mathrm{in}}} = \frac{G_{\text{io-o}}}{Z_{\text{in-o}}} = \frac{D}{L}\frac{1}{s}, \tag{2.64}$$

$$Y^{\mathrm{Y}}_{\text{o-o}} = \frac{\hat{i}_{\mathrm{o}}}{\hat{u}_0} = Y_{\text{o-o}} + \frac{G_{\text{io-o}}T_{\text{oi-o}}}{Z_{\text{in-o}}} = Y_{\text{o-sci}} = \frac{1}{L}\frac{1}{s}, \tag{2.65}$$

$$G^{\mathrm{Y}}_{\text{co-o}} = \frac{\hat{i}_{\mathrm{o}}}{\hat{d}} = G_{\text{co-o}} - \frac{G_{\text{io-o}}G_{\text{ci-o}}}{Z_{\text{in-o}}} = \frac{U_{\mathrm{in}}}{L}\frac{1}{s}. \tag{2.66}$$

The parasitic resistances of the inverter components are omitted in order to ease the comparison of the CF and VF inverters. The calculation of the VF VSI transfer functions including the parasitic resistances can be made based on (2.61)-(2.66) and the CF VSI transfer functions calculated in Appendix A.

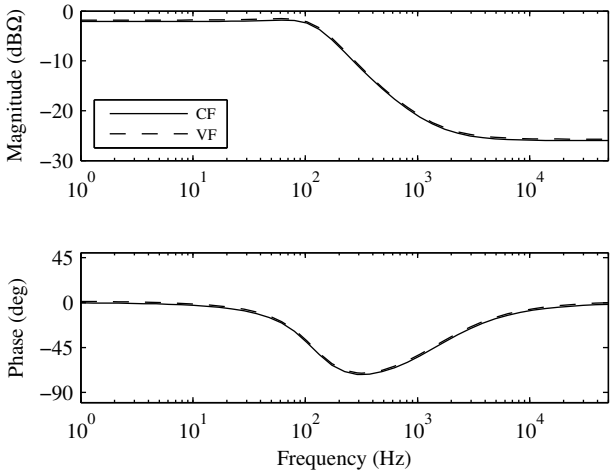


Fig. 2.17: Input impedance $Z_{\text{in-o}}$.

The output admittance of the VF VSI in (2.65) is the output admittance of the CF VSI with short-circuited input given in (2.24), which is quite obvious because the voltage source feeding the VSI in Fig. 2.16 is dynamically a short circuit, i.e. its internal impedance is zero. The input impedance of both the CF and VF VSI is the same, because according to (2.59) $Y_{\text{in}}^{\text{Y}} = 1/Z_{\text{in}}^{\text{H}}$ as shown in Fig. 2.17. When the input impedance is observed from the input terminals, the source feeding the converter is dynamically decoupled from the converter and thus does not short the input capacitor.

The output admittances of the CF and VF VSI are shown in Fig. 2.18. In the VF VSI, the voltage source shorts the input capacitor and it does not influence the output admittance as it does in the CF VSI. It can be concluded that the VF VSI output admittance resembles the output admittance of a VSI-type PV inverter in the CVR (Fig. 2.14), but as soon as the dynamic resistance of the PVG increases (i.e., the operating point moves toward the MPP), the output impedance models derived with the VF model can lead to false conclusions in the grid-interaction research. Therefore, the type of input source has to be taken into account properly.

The control-to-output-current transfer functions are shown in Fig. 2.19. They follow the similar behavior as the source affected $G_{\text{co-o}}$ in Fig. 2.12. The VF converter control-to-output-current transfer function has the properties of the PV inverter in the CVR, i.e. it does not incorporate the RHP zero of the CF inverter. This means that the VF inverter is a minimum-phase system compared to the non-minimum-phase dynamics of the CF inverter. Although the VF inverter has some of the properties of the PV inverter operating in the CVR, the VF model cannot be used to model the PV inverter because

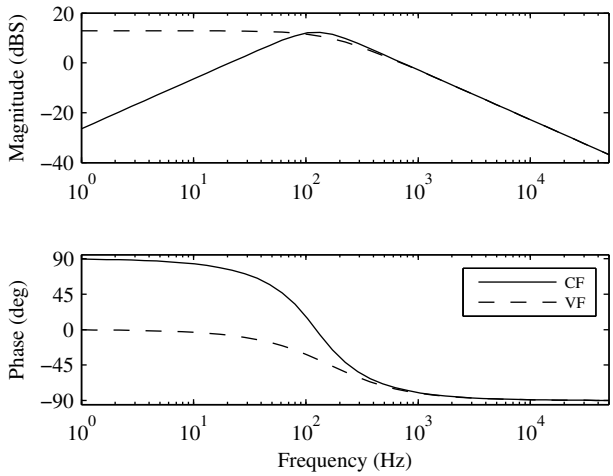


Fig. 2.18: Output admittance $Y_{\text{o-o}}$.

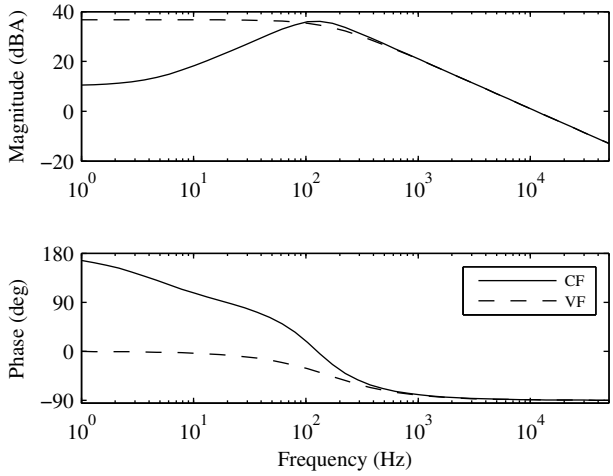


Fig. 2.19: Control-to-output-current transfer function $G_{\text{co-o}}$.

it does not suffice for the input-voltage-controlled converter.

2.6 Dynamic model of a current-fed semi-quadratic buck-boost converter

If the desired input voltage of a PV converter is less than the peak grid voltage, a converter with buck-boost-type conversion ratio is needed. If the PVG in such a case is composed of only a single PV module, the converter has to be capable of handling the wide

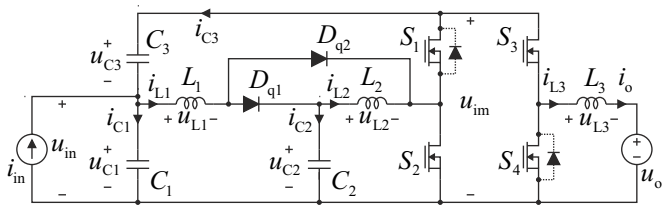


Fig. 2.20: Current-fed semi-quadratic buck-boost converter.

conversion-ratio requirement. The current-fed semi-quadratic buck-boost (CFSQBB) converter ([P4]-[P6]) proposed for modular transformerless PV applications is shown in Fig. 2.20 with the defined components and polarities of the relevant currents and voltages. The switches S_1 and S_4 can be equally substituted with diodes. The diodes D_{q1} and D_{q2} with the inductor L_2 and capacitor C_2 form a quadratic element. The converter integrates a quadratic current-step-down converter at the input side to handle the wide conversion ratio and a current-step-up converter (i.e., the VSI-type converter) to handle the grid-side controls. Cascaded with the unfolding full-bridge, the CFSQBB can be used as a single-phase PV micro inverter. The placement of the capacitor C_3 between the positive terminals of the input and the intermediate voltages (u_{in}, u_{im}, respectively) reduces the voltage stress of the capacitor by the amount of input voltage compared to the conventional placement directly to the intermediate or dc-link terminals. The CFSQBB converter may be controlled either in single- or dual-PWM mode depending on the desired properties.

In the single-PWM mode, the on-time switches (S_1 and S_4) of the buck and boost parts are controlled by the same duty ratio and the off-time switches (S_2 and S_3) by the complement of the duty ratio. During the on-time, the switches S_2 and S_3 and the diode D_{q2} are off and the switches S_1 and S_4 and the diode D_{q1} are conducting yielding the on-time circuit structure given in Fig. 2.21. During the off-time, the switches S_2 and S_3 and the diode D_{q2} are conducting and the switches S_1 and S_4 and the diode D_{q1} are off yielding the off-time circuit structure given in Fig. 2.22. Applying the averaging teqhnique for the on- and off-time subcircuits, the average voltages across the inductors,

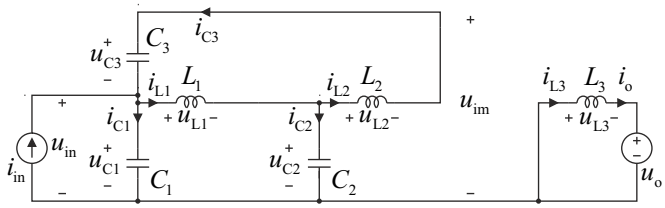


Fig. 2.21: CFSQBB converter during on-time.

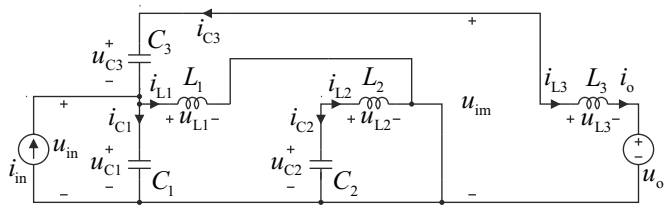


Fig. 2.22: CFSQBB converter during off-time.

the average currents through the capacitors as well as the average input voltage (u_{in}), intermediate voltage (u_{im}) and output current (i_{o}) become as given in (2.67).

$$\langle u_{\mathrm{L1}}\rangle = \langle u_{\mathrm{C1}}\rangle - \langle d\rangle \langle u_{\mathrm{C2}}\rangle \tag{2.67}$$
$$\langle u_{\mathrm{L2}}\rangle = \langle u_{\mathrm{C2}}\rangle - \langle d\rangle \langle u_{\mathrm{C1}}\rangle - \langle d\rangle \langle u_{\mathrm{C3}}\rangle \tag{2.68}$$
$$\langle u_{\mathrm{L3}}\rangle = (1 - \langle d\rangle) \langle u_{\mathrm{C1}}\rangle + (1 - \langle d\rangle) \langle u_{\mathrm{C3}}\rangle - \langle u_{\mathrm{o}}\rangle \tag{2.69}$$
$$\langle i_{\mathrm{C1}}\rangle = \langle i_{\mathrm{in}}\rangle - \langle i_{\mathrm{L1}}\rangle + \langle d\rangle \langle i_{\mathrm{L2}}\rangle - (1 - \langle d\rangle) \langle i_{\mathrm{L3}}\rangle \tag{2.70}$$
$$\langle i_{\mathrm{C2}}\rangle = \langle d\rangle \langle i_{\mathrm{L1}}\rangle - \langle i_{\mathrm{L2}}\rangle \tag{2.71}$$
$$\langle i_{\mathrm{C3}}\rangle = \langle d\rangle \langle i_{\mathrm{L2}}\rangle - (1 - \langle d\rangle) \langle i_{\mathrm{L3}}\rangle \tag{2.72}$$
$$\langle u_{\mathrm{im}}\rangle = \langle u_{\mathrm{C1}}\rangle + \langle u_{\mathrm{C3}}\rangle \tag{2.73}$$
$$\langle u_{\mathrm{in}}\rangle = \langle u_{\mathrm{C1}}\rangle \tag{2.74}$$
$$\langle i_{\mathrm{o}}\rangle = \langle i_{\mathrm{L3}}\rangle \tag{2.75}$$

In order to maintain flux linkage and charge balances, the average voltages across the inductors and average currents through the capacitors have to be zero. According to these principles, the operating-point-related steady-state variables become with denoting $D' = 1 - D$

$$\begin{gathered} I_{\mathrm{L1}} = I_{\mathrm{in}}, \qquad I_{\mathrm{L2}} = D I_{\mathrm{in}}, \qquad I_{\mathrm{L3}} = \frac{D^2}{D'} I_{\mathrm{in}}, \\ U_{\mathrm{C1}} = \frac{D^2}{D'} U_{\mathrm{o}}, \quad U_{\mathrm{C2}} = (1 + D)\, U_{\mathrm{o}}, \quad U_{\mathrm{C3}} = \frac{D}{D'} U_{\mathrm{o}}, \\ U_{\mathrm{im}} = \frac{1}{D'} U_{\mathrm{o}}, \qquad U_{\mathrm{in}} = \frac{D^2}{D'} U_{\mathrm{o}}, \qquad I_{\mathrm{o}} = \frac{D^2}{D'} I_{\mathrm{in}}. \end{gathered} \tag{2.76}$$

In the dual PWM mode, the duty ratios of the buck and boost switch pairs (S_1, S_3 and S_2, S_4, respectively) are controlled separately, allowing e.g. dedicated control systems

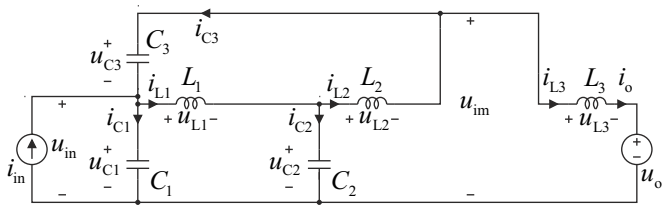


Fig. 2.23: CFSQBB converter during on-off-time.

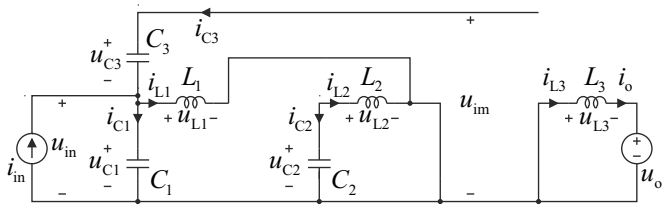


Fig. 2.24: CFSQBB converter during off-on-time.

for the output current and input voltage as well as separate control of the intermediate voltage, which is the feasible control scheme of the single-phase modular inverter application. Besides the on- and off-times, the dual-PWM operated circuit can exhibit two extra states denoted by on-off- and off-on-times. During the on-off-time, the switches S_2 and S_4 and the diode D_{q2} are off and the switches S_1 and S_3 and the diode D_{q1} are conducting yielding the on-off-time circuit structure given in Fig. 2.23. During the off-on-time, the switches S_2 and S_4 and the diode D_{q2} are conducting and the switches S_1 and S_3 and the diode D_{q1} are off yielding the off-on-time circuit structure given in Fig. 2.24.

In order to solve the average voltages across the inductors, average currents through the capacitors as well as average input voltage, intermediate voltage and output current, synchronous PWM generation is assumed. The switching frequencies are assumed to be equal as well as the beginning of the on-times of the buck and boost parts. The synchronous PWM generation is realised by a digital control system. An extra state appears between on- and off-times when $d_1 \neq d_2$, where d_1 and d_2 are the duty ratios of the buck- and boost-parts, respectively. If $d_1 > d_2$, the extra state is the on-off-time and if $d_1 < d_2$, the extra state is the off-on-time. The average values can be solved by common average integral, where T_s is the cycle time. For $d_1 < d_2$ we get the average inductor voltages given by

$$\begin{aligned}
\langle u_{L1} \rangle =& \frac{1}{T_s} \left(\int_0^{d_1 T_s} (u_{C1} - u_{C2})\, \mathrm{d}t + \int_{d_1 T_s}^{d_2 T_s} u_{C1} \mathrm{d}t + \int_{d_2 T_s}^{T_s} u_{C1} \mathrm{d}t \right), \\
\langle u_{L2} \rangle =& \frac{1}{T_s} \left(\int_0^{d_1 T_s} (u_{C2} - u_{C1} - u_{C3})\, \mathrm{d}t + \int_{d_1 T_s}^{d_2 T_s} u_{C2} \mathrm{d}t + \int_{d_2 T_s}^{T_s} u_{C2} \mathrm{d}t \right),
\end{aligned} \tag{2.77}$$

$$\langle u_{\mathrm{L3}}\rangle = \frac{1}{T_{\mathrm{s}}}\left(\int_{0}^{d_1T_{\mathrm{s}}} -u_{\mathrm{o}}\mathrm{d}t + \int_{d_1T_{\mathrm{s}}}^{d_2T_{\mathrm{s}}} -u_{\mathrm{o}}\mathrm{d}t + \int_{d_2T_{\mathrm{s}}}^{T_{\mathrm{s}}} (u_{\mathrm{C1}} + u_{\mathrm{C3}} - u_{\mathrm{o}})\,\mathrm{d}t\right),$$

and the average capacitor currents given by

$$\begin{aligned}
\langle i_{\mathrm{C1}}\rangle &= \frac{1}{T_{\mathrm{s}}}\left(\int_{0}^{d_1T_{\mathrm{s}}} (i_{\mathrm{in}} - i_{\mathrm{L1}} + i_{\mathrm{L2}})\,\mathrm{d}t + \int_{d_1T_{\mathrm{s}}}^{d_2T_{\mathrm{s}}} (i_{\mathrm{in}} - i_{\mathrm{L1}})\,\mathrm{d}t + \int_{d_2T_{\mathrm{s}}}^{T_{\mathrm{s}}} (i_{\mathrm{in}} - i_{\mathrm{L1}} - i_{\mathrm{L3}})\,\mathrm{d}t\right),\\
\langle i_{\mathrm{C2}}\rangle &= \frac{1}{T_{\mathrm{s}}}\left(\int_{0}^{d_1T_{\mathrm{s}}} (i_{\mathrm{L1}} - i_{\mathrm{L2}})\,\mathrm{d}t + \int_{d_1T_{\mathrm{s}}}^{d_2T_{\mathrm{s}}} -i_{\mathrm{L2}}\mathrm{d}t + \int_{d_2T_{\mathrm{s}}}^{T_{\mathrm{s}}} -i_{\mathrm{L2}}\mathrm{d}t\right),\\
\langle i_{\mathrm{C3}}\rangle &= \frac{1}{T_{\mathrm{s}}}\left(\int_{0}^{d_1T_{\mathrm{s}}} i_{\mathrm{L2}}\mathrm{d}t + \int_{d_1T_{\mathrm{s}}}^{d_2T_{\mathrm{s}}} 0\mathrm{d}t + \int_{d_2T_{\mathrm{s}}}^{T_{\mathrm{s}}} -i_{\mathrm{L3}}\mathrm{d}t\right),
\end{aligned} \tag{2.78}$$

and the averages of intermediate voltage, input voltage and output current given by

$$\begin{aligned}
\langle u_{\mathrm{im}}\rangle &= \langle u_{\mathrm{C1}}\rangle + \langle u_{\mathrm{C3}}\rangle,\\
\langle u_{\mathrm{in}}\rangle &= \langle u_{\mathrm{C1}}\rangle,\\
\langle i_{\mathrm{o}}\rangle &= \langle i_{\mathrm{L3}}\rangle.
\end{aligned} \tag{2.79}$$

For $d_1 > d_2$ we would get exactly the same averages as resulting from (2.77)-(2.79). For the dual-PWM mode, the operating-point-related steady-state variables become with denoting $D_2' = 1 - D_2$ and $D_1' = 1 - D_1$

$$\begin{aligned}
&I_{\mathrm{L1}} = I_{\mathrm{in}}, \qquad I_{\mathrm{L2}} = D_1 I_{\mathrm{in}}, \qquad I_{\mathrm{L3}} = \frac{D_1^2}{D_2'} I_{\mathrm{in}},\\
&U_{\mathrm{C1}} = \frac{D_1^2}{D_2'} U_{\mathrm{o}}, \quad U_{\mathrm{C2}} = \frac{1 - D_1^2}{D_2'} U_{\mathrm{o}}, \quad U_{\mathrm{C3}} = \frac{D_1}{D_2'} U_{\mathrm{o}},\\
&U_{\mathrm{im}} = \frac{1}{D_2'} U_{\mathrm{o}}, \qquad U_{\mathrm{in}} = \frac{D_1^2}{D_2'} U_{\mathrm{o}}, \qquad I_{\mathrm{o}} = \frac{D_1^2}{D_2'} I_{\mathrm{in}}.
\end{aligned} \tag{2.80}$$

According to (2.76) and (2.80), the conversion ratio between the input $(U_{\mathrm{o}}, I_{\mathrm{in}})$ and output $(U_{\mathrm{in}}, I_{\mathrm{o}})$ variables is semi-quadratic. The power-fluctuation-induced voltage ripple in the intermediate voltage is efficiently attenuated from the input voltage thanks to the quadratic step-down conversion ratio D^2 (i.e., the intermediate voltage ripple is stepped down to the input voltage also in a quadratic manner), which can be further attenuated with the input-voltage control. The dynamic model is calculated for the dual-PWM-operated converter, because the dual-PWM is the desired mode of the single-

phase inverter application. The computation of the average model including the parasitic resistances can be carried out by substituting the subcircuit equations including the parasitics into (2.77)-(2.79). Such averaging and the linearization of the average model is space-consuming mechanical work, and therefore, we skip directly to the operating point including the parasitic resistances, which can be given by

$$U_{\mathrm{in}} - D_1 U_{\mathrm{C3}} - I_{\mathrm{in}} r_{\mathrm{L1}} + D_1^2 I_{\mathrm{in}} r_{\mathrm{C3}} - D_1 I_{\mathrm{in}} r_{\mathrm{C3}} = 0, \tag{2.81}$$

$$U_{\mathrm{C3}} - D_1 \left(U_{\mathrm{im}} + I_{\mathrm{in}} r_{\mathrm{L2}}\right) - D_1^2 I_{\mathrm{in}} \left(r_{\mathrm{C1}} + r_{\mathrm{C2}} - r_{\mathrm{L2}}\right) = 0, \tag{2.82}$$

$$D_2'^2 U_{\mathrm{im}} - D_2' \left[D_1^2 I_{\mathrm{in}} \left(r_{\mathrm{C1}} + r_{\mathrm{C2}}\right) + U_{\mathrm{o}}\right] - D_1^2 I_{\mathrm{in}} r_{\mathrm{L3}} = 0, \tag{2.83}$$

and to the the linearized state-space given in (2.84). The merged resistances and voltages in (2.84) are given in (2.85).

$$\begin{aligned}
\frac{\mathrm{d}\hat{u}_{\mathrm{C1}}}{\mathrm{d}t} =& -\frac{1}{C_1}\hat{i}_{\mathrm{L1}} + \frac{D_1}{C_1}\hat{i}_{\mathrm{L2}} - \frac{D_2'}{C_1}\hat{i}_{\mathrm{L3}} + \frac{1}{C_1}\hat{i}_{\mathrm{in}} + \frac{D_1 I_{\mathrm{in}}}{C_1}\hat{d}_1 + \frac{D_1^2 I_{\mathrm{in}}}{D_2' C_1}\hat{d}_2 \\
\frac{\mathrm{d}\hat{u}_{\mathrm{C2}}}{\mathrm{d}t} =& \frac{D_1}{C_2}\hat{i}_{\mathrm{L2}} - \frac{D_2'}{C_2}\hat{i}_{\mathrm{L3}} + \frac{D_1 I_{\mathrm{in}}}{C_2}\hat{d}_1 + \frac{D_1^2 I_{\mathrm{in}}}{D_2' C_2}\hat{d}_2 \\
\frac{\mathrm{d}\hat{u}_{\mathrm{C3}}}{\mathrm{d}t} =& \frac{D_1}{C_3}\hat{i}_{\mathrm{L1}} - \frac{1}{C_3}\hat{i}_{\mathrm{L2}} + \frac{I_{\mathrm{in}}}{C_3}\hat{d}_1 \\
\frac{\mathrm{d}\hat{i}_{\mathrm{L1}}}{\mathrm{d}t} =& \frac{1}{L_1}\hat{u}_{\mathrm{C1}} - \frac{D_1}{L_1}\hat{u}_{\mathrm{C3}} - \frac{R_1}{L_1}\hat{i}_{\mathrm{L1}} + \frac{R_2}{L_1}\hat{i}_{\mathrm{L2}} - \frac{r_{\mathrm{C1}} D_2'}{L_1}\hat{i}_{\mathrm{L3}} + \frac{r_{\mathrm{C1}}}{L_1}\hat{i}_{\mathrm{in}} - \frac{U_1}{L_1}\hat{d}_1 + \frac{D_1^2 I_{\mathrm{in}} r_{\mathrm{C1}}}{D_2' L_1}\hat{d}_2 \\
\frac{\mathrm{d}\hat{i}_{\mathrm{L2}}}{\mathrm{d}t} =& -\frac{D_1}{L_2}\hat{u}_{\mathrm{C1}} - \frac{D_1}{L_2}\hat{u}_{\mathrm{C2}} + \frac{1}{L_2}\hat{u}_{\mathrm{C3}} + \frac{R_2}{L_2}\hat{i}_{\mathrm{L1}} - \frac{R_3}{L_2}\hat{i}_{\mathrm{L2}} - \frac{D_1 r_{\mathrm{C1}}}{L_2}\hat{i}_{\mathrm{in}} - \frac{U_2}{L_2}\hat{d}_1 \\
\frac{\mathrm{d}\hat{i}_{\mathrm{L3}}}{\mathrm{d}t} =& \frac{D_2'}{L_3}\hat{u}_{\mathrm{C1}} + \frac{D_2'}{L_3}\hat{u}_{\mathrm{C2}} - \frac{r_{\mathrm{C1}} D_2'}{L_3}\hat{i}_{\mathrm{L1}} - \frac{R_4}{L_3}\hat{i}_{\mathrm{L3}} + \frac{r_{\mathrm{C1}} D_2'}{L_3}\hat{i}_{\mathrm{in}} - \frac{1}{L_3}\hat{u}_{\mathrm{o}} - \frac{U_3}{L_3}\hat{d}_2 \\
\hat{u}_{\mathrm{im}} =& \left(1 + r_{\mathrm{C1}} C_1 \frac{\mathrm{d}}{\mathrm{d}t}\right)\hat{u}_{\mathrm{C1}} + \left(1 + r_{\mathrm{C2}} C_2 \frac{\mathrm{d}}{\mathrm{d}t}\right)\hat{u}_{\mathrm{C2}} \\
\hat{u}_{\mathrm{in}} =& \left(1 + r_{\mathrm{C1}} C_1 \frac{\mathrm{d}}{\mathrm{d}t}\right)\hat{u}_{\mathrm{C1}} \\
\hat{i}_{\mathrm{o}} =& \hat{i}_{\mathrm{L3}}
\end{aligned} \tag{2.84}$$

$$\begin{aligned}
R_1 &= r_{\mathrm{C1}} + r_{\mathrm{L1}} + D_1 r_{\mathrm{C3}} \\
R_2 &= D_1 \left(r_{\mathrm{C1}} + r_{\mathrm{C2}}\right) \\
R_3 &= r_{\mathrm{C3}} + r_{\mathrm{L2}} + D_1 \left(r_{\mathrm{C1}} + r_{\mathrm{C2}} - r_{\mathrm{L2}}\right) \\
R_4 &= D_2' \left(r_{\mathrm{C1}} + r_{\mathrm{C2}}\right) + r_{\mathrm{L3}} \\
U_1 &= U_{\mathrm{C3}} - D_1 I_{\mathrm{in}} \left(r_{\mathrm{C1}} + r_{\mathrm{C3}}\right) + I_{\mathrm{in}} r_{\mathrm{C3}} \\
U_2 &= U_{\mathrm{im}} + D_1 I_{\mathrm{in}} \left(r_{\mathrm{C1}} + r_{\mathrm{C2}} - r_{\mathrm{L2}}\right) - I_{\mathrm{in}} r_{\mathrm{C3}} \\
U_3 &= U_{\mathrm{im}} - D_1^2 I_{\mathrm{in}} \left(r_{\mathrm{C1}} + r_{\mathrm{C2}}\right) / D_2'
\end{aligned} \tag{2.85}$$

The transfer-function set of the CFSQBB, given in (2.86) based on (2.84), has one extra input and output variables compared to the regular H-parameters. The effect of the non-ideal Norton equivalent source can be solved by substitutig $\hat{i}_{\text{in}} = \hat{i}_{\text{inS}} - Y_{\text{S}}\hat{u}_{\text{in}}$ into (2.86), which yields (2.87)-(2.98).

$$\begin{bmatrix} \hat{u}_{\text{im}} \\ \hat{u}_{\text{in}} \\ \hat{i}_{\text{o}} \end{bmatrix} = \begin{bmatrix} Z_{\text{im-o}} & T_{\text{oim-o}} & G_{\text{cim1-o}} & G_{\text{cim2-o}} \\ Z_{\text{in-o}} & T_{\text{oi-o}} & G_{\text{ci1-o}} & G_{\text{ci2-o}} \\ G_{\text{io-o}} & -Y_{\text{o-o}} & G_{\text{co1-o}} & G_{\text{co2-o}} \end{bmatrix} \begin{bmatrix} \hat{i}_{\text{in}} \\ \hat{u}_{\text{o}} \\ \hat{d}_1 \\ \hat{d}_2 \end{bmatrix} \tag{2.86}$$

$$Z^{\text{SA}}_{\text{im-o}} = \frac{\hat{u}_{\text{im}}}{\hat{i}_{\text{inS}}} = \frac{Z_{\text{im-o}}}{1 + Y_{\text{S}} Z_{\text{in-o}}} \tag{2.87}$$

$$T^{\text{SA}}_{\text{oim-o}} = \frac{\hat{u}_{\text{im}}}{\hat{u}_{\text{o}}} = \frac{1 + Y_{\text{S}} \left(Z_{\text{in-o}} - \dfrac{T_{\text{oi-o}} Z_{\text{im-o}}}{T_{\text{oim-o}}} \right)}{1 + Y_{\text{S}} Z_{\text{in-o}}} T_{\text{oim-o}} \tag{2.88}$$

$$G^{\text{SA}}_{\text{cim1-o}} = \frac{\hat{u}_{\text{im}}}{\hat{d}_1} = \frac{1 + Y_{\text{S}} \left(Z_{\text{in-o}} - \dfrac{G_{\text{ci1-o}} Z_{\text{im-o}}}{G_{\text{cim1-o}}} \right)}{1 + Y_{\text{S}} Z_{\text{in-o}}} G_{\text{cim1-o}} \tag{2.89}$$

$$G^{\text{SA}}_{\text{cim2-o}} = \frac{\hat{u}_{\text{im}}}{\hat{d}_2} = \frac{1 + Y_{\text{S}} \left(Z_{\text{in-o}} - \dfrac{G_{\text{ci2-o}} Z_{\text{im-o}}}{G_{\text{cim2-o}}} \right)}{1 + Y_{\text{S}} Z_{\text{in-o}}} G_{\text{cim2-o}} \tag{2.90}$$

$$Z^{\text{SA}}_{\text{in-o}} = \frac{\hat{u}_{\text{in}}}{\hat{i}_{\text{inS}}} = \frac{Z_{\text{in-o}}}{1 + Y_{\text{S}} Z_{\text{in-o}}} \tag{2.91}$$

$$T^{\text{SA}}_{\text{oi-o}} = \frac{\hat{u}_{\text{in}}}{\hat{u}_{\text{o}}} = \frac{T_{\text{oi-o}}}{1 + Y_{\text{S}} Z_{\text{in-o}}} \tag{2.92}$$

$$G^{\text{SA}}_{\text{ci1-o}} = \frac{\hat{u}_{\text{in}}}{\hat{d}_1} = \frac{G_{\text{ci1-o}}}{1 + Y_{\text{S}} Z_{\text{in-o}}} \tag{2.93}$$

$$G^{\text{SA}}_{\text{ci2-o}} = \frac{\hat{u}_{\text{in}}}{\hat{d}_2} = \frac{G_{\text{ci2-o}}}{1 + Y_{\text{S}} Z_{\text{in-o}}} \tag{2.94}$$

$$G^{\text{SA}}_{\text{io-o}} = \frac{\hat{i}_{\text{o}}}{\hat{i}_{\text{inS}}} = \frac{G_{\text{io-o}}}{1 + Y_{\text{S}} Z_{\text{in-o}}} \tag{2.95}$$

$$Y^{\text{SA}}_{\text{o-o}} = \frac{\hat{i}_{\text{o}}}{\hat{u}_{\text{o}}} = \frac{1 + Y_{\text{S}} \left(Z_{\text{in-o}} + \dfrac{T_{\text{oi-o}} G_{\text{io-o}}}{Y_{\text{o-o}}} \right)}{1 + Y_{\text{S}} Z_{\text{in-o}}} Y_{\text{o-o}} \tag{2.96}$$

$$G^{\text{SA}}_{\text{co1-o}} = \frac{\hat{i}_{\text{o}}}{\hat{d}_1} = \frac{1 + Y_{\text{S}} \left(Z_{\text{in-o}} - \dfrac{G_{\text{ci1-o}} G_{\text{io-o}}}{G_{\text{co1-o}}} \right)}{1 + Y_{\text{S}} Z_{\text{in-o}}} G_{\text{co1-o}} \tag{2.97}$$

$$G^{\text{SA}}_{\text{co2-o}} = \frac{\hat{i}_{\text{o}}}{\hat{d}_2} = \frac{1 + Y_{\text{S}} \left(Z_{\text{in-o}} - \dfrac{G_{\text{ci2-o}} G_{\text{io-o}}}{G_{\text{co2-o}}} \right)}{1 + Y_{\text{S}} Z_{\text{in-o}}} G_{\text{co2-o}} \tag{2.98}$$

The dynamic properties of the CFSQBB converter will be discussed in more detail in the next chapter, where its control-system design in the micro-inverter application is studied. The calculation of both the source and non-source-affected open-loop transfer functions of the CFSQBB is provided in Appendix B as a Matlab script.

3 CLOSED-LOOP FORMULATION & CONTROL-SYSTEM DESIGN

This chapter presents the dynamic formulation of the input-voltage and output-current controlled converters as well as the converter with the cascaded control scheme. Control-system design examples are shown for the VSI-type PV inverter as well as for an inverter based on the CFSQBB converter. The closed-loop analysis reveals the relation between the input-voltage-control stability of the VSI with the cascaded control scheme and the size of its input capacitor as well as the negative output impedance originating from the multiplier-based grid synchronization. The theory is derived in the continuous-time domain although the controllers are implemented with a microprocessor in the discrete-time domain. The control delay imposed by the discrete implementation is taken into account by Padé approximant of the time delay. The feasibility of such an analysis is verified in the experimental measurements.

3.1 Input-voltage control

The control-block diagram of an input-voltage-controlled converter is shown in Fig. 3.1, where G_a is the modulator gain, G_vc is the input-voltage controller transfer function, $u_\mathrm{ref}^\mathrm{uin}$ is the input-voltage reference generated by the MPPT facility, $G_\mathrm{se}^\mathrm{in}$ is the input-voltage-sensing gain and $R_\mathrm{eq}^\mathrm{in}$ is the equivalent input-current-sensing resistor. The duty ratio $\hat{d}$ can be given according to Fig. 3.1 by

$$\hat{d} = G_\mathrm{a} G_\mathrm{vc} \left(\hat{u}_\mathrm{ref}^\mathrm{uin} - G_\mathrm{se}^\mathrm{in} \hat{u}_\mathrm{in} \right). \tag{3.1}$$

The closed-loop input voltage $\hat{u}_\mathrm{in}$ can be solved according to Fig. 3.1 yielding

$$\begin{aligned} \hat{u}_\mathrm{in} =& Z_\mathrm{in\text{-}o} \hat{\hat{i}}_\mathrm{in} + T_\mathrm{oi\text{-}o} \hat{u}_\mathrm{o} + G_\mathrm{ci\text{-}o} G_\mathrm{a} G_\mathrm{vc} \left(u_\mathrm{ref}^\mathrm{uin} - G_\mathrm{se}^\mathrm{in} u_\mathrm{in} \right) \\ =& \frac{Z_\mathrm{in\text{-}o}}{1 + L_\mathrm{in}} \hat{\hat{i}}_\mathrm{in} + \frac{T_\mathrm{oi\text{-}o}}{1 + L_\mathrm{in}} \hat{u}_\mathrm{o} + \frac{L_\mathrm{in}}{1 + L_\mathrm{in}} \frac{1}{G_\mathrm{se}^\mathrm{in}} \hat{u}_\mathrm{ref}^\mathrm{in}, \end{aligned} \tag{3.2}$$

where the input-voltage-control loop denoted by L_in is

$$L_\mathrm{in} = G_\mathrm{se}^\mathrm{in} G_\mathrm{vc} G_\mathrm{a} G_\mathrm{ci\text{-}o}. \tag{3.3}$$

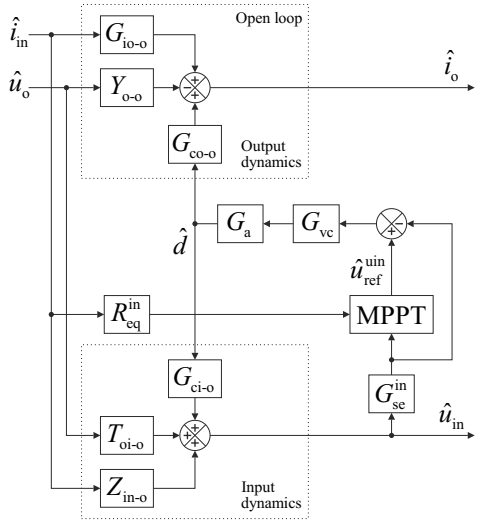


Fig. 3.1: Control-block diagram of the input-voltage-controlled converter.

The stability of the input-voltage control loop can be determined by applying the Nyquist stability criterion to L_{in}.

The closed-loop output current i_{o} can be solved according to Fig. 3.1 yielding

$$\hat{i}_{\text{o}} = G_{\text{io-o}}\hat{i}_{\text{in}} - Y_{\text{o-o}}\hat{u}_{\text{o}} + G_{\text{co-o}}G_{\text{a}}G_{\text{vc}}\left(u_{\text{ref}}^{\text{uin}} - G_{\text{se}}^{\text{in}}u_{\text{in}}\right). \tag{3.4}$$

Substituting (3.2) into (3.4) yields

$$\begin{aligned}\hat{i}_{\text{o}} = &\left(\frac{G_{\text{io-o}}}{1+L_{\text{in}}} + \frac{L_{\text{in}}}{1+L_{\text{in}}}G_{\text{io-}\infty}\right)\hat{i}_{\text{in}} - \left(\frac{Y_{\text{o-o}}}{1+L_{\text{in}}} + \frac{L_{\text{in}}}{1+L_{\text{in}}}Y_{\text{o-}\infty}\right)\hat{u}_{\text{o}} \\ &+ \frac{L_{\text{in}}}{1+L_{\text{in}}}\frac{G_{\text{co-o}}}{G_{\text{ci-o}}}\frac{1}{G_{\text{se}}^{\text{in}}}\hat{u}_{\text{ref}}^{\text{in}},\end{aligned} \tag{3.5}$$

where the ideal forward current gain $G_{\text{io-}\infty}$ is given in (3.6) and the ideal output admittance $Y_{\text{o-}\infty}$ was given earlier in (2.25).

$$G_{\text{io-}\infty} = G_{\text{io-o}} - \frac{Z_{\text{in-o}}G_{\text{co-o}}}{G_{\text{ci-o}}} \tag{3.6}$$

The input-dynamics of the input-voltage controlled converter can be summarized according to (3.2) by

$$Z_{\text{in-c}}^{\text{in}} = \frac{\hat{u}_{\text{in}}}{\hat{i}_{\text{in}}} = \frac{Z_{\text{in-o}}}{1+L_{\text{in}}}, \tag{3.7}$$

$$T_{\text{oi-c}}^{\text{in}} = \frac{\hat{u}_{\text{in}}}{\hat{u}_{\text{o}}} = \frac{T_{\text{oi-o}}}{1 + L_{\text{in}}}, \tag{3.8}$$

$$G_{\text{ci-c}}^{\text{in}} = \frac{\hat{u}_{\text{in}}}{\hat{u}_{\text{ref}}^{\text{uin}}} = \frac{L_{\text{in}}}{1 + L_{\text{in}}} \frac{1}{G_{\text{se}}^{\text{in}}}, \tag{3.9}$$

and the output dynamics according to (3.5) by

$$G_{\text{io-c}}^{\text{in}} = \frac{\hat{i}_{\text{o}}}{\hat{i}_{\text{in}}} = \frac{G_{\text{io-o}}}{1 + L_{\text{in}}} + \frac{L_{\text{in}}}{1 + L_{\text{in}}} G_{\text{io-}\infty}, \tag{3.10}$$

$$Y_{\text{o-c}}^{\text{in}} = \frac{\hat{i}_{\text{o}}}{\hat{u}_{\text{o}}} = \frac{Y_{\text{o-o}}}{1 + L_{\text{in}}} + \frac{L_{\text{in}}}{1 + L_{\text{in}}} Y_{\text{o-}\infty}, \tag{3.11}$$

$$G_{\text{co-c}}^{\text{in}} = \frac{\hat{i}_{\text{o}}}{\hat{u}_{\text{ref}}^{\text{uin}}} = \frac{L_{\text{in}}}{1 + L_{\text{in}}} \frac{G_{\text{co-o}}}{G_{\text{ci-o}}} \frac{1}{G_{\text{se}}^{\text{in}}}, \tag{3.12}$$

where the subscript extension '-c' denotes the closed-loop transfer function and superscript 'in' denotes that the input-voltage loop is connected.

The low frequency behavior of the transfer functions can be approximated by considering the input-voltage-loop gain L_{in}. At the low frequencies, i.e., below the loop-gain crossover frequency, the coefficient $1/(1 + L_{\text{in}}) \approx 0$, and therefore the low-frequency closed-loop input impedance $Z_{\text{in-c}}^{\text{in}}$ and the reverse voltage transfer ratio $T_{\text{oi-c}}^{\text{in}}$ are zero, which means that the input-voltage control transforms the converter input port into ideal voltage source at the low frequencies, and therefore low-frequency instability cannot be expected based on the inverse minor-loop gain. On the other hand, at the low frequencies, $L_{\text{in}}/(1 + L_{\text{in}}) \approx 1$, which means that the closed-loop forward current gain $G_{\text{io-c}}^{\text{in}}$ and the output admittance $Y_{\text{o-c}}^{\text{in}}$ are determined by $G_{\text{io-}\infty}$ and $Y_{\text{o-}\infty}$ within the control bandwidth. When the input-voltage control is ideal (i.e., $L_{\text{in}} \to \infty$), $G_{\text{io-c}}^{\text{in}} = G_{\text{io-}\infty}$ and $Y_{\text{o-c}}^{\text{in}} = Y_{\text{o-}\infty}$, which justify the naming ideal forward current gain and ideal output admittance.

At the frequencies above the input-voltage-loop-gain crossover frequency, the coefficient $1/(1+L_{\text{in}}) \approx 1$, which means that $Z_{\text{in-c}}^{\text{in}}$ and $T_{\text{oi-c}}^{\text{in}}$ are determined by their open-loop counterparts $Z_{\text{in-o}}$ and $T_{\text{oi-o}}$. At the high frequencies, $L_{\text{in}}/(1 + L_{\text{in}}) \approx 0$, and therefore, $G_{\text{io-c}}^{\text{in}}$ and $Y_{\text{o-c}}^{\text{in}}$ are determined also by their open-loop counterparts $G_{\text{io-o}}$ and $Y_{\text{o-o}}$. These observations can be used to predict the behavior of the input-voltage controlled converter to some extent before actually tuning the controller. The ideal output admittance $Y_{\text{o-}\infty}$ at the low frequencies can be approximated by $I_{\text{o}}/U_{\text{o}}$. This means that if the two-stage conversion scheme (Fig. 1.5b) is applied, the operating-point-dependent zero of the VSI-type PV inverter is always at the origin based on (2.57) regardless of the operating point of the PVG. This is beneficial for the VSI and, in practice, means that it is fed from a constant power source instead of a current source. According to Messo et al. (2012), the operating-point-dependent dynamic resistance of the PVG (r_{pv}) is also reflected to the output port of the preregulator if it is operated with open-loop-based MPPT. Therefore,

in such a case, the inverter control dynamics contain a zero that may be located both at the RHP or LHP depending on the operating point of the PVG. Consequently, the input-voltage control is a highly recommended practice for the preregulator in the two-stage conversion scheme.

3.2 Output-current control

The first step of the procedure to solve the output-controlled-converter dynamics is the linearization of the duty ratio due to the multiplier-based synchronization (Fig. 1.5a and Fig. 1.5b). The output-current reference is shaped according to the output voltage waveform in order to inject current at near unity power factor to the grid without the need for more complex phase-locked-loop-based (PLL) synchronization methods (Blaabjerg et al., 2006). The duty ratio in the time-domain can be given by

$$d = G_{\mathrm{a}} G_{\mathrm{cc}} \left(G_{\mathrm{se}}^{\mathrm{out}} u_{\mathrm{o}} u_{\mathrm{ref}}^{\mathrm{io}} - R_{\mathrm{eq}}^{\mathrm{out}} i_{\mathrm{o}} \right), \tag{3.13}$$

and in the frequency domain by

$$\hat{d} = G_{\mathrm{a}} G_{\mathrm{cc}} \left(G_{\mathrm{se}}^{\mathrm{out}} U_{\mathrm{o}} \hat{u}_{\mathrm{ref}}^{\mathrm{io}} + G_{\mathrm{se}}^{\mathrm{out}} U_{\mathrm{ref}}^{\mathrm{io}} \hat{u}_{\mathrm{o}} - R_{\mathrm{eq}}^{\mathrm{out}} \hat{i}_{\mathrm{o}} \right), \tag{3.14}$$

where the elements either in the time or frequency domain are defined as follows: G_{cc} is the current controller, $G_{\mathrm{se}}^{\mathrm{out}}$ output-voltage-sensing function, $R_{\mathrm{eq}}^{\mathrm{out}}$ the equivalent output-current-sensing resistor and $u_{\mathrm{ref}}^{\mathrm{io}}$ the current-reference voltage signal. According to (3.14), the control-block diagram of the output-current controlled converter can be presented as shown in Fig. 3.2.

The closed-loop output current can be solved from Fig. 3.2 yielding

$$\begin{aligned} \hat{i}_{\mathrm{o}} =& G_{\text{io-o}} \hat{i}_{\mathrm{in}} - Y_{\text{o-o}} \hat{u}_{\mathrm{o}} + G_{\text{co-o}} G_{\mathrm{a}} G_{\mathrm{cc}} \left(G_{\mathrm{se}}^{\mathrm{out}} U_{\mathrm{o}} \hat{u}_{\mathrm{ref}}^{\mathrm{io}} + G_{\mathrm{se}}^{\mathrm{out}} U_{\mathrm{ref}}^{\mathrm{io}} \hat{u}_{\mathrm{o}} - R_{\mathrm{eq}}^{\mathrm{out}} \hat{i}_{\mathrm{o}} \right) \\ =& \frac{G_{\text{io-o}}}{1 + L_{\mathrm{out}}} \hat{i}_{\mathrm{in}} - \left(\frac{Y_{\text{o-o}}}{1 + L_{\mathrm{out}}} - \frac{L_{\mathrm{out}}}{1 + L_{\mathrm{out}}} Y_{\mathrm{ff}} \right) \hat{u}_{\mathrm{o}} + \frac{1}{R_{\mathrm{eq}}^{\mathrm{out}}} \frac{L_{\mathrm{out}}}{1 + L_{\mathrm{out}}} \hat{u}_{\mathrm{ref}}^{\mathrm{io}}, \end{aligned} \tag{3.15}$$

where the output-current-loop gain L_{out} is given in (3.16), the feedforward admittance Y_{ff} originating from the grid synchronization is given in (3.17) and the steady-state current reference $U_{\mathrm{ref}}^{\mathrm{io}}$ in (3.17) is given in (3.18). Applying the Nyquist stability criterion to the output-current-loop gain L_{out} determines the stability of the output-current control.

$$L_{\mathrm{out}} = R_{\mathrm{eq}}^{\mathrm{out}} G_{\mathrm{cc}} G_{\mathrm{a}} G_{\text{co-o}} \tag{3.16}$$

$$Y_{\mathrm{ff}} = \frac{1}{R_{\mathrm{eq}}^{\mathrm{out}}} G_{\mathrm{se}}^{\mathrm{out}} U_{\mathrm{ref}}^{\mathrm{io}} \tag{3.17}$$

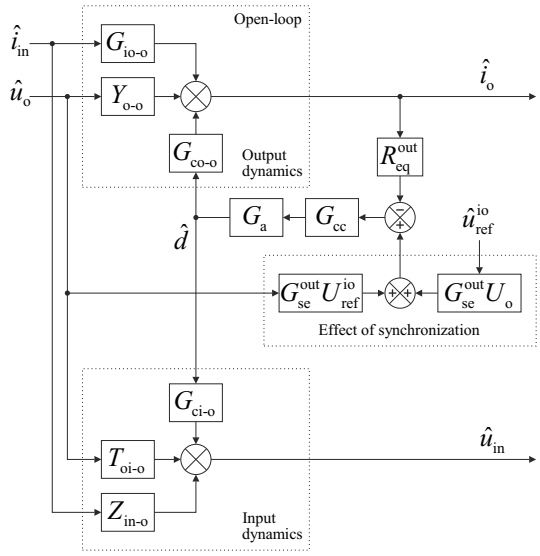


Fig. 3.2: Control-block diagram of the output-current-controlled converter.

$$U_{\text{ref}}^{\text{io}} = \frac{I_{\text{o}} R_{\text{eq}}^{\text{out}}\,(s=0)}{U_{\text{o}} G_{\text{se}}^{\text{out}}\,(s=0)} \tag{3.18}$$

The closed-loop input voltage can be solved according to Fig. 3.2 by

$$\hat{u}_{\text{in}} = Z_{\text{in-o}}\hat{\hat{i}}_{\text{in}} + T_{\text{oi-o}}\hat{u}_{\text{o}} + G_{\text{ci-o}}G_{\text{a}}G_{\text{cc}}\left(G_{\text{se}}^{\text{out}}U_{\text{o}}\hat{u}_{\text{ref}}^{\text{io}} + G_{\text{se}}^{\text{out}}V_{\text{c}}\hat{u}_{\text{o}} - R_{\text{eq}}^{\text{out}}\hat{\hat{i}}_{\text{o}}\right). \tag{3.19}$$

Substituting (3.15) into (3.19) yields

$$\begin{aligned}\hat{u}_{\text{in}} = &\left(\frac{Z_{\text{in-o}}}{1+L_{\text{out}}} + \frac{L_{\text{out}}}{1+L_{\text{out}}}Z_{\text{in-}\infty}\right)\hat{\hat{i}}_{\text{in}} \\ &+ \left[\frac{T_{\text{oi-o}}}{1+L_{\text{out}}} + \frac{L_{\text{out}}}{1+L_{\text{out}}}\left(T_{\text{oi-}\infty} + \frac{G_{\text{ci}}}{G_{\text{co}}}Y_{\text{ff}}\right)\right]\hat{u}_{\text{o}} \\ &+ \frac{1}{R_{\text{eq}}^{\text{out}}}\frac{L_{\text{out}}}{1+L_{\text{out}}}\frac{G_{\text{ci}}}{G_{\text{co}}}G_{\text{se}}^{\text{out}}U_{\text{o}}\hat{u}_{\text{ref}}^{\text{io}},\end{aligned} \tag{3.20}$$

where the ideal reverse voltage transfer ratio $T_{\text{oi-}\infty}$ is defined in (3.21) and the ideal input impedance $Z_{\text{in-}\infty}$ was defined earlier in (2.17).

$$T_{\text{oi-}\infty} = T_{\text{oi-o}} + \frac{G_{\text{ci-o}}Y_{\text{o-o}}}{G_{\text{co-o}}} \tag{3.21}$$

The input dynamics of the output-current-controlled converter can be summarized ac-

cording to (3.20) by

$$Z_{\text{in-c}}^{\text{out}} = \frac{\hat{u}_{\text{in}}}{\hat{i}_{\text{in}}} = \frac{Z_{\text{in-o}}}{1+L_{\text{out}}} + \frac{L_{\text{out}}}{1+L_{\text{out}}} Z_{\text{in-}\infty}, \tag{3.22}$$

$$T_{\text{oi-c}}^{\text{out}} = \frac{\hat{u}_{\text{in}}}{\hat{u}_{\text{o}}} = \frac{T_{\text{oi-o}}}{1+L_{\text{out}}} + \frac{L_{\text{out}}}{1+L_{\text{out}}} \left(T_{\text{oi-}\infty} + \frac{G_{\text{ci-o}}}{G_{\text{co-o}}} Y_{\text{ff}} \right), \tag{3.23}$$

$$G_{\text{ci-c}}^{\text{out}} = \frac{\hat{u}_{\text{in}}}{\hat{u}_{\text{ref}}^{\text{io}}} = \frac{1}{R_{\text{eq}}^{\text{out}}} \frac{L_{\text{out}}}{1+L_{\text{out}}} \frac{G_{\text{ci}}}{G_{\text{co}}} G_{\text{se}}^{\text{out}} U_{\text{o}}, \tag{3.24}$$

and output dynamics according to (3.15) by

$$G_{\text{io-c}}^{\text{out}} = \frac{\hat{i}_{\text{o}}}{\hat{i}_{\text{in}}} = \frac{G_{\text{io-o}}}{1+L_{\text{out}}}, \tag{3.25}$$

$$Y_{\text{o-c}}^{\text{out}} = \frac{\hat{i}_{\text{o}}}{\hat{u}_{\text{o}}} = \frac{Y_{\text{o-o}}}{1+L_{\text{out}}} - \frac{L_{\text{out}}}{1+L_{\text{out}}} Y_{\text{ff}}, \tag{3.26}$$

$$G_{\text{co-c}}^{\text{out}} = \frac{\hat{i}_{\text{o}}}{\hat{u}_{\text{ref}}^{\text{io}}} = \frac{1}{R_{\text{eq}}^{\text{out}}} \frac{L_{\text{out}}}{1+L_{\text{out}}}, \tag{3.27}$$

where the superscript 'out' denotes that the output-current-control loop is connected.

The transfer function $G_{\text{ci-c}}^{\text{out}}$ in (3.24) between the output-current reference and the input voltage determines the properties of the input-voltage control in the cascaded control scheme. It can be seen that the original control-to-output-current transfer function $G_{\text{co-o}}$ in (3.24) is located in the denominator, which means that the operating point dependent zero of $G_{\text{co-o}}$ in (2.57) introduces a pole to $G_{\text{ci-c}}^{\text{out}}$, which may locate in the RHP and is one of the explanations why the CF VSI with mere output-current control is unstable.

Another explanation is the input impedance of the output-current-controlled converter $Z_{\text{in-c}}^{\text{out}}$ given in (3.22). The behavior of $Z_{\text{in-c}}^{\text{out}}$ at the frequencies below the current-loop-gain crossover frequency is determined by $Z_{\text{in-}\infty}$, which can be approximated by $-U_{\text{in}}/I_{\text{in}}$ at the named frequencies. At the MPP, $U_{\text{in}}/I_{\text{in}}$ equals the low-frequency value of the PVG impedance (r_{pv}) with a negative sign, and therefore the output-current-controlled converter becomes unstable at the MPP owing to the minor-loop gain instability. This condition is valid also for the output-voltage-controlled PV converter (Leppäaho et al., 2010), which implies that mere output-side control of a PV converter cannot be used for maximum power transfer.

According to (3.26), the output admittance $Y_{\text{o-c}}^{\text{out}}$ of the output-current-controlled converter is determined by the feedforward admittance Y_{ff} with a negative sign up to the current-loop-crossover frequency. Therefore, the inverter output impedance $1/Y_{\text{o-c}}^{\text{out}}$ has negative-incremental-resistor-like behavior at those frequencies. It can be seen from (3.26), that if $Y_{\text{ff}} = 0$, the low-frequency behavior of the output admittance resembles ideal current source, i.e. the low-frequency admittance is zero. Consequently, it can

be deduced that grid synchronization can impair the current-source property of a grid-connected inverter.

3.3 Cascaded control scheme

In the cascaded control scheme, the MPPT facility generates the input-voltage reference which is subtracted from the input-voltage-feedback signal because the control signal, i.e. the output current reference, has to be increased in order to decrease to input voltage. The input-voltage-error signal is then fed to the input voltage controller, whose output is used as the control variable for the output-current-controlled converter in Fig. 3.2. The control-block diagram of the cascaded control scheme can be given according to the transfer functions (3.22)-(3.27) as shown in Fig. 3.3, where $G_{\mathrm{vc}}^{\mathrm{in}}$ denotes the input-voltage controller, $G_{\mathrm{se}}^{\mathrm{in}}$ the input-voltage-sensing gain and $R_{\mathrm{eq}}^{\mathrm{in}}$ the equivalent input-current-sensing resistor.

According to Fig. 3.3, the output-current reference $\hat{u}_{\mathrm{ref}}^{\mathrm{io}}$ can be given by

$$\hat{u}_{\mathrm{ref}}^{\mathrm{io}} = G_{\mathrm{vc}}^{\mathrm{in}} \left(G_{\mathrm{se}}^{\mathrm{in}} \hat{u}_{\mathrm{in}} - \hat{u}_{\mathrm{ref}}^{\mathrm{uin}} \right), \tag{3.28}$$

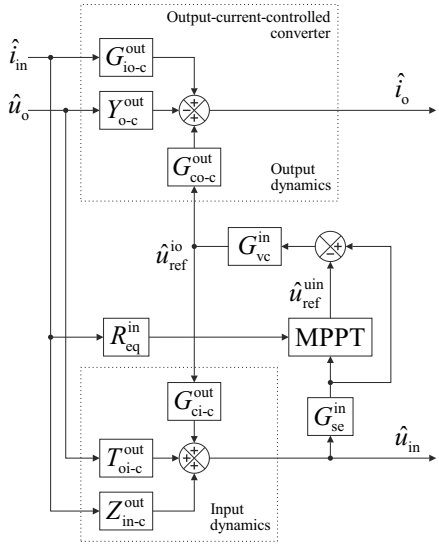


Fig. 3.3: Control-block diagram of the cascaded control scheme.

and the closed-loop input voltage can be solved by

$$\begin{aligned}\hat{u}_{\text{in}} =& Z_{\text{in-c}}^{\text{out}}\hat{i}_{\text{in}} + T_{\text{oi-c}}^{\text{out}}\hat{u}_{\text{o}} + G_{\text{ci-c}}^{\text{out}}G_{\text{vc}}^{\text{in}}\left(G_{\text{se}}^{\text{in}}\hat{u}_{\text{in}} - \hat{u}_{\text{ref}}^{\text{uin}}\right)\\ =& \frac{Z_{\text{in-c}}^{\text{out}}}{1-L_{\text{in}}}\hat{i}_{\text{in}} + \frac{T_{\text{oi-c}}^{\text{out}}}{1-L_{\text{in}}}\hat{u}_{\text{o}} + \frac{1}{G_{\text{se}}^{\text{in}}}\frac{L_{\text{in}}}{1-L_{\text{in}}}\hat{u}_{\text{ref}}^{\text{uin}},\end{aligned} \tag{3.29}$$

where the input-voltage-control loop gain L_{in}, which determines the input-voltage-control stability, is defined as

$$L_{\text{in}} = G_{\text{se}}^{\text{in}}G_{\text{vc}}^{\text{in}}G_{\text{ci-c}}^{\text{out}}. \tag{3.30}$$

The closed-loop output current can be given according to Fig. 3.3 by

$$\hat{i}_{\text{o}} = G_{\text{io-c}}^{\text{out}}\hat{i}_{\text{in}} - Y_{\text{o-c}}^{\text{out}}\hat{u}_{\text{o}} + G_{\text{co-c}}^{\text{out}}G_{\text{vc}}^{\text{in}}\left(G_{\text{se}}^{\text{in}}\hat{u}_{\text{in}} - \hat{u}_{\text{ref}}^{\text{uin}}\right). \tag{3.31}$$

Substituting (3.29) into (3.31) yields

$$\begin{aligned}\hat{i}_{\text{o}} =& \left(\frac{G_{\text{io-c}}^{\text{out}}}{1-L_{\text{in}}} - \frac{L_{\text{in}}}{1-L_{\text{in}}}G_{\text{io-}\infty}^{\text{out}}\right)\hat{i}_{\text{in}} - \left(\frac{Y_{\text{o-c}}^{\text{out}}}{1-L_{\text{in}}} - \frac{L_{\text{in}}}{1-L_{\text{in}}}Y_{\text{o-}\infty}^{\text{out}}\right)\hat{u}_{\text{o}}\\ & - \frac{1}{G_{\text{se}}^{\text{in}}}\frac{L_{\text{in}}}{1-L_{\text{in}}}\frac{G_{\text{co-c}}^{\text{out}}}{G_{\text{ci-c}}^{\text{out}}}\hat{u}_{\text{ref}}^{\text{uin}},\end{aligned} \tag{3.32}$$

where

$$G_{\text{io-}\infty}^{\text{out}} = G_{\text{io-c}}^{\text{out}} - \frac{Z_{\text{in-c}}^{\text{out}}G_{\text{co-c}}^{\text{out}}}{G_{\text{ci-c}}^{\text{out}}}, \tag{3.33}$$

$$Y_{\text{o-}\infty}^{\text{out}} = Y_{\text{o-c}}^{\text{out}} + \frac{T_{\text{oi-v}}^{\text{out}}G_{\text{co-c}}^{\text{out}}}{G_{\text{ci-c}}^{\text{out}}}. \tag{3.34}$$

The closed-loop input dynamics of the converter under the cascaded control scheme can be summarized according to (3.29) as given in (3.35)-(3.37). Substituting the output-current-controlled-converter transfer functions (3.22)-(3.24) into (3.35)-(3.37) yields the closed-loop transfer functions given by the original open-loop trasfer functions as defined in (3.38)-(3.40)

$$Z_{\text{in-c}}^{\text{out-in}} = \frac{\hat{u}_{\text{in}}}{\hat{i}_{\text{in}}} = \frac{Z_{\text{in-c}}^{\text{out}}}{1-L_{\text{in}}} \tag{3.35}$$

$$T_{\text{oi-c}}^{\text{out-in}} = \frac{\hat{u}_{\text{in}}}{\hat{u}_{\text{o}}} = \frac{T_{\text{oi-c}}^{\text{out}}}{1-L_{\text{in}}} \tag{3.36}$$

$$G_{\text{ci-c}}^{\text{out-in}} = \frac{\hat{u}_{\text{in}}}{\hat{u}_{\text{ref}}^{\text{uin}}} = \frac{1}{G_{\text{se}}^{\text{in}}}\frac{L_{\text{in}}}{1-L_{\text{in}}} \tag{3.37}$$

$$Z_{\text{in-c}}^{\text{out-in}} = \frac{Z_{\text{in-o}}}{(1+L_{\text{out}})(1-L_{\text{in}})} + \frac{L_{\text{out}}}{(1+L_{\text{out}})(1-L_{\text{in}})} Z_{\text{in-}\infty} \tag{3.38}$$

$$T_{\text{oi-c}}^{\text{out-in}} = \frac{T_{\text{oi-o}}}{(1+L_{\text{out}})(1-L_{\text{in}})} + \frac{L_{\text{out}}}{(1+L_{\text{out}})(1-L_{\text{in}})} \left(T_{\text{oi-}\infty} + \frac{G_{\text{ci-o}}}{G_{\text{co-o}}} Y_{\text{ff}} \right) \tag{3.39}$$

$$G_{\text{ci-c}}^{\text{out-in}} = \frac{1}{G_{\text{se}}^{\text{in}}} \frac{L_{\text{in}}}{1-L_{\text{in}}} \tag{3.40}$$

The closed-loop output dynamics of the converter under the cascaded control scheme can be summarized according to (3.32) as given in (3.41)-(3.43), and the substitution of the output-current-controlled converter output dynamics from (3.25)-(3.27) into (3.41)-(3.43) yields (3.44)-(3.46).

$$G_{\text{io-c}}^{\text{out-in}} = \frac{\hat{i}_{\text{o}}}{\hat{i}_{\text{in}}} = \frac{G_{\text{io-c}}^{\text{out}}}{1-L_{\text{in}}} - \frac{L_{\text{in}}}{1-L_{\text{in}}} G_{\text{io-}\infty}^{\text{out}} \tag{3.41}$$

$$Y_{\text{o-c}}^{\text{out-in}} = \frac{\hat{i}_{\text{o}}}{\hat{u}_{\text{o}}} = \frac{Y_{\text{o-c}}^{\text{out}}}{1-L_{\text{in}}} - \frac{L_{\text{in}}}{1-L_{\text{in}}} Y_{\text{o-}\infty}^{\text{out}} \tag{3.42}$$

$$G_{\text{co-c}}^{\text{out-in}} = \frac{\hat{i}_{\text{o}}}{\hat{u}_{\text{ref}}^{\text{uin}}} = -\frac{1}{G_{\text{se}}^{\text{in}}} \frac{L_{\text{in}}}{1-L_{\text{in}}} \frac{G_{\text{co-c}}^{\text{out}}}{G_{\text{ci-c}}^{\text{out}}} \tag{3.43}$$

$$G_{\text{io-c}}^{\text{out-in}} = \frac{G_{\text{io-o}}}{(1+L_{\text{out}})(1-L_{\text{in}})} - \frac{L_{\text{in}}}{1-L_{\text{in}}} G_{\text{io-}\infty} \tag{3.44}$$

$$Y_{\text{o-c}}^{\text{out-in}} = \frac{Y_{\text{o-o}}}{(1+L_{\text{out}})(1-L_{\text{in}})} - \frac{L_{\text{in}}}{1-L_{\text{in}}} Y_{\text{o-}\infty} - \frac{L_{\text{out}}}{(1+L_{\text{out}})(1-L_{\text{in}})} Y_{\text{ff}} \tag{3.45}$$

$$G_{\text{co-c}}^{\text{out-in}} = -\frac{1}{G_{\text{se}}^{\text{in}}} \frac{L_{\text{in}}}{1-L_{\text{in}}} \frac{G_{\text{co-o}}}{G_{\text{ci-o}}} \tag{3.46}$$

The closed-loop output admittance $Y_{\text{o-c}}^{\text{out-in}}$ in (3.45) shows that at the frequencies lower than the input-voltage-loop-gain crossover frequency, the input-voltage loop gain L_{in} attenuates the feedforward-admittance (Y_{ff}) term, and the low-frequency behavior of the output admittance is determined by $Y_{\text{o-}\infty}$. This is beneficial for the utility grid because in case of the cascaded control scheme, the negative-resistor-like behavior of the inverter output impedance is located between the crossover frequencies of the input-voltage and output-current loops, whereas in output-current-controlled converter such behavior also dominates at the low frequencies.

3.4 Control-system design

In this section, control-system-design examples are shown for the VSI and CFSQBB-type inverters. The controllers are designed in the continuous time domain by utilizing typical loop-shaping techniques. The continuous controllers are transformed into the discrete

time domain by bilinear transformation for the practical utilization in a microprocessor-based control system (Franklin et al., 1998).

3.4.1 VSI-type inverter

The VSI-type PV inverter is shown in Fig. 3.4 with its control system. The sensing functions are first-order low-pass filters with the cut-off frequency tuned at half the switching frequency. The low-frequency gain of the equvalent input and output-current-sensing resistors $R_{\mathrm{eq}}^{\mathrm{in}}$ and $R_{\mathrm{eq}}^{\mathrm{out}}$ as well as the input-voltage-sensing gain $G_{\mathrm{se}}^{\mathrm{in}}$ is set to unity. The low-frequency gain of the output-voltage-sensing gain $G_{\mathrm{se}}^{\mathrm{out}}$ is set to $1/U_{\mathrm{o}}$. The modulator gain G_{a} is also set to unity. In addition, it includes the processing delay of the discrete control-system implementation by second-order Padé approximation, which only affects the phase behavior of G_{a}, starting from approximately decade lower than the sampling frequency. The sampling frequency used in this thesis is the same as the switching frequency of the converter. The calculation of the numerical closed-loop transfer functions is provided in Appendix C as a Matlab script.

The current-controller design is based on the output-current loop L_{out} given in (3.16), where the main contributor is the control-to-output-current transfer function $G_{\mathrm{co\text{-}o}}$. The source-affected control-to-output-current transfer function $G_{\mathrm{co\text{-}o}}^{\mathrm{SA}}$ incorporates the operating-point-dependent zero given in (2.57) that is located on the RHP in the CCR and on the LHP in the CVR. At the MPP, the zero is located at the origin as was shown earlier in Fig. 2.12.

If the output-current-controlled converter is designed to operate in the CCR in a stable manner, the control bandwidth of the current loop is, in practice, limited by the RHP-zero frequency. In a typical single-phase inverter, the RHP-zero frequency is in the order of a few tens of Hz at maximum. Such low-bandwidth output-current controller has no practical usage but will work as demonstrated in (Nousiainen et al., 2011a). A

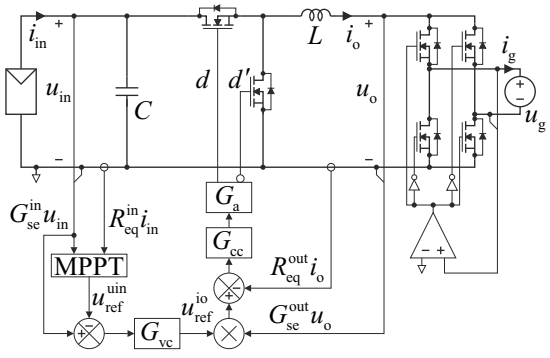


Fig. 3.4: VSI-type inverter and its control system.

high-bandwidth current loop can be easily designed in the CVR because the zero of $G_{\text{co-o}}^{\text{SA}}$ lies in the LHP and the converter dynamics resemble the first-order dynamics of the VSI fed by a voltage source. However, the converter becomes unstable with the high-bandwidth current loop when the operating point reaches the MPP or enters into the CCR as discussed earlier.

An output-current loop with a 4 kHz control bandwidth was designed in the CVR based on a conventional PI-type controller with an additional high-frequency pole as defined in (3.47), where $k_{\text{cc}} = 0.4$, $\omega_{\text{z-cc}} = 2\pi 500$ Hz and $\omega_{\text{p-cc}} = 2\pi 50$ kHz.

$$G_{\text{cc}} = k_{\text{cc}} \frac{s + \omega_{\text{z-cc}}}{s\left(\dfrac{s}{\omega_{\text{p-cc}}} + 1\right)}, \tag{3.47}$$

The high-frequency pole $\omega_{\text{p-cc}}$ was set to half the switching frequency in order to filter out high-frequency noise. The pole cannot be located at too low a frequency with respect to the bandwidth goal in order to not affect the phase margin (PM). The zero $\omega_{\text{z-cc}}$ is located at sufficiently high frequency in order to provide high low-frequency gain, but also the effect of the zero on the PM has to be considered, which limits its frequency. The gain k_{cc} sets the desired crossover frequency of the loop. The predicted source-affected output-current-loop gains are shown in Fig. 3.5 indicating that the phase (PM) and gain (GM) margins of the current loop are 60° and 11 dB, respectively. In terms of operating point, the loop gain clearly behaves as discussed above.

The dynamic properties of the input-voltage control are determined by the input-

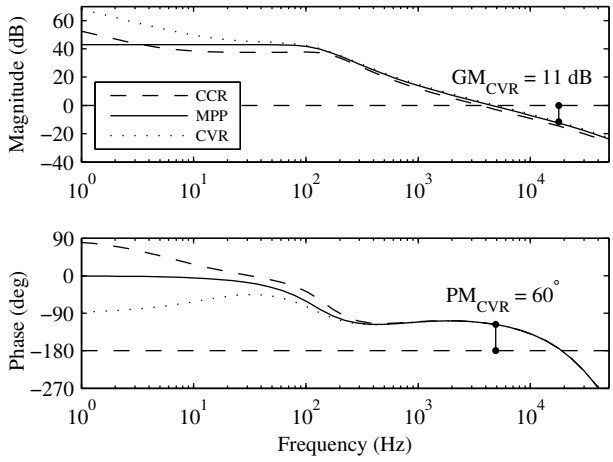


Fig. 3.5: Output-current-loop gain L_{out}.

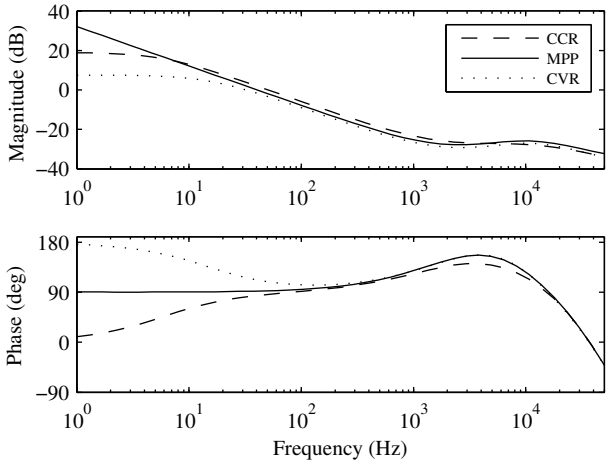


Fig. 3.6: Control-to-input-voltage transfer function of the output-current-controlled converter ($G_{\text{ci-c}}^{\text{out-SA}}$).

voltage-loop gain L_{in}, where the main contributor is the transfer function $G_{\text{ci-c}}^{\text{out}}$, given in (3.37), from the output-current reference to the input voltage. The source-affected $G_{\text{ci-c}}^{\text{out}}$ is shown in Fig. 3.6. The low-frequency phase of $G_{\text{ci-c}}^{\text{out-SA}}$ in Fig. 3.6 at the MPP is 90° due to a pole at the origin. The phase is 180° in the CVR due to a LHP pole and zero in the CCR due to a RHP pole. This can be explained by substituting the associated source-affected transfer functions without parasitic resistances into $G_{\text{ci-c}}^{\text{out}}$ yielding (3.48).

$$G_{\text{ci-c}}^{\text{out-SA}} = \frac{1}{R_{\text{eq}}^{\text{out}}} \frac{L_{\text{out}}}{1+L_{\text{out}}} \frac{-\dfrac{1}{LC}\left(U_{\text{o}} + I_{\text{o}} L s\right)}{\dfrac{U_{\text{in}}}{L}\left[s - \dfrac{1}{C}\left(\dfrac{1}{R_{\text{pv}}} - \dfrac{1}{r_{\text{pv}}}\right)\right]} G_{\text{se}}^{\text{out}} U_{\text{o}}. \tag{3.48}$$

Eq. (3.48) shows that the zero of the source-affected control-to-output-current transfer function $G_{\text{co-o}}^{\text{SA}}$ in (2.57) is transformed into a pole in the input-voltage loop when the bandwidth of the output-current loop is high (i.e. $L_{\text{out}}/(1+L_{\text{out}}) \approx 1$). In case of a RHP pole (i.e. the converter operates in the CCR), the bandwidth of the input-voltage loop has to be higher than the RHP-pole frequency for stable operation with a reasonable performance (Skogestad and Postlethwaite, 1998). Various papers discussing the input-voltage control of a PV inverter do not recognize the existence of the RHP pole (Kadri et al., 2011; Villanueva et al., 2009; Yazdani and Dash, 2009).

The input-voltage-control bandwidth of a single-phase inverter, on the other hand, is limited because of the power-fluctuation-induced input-voltage ripple at twice the grid

frequency. The ripple voltage passing the input-voltage controller will pollute the grid-current reference with the second harmonic component. Therefore, sufficient attenuation is needed at the named frequency. In practice, the input-voltage-control bandwidth of a single-phase inverter is typically limited to a few tens of Hertz. This implies that the allowable input-voltage-control bandwidth has a certain range between the RHP pole and the ripple frequencies. Therefore, the RHP pole, which is inversely proportional to the input capacitance, has to be located at a sufficiently low frequency. Later in this chapter this observation is used to derive a rule for minimum input capacitance.

Due to the minimum-bandwidth requirement of the input-voltage control, the worst-case operating point in terms of the input-voltage control can be defined to be the point where the PV current is the highest and the PV voltage is the lowest, because then the RHP-pole frequency is the highest. The input-voltage controller of the inverter was designed in the CCR by using the PI-type controller defined in (3.49), where $k_{\mathrm{vc}} = 0.4$, $\omega_{\text{z-vc}} = 2\pi 4$ Hz and $\omega_{\text{p-vc}} = 2\pi 75$ Hz. The pole and zero of the voltage controller are located in a similar manner as the pole and zero of the current controller.

$$G_{\mathrm{vc}} = k_{\mathrm{vc}} \frac{s + \omega_{\text{z-vc}}}{s\left(\dfrac{s}{\omega_{\text{p-vc}}} + 1\right)}, \tag{3.49}$$

The predicted input-voltage loop gains at the three operating points are shown in Fig. 3.7. Minimum PM of 49° is obtained with a crossover frequency of 22 Hz. It can be deduced that the PM is always positive at voltages higher than the MPP voltage. The

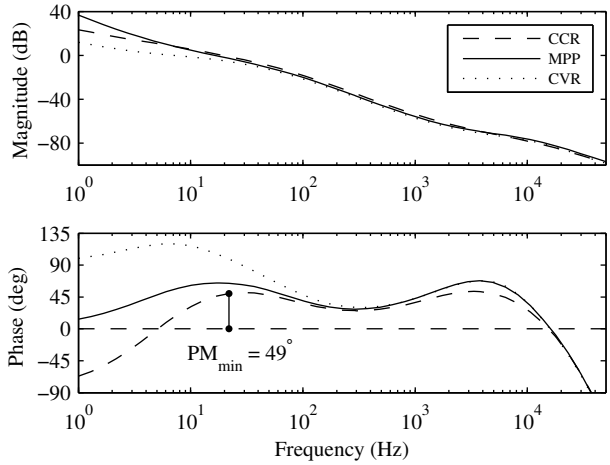


Fig. 3.7: Input-voltage-loop gain L_{in}.

PM can be construed as the difference between the loop phase and zero, because the voltage reference has to be subtracted from the measurement (i.e. the control signal has to be increased to decrease the input voltage).

3.4.2 Semi-quadratic buck-boost-type inverter

The inverter based on the CFSQBB converter utilizing the unfolder is shown in Fig. 3.8 with its control system, where $G_{\mathrm{se}}^{\mathrm{in}}$, $G_{\mathrm{se}}^{\mathrm{im}}$ and $G_{\mathrm{se}}^{\mathrm{out}}$ are the input, intermediate and output-voltage sensing gains, $R_{\mathrm{eq}}^{\mathrm{in}}$ and $R_{\mathrm{eq}}^{\mathrm{out}}$ are the equivalent input and output-current sensing resistors, $G_{\mathrm{vc}}^{\mathrm{in}}$ and $G_{\mathrm{vc}}^{\mathrm{im}}$ denote the input and intermediate-voltage controllers and G_{cc} denotes the output-current controller. The sensing gains are first-order low-pass filters tuned at half the switching frequency, whose low-frequency gain is set to unity, exept $G_{\mathrm{se}}^{\mathrm{out}}$, whose low-frequency gain is set to $1/U_{\mathrm{o}}$. The modulator gain G_{a} is set to unity and includes the processing delay. The CFSQBB inverter employs the two-stage conversion scheme, where input-voltage control is implemented at the PVG side and the cascaded control scheme at the grid side. The operating-point related parameters and the component values of the converter are given in Table 3.1. The transfer functions presented in this section can be calculated according to Appendix D.

The source-affected transfer function $G_{\mathrm{ci1\text{-}o}}^{\mathrm{SA}}$ between the duty ratio $\hat{d}_1$ and the input voltage u_{in} in the three operating points defined in Table. 3.1 is shown in Fig. 3.9. The difference between the operating points is in the damping of the transfer function $G_{\mathrm{ci1\text{-}o}}^{\mathrm{SA}}$. When the operating point is moved to the higher voltages, especially above the MPP voltage, low r_{pv} attenuates the resonant behavior of $G_{\mathrm{ci1\text{-}o}}^{\mathrm{SA}}$. Design of the low-bandwidth

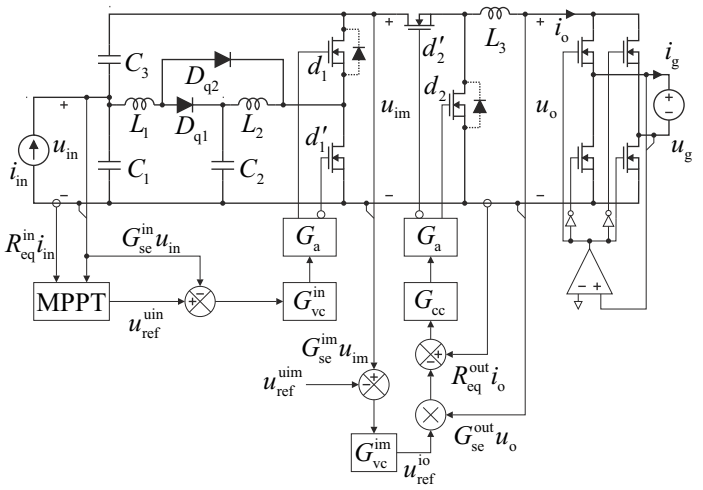


Fig. 3.8: Semi-quadratic buck-boost-type inverter and its control system.

Table 3.1: Operating-point parameters of the CFSQBB inverter.

	I_{in} (A)	U_{in} (V)	U_{im} (V)	U_{o} (V)	r_{pv} (Ω)	f_{sw} (kHz)
CCR	7.84	15.0	370	230	56.0	
MPP	7.33	25.9	370	230	3.5	150
CVR	5.70	29.0	370	230	0.8	
	C_1 (μF)	L_1 (μH)	C_2 (μF)	L_2 (μH)	C_3 (μF)	L_3 (μH)
	20	220	20	1000	660	1000

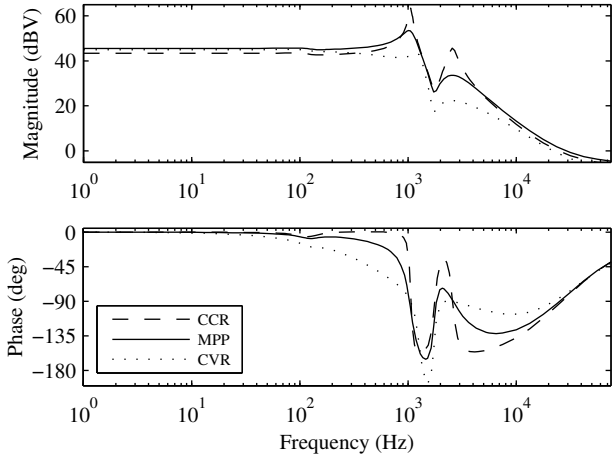


Fig. 3.9: Control-to-input-voltage transfer function $G_{\mathrm{ci1\text{-}o}}^{\mathrm{SA}}$.

integral-type (I) input-voltage controller defined in (3.50) is a straightforward task. The controller gain $k_{\mathrm{in}} = 1.2$ is selected to keep the peaking of the resonance in the input-voltage loop $L_{\mathrm{in}} = G_{\mathrm{se}}^{\mathrm{in}} G_{\mathrm{vc}}^{\mathrm{in}} G_{\mathrm{a}} G_{\mathrm{ci1\text{-}o}}^{\mathrm{SA}}$ at approximately 1 kHz well below the 0 dB line as shown in Fig. 3.10, which shows the input-voltage-loop gain in the three different operating points. The resulting minimum phase and gain margins of the input-voltage-control loop according to Fig. 3.10 are 12 dB and 86°, respectively.

$$G_{\mathrm{vc}}^{\mathrm{in}} = \frac{k_{\mathrm{in}}}{s} \tag{3.50}$$

The transfer function between the output current $\hat{i}_{\mathrm{o}}$ and the duty ratio $\hat{d}_2$ when the input-side control is at open loop ($G_{\mathrm{co2\text{-}o}}$) is shown in Fig. 3.11 with the source effect, whereas Fig. 3.12 shows the same transfer function when the input-side control is at closed loop ($G_{\mathrm{co2\text{-}c}}^{\mathrm{in}}$), which can be solved by substituting the duty ratio $\hat{d}_1$, which can be solved from Fig. 3.8, into the open-loop transfer function set of the CFSQBB given

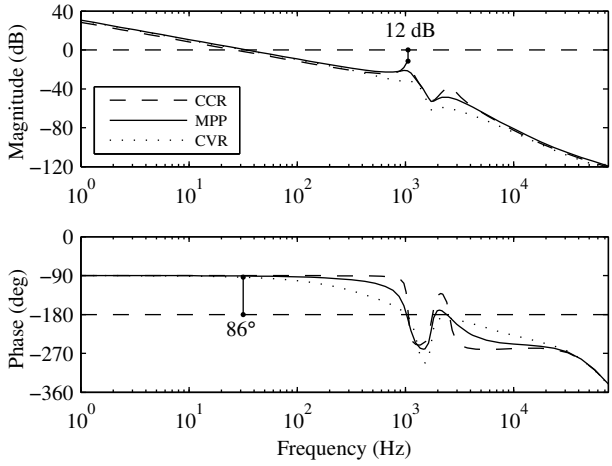


Fig. 3.10: Input-voltage-loop gain L_{in}.

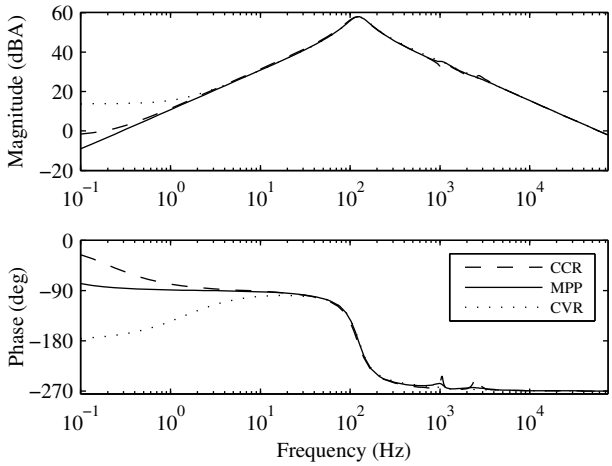


Fig. 3.11: Control-to-output-current transfer function $G^{\mathrm{SA}}_{\mathrm{co2\text{-}o}}$.

in (2.86). According to Nousiainen and Suntio (2011), $G^{\mathrm{in}}_{\mathrm{co2\text{-}c}}$ can be given as shown in (3.51), where the superscript 'in' denotes that the input-voltage-control loop is connected.

$$G^{\mathrm{in}}_{\mathrm{co2\text{-}c}} = G_{\mathrm{co2\text{-}o}} - \frac{L_{\mathrm{in}}}{1 + L_{\mathrm{in}}} \frac{G_{\mathrm{co1\text{-}o}} G_{\mathrm{ci2\text{-}o}}}{G_{\mathrm{ci1\text{-}o}}}. \tag{3.51}$$

Fig. 3.11 shows that the output-current-control loop has similar operating-point-dependent zero as the VSI-type PV inverter that shifts between the left and right halves

of the complex plane when the CFSQBB operates at open loop. Fig. 3.12 shows that the input-voltage control shifts the zero very close to the origin regardless of the operating point as discussed earlier, which simplifies the design of the cascaded control loop. The output-current-loop gains $L_{\text{out}} = R_{\text{eq}}^{\text{out}} G_{\text{cc}} G_{\text{a}} G_{\text{co2-c}}^{\text{in}}$ are shown in Fig. 3.13. The PI-type output-current controller is shown in (3.52), where $k_{\text{cc}} = 0.05$, $\omega_{\text{z-cc}} = 2\pi 50$ kHz and $\omega_{\text{p-cc}} = 2\pi 1$ kHz. The stability of L_{out} is determined by the location of the aforementioned zero, which still may locate either on the RHP or the LHP depending on e.g.

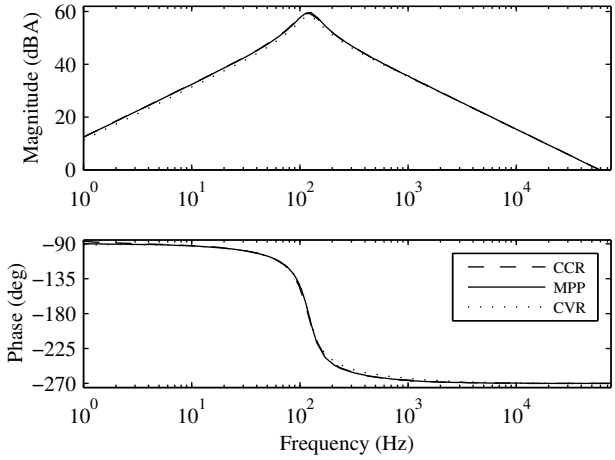


Fig. 3.12: Control-to-output-current transfer function $G_{\text{co2-c}}^{\text{in-SA}}$ when the input-voltage loop is connected.

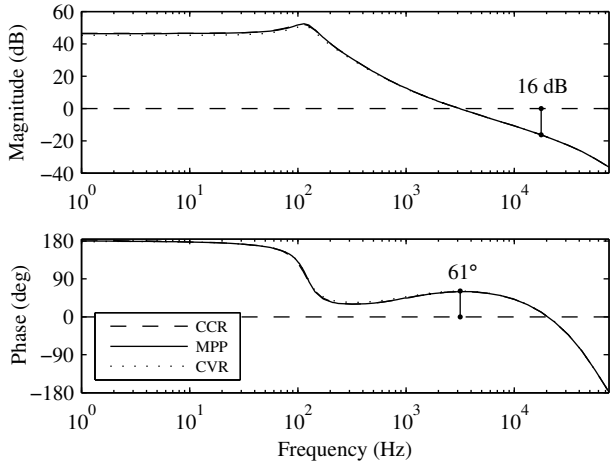


Fig. 3.13: Output-current-loop gain L_{out}.

parasitics or other anomalies in the system, although very close to the origin. Nevertheless, the intermediate voltage loop is needed to guarantee proper intermediate voltage level in the changing conditions even if the converter was theoretically stable at steady state without it.

$$G_{\mathrm{cc}} = k_{\mathrm{cc}} \frac{s + \omega_{\mathrm{z\text{-}cc}}}{s\left(\dfrac{s}{\omega_{\mathrm{p\text{-}cc}}} + 1\right)}, \tag{3.52}$$

The transfer function between the output-current reference $\hat{u}_{\mathrm{ref}}^{\mathrm{io}}$ and the intermediate voltage $\hat{u}_{\mathrm{im}}$ can be given according to Nousiainen and Suntio (2011) by

$$G_{\mathrm{cim2\text{-}c}}^{\mathrm{in\text{-}out}} = -\frac{L_{\mathrm{out}}}{1 - L_{\mathrm{out}}} \frac{G_{\mathrm{cim2\text{-}c}}^{\mathrm{in}}}{G_{\mathrm{co2\text{-}c}}^{\mathrm{in}}} \frac{1}{R_{\mathrm{eq}}^{\mathrm{out}}} G_{\mathrm{se}}^{\mathrm{out}} U_{\mathrm{o}}, \tag{3.53}$$

where

$$G_{\mathrm{cim2\text{-}c}}^{\mathrm{in}} = G_{\mathrm{cim2\text{-}c}} - \frac{L_{\mathrm{in}}}{1 + L_{\mathrm{in}}} \frac{G_{\mathrm{cim1\text{-}o}} G_{\mathrm{ci2\text{-}o}}}{G_{\mathrm{ci1\text{-}o}}}. \tag{3.54}$$

The intermediate-voltage-controller design is based on the soure-affected transfer function (3.53), which is shown at the three operating points in Fig. 3.14. The PI-type intermediate voltage controller is defined in (3.55), where $k_{\mathrm{vc}}^{\mathrm{im}} = 0.1$, $\omega_{\mathrm{z\text{-}vc}}^{\mathrm{im}} = 2\pi 5$ Hz and $\omega_{\mathrm{p\text{-}vc}}^{\mathrm{im}} = 2\pi 50$ Hz. The resulting intermediate-voltage-loop gains $L_{\mathrm{im}} = G_{\mathrm{se}}^{\mathrm{im}} G_{\mathrm{vc}}^{\mathrm{im}} G_{\mathrm{cim2\text{-}c}}^{\mathrm{in\text{-}out}}$ are shown in Fig. 3.15, where the phase margin is 55° and the control bandwidth ap-

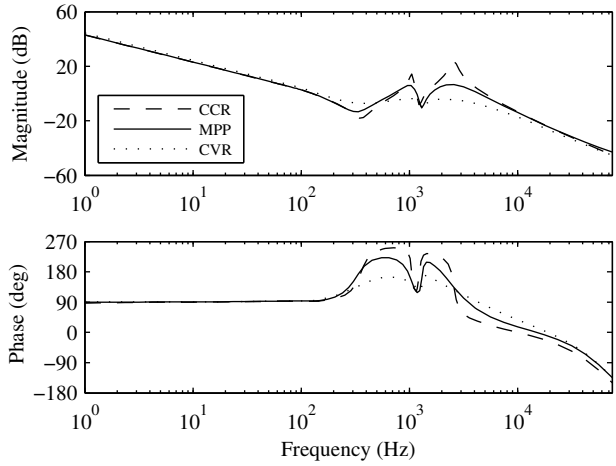


Fig. 3.14: Control-to-intermediate voltage transfer function $G_{\mathrm{cim2\text{-}c}}^{\mathrm{in\text{-}out\text{-}SA}}$.

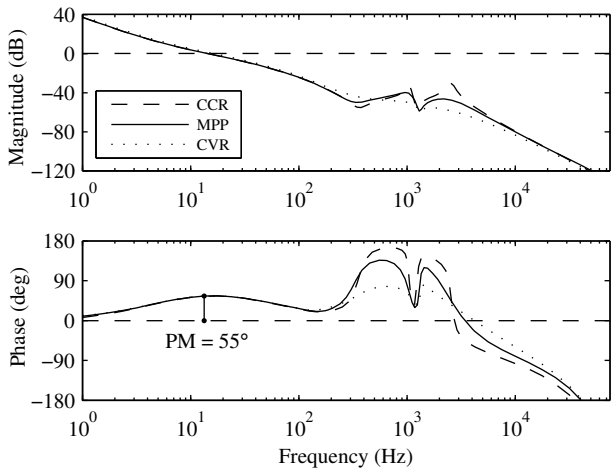


Fig. 3.15: Intermediate-voltage-loop gain L_{im}.

proximately 15 Hz.

$$G_{\mathrm{vc}}^{\mathrm{im}} = k_{\mathrm{vc}}^{\mathrm{im}} \frac{s + \omega_{\mathrm{z\text{-}vc}}^{\mathrm{im}}}{s\left(\dfrac{s}{\omega_{\mathrm{p\text{-}vc}}^{\mathrm{im}}} + 1\right)}, \tag{3.55}$$

3.5 Negative output impedance in VSI-type inverter

According to (3.26), the behavior of the output-current-controlled converter output admittance $Y_{\mathrm{o\text{-}c}}^{\mathrm{out}}$ is determined at frequencies lower than the output-current-loop gain crossover frequency by the feedforward admittance Y_{ff} with a negative coefficient. According to (3.17), the feedforward admittance is a pure conductance, and therefore $Y_{\mathrm{o\text{-}c}}^{\mathrm{out}}$ behaves as a negative incremental conductance within the output-current-control bandwidth. The output admittances of the output-current controlled VSI are shown in Fig. 3.16 at the three operating points. Fig. 3.16 clearly demonstrates the negative-incremental-conductance-like behavior of the output admittance at the low frequencies. The low-frequency magnitude also demonstrates the power-dependency of the feedfoward admittance, i.e. at higher power levels the problem is more severe.

The closed-loop output admittance $Y_{\mathrm{o\text{-}c}}^{\mathrm{out\text{-}in}}$ in (3.45) shows that the input-voltage loop gain L_{in} attenuates the negative feedforward admittance term at the frequencies below the input-voltage-loop gain crossover frequency, where the low-frequency behavior of the output admittance is determined by $Y_{\mathrm{o\text{-}\infty}}$. Accordingly, in case of the cascaded

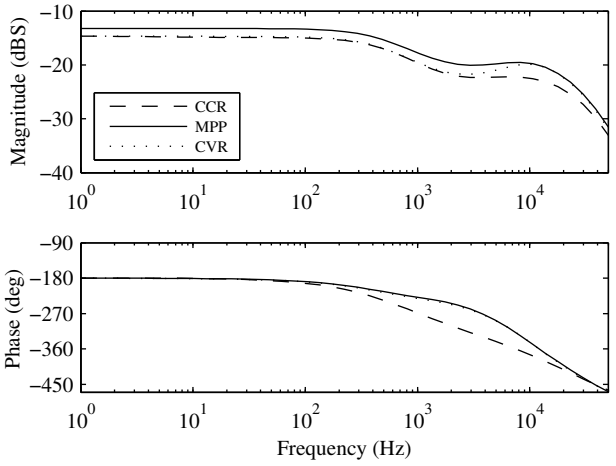


Fig. 3.16: Output admittance of the output-current-controlled VSI ($Y_{\text{o-c}}^{\text{out-SA}}$).

control scheme, the negative-incremental-conductance-like behavior is located between the crossover frequencies of the input-voltage and output-current-loop gains, whereas in the output-current-controlled converter such behavior dominates from dc up to the output-current-loop-gain crossover frequency. Therefore, the inverter/grid interface is not prone to minor-loop-gain induced low-frequency instability but the instability would likely take place at the harmonic frequencies. Fig. 3.17 shows the output admittances of the VSI under the cascaded control scheme in the three operating points. The output admittances clearly bahave in terms of the negative-incremental conductance as discussed above.

Fig. 3.18 shows the output admittances of the VSI under the cascaded control scheme when $Y_{\text{ff}} = 0$, i.e. the synchronization has no effect on the output admittance. It can be depicted from Fig. 3.18 and Fig. 3.17 that the output admittance has some negative-incremental-conductance behavior due to the cascaded control scheme, which is amplified by the grid synchronization at the named frequencies. The grid synchronization also reduces the current-source property of the inverter by increasing the magnitude of the output admittance. The negative-conductance-like output admittance makes the inverter prone to instability and contributes to the harmonic resonance problems in the utility grid as discussed earlier. It is crucial to trace the origins of such behaviour to enable large-scale utilization of renewable energy systems relying on power electronics technology.

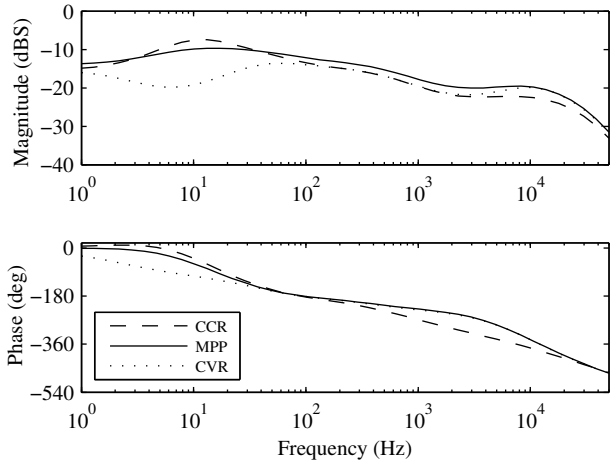


Fig. 3.17: Output admittance of the VSI with cascaded control scheme ($Y_{\text{o-c}}^{\text{out-in-SA}}$).

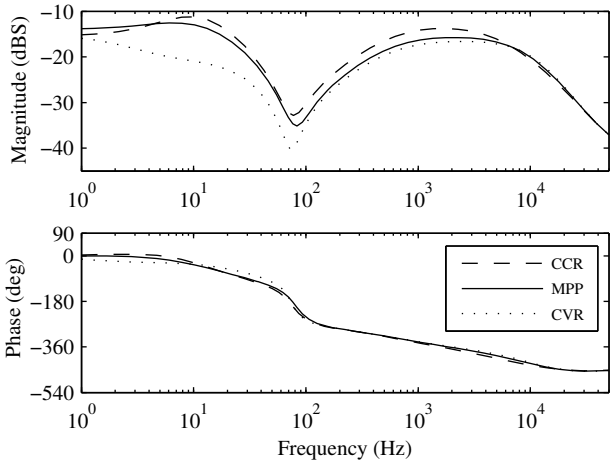


Fig. 3.18: Output admittance $Y_{\text{o-c}}^{\text{out-in-SA}}$ when $Y_{\text{ff}} = 0$.

3.6 Input-capacitor selection of VSI-type inverter

It is a common practice to connect a capacitor at the input terminals of the VSI-type PV inverter for power decoupling purposes. The type of the input capacitor plays a key role in improving the reliability of the PV inverter as discussed by Petrone et al. (2008). Electrolytic capacitors are usually used because they have high capacitance to volume ratios and are relatively cheap. However, electrolytic capacitors are known to have limited life times at elevated temperatures. Minimizing the input capacitance would allow the

use of other types of capacitors which would not have similar life-limiting properties as the electrolytic capacitors have. On the other hand, the input-capacitor minimization has been observed to introduce e.g. sub-harmonic oscillation problems or even instability (Fratta et al., 2002).

Traditionally, the design criteria in the input capacitor selection of VSI-type inverters have originated from the energy stored in the dc-link capacitor. Energy-based design criteria leads to constraints between the capacitance and e.g. maximum input voltage ripple or maximum input voltage overshoot or dip during the load transients (Fratta et al., 2002; Gu and Nam, 2005; Liserre et al., 2004). This section proposes a new design constraint for the input capacitance based on the observed RHP pole in the input-voltage-control loop of the cascaded control scheme taking into account the limitations imposed by the single-phase inverter input-voltage ripple.

3.6.1 Input-voltage-ripple-based constraint

The single-phase inverter output power inherently fluctuates at twice the grid frequency. This can be explained by formulating the time-varying grid power assuming sinusoidal grid voltage and current in phase with each other by

$$p_{\mathrm{grid}} = \sqrt{2}U_{\mathrm{grid}}\sin\left(\omega_{\mathrm{grid}}t\right)\sqrt{2}I_{\mathrm{grid}}\sin\left(\omega_{\mathrm{grid}}t\right) = P_{\mathrm{grid}}\left[1-\cos\left(2\omega_{\mathrm{grid}}t\right)\right], \tag{3.56}$$

where U_{grid}, I_{grid} and P_{grid} are the RMS grid voltage, current and power, and the grid angular frequency is denoted by ω_{grid}. Consequently, the same power fluctuation is evident at the dc-side of the VSI-type inverter. Assuming constant input current and high dc-value in the input voltage compared to the ripple component (i.e. $P_{\mathrm{in}}/u_{\mathrm{in}} \approx I_{\mathrm{in}}$), a simple equation can be solved for the capacitor current given by

$$i_{\mathrm{C}} = C\frac{\mathrm{d}u_{\mathrm{C}}}{\mathrm{d}t} = I_{\mathrm{in}} - I_{\mathrm{in}}\left[1-\cos\left(2\omega_{\mathrm{grid}}t\right)\right] = I_{\mathrm{in}}\cos\left(2\omega_{\mathrm{grid}}t\right), \tag{3.57}$$

which can be used to approximate the input-voltage ripple. Integration of (3.57) with the assumptions of $u_{\mathrm{in}} = u_{\mathrm{C}}$, initial input voltage is U_{C} and assuming ideal conversion efficiency yields

$$u_{\mathrm{in}} = U_{\mathrm{in}} + \frac{I_{\mathrm{in}}}{2\omega_{\mathrm{grid}}C}\sin\left(2\omega_{\mathrm{grid}}t\right), \tag{3.58}$$

from where the peak-to-peak input-voltage ripple can be solved by

$$\Delta u_{\mathrm{in}} = \frac{I_{\mathrm{in}}}{\omega_{\mathrm{grid}}C}. \tag{3.59}$$

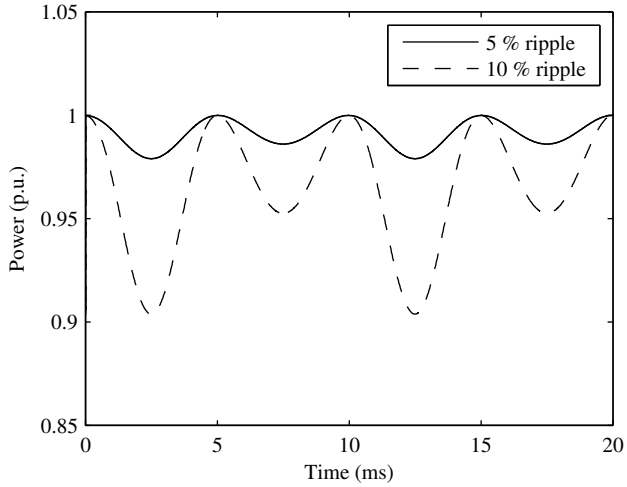


Fig. 3.19: PV power fluctuation due to input-voltage ripple at twice the grid frequency.

Eq. (3.59) gives an estimate for the input-voltage ripple component of a single-phase PV inverter. The input-voltage-feedback loop has to be designed in such a way that sufficient attenuation is obtained at the ripple frequency in order to prevent the ripple from polluting the grid current reference, and thus the grid current, with the second harmonic component (Brekken et al., 2002). On the other hand, any fluctuation of the operating point around the MPP will decrease the PVG utilization ratio, i.e. the ratio of the MPP power and the actual average power of the PVG. Fig. 3.19 illustrates the effect of 100 Hz PVG voltage ripple on the PVG output power, where the ripple component is either 5 % or 10 % of the MPP voltage. Accordingly, the input capacitor has to be large enough for acceptable PVG utilization ratio.

3.6.2 Control-system-design-based constraint

As has been discussed earlier, a photovoltaic inverter requires a cascaded input-output control scheme where the outer grid-current-feedback loop controls the grid gurrent and the inner input-voltage-feedback loop controls the input voltage according to the reference generated by the MPPT facility. The dynamic properties of the input-voltage-feedback loop in such a case are determined by the transfer function $G_{\text{ci-c}}^{\text{out}}$ in (3.24) between the input voltage $\hat{u}_{\text{in}}$ and the output-current reference $\hat{u}_{\text{ref}}^{\text{io}}$. Because the control-to-output-current transfer function $G_{\text{co-o}}$ is in the denominator in (3.24), the RHP zero in $G_{\text{co-o}}$ given in (2.48) may be transformed into a RHP pole.

Assuming high bandwidth grid-current control (i.e., $L_{\text{out}}/\left(1+L_{\text{out}}\right) \approx 1$), the source-affected $G_{\text{ci-c}}^{\text{out}}$ in (3.48) has a pole approximately at the same frequency as the zero

in the source-affected $G_{\text{co-o}}$ defined in (2.57). Accordingly, the location of the pole in $G_{\text{ci-c}}^{\text{out-SA}}$ on the complex plane is defined in the same manner as the location of the zero defined in (2.58). I.e., the control-to-input-voltage transfer function $G_{\text{ci-c}}^{\text{out-SA}}$ has a RHP pole when the operating point is located in the CCR of a PVG. In case of a RHP pole in the control loop, the loop-gain crossover frequency ω_{loop} has to be greater than the RHP-pole frequency in order to achieve stable operation with reasonable control performance as defined by Skogestad and Postlethwaite (1998). Kolar et al. (2011) defines a factor of two between the necessary crossover frequency and the RHP pole frequency for acceptable control performance. However, a control-system design should be verified in each application also by the relevant phase and gain margins in the feedback loop.

A VSI-type single-phase inverter requires a minimum input voltage $U_{\text{in-min}}$ that is the peak value of the grid voltage with sufficient margin. This minimum-voltage operating point most probably lies in the CCR of a PVG, since the MPP voltage cannot be specified as the minimum input voltage due to uncertainties in the PVG configuration and environmental conditions. The worst case operating point in terms of the input-voltage control occurs when the RHP-pole frequency is the highest, which according to (2.57) can be given by

$$\omega_{\text{RHP-max}} = \frac{I_{\text{in-max}}}{U_{\text{in-min}} C_{\text{min}}}, \tag{3.60}$$

because in the CCR $r_{\text{pv}} >> R_{\text{pv}}$. An inequality for the voltage-loop crossover frequency ω_{loop} can be given according to (3.60) and ω_{grid} by

$$k_{\text{grid}}\omega_{\text{grid}} \geq \omega_{\text{loop}} \geq k_{\text{RHP}}\omega_{\text{RHP,max}}. \tag{3.61}$$

A safety factor $k_{\text{RHP}} = 2$ in (3.61) is proposed e.g. by Kolar et al. (2011). Brekken et al. (2002) defines a safety factor $k_{\text{grid}} = 2/10$ to determine the maximum input-voltage-loop crossover for single-phase inverter in high input-voltage-ripple conditions (i.e., minimum input capacitor is connected), although higher bandwidths may be achieved with larger capacitors.

Because the worst-case operating point is assumed to exist in the CCR, the maximum input current $I_{\text{in-max}}$ could be assumed to be the short-circuit current of the PVG (I_{sc}), because in the CCR $i_{\text{pv}} \approx I_{\text{sc}}$. According to Chen, Li, Brady and Lehman (2010), PV inverters are sized according to a certain threshold irradiance lower than the irradiance in standard test conditions (1000 W/m^2, 1.5 spectrum air mass). I.e., according to Chen, Li, Brady and Lehman, an example 10 kW peak power system could be interfaced to the utility grid using a 7 kW inverter in order to find an optimum balance between the inverter costs and the costs due to loss of energy caused by the undersized inverter operating at the lower power levels than the potential maximum PV power.

Some studies show that the global solar irradiation combined of the direct and diffuse components may well exceed the 1000 W/m^2 or even the solar constant of 1361 W/m^2 (i.e., solar irradiance spectrum at top of the atmosphere) (Luoma et al., 2012). The excess irradiance is caused by e.g. dry air formations and particles in higher atmospheric levels according to Balafas et al. or cloud enhancement according to Luoma et al.. Such excess irradiance could compromise the inverter stability based on (3.60) and (3.61), especially if the inverter is undersized as discussed earlier. A maximum input current can thus be presented as $I_{\text{in,max}} = k_{\text{i}} I_{\text{sc}}$, where a safety margin $k_{\text{i}} = 1.5$ is selected based on observed maximum momentary irradiances of 1500 W/m^2 by Luoma et al.. Combining the rules in (3.60) and (3.61), a minimum input capacitance C_{min} guaranteeing stable operation of a single-stage single-phase VSI-type PV inverter in all possible operating points along the PVG IV-curve can be given by

$$C_{\text{min}} = \frac{k_{\text{RHP}} k_{\text{i}}}{k_{\text{grid}}} \frac{I_{\text{sc}}}{U_{\text{in-min}} \omega_{\text{grid}}}. \tag{3.62}$$

Fig. 3.20 illustrates the proposed constraints between the minimum input capacitance normalized by the PVG short-circuit current ($C_{\text{min}}/I_{\text{sc}}$) and the input-voltage-loop crossover frequency ($k_{\text{grid}}\omega_{\text{grid}}$) for the single-stage single-phase VSI-type PV inverter based on (3.62). The border between stable and unstable regions is obtained using $k_{\text{i}} = 1$ and $k_{\text{RHP}} = 1$, i.e. without the safety margins. However, the figure also presents the minimum capacitance when the safety margins discussed earlier are included ($k_{\text{i}} = 1.5$ and $k_{\text{RHP}} = 2$). The minimum input voltage is assumed to be 340 V for the single-phase

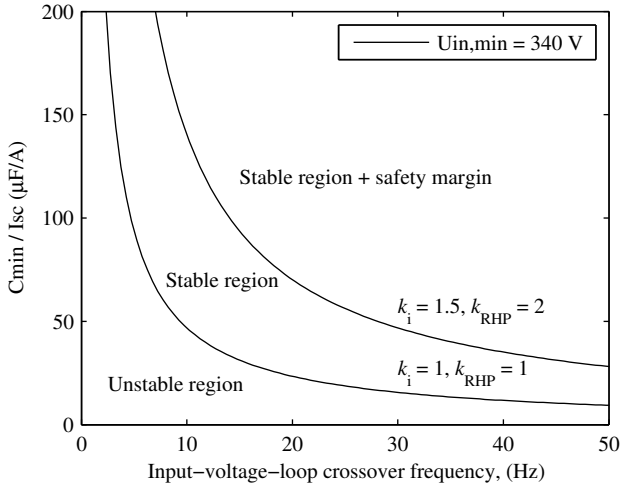


Fig. 3.20: $C_{\text{min}}/I_{\text{sc}}$ as a function of voltage-loop crossover frequency f_{loop}.

inverter in a 230 V utility grid (peak voltage is 325 V). According to Fig. 3.20, the control-system-based design criterion becomes significant with low input-voltage-loop-bandwidth requirement. It can be approximated that a reasonable trade-off between the minimum input capacitance and the voltage-loop crossover is between 10–30 Hz for the single-phase inverter, which results in capacitances between 50–150 μF/A.

Based on the analysis presented in this section, the input-voltage-control instability could occur in a single-phase PV inverter for two possible reasons. Either the input voltage controller bandwidth is designed to be too low compared to the RHP pole frequency and the converter operation could be stabilized by retuning the controller according to $\omega_{\text{loop}} \geq k_{\text{RHP}}\omega_{\text{RHP,max}}$ in (3.61). In another case, the input-voltage-control bandwidth cannot be increased due to the violation of the rule $k_{\text{grid}}\omega_{\text{grid}} \geq \omega_{\text{Loop}}$ in (3.61). In such a case, the only option is to increase the input capacitance so that the frequency of the RHP pole $\omega_{\text{RHP-max}}$ in (3.60) would be well below the input-voltage-loop crossover ω_{loop}. In either case, stable operation of a PV inverter can be guaranteed only by considering the sizing constraint between the input capacitance and the input-voltage-control-loop crossover as presented.

Typically, the input capacitor design is based on energy-based design criteria, e.g. input-voltage ripple or transient behavior. The energy-based criteria are important, although subjective, and do not necessarily guarantee inverter stability. Therefore, in addition to the energy-based criteria, the proposed control-system-based rule has to always be considered because it determines inverter stability which results in more reliable and robust PV inverter design.

4 EXPERIMENTAL MEASUREMENTS

This chapter presents experimental verification for the theoretical findings presented earlier in this thesis. The properties of a PVG are verified with respect to the properties of a commercial solar array simulator. A small-scale VSI-type inverter is used to verify the effect of the PVG on the interfacing converter and the validity of the proposed input-capacitor-design rule as well as the property of negative-incremental-resistor-like behavior in the output impedance of the inverter caused by the multiplier-based grid synchronization. A full-scale single-PV-module-fed CFSQBB inverter prototype is implemented in order to verify its dynamic modeling and claimed properties as well as its feasibility in the intended application.

The control systems of the experimental inverters are implemented with a eZdspF28335 controller board manufactured by Spectrum Digital based on Texas Instruments' floating-point processor. The frequency responses have been measured using Venable Instruments' frequency response analyzer Model 3120 with an impedance measurement kit. In addition to the frequency responses, the conventional time-domain measurements are used to verify the information given by the frequency-domain analyses and to emphasize their importance.

4.1 Photovoltaic generator & solar array simulator

The input source has a significant effect on interfacing converter dynamics as discussed in Chapter 2. A PVG is internally a power-limited non-linear current source having both constant-current (CC) and constant-voltage (CV) like properties depending on the operating point, which implies that the dynamics of a PV interfacing converter cannot be validated solely by using a voltage or current source as the input source. Therefore, the validation should be performed using a real PVG as the input source.

If a real PVG is to be used in the converter validation process, an artificial light source providing controllable illumination should be used to guarantee the repeatability of the measurements. This can be accomplished cost-effectively in small scale but is impractical for larger systems. Therefore, a PVG is usually replaced with a power electronic substitute, i.e. a solar array simulator, so that the time-invariant conditions can be guaranteed in the validation process. The input sources used in the experimental measurements were Raloss SR30-36 PV module composed of 36 series-connected monocrystalline silicon cells

illuminated by an artificial light unit and Agilent E4360A solar array simulator. The purpose of this section is to validate the theoretical analysis regarding the PVG as an input source and prove the feasibility of the used solar array simulator for later usage.

In the standard test conditions (1000 W/m^2 irradiance, 1.5 spectrum air mass, 25 °C module temperature), the Raloss PV module produces short-circuit current of 1.9 A, open-circuit voltage of 21.8 V, and maximum power of 30.8 W. The module was illuminated by a fluorescent lamp unit that was able to produce an irradiance level of approximately 500 W/m^2 yielding short-circuit current of 1.0 A and open-circuit voltage of 19.2 V at the module temperature of approximately 45 °C. The MPP current of the artificially-illuminated module was 0.91 A at the voltage of 15.9 V.

The measured impedances of the Raloss PV module are shown in Fig. 4.1 in open-circuit (OC) and short-circuit (SC) conditions as well as at the MPP. The dynamic resistance r_{pv} represents the low-frequency value of the impedance, and is the most significant variable that will have an effect on the interfacing converter dynamics as discussed earlier. The dynamic capacitance, in turn, can be approximated from the PVG impedance (Fig. 4.1) as

$$c_{\mathrm{pv}} \approx \frac{1}{2\pi r_{\mathrm{pv}} f_{\text{-3dB}}}, \tag{4.1}$$

where $f_{\text{-3dB}}$ is the cut-off frequency of the impedance magnitude curve. Eq. (4.1) gives a good estimate for c_{pv} in the CCR, since $r_{\mathrm{d}}||r_{\mathrm{sh}} >> r_{\mathrm{s}}$. In the CVR, (4.1) slightly underestimates c_{pv} since $r_{\mathrm{d}}||r_{\mathrm{sh}}$ and r_{s} are in the same order of magnitude, but is still

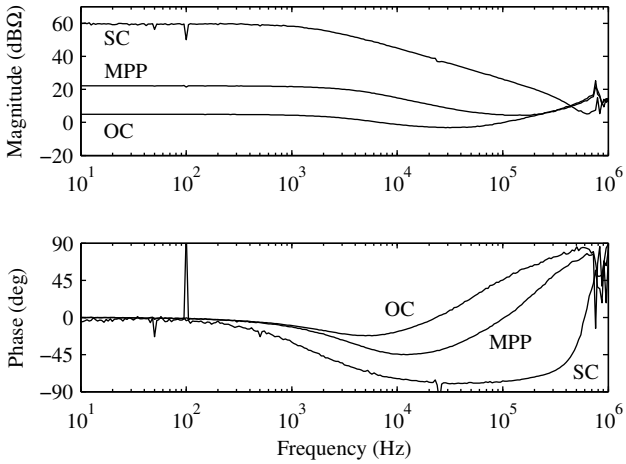


Fig. 4.1: PVG impedances at short circuit (SC), maximum power point (MPP) and open circuit (OC).

sufficiently accurate.

The tested commercial power electronic substitute has three different modes of operation: SAS, table and fixed modes. In SAS-mode, the simulator is programmed using three reference points: short circuit current and open circuit voltage as well as current and voltage at the MPP. In the table-mode, the IV-curve is represented by voltage-current pairs with a limitation that the voltage points must be ascending and the current points descending. In fixed mode, a maximum voltage is given and the simulator operates as a voltage limited current source having rectangular IV-curve characteristics.

Measured dynamic resistances and capacitances from the Raloss PV module and the Agilent solar array simulator are shown in Figs. 4.2 and 4.3. Later on in the figures, the solar array simulator at the two different operating modes will be referred to as 'Table' and 'SAS'. Based on r_{pv} of the real PVG, it can be seen that the curve has two distinct slopes. Because r_{pv} is presented in dBΩ, it is clear that r_{pv} would be best approximated with a two-diode (i.e. double exponential) model as opposed to the single-diode model of Fig. 2.8, although the single-diode model is sufficient in most cases in power-electronic applications (Villanueva et al., 2009). The same double-exponential characteristics are also visible in Fig. 4.3, which presents the measured dynamic capacitances.

Based on Fig. 4.2, the solar array simulator produces similar double-exponential characteristics in respect to r_{pv} when it is used in the table-mode. However, its dynamic resistance in the SAS-mode is constant in the CV region as can be seen in Fig. 4.2. This indicates that the dynamic resistance of a real PVG can be emulated with higher precision by using the table mode. The operating mode of the solar array simulator does not affect the emulated dynamic capacitance as can be seen in Fig. 4.3. The capacitance of the

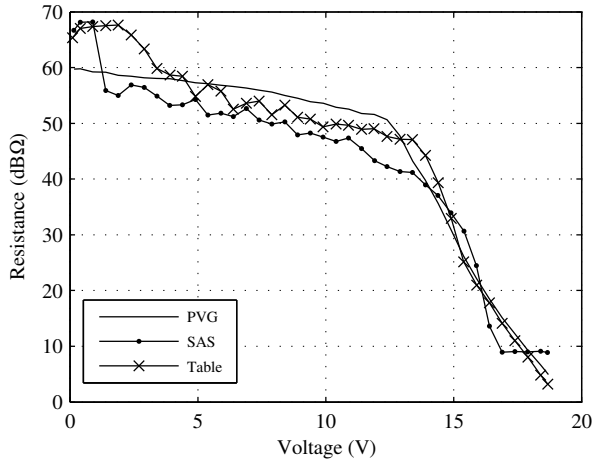


Fig. 4.2: Measured dynamic resistances.

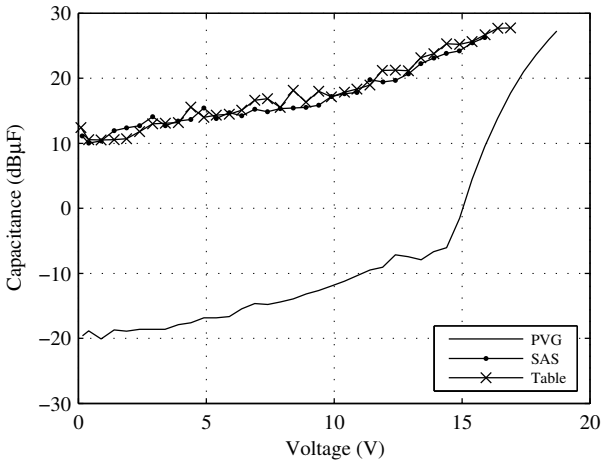


Fig. 4.3: Measured dynamic capacitances.

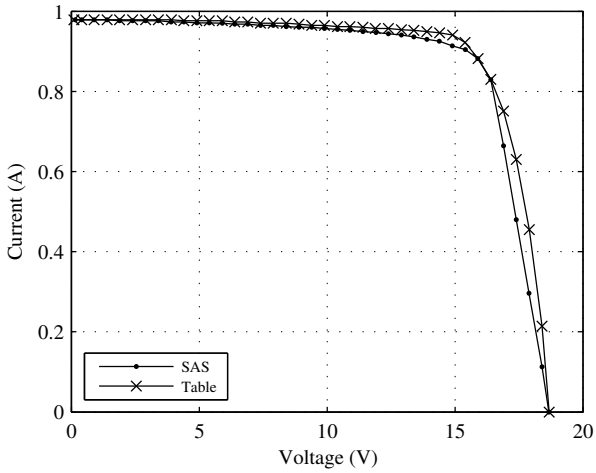


Fig. 4.4: Solar array simulator IV-curve comparison.

solar array simulator is considerably higher (up to 30 dBμF higher) than the capacitance of the real PVG and it does not show the double-exponential characteristics.

Fig. 4.4 presents the IV-curves of solar array simulator in SAS and table-modes. It was stated earlier that the dynamic resistance in the SAS-mode is constant in the CV region. Constant dynamic resistance implies that the IV-curve is a straight line in the CV region as can be noticed from Fig. 4.4. In table-mode, the solar array simulator produces the IV-curve correctly, and thus also the dynamic resistance as was analyzed in Section 2.4. It is worth noting that a solar array simulator can produce the dynamic resistance of a PVG correctly only if the simulator produces the IV-curve correctly when

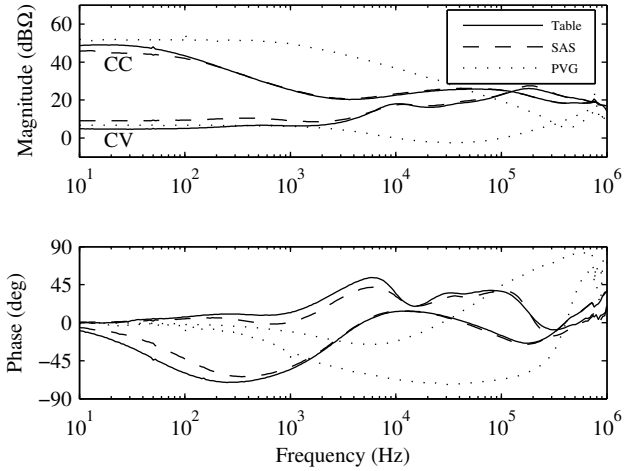


Fig. 4.5: Impedance comparison.

loaded with the specific power electronic device under test.

Figs. 4.2-4.3 compared the PVG and the electronic substitute in terms of r_{pv} and c_{pv}. Fig. 4.5 presents the measured PVG and solar array simulator impedances in the CCR and CVR of the IV-curve. By considering the impedance in the CCR, the solar array simulator shows PVG-like characteristics but with a higher capacitance up to ca. 2 kHz. The impedance in the CVR correlates up to the same frequency range. After the ca. 2 kHz frequency the solar array simulator impedance does not show similar resistive-capacitive characteristics as the real PVG does. Figs. 4.1 and 4.5 show that the phase of the PVG impedance lies between $\pm 90°$. A solar array simulator should show similar passive-circuit-like characteristics so that it would be justified to substitute the PVG with the solar array simulator, as is the case in Fig. 4.5. The higher capacitance of the solar array simulator can affect the behavior of a converter having small input capacitor but is small enough not to affect typical single-phase PV inverters.

4.2 VSI-based inverter

The VSI-type inverter was fed by the Raloss PV module illuminated with the artificial light unit in the measurements. Fig. 4.6 shows the source-affected control-to-output-current transfer functions ($G^{\mathrm{SA}}_{\mathrm{co\text{-}o}}$) in the CCR and CVR as wells as at the MPP. The frequency responses behave as the analytic transfer function given in (2.55) predict. In the CVR, the location of the zero defined in (2.57) is clearly in the LHP and the transfer function begins to follow the properties of the VF VSI (first-order dynamics and low-frequency phase of 0°). In the CCR, the low-frequency phase is 180° and the zero lies in

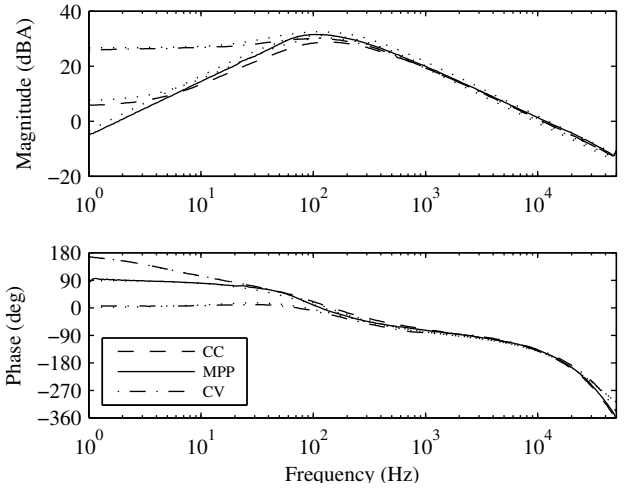


Fig. 4.6: Measured and predicted control-to-output-current transfer functions ($G^{\mathrm{SA}}_{\mathrm{co\text{-}o}}$). The predictions marked with dotted lines overlap with the measurements.

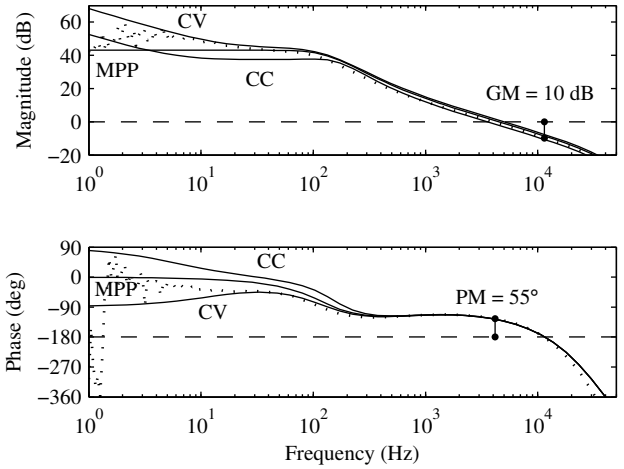


Fig. 4.7: Measured (dotted line) and predicted output-current loop gains (L_{out}).

the RHP similarly as the zero of the nominal CF VSI showing the second-order dynamics compared to the VF VSI. At the MPP, the low-fequency phase of the transfer function is 90°, which means that the zero is located at the origin of the complex plane. It can be concluded that the CF VSI model with the effect of the PVG dynamic resistance produces accurate models of the inverter dynamics.

Fig. 4.7 shows the output-current-loop gain L_{out} in the CVR with the controller design given in Section 3.4. The loop gain was measured only in the CVR, because the output-

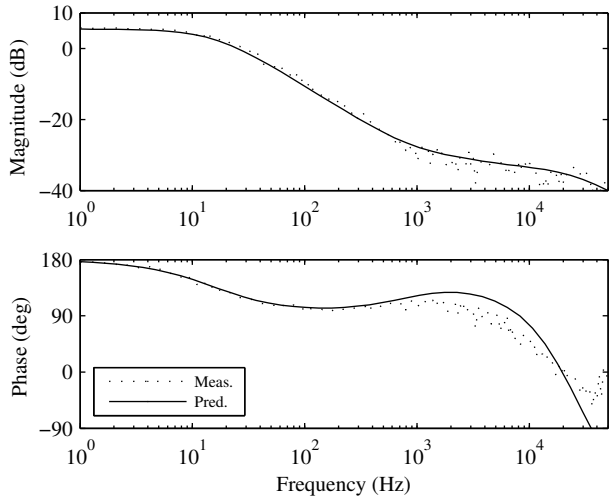


Fig. 4.8: Control-to-input-voltage transfer function $G_{\text{ci-c}}^{\text{out-SA}}$ in the CVR.

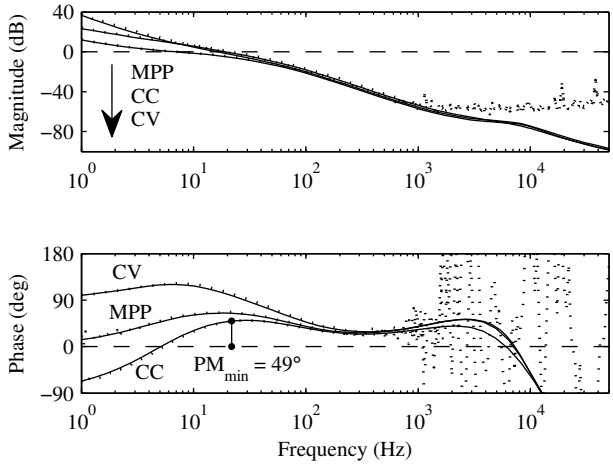


Fig. 4.9: Measured (dotted line) and predicted input-voltage loop gains (L_{in}).

current-controlled converter becomes unstable as the operating point reaches the MPP, and therefore cannot be measured at the MPP or in the CCR. It can be concluded from Fig. 4.7 that the discrete-time controller correlates with the designed continuous-time controller because the measured loop gain follows the predicted one.

The source-affected transfer function between the output-current reference and the input voltage $G_{\text{ci-c}}^{\text{out-SA}}$ is also a property of the output-current-controlled converter, and therefore can be measured only in the CVR as shown in Fig. 4.8, which verifies the validity

of the transfer function (3.48). The transfer function $G_{\text{ci-c}}^{\text{out-SA}}$ provides the tool for the input-voltage-control design. Eq. (3.48) showed that the zero of the control-to-output-current transfer function G_{co} is transformed into a pole in $G_{\text{ci-c}}^{\text{out}}$. Fig. 4.8 corresponds to the analysis as the low-frequency pole is clearly located in the LHP.

The input-voltage controller designed in Section 3.4 was transported into the microprosessor and the measured input-voltage-loop gains L_{in} are presented in Fig. 4.9. The low-frequency phase of L_{in} in Fig. 4.9 effectively demonstrates the movement of the pole along the complex plane as it does in Fig. 4.6. It can be deduced that the worst-case operating point for the input-voltage control is the minimum-input-voltage operating point as also concluded earlier. The minimum measured PM of the input-voltage-feedback loop was 49°.

4.2.1 Input-voltage-control stability

Fig. 4.10 illustrates the measurement and prediction of stable and unstable input-voltage loops for a single-phase VSI-type PV inverter in the CCR. Because the loop incorporates one RHP pole, the Nyquist contour must encircle the point (-1, 0) counterclockwise once for stable operation. The unstable loop is implemented to illustrate the feasibility of the design rule between the minimum inverter input capacitance and the stability of the input-voltage-feedback loop given in Section 3.6.2. Basically, the purpose is to vertically shift between the stable and unstable region in Fig. 3.20 by lowering the controller gain and thus the loop crossover frequency.

Time-domain evidence of the instability due to negative PM caused by the RHP pole

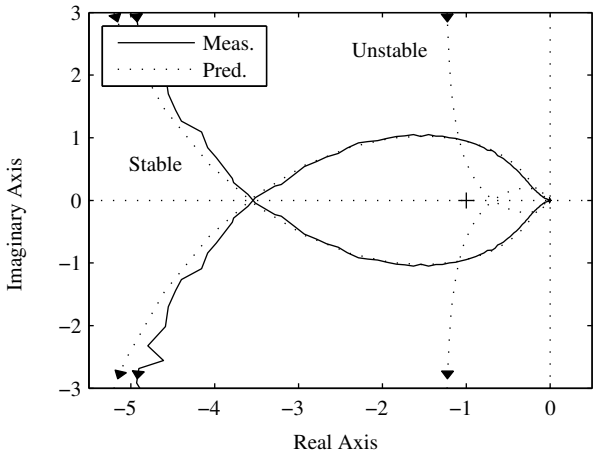


Fig. 4.10: Nyquist plots of input-voltage loop gains L_{in} in the CC region.

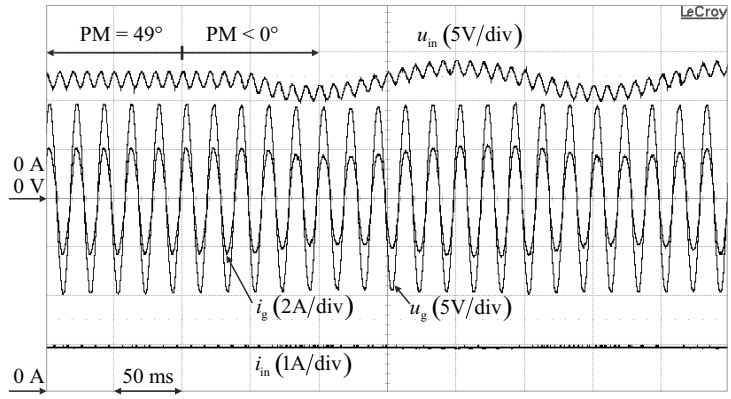


Fig. 4.11: Input-voltage oscillation in the CC region due to negative PM.

in the loop is presented in Fig. 4.11, where the controller gain, and therefore also the control bandwidth is lowered at 100 ms. The reduction of the loop gain changes the PM from the original 49° to a slightly negative value. The lower control bandwidth basically violates the control-theory rule which states that in case of a RHP pole in the loop, the control bandwidth has to be grater than the RHP pole frequency. The instability in Fig. 4.11 is evident as a sub-harmonic oscillation shown in the inverter output variables, i.e. the input voltage and output current.

This kind of instability was predicted earlier in Section 3.6.2 to occur in a PV inverter if the input voltage controller bandwidth is designed to be too low compared to the RHP pole frequency, as was the case in Fig. 4.11. In such a case, the converter can be stabilized by retuning the controller. However, it might be possible that the input-voltage-control bandwidth cannot be increased because the control bandwidth, on the other hand, has to be well below the double grid frequency in order to prevent the inherent input-voltage ripple at the double grid frequency from polluting the output-current reference with the second harmonic component. In such a case, the only option is to increase the input capacitance so that the frequency of the RHP pole would be well below the input-voltage-loop crossover frequncy. Nevertheless, the sizing constraint of the input capacitor with respect to the input-voltage control given in this thesis is a powerful tool to optimize the inverter design without compromising its low-frequency stability.

4.2.2 Negative output impedance

The measured and predicted closed-loop output admittances with and without the synchronization (i.e. $Y_{\mathrm{ff}} = 0$) at the MPP are shown in Fig. 4.12. The figure shows that the converter output admittance has some properties of the negative incremental conductance behavior originating from the cascaded control scheme, which is amplified by

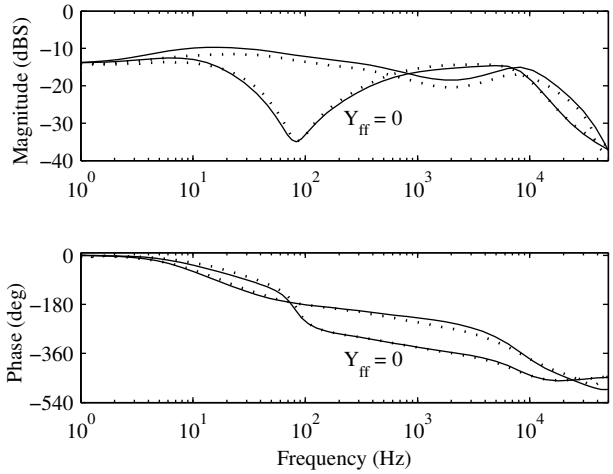


Fig. 4.12: Measured (dotted lines) and predicted $Y_{\text{o-c}}$ at the MPP.

the application of the multiplier-based grid synchronization at the frequencies between the output-current and input-voltage-loop gain crossover frequencies. This phenomenon may expose the inverter to instability, reduce damping in the grid and contribute to the harmonic resonance problems. The grid synchronization also reduces the current-source property of the inverter by increasing the magnitude of the output admittance.

It is well known and analyzed also in this thesis that the stability of an interconnected voltage-fed system can be assessed by applying the Nyquist stability criterion to the impedance ratio of the load and source subsystems known as the minor-loop gain, whereas the stability of a current-fed system has been shown to be determined by the inversion of the minor-loop gain. Violation of the inverse-minor-loop-gain-based stability criterion requires a condition where the input impedance of the load subsystem is greater in magnitude than the output impedance of the source subsystem (i.e. $Z_{\text{in}} > Z_{\text{o}}$) while the phase difference of the impedances exceeds 180°. The phase difference may exceed 180° if either the load or source subsystem possesses the property of the negative incremental conductance (or resistance). Therefore, it is obvious that the inverter with an output admittance shown in Fig. 4.12 is prone to instability where the problem is emphasized with the multiplier-based synchronization.

A CL-filter shown Fig. 4.13, whose input impedance is denoted by $Z_{\text{in}}^{\text{CL}}$, was connected at the output of the inverter in order to demonstrate the existence and effect of the negative-resistor-like behaviour. The measured inverse minor-loop gains ($Z_{\text{in}}^{\text{CL}} Y_{\text{o-c}}^{\text{out-in-SA}}$) in the CVR (solid line) and at the MPP (dashed line) are presented in Fig. 4.14 as Nyquist plots. The plots predict that the system is stable in the CVR but will become

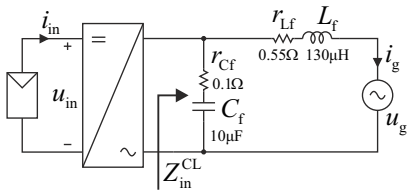


Fig. 4.13: Inverter cascaded with a CL-type filter.

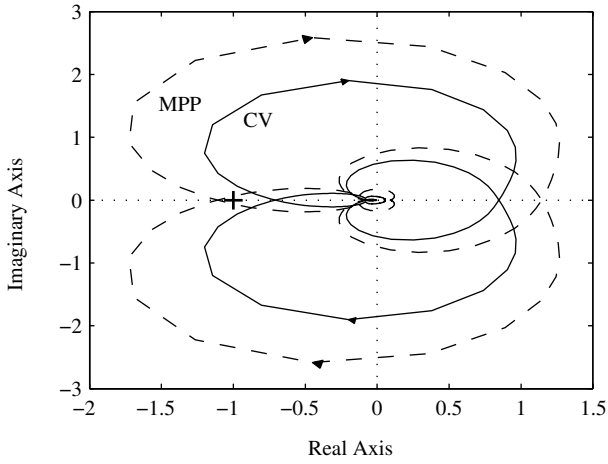


Fig. 4.14: Inverse minor-loop gains of the inverter/filter interface.

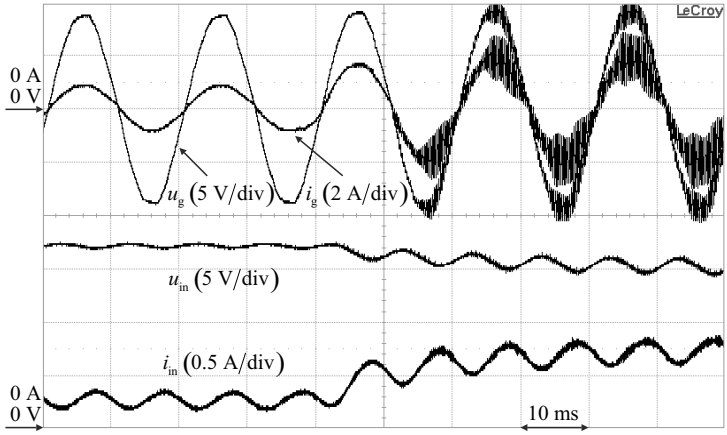


Fig. 4.15: Output-side oscillation due to negative output impedance.

unstable when the operating point shifts toward the MPP. Fig. 4.15 shows the time-domain behavior of the input and output voltages and currents when the operating point is moved from the CVR to the MPP validating the information given by Fig. 4.14.

4.3 Semi-quadratic buck-boost-type inverter

The CFSQBB inverter prototype was fed by the Agilent E4360A solar array simulator emulating a PV module having short-circuit current of 8.02 A, open-circuit voltage of 33.1 V, MPP voltage of 25.9V and the MPP current of 7.33A in the standard test conditions. Figs. 4.16 and 4.17 show the open-loop input impedance Z_{in} and the source-affected control-to-input-voltage transfer function $G_{\text{ci1-o}}^{\text{SA}}$ at the three operating points, respectively, with predicted transfer functions at the MPP. The predicted transfer func-

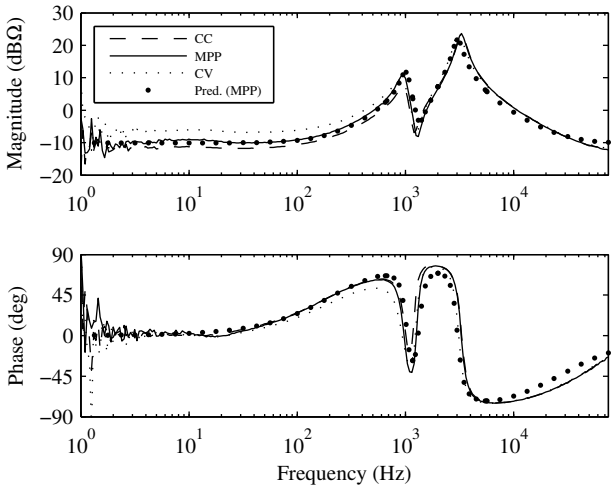


Fig. 4.16: Input impedance.

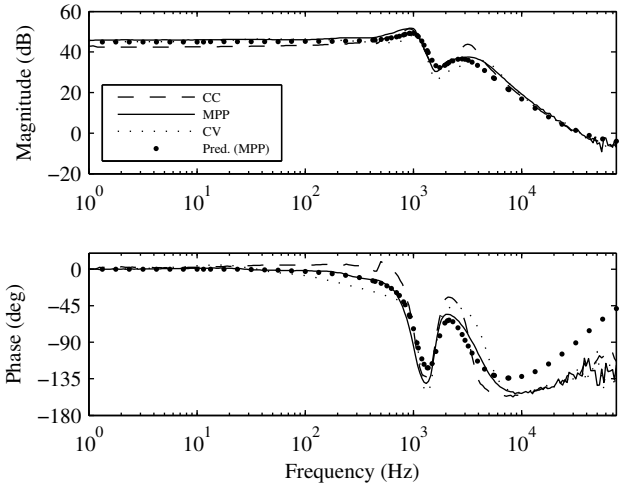


Fig. 4.17: Control-to-input-voltage transfer function.

tions correlate well with the measurements, and thereby validate the dynamic model of the CFSQBB presented earlier. The resonant behavior of $G_{\text{ci1-o}}^{\text{SA}}$ implies that the input-voltage controller should be designed in the CCR.

The CFSQBB converter's capability to handle the wide conversion ratios required by the PV micro inverters is demonstrated in Figs. 4.18 and 4.19, where the converter operates at its nominal MPP operating point given in Table 3.1. Thanks to the semi-quadratic conversion ratio, there is no need to apply extreme duty ratios, which are hard to implement at high switching frequencies in the practical converter. Fig. 4.18 shows the input and intermediate voltages ($u_{\text{in}}, u_{\text{im}}$, respectively) as well as the voltage over the capacitor C_2 (u_{C2}). Fig. 4.19 shows the inductor L_1, L_2 and L_3 currents ($i_{\text{L1}}, i_{\text{L2}}$, i_{L3}) that exhibit the same semi-quadratic conversion ratio as in Fig. 4.18. The high-

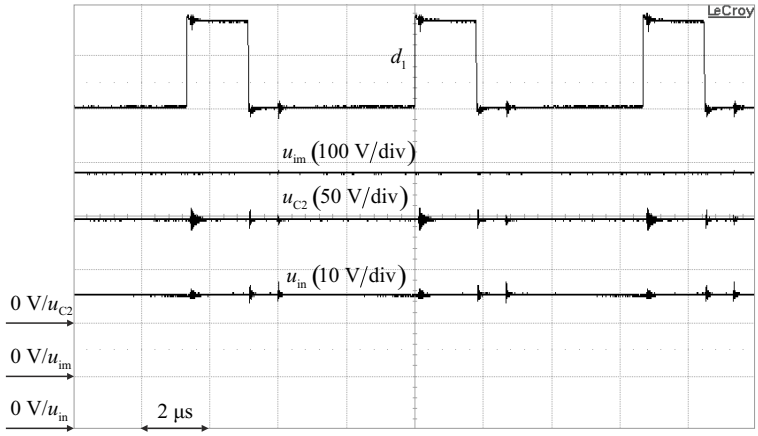


Fig. 4.18: Steady-state voltages of the CFSQBB.

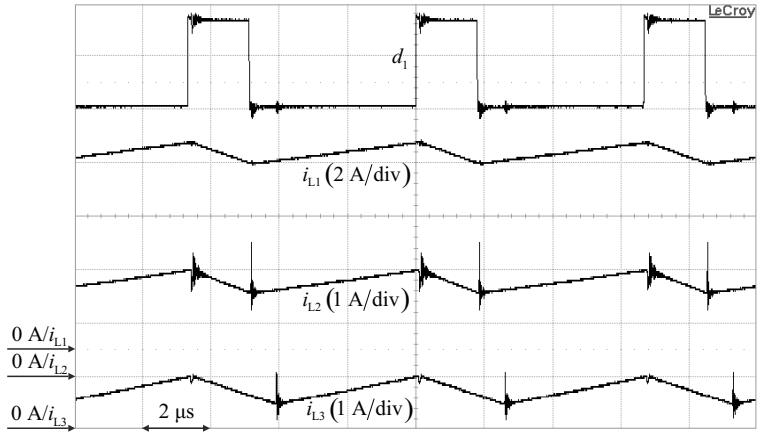


Fig. 4.19: Steady-state currents of the CFSQBB.

frequency noise in the inductor currents at the switching instances is due to small parasitic capacitances between the inductor windings.

The controllers defined in Section 3.4 were implemented with a microprocessor in order to prove the feasibility of the CFSQBB in the micro inverter application. Fig. 4.20 shows the grid voltage (u_g) and current (u_g) as well as the input and intermediate voltages of the CFSQBB inverter at steady state. The waveforms indicate a well-behaving control system. It can be seen that the input voltage is nearly pure dc without the need for large power decoupling capacitors to be connected at the inverter input terminals. The transient behavior of the inverter is shown in Fig. 4.21, where the input current is stepped from half to nominal, i.e. the figure demonstrates the CFSQBB inverter operation under changes in the irradiance. Such fast changes are not expected in a real PV application, but the inverter's ability to handle them predicts that the inverter will behave well during

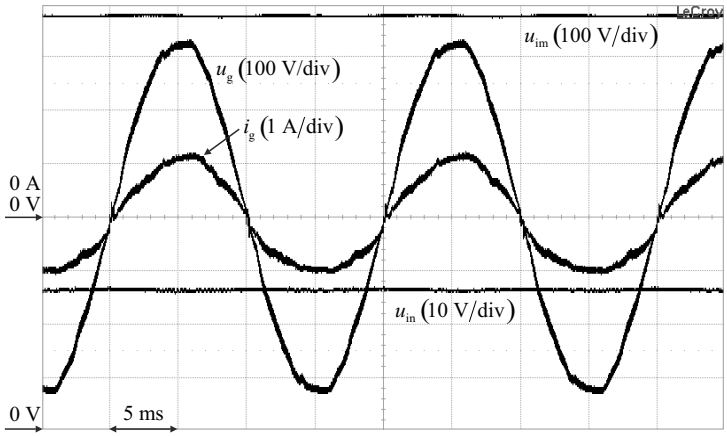


Fig. 4.20: Steady-state waveforms of the CFSQBB inverter.

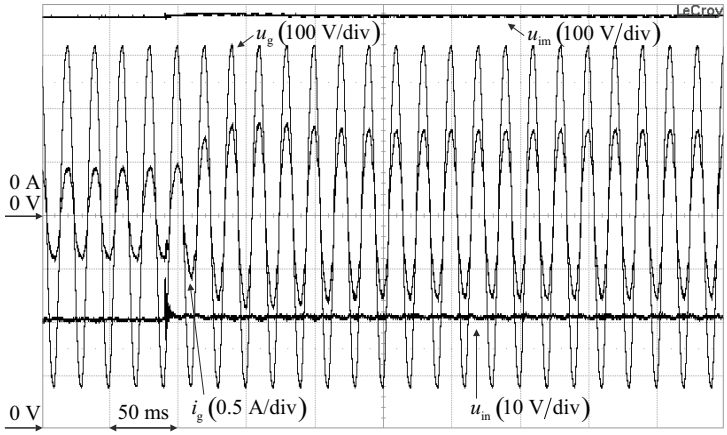


Fig. 4.21: CFSQBB inverter input-current step.

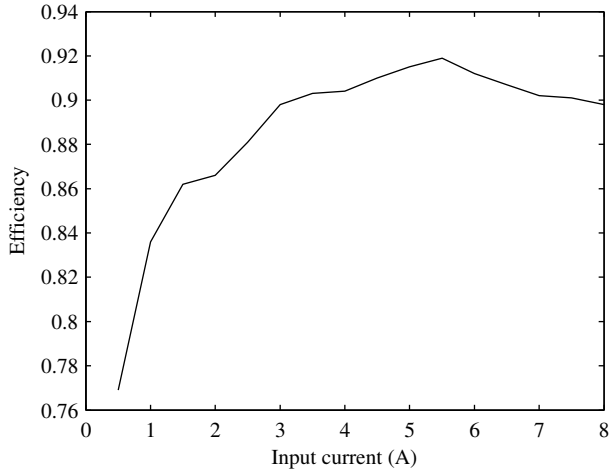


Fig. 4.22: CFSQBB efficiency.

all the natural changes in the irradiance.

The efficiency of a PV converter is an important factor in order to estimate the return of investment for the PV power plant and in order to compare the new converter topology to existing ones. The efficiency of the CFSQBB converter was measured in such a way that the operating point voltages were kept constant and the input current was varied, which gives a good estimate of the converter efficiency under changing irradiance. The CFSQBB efficiency is shown in Fig. 4.22 showing peak efficiency of approximately 92 %, which is a promising figure for an early prototype converter which was not fully optimized regarding efficiency.

5 SUMMARY OF THE THESIS

This chapter summarizes the thesis. A recap of the main scientific contributions and findings in the thesis are provided with discussion on important future research topics in the field of PV inverters that have come up during the thesis work.

5.1 Final conclusions

Grid connection is the way to fully exploit PV energy. A grid integration of the PVG requires at least an inverter between the PVG and the utility grid, but might also contain an additional dc-dc preregulator between the PVG and the inverter. The task of the PV inverter is to locate the MPP of the PVG and inject maximal high-quality current to the ultility grid. In the future, according to some studies, the inverters should include e.g. grid voltage supporting functions in order to maintain the stability of the grid although one inverter cannot control the grid voltage. The low efficiency of the PVG emphasizes the necessity for low-cost high-efficiency inverters in order to make the investment on the PV system economically feasible. One of the current solutions to the problem is the transformerless single-stage single-phase string inverter. The transformerless inverters are usually variations of VSI topologies with an additional input capacitor for enabling connection to the PVG and providing power decoupling. The main concern in the transformerless inverters is the elimination of ground-leakage current caused by the inverter common-mode voltage and the stray capacitor associated to the PV modules.

The transformerless single-phase VSI-type inverters require the dc-link voltage to be higher than the peak of the grid voltage. As a consequence, the PV input source has to be a high-voltage string or series connection of PV modules. Optimal operation of a string requires uniform irradiation conditions which is often not the case, especially in the built environment. In order to reduce the detrimental effects of the partial shading on energy production, PV-module-based micro-inverter concepts are used. The micro inverters are prone to reduced efficiency due to the required wide conversion ratio but have shown to be capable of outperforming the string-inverter systems, especially in the locations susceptible to partial shading.

This thesis studied the dynamic properties of a VSI-type PV inverter and proposed a new converter topology, known as current-fed semi-quadratic buck-boost converter, which cascaded with an unfolding full-bridge inverter forms a transformerless PV micro

inverter. The proposed topology is capable of handling wide conversion ratios that, with dedicated input-voltage control, yield good power decoupling without the need to connect a large capacitor bank to the input terminals of the converter. This thesis provides a dynamic model and control-system-design example for the proposed converter as well as experimental measurements proving its feasibility in the intended PV-micro-inverter application.

The PV and other renewable-energy-based inverters have been observed to suffer from reliability problems, reduce damping in the grid, excite harmonic resonances, and cause harmonic distortion. These phenomena are expected to increase in the future because of the advantageous public and political climates favoring renewable energies. Such problems can lead to production outages and compromise the stability of the utility grid. It has been shown that the stability and oscillatory behavior of an interconnected system composing of independently stable source and load subsystems can be assessed by the ratio of the corresponding source and load subsystem impedances. It was shown theoretically and by experimental measurements that negative-inceremental-resistor-like behavior at the output of the PV inverter makes the inverter/grid interface prone to instability. The negative-incremental-resistor-like behavior was observed to originate in the VSI-type PV inverter from the cascaded control scheme, which was significantly amplified by the multiplier-based grid synchronization. The synchronization also reduced the current-source property of the inverter by increasing the magnitude of the inverter output admittance, which makes the inverter sensitive to harmonic grid voltages. Such behavior cannot be studied by conventional time-domain analyses, but requires a frequency-domain model of the inverter. It is crucial to trace the origin of such behavior in order to enable large-scale utilization of renewable energies with minimal harm to the utility grid.

In order to construct a small-signal model of a converter, the proper selection of input, output and state variables is of prime importance. The input variables represent uncontrollable system inputs whereas the system outputs, i.e. the output variables, can be controlled. The state variables are conventionally capacitor voltages and inductor currents. The system inputs and outputs are converter terminal voltages and currents either at the source or load side. If the converter is fed from a stiff voltage source or the converter input current is controlled, the converter has to be analyzed as a VF converter. If the converter is fed from a stiff current source or the converter input voltage is controlled, the converter has to be analyzed as a CF converter. In order to transfer maximum power, the input-side variable of the PV inverter has to be controlled. The input-voltage control is the feasible method to track the MPP of the PVG, whereas input-current control has been shown to suffer from controller saturation and is not recommended. The output current of a PV inverter is controlled in order to enhance the current-source property of the inverter and quality of the current injected to the grid.

In such a case, the input-voltage control is implemented by a cascaded control scheme where an inner output-current loop controls the grid current and an outer input-voltage loop controls the input voltage by providing the grid-current reference. Consequently, vast majority of PV inverters have to be analyzed as CF inverters. Actually, the majority of renewables-related inverters, such as wind power inverters, employ the same cascaded control structure.

The PVG is internally a current source with limited output voltage and power due to the behavior of the semiconductor junction. The PVG acts like a current source at voltages lower than the MPP voltage (CCR) and has the properties of a voltage source at voltages higher than the MPP voltage (CVR). Consequently, the open-loop dynamics of the VSI in PV applications resemble the dynamics of a CF VSI in the CCR and has the dynamic properties of a VF VSI in the CVR. However, the VF model cannot be used because it does not suffice for the input-voltage-controlled converter. Also, the VF VSI shows first-order dynamics, because the voltage source feeding the inverter dynamically short circuits the input capacitor, whereas the CF VSI has an operating-point-dependent resonance and second order dynamics as well as a RHP zero in the output-current-control dynamics. Therefore, the use of the VF model can lead to false conclusions regarding the current-loop stability or in the grid-interaction studies. The method to include the non-linear behavior of the PVG to the inverter dynamics was presented, and the dynamic model consisting of the CF inverter model and the PVG impedance was proven to be accurate by experimental measurements using an inverter prototype fed by a real PVG.

The dynamic properties of a PVG are determined by its dynamic resistance and capacitance. This thesis also provided the validation of a real PVG and a commercial solar array simulator in terms of dynamic resistance and capacitance. The behavior of the PVG dynamic resistance also supports the dual nature of the PVG: the dynamic resistance is high in the CCR and low in the CVR, whereas the internal impedance of an ideal current source is infinite and the internal impedance of an ideal voltage source is zero. The validated solar array simulator was noticed to reproduce the dynamic resistance properly but the dynamic capacitance was noticed to be considerably larger than the capacitance of a real PVG. This can affect the behavior of the converter if its input capacitor is small. The output impedance of the PVG shows passive-circuit-like behavior, i.e. the phase of its output impedance lies between $\pm 90°$. The solar array simulator has to follow the same behavior in order to justify its usage as a substitute for the real PVG, which was the case with the tested simulator proving its feasibility as a source in the experimental measurements.

The VSI was shown to incorporate an operating-point dependent low-frequency zero in the output-current-control dynamics, whose location on the complex plane is dependent on the dynamic and static resistances of its input source. In the CCR, the zero lies in the

RHP and in the CVR the zero is located in the LHP. The RHP zero, in practice, limits the output-current-control bandwidth to the frequency of the zero. However, such low-bandwidth output-current control has no practical usage, and therefore the current loop is designed in the CVR, where the aforementioned zero lies in the LHP allowing stable high-bandwidth loop. Consequently, the inverter becomes unstable when the operating point reaches the MPP or enters the CCR under an output-current control. Therefore, the input-voltage loop is needed for enabling stable operation in all the regions of the PVG and not just to track the MPP.

It was shown that the operating-point dependent zero in the output-current-control dynamics transforms into a pole in the input-voltage-control dynamics in case of the cascaded control scheme. Consequently, the single-stage VSI in PV applications has a RHP pole in the CCR. In case of a RHP pole in the control loop, the loop bandwidth, in practice, has to be higher than the RHP pole frequency for stable operation with reasonable performance. The frequency of the pole was shown to be inversely proportional to the VSI input capacitance. This observation was used to derive a design rule for the minimum input capacitance for the single-stage VSI in PV application based on the stability of the input-voltage-control loop. The input-voltage control bandwidth of a single-phase inverter is, on the other hand, limited by the inherent power fluctuation of the single-phase grid at twice the grid freqency causing the input-voltage ripple at the named frequency. Typically, the maximum input-voltage-control bandwidth is limited to few tens of Hertz in order to prevent the ripple voltage passing through the input-voltage controller and polluting the grid current reference with the second harmonic component. Therefore, the allowed input-voltage-control bandwidth has a certain window between the RHP pole and the ripple frequency. If the control bandwidth cannot be increased due to the violation of the maximum control bandwidth, the input capacitance has to be increased according to the provided design rule. Typically, the input capacitor is designed based on e.g. the magnitude of the input-voltage ripple, which is a subjective quantity and does not necessarily guarantee inverter stability as the new design rule does. The feasibility of the design rule was proven experimentally, and its violation was shown to cause subharmonic oscillation at the inverter input voltage and output current.

This thesis has provided the means and formulation for the frequency-domain modeling of single-phase PV inverters. The non-linear behavior of the PVG was taken into account by the operating-point dependent dynamic resistance and its effect on the inverter dynamics was presented. The methods presented in this thesis can be used as guidelines by the researchers as well as practicing engineers in designing robust and well-behaving PV systems.

5.2 Future research topics

The development of the MPP-tracking algorithms was considered to be out of the scope of this thesis. The improvement of the existing algorithms or even invention of new ones is an important research topic in PV systems, especially the development of algorithms capable of locating the global MPP in partially shaded conditions. However, the MPP-tracking algorithms typically process both the input current and voltage, which introduces both input-voltage feedback and input-current feedforward terms to the dynamics of the PV system, which might bring up new important observations on the properties of the system. In some cases the tracking algorithms process output voltage and current, which will introduce e.g. output-voltage feedforward to the system. The output-voltage feedforward was shown to be harmful in the case of grid synchronization. The properties of the MPP-tracking algorithms would be expected to have an effect at the low frequencies due to their relatively slow operating speed. This kind of aspect of MPP-tracking has not been studied.

The multiplier-based grid synchronization was shown to produce negative-incremental resistor-like behavior at the inverter output impedance, which is one of the origins of the grid-interaction problems. However, a multitude of different grid-synchronization methods have been presented in the technical literature that are typically compared only by their ability to track the grid angle as accurately as possible or their step responses to e.g. frequency jumps in the grid. The various synchronization methods have never been compared in terms of their effect on the inverter output impedance, although all of the synchronization methods process the grid voltage, and therefore introduce output-voltage feedforward which will have some effect on the output impedance of the inverter. Such comparison could reveal which of the synchronization methods are best regarding the minimization or even elimination of the negative-output-impedance behavior. In addition, the emerging control methods such as the grid-voltage-supporting functions or resonant current controllers and their possible contribution to the grid interactions should be studied in order to enable large-scale utilization of the renewables.

The photovoltaic inverters also present various practical design issues to be solved, such as the elimination of the common-mode current, problems regarding the use of the new high-frequency-capable switching components and efficiency improvement as well as minimization of electromagnetic interference issues not only at the grid side but also at the PVG side, where the high switching frequency and long cables can introduce interference problems.

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A NOMINAL AND SOURCE-AFFECTED H-PARAMETERS OF VSI-TYPE CONVERTER

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% This m-file calculates the nominal and source-affected open-loop           %
% transfer functions of a VSI-type converter in photovoltaic application.   %
%                                                                            %
% Lari Nousiainen                                                            %
% Tampere University of Technology                                           %
% Department of Electrical Energy Engineering                                %
% 2012                                                                       %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Converter parameters
C     = 2200e-6;
L     = 220e-6;
r_C   = 50e-3;
r_L   = 100e-3;
r_ds1 = 15e-3;
r_ds2 = 15e-3;
fs    = 100e3;
Rs1   = 0.1; % Current-sensing resistor
Rs2   = 0.1; % Current-sensing resistor
s = tf('s');

% Operating point parameters

% Select operating point
op = 0; % 0 = CCR, 1 = MPP, 2 = CVR
% CCR
    if op == 0
        Iin  = 1.01;
        Uin  = 12.2;
        Uo   = 8.0;
        r_pv = 360;
    end

% MPP
    if op == 1
        Iin  = 0.95;
```

```
        Uin  = 15.6;
        Uo   = 8.0;
        r_pv = 16.4;
    end

% CVR
    if op == 2
        Iin  = 0.71;
        Uin  = 17.4;
        Uo   = 8.0;
        r_pv = 4.0;
    end

% Steady-state solution
    duty = [Uin+r_C*Iin , -((r_C+r_ds1-r_ds2+Rs1-Rs2)*Iin+Uo) ,...
            -(r_L+r_ds2+Rs2)*Iin ];
    R = roots(duty);
    D = R(1);          % Duty ratio
    D1 = 1-D;          % Complementary duty ratio
    Uc = Uin;
    IL = Iin/D;
    Io = Iin/D;

% State matrices
    R1 = r_L + D*(r_C + r_ds1 + Rs1) + D1*(r_ds2 + Rs2);
    U1 = Uin + r_C*Iin - (r_C + r_ds1 - r_ds2 + Rs1 - Rs2)*Iin/D;
    Am = [-R1/L, D/L
          -D/C,    0];
    Bm = [D*r_C/L, -1/L,      U1/L
             1/C,    0, -Iin/D/C];
    Cm = [-D*r_C, 1
              1, 0];
    Dm = [r_C, 0, -r_C*Iin/D
          0, 0,          0];
    Im = eye(2);

% H-parameters
    Hpar = Cm * inv(s*Im - Am) * Bm + Dm;
    Hpar = minreal(Hpar);

    Zin =  Hpar(1,1);
    Toi =  Hpar(1,2);
    Gci =  Hpar(1,3);
    Gio =  Hpar(2,1);
    Yo  = -Hpar(2,2);
    Gco =  Hpar(2,3);

% Source-affected H-parameters
```

```
Ys = 1/r_pv;

Zin_oco = Zin + Toi*Gio/Yo;
Zin_inf = Zin - Gio*Gci/Gco;

Zin_SA = Zin/(1 + Ys*Zin);
Toi_SA = Toi/(1 + Ys*Zin);
Gci_SA = Gci/(1 + Ys*Zin);

Gio_SA = Gio/(1 + Ys*Zin);
Yo_SA = (1 + Ys*Zin_oco)/(1 + Ys*Zin)*Yo;
Gco_SA = (1 + Ys*Zin_inf)/(1 + Ys*Zin)*Gco;
```

B NOMINAL AND SOURCE-AFFECTED H-PARAMETERS OF CFSQBB CONVERTER

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% This m-file calculates the nominal and source-affected open-loop      %
% transfer functions of a CFSQBB converter in photovoltaic application. %
%                                                                       %
% Lari Nousiainen                                                       %
% Tampere University of Technology                                      %
% Department of Electrical Energy Engineering                           %
% 2012                                                                  %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Converter parameters
Uim = 370;
Uo = 230;
r_C1 = 0.3;
r_C3 = 0.1;
r_C2 = 0.1;
r_L1 = 0.08;
r_L2 = 0.3;
r_L3 = 0.3;

C1 = 20e-6;
C3 = 660e-6;
C2 = 20e-6;

L1 = 220e-6;
L2 = 1e-3;
L3 = 1e-3;

fs = 150e3;
Ts = 1/fs;

% Operating point parameters

% Select operating point
op = 0; % 0 = CCR, 1 = MPP, 2 = CVR

% CCR
```

```
    if op == 0
        Iin = 7.84;
        Uin = 15;
        r_pv = 56;
    end

% MPP
    if op == 1
        Iin = 7.33;
        Uin = 25.9;
        r_pv = 3.5;
    end

% CVR
    if op == 2
        Iin = 5.7;
        Uin = 29;
        r_pv = 0.8;
    end

% Nominal open-loop transfer functions
a = Iin*(r_C1 + r_C3 - r_L2);
b = (Uim - Iin*r_C2 + Iin*r_L2);
c = Iin*r_C2;
d = Iin*r_L1 - Uin;

D1_roots = roots([a b c d]);
D1 = D1_roots(3);

a = Uim;
b = -D1^2*Iin*(r_C1 + r_C3) - Uo;
c = -D1^2*Iin*r_L3;

D2p_roots = roots([a b c]);
D2p = D2p_roots(1);
D2 = 1 - D2p;

I_L1 = Iin;
I_L2 = D1*Iin;
I_L3 = D1^2*Iin/(1-D2);

U_C1 = Uin;
U_C3 = Uim - Uin;
U_C2 = D1*Uim + D1*Iin*r_L2 + D1^2*Iin*(r_C1 + r_C3 - r_L2);

% Dynamic Model

s = tf('s');
```

```
% Matrices

A11 = 0;
A12 = 0;
A13 = 0;
A14 = -1/C1;
A15 = D1/C1;
A16 = -D2p/C1;

A21 = 0;
A22 = 0;
A23 = 0;
A24 = 0;
A25 = D1/C3;
A26 = -D2p/C3;

A31 = 0;
A32 = 0;
A33 = 0;
A34 = D1/C2;
A35 = -1/C2;
A36 = 0;

A41 = 1/L1;
A42 = 0;
A43 = -D1/L1;
A44 = (-r_C1 - r_L1 - D1*r_C2)/L1; %% -R1/L1
A45 = D1*(r_C1 + r_C2)/L1; %% R2/L1
A46 = -r_C1*D2p/L1;

A51 = -D1/L2;
A52 = -D1/L2;
A53 = 1/L2;
A54 = D1*(r_C1 + r_C2)/L2; %% R2/L2
A55 = (-r_C2 - r_L2 - D1*(r_C1 + r_C3 - r_L2))/L2; %% -R3/L2
A56 = 0;

A61 = D2p/L3;
A62 = D2p/L3;
A63 = 0;
A64 = -D2p*r_C1/L3;
A65 = 0;
A66 = (-D2p*(r_C1 + r_C3) - r_L3)/L3; %% -R4/L3

B11 = 1/C1;
B12 = 0;
B13 = I_L2/C1;
```

```
B14 = I_L3/C1;

B21 = 0;
B22 = 0;
B23 = I_L2/C3;
B24 = I_L3/C3;

B31 = 0;
B32 = 0;
B33 = I_L1/C2;
B34 = 0;

B41 = r_C1/L1;
B42 = 0;
B43 = (-U_C2 + I_L2*(r_C1 + r_C2) - I_L1*r_C2)/L1; %% -U1/L1
B44 = I_L3*r_C1/L1;

B51 = -D1*r_C1/L2;
B52 = 0;
B53 = (-Uim + I_L2*(r_L2 - r_C1 - r_C3) + I_L1*r_C2)/L2; %% -U2/L2
B54 = 0;

B61 = D2p*r_C1/L3;
B62 = -1/L3;
B63 = 0;
B64 = (-Uim + I_L3*(r_C1 + r_C3))/L3; %% -U3/L3

C11 = 1;
C12 = 1;
C13 = 0;
C14 = -r_C1;
C15 = D1*(r_C1 + r_C3);
C16 = -D2p*(r_C1 + r_C3);

C21 = 1;
C22 = 0;
C23 = 0;
C24 = -r_C1;
C25 = D1*r_C1;
C26 = -D2p*r_C1;

C31 = 0;
C32 = 0;
C33 = 0;
C34 = 0;
C35 = 0;
C36 = 1;
```

```
D11 = r_C1;
D12 = 0;
D13 = I_L2*(r_C1 + r_C3);
D14 = I_L3*(r_C1 + r_C3);

D21 = r_C1;
D22 = 0;
D23 = I_L2*r_C1;
D24 = I_L3*r_C1;

D31 = 0;
D32 = 0;
D33 = 0;
D34 = 0;

Am = [A11 A12 A13 A14 A15 A16
      A21 A22 A23 A24 A25 A26
      A31 A32 A33 A34 A35 A36
      A41 A42 A43 A44 A45 A46
      A51 A52 A53 A54 A55 A56
      A61 A62 A63 A64 A65 A66];

Bm = [B11 B12 B13 B14
      B21 B22 B23 B24
      B31 B32 B33 B34
      B41 B42 B43 B44
      B51 B52 B53 B54
      B61 B62 B63 B64];

Cm = [C11 C12 C13 C14 C15 C16
      C21 C22 C23 C24 C25 C26
      C31 C32 C33 C34 C35 C36];

Dm = [D11 D12 D13 D14
      D21 D22 D23 D24
      D31 D32 D33 D34];

Im = eye(6);

H = (s*Im - Am)\Bm;
H = balred(H,6);
H = Cm*H + Dm;
H = balred(H,6);

% Open loop intermediate dynamics
Zim = H(1,1);
Toim = H(1,2);
Gcim1 = H(1,3);
```

```
Gcim2 = H(1,4);

% Open loop input dynamics
Zin = H(2,1);
Toi = H(2,2);
Gci1 = H(2,3);
Gci2 = H(2,4);

% Open loop output dynamics
Gio = H(3,1);
Yo = -H(3,2);
Gco1 = H(3,3);
Gco2 = H(3,4);

% Source-affected transfer functions
    Ys = 1/r_pv;

    Zim_SA = minreal(Zim/(1 + Ys*Zin));
    Toim_SA = (1 + Ys*(Zin - Toi*Zim/Toim))/(1 + Ys*Zin)*Toim;
    Gcim1_SA = (1 + Ys*(Zin - Gci1*Zim/Gcim1))/(1 + Ys*Zin)*Gcim1;
    Gcim2_SA = (1 + Ys*(Zin - Gci2*Zim/Gcim2))/(1 + Ys*Zin)*Gcim2;

    Zin_SA = Zin/(1 + Ys*Zin);
    Toi_SA = Toi/(1 + Ys*Zin);
    Gci1_SA = Gci1/(1 + Ys*Zin);
    Gci2_SA = Gci2/(1 + Ys*Zin);

    Gio_SA = Gio/(1 + Ys*Zin);
    Yo_SA = (1 + Ys*(Zin + Toi*Gio/Yo))/(1 + Ys*Zin)*Yo;
    Gco1_SA = (1 + Ys*(Zin - Gci1*Gio/Gco1))/(1 + Ys*Zin)*Gco1;
    Gco2_SA = (1 + Ys*(minreal(Zin - Gci2*Gio/Gco2, 1e-2)))/...
              (1 + Ys*Zin)*Gco2;
```

C CLOSED-LOOP TRANSFER FUNCTIONS OF VSI-TYPE PV INVERTER

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% This m-file calculates the source-affected closed-loop                       %
% transfer functions of a VSI in photovoltaic application.                     %
%                                                                              %
% It is assumed that the m-file calculating the source-affected transfer      %
% functions has been run.                                                      %
%                                                                              %
% Lari Nousiainen                                                              %
% Tampere University of Technology                                             %
% Department of Electrical Energy Engineering                                  %
% 2012                                                                         %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Sensing parameters

    Req_in  = 1/(s/(2*pi*fs/2) + 1);
    Req_out = 1/(s/(2*pi*fs/2) + 1);
    Gse_in  = 1/(s/(2*pi*fs/2) + 1);
    Gse_out = 1/Uo*1/(s/(2*pi*fs/2) + 1);

% Current controller

    k_i  = 0.4;
    wp_i = 2*pi*50e3;
    wz_i = 2*pi*0.5e3;

    Gcc = k_i*(s + wz_i)/(s^2/wp_i + s);

% Voltage controller

    k_u  = 0.4;
    wp_u = 2*pi*75;
    wz_u = 2*pi*4;

    Gvc = k_u*(s + wz_u)/(s^2/wp_u + s);

% Closed loop
```

```
    [pn pd] = pade(1/100e3,2);
    Gdelay  = tf(pn,pd);
    Ga = Gdelay;

    Lout    = minreal(Req_out*Ga*Gcc*Gco);  % Current loop
    Uref_io = Req_out*Io/(Gse_out*Uo);

    Yff = 1/Req_out*Gse_out*Uref_io;

% Output dynamics with current loop
    Gio_out = minreal(Gio/(1 + Lout));
    Yo_out  = minreal(Yo/(1 + Lout) - Lout/(1 + Lout)*Yff);
    Gco_out = minreal(1/Req_out*Lout/(1 + Lout));

% Input dynamics with current loop
    Zin_inf = minreal(Zin - Gio*Gci/Gco);
    Toi_inf = minreal(Toi + Yo*Gci/Gco);

    Zin_out = minreal(Zin/(1 + Lout) + Lout/(1 + Lout)*Zin_inf);
    Toi_out = minreal(Toi/(1 + Lout) + Lout/(1 + Lout)*(Toi_inf...
              + Gci/Gco*Yff));
    Gci_out = minreal(1/Req_out*Lout/(1 + Lout)*Gci/Gco*Gse_out*Uo);

    Lin = minreal(Gse_in*Gvc*Gci_out); % Voltage loop

% Closed loop input dynamics
    Zin_c = Zin_out/(1 - Lin);
    Toi_c = Toi_out/(1 - Lin);
    Gci_c = 1/Gse_in*Lin/(1 - Lin);

% Closed loop output dynamics
    Gio_out_inf = minreal(Gio_out - Zin_out*Gco_out/Gci_out);
    Yo_out_inf  = minreal(Yo_out + Toi_out*Gco_out/Gci_out);

    Gio_c = Gio_out/(1 - Lin) - Lin/(1 - Lin)*Gio_out_inf;
    Yo_c  = Yo_out/(1 - Lin) - Lin/(1 - Lin)*Yo_out_inf;
    Gco_c = -1/Gse_in*Lin/(1 - Lin)*Gco/Gci;
```

D CONTROL-RELATED TRANSFER FUNCTIONS OF CFSQBB PV INVERTER

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% This m-file calculates the source-affected closed-loop                 %
% transfer functions of a CFSQBB in photovoltaic application.            %
%                                                                         %
% It is assumed that the m-file calculating the source-affected transfer %
% functions has been run.                                                 %
%                                                                         %
% Lari Nousiainen                                                         %
% Tampere University of Technology                                        %
% Department of Electrical Energy Engineering                             %
% 2012                                                                    %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Measurements
    Gse_in  = 1/(s/(2*pi*fs/2) + 1);
    Gse_im  = 1/(s/(2*pi*fs/2) + 1);
    Gse_out = 1/Uo*1/(s/(2*pi*fs/2) + 1);
    Req_out = 1/(s/(2*pi*fs/2) + 1);

    [pn pd] = pade(1/150e3,2);
    Gdelay  = tf(pn,pd);
    Ga = Gdelay;

% Input-voltage controller
    k = 1.2;
    Gvc_in = k/s;

    Lin = minreal(Gse_in*Gvc_in*Ga*Gci1_SA, 1e-1);

    Gco2_in_SA  = minreal(Gco2_SA,1e-1) - minreal(Lin/(1 + Lin),...
                  2.6e-1)*minreal(Gco1_SA*Gci2_SA/Gci1_SA,2e-1);
    Gcim2_in_SA = minreal(Gcim2_SA,1e-2) - minreal(Lin/(1 + Lin),...
                  2.6e-1)*minreal(Gcim1_SA*Gci2_SA/Gci1_SA,1e-2);

% Output-current controller
    k_o  = 0.05;
    wp_o = 2*pi*50e3;
```

```
    wz_o = 2*pi*1e3;
    Gcc  = k_o*(s+wz_o)/(s^2/wp_o+s);

    Lout = minreal(Gcc*Ga*Gco2_in_SA*Req_out);

    Gcim2_in_out_SA = -minreal(Lout/(1 - Lout),4e-1)*...
                       minreal(Gcim2_in_SA,1e-2)/minreal(Gco2_in_SA,...
                       1e-2)*minreal(1/Req_out*Gse_out*Uo);

% Intermediate-voltage controller
    k_im  = 0.1;
    wp_im = 2*pi*50;
    wz_im = 2*pi*5;
    Gvc_im = k_im*(s+wz_im)/(s^2/wp_im+s);

    Lim = Gvc_im*Gcim2_in_out_SA*Gse_im;
```

E PHOTOGRAPHS OF PROTOTYPES AND MEASUREMENT SETUP

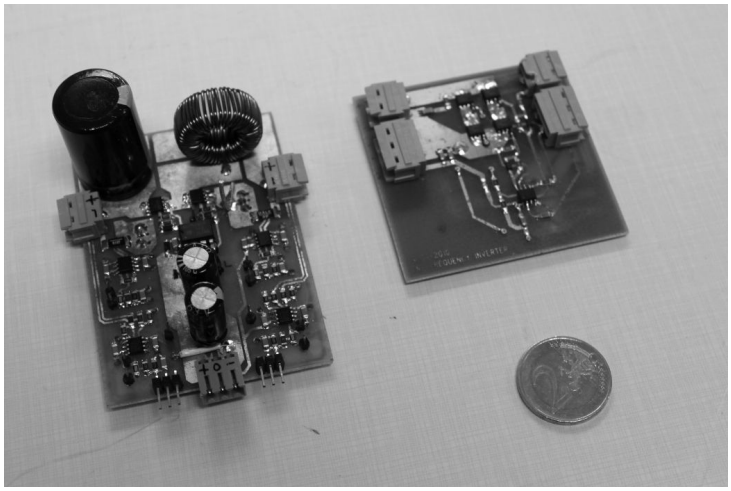

Fig. E.1: VSI-type converter and unfolder.

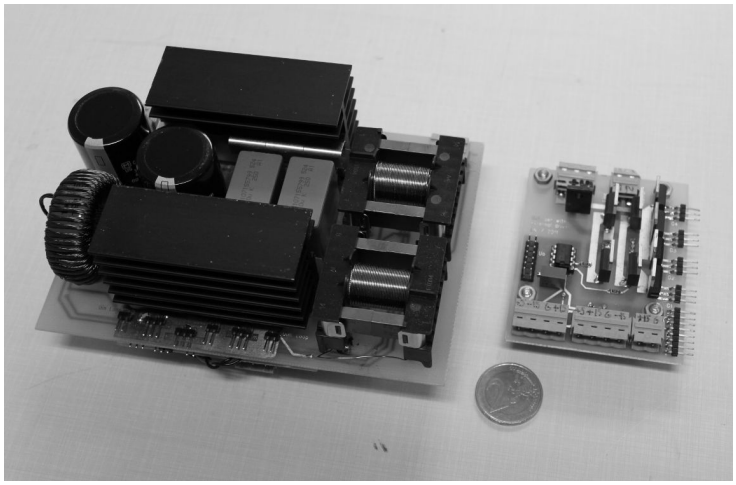

Fig. E.2: CFSQBB converter and unfolder.

Fig. E.3: Laboratory setup.

Fig. E.4: Experimental PVG and light unit.

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