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Additive and Digital Fabrication of 3D Interconnects in MEMS Packaging Using Printing Technologies

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Additive and Digital Fabrication of 3D Interconnects in MEMS Packaging Using Printing Technologies

Thesis for the degree of Doctor of Science in Technology to be presented with due permission for public examination and criticism in Rakennustalo Building, Auditorium RG202, at Tampere University of Technology, on the 15th of June 2018, at 12 noon.

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Abstract

With the introduction of electrically functional inks and continuous development of printing equipment, the application of printed electronics in the fabrication of electronic circuits, structures and devices has been steadily growing over recent years. Among printed electronic methods, digital printing has the potential to be integrated within silicon-based microelectronics such as microelectromechanical devices (MEMS). Currently, MEMS manufacturing and packaging involves subtractive processes like lithography which are time consuming and need extensive processing conditions and expensive facilities.

This thesis investigates the feasibility of using printing technologies for the selected parts of the MEMS packaging. Additive, maskless and non-contact printing technologies are digitally controlled by computer and have the potential to reduce turnaround time compared with lithographic processes. These methods could be used for the substrate with any morphology and composition; and also enable the deposition of functional inks with high level of precision on designated places defined by the graphics or codes prepared by the computer software. In summary, printing technologies provide the possibility to reduce harmful waste, consumption of the material and chemicals, process steps, and process time compared to subtractive processes.

The focus of this research has been on the fabrication of the 3D interconnects in parts of the MEMS packaging. The fabrication methods used in this work are piezo drop on demand (DOD) inkjet printing, super-fine inkjet technology (SIJ) and aerosol jet printing (AJP). Also, a combination of metal nanoparticle and dielectric inks have been used for the experiments reported in this thesis. The reported results show promising potential for additive methods to be used in electronics manufacturing in coming years with more developments and refinements in inkjettable functional materials and printing devices. In this thesis inkjet printing is utilized to fabricate 3D interconnects by the partial metallization of through silicon vias (TSVs). The via metallization could result in low resistance vias suitable for some MEMS applications. Complete filling of high density vias with diameters of less than 30 µm using super-fine inkjet technology is also demonstrated. As well, aerosol jet printing is successfully used to make a conductive bridge with low resistance between the device layer and handle wafer in silicon on insulator (SOI) MEMS. In addition, inkjet printing technologies are used to fill the TSVs to planarize wafer surface which enables placement of solder balls on top of the TSVs and increasing the I/O density of 3D TSV interposers by four times without using the next generation of TSV nodes. Moreover, successful fabrication of silver micropillars/bumps with inkjet printing is demonstrated for use in flip-chip fabrication methods instead of using stud bumps fabricated by wire bonding. The results indicate that the bare dies with the printed bumps can increase the contact reliability of flip-chip bonded samples.

Preface

This work was carried out at Printable Electronics Research Group, Laboratory of Electronics and Communications Engineering, Tampere University of Technology (TUT), Tampere, Finland, between 2013-2017.

The thesis was financially supported by Prominent (EU and Tekes) and Naked Approach projects and also The Tuula and Yrjö Neuvo Fundation. The financial support is gratefully acknowledged.

I wish to express my gratitude to my supervisor Prof. Matti Mäntysalo for his trust, guidance and support throughout my whole research and thesis work in the Printed Electronics Research Group. I also would like to thank my co-authors M.Sc. J. Liljeholm (KTH and Silex Microsystems), B.Sc. T. Lammi (TUT), Dr. G. Mårtenson (Mycronic), Dr. T. Ebefors (Silex Microsystems), Prof. F. Niklaus (KTH), M.Sc. M-M. Laurila (TUT), Dr. T. Kraft (TUT), Dr. A. Torkkeli (Murata Electronics); and of course all the current and former colleagues in PE research group especially M.Sc. Mika-Matti Laurila whose help, expertise and attitude was always a big and valuable help during this research work.

I would like to take this opportunity and thank all my friends in Finland for their true friendship, encouragement and support during the last seven years especially Zahra, Behnam, Kaveh, Mehdi, Milad, Mehrnaz, Nazanin, Mitra, Aida and Paula. I will never forget the great and unforgettable time that I spent with you guys. Love you all!

Most of all, I wish to express my deepest gratitude and love to my mother and brother back home especially my mother for her unconditional love and constant support through my university career and life in general.

This thesis is dedicated to the memory of my beloved father Mehdi Khorramdel (1950-2010).

Tampere, November 2017

Behnam Khorramdel

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List of Symbols and Abbreviations

3D	Three-Dimensional
ACA	Anisotropically Conductive Adhesive
AJP	Aerosol Jet Printing
BGA	Ball Grid Array
CAD	Computer Aided Design
CSP	Chip Scale Package
CTE	Coefficient of Thermal Expansion
CVD	Chemical Vapor Deposition
DOD	Drop on Demand
DRIE	Deep Reactive Ion Etching
E-Jet	Electrohydrodynamic Inkjet
EMC	Electromagnetic Compatibility
I/O	Input/Output
IC	Integrated Circuit
LPCVD	Low Pressure Chemical Vapor Deposition
MEMS	Micro-Electro-Mechanical Systems
PCB	Printed Circuit Board
PECVD	Plasma Enhanced Chemical Vapor Deposition
PMMA	Polymethylmethacrylate
PVD	Physical Vapor Deposition
RDL	Redistribution Layer
RFID	Radio Frequency Identification
RIE	Reactive Ion Etching
SIJ	Super Inkjet
SOI	Silicon on Insulator

TFT	Thin Film Transistor
TSV	Through Silicon Via
UBM	Under Ball Metallurgy
UV	Ultraviolet
WLP	Wafer Level Packaging

List of Publications

I. B. Khorramdel and M. Mäntysalo, “Inkjet filling of TSVs with silver nanoparticle ink,” in Proceedings of the 5th Electronics System-Integration Technology Conference (ESTC), 2014, pp. 1–5.

II. B. Khorramdel and M. Mäntysalo, “Fabrication and electrical characterization of partially metallized vias fabricated by inkjet,” J. Micromechanics Microengineering, vol. 26, no. 4, p. 45017, Apr. 2016.

III. B. Khorramdel, M. M. Laurila, and M. Mäntysalo, “Metallization of high density TSVs using super inkjet technology,” in 2015 IEEE 65th Electronic Components and Technology Conference (ECTC), 2015, pp. 41–45.

IV. B. Khorramdel, A. Torkkeli, and M. Mäntysalo, “Electrical Contacts in SOI MEMS Using Aerosol Jet Printing,” IEEE J. Electron Devices Soc., pp. 1–1, 2017.

V. B. Khorramdel, T. M. Kraft, and M. Mäntysalo, “Inkjet printed metallic micropillars for bare-die flip-chip bonding,” Flex. Print. Electron., vol. 2, no. 4, p. 45005, Oct. 2017.

VI. B. Khorramdel et al., “Inkjet printing technology for increasing the I/O density of 3D TSV interposers,” Microsystems Nanoeng., vol. 3, p. 17002, Apr. 2017.

1 Introduction

Growing consumer demands for the miniaturization of electronic devices and sensors shows the important role of MEMS technologies and devices in our everyday life (e.g. accelerometers in cars or consumer electronics, gyroscopes, microphones, pressure sensors, etc.). Accordingly, fabrication technologies and processes have developed quickly over the last few years in an effort to achieve low-cost and high volume production with minimal material consumption. The current manufacturing is depended on subtractive processing methods and lithography-based technologies which involve several process steps and a large amount of waste water. Hence, novel additive, digital and maskless fabrication methods could be integrated with the existing semiconductor and microelectronic packaging field in order to draw benefits from both technologies to simplify the fabrication process and increase its flexibility and cost efficiency.

1.1 Aim and scope of the thesis

Today, thanks to developments in printing technologies and nanoparticle/dielectric inks, there is a significant potential to use additive, maskless and digitally controlled methods instead of subtractive processes for selected parts of the MEMS manufacturing and packaging. The aim of this work is to investigate the feasibility of printing technologies (piezo inkjet printing, electrohydrodynamic jetting/super-fine inkjet (SIJ) and aerosol jet printing (AJP)) to be used for vertical interconnects in MEMS packaging. Most of the experiments and material selection in this thesis were done in close collaboration with well-known companies active in electronic manufacturing in order to be aligned with industry requirements. Demonstrated outcomes of this study show how different printing technologies can be beneficial by reducing the amount of waste (i.e. material, chemical, and water), process steps, processing time, capital investment to set up new process lines and also energy consumption compared with the existing methods.

In this thesis, partial metallization of through silicon vias (TSVs) using drop on demand inkjet printing and conductive nanometal ink is shown and the electrical performance of the metallized vias is tested. In addition, super-fine inkjet technology was shown to be promising for complete filling of high density TSVs with conductive nanometal ink where conventional inkjet cannot be used. Furthermore, aerosol jet printing was also successfully used to make ohmic contact between the device layer and handle wafer in silicon on insulator (SOI) MEMS.

Also, introducing a novel approach (placing the solder balls on top of the vias) to increase the input/output density of the 3D TSV interposers using inkjet technologies (piezo and SIJ) has been another outcome of this thesis. Finally, it was demonstrated that metal micropillars fabricated by inkjet printing could be an alternative to the stud bumps fabricated by wire bonding that are needed for assembling the chips on printed circuit boards (PCBs).

1.2 Structure of the thesis

This thesis is divided into four chapters and a conclusion outlining the work presented in six publications. Chapter 1 briefly explains the motivation of this work and then its scope, aim and main outcomes of the research work; and finally the structure of the thesis and contribution of the authors. Chapter 2 presents a background about the MEMS followed by the existing MEMS fabrication and packaging methods. In chapter 3 digital and additive fabrication methods are discussed with the three fabrication methods used in the thesis explained in more detail. Also, ink requirements, behavior of printed inks on substrates, sintering and curing are covered in this chapter. In chapter 4 the application of digital methods in MEMS packaging is presented with the focus on the selected parts of the MEMS packaging with potential to be fabricated by printing instead of conventional methods. For every selected part, materials, methods and results are well explained which are mainly reported from the publications appended to the end of this dissertation. Finally, the conclusion summarizes all the studies done for this thesis and their outcomes with a description of the developments that still need to be addressed in the future.

1.3 Authors's contribution

The current thesis includes six scientific publications that are prepared by collaboration as follows:

Publication I, *Inkjet filling of TSVs with silver nanoparticle ink*
The author was the main contributor to this paper by doing all the printing job, imaging, sample characterization and result analysis. The manuscript was written by the main author and revised and improved by the co-author.

Publication II, *Fabrication and electrical characterization of partially metallized vias fabricated by inkjet*
This paper continues the work done in **Publication I**. The author was the main contributor to this paper. The author carried out the printing, imaging, electrical characterization and result analysis. E. Tuovinen, Aalto University helped for dicing and preparation of the cross-sections, and P. Greerinck, Ghent University helped for the thinning process completed on the chips under supervision of the author. The manuscript was written by the author and revised and improved by the co-author.

Publication III, *Metallization of high density TSVs using super inkjet technology*
The author did the printing experiments, imaging, sample characterization and result analysis. M-M. Laurila had a valuable contribution for using SIJ printer for the via filling. In addition to the author, E. Tuovinen, Aalto University also helped for preparing the via cross-sections under supervision of the author. The manuscript was written by the author and revised and improved by M. Mäntysalo.

Publication IV, *Electrical contacts in SOI MEMS using aerosol jet printing*
The author did the post treatment on the printed sample, characterized cross-sections, did the whole electrical characterization and analyzed the results. M. Mäntysalo helped for the data analysis and also reviewed and improved the manuscript. J. Manni, Top Analytica helped for making the cross-sections using BIB technique under supervision of the author. L. Seronveaux, Sirris contributed for the aerosol jet printing under author's supervision. The manuscript was written by the author in collaboration with co-authors.

Publication V, *Inkjet printed metallic micropillars for bare die flip-chip bonding*
The author was the main contributor to this work by doing the printing trials, imaging, characterization, electrical measurements, result analysis and writing most of the manuscript. T. Kraft contributed by writing parts of the manuscript, data analysis, and performing the flip-chip bonding. M. Mäntysalo helped for the data analysis and also revised and improved the manuscript.

Publication VI, *Inkjet printing technology for increasing the I/O density of 3D TSV interposers*

The author managed, monitored and supervised the via filling processes and UBM printing. The author also did the imaging, characterization and result analysis. T. Lammi helped for the via filling using the piezo inkjet printing. M-M. Laurila helped to use SIJ technology to fill the vias and deposition of metal UBM layer. G. Mårtensson contributed for the final solder ball attachment and also wrote a paragraph for the manuscript. J. Liljeholm had a valuable contribution for writing the introduction of the manuscript. T. Ebefors acted as an advisor from the industry. M. Mäntysalo and F. Niklaus revised and improved the manuscript. J. Manni, Top Analytica helped for making the cross-sections and J. Kiilunen, TUT helped for doing temperature cycling tests under supervision of the author.

2 Overview of MEMS

Microelectromechanical systems (MEMS) are tiny devices in the size range of micrometers to millimeters integrating electrical and mechanical components. In 21th century the demand for producing smaller and lighter microelectronic devices has been growing all the time and this trend is ongoing to make even better products in coming years. MEMS devices are usually including microsensors, microelectronics, mechanical microstructures and microactuator units which need to be packaged in a proper manner to be protected from the outside world. MEMS process technology can be used for a wide range of MEMS-based devices such as inertial sensors (e.g. accelerometers and gyroscopes), pressure sensors, chemical sensors, optical and bio-MEMS devices or printheads which all play an important role in our everyday life.

2.1 MEMS fabrication methods

MEMS devices are typically fabricated by semiconductor fabrication and micromachining process. Therefore, this process involves masking, lithography, deep reactive ion etching (DRIE), wet etching and thin film deposition. At the end, the whole MEMS structure needs to be packaged properly in order to be protected from the outside world. However, for some sensing applications like pressure sensors, MEMS sensor need to be in contact with environment. Other than the protection, packaging can help to dissipate the generated heat by device inside and also enables the mechanical and electrical connection of packaged devices to outside environment. There are some issues in MEMS packaging to be addressed like electrical insulation, encapsulation, mounting and device interconnection [1].

Silicon because of its unique microfabrication properties is the most ideal material for MEMS. Silicon is a popular material for MEMS for several reasons [2]: (1) Ideal structural material with high Young's modulus but light as aluminum, (2) Great flexibility in design and manufacture, (3) Shows virtually no mechanical hysteresis, (4) Ideal candidate to accept coatings and thin film layers, (5) High melting point at 1400 °C, (6) Small and optimum coefficient of thermal expansion (2.5 ppm.$°C^{-1}$), (7) Can be integrated into electronics on the same substrate and is mechanically stable. Micromachining technique could be used to fabricate micron sized structures such as diaphragms, cavities, beams and suspended masses for mems-based sensors [3]. Processes like photolithography, patterning thin films and etching (wet or dry) are so common in MEMS fabrication and all are associated with silicon micromachining [3]. Therefore in the following these processes are covered briefly.

2.1.1 Photolithography and etching

Photolithography is basically used to transfer a predesigned pattern to a thin film (e.g. Cu, SiO_2, etc.) which is already formed on whole silicon substrate. In order to do this pattern transfer, at first deposited thin film needs to be coated by photoresist material using spin coating. In the next step, patterned mask is placed on top of the photoresist material. Mask plate is covered with chromium metal film to be opaque to ultraviolet (UV) light except the pattern area which needs to be transparent to UV light. After UV exposure, the exposed area on photoresist layer is either strengthened in negative photoresists or weakened in positive photoresists. Afterwards, the substrate is immersed in a chemical developer to dissolve and wash unexposed resist (negative photoresist) or exposed resist (positive photoresist). In the last step, a chemical like hydrochloric acid is used to etch away the parts of the thin film which are not covered by resist material and then finally a harsh chemical like hot sulfuric acid is used to react with just resist material but not the thin film. With this approach at the end the result could be a cavity in thin film or an excess layer of patterned thin film on top of the silicon substrate (see Figure 2.1).

In case of thin film deposition of noble metals that cannot react with chemical etching, lift-off process is used. In this technique, after the photoresist patterning, a thin film of noble metal is formed on top of the patterned photoresist by thermal evaporation. In the last step, by lift-off or acetone rinsing, the photoresist with metal film on top of that is removed so that only the thin film on top of silicon is remained.

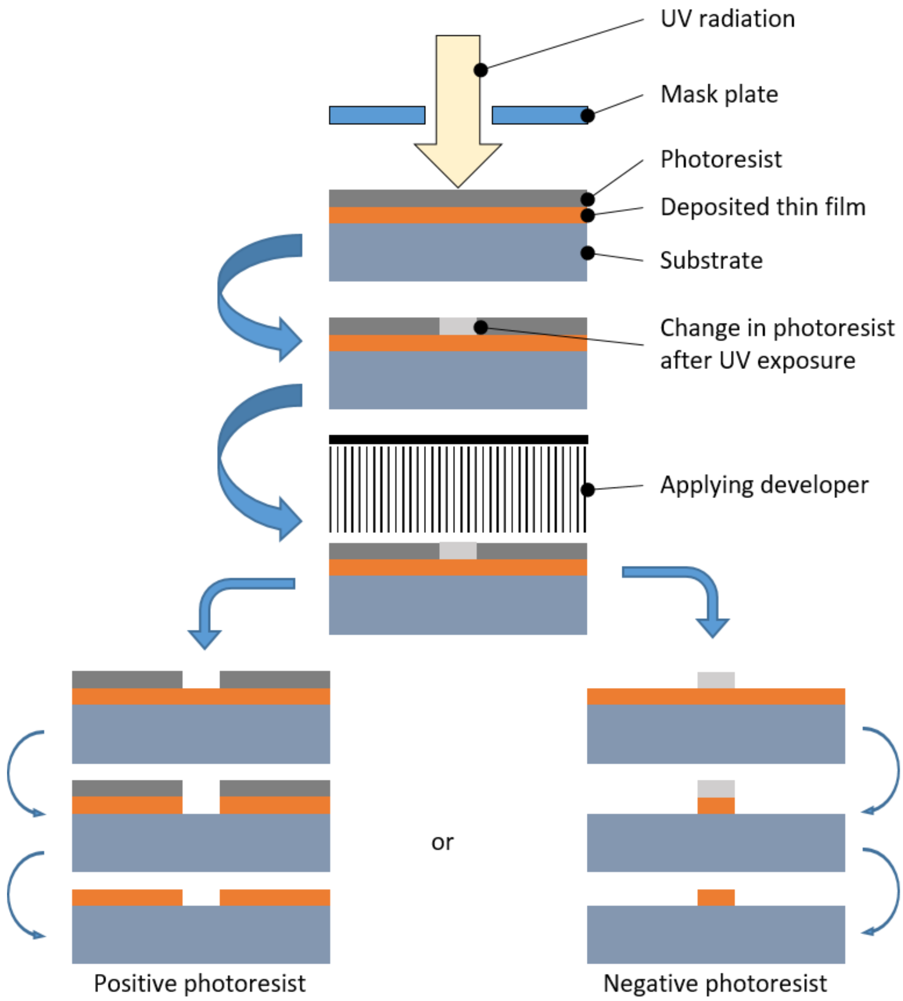
UV radiation
Mask plate
Photoresist
Deposited thin film
Substrate
Change in photoresist after UV exposure
Applying developer
or
Positive photoresist
Negative photoresist

Figure 2.1: Schematic of photolithography process for positive and negative photoresist processes.

2.1.2 Micromachining

Micromachining technique is used to remove materials by wet or dry etching to create three dimensional (3D) features [4], [5]. For instance all the TSVs used for this dissertation were fabricated by dry etching using DRIE. Two main categories of micromachining are bulk and surface micromachining. In bulk micromachining, isotropic or anisotropic wet etching is used to etch inside the material (Figure 2.2a). In surface micromachining as shown in Figure 2.2b, structural layer is formed on top of the sacrificial layer and then the sacrificial layer is removed by etching to release the structural layer.

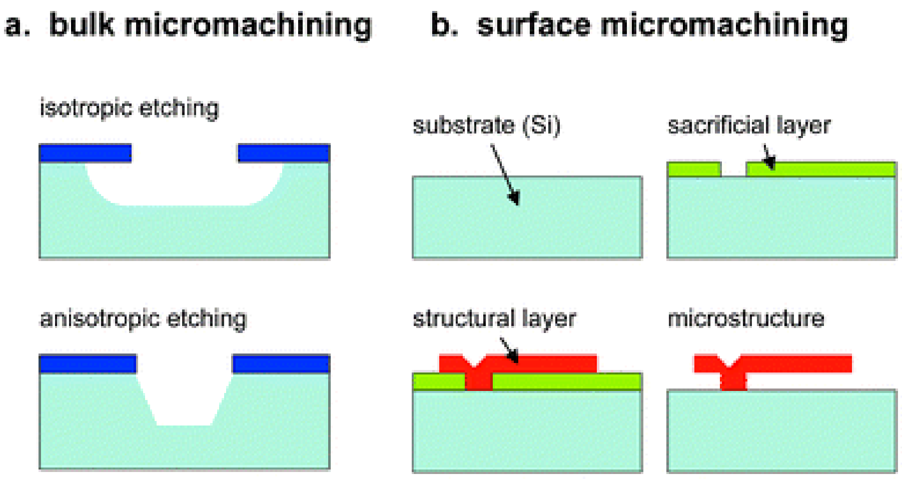

Figure 2.2: Schematic of bulk and surface micromachining for MEMS. [4] © 2003 Analyst

2.1.3 Thin film deposition techniques

Deposition of thin films in the range of few nanometers to about 100 micrometers plays a very important role in MEMS fabrication. Thin films deposited on the surface could be patterned by photolithography and etching processes described earlier. Thin films can be formed by chemical reactions like chemical vapor deposition (CVD), electroplating or thermal oxidation; or physically with no chemical reactions like physical vapor deposition (PVD). The deposition method is selected considering the target application and also advantages and limitations of the deposition methods.

In CVD, the substrate is placed inside a reactor chamber with some gases inside. The chamber is heated so that the gases react together and the produced solid material forms on top of the substrate. In MEMS fabrication, low pressure CVD (LPCVD) is more used since it provides film with very good uniformity and high quality. In addition, with LPCVD it is possible to cover both sides of many wafers at the same time. However, deposition in LPCVD takes a long time and requires a high temperature (>600 °C). On the other hand plasma enhanced CVD (PECVD) can be operated at much lower temperatures but the quality of the coverage is lower than the films formed in higher temperatures [6].

Thermal oxidation is used when we are dealing with the material that can be oxidized like silicon. For example the silicon dioxide film can be grown on top of silicon when it reacts with an atmosphere with water vapor in 1000 °C for one hour [7].

In PVD, the thin film material physically moves to the substrate and then after condensation makes a thin metal layer without any chemical reaction. Release of the material can happen by the evaporation or sputtering. In evaporation, the substrate is placed inside a chamber with the vacuum and the source metal is heated and melted until the material is released and then condensed on top of the substrate as a thin film of metal. In sputtering same as evaporation, both the source material and substrate are in a vacuum chamber but also an inert gas like argon is purged at low pressure inside the chamber. Next, the plasma gas is ignited by RF source or DC power source to ionize the gas. Later, the source material is bombarded by the accelerated ions and then atoms of the source material are released and condensed on top of the substrate. PVD process is more flexible compared with CVD and also cheaper. However, the quality of the films formed by CVD is better than the films deposited by PVD.

In electroplating, the wafer or substrate is placed inside an electrolyte solution and connected to counter electrode. The film is formed on top of the wafer by activation of a DC voltage source between the electrode and the conductive part of the substrate (seed layer). On the other hand, in electroless plating there is no need to have electrode, voltage source and connection to the substrate. The film is formed on parts of the substrate which high enough electrochemical potential can be formed with the solution. In contrast with electroplating, it is not possible to properly adjust the uniformity and thickness of the films. [8]

2.2 MEMS packaging methods

MEMS devices or micromachined elements are very fragile and sensitive and could be damaged easily during the dicing process. Therefore, delicate MEMS devices need to be packed to survive the dicing particles and slurry and also be protected against external factors that affect the operation of MEMS like e.g. humidity, contamination, heat, particles and impact. Wafer level packaging (WLP) is used because it is affordable, and also provides shortest electrical path, reduced parasitics and higher speed [9]. In WLP the whole wafer with MEMS devices is packaged first and then will be diced. Thus, it is more cost efficient than when packaging is done in the last step after the wafer dicing and device fabrication. Also, in WLP it is possible to do the testing and device interconnections while all devices are on the same wafer rather than testing many separated devices. There are two approaches for WLP: fan-in and fan-out which is newer (shown in Figure 2.3).

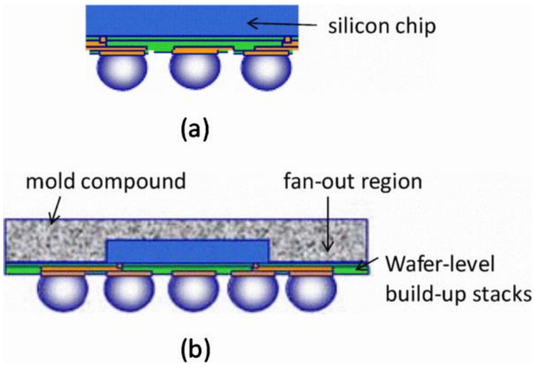
silicon chip
(a)
mold compound
fan-out region
Wafer-level
build-up stacks
(b)

Figure 2.3: (a) Fan-in and (b) Fan-out wafer level packaging. [9] © 2010 IEEE

In fan-in WLP (Figure 2.3a), dicing and singulation is done after the whole wafer with large number of MEMS devices is packaged. The size of every single package after the dicing is exactly the same as the size of the dies inside which is the reason to call it true chip scale package (CSP). It is in contrast with CSP in which the final package area is a bit larger than the chip footprint.

In fan-out WLP (Figure 2.3b), there is no need for a silicon wafer as the substrate. In simple terms, in wafer reconstitution process shown in Figure 2.4, dies from a device wafer are placed (distance between the dies is called fan-out area) on a carrier laminated by adhesive and then overmolded by an epoxy molding compound. Next, the epoxy is cured and carrier and adhesive are delaminated to create a reconstituted wafer ready for redistribution layer (RDL) and bumping processing and finally singulation [10]. Thin reconstituted wafers and fan-out capability allows for making thinner packages, increasing the number of inputs/outputs (I/Os) and heterogeneous integration.

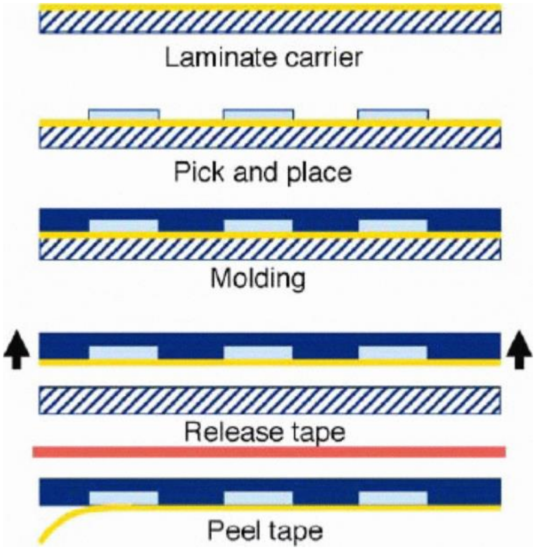
Laminate carrier
Pick and place
Molding
Release tape
Peel tape

Figure 2.4: Wafer reconstitution process. [10] © 2008 IEEE

WLP combined with three-dimensional integration or 3D integration is a packaging method which is more common for MEMS packaging [9]. In this method, a cap wafer with through silicon vias (TSVs) and cavities is bonded to the MEMS wafer so that the cavities are aligned on top of the MEMS structures (see Figure 2.5).

A functional getter material is needed to be deposited into the cavities of the cap wafer in order to absorb the residual gases and moisture trapped in the cavities. It is particularly important for the performance and lifetime of the devices with movable parts. The MEMS structure can be connected to the outside of the package by the polysilicon TSVs passing vertically through the cap wafer. The other end of the TSVs are connected to the RDL and then to the bumps with under-bump-metallurgy (UBM) pads underneath.

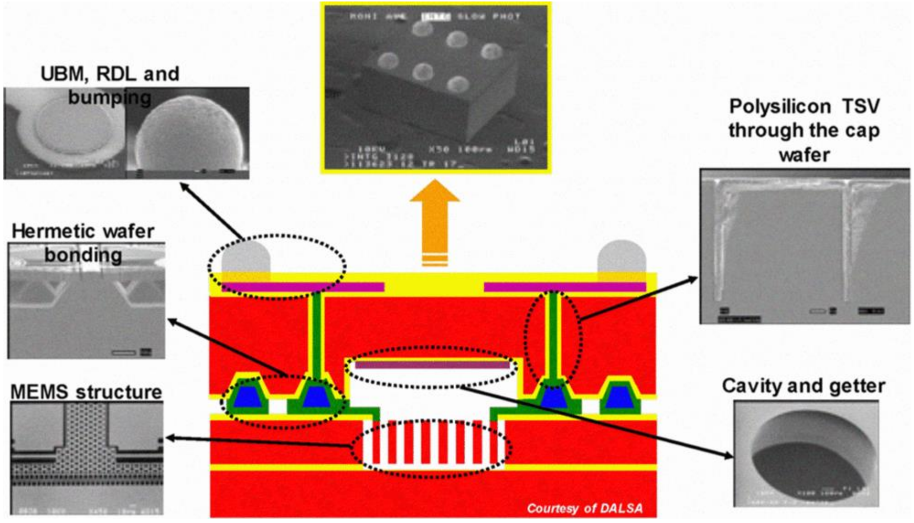
UBM, RDL and bumping
Hermetic wafer bonding
MEMS structure
Polysilicon TSV through the cap wafer
Cavity and getter
Courtesy of DALSA

Figure 2.5: WLP integration for MEMS. [9] © 2010 IEEE

3 Digital and additive fabrication methods

In this chapter, basics of three different additive and digitally controlled fabrication methods that are used in this research are shortly explained: *inkjet printing, super-fine inkjet printing and aerosol jet printing*. Thanks to nanoparticle inks and dielectric inks, the past decade has seen a growing interest in using ink-based additive methods for specific parts of the manufacturing process of electronic devices and MEMS. In these methods the print pattern is designed or coded digitally with computer and then can be contactless printed on different type of substrates (rigid, flexible, brittle, non-uniform/3D). In general, additive and digital fabrication can be much more flexible compared with conventional subtractive methods like lithography with longer manufacturing process flow as illustrated in Figure 3.1. These type of fabrication methods with fewer process steps and more flexibility, could have a good potential to reduce the cost extensively by jetting the material on demand which can decrease the waste water, usage of materials, chemicals, energy use, capital investment and processing time. [11]–[13]

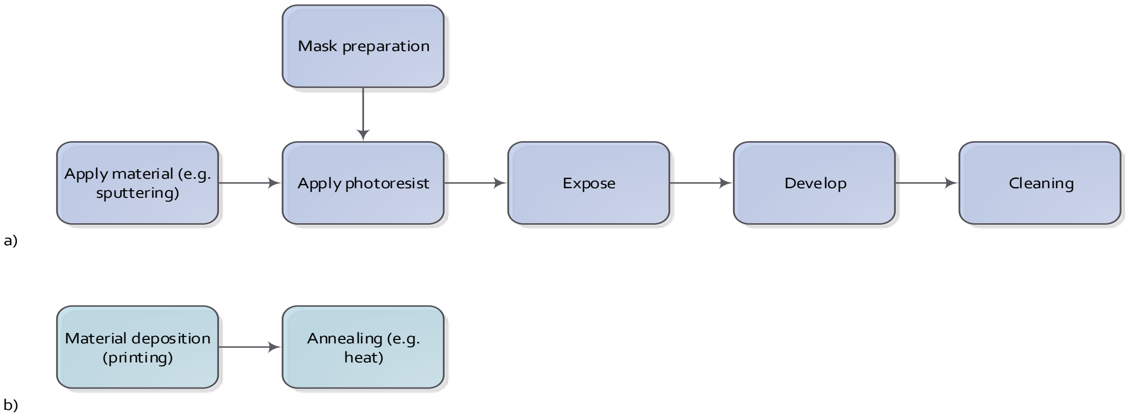
Mask preparation
Apply material (e.g. sputtering)
Apply photoresist
Expose
Develop
Cleaning
a)
Material deposition (printing)
Annealing (e.g. heat)
b)

Figure 3.1: Process flow of (a) subtractive and (b) additive fabrication.

3.1 Printing methods

In this thesis work, conventional inkjet printing (Dimatix DMP 2800), super-fine inkjet technology (SIJ-S050) and aerosol jet printing (Optomec 300 CE) were employed for microfabrication processes. Table 3-1 summarizes the comparison of these technologies based on system specifications. These printing systems are covered in more detail in below.

Table 3-1: Comparison of conventional inkjet, super-fine inkjet and aerosol jet printing.

	Dimatix DMP 2800	**SIJ printer (SIJ-S050)**	**Optomec AJ 300 CE**
Deposition principle	piezo inkjet	Electrohydrodynamic	Continuous aerosol mist
Ink viscosity range (mPa·s)	2-30 (low) Thin electrode at medium resolution	0.5-10000 (low to medium) Very thin electrode at ultrahigh resolution	0.7-1000 (low to medium) Thin electrode at high resolution
Droplet size	1 and 10 pL nominal (10 pL was used)	0.1 fl – 10 pL	$5.2\text{x}10^{-4}$ – $6.5\text{x}10^{-2}$ pL
Number of nozzles	16 nozzles (only one nozzle was used)	Single	Single
Printable area (mm^2)	210 x 315	50 x 50	300 x 300
Image transfer	Raster based	Vector from data	Vector from data
System positional accuracy (µm)	± 5	0.1	± 5
Position repeatability (µm)	± 25	± 0.2	± 2
Axis speed (mm/s)	Depends on drop spacing	10	Maximum 200

3.1.1 Inkjet printing technology

Conventional inkjet printing can be divided to continuous inkjet (CIJ) and drop on demand (DOD) categories. In continuous inkjet, a stream of droplets is ejected continuously out of the nozzle by the pressure and then passes first through the charging electrode to be charged and then deflection plates. Droplets that are needed to be printed are deflected by electric field towards the substrate and other droplets are collected by the gutter and will be used again. The recycling or wasting the ink and also poor position accuracy of printed droplets are the limitations of CIJ to be used in micro-manufacturing. Another limiting factor is the size of the droplets that is twice the nozzle diameter. However, this method is still suitable for printing the labels for the food packages or drugs [1] even on non-planar substrates [14].

In DOD method, drops are only injected for each black pixel in the pattern. The printing pattern/file is prepared by printer software or other graphic design software. In most of the DOD inkjet printers it is just possible to adjust the resolution in x direction and accordingly the resolution depends on the printing direction.

There are two main types of bubble jet or piezo heads that can be used for DOD printing. In the bubble jet, like the printers for home or office use, ink is heated to the boiling point and then a bubble made by the ink evaporation, cause the ejection of droplet. In piezoelectric actuation, voltage is applied to a piezo crystal (lead zirconium titanate). This actuation or distortion results in an acoustic wave that is needed for jetting droplets (Figure 3.2). Figure 3.3 shows the Dimatix DMP-2800 inkjet printer with the cartridge installed which is used for the experiments reported in this thesis. In the most of DOD inkjet printers like Dimatix used in this thesis, the printhead moves in horizontal swipes and the stage vertically to reach to the final geometry. There are also commercial inkjet printers (e.g. iTi XY 2.0 MDS inkjet printer) with the stationary printhead and moving substrate so that the resolution can be adjusted for both x and y directions.

Droplets should be jetted with appropriate speed and without misdirection and long tails. Different parameters can affect the jetting and size of the droplets. Firing pulse amplitude can affect the drop velocity and size of the droplets. Pulse width also affects the size of the droplets. Another parameter that affect the volume of the droplets is the size of the nozzle diameter. For instance, a printhead with nozzle diameter of 26.73 µm can produce droplets with the volume of 10 pl and a nozzle with diameter of 12.41 µm produces 1 pl droplets [15].

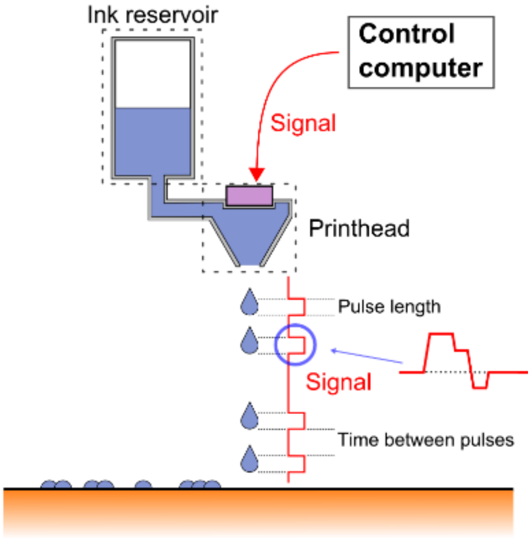
Ink reservoir
Control computer
Signal
Printhead
Pulse length
Signal
Time between pulses

Figure 3.2: Schematic of piezo DOD inkjet printing operation principle. [16]

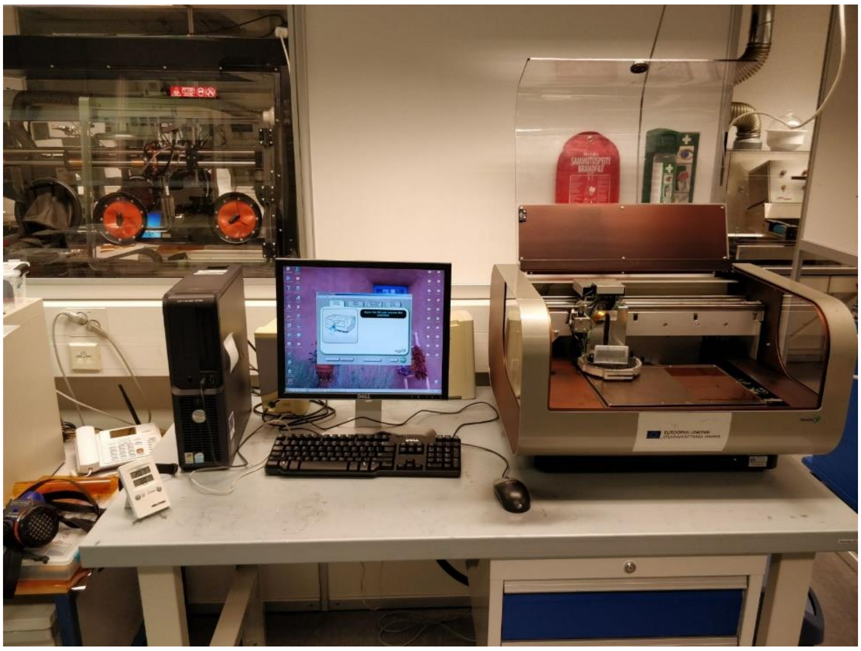

Figure 3.3: Photograph of Dimatix DMP-2800 inkjet printer used for this thesis.

3.1.2 Super-fine inkjet technology

Super-fine inkjet technology is in fact a commercial version of electrohydrodynamic inkjet (E-Jet) developed by SIJ Technology Inc. in Tsukuba Japan (see [17]). This technology is one type of inkjet technology which allows very precise jetting of sub-femtoliter droplets; which is thousand times smaller than the smallest droplets (1 pl) produced by conventional inkjet printers [18]. Therefore SIJ is the best available inkjet method for applications that very high level of miniaturization and resolution is needed (e.g. redistribution layers [19]–[21]). Printing conductive lines with the width of less than one micron and pitch of 2.5 µm is demonstrated by the printer manufacturer [22], while with conventional inkjet the minimum achievable width has been about 20 µm [19]. This technology consumes minimum possible amount of material between digital and additive fabrication methods and accordingly has minimum environmental impact.

Figure 3.4 illustrates the SIJ printer functional parts and Figure 3.5 shows the SIJ printer (SIJ-5050) which is used for the experiments represented in this thesis. The needle shape nozzle is made of glass which is filled by ink. During the printing an electrode charges the ink when there is a potential difference between the grounded stage and ink meniscus. When the electric field between the substrate and the meniscus at the nozzle tip is strong enough and goes over a specific threshold, the ink comes out of the capillary hole of the nozzle. The strength of the electric field can be affected by different parameters that can be changed by computer software like bias voltage, maximum voltage, the distance between the nozzle tip and substrate, speed of the stage and pulse frequency. [17]

In SIJ the print file is a vector based pattern which is prepared by a type of coding and defines the movements of the stage in both x and y directions while nozzle is fixed. Therefore the resolution is not depended on the printing direction. The resolution of the stage movements (0.1 µm) in x and y directions is the same [22].

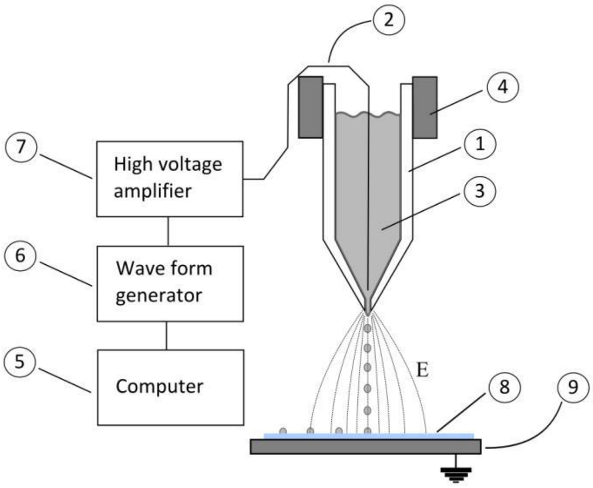

Figure 3.4: Illustration of the SIJ functional parts. 1: nozzle, 2: charging electrode, 3: functional ink, 4: magnetic nozzle holder, 8: substrate and 9: movable xy-stage. [19]

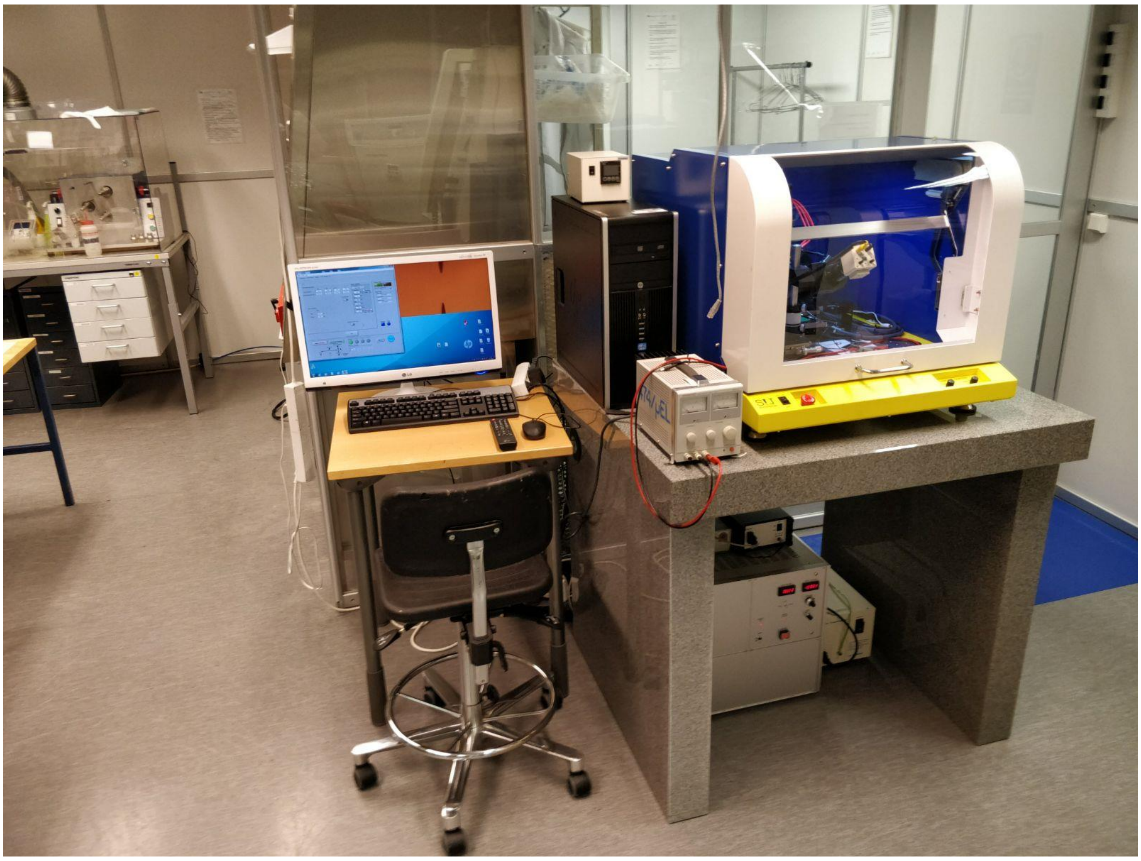

Figure 3.5: Photograph of the SIJ printer (SIJ-S050) used for this thesis.

3.1.3 Aerosol jet printing

Aerosol jet printing (AJP) is a non-contact and maskless technology that can be used to deposit different type of materials (conductive, dielectric, biomaterial, etc.) with very high precision on top of rigid or flexible substrates no matter how much they are conductive. It is in contrast with the SIJ that level of conductivity of the substrates affect the printing. AJP has some advantages and differences compared with conventional inkjet printing: (1) Materials with a wide range of viscosities up to 1000 mPa·s can be dispensed while inkjettable inks have viscosities not more than 20 mPa·s (highly viscous materials could be used for fabricating 3D features). (2) AJP allows higher resolution than inkjet printing so that minimum achievable resolution could be 10 µm width [23] or even down to 5 µm while the very good resolution for inkjet is 20 µm [24]. (3) The distance between the nozzle and the substrate in AJP can be larger and variable (1-5 mm) while this distance in inkjet printers is fixed during the printing and typically 1 mm or less. Thus, this technology is a promising technology for printing over non-flat, curved and 3D surfaces. (4) AJP is a vector based printing method driven by computer aided design (CAD) which is in contrast with inkjet printing with raster based movement of printhead. Vector based movement in AJP (similar to SIJ) enables much more freedom in printing complex geometry. It also provides same resolution in both x and y directions similar to SIJ method.

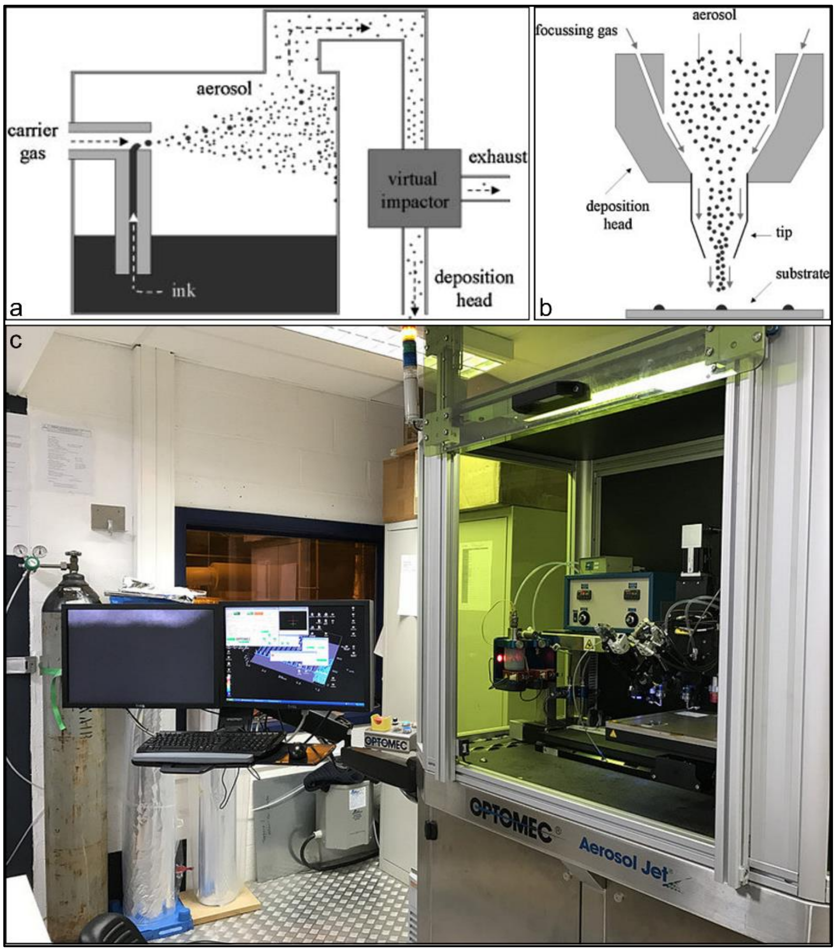
aerosol
carrier gas
exhaust
virtual impactor
ink
deposition head
a
focussing gas
aerosol
deposition head
tip
substrate
b
c
OPTOMEC
Aerosol Jet

Figure 3.6: Schematic of AJP (a) operation principle and (b) deposition head [25] © 2007 John Wiley and Sons; and (c) photograph of the aerosol jet printer 300 CE used for this thesis.

AJP working principle is quite different from conventional inkjet and SIJ (see Figure 3.6): (1) The ink is loaded to an atomizer in first place. In case of using highly viscous inks (up to 1000 mPa·s) pneumatic atomizer is used and in case of using inks with very low viscosity (>5 mPa·s) ultrasonic atomizer is used. (2) Introducing an inert gas flow (N_2) into the atomizer over the ink, starts atomize the ink and make mist of ink particles inside the atomizer. (3) Finer ink particles with size of smaller than 5 µm flow to the virtual impactor (for pneumatic atomizers) which is between the atomizer tank and the nozzle. In virtual impactor the stream of aerosol is densified by removing the extra gas. (4) In the head of the nozzle, flow of sheath gas (N_2) focuses the mist to a very narrow stream which helps to avoid nozzle clogging and ink spraying. Whenever printing should be stopped during printing a pattern, a mechanical shutter at the tip of the nozzle stops the flow of ink stream.

3.2 Materials and post-processing

3.2.1 Requirements for inks

There are different factors that should be always considered for inkjet printing technologies like ink, substrate properties and printing resolution. The most important factor is the ink or material that is used for the printing. In fact more compatible and optimized inks available for inkjet printing, means more application for this technology. Thus, still new type of nanometal and silicon nanoparticle inks need to be developed and studied.

Inks after the sintering or curing can act as a conductive, semiconductive or insulating material. In order to have good jetting results, physical properties like viscosity and surface tension and also chemical properties of the inks need to be compatible with the printheads or nozzles [26]. For the inkjet printing, viscosity of less than 20 mPa·s is typically suitable [27]. Inks with the viscosity range of 1-1000 mPa·s could be jetted with aerosol jet printer. In addition, a large variety of fluids can be dispensed or jetted with SIJ technology. Inks with the viscosity in the range of 0.5 to about 10000 mPa·s (non-heated) could be used with SIJ technology.

For the solvents (nanoparticles carrier) it is best to use the solvents that evaporate slowly so that the fast evaporation in the nozzle cannot cause dryness and clogging. In case it is not possible, then a chemical additive like glycol can be added to lower the evaporation rate of the solvent. As for the inks with very high viscosity, a diluent can be added or higher printhead temperature can be used to bring the viscosity in the optimum range. Also for the optimization of the surface tension, surfactant can be added if needed. Solvents with high surface tension cannot be jetted properly. [26]

For the inks with nanoparticles, it is needed to have nanoparticles dispersed during the whole shelf time. For that reason dispersant agents are used to cover the nanoparticles so that the particles cannot be agglomerated and settled down quickly. However, still just before the printing it is recommended to filter the ink with a filter with the size of hundred times smaller than the size of the nozzle. Other than the filtration, the ink can be degassed just before loading the printhead or nozzle to make the jetting even better.

3.2.2 Interaction of ink and substrate

After collision of the droplet to the substrate, the ink spreads on the substrate to a specific extent. Three different levels of wetting can happen after contact of droplets with smooth substrate as shown in Figure 3.7. If the contact angle (θ) of the droplet on the substrate is smaller than 90° (<< 90°) then the wetting of the substrate is good and it happens in case the surface tension of the ink is smaller than the surface energy of the substrate. In case the contact angle is larger than 90° (>> 90°), the wetting is poor and contact angle of 0° occurs in case of complete wetting [28]. To change the level of wetting, the surface tension of the ink or the surface energy of the substrate can be changed. However, since the surface tension of the inks are fixed and adjusted to be compatible with printheads, changing the surface energy of the substrates is more common and convenient. There are different types of the pre-treatments that can be done on the substrates to decrease or increase the substrate wettability depending on the need, like plasma cleaning, UV ozone cleaning, pyrolytic coating or chemical treatments [29]. Cleaning and improving the wetting can also make a better adhesion between the ink and substrate. Adhesion promoters can also be added to the inks to increase the adhesion.

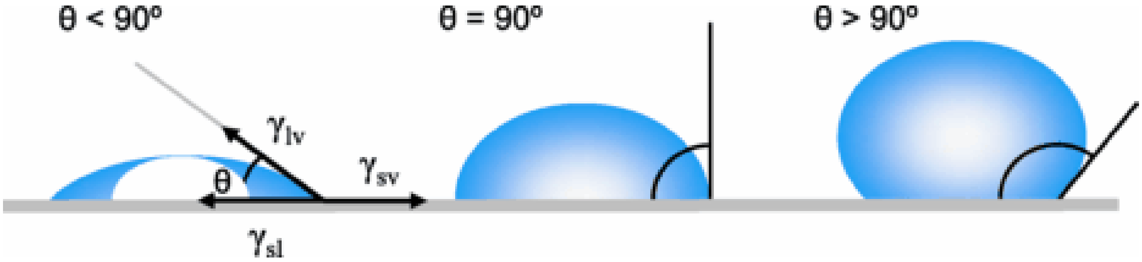

Figure 3.7: Three different levels of droplet wetting on top of the smooth substrate. Solid-vapor interfacial energy is denoted by γ_{sv}, solid-liquid by γ_{sl} and liquid-vapor by γ_{lv}. [28] © 2013 Springer.

Other than the surface treatment, increasing the substrate temperature can also decrease the wetting. Regarding the printed lines, at constant temperature there are two parameters that affect the shape of the lines: the space between the droplets or resolution, and the printing speed (see Figure 3.8). It is good to be noted that in case of having constant delay, changing the temperature has the similar effect. In other word, with more delay, droplets can be dried before next coming droplet and with constant delay, a higher temperature can dry the droplets faster.

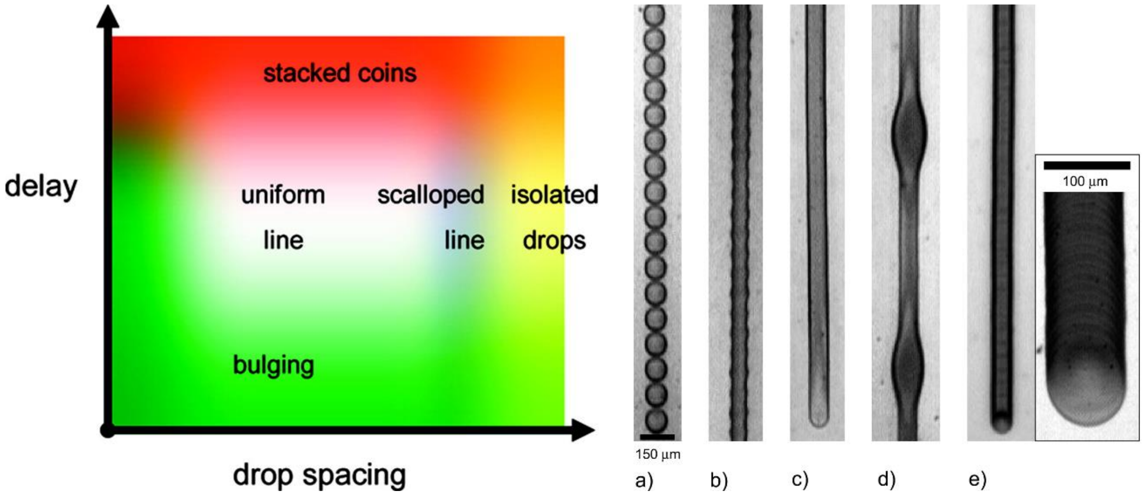

Figure 3.8: Formation of inkjet printed lines at constant temperature as a functions of drop spacing and delay. (a) Individual droplets, (b) scalloped, (c) uniform, (d) bulging, and (e) stacked coins. [30] © 2008 American Chemical Society.

As pointed out earlier, in most of the piezo DOD inkjet printers, printhead moves horizontally and printing is in parallel mode. It means that the shape and quality of the vertical and horizontal lines are different. It is because in vertical line every droplet has time to be dried before another droplet comes down. Therefore, horizontal printed line is more uniform compared with vertical line with stacked coins structure.

3.2.3 Sintering and curing of inks

In case the inks are based on the nanoparticles, nanoparticles should weld to each other and densify in order to make the printed ink conductive. Beside the organic solvents or water used in the inks, other compounds also added to cover the individual particles and make the ink dispersion as stable as possible without the agglomeration. Therefore, to make the connectivity between the particles and also for the mechanical adhesion of the ink, enough heat, depending on the ink, is needed to remove first the solvent and then dispersing agent material around the nanoparticles.

After evaporation of the solvent and all other additives, nanoparticles in neck-growth stage coalesce and then gradually larger grains and denser structure with less porosity is formed suitable for good electrical conductivity (see Figure 3.9). Three stages of sintering of gold nanoparticles is well investigated before by Ingham et al. [31]. Since nanoscale particles have a much larger atomic surface/volume ratio compared with the same material in bulk size, the melting point of the nanoparticles is much lower. Dependency of the melting point of gold nanoparticles on the particle size is studied in the seventies by Buffat and Borel [32]. Lower melting point allows for using a wider range of substrates even polymer based substrates that cannot stand very high temperatures.

In recent years, sintering of metallic nanoparticle inks with different sintering techniques (e.g. conventional heating, laser, microwave, flash sintering, infrared and plasma) has been under investigation [33]–[42]. The difference between these methods is mostly related to the time that is needed for sintering or the area on the substrate that is affected by the heat. Therefore, the biggest advantage of alternative sintering methods (e.g. plasma, microwave flash and infrared) is that temperature sensitive substrates can be used. Also in case of copper sintering, there is no need for nitrogen or other inert atmosphere to avoid oxidation in conventional thermal sintering. Soltani et al. [43] have demonstrated laser sintering of copper nanoparticles on top of silicon wafer in ambient atmosphere which can be just concentrated on the printed area and also is much faster than oven sintering. The degree of the sintering and resistivity is mostly influenced by the temperature rather than the time the particles are exposed to heat, so that with higher temperature, shorter time is needed [44].

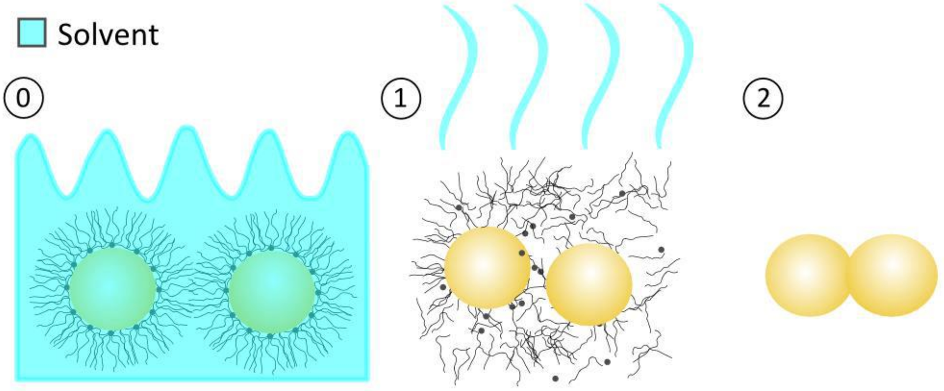

Figure 3.9: Sequence of sintering for the metal nanoparticle inks: solvent evaporation, separation of the polymer coating and coalescence of the nanoparticles. [19]

Dielectric material is used to insulate conductive parts from each other in electronics manufacturing. Most of UV curable dielectric inks are consist of monomers or oligomers, photoinitiators and additives [26]. When the printed ink after pre-baking and solvent evaporation is exposed to the UV light, monomers and oligomers are activated which result in polymer cross-linking and curing. In the formulation, photoinitiators help to promote polymerization reactions and additives can help for better adhesion or change the wetting behavior and viscosity of the ink. After the curing, hard baking is done to improve the final properties and also evaporation of remaining material except the polymeric structure. (see Figure 3.10)

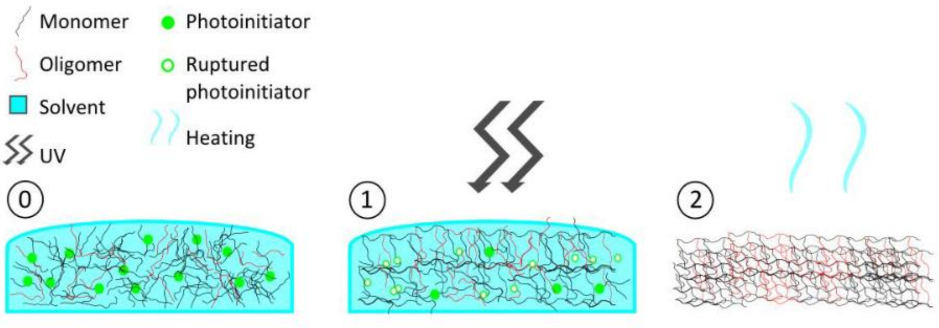
Monomer
Photoinitiator
Oligomer
Ruptured photoinitiator
Solvent
Heating
UV
⓪
①
②

Figure 3.10: Sequence for the curing of dielectric inks: (1) UV curing and (2) hard baking. [19]

4 Application of printing technologies to MEMS packaging

In the current conventional approach for MEMS manufacturing and packaging, subtractive methods like photolithography and thin-film technologies are used for material deposition. As pointed out in chapter 3, subtractive methods involve many process steps like mask preparation, applying photoresist, exposing, developing and cleaning. In contrast, in an additive fabrication process flow there are just two steps: contactless deposition of material only wherever is desired and then annealing or curing of material to be functional (see Figure 3.1). In additive method it is also possible to deposit even several material in the same step and deposit the material with no contact on nonplanar and/or sensitive substrates. Therefore, an additive manufacturing process can be much more flexible, consume less material, produce less waste and be more environmental friendly compared with conventional methods. However, still patterning resolution is not yet as good as lithography (<10 nm) [45], which can be improved by decreasing the volume of droplets (e.g. with SIJ), printing speed, surface treatments or optimization of the ink [1].

In MEMS manufacturing and packaging process, there are some parts that conductive, semiconductive or dielectric materials with specific properties need to be deposited on the surface or cavities in a subtractive manner. For the reasons mentioned above, the integration of alternative additive methods to the existing manufacturing process enables having the benefits from both technologies at the same time. This integrated approach can simplify the fabrication process, increase flexibility, decrease initial investment costs for production line, reduce production cost and environmental impact.

Figure 4.1 shows selected parts of the MEMS manufacturing and packaging, that additive and digital methods can potentially be used over existing conventional methods. In this chapter we explain these selected parts and see to what extent additive approach can be useful for fabrication of these parts.

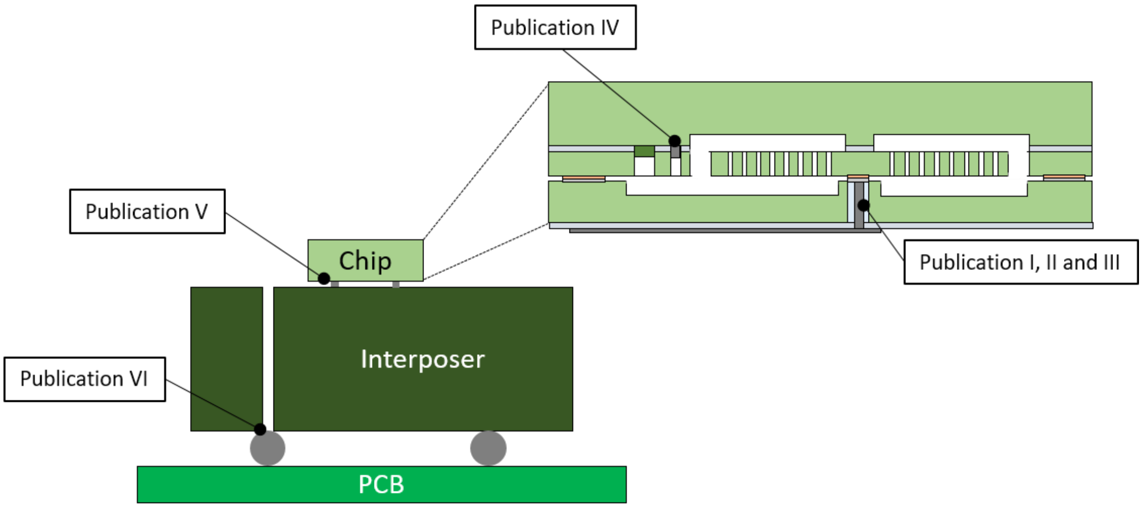

Figure 4.1: Selected parts of MEMS packaging with the potential to be fabricated by printing technologies.

4.1 Requirements specification for printing

In the case of TSV metallization (see 4.2), requirement for electrical conductivity depends heavily on the application. For instance, for RF devices 1 to 10 Ω might be required but for low frequency interconnection 100 Ω to 1 kΩ is acceptable and for electromagnetic compatibility (EMC) shielding even 1 MΩ might be enough. In our application and research, doped polysilicon would be the first choice to completely fill the vias and providing an all silicon structure with high thermal budget for subsequent processing. However, due to lack of inkjettable Si ink, commercially available nanometal inks with good conductivity and low electrical loss were considered as an alternative (e.g. Ag, Au or Cu inks). Gold ink could increase the cost and copper at high temperatures can diffuse into the silicon crystal which is harmful plus this fact that jettability and sintering of copper ink because of oxidation could be problematic. Therefore silver ink was selected as the optimum and cost efficient material with low resistivity to be used for the inkjet printing and metallization of the vias. Via resistance ≤10 Ω was the aim in our research and silver ink could provide reasonable conductivity which will be shown in 4.2. Polymer conductors like PEDOT:PSS and doped polyaniline (PANI) with the conductivities up to 4600 S/cm [46] and 4.60×10^{-7} S/cm [47] respectively, could also be considered but resistance of these materials is much higher than the nanometal inks. In addition, polymer conductors with low thermal budget cannot survive high temperatures in subsequent processing like bonding. Depending on the application, completely filled and void free vias or partially metallized vias are needed. Both of these cased are demonstrated in this thesis and will be covered in 4.2 below. For the complete filling using the inks with higher solid content could make the process faster but these type of inks with higher viscosities cannot be necessarily jetted and depends on the printing equipment and their availability.

In the case of wafer contact (see 4.3) also doped polysilicon is the first choice for the reasons mentioned above; but again because of lack of inkjettable silicon ink, nanometal inks can be considered. inkjettable silver and gold inks would be the second alternative for inkjet printing but it was found that these inks cannot provide ohmic contact in case of using p+ silicon. Therefore, aluminum ink can be chosen to be dispensed additively to the vias that can provide ohmic contact after the high temperature sintering.

In the case of interposer (see 4.5 below), complete filling of TSVs with copper, which would be attractive from inkjet printing point of view, will not work for the rigid interposers due to the mechanical stress from coefficient of thermal expansion (CTE) mismatch between silicon and copper. Therefore, in this specific case conventional copper plating was used to conformally plate the inner walls of the BS via holes and fill the FS vias. After via metallization the vias need to be filled with an elastic material using inkjet printing. This material should have low Young’s modulus and/or CTE close to that of silicon. Soft polymer based filling material that withstands the post processing soldering temperatures required for flip-chip assembly without changing the properties of the filling material is a potential candidate.

In short, TSV requirements are different for different applications like IC, interposer and MEMS. For IC, TSVs are just used for contacting thinned IC from the back side. For the case of interposer, TSVs are used to rerouting and no hermetic sealing is needed. It is a middle-wafer between IC and outer package or circuit which has no cavities. In MEMS, the TSVs are used either through the SOI layer or through the capping wafer. In the latter case it needs to be integrated with hermetic encapsulation with cavities and inner pressure control. That is more challenging than IC/interposer. Accordingly, it should be noted that the microstructure of the nanoparticle inks after the sintering will be with less boundaries but still with holes, so that making completely hermetic cavities is not possible with inkjet printing. However, in cases that hermecity is not required like interposer/IC, using nanoparticle inks is not problematic.

Detailed description of reliability is beyond this thesis, but in general the most relevant test for material interfaces, like interconnections, or ink material and silicon is thermal cycling which has been done to some level in this thesis. The different thermal expansion coefficient of materials causes cyclic load which may cause propagating failures. Another relevant reliability issue is high temperature storage life. Long storage at elevated temperature accelerates potential unwanted chemical reactions between ink material and silicon that needs to be addressed in material selection for inkjet printing.

4.2 TSV metallization

TSVs are one of the key elements in MEMS wafer level packaging and 3D integration that enables reduction of the die sizes to highest level and also integration of the MEMS, ICs and sensors. The short vias in cap wafers for instance are used to make shortest electrical path between the MEMS devices inside the cavities in one level and RDL tracks in another level. In order to have this shortest possible connection, the vias need to be metallized by a conductive material. For this purpose, blind vias in thick wafers (not totally etched through the wafer) are first covered by insulation and diffusion barrier layers. Next, a thin, uniform and continuous seed layer (e.g. Cu) is deposited as a base layer (using CVD/PVD) for the next phase which is growth of conductive material (typically copper) using plating [48]. After the plating, wafer thinning is done to open the bottom of the vias and finally excess copper is removed by polishing. For the interposer application with vias through the wafer, at the time of via plating, Cu redistribution layer (RDL) can also be plated on the both front side (FS) and back side (BS) of the wafer [49].

For most applications vias need to be completely filled but in some cases just partial metallization and lining with conductive material can be acceptable. Two main and stablished processes to fabricate conductive vias are electrodeposition of copper [50]–[55] or CVD of polysilicon [56], [57]. In case of complete filling the mismatch between the CTE of silicon and the metal filling can be problematic because of the stress induced by the thermal expansion; therefore, partial metallization could cause fewer yield and reliability issues compared with complete filling [58]. The current existing methods described above for the via metallization are mature but complicated with many process steps, time consuming, expensive and not environmental friendly because of the waste material. Therefore, alternative additive methods like inkjet enhanced technologies that can deposit the material just over the vias could be beneficial. These alternative methods with fewer process steps can simplify the metallization process for the vertical interconnects, reduce the cost and processing time and be much more environmental friendly.

In [59] a non-commercial silver ink is used to show how to achieve a homogeneous coverage of silver on the via walls. They claimed that metallization of just the via walls is more beneficial because of possible cracks during the sintering of completely filled vias. Fabrication of RDL and TSVs using a combination of inkjet and flexo printing is studied by K. Eiroma [60]. Plasma etched vias were covered only partially and then electrically characterized. In [61], commercial copper nanometal ink was used for the via filling and the effect of substrate temperature on the uniformity of the interconnect profile over the via is demonstrated. It is also concluded that crack-like void formation during the printing on the substrate with 30 °C could be attributed to the solvent evaporation. N. Quack et al. [62] have used commercial gold nanometal ink and a non-commercial inkjet setup to completely fill the vias with diameter of 50-100 µm without any void. The reported via resistance was 5 mΩ (<10% of the bulk resistivity).

In **Publication I**, tapered TSVs with top diameter of 80 µm and depth of 115 µm were metallized by the silver nanometal ink (NPS-J from Harima) and DOD inkjet printing (DMP-2800 printer) equipped with a cartridge producing 10 pl droplets. Provided tapered vias were fabricated in five steps. First in lithography step the photoresist etch mask is deposited and patterned. Then TSVs are etched by plasma followed by photoresist mask removal. Later, the TSV sidewall roughness is reduced by thermal oxidation and oxide etch. Finally, a thermal oxide layer is grown for the purpose of electrical insulation.

For the printing a pattern with 13 pixels and resolution of 5080 dpi (5 µm every pixel) was designed (Figure 4.2) so that every pixel was representing a droplet. Smaller circle in Figure 4.2 shows the diameter of droplet in air (26.73 µm for 10 pl droplet).

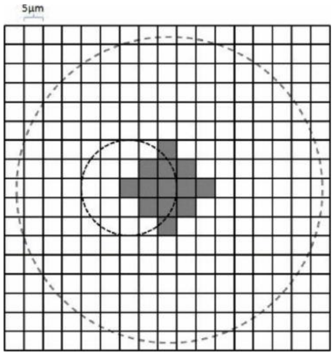

Figure 4.2: Printing pattern designed with the resolution of 5080 dpi. [63] © 2014 IEEE

The main aim of the study was to understand the effect of delay time between the layers and substrate temperature on the filling ratio and also quality and uniformity of the metal coverage of the via walls. Therefore three different substrate temperature was chosen and for every case printing with no delay and 30 seconds delay between the layers was tested. Sintering of the ink in all cases was done in 220 °C for one hour as recommended by the ink manufacturer.

Figure 4.3 shows the optical micrographs of cross-sections of all six cases after the sintering. Quality of the metal coverage was acceptable in all cases without any voids or cracks which can affect the conductivity of the vias adversely. From the results and thickness measurements it was understood that: (1) The substrate temperature and the delay between printing the consecutive layers both affect the number of the droplets that can be printed to the vias. However, it was concluded that the effect of the substrate temperature is more to print more droplets inside the vias. (2) The most ideal case was the case (Figure 4.3e) with substrate temperature of 60 °C and no delay between the printed layers. It was concluded because no over-flooding was observed and the wall coverage was maximum between all the cases. Also the coverage of the metal on top and middle of the vias was uniform. Higher temperatures could be beneficial in case of complete filling because of the faster solvent evaporation; but at the same time it may cause dryness of the nozzles and have a negative effect on the jetting reliability due to clogging of nozzles.

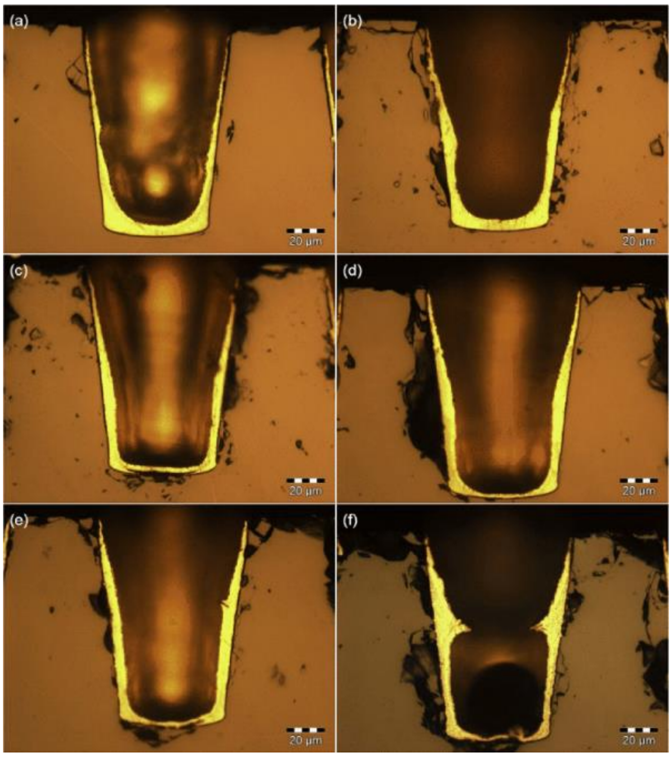

Figure 4.3: Optical images of cross-sections of the metallized vias. (a) substrate temperature (ST): 40 °C, delay: 0 sec, 4 layers, (b) ST: 40 °C, delay: 30 sec, 5 layers, (c) ST: 50 °C, delay: 0 sec, 6 layers, (d) ST: 50 °C, delay: 30 sec, 6 layers, (e) ST: 60 °C, delay: 0 sec, 6 layers and (f) ST: 60 °C, delay: 30 sec, 7 layers. [63] © 2014 IEEE

In **Publication II**, electrical performance of the partially metallized vias is investigated. The via structure used in **Publication I** were metallized by the same approach introduced in **Publication I**.

Sample for the electrical characterization of the vias was prepared in five steps as shown in Figure 4.4 and reported in [64]. After preparing the sample, a Keithley 2400 sourcemeter attached to a probe station was used for the electrical characterization of two pairs of metallized vias by landing of two probes on the two measurement pads. The resistance of 8.8 Ω for the whole structure including two pads and conductive tracks on top side (length: 5 mm, width: 100 µm), two via sidewall metallization and bottom track (length: 4 mm, width: 100 µm) on back side. With exclusion of printed metal layers on top and back sides from the total resistance and considering that both vias have same resistance, it was concluded that the resistance of a single via with a void free sidewall metallization could be less than 4 Ω which could be acceptable for some MEMS applications.

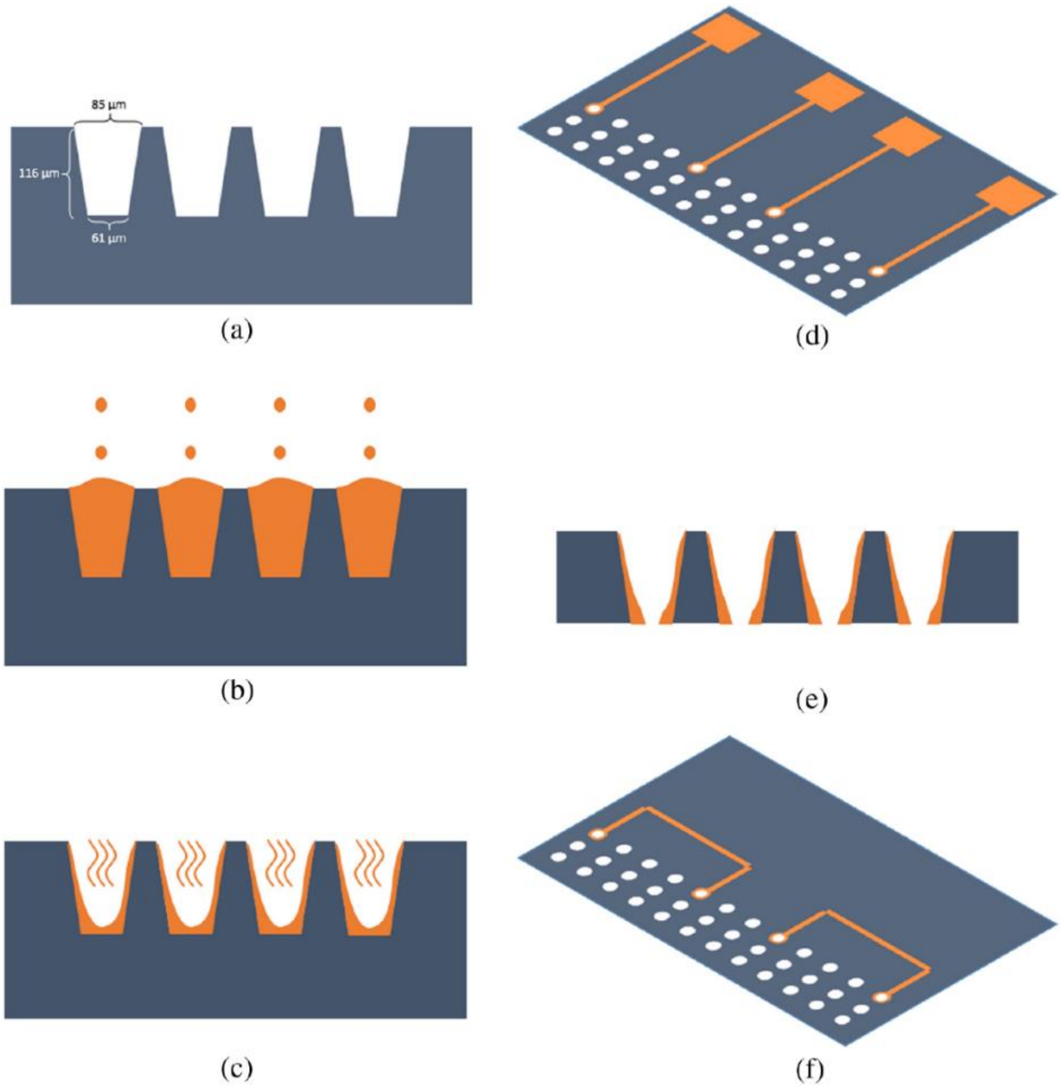

Figure 4.4: Sequence for the preparation of the sample for the electrical characterization: (a) fabrication of the vias, (b) vial filling by the inkjet printing, (c) solvent evaporation and sintering, (d) printing and sintering of conductive tracks and pads on the top side, (e) thinning of the sample to 100 µm, and (f) printing and sintering of conductive tracks on the bottom of thinned sample. [64]

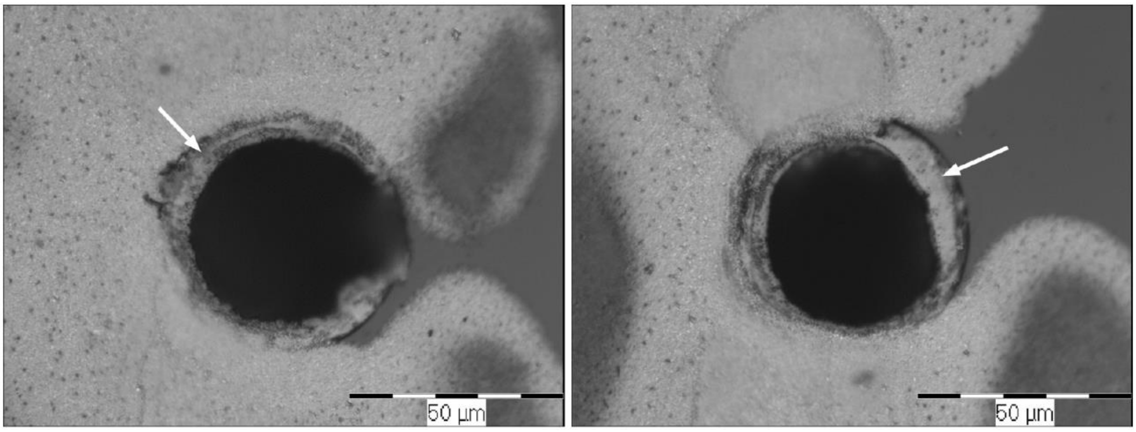

Figure 4.5: Coverage of the ink at the bottom of the vias after the thinning process. [64]

In order to increase the density of the 3D interconnections, very thin vias are needed with minimum possible pitch in between which enable increasing number of input/outputs per package. Very thin vias cannot be metallized by the conventional inkjet printers because the diameter of the produced droplets is usually larger than the diameter of the vias. In addition, the drop placement accuracy of conventional inkjet is limited to some micrometers. There are 1 pl cartridges available for inkjet printer that can provide droplets with diameter of 12.4 µm but the jetting is not stable enough and the nozzles cannot be functional long enough. Hence, another technology with much finer droplets need to be used for the case of high density vias.

In **Publication III**, feasibility of high density via metallization using super-fine inkjet technology (SIJ) was studied. SIJ printer can produce super-fine droplets with the size of less than one micron and volume of 0.1 femtoliter. Also, the evaporation of the solvent during the printing can happen much faster compared with the conventional inkjet without increasing the substrate temperature due to very small droplets. In addition, very small size of the droplets decreases the chance of air pocket formation inside the via fillings.

In **Publication III**, three different printing trials were tested with three different types of silver nanoparticle inks. Metallization of ten vias in a row with the top diameter of 23 µm was done by the bumping mode of the SIJ printer so that the nozzle comes over a via and dispense the ink inside the via until it is totally filled and then moves to the next via as shown in Figure 4.6. There are several printing parameters that can affect the printing time over a single via to fill it completely (e.g. amplitude voltage, bias voltage, waveform and frequency). Since the maximum printing time in bumping mode is 30 seconds, printing parameters were set so that a via with volume of 32.4 pl could be filled in 30 seconds. Because of the fast solvent evaporation and the delay until the nozzle comes over a via again (~120 s), every via can be filled for several times until there is no more room for printing more ink.

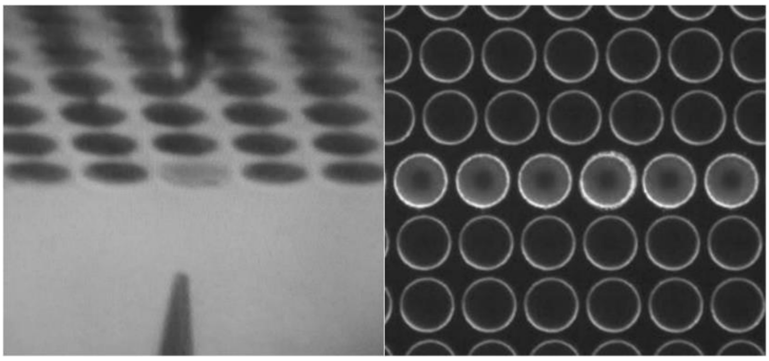

Figure 4.6: Bird view (left) and top view (right) of the filled vias by SIJ technology. Nozzle and its mirror image is shown in the left picture. [65] © 2015 IEEE

Between the three inks that were tested, NPS-J silver ink from Harima Chemicals with the metal content of 62~67 wt% was better compared with DGP 40LT-15C and cAg-2000 silver inks. After filling the vias completely by four times of printing inside the vias, samples were sintered in 220 °C for one hour as recommended by the ink manufacturer. Next, cross-sections of the metallized vias were made by dicing saw. Figure 4.7 shows the cross-sectional SEM image of the metallized vias that are completely filled uniformly with no substrate heating. The adhesion of the ink to the non-treated vias was very good so that the filling material could survive after the dicing saw cutting. Therefore, it was concluded that NPS-J silver ink could be a better and more reliable ink for the metallization of high density vias using SIJ technology.

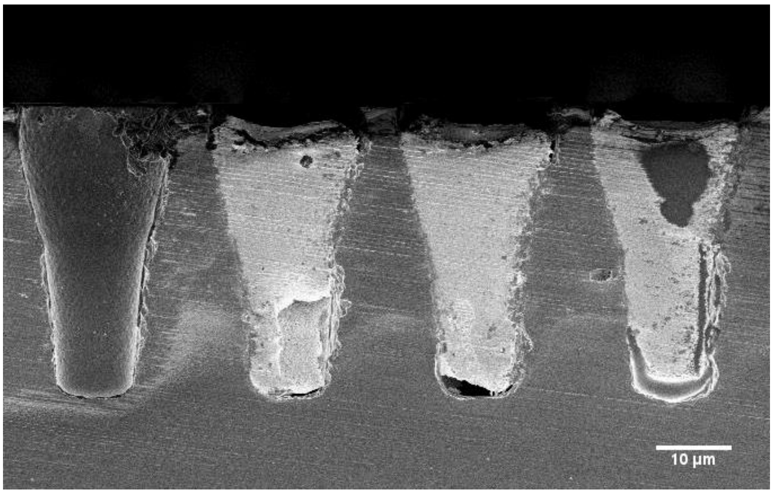

Figure 4.7: SEM cross-sectional image of the thin vias completely filled by NPS-J silver ink. [65] © 2015 IEEE

4.3 Making electrical contacts for SOI MEMS

Making the electrical bridge between the device layer and handle wafer for the silicon on insulator (SOI) MEMS is another part which is being done with packaging and wafer-level technologies. However, in case of increasing the size of the package or stresses related to the packaging, performance of the devices may be degraded. Also, wafer-level technologies, involve many process steps so that the cost of the device processing is increased and in the worst case the uniformity of the device layer thickness and performance of the device can be degraded. Therefore, a digital and additive metallization method with the minimum waste material and process steps can be a good and game changer alternative.

In **Publication IV**, aerosol jet printing (AJP) is introduced to jet a nanometal ink into designated cavities with no contact to make the connection between the device layer and the handle wafer. DOD inkjet printing could also be used to make this connection using gold nanoparticle inks in case of having MEMS devices built on n++ wafers. The samples were MEMS accelerometers with additional oblong or rectangular shape vias through the device layer (50 µm) provided by Murata Electronics. Diluted aluminum ink (Al-IS1000) from Applied Nanotech was used as the feed to the Aerosol Jet 300 CE with pneumatic atomizer manufactured by Optomec. As shown in Figure 4.8a, 10 sections of the wafer each including ten oblong and ten rectangular shape cavities (60 µm x 240 µm) were selected for the metallization. The cavities in every section were metallized by a specific set of printing parameters to see mostly the effect of geometry of the cavities and jetting time (from 1 to 10 seconds) on the quality of the printed material and also electrical performance of the connecting bridge. Optical microscopy (Figure 4.9) images showed that longer printing time can result in more uniform coverage at the bottom of the cavities. Splashes of the ink could be controlled by changing the ink viscosity and gas flow rate, shorter jetting time and using better nozzles.

After jetting over all the cavities. The wafer was first placed in the oven to make the ink dry. Later for the sintering the wafer was placed for just two minutes in a high temperature oven heated up to 800 °C as recommended by the ink manufacturer.

After the sintering, the four-point resistance measurement setup illustrated in Figure 4.8 b&d was used to do the electrical measurement over two adjacent frames; meaning that the measured resistance is for two vias and small part of silicon. Figure 4.10a shows the overall results out of the four-point via resistance measurements for all sections (1-10). The bars show 95% confidential intervals. The results showed the minimum resistance of 7.7 Ω and maximum resistance of 27.3 Ω. Therefore, resistance of less than 4 Ω was achievable for a single via. It was understood that the variation for the sections 1, 2 and

10 with shorter jetting time could be attributed to the amount of the material and process variation. Also, it was not possible to conclude that oblong cavities result in poorer connectivity. Figure 4.10b also shows decrease in the resistance as a function of jetting time. It could be claimed that five seconds is a critical point that the connection all around the bottom of the cavity is made and the resistance stabilizes. Couple of ohms increase in the resistance for ten seconds printing compared with seven seconds printing was related to the normal process variation.

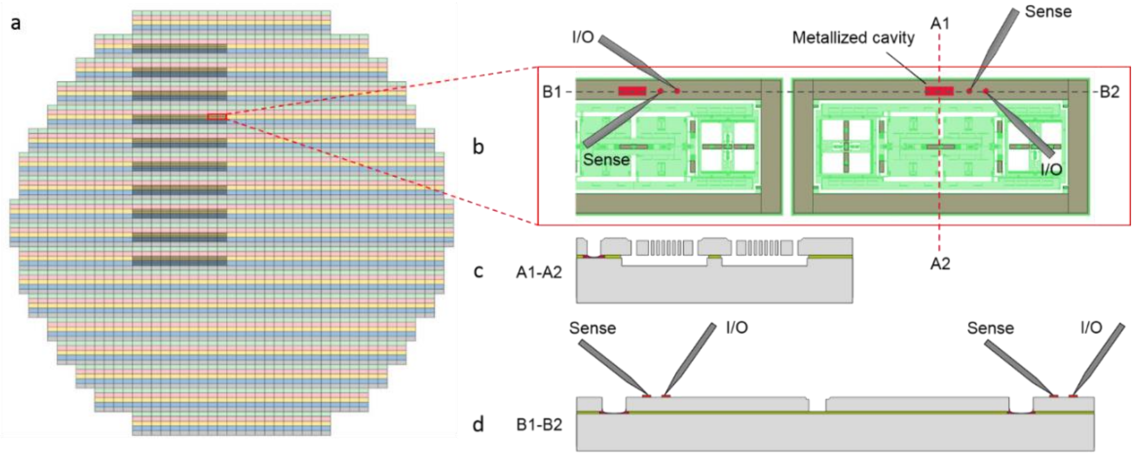

Figure 4.8: Schematic pictures of (a) metallized vias on device layer, (b) electrical measurement setup, (c) vertical cross-section of device frame and (d) horizontal cross-section of two neighbor device frames in electrical measurement. [66] © 2017 IEEE

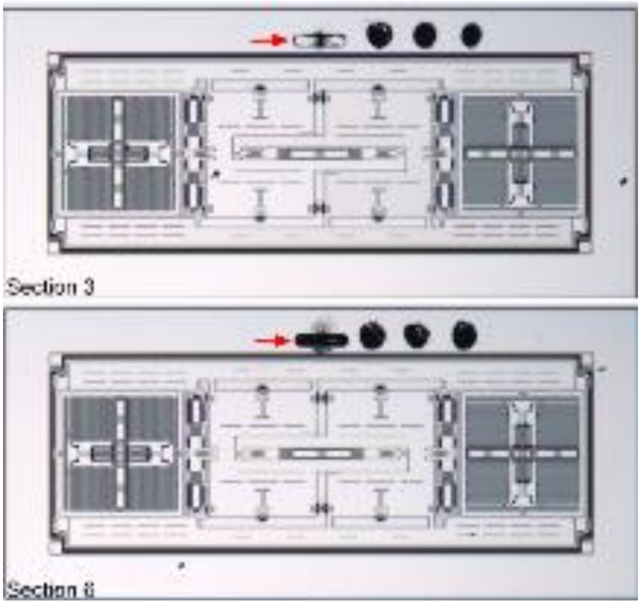

Figure 4.9: Top view if the metallized cavities after the sintering. Section 3 is after 1.5 sec printing and section 6 after 10 sec printing. [66] © 2017 IEEE

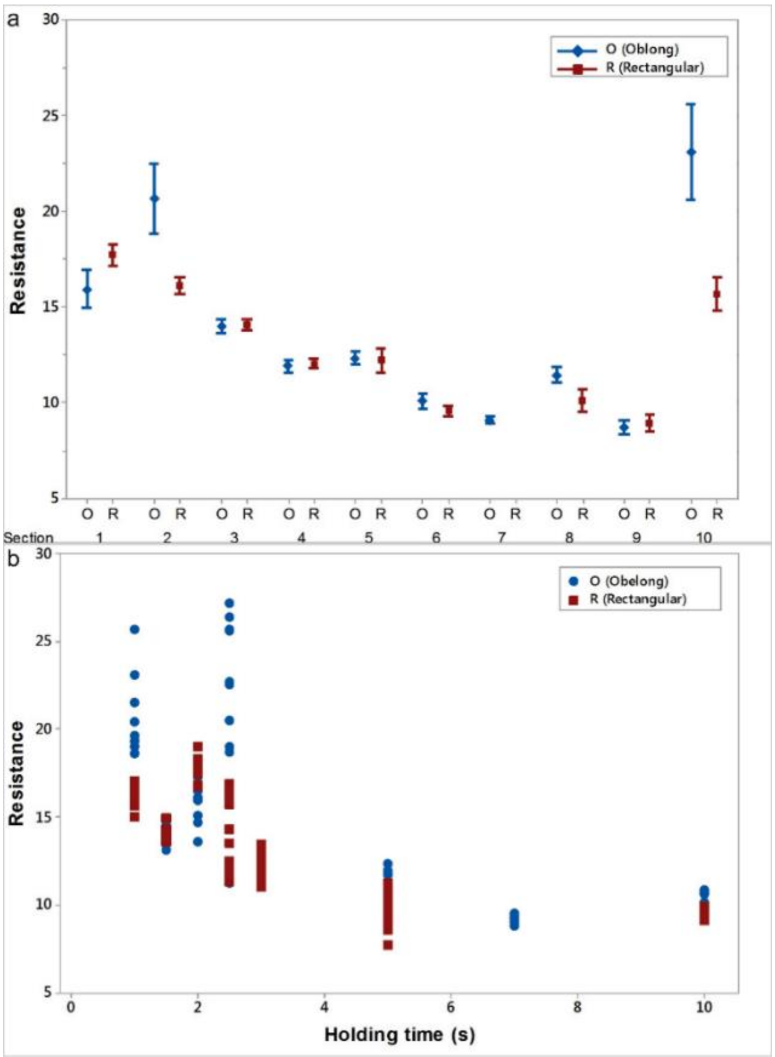

Figure 4.10: (a) Four-point via resistance measurements for sections 1-10 (sec 1: 2 sec printing, sec 2: 1 sec, sec 3: 1.5 sec, sec 4: 2.5 sec, sec 5: 3 sec, sec 6: 10 sec, sec 7: 7 sec, sec 8 and 9: 5 sec and sec 10: 2.5 sec). (b) The effect of jetting time on the resistance. [66] © 2017 IEEE

Cross-section of the metallized vias was imaged using SEM to study the effect of jetting time or amount of printed material on the uniformity of the metal coverage and resistance of the vias. Figure 4.11a shows a cavity without any metallization as a reference. Figure 4.11 (b) is showing a metallized via with 2.5 seconds printing (c) 1.5 seconds printing and (d) after 7 seconds printing. It can be seen that how printing more material can improve the conductivity. It could be explained by this fact that by longer jetting there is more chance for more uniform and better coverage at the very bottom corners of the cavities and having better connectivity. On the contrary, the poor coverage with the short printing time (Figure 4.11b&c) results in a lower connectivity but still beneficial and enough for making a conductive bridge.

Additive and digital fabrication of the metal contacts in this work was found to be much more straightforward and promising compared with the printing processes already explained in Publications I, II and III. It is because of this fact that dispensing just a small amount of ink can be much faster so that it can be considered for fabrication of a large number of wafer contacts with ohmic contact.

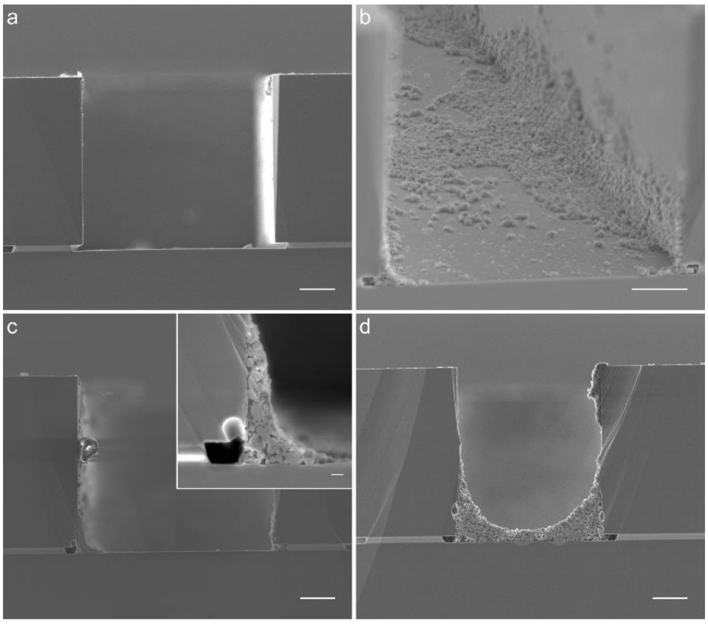

Figure 4.11: SEM images showing cross-section of the (a) non-metallized cavity, (b) partially metallized cavity after 2.5 seconds jetting, (c) partially metallized cavity after 1.5 seconds jetting and (d) partially metallized cavity after 7 seconds jetting. Scale bars are 10 µm. [66] © 2017 IEEE

4.4 Fabrication of metallic micropillars for bare-die flip-chip bonding

MEMS packages are assembled on the interposers by wafer level solder bump processes or stud bumps fabricated by wire bonding in chip level. In **Publication V**, the feasibility of using inkjet printed silver micropillars instead of stud bumps is investigated to avoid wire bonding or packaging of the chips. The introduced approach could decrease the cost and also increase the functionality and pitch density of the chips because of smaller diameter of printed micropillars compared with the bumps fabricated by wire bonder (50-70 µm).

In contrast with Publications I, II and III that jetting nanometal inks to fabricate metallized TSVs was not promising, here DOD inkjet printer was successfully used to print 3D metal micropillars using NPS-J silver ink from Harima on two edges of the test chips. It was understood that substrate temperature (solvent evaporation during the printing), printing speed (controlled by print resolution) and initial wetting of the ink play an important role for the growth of the micropillars. Therefore, the substrate temperature was set to the maximum (50 °C) and a special chemical surface treatment was done (using 2.5% 3M EGC-1720) on the substrate to obtain the optimal wetting of ink at the beginning of printing. Figure 4.12 shows the effect of chemical treatment on the initial wetting of first printed droplets. Micropillars with different numbers of droplets (8, 10, 12 and 14) and approximate heights of 20.9 µm, 25.9 µm, 33.3 µm and 35.9 µm were printed/fabricated (see Figure 4.13). Diameters of 22 µm for the printed micropillars and a height of approx. 3 µm per droplet were measured. Theoretical calculations also resulted 3 µm height for each dried droplet. Calculations were based on volume of droplets after solvent evaporation and radius of the micropillars (11 µm). Comparison of experimental heights and theoretically calculated heights are shown in Figure 4.14. First droplets do not contribute to the height of the micropillars and just wet the substrate; therefore first droplets are excluded for the calculation of theoretical data points. Slight difference for the pillars fabricated by 10 and 14 droplets could be related to the process variation that may result in higher or lower metal in every droplet.

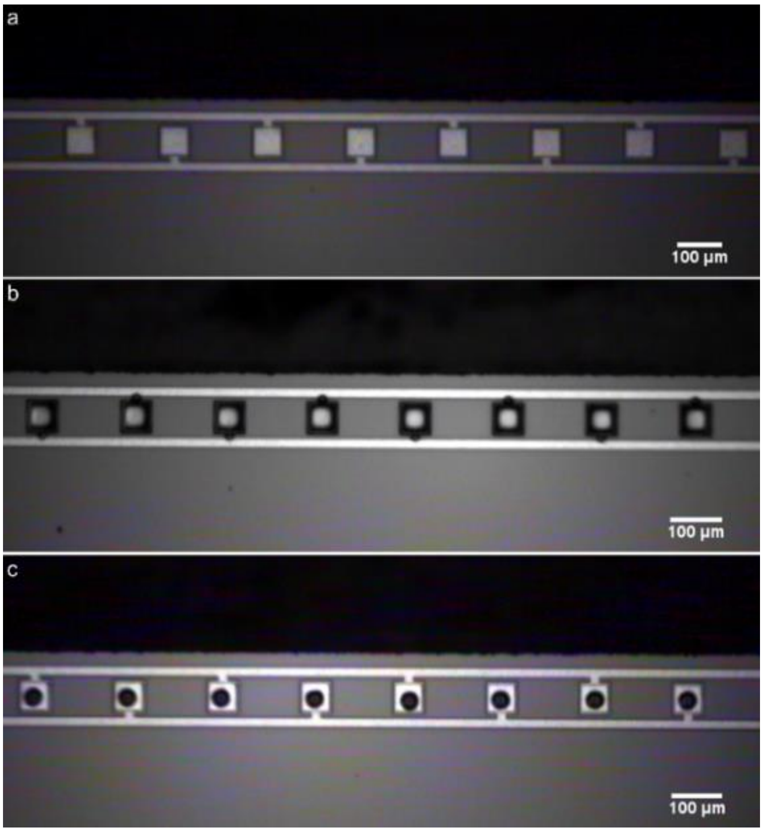

Figure 4.12: Magnified top view of the edge of the bare dies with (a) Aluminum pads before printing, (b) droplets printed on top of pads with no surface treatment and (c) droplets printed on top of pads with chemical surface treatment. [67]

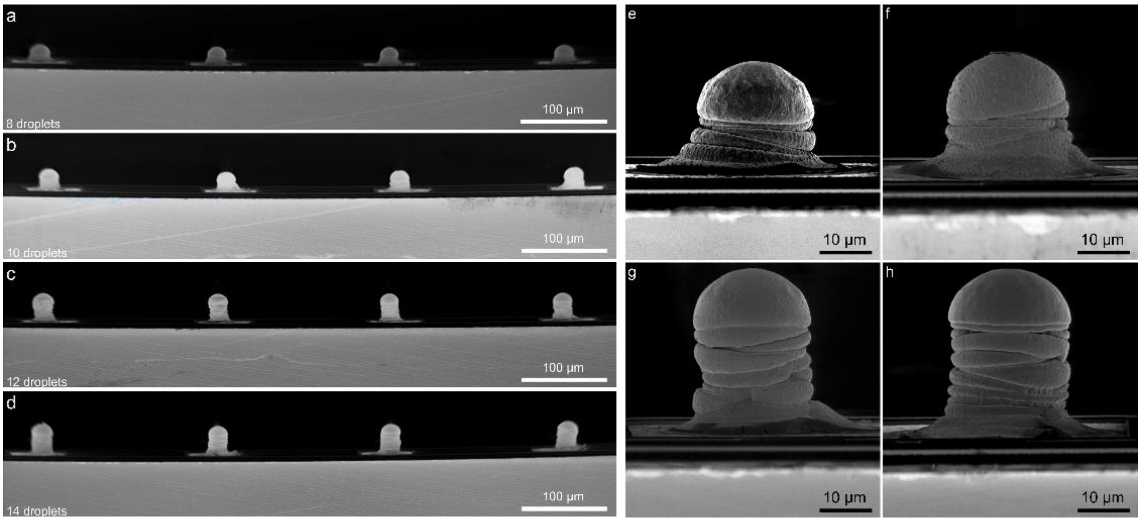
a
8 droplets
100 µm
b
10 droplets
100 µm
c
12 droplets
100 µm
d
14 droplets
100 µm
e
10 µm
f
10 µm
g
10 µm
h
10 µm

Figure 4.13: SEM images of fabricated micropillars by (a) 8 droplets (single pillar shown in (e)), (b) 10 droplets (single pillar shown in (f)), (c) 12 droplets (single pillar shown in (g)) and (d) 14 droplets (single pillar shown in (h)). [67]

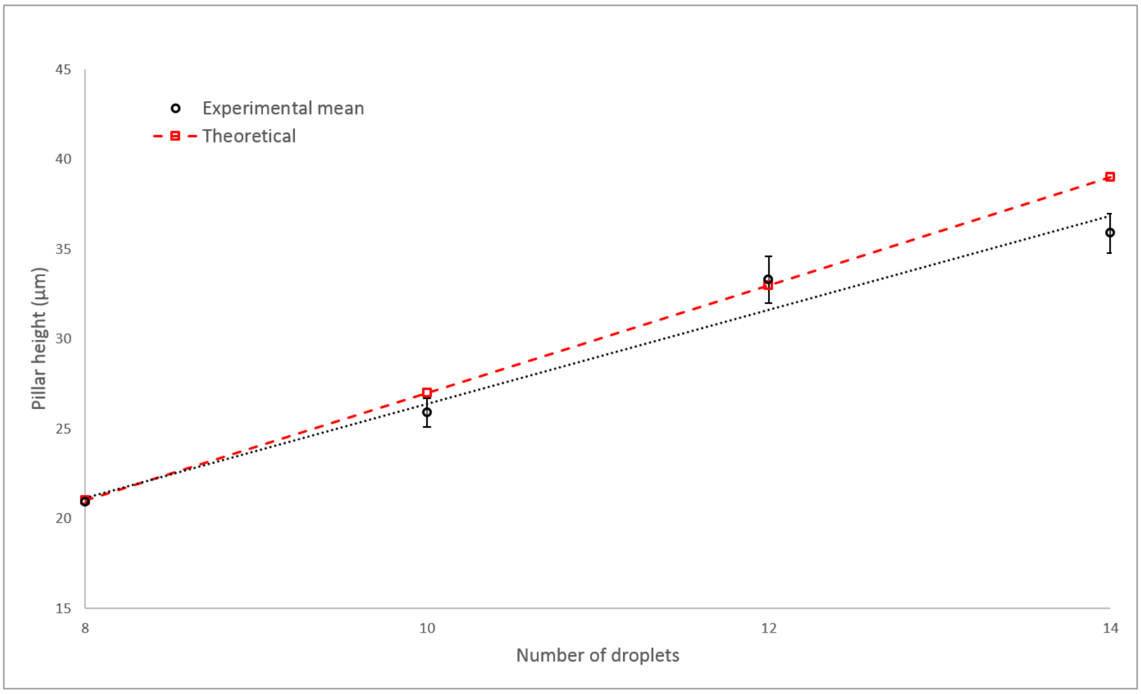

Figure 4.14: Comparison of the experimental heights of the printed pillars with the theoretically calculated heights. [67]

After printing the micropillar bumps on the Al pads, samples were sintered on a hotplate heated to 200 °C for one hour and then cleaned by plasma (ionized gas). Next, as proof of concept, test chips with the printed bumps were finally aligned and assembled on top of the PCB substrate (as shown in Figure 4.15) using flip-chip bonding while the anisotropically conductive adhesive (ACA) was already pre-bonded over the substrate. Bonding can be even done just with the ACA to provide mechanical adhesion and chip-pad interconnection. However, to improve the reliability of the interconnects, printed bumps are needed in addition to ACA layer.

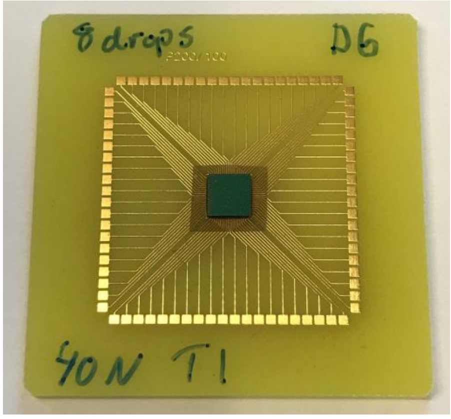

Figure 4.15: Bumped test chip placed and bonded over the PCB substrate using flip-chip bonding. [67]

After the bonding, resistance between the adjacent and connected pads (1-3, 2-4, 3-5, etc.) were measured. Two bonded chips with no bump also were tested to see the effect of using printed bumps. Figure 4.16 presents the cumulative distribution of measured values of bonded chips with and without the printed micropillars/bumps which shows the positive effect of bumps (with bumps, sharp distribution <5 Ω at 1.2 Ω).

Since the high resistance or an open circuit could just be because of just one failed connection on one pad, it was decided to classify the whole data of resistance measurements. Resistances less than 5 Ω (2.5 Ω/bump + trace) were classified as good, between 5-60 Ω as poor and higher than 60 Ω as failure or open circuit. In addition, most of the open circuits were found to be from the corners where proper alignment is not possible because of the failure coming from the PCB design. Hence, the values from the corners were excluded in order to make a better conclusion. Figure 4.17 depicts the proportion of I/O connection performance for the bonded samples with and without bumps. It could be concluded that reliability of the I/O connections can be dramatically improved by using printed bumps so that about 88% of the bumped pads had a resistance less than 2.5 Ω per bump while this quality of connection was seen just for 17% of the pads with no printed bump. Furthermore, it was found that the height of the pillars or droplet count do not have significant effect on the resistance and failure rate.

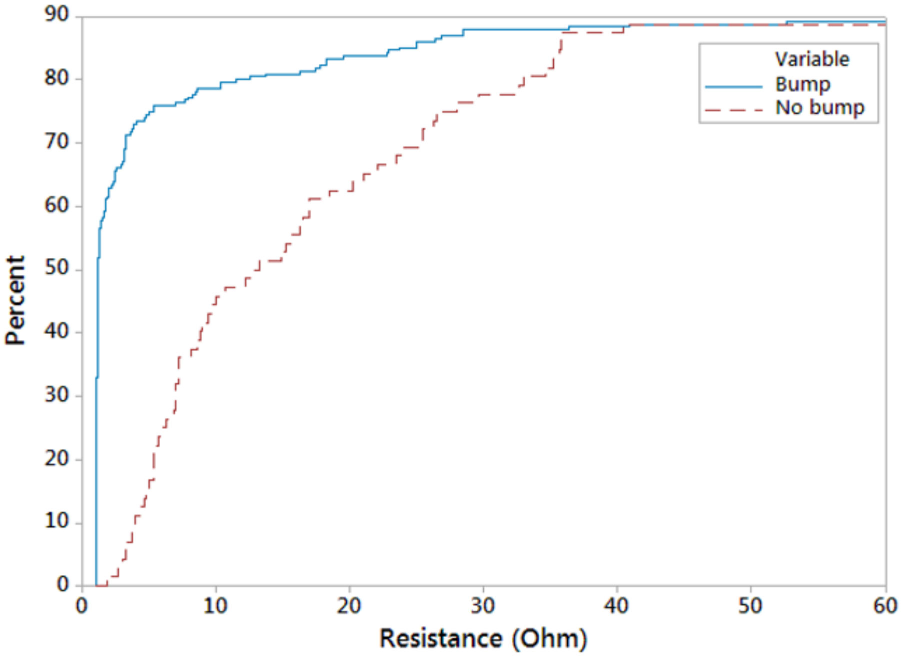

Figure 4.16: Cumulative distribution of resistance values of the bonded samples with and without printed micropillars or bumps. [67]

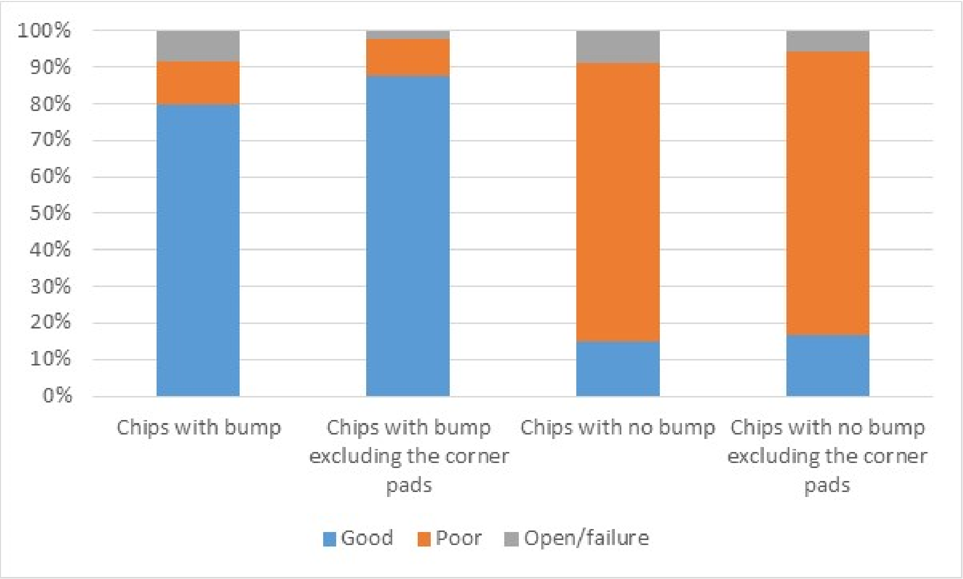

Figure 4.17: Representation of I/O connection performance for the bonded samples with or without the printed bumps. Good: <5 Ω/pair or 2.5 Ω/bump, Poor: 5-60 Ω, Open circuit/failure: >60 Ω. [67]

4.5 Increasing the I/O density of 3D TSV interposers

Filling of the through silicon vias by polymers can also be beneficial for 3D wafer level packaging (3D WLP) and interposer applications. Interposers are used in packaging to have higher integration level of integrated circuits chips (ICs) and printed circuit boards (PCBs) which enable moving towards miniaturization and increasing functionalities [68], [69]. In addition, silicon interposers can act as a suitable interface between the PCB and IC and MEMS dies to decrease the stresses originating from different I/O densities between the components and CTE mismatch between materials used in different levels like silicon (for MEMS and ICs chips) and polymer laminates (for PCBs).

In the current conventional fabrication approach for the silicon interposers, the solder balls are placed next to the hollow metallized vias. This kind of fabrication has a large footprint that results in low I/O density. There are two solutions to decrease the pitch between the solder balls and increase the I/O density: reducing the via diameters and/or placing the UBM pads and solder balls directly on top of the vias. The conformal metallization of smaller vias by chemical vapor deposition (CVD) or physical vapor deposition (PVD) is problematic with practical limitations. Hence, the second solution (placing the solder balls on top of vias) is preferable.

In **Publication VI**, the feasibility of placing the UBM pads and solder balls on top of the hollow TSVs filled with a compatible material, is well investigated. Comparison of the conventional fabrication approach with the approach presented in **Publication VI** is presented in Figure 4.18. Inkjet technologies (DOD and SIJ) were used to fill the vias with an inkjettable UV-curable hybrid polymer in order to be able to deposit UBM layer directly on top of the vias with SIJ technology and later dispensing the solder balls on top of the UBM layers as a proof of concept. Metallized TSVs could also be fabricated inkjet printing and copper ink; however, even though the results in Publications I, II and III were promising, it was found that metal inkjet printing for the partial metallization could be challenging and is still not mature enough to be used instead on conventional copper plating.

The filling material/ink need to be selected based on four important parameters: (1) low Young’s modulus to introduce least possible stress, (2) low-k for obtaining good RF properties, (3) CTE as close as possible to the CTE value of Si and Cu to have the minimum stress level during temperature cycling and soldering process and finally (4) low shrinkage during the curing process of material. According to the mentioned criteria, an inkjettable UV-curable ink with commercial name of InkOrmo from micro resist technology was found as the most optimum material to fill the hollow vias.

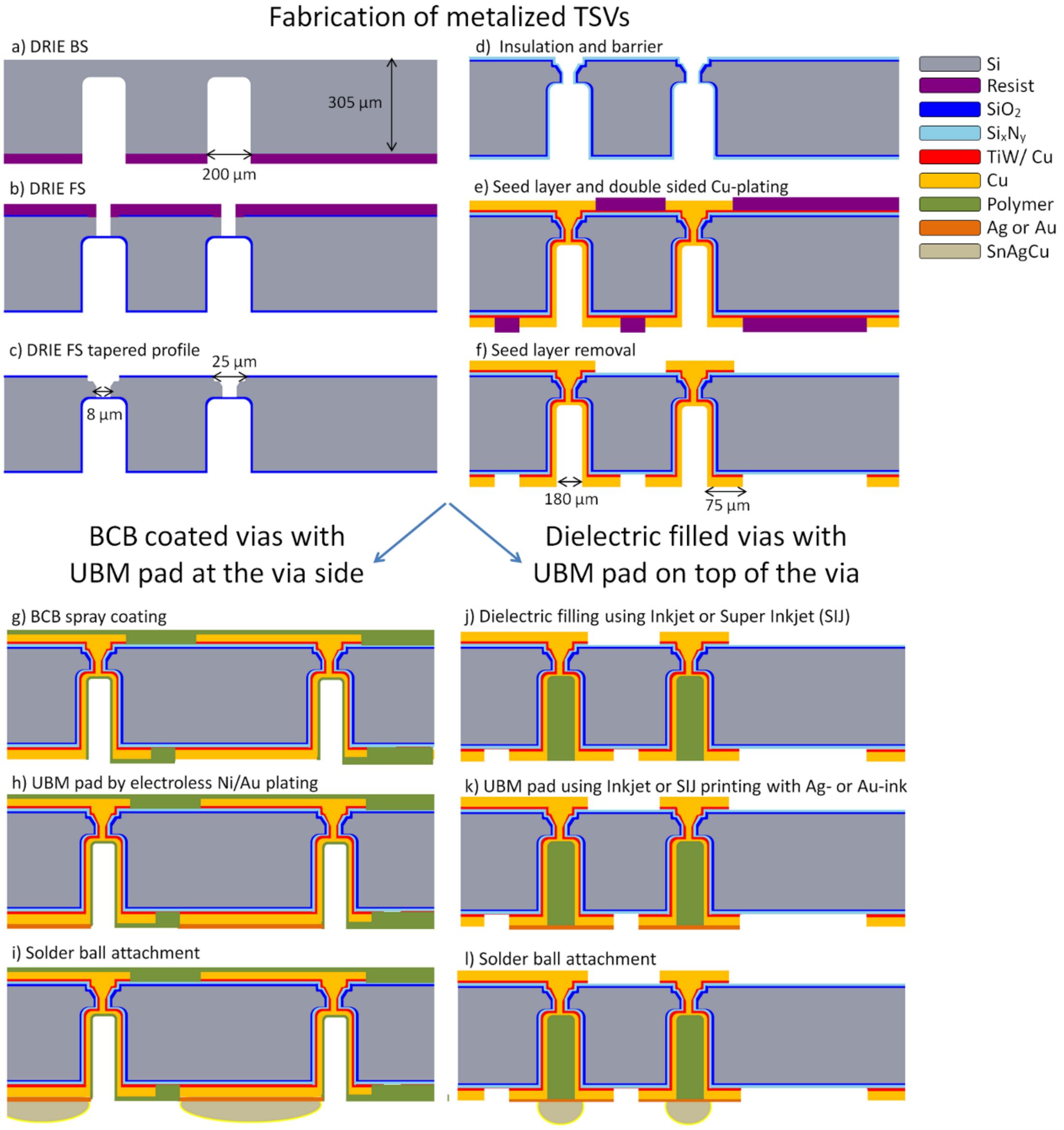
Fabrication of metalized TSVs
a) DRIE BS
305 µm
200 µm
b) DRIE FS
c) DRIE FS tapered profile
25 µm
8 µm
d) Insulation and barrier
e) Seed layer and double sided Cu-plating
f) Seed layer removal
180 µm
75 µm
Si
Resist
SiO₂
SixNy
TiW/ Cu
Cu
Polymer
Ag or Au
SnAgCu
BCB coated vias with UBM pad at the via side
Dielectric filled vias with UBM pad on top of the via
g) BCB spray coating
h) UBM pad by electroless Ni/Au plating
i) Solder ball attachment
j) Dielectric filling using Inkjet or Super Inkjet (SIJ)
k) UBM pad using Inkjet or SIJ printing with Ag- or Au-ink
l) Solder ball attachment

Figure 4.18: (a-f) Sequence for the fabrication of TSVs. (g-i) Conventional fabrication method with the solder balls beside the vias. (j-l) The alternative approach to place the solder balls on top of the vias to increase the I/O density. [49]

Dimatix inkjet printer (DMP-2800) with 10 pl cartridge (DMC-11610) and super-fine inkjet technology (SIJ-S050) both were used to dispense the dielectric ink into the vias. The pattern made for the Dimatix inkjet printer was a square pattern with 11 x 11 pixels (121 droplets) with the resolution of 5080 dpi (drop space of 5 µm). For the solvent evaporation during the via filling vacuum oven was used to avoid formation of the air pockets inside the fillings. After the printing, the dielectric was prebaked (50-60 °C for 15-30 min), then UV-cured for about 20 seconds (500-1500 mJ cm^{-2}) and finally the samples were placed on the hotplate heated to 150 °C for three hours for the final polymer hard baking. Light microscope images of the cross-section of filled vias showed sufficient level of filling with no air pockets for both Dimatix printer and SIJ printer. However, filling level and planarity of filling at the surface of the vias was better for the vias filled by SIJ technology. In addition, it was understood that for the applications with small number of vias, SIJ technology would be faster for the via filling compared with the conventional inkjet printing. It should be noted here that detachment of the filling could be observed because of not proper substrate cleaning. For the adhesion issues, adhesion promoters could be beneficial.

Cross-sections of the filled vias after 250, 750 and 1000 cycles of temperature cycling test were imaged by SEM to investigate the reliability of the TSV interposers. As shown in Figure 4.19, shrinkage and delamination of the polymer filling was increased by increasing the number of temperature cycles. The defects could be related to the mismatch between the CTE values, polymer shrinkage and adhesion issues. The interface between the Cu and Si was not affected by temperature cycling test up to 1000 cycles**.** It can be said that jetting dielectric material into the via cavities has its own challenges, but clearly is more reasonable in longer run compared with fabrication of metallized TSVs which is covered in Publications I, II and III.

For deposition of Ag or Au UBM layer on top of the filled vias again both conventional inkjet printing and SIJ technology were used. Printing the silver UBM layer by conventional inkjet was not successful since the ink tended to be in the center so that the silver coverage at the top edge of the vias was not enough for good electrical connection to the copper RDL layers. On the other hand, printing Au UBM layer using SIJ technology and spiral movement of the nozzle was quite promising because of a good circular coverage on the whole via filling and copper collar around the edge of the vias as shown in Figure 4.20. After UBM layer deposition, two samples were studied after 250 and 500 cycles of temperature cycling test to see the reliability of the UBM pads. As depicted in Figure 4.21, after 250 cycles, micro-cracks were observed for the sample 1 at the interface between the edge of the via and copper collar and just one micro-crack was observed for the sample 2. However, by addition of 250 more cycles, no other defect was added to the UBM pads.

The electrical testing of the via chains with the filling after temperature cycling reliability testing (-40 °C to +125 °C) up to 1000 cycles showed no open circuit or significant change in the electrical resistance of the vias. Hence, it was concluded that the difference between the CTE of Si, Cu and polymer filling material do not affect the electrical functionality of the TSVs by for example damaging the plated copper lining during the temperature cycling.

For the proof of concept, SnAgCu paste was successfully jetted on top of Au UBM pads as shown in Figure 4.22a. Figure 4.22b illustrate how jetting the solder balls on top of the vias could result in a higher I/O density and lower pitch. It is shown that pitch between the balls can be decreased from 1000 µm (1 I/O per mm^2) to 500 µm (four solder balls per mm^2) that results in four times higher I/O density without decreasing dimensions of the TSVs.

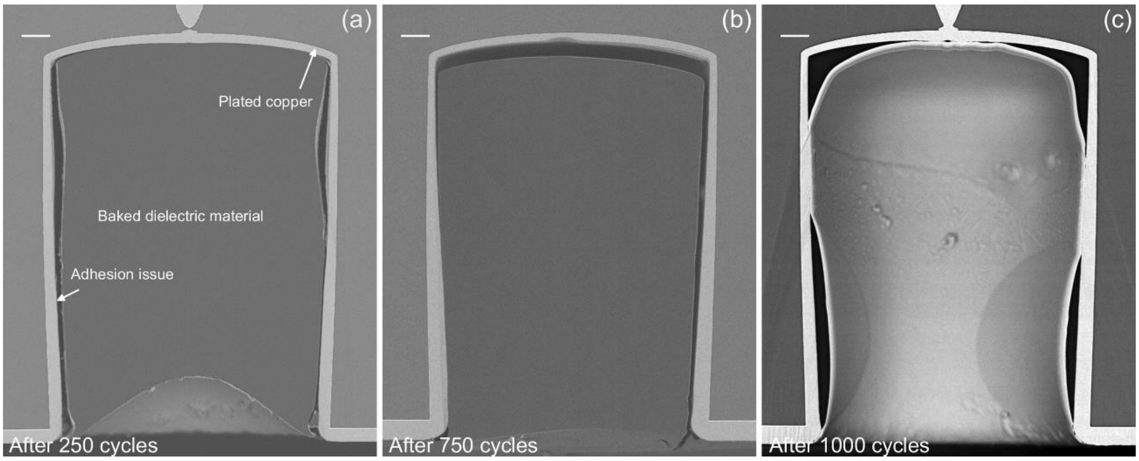
(a)
Plated copper
Baked dielectric material
Adhesion issue
After 250 cycles
(b)
After 750 cycles
(c)
After 1000 cycles

Figure 4.19: SEM cross-sectional images of the vias filled by the polymer after the tempreture cycling stress test with (a) 250 cycles, (b) 750 cycles and (c) 1000 cycles. Scale bars: 20 µm. [49]

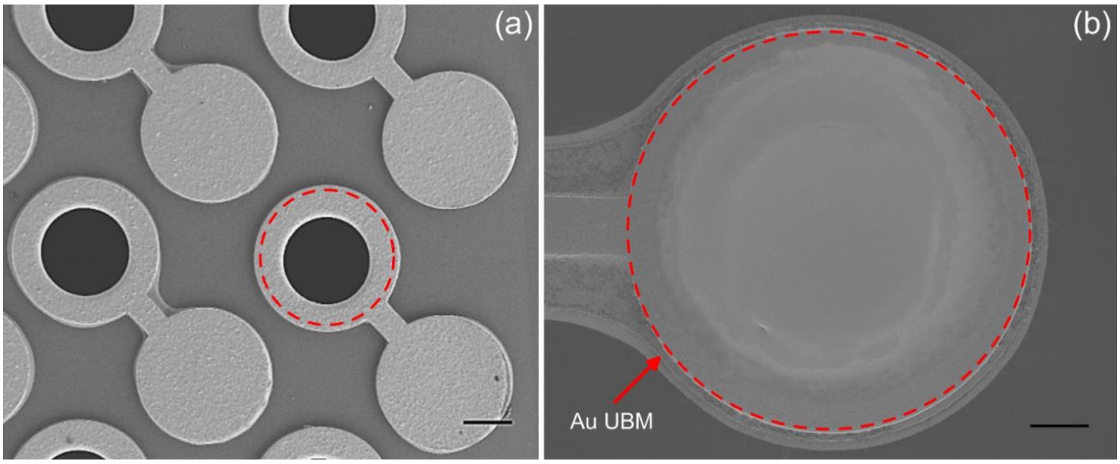

Figure 4.20: SEM images showing (a) top view of the empty vias and (b) UBM layer deposited over the via filled already by the polymer material using SIJ technology. Scale bar for (a) is 100 µm and for (b) is 50 µm. [49]

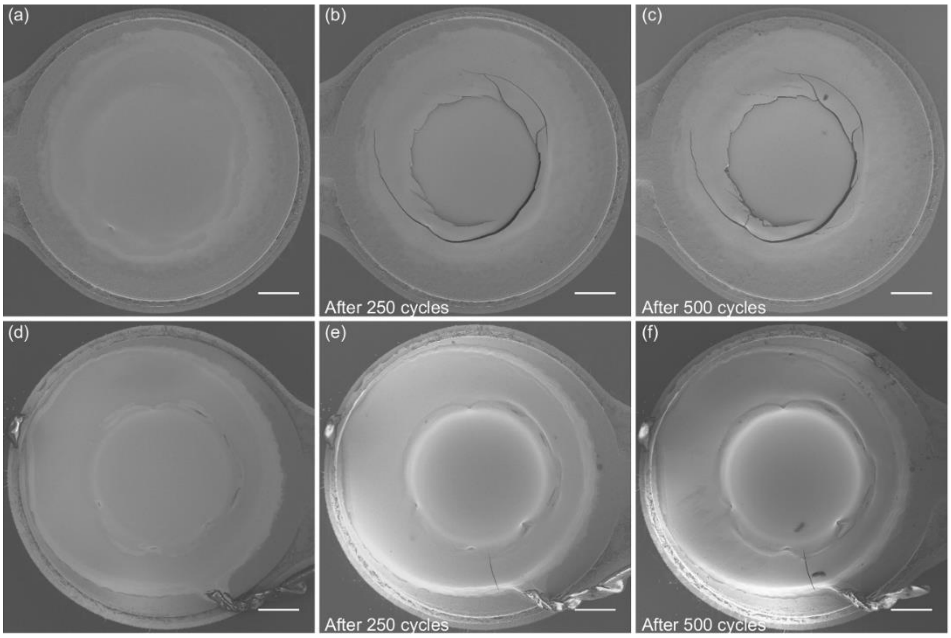
(a)
(b)
(c)
After 250 cycles
After 500 cycles
(d)
(e)
(f)
After 250 cycles
After 500 cycles

Figure 4.21: SEM images of the deposited UBM layers. Sample #1: (a) before temperature cycling test, (b) after 250 cycles and (c) after 500 cycles. Sample #2: (d) before temperature cycling test, (e) after 250 cycles and (f) after 500 cycles. Scale bars: 50 µm. [49]

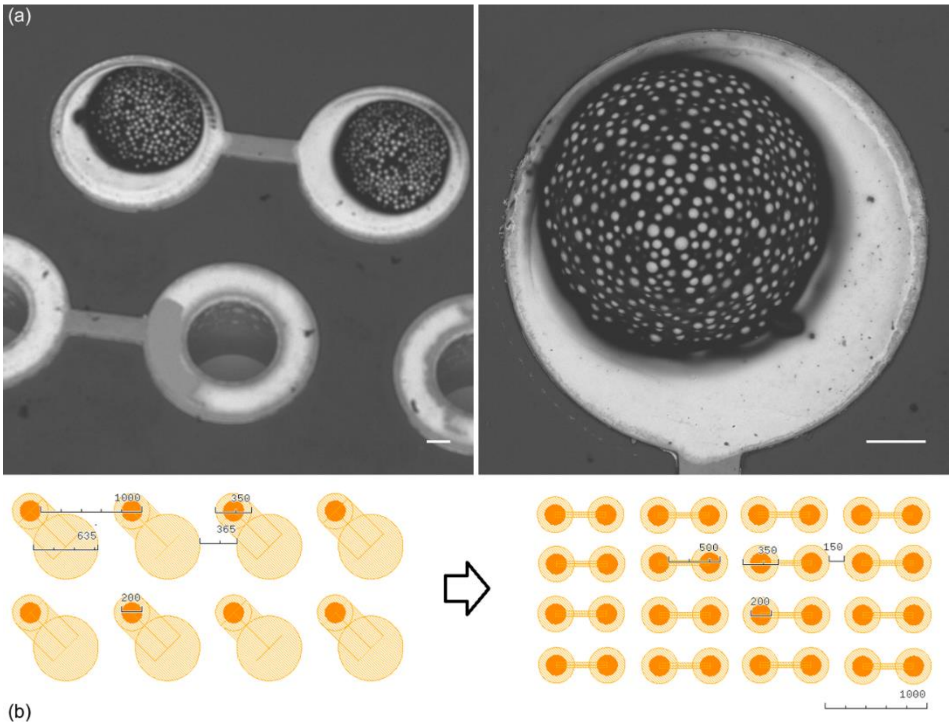
(a)
1000
635
350
365
200
500
350
150
200
1000
(b)

Figure 4.22: (a) SEM images showing the feasibility of solder ball placement over the vias. Scale bars are 50 µm. (b) The schematic picture demonstrates how the I/O density of TSV interposer can be increased with the reported approach in [49].

4.6 Pros and cons of using printing technologies for the fabrication of 3D interconnects

The results out of the individual papers appended to this thesis are already reported in this chapter separately. Nevertheless, Table 4-1 summarizes pros and cons of using printing technologies for making 3D interconnects to highlight the results better.

Table 4-1: Pros and cons of using printing technologies for making 3D interconnects.

	Pros	Cons
TSV metallization **(Publications I, II and III)**	+ partial metallization without void and or cracks + promising electrical performance (< 4 Ω/via) + possible to metallize thin and high density TSVs using SIJ technology	- not easy to completely fill the vias because of the ink shrinkage - not mature enough to print metal with consistent thickness from top to bottom of the vias like e.g. copper plating - not mature yet to be applied for the wafer level and large number of devices
Wafer contact **(Publication IV)**	+ making the ohmic contact with the minimum amount of material (<4 Ω/via) with Al ink and AJP + it is feasible to make the contacts in large scale and wafer level	- currently not possible to make ohmic contact using common and commercial inkjet inks (e.g. Ag and Au) and piezo inkjet in case of MEMS devices built on p-type wafers
Micropillar printing **(Publication V)**	+ feasible to fabricate and reproduce uniform µpillars + printed µpillars with small diameter enables increasing the pitch density and level of miniaturization + printed µpillars can result in higher contact reliability	- still the process should be optimized for printing on horizontal edges and vertical edges of the chips at the same round of printing
TSV interposer **(Publication VI)**	+ printing was successfully used to increase the I/O density of 3D TSV interposers by four times without making the vias thinner + electrical testing result after the temperature cycling was promising and did not show significant effect on DC resistance of the vias	- making a planar finish for the polymer filling is challenging - using SIJ to print UBM layers was successful but SIJ is still not a suitable option for printing large numbers of UBM layers - complete filling of the vias by polymer material was successful but still better equipment is needed for large number of vias - after the temperature cycling, shrinkage and delamination of the polymer filling as well as some micro-cracks were observed that should be addressed for future studies

Conclusions

Over the past few years, popularity of printed electronics and especially inkjet printing technologies has been increasing in the research and development field. However, still more studies and information is needed before using digital and non-contact fabrication methods in electronics manufacturing industry and at large scales. In fact, integration of new methods and processes into the existing production lines should not compromise reliability, yield, throughput or device quality. This thesis, and its publications, mainly look into the feasibility of using digital and non-contact methods instead of subtractive processes, in selective parts of the MEMS manufacturing and packaging. The results reported in this thesis show that maskless, additive and cost saving printing technologies offer attractive possibilities to be implemented in MEMS manufacturing.

In **Publication I and II**, piezo inkjet printing was used to partially metallize TSVs with conductive nanometal ink. The quality of the metal layer was acceptable with no voids or cracks. In **Publication I**, it was found that printing over vias heated to 60 °C and no delay between the printed layers during the printing can be more optimal. Heating of the vias to higher temperatures could be favorable for the complete filling of the vias because of the faster solvent evaporation during the printing but also it may result in dryness of the nozzles and poor jetting. In **Publication II**, the electrical performance of the partially metallized vias was studied and it was realized that the resistance of a single metallized via from top to bottom can be less than 4 Ω which could be beneficial for some MEMS applications. In the case of high density TSVs, since the droplet diameter of conventional inkjet is not small enough for metallization of very narrow vias, super-fine inkjet technology (SIJ) with sub-femtoliter droplets was used in **Publication III** to fill the vias completely with conductive metal ink. Just four times of printing was enough to completely fill thin vias without heating the substrate during the printing. The uniformity and quality of the fillings was promising.

In **Publication IV**, using aerosol jet printing to make electrical contacts in SOI MEMS devices (here MEMS accelerometer) was introduced. Ohmic connection between the device layer (p-type) and handle wafer (p-type) over the buried oxide was successfully made with the minimum amount of material (Al nanometal ink). The resistance of a single via was measured less than 4 Ω even with a short jetting time. The effect of the via shapes was not significant on the resistance. It was shown that printing or jetting time has the most important role to decrease the resistance of the vias. Piezo inkjet printing can also be used for making a proper contact using inkjettable gold inks in case of availability of MEMS devices built on n++ wafers.

In **Publication V**, inkjet printing is used to fabricate 3D silver bumps as an alternative to stud bumps and their potential use in flip-chip fabrication methods is studied. Smaller diameter of inkjet printed bumps can enable increasing the pitch density and level of miniaturization. The inkjet printed silver bumps with high level of uniformity and reproducibility could be fabricated. This study also shows that the printed bumps can result in much higher contact reliability in flip-chip bonding of bare dies compared with the unbumped chips with just anisotropic conductive film. It is reported that about 88% of the bumped pads had a resistance less than 2.5 Ω per bumps compared with just 17% for the unbumped dies.

In **Publication VI**, a novel approach is proposed to increase the I/O density of 3D TSV interposers. In the current approach, solder balls needed for the assembly of the interposers are placed beside the vias which requires a large footprint. This publication reports how additive methods (piezo inkjet and super inkjet) can be used to decrease the footprint and increase the functionality of the interposers. Piezo inkjet and SIJ technology were used to fill and planarize the TSVs (almost planar surface with SIJ) by a dielectric polymer with low Young's modulus. Later SIJ technology was successfully used to deposit circular UBM pads on top of the vias using Au or Ag inks. Finally as a proof of concept, SnAgCu-based solder balls were jetted on top of the UBM pads. In this way, density of I/Os could be increased by four times without making the vias thinner and smaller. Regarding the reliability, electrical testing after up to 1000 temperature cycles (-40 °C to +125 °C) did not show a significant effect on DC resistance of the vias. Shrinkage and delamination of the polymer filling as well as some micro-cracks was seen resulted by temperature cycling stress test, that need to addressed for future refinements.

In conclusion, digital and non-contact fabrication technologies could have good potential to be integrated with the silicon-based electronics for process simplification and cost reduction. However, non-contact and digitally controlled fabrication methods are still in the research and development stage and in order to be used for large volume production still new types of metallic and silicon nanoparticle inks need to be developed. For example, developing silicon inks with good jettability and enough solid content to be used for TSV filling or developing commercial inkjettable Ti inks or other inks that can be used as functional material within the hermetic cavities to control the gas pressure inside the device. Furthermore, better equipment still needs to be developed in the future to meet the requirement of the industry. For instance, different printing technologies could be combined to one machine, capability of handling wafers cassette-to-cassette can be added or nozzles and printhead improvements to be more suitable for large volume production.

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