Tampere University

Dawit Erfo Elcho

MITIGATION OF CURRENT HARMONIC DISTORTION IN THREE-PHASE LCL-TYPE FILTER INTERFACED INVERTERS

Faculty of Computing and Electrical Engineering
Master of Science Thesis
April 2019

ABSTRACT

Dawit Erfo Elcho: Mitigation of current harmonic distortion in three-phase LCL-type filter interfaced inverters
Master of Science Thesis
Tampere University
Power Electronics
April 2019

It is a common practice to use an LCL-filter to attenuate the high-frequency harmonic distortions in grid-connected converters to stay within the limit set by different harmonic limit standards. However, to deal with low-order harmonics, optimal ac current-control techniques are preferred as they are cost-effective solutions. Several previous studies showed that whether LCL-filter is damped actively or passively causes more losses. Moreover, it increases the cost and design complexity of the system since LCL-filter introduces new state variables in the dynamical model compared to simple an L-type filter. Thus, harmonic mitigation under distorted and unbalanced grid conditions in LCL filter interfaced inverters is still an open research topic.

In this thesis, two current-control techniques: proportional-integral (PI) and proportional-resonant (PR) controllers for current-fed passively damped LCL-filter interfaced grid-connected inverter are examined. Inverter-side current-control is adopted in LCL-filter interfaced inverters to have a safe operation. However, the presence of the harmonic distortion in the grid-side cannot be adequately compensated under sever grid conditions. Thus, it is necessary to adopt proportional grid-voltage feedforward in dq-domain and capacitor-current feedforward in $\alpha\beta$-domain to inject pure sinusoidal currents to the grid. Moreover, the conventional synchronous reference frame PLL (SRF-PLL) that generates the angle and frequency for the current controllers lacks the capability to suppress high disturbance under unbalanced and distorted grid voltage conditions. Hence, the scarcity of the SRF-PLL to attenuate disturbances is reduced by introducing a prefiltering stage that utilizes delayed signal cancellation (DSC) techniques.

Based on the techniques mentioned above, the harmonic content of the grid-side current was kept below what standards recommend. The feedforward terms in both domains showed an excellent performance in suppressing the low-order harmonics from the grid-current in distorted grid voltage case. There were also some crucial differences in the performances of the current-control techniques. Enhancements on the quality of the grid current were also made by utilizing $\alpha\beta$CDSC-PLL and dqADSC-PLL in distorted and unbalanced grid voltage conditions, respectively. The operation and performance of the two current-control methods were verified by experimental results from the laboratory test bench at Tampere University Hervanta campus.

Keywords: grid-connected inverter, LCL-filter, control design, PI-control, PR-Control, harmonic compensator, grid-voltage feedforward, capacitor-current feedforward, dqADSC-PLL, $\alpha\beta$CDSC-PLL

TIIVISTELMÄ

Dawit Erfo Elcho: Mitigation of current harmonic distortion in three-phase LCL-type filter interfaced inverters
Diplomi-insinöörin tutkinto
Tampereen yliopisto
Tehoelektroniikka
Huhtikuu 2019

Yleinen käytäntö on käyttää LCL-suodinta lieventamaan harmonisia yliaaltoja verkkoon kytketyissä vaihtosuuntajissa pysyäkseen eri standardien asettamissa rajoissa. Alempien harmonisten yliaaltojen rajaamiseksi voidaan käyttää LCL-suotimen lisäksi kustannustehokkaita aktiivisia virransäätimiä. LCL-suodin tuo uusia tilamuuttujia verrattuna yksinkertaisen L-tyyppisen suotimen dynaamiseen malliin. Tällöin LCL-suotimen harmonisten yliaaltohäiriöiden vähentäminen vääristyneissä tai epätasapainoisissa verkkojännitteen olosuhteissa on edelleen avoin tutkimusaihe.

Tässä työssä tarkastellaan kahta virransäätötapaa verkkoon kytketylle vaihtosuuntaajalle, joilla on rajapintana passiivisesti vaimennettu LCL-suodin: PI-säädintä (engl. proportional-integral controller) sekä PR-säädintä (engl. proportional-resonant controller). Invertteripuolen virransäätö otetaan käyttöön LCL-suotimissa olevissa vaihtosuuntaajassa turvallisen toiminnan varmistamiseksi. Siitä huolimatta, harmonisen yliaallon läsnäoloa ei kuitenkaan voida riittävällä tavalla kompensoida eri verkkojännitteen olosuhteissa. Näin ollen on välttämätöntä ottaa käyttöön verkkojännitteen myötäkytkentä, dq-tasossa ja kondensaattorivirran myötäkytkentä $\alpha\beta$-tasossa, jotta sahkon siirto tapahtuu mahdollisimman tehokkaasti. Lisäksi tavanomainen vaihelukittu silmukalta (engl. phase-locked loop, PLL), joka muodostaa kulman ja taajuuden virransäätimelle, puuttuu kyky pienentää harmonisia yliaaltoja epätasapainoisissa ja vääristyneissä verkkojännitteen olosuhteissa. Siten SRF-PLL:n yliaaltojen vaimentamista voidaan tehostaa ottamalla käyttöön esisuodatusvaihe, jossa käytetään viivästettyjä signaalinpoistomenetelmiä (engl. delayed signal cancellation, DSC).

Edellä mainituilla tekniikoilla onnistuttiin verkkopuolen virran harmoniset yliaaltohäiriöt pitämään vaadittujen standardien sisällä. Tämä diplomityö tuotti tietoa PR- ja PI-säätimien eroista harmonisten häiriöiden vähentämisessä. Molempien virransäätimien myötäkytkentätermit suoriutuivat erinomaisesti häiriökomponenttien alentamisessa verkkovirrasta. Lisäksi virranlaatua pystyttiin parantamaan käyttämällä vaihelukittu silmukoita $\alpha\beta$CDSC-PLL ja dqADSC-PLL. Virransäätimien suorituskyky ja toiminta varmistettiin kokeellisilla testeillä Tampereen yliopiston Hervannan kampuksen laboratoriotestipenkillä.

Avainsanat: verkkoon kytketty invertteri, LCL-suodin, PI-säädin, PR-säädin, yliaaltokompensaattori, verkkojännitteen myötäkytkentä, kondensaattorivirran myötäkytkentä, dqADSC-PLL, $\alpha\beta$CDSC-PLL

PREFACE

This Master of Science thesis was done for the Laboratory of Electrical Energy Engineering at Tampere University (TAU). The examiner of the thesis was Professor Sami Repo.

I would like to thank Assistant Professor Tuomas Messo for offering me this interesting topic from which I learned a lot. A very special thanks for his helpful comments and encouragement during the whole master thesis process. Special thanks belong to him for allowing me to get access to the laboratory and for helping me with measurements.

My special words of gratitude also go to my friends who have shown their interest in my thesis in one way or another and for being a major source of support when I needed the most. Thanks guys for always being there for me.

I am also lucky to say I have a family in Finland. A very special word of thanks goes for Väänänen family, who have been great for me over the years and support me in every form I could ask for. I am also very grateful to Aapo Väänänen for his amazing sense of respect when helping me with the editing of the thesis language.

I acknowledge my deep sense of gratitude to my loving parents, brothers, and sisters back in Ethiopia for being a constant source of inspiration and motivation. This thesis is dedicated to them.

Tampere, 15th April 2019

Dawit Erfo Elcho

CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS AND ABBREVIATIONS

α	Real component in stationary reference frame
β	Imaginary component in stationary reference frame
ω_s	Grid fundamental angular frequency
φ	Angle of a space vector
A	State matrix
AC	Alternating current
B	Input matrix
C	Output matrix
C	Capacitance
C_f	Output-filter capacitance
CB-PWM	Carrier-based pulse-width modulation
CFI	Current-fed inverter
T_C	Clarke transformation matrix
D	Input-output matrix
d	Duty ratio
G_{cLdd-o}	D-channel ol. control-to-inductor-current tf.
G_{cid-o}	D-channel ol. input-to-output tf.
G_{cid-o}	D-channel open-loop (ol.) control-to-input transfer function (tf.)
G_{codq-o}	D-channel to q-channel cross-coupling tf. at open loop
G_{cLdq-o}	D-channel to q-channel ol. control-to-inductor-current tf.
Y_{odd-o}	D-component of inverter output admittance
T_{oid-o}	D-component output-to-input transfer function
d'	Complement of the duty ratio
D_d	Steady-state value of duty ratios direct component
d_d	Direct component of duty ratio
D_q	Steady-state value of duty ratios quadrature component
d_q	Quadrature component of duty ratio
DC	Direct current
G_{ff}	Proportional grid voltage feedforward

i_{L2d}	Grid-side inductor current d-component
I_{L2d}	Grid-side inductor current d-component steady-state value
$i_{L2-i(i=a,b,c)}$	Grid-side inductor current of phase i
i_{L2q}	Grid-side inductor current q-component
I_{L2q}	Grid-side inductor current q-component steady-state value
HC	Harmonic compensator
ICF	Inverter-side current feedback
I	Identity matrix
i_{in}	Input current of the converter
L_{in}	Input-voltage control loop
G_{vc}	Input-voltage controller
G_{cd}	Inverter current controller d-component
G_{cq}	Inverter current controller q-component
I_{L1d}	Inverter-side inductor current 2-component steady-state value
i_{L1d}	Inverter-side inductor current d-component
I_{L1d}	Inverter-side inductor current d-component steady-state value
$i_{L1-i(i=a,b,c)}$	Inverter-side inductor current of phase i
i_{L1q}	Inverter-side inductor current q-component
s	Laplace variable
MIMO	Multiple-input multiple-output
ODE	Ordinary differential equation
G	Open-loop input-to-output transfer function matrix
L_{out}	Output-current control loop
i_{Cf}	Output-filter capacitor current
T_P	Park transformation matrix
PLL	Phase-locked-loop
G_{cLqq-o}	Q-channel ol. control-to-inductor-current tf.
G_{ciq-o}	Q-channel ol. control-to-input tf.
G_{ciq-o}	Q-channel ol. input-to-output tf.
G_{coqd-o}	Q-channel to d-channel cross-coupling tf. at open loop
G_{cLqd-o}	Q-channel to d-channel ol. control-to-inductor-current tf.
Y_{oqq-o}	Q-component of inverter output admittance
T_{oiq-o}	Q-component Output-to-input transfer function

q	Quadrature component of a space-vector transformed variable
SISO	Single-input single-output
SPWM	Sinusoidal pulse-width modulation
T_s	Switching period
THD	Total harmonic distortion
$\boldsymbol{u}$	Vector containing input variables
$\mathbf{U}$	Vector containing Laplace transformed input variables
$\mathbf{Y}$	Vector containing Laplace transformed output variables
$\boldsymbol{y}$	Vector containing output variables
$\boldsymbol{x}$	Vector containing state variables

1 INTRODUCTION

In recent years, there has been an increasing interest in integrating renewable energy sources in power production. The main reason for this unprecedented interest is the rising environmental concerns due to the excessive use of fossil fuels [1, 2]. In addition, the growing world population and the expedition for higher living standards are also some of the main contributors to the search for new solutions [3]. The particular interest has made the research in renewable energy resources grow extensively. One of the research areas has been how these sources are integrated into the grid [4]. The direct connection between renewable sources and the grid requires inverters, which enable the connection to be more reliable by ensuring the power transferred to the grid to a usable form [5, 6].

As the number of grid-connected converters increases, one of the demands present in all grid-connected system standards is the quality of the current fed to the power system [7]. The integration of power electronics come with a price as discussed in [8, 9, 10], harmonic distortion, reduce damping and stability issues in the power system are among the main ones. Thus, the converter should be able to produce sinusoidal currents with low Total Harmonic Distortion (THD) also in the presence of unbalanced and distorted grid voltages. Consequently, there is a growing interest in using an LCL-type filter in grid-connected inverters, which has excellent effectiveness to attenuate higher-order harmonics to meet the international standards and regulations [11].

However, despite the capability of the LCL filter to attenuate high-frequency harmonics, its low-inductance behaviour increases its susceptibility to low-order harmonics in the current produced by the inverter. To deal with the low-order harmonics (5th, 7th, 11th, 13th, etc.), control techniques are preferred, as increasing the inductance leads to an increase in the cost and volume of the LCL filter [12, 13]. For this reason, current-control is recommended in multiple works of literature as part of grid-connected converters. In addition to their capability to mitigate low-order harmonics, current-controlled converters have several advantages such as fast response, better stability and safety as it has been reported in [6]. Out of all the current-control techniques proposed in the literature, this thesis focuses on proportional-integrator (PI) and proportional-resonant (PR)-based control techniques.

In LCL-type filter interfaced grid-connected converters, inverter-current feedback (ICF) control is widely used in industry since it is cost effective and the safest choice from a protection perspective. However, as reported in many works of literature, the dynamics of the inverter becomes complicated, particularly when the uncertain nature of the grid

background distortion and unbalance are considered [14, 15]. Moreover, in inverter-side current control, the inverter performance becomes unsatisfactory at sever grid voltage conditions. Thus, proportional grid-voltage feedforward and capacitor-current feedforward for synchronous and stationary reference frame are required to inject pure sinusoidal currents to the grid, respectively. These feedforward terms are shown to improve the output impedance of the inverter.

Furthermore, the major challenge associated with phase-locked-loop (PLL) is its capability to suppress high disturbance under unbalanced or distorted grid voltage without degrading the dynamical performance of the inverter. To improve the performance of PLLs under adverse grid conditions introducing prefiltering stage into their structures have been proposed in literature [16, 17, 18, 19]. This thesis will evaluate the performance of different PLL thechniques under different grid voltage scenarios in detail together with the current-control techniques as mentioned above already. The proposed PLLs are $\alpha\beta$CDSC-PLL for harmonic distorted grid voltage since it can be tuned to multiple harmonics and dqADSC-PLL for unbalanced grid condition, respectively.

Finally, the operation of the current controllers designed is verified with a test bench in the laboratory of Tampere University at Hervanta campus. The test bench enables to authenticate a three-phase converter model and control of an induction motor. The control techniques are implemented both in dq- and $\alpha\beta$-domains using PI- and PR-based controllers.

The thesis is structured as follows; Chapter 2 presents the background of the thesis, the small-signal model of the inverter topology studied in this thesis is derived. Chapter 3 provides an introduction to the state-of-the-art control techniques in grid-connected converters and the control designs for both dq-domain using PI-controllers and $\alpha\beta$-domain using PR-based controllers. Grid synchronisation methods that generate the accurate phase information of the fundamental component of the grid voltage even under sever grid conditions are presented in Chapter 4. Chapter 5 evaluates the performance of the current-control techniques with simulation and laboratory results. A case study approach was used to allow a comparison between the current-control techniques. The chapter also shows the results obtained from the proposed delayed-signal cancellations compared with the conventional SRF-PLL. Finally, conclusions are drawn in Chapter 6.

2 BACKGROUND OF THE THESIS

This chapter discusses the modeling and analysis of grid-connected converters. The chapter starts by reviewing some of the fundamental concepts that will be used throughout the thesis. Next, the dynamical model of a current-fed inverter with LCL-type filter is derived without the effect of source and load impedance as it is done in literature [20]. The dynamical model is derived in dq-domain where the ac signals are transformed to dc signals exploiting linear current-control techniques discussed in Chapter 3.

2.1 Reference Frame Transformation

While dealing with the modeling and analysis of three-phase systems, it is a common practice to transform all variables from the three-phase system to orthogonal and synchronous reference frames. As it is done in literature [6, 20, 21], we start by introducing a three-phase system with alternating currents. Considering a balanced three-phase voltage source with a resistive-inductive load, the voltage or current waveforms have the same amplitude and frequency in all the three-phase angles. Yet, their phases are rotated by $2\pi/3$ with respect to each other.

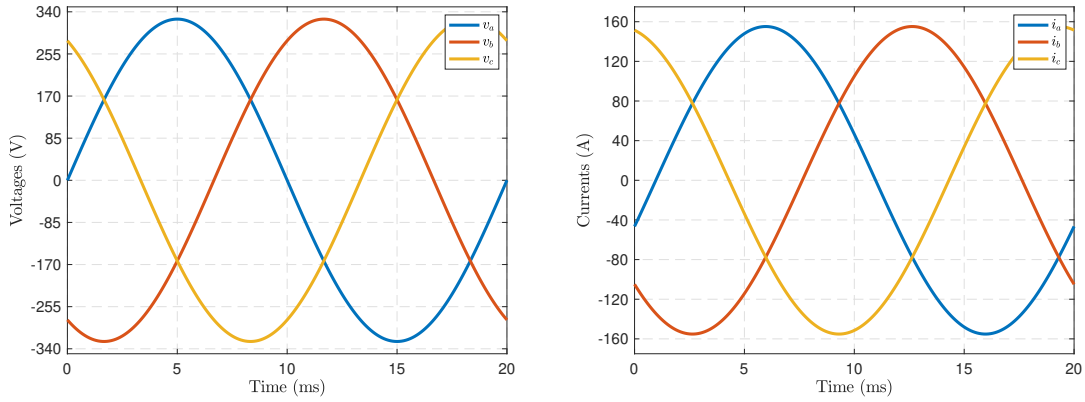


Figure 2.1. *Balanced three-phase voltages and currents.*

Fig. 2.1 shows the waveforms of three-phase voltages and currents. The amplitude and the angle difference between the phase voltages and their corresponding phase currents are due to the load impedance connected to the voltage source, which in this case was $Z = R + j\omega L$ with $R = 2\Omega$ and $L = 2mH$, correspondingly.

2.1.1 Stationary and Synchronous Reference Frames

A balanced three-phase system is mapped to a stationary orthogonal reference frame ($\alpha\beta$-domain) or vice versa using Clarke's transformation matrices given below

$$\boldsymbol{T}_C = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \qquad \boldsymbol{T}_C^{-1} = \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix}. \tag{2.1}$$

When transforming three-phase quantities into the stationary orthogonal reference frame, we often require only the α- and β-components. The 0-component is negligible in symmetrical ideal grid condition. However, in unbalanced condition, the three-phase system and the results obtained by using this transformation must be regarded critically. The three-phase system presented in Fig. 2.1 is mapped in stationary orthogonal reference frame in Fig. 2.2.

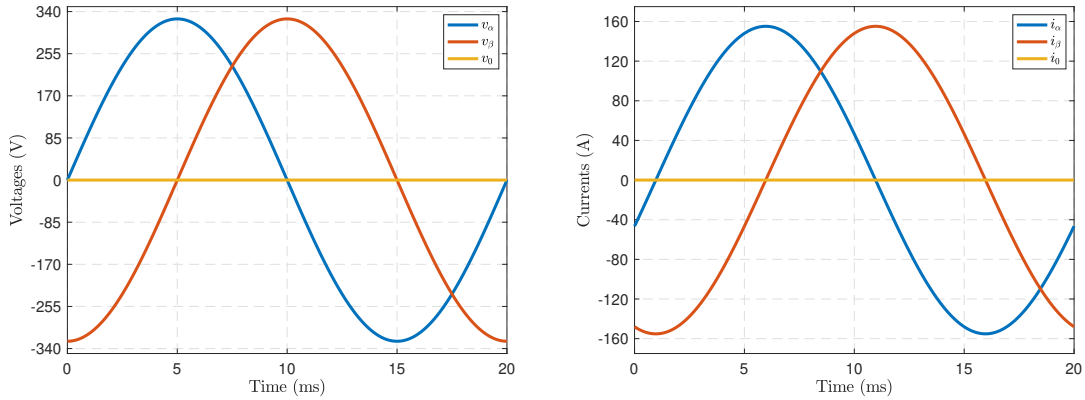


Figure 2.2. *Balanced three-phase voltages and currents in stationary $\alpha\beta 0$ reference frame.*

Furthermore, the so-called Park transformation transforms the three-phase system to a rotating reference frame (dq-domain), and vice versa using the following matrices

$$\begin{aligned} \boldsymbol{T}_P &= \frac{2}{3}\begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi)}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \\ \boldsymbol{T}_P^{-1} &= \begin{bmatrix} \cos\theta & -\sin\theta & 1 \\ \cos\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ \cos\left(\theta + \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) & 1 \end{bmatrix}. \end{aligned} \tag{2.2}$$

In synchronous reference frame the three-phase variables become constant in a steady-state as shown in Fig. 2.3. This enables the use of conventional PI-controllers.

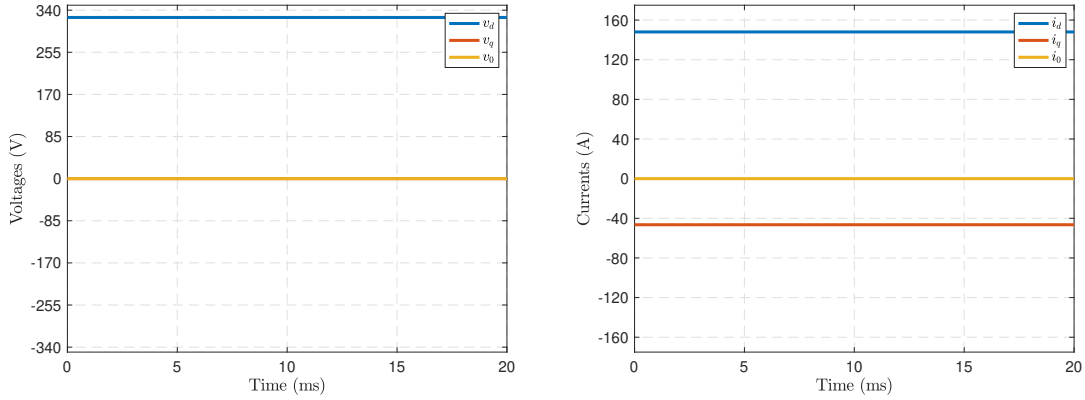


Figure 2.3. *Balanced three-phase voltages and currents in rotating $dq0$ reference frame.*

2.1.2 State-space Vector

A state-space vector is introduced to alleviate the understanding of stationary and synchronous reference frames. A space vector is a representation of a three-phase instantaneous quantity in the complex plane with real and imaginary components. Fig. 2.4 shows how a three-phase system is mapped to the $\alpha\beta$-reference frame and further rotated with a speed ω_s to obtain the dq-reference frame.

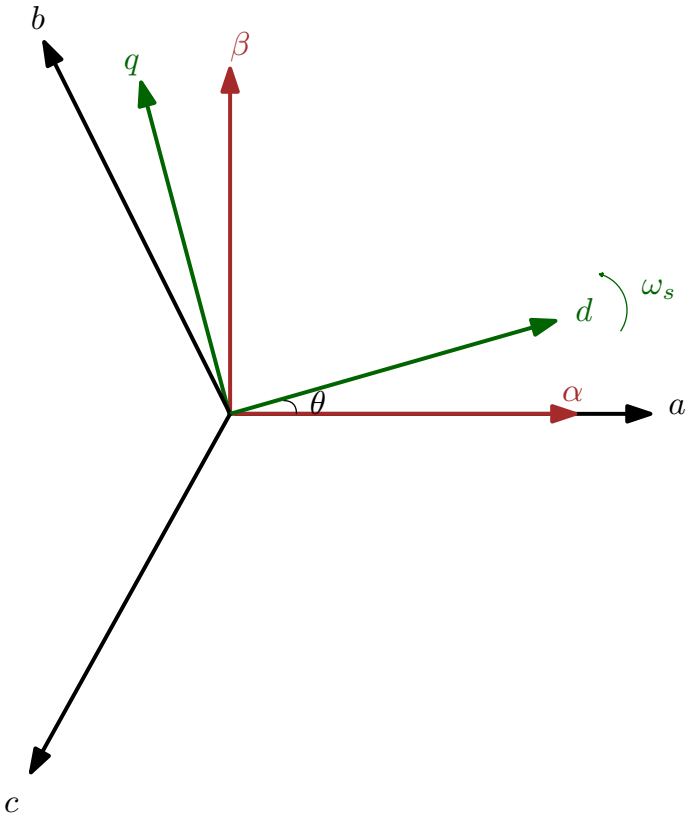


Figure 2.4. *Stationary $\alpha\beta$ frame and rotating dq frame.*

Using $Fortescue$ operator space vector is defined as

$$\begin{aligned} \boldsymbol{x}^{\alpha\beta}(t) = x_\alpha(t) + jx_\beta(t) = \frac{2}{3}(x_a(t) + x_b(t)a + x_c(t)a^2) \\ x_0 = \frac{x_a(t) + x_b(t) + x_c(t)}{3} \end{aligned} \tag{2.3}$$

where a and a^2 are equivalent to unity vectors displaced by $2\pi/3$. The α- and β-components of the space vector are expressed as a function of a-, b- and c-components as it is done in stationary orthogonal reference frame transformation. Further, multiplying the space vector by $e^{-j\omega_s t}$ transforms it from the stationary complex plane to a rotating complex plane. The latter is equivalent to the dq-reference frame.

$$\begin{aligned} \boldsymbol{x}^{dq} = \boldsymbol{x}^{\alpha\beta} e^{-j\omega_s t} \\ x^0 = \frac{1}{3}(x_a + x_b + x_c) \end{aligned} \tag{2.4}$$

which can be given in matrix form and its inverse as follows:

$$\boldsymbol{x}^{dq} = \begin{bmatrix} \cos\theta & \sin\theta & 0 \\ -\sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix} \boldsymbol{x}^{\alpha\beta} \qquad \boldsymbol{x}^{\alpha\beta} = \begin{bmatrix} \cos\theta & -\sin\theta & 0 \\ \sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix} \boldsymbol{x}^{dq}. \tag{2.5}$$

In symmetrical and ideal grid condition the zero sequence component is negligible [26]. Thus, it is not taken it account.

2.2 Case Study

The utilization of electronic converters as an interface to power sources, energy storages, and power consumers has increased extensively [4, 6]. These applications include power systems where renewable energy sources like wind and solar power sources are integrated with storage elements. Moreover, ac motors that need to be controlled accurately like in industries, ships, electric vehicles integrated to utility grid are also some of the applications.

In this section, the state space model of a grid-connected converter is derived. The dynamical model of a linear system that needs to be controlled can be derived by ordinary differential equations (ODEs) of the states, inputs, and outputs. The dynamical model of the systems can be represented by state-space representation as follows

$$\begin{aligned} \frac{d\boldsymbol{x}}{dt} = \boldsymbol{Ax} + \boldsymbol{Bu} \\ \boldsymbol{y} = \boldsymbol{Cx} + \boldsymbol{Dx} \end{aligned} \tag{2.6}$$

where $\boldsymbol{x}$, $\boldsymbol{u}$ and $\boldsymbol{y}$ are the state, input and output space vectors, respectively. Furthermore, the **A**, **B**, **C** and **D** are the state, input, output and input-output matrices, respectively.

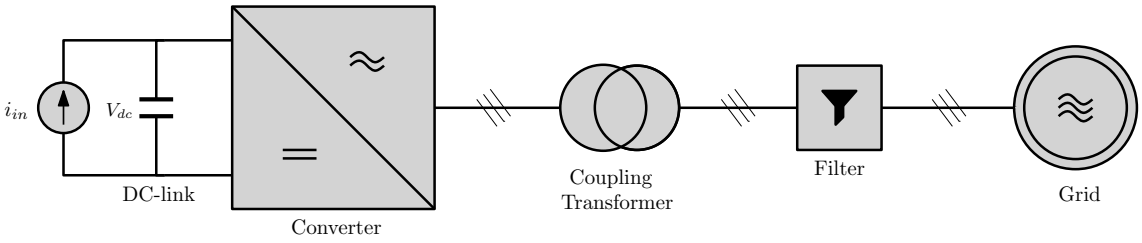


Figure 2.5. *Grid-connected converter system.*

Fig. 2.5 shows a grid-connected converter system. As depicted, it consists of a power supply, dc-link, converter, an optional coupling transformer, a filter, and a grid. The power supply denoted by i_{in} can be for instance renewable energy sources, such as photovoltaic (PV) power source. The dc-link operates as storage to maintain a constant dc-side voltage. The converter is used to convert the dc input to ac output or vice versa. The coupling transformer is used to step-down the voltage fed from the grid to the converter. However, in this thesis, the transformer is neglected as the focus is on the low voltage grid. The filter is used to attenuate the frequency components in the grid currents which are generated by the high-frequency switching of the converter.

2.2.1 Power Stage of CFI with LCL-type Filter

The power stage is depicted in Fig. 2.6. The converter topology is used in low voltage systems due to its price, low switching losses, and controllability. The power stage is fed from a current source. This is typical for instance in photovoltaic systems, where irradiance induces constant direct current [20].

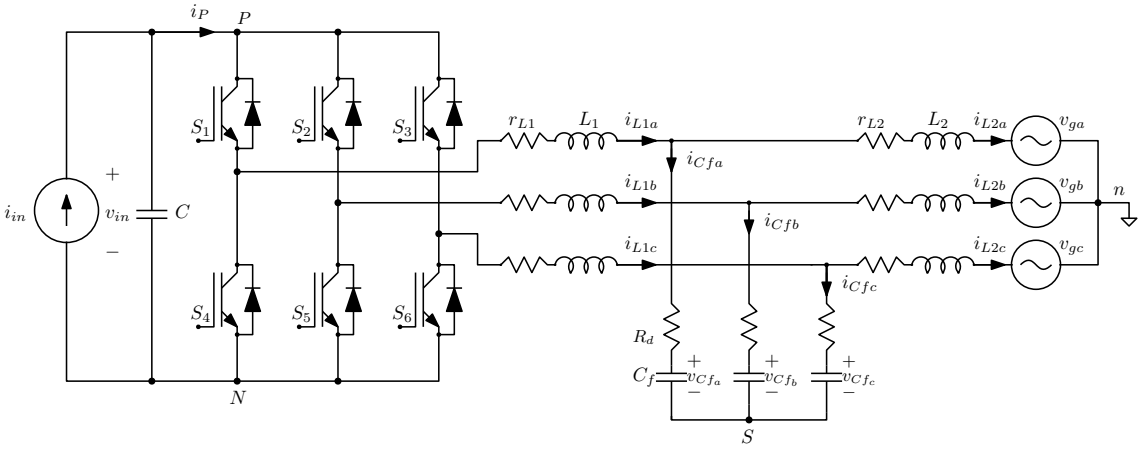


Figure 2.6. *Current-fed inverter with LCL-type filter.*

It was pointed in [2, 22] that the input source type (i.e., voltage or current) defines the dynamics of a converter. Thus, the true nature of the source needs to be taken into account. In a three-phase inverter used in interfacing PV power sources, the maximum power from the inverter is extracted by controlling the input-voltage, which is why a current-fed topol-

ogy utilized rather than voltage-fed topology. Furthermore, according to control theory, only output can be controlled and in CF inverter the output is the input-voltage, i.e., dc-voltage.

Furthermore, the power stage has an input capacitor that enables control over the dc-side voltage. The inverter has six controllable switches and the continuity of the dc current is guaranteed by adding dead-time at the switching instants. In real time applications, this makes sure the upper and lower switches at each phase are not conducting simultaneously. Thus, current flows through the anti-parallel diode.

As it is discussed in literature [12, 23], in high power applications L-type filter may not be the best choice as it can not effectively attenuate the harmonic components produced by the converter. Moreover, higher values of inductance required when they are used, but they come at the expense of filter price and degrading the dynamical response of the converter. Consequently, LCL-filter type filters are preferred since they enable higher power range with low inductance and capacitance values. The only constraint is the design complexity they add to the system. In order to avoid resonance problem induced by the LCL-type filter, the power stage utilizes a passive damping method as it easy to implement. This is realized by connecting a series resistors with the ac side capacitors (i.e., filter capacitor) as it is proposed in [12, 20]. The parasitic resistances of the filter capacitor can also be added to these damping resistors.

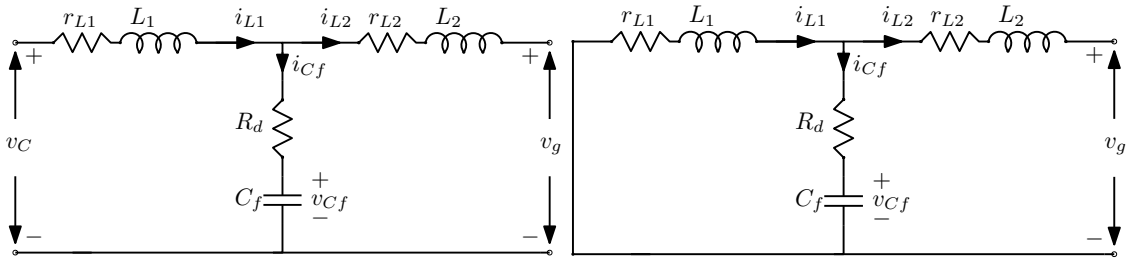
2.2.2 Average State-space Model

Dynamic modeling of a three-phase inverter with LCL-type filter has been previously reported in numerous literature works such as [4, 20, 24, 25]. The average model is used in most control strategies of grid-connected converters to neglect the switching behavior of the semiconductor switches. Subsequently, a modulation stage is required to generate the switching signals applied to the switches. The most frequently used modulation scheme and the one used in this thesis is discussed further in the next chapter.

Regarding the CFI shown in Fig. 2.6, the system inputs are the input current i_{in} and the grid voltage $\boldsymbol{v}_{g,abc}$. Thus, the outputs are the Input-voltage v_{in} and the grid current $\boldsymbol{i}_{L2,abc}$. The inverter-side inductor current $\boldsymbol{i}_{L1,abc}$ is also selected as the controlled output. The state variables are the phase inductor currents $\boldsymbol{i}_{L1,abc}$, $\boldsymbol{i}_{L2,abc}$ and Input-voltage v_{in}.

When phase leg is connected to the P- or N-terminal, the equivalent circuits are depicted in Fig. 2.7. Notice that the on-time resistances caused by the transistors of the inverter are neglected for simplicity. Afterward, the corresponding equations using Kirchhoff's circuit laws are derived respectively.

From the equivalent circuits the inductor voltages and capacitor currents, when the P-



(a) *P-terminal conducting.* ***(b)*** *N-terminal conducting.*

Figure 2.7. *Equivalent circuits of grid-connected converter with LCL filter.*

terminal is conducting as shown in Fig. 2.7a are given as

$$\begin{aligned} v_{L1} &= v_C - r_{L1}i_{L1} - R_d i_{Cf} - v_{Cf} - v_{SN} \\ v_{L2} &= v_{Cf} - R_d i_{Cf} - r_{L2}i_{L2} + v_g - v_{nS} \\ i_{Cf} &= i_{L1} - i_{L2} \\ v_{in} &= v_C \\ i_o &= i_{L2} \end{aligned} \tag{2.7}$$

where v_{SN} and v_{nS} are the common-mode voltages. Similarly, when the phase-leg is connected to the N-termminal as shown in Fig. 2.7b, the corresponding equations are given as

$$\begin{aligned} v_{L1} &= -r_{L1}i_{L1} - R_d i_{Cf} - v_{Cf} - v_{SN} \\ v_{L2} &= v_{Cf} + R_d i_{Cf} - r_{L2}i_{L2} + v_g - v_{nS} \\ i_{Cf} &= i_{L1} - i_{L2} \\ v_{in} &= v_C \\ i_o &= i_{L2}. \end{aligned} \tag{2.8}$$

Because all the phases are assumed to be symmetrical, for arbitrary phase i, substituting the capacitor currents and multiplying the inductor voltages equation (2.7) with the duty ratio d and the ones in equation (2.8) with the complementary duty ratio d' gives the average inductor voltages. Further dividing with their respective inductor values gives

$$\frac{d}{dt}\langle i_{L1-i}\rangle = \frac{1}{L_1}\left[d_i\langle v_C\rangle - (r_{L1}+R_d)\langle i_{L1-i}\rangle + R_d\langle i_{L2-i}\rangle - \langle v_{Cf-i}\rangle - \langle v_{SN}\rangle\right] \tag{2.9}$$

$$\frac{d}{dt}\langle i_{L2-i}\rangle = \frac{1}{L_{2-i}}\left[\langle v_{Cf-i}\rangle + R_d\langle i_{L1-i}\rangle - (r_{L2}+R_d)\langle i_{L2-i}\rangle - \langle v_{g-i}\rangle - \langle v_{nS}\rangle\right] \tag{2.10}$$

where r_{L1} and r_{L2} are fro inductor parasitic resistances and R_d denotes damping resistance . Further, the average capacitor voltage can be given as

$$\frac{d}{dt}\langle v_C\rangle = \frac{1}{C}\left[\langle i_{in}\rangle - d_A\langle i_{La}\rangle - d_B\langle i_{Lb}\rangle - d_C\langle i_{Lc}\rangle\right]. \tag{2.11}$$

Furthermore, the filter capacitor average voltage for phase i is given as follows

$$\frac{d}{dt}\langle v_{Cf-i}\rangle = \frac{1}{C_f}\left[\langle i_{L1-i}\rangle - \langle i_{L2-i}\rangle\right]. \tag{2.12}$$

The averages of the outputs are given as

$$\langle v_{in}\rangle = \langle v_C\rangle \tag{2.13}$$

$$\langle i_{o-i}\rangle = \langle i_{L2-i}\rangle. \tag{2.14}$$

Utilizing the space vector introduced in equations (2.3) and (2.22) we can express the average state space model presented in equations (2.9-2.14) in dq-domain as

$$\begin{aligned}\frac{d}{dt}\langle i_{L1d}\rangle &= \frac{1}{L_1}\left[d_d\langle v_C\rangle - (r_{L1}+R_d)\langle i_{L1d}\rangle + \omega_s L_1\langle i_{L1q}\rangle + R_d\langle i_{L2d}\rangle - \langle v_{Cfd}\rangle\right]\\ \frac{d}{dt}\langle i_{L1q}\rangle &= \frac{1}{L_1}\left[d_q\langle v_C\rangle - (r_{L1}+R_d)\langle i_{L1q}\rangle - \omega_s L_1\langle i_{L1d}\rangle + R_d\langle i_{L2q}\rangle - \langle v_{Cfq}\rangle\right]\end{aligned} \tag{2.15}$$

$$\begin{aligned}\frac{d}{dt}\langle i_{L2d}\rangle &= \frac{1}{L_2}\left[\langle v_{Cfd}\rangle + R_d\langle i_{L1d}\rangle - (r_{L2}+R_d)\langle i_{L2d}\rangle + \omega_s L_2\langle i_{L2q}\rangle - \langle v_{gd}\rangle\right]\\ \frac{d}{dt}\langle i_{L2d}\rangle &= \frac{1}{L_2}\left[\langle v_{Cfq}\rangle + R_d\langle i_{L1q}\rangle - (r_{L2}+R_d)\langle i_{L2q}\rangle - \omega_s L_2\langle i_{L2d}\rangle - \langle v_{gq}\rangle\right]\end{aligned} \tag{2.16}$$

$$\begin{aligned}\frac{d}{dt}\langle v_{Cfd}\rangle &= \frac{1}{C_f}\left[\langle i_{L1d}\rangle - \langle i_{L2d}\rangle + \omega_s C_f\langle v_{Cfq}\rangle\right]\\ \frac{d}{dt}\langle v_{Cfq}\rangle &= \frac{1}{C_f}\left[\langle i_{L1q}\rangle - \langle i_{L2q}\rangle - \omega_s C_f\langle v_{Cfd}\rangle\right]\end{aligned} \tag{2.17}$$

$$\frac{d}{dt}\langle v_C\rangle = \frac{1}{C}\Big(\langle i_{in}\rangle - \frac{3}{2}(d_d\langle i_{L1da}\rangle + d_q\langle i_{L1q}\rangle\Big) \tag{2.18}$$

$$\langle v_{in}\rangle = \langle v_C\rangle \tag{2.19}$$

$$\begin{aligned}\langle i_{od}\rangle &= \langle i_{L2d}\rangle\\ \langle i_{oq}\rangle &= \langle i_{L2q}\rangle.\end{aligned} \tag{2.20}$$

The steady-state operating point can be solved from equations (2.15 -2.20) by letting the derivatives to be zero and replacing the lowercase average values with their corresponding uppercase steady-state values. It is utterly time-consuming to solve all operating points symbolically [20]. Thus, MATLAB with Symbolic Toolbox is used to obtain numerical values. A MATLAB-code used to calculate the steady-state values with all the parasitics losses is given in Appendix A.

However, in order to solve the steady-state values symbolically all the resistive losses are neglected. Moreover, the inductor current at grid side is assumed to be synchronized to

the grid voltage ($V_{gq} = 0$) and the inverter is assumed to operate at unity-factor which leads to ($I_{L2q} = 0$). All these procedures yield the following simplification

$$D_d = \frac{(1 - \omega_s^2 L_1 C_f) V_{gd}}{V_{in}} \tag{2.21}$$

$$D_q = \frac{2(1 - (1 - \omega_s^2 L_2 C_f)(1 - \omega_s^2 L_1 C_f)) I_{in}}{3\omega_s C_f V_{gd}} \tag{2.22}$$

$$I_{L1d} = \frac{2}{3D_d} I_{in} - \frac{D_q}{D_d} \omega_s C_f V_{gd}, \quad I_{L1q} = \omega_s C_f V_{gd} \tag{2.23}$$

$$I_{L2d} = \frac{1}{\omega_s^2 C_f L_2} I_{L1d} \tag{2.24}$$

$$V_{Cfd} = \frac{1}{\omega_s C_f} I_{L1q}, \quad V_{Cfq} = \frac{I_{L2d} - I_{L1d}}{\omega_s C_f}, \quad V_C = V_{in}. \tag{2.25}$$

2.2.3 Linearized State-space Model

In order to express the average state-space mode to a linearized model, we need to linearize the nonlinear system at the operating points defined in equations (2.21-2.25) using first-order approximation of the Taylor-series.

After obtaining the linearized-state space model in synchronous reference frame, the dynamical model is expressed by ODEs presented in equation (2.6), where the states, the inputs, and the outputs are the followings

$$\begin{aligned} \boldsymbol{x} &= \begin{bmatrix} \hat{i}_{L1d} & \hat{i}_{L1q} & \hat{i}_{L2d} & \hat{i}_{L2q} & \hat{v}_{Cfd} & \hat{v}_{Cfq} & \hat{v}_C \end{bmatrix}^T \\ \boldsymbol{u} &= \begin{bmatrix} \hat{i}_{in} & \hat{v}_{gd} & \hat{v}_{gq} & \hat{d}_d & \hat{d}_q \end{bmatrix}^T \\ \boldsymbol{y} &= \begin{bmatrix} \hat{v}_{in} & \hat{i}_{L1d} & \hat{i}_{L1q} & \hat{i}_{L2d} & \hat{i}_{L2q} \end{bmatrix}^T \end{aligned} \tag{2.26}$$

and the state $\boldsymbol{A}$, input $\boldsymbol{B}$, output $\boldsymbol{C}$ and input-output $\boldsymbol{D}$ matrices are defined as

$$\boldsymbol{A} = \begin{bmatrix} -\frac{r_{L1}+R_d}{L_1} & \omega_s & \frac{R_d}{L_1} & 0 & -\frac{1}{L_1} & 0 & \frac{D_d}{L_1} \\ -\omega_s & -\frac{r_{L1}+R_d}{L_1} & 0 & \frac{R_d}{L_1} & 0 & -\frac{1}{L_1} & \frac{D_q}{L_1} \\ \frac{R_d}{L_2} & 0 & -\frac{r_{L2}+R_d}{L_2} & \omega_s & \frac{1}{L_2} & 0 & 0 \\ 0 & \frac{R_d}{L_2} & -\omega_s & -\frac{r_{L2}+R_d}{L_2} & 0 & \frac{1}{L_2} & 0 \\ \frac{1}{C_f} & 0 & -\frac{1}{C_f} & 0 & 0 & \omega_s & 0 \\ 0 & \frac{1}{C_f} & 0 & -\frac{1}{C_f} & -\omega_s & 0 & 0 \\ -\frac{3D_d}{2C} & -\frac{3D_q}{2C} & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{2.27}$$

$$\boldsymbol{B} = \begin{bmatrix} 0 & 0 & 0 & \frac{V_{in}}{L_1} & 0 \\ 0 & 0 & 0 & 0 & \frac{V_{in}}{L_1} \\ 0 & -\frac{1}{L_2} & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{L_2} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C} & 0 & 0 & -\frac{3I_{L1d}}{2C} & -\frac{3I_{L1q}}{2C} \end{bmatrix} \tag{2.28}$$

$$\boldsymbol{C} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 \end{bmatrix} \tag{2.29}$$

$$\boldsymbol{D} = [\boldsymbol{0}_{5X5}]. \tag{2.30}$$

The linearized state-space is further transformed into frequency-domain by Laplace transformation. Consequently, performance specifications and sensitivities of the system are easier to investigate since time-domain makes it very complex exploiting theses features.

$$\begin{aligned} s\boldsymbol{X}(s) &= \boldsymbol{A}\boldsymbol{X}(s) + \boldsymbol{B}\boldsymbol{U}(s) \\ \boldsymbol{Y}(s) &= \boldsymbol{C}\boldsymbol{X}(s) + \boldsymbol{D}\boldsymbol{U}(s) \end{aligned} \tag{2.31}$$

Manipulating the linearized state-pace model gives the transfer function between the input and output

$$\boldsymbol{Y}(s) = [\boldsymbol{C}(s\boldsymbol{I} - \boldsymbol{A})^{-1}\boldsymbol{B} + \boldsymbol{D}]\boldsymbol{U}(s) = \boldsymbol{G}\boldsymbol{U}(s). \tag{2.32}$$

The resulted open-loop input-to-output transfer function is presented in matrix form as

$$\begin{bmatrix} \hat{v}_{in} \\ \hat{i}_{L1d} \\ \hat{i}_{L1q} \\ \hat{i}_{L2d} \\ \hat{i}_{L2q} \end{bmatrix} = \begin{bmatrix} Z_{in-o} & T_{oid-o} & T_{oiq-o} & G_{cid-o} & G_{ciq-o} \\ G_{iLd-o} & T_{oLdd-o} & T_{oLqd-o} & G_{cLdd-o} & G_{cLqd-o} \\ G_{iLq-o} & T_{oLdq-o} & T_{oLqq-o} & G_{cLdq-o} & G_{cLqq-o} \\ G_{iod-o} & -Y_{odd-o} & -Y_{oqd-o} & G_{codd-o} & G_{coqd-o} \\ G_{ioq-o} & -Y_{odq-o} & -Y_{oqq-o} & G_{codq-o} & G_{coqq-o} \end{bmatrix} \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_{gd} \\ \hat{v}_{gq} \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix} \tag{2.33}$$

where the *G*, *T*, *Y*, and *Z*, denote the transfer functions between the input and output variables. Furthermore, -o denotes the transfer functions being open-loop functions. The presented transfer function matrix is modified as the actual current flows out of the inverter, thus the admittances Y_{odd-o}, Y_{oqd-o}, Y_{odq-o} and Y_{oqq-o} have to be multiplied by -1.

A it is discussed in [26], the open-loop input-to-output transfer function in 2.33 can be simplified and provided as transfer matrices due to the inherent multivariable nature of the inverter

$$\begin{bmatrix} \hat{\boldsymbol{v}}_{in} \\ \hat{\boldsymbol{i}}_{L1} \\ \hat{\boldsymbol{i}}_{L2} \end{bmatrix} = \begin{bmatrix} Z_{in-o} & \boldsymbol{T}_{oi-o} & \boldsymbol{G}_{ci-o} \\ \boldsymbol{G}_{iL-o} & \boldsymbol{T}_{oL-o} & \boldsymbol{G}_{cL-o} \\ \boldsymbol{G}_{io-o} & -\boldsymbol{Y}_{o-o} & \boldsymbol{G}_{co-o} \end{bmatrix} \begin{bmatrix} \hat{\boldsymbol{i}}_{in} \\ \hat{\boldsymbol{v}}_{g} \\ \hat{\boldsymbol{d}} \end{bmatrix} \tag{2.34}$$

where all the transfer functions are 2x2 matrices.

System control design and analysis are operated using the transfer functions given in (2.33) for the reason that the inverter is seen as multiple-input multiple-output (MIMO) system. Note that the input voltage $\hat{v}_{in}$ and the input current $\hat{i}_{in}$ are scalar variables, hence, the input impedance Z_{in-o} in (2.34) is also a scalar.

3 CURRENT CONTROL TECHNIQUES

This chapter provides an introduction to the state-of-the-art control techniques in grid-connected converters. The control structure and most frequently used modulation scheme are presented first. Next, the two control schemes that are commonly used in grid-connected converters are studied; these control schemes are proportional-integral (PI) control and proportional-resonant (PR) control.

3.1 Control Structures and Modulation Scheme

One of the demands present in grid-connected systems is the quality of the current-fed to the power system. Over the last few decades, a considerable amount of research has been done to meet standards used in grid-tied systems like IEC61727 in Europe and IEEE-1547 in the USA [6, 27]. For any distributed source, the amount of harmonics in the current fed to the grid should not exceed limits imposed by these utility standards.

In grid-connected converters, current-control is an essential part of the converters [7, 27]. Current-controlled converters have several advantages: they provide fast response, better stability and safety. This chapter will present two of the main current-control techniques used widely in the industry. Among the existing current-control techniques presented in [7, 27, 28], this thesis will investigate the linear current controllers in dq-domain proportional-integral (PI) and $\alpha\beta$-domain proportional-resonant (PR) current controllers.

The thesis does not engage with a model predictive control (MPC) although its getting popularity nowadays. Despite the ability of the MPC to track precise reference tracking, the control technique is overburdened by the complex computational requirements [29, 30].

3.1.1 Harmonic Emission

In ideal network the voltage and current oscillate with a fundamental frequency of 50 or 60 Hz. The grid voltage and the current flowing between the grid and the device connected to it are both sinusoidal and in the same phase with each other. In such situations, the load is purely resistive. However, in real life, the voltage and current waveforms are distorted. Which means they contain other frequencies that are multiples of the fundamental

frequency. Thus, the waveforms are not pure sinusoidal anymore. Fig. 3.1 presents a distorted signal which consists of the fundamental frequency along with the 5th and 7th harmonic components.

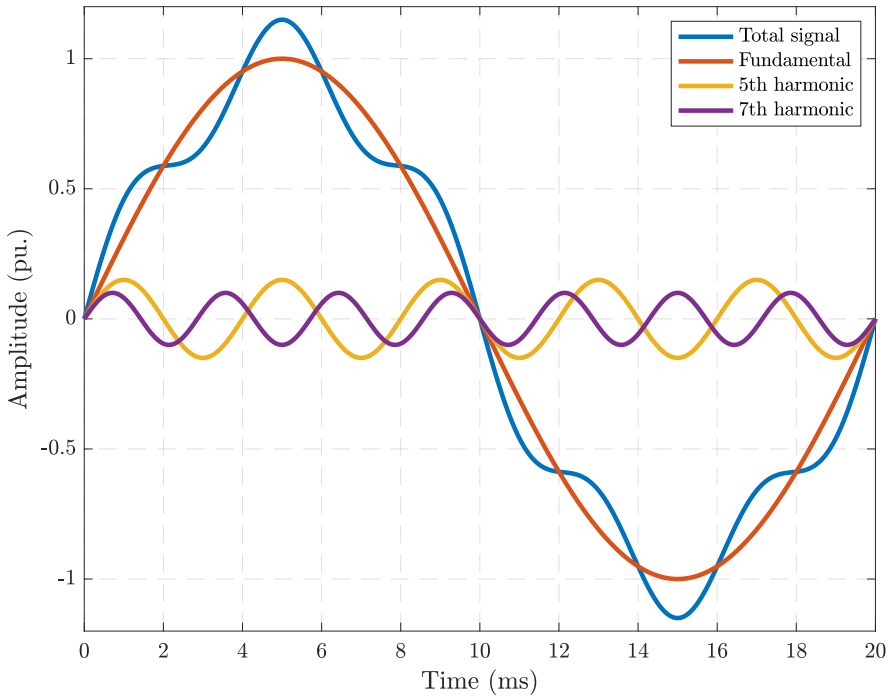


Figure 3.1. *Distorted signal divided into its harmonic components*

In grid-connected converters, the sources of harmonic currents are three-phase power converters utilized. It is a common practice to specify the harmonic content injected by these converters at the point of common coupling (PCC). At this point, the system output should less affected from harmonic distortions and not recommended to exceed certain harmonic levels. This ensures that no adverse effects are caused to other equipment connected to the utility system. According to [31, 32], the total harmonic current distortion recommended in IEEE Std 519-1992 shall be less than 5% and each harmonic shall be limited to the percentages listed in Table 3.1. The limits are for six-pulse converter as they

Table 3.1. *Current distortion limits at PCC.*

Harmonic Order	Distortion limits %
$3^{rd} - 9^{th}$	< 4
$11^{th} - 15^{th}$	< 2
$17^{th} - 21^{th}$	< 1.5
$23^{th} - 33^{th}$	< 0.6
Above 33^{rd}	< 0.3

are the most common grid-connected converters. IEEE Std 519-1992 gives a conversion formula for converters with pulse numbers greater than six.

3.1.2 Control Structure

Fig. 3.2 shows the control structure of an inverter with a grid-side filter. The controller maintains the dc-link voltage at its reference value using a cascaded control loop. As it is visualized in the figure, the outer-loop maintains the dc-link voltage by regulating the reference for the inner loop controller, which is the current controller. The inner-loop regulates the grid currents by manipulating the voltage applied to the grid by the converter.

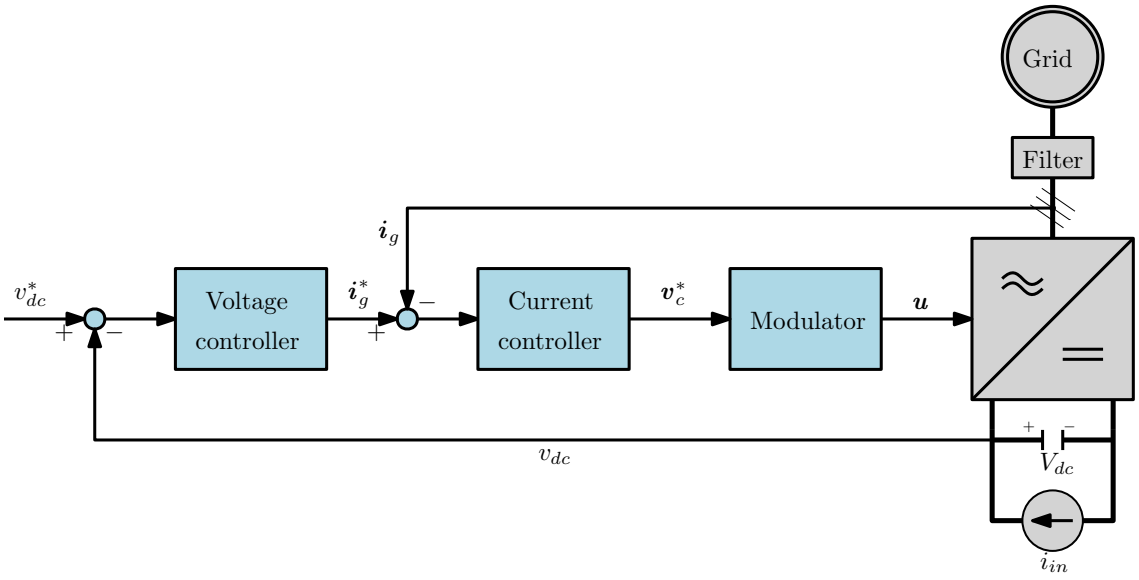


Figure 3.2. *Cascaded control structure of grid-tied converter.*

In synchronous reference frame, the current controller becomes a MIMO problem. Thus, the control system consists of two PI-controllers one for the d and the other for the q-component of the current, whereas in $\alpha\beta$-domain PR-controllers can be used to regulate the inverter currents. In cascade structure, the inner control loop has to be faster. Otherwise, the controller will not be able to follow the reference generated by the outer control-loop. As it can be seen from the figure, the inverter-side output-current is usually controlled instead of the grid-side current in order to limit the inverter current within safety limits.

In the controller structure, modulation is used to translate the voltage obtained from the inner control-loop to switching signals that are applied to the semiconductor switches of the converter. In the next subsection is explained briefly the most frequently used modulation scheme.

3.1.3 Carrier-Based pulse-width Modulation

In power electronic converters, the amplitude and frequency of electrical signals are transformed from one form to the other using semiconductor-based switches, i.e., modulation. However, the on and off nature of these switches create harmonic components that need to be minimized. Thanks to the semiconductor technology, switches with high frequency, less distortion and losses are on the market [33].

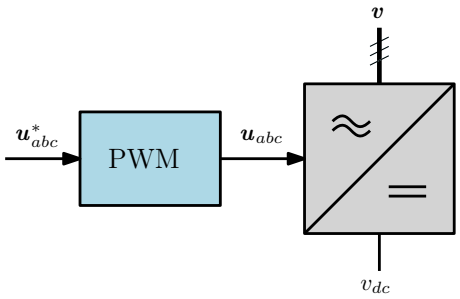


Figure 3.3. *Carrier-based pulse-width modulation.*

There are different modulation techniques, but this thesis focuses on CB-PWM as it will be used in the simulation model later on. In CB-PWM the reference sinusoidal voltage signals are compared with triangular carrier signals which have a switching frequency of the semiconductor switches of the converter. Subsequently, the generated pulses are applied to the switches of the converters. This is shown in Fig. 3.3 for a three-phase CB-PWM. The reference signal generated by the controller is scaled to a modulating signal $\boldsymbol{u}^*_{abc}$ which amplitude is equivalent to the modulation index. The modulating signal

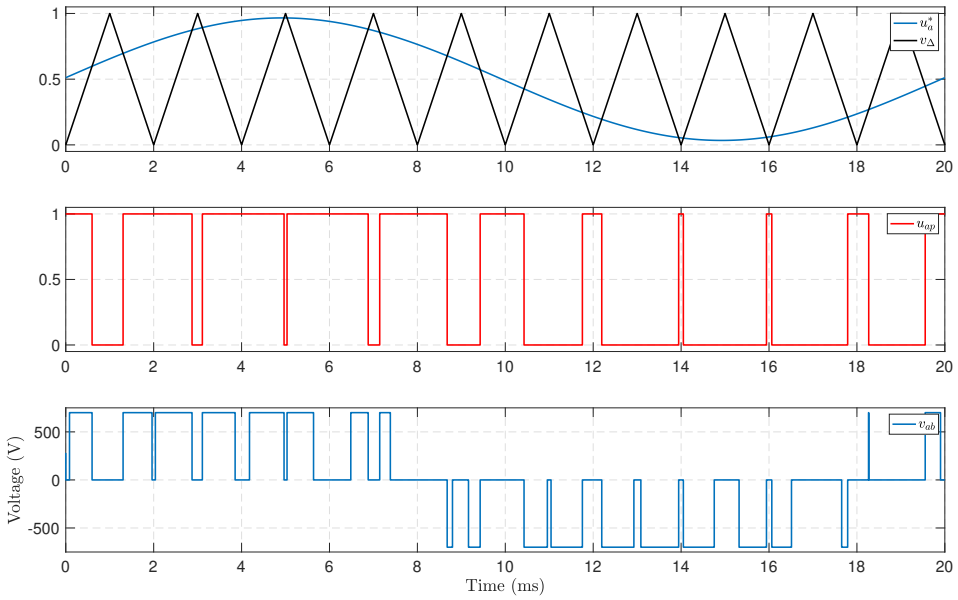


Figure 3.4. *Carrier-based pulse-width modulation operating principle.*

is further translated to switching signals $\boldsymbol{u}_{abc}$ that are then applied to the switchings of the

converter. Moreover, since the modulating signal is sinusoidal the modulation technique is also referred as sinusoidal PWM (SPWM).

A carrier signal has significantly higher frequency than the fundamental frequency. In Fig. 3.3 is shown the operation principle of a CB-PWM with a carrier frequency of 250 Hz. The figure visualizes a CB-PWM for a positive half cycle, which can also be further extended for all the three-phase legs. The reference signal u_a^* and carrier signal u_Δ are displayed in the same figure.

The next two subfigures illustrate the generated switching signal u_{ap} for the positive half cycle and line-to-line voltage (v_{ab}), respectively. The use of PWM introduces excessive- and inter-harmonics as shown in Fig. 3.5. These harmonic components need to be filtered out before they are fed to the grid to meet the different standards related to grid-tied systems [6, 27]. In Fig. 3.5 is depicted as the frequency component of the generated phase voltage v_a, when a 250 Hz carrier frequency is utilized.

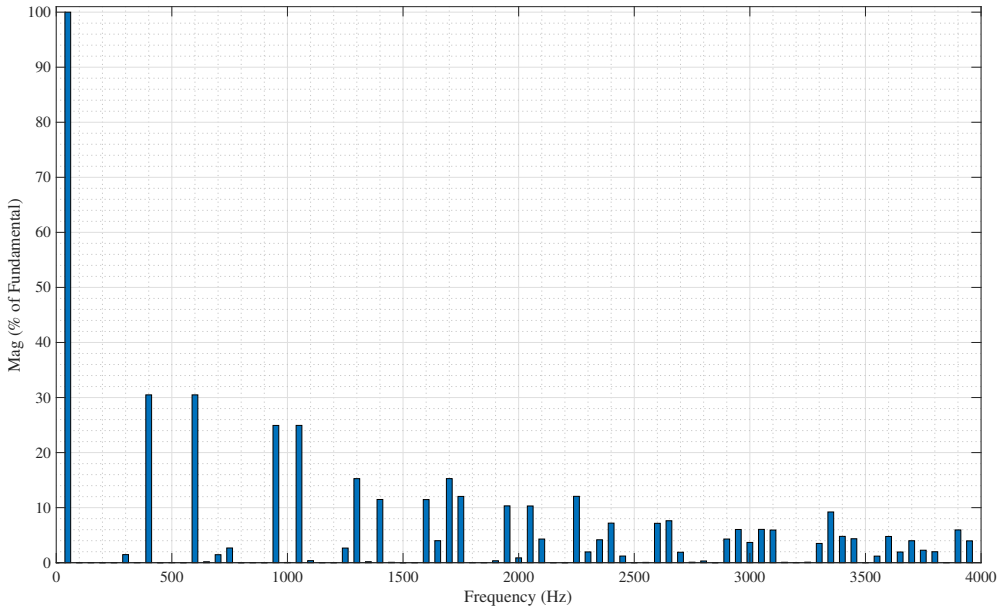


Figure 3.5. *Frequency component of v_a.*

In this thesis, however, a 10 kHz switching frequency is used. It is recommended that for further detail on PWM techniques, a reader is referred to [33, 34].

3.2 Current Controller in Synchronous Reference Frame

In synchronous reference frame PI-controllers are used, due to their capability for controlling dc variables [27]. As a result, the park transformation given in (2.2) is used to transform the grid current from three-phase to dq-reference frame that rotates synchronously with the grid voltage.

3.2.1 PI Control Structure and Working Principle

The PI-controller presents the following continuous-time expression

$$u(t) = K_p u(t) + K_i \int e(t)dt \tag{3.1}$$

while its frequency-domain representation is given by

$$G_{PI}(s) = K_p + \frac{K_i}{s} \tag{3.2}$$

The implementation of this type of controller is depicted in Fig. 3.6 with anti-windup. Constraints are present in real control systems; in power converters the duty cycle modulator has to be limited in order the converter works properly. The anti-windup scheme is used to avoid undesired closed-loop behavior that would damage the power converter such as poor transient response. The strategy has no effect on the output $u(t)$, if the unsaturated PI output $v(t)$ is within the linear range (i.e., $e(t) = 0$).

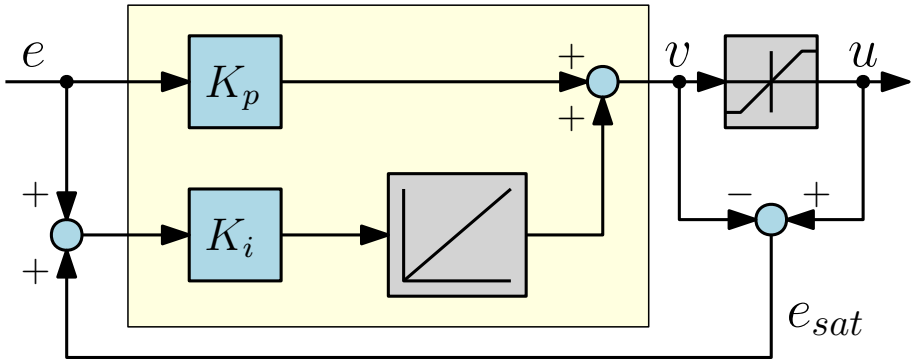


Figure 3.6. *PI-control with anti-windup scheme.*

PI-controller is a form of PID-controller where the derivative term is set to be zero, as it is sensitive to measurement noises. The proportional part of the PI-controller reduces the steady-state error and the integral part corrects the residual error in order to make sure the system is reaching its target value [35].

3.2.2 Current Controller Design

The dq-control structure is normally associated with PI-controllers. Therefore, dq-control will be used afterward for referring controls in the synchronous reference frame. The transfer function of the controller in dq coordinates can be given as

$$G_{PI-dq}(s) = \begin{bmatrix} G_{cd} & 0 \\ 0 & G_{cq} \end{bmatrix} = \begin{bmatrix} K_p + \frac{K_i}{s} & 0 \\ 0 & K_p + \frac{K_i}{s} \end{bmatrix} \tag{3.3}$$

where G_{cd} and G_{cq} are the controllers for the d and q channels, respectively. In order to obtain unity power factor, the q-channel output-current reference is usually set to zero. Hence, identical controller transfer functions are used for both d and q-components of the output-current. From the open-loop input-to-output transfer function matrix given in equation (2.33) the transfer functions from $\hat{d}_d$ to $\hat{i}_{L1d}$ (G_{cLdd-o}), $\hat{d}_q$ to $\hat{i}_{L1q}$ (G_{cLqq-o}), and $\hat{d}_d$ to $\hat{v}_{in}$ (G_{cid-o}) are the controlled ones.

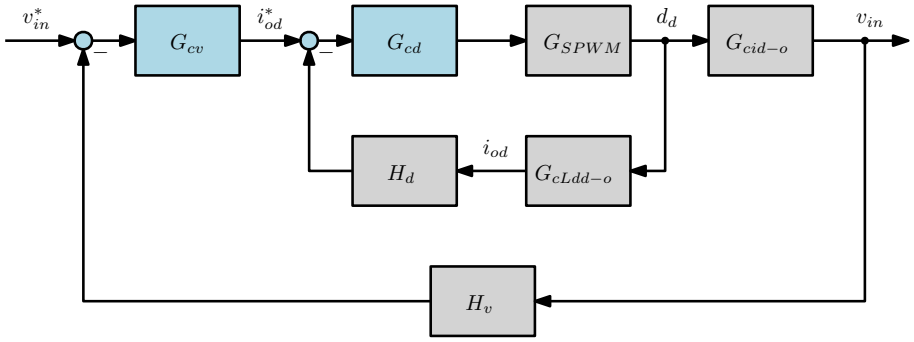


Figure 3.7. *Cascaded-control block diagram.*

As it is discussed above (3.1.2), the output-current-control is implemented in a cascaded-control manner as it is done in many other grid-connected inverter applications [4, 20, 24]. Fig. 3.7 presents the cascaded input-voltage-output-current-control block, where G_{SPWM} is the modulator gain and H_d and H_v are output-current and dc-voltage sensor gain, respectively.

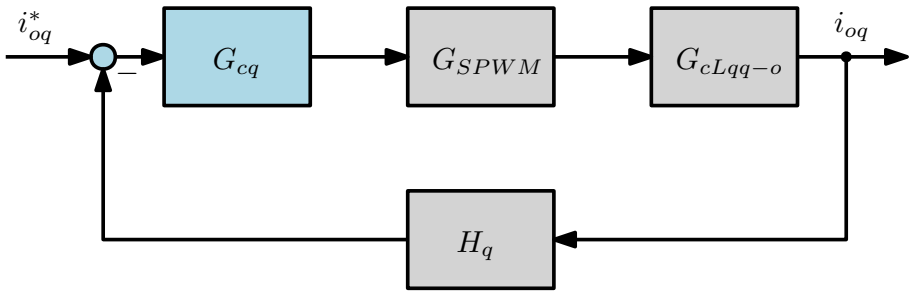


Figure 3.8. *Output-current q-component control block.*

Fig. 3.8 shows the control block diagram of the output-current q-component where H_q is its sensing gain. The main disadvantages of PI-controllers are the inability of the controller to track the reference values without a steady-state error and poor disturbance rejection capability. The main reason for this is, due to the fact that the integral part is sensitive to periodic disturbances. In grid-connected converters, to achieve compensation, additional phase-locked-loop (PLL) circuit and feedforward [24, 36, 37] are added to the control systems.

3.2.3 Parameters and Controller Tuning

The parameters related to the grid, converter and the LCL-type filter are presented in Table 3.2. The grid values are chosen according to the EU standards and the filter values according to the LCL filter manufactured by Platthaus GmbH that is implemented in the laboratory test bench [38]. If one wishes to design an LCL filter for three-phase grid-connected converters, there are a number of literature on the step-by-step design procedure addressing the limiting constraints such as a maximum allowable current ripple in the grid-side current, switching ripple attenuation, size and the total cost of the filter [12, 23].

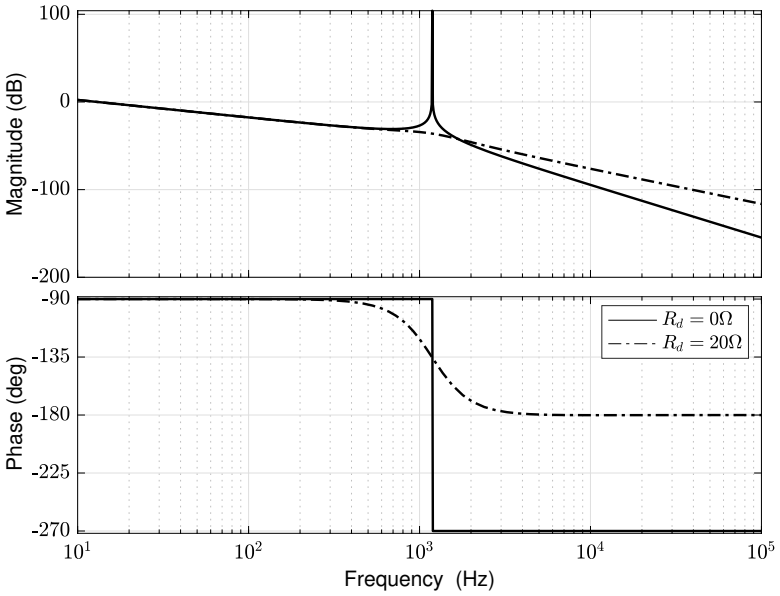


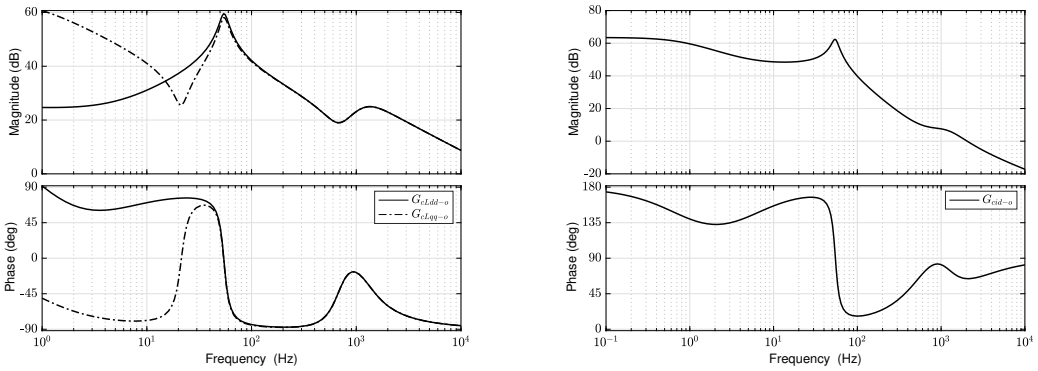
Figure 3.9. *Frequency response of LCL-fiter.*

LCL-filter damping is implemented passively with resistors in series with the capacitors to resonate the resonance frequency as shown in Fig. 3.9. The resistance is approximated 1/3 of the capacitor impedance at the LCL-filter resonance frequency to maintain the grid-side current at grid interfaced systems standards.

Table 3.2. *Grid, converter, and LCL-type filter parameters.*

$V_{g,abc}$	$230\ V$	V_{gd}	$325\ V$	f_s	$50\ Hz$
ω_s	$2\ \pi f_s$	I_{in}	$6\ A$	I_{L2q}	$0\ A$
C	2x$750\ \mu F$	C_f	$6.6\ \mu F$	R_d	$20\ \Omega$
L_1	$4.1\ mH$	r_{rL1}	$100\ m\Omega$	f_{sw}	$10\ kHz$
L_2	$8.1\ mH$	r_{rL2}	$300\ mH$	f_{res}	$1187\ Hz$

The controlling method is presented in Fig. 3.7 and 3.8. The open-loop control to inverter current d-component transfer function G_{cLdd-o}, the open-loop control to inverter current q-component transfer function G_{cLqq-o}, and input-voltage transfer function G_{cid-o} are shown in Fig. 3.10.



(a) *Open-loop control-to-inverter-current.* ***(b)*** *Open-loop control-to-input-voltage.*

Figure 3.10. *The control to inverter current transfer functions G_{cLdd} and G_{cLqq}.*

The input-voltage and output-current d-component are controlled in a cascaded manner as shown in Fig 3.7. Assuming the modulator gain G_{SPWM}, output-current and dc-voltage sensor gains (H_d and H_v) are unity, the loop gain for the input-voltage controller tuning can be given as

$$L_{in} = \frac{L_{outd}}{1 + L_{outd}} \frac{G_{cid-o}}{G_{cLdd-o}} \tag{3.4}$$

where L_{outd} (i.e., $G_{cd}G_{cLdd-o}$) is the loop gain of the inner control loop. The parameters of the chosen current controllers G_{cd} and G_{cq} are given in the Table 3.3. As it is suggested in most literature works the simplest method of dealing with the resonance behavior in passively damped LCL-filter is to limit the bandwidth of the current controller below that of the resonance frequency in order to have a stable system [23, 25, 26]. Hence, as shown in Fig. 3.12 the bandwidth of the current controller loops for both d and q-components is limited with the resonance behavior of the filter (i.e., current-control bandwidth is kept below the resonance frequency of the LCL filter).

Using loop-shaping techniques, the control parameters for the input-voltage controller are obtained as it is done for the current controllers. At the low-frequency part of the control-to-input-voltage as it is shown in Fig. 3.10b the phase starts from 180° implying that the control signal has to be inverted. The chosen parameters for the voltage controller are also given in the table. The tuning was done while keeping in mind the inner-loop has to be fast enough so that the output controller operates properly.

The PI-controllers for both d and q-channels were designed to achieve a crossover frequency while considering the control delay. This is because the delay effect caused by digital control decreases the phase in the closed-loop measurements. First-order Padé

approximation is used for the delay and it can be described as

$$G_{delay} = e^{-sT_{del}} \tag{3.5}$$

where T_{del} is 1.5 times the switching period of the converter.

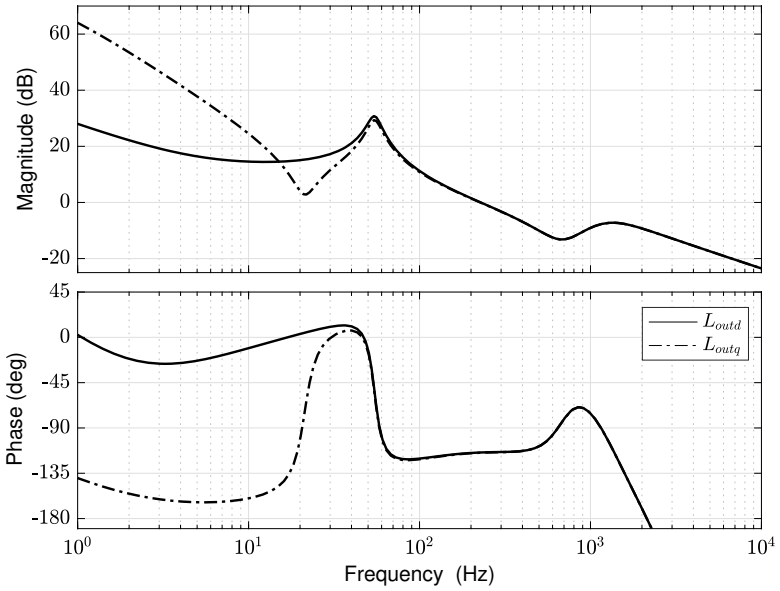


Figure 3.11. *Closed-loop control-to-inverter-current.*

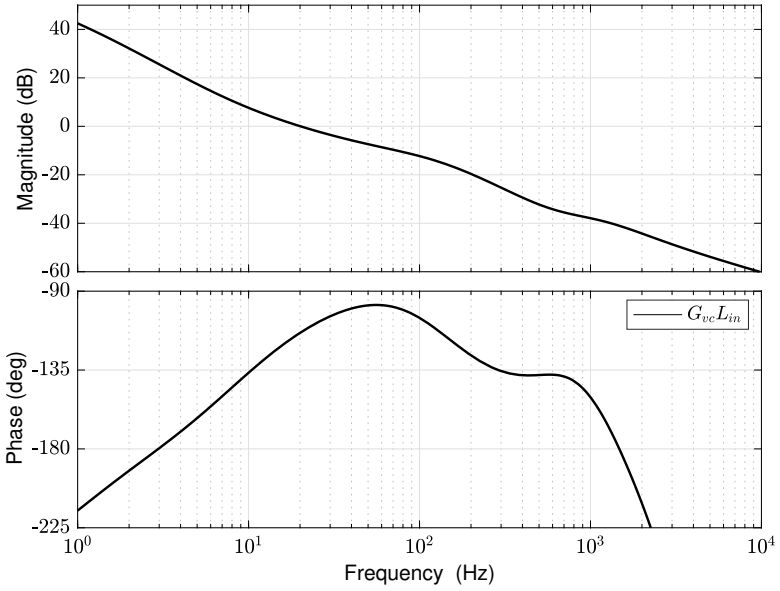


Figure 3.12. *Closed-loop input-voltage.*

The effect of the current-control on the magnitude of output admittance can be obtained from the closed-loop output admittances with PLL, dc-voltage control and proportional

grid-voltage feedforward [24, 39, 40]. The closed-loop output , on the other hand, are defined from the inverse of these closed-loop admittances. It is recommended that for further detail on the formation of the inverters impedances a reader is referred to [20].

Table 3.3. *Control parameters.*

Inverter current controller				Input-voltage controller			
CF	227 Hz	PM	65°	CF	20 Hz	PM	65°
K_p	0.0245	K_i	9.2257	K_{pv}	0.2900	K_{iv}	15.4882

An ideal current source is shown to have an infinite output impedance. That is why the harmonic mitigation of the grid-connected inverter is determined by the magnitude of inverter output impedance [36, 41]. Note that the inverter output impedance without the effects of dc-voltage control, PLL and feedforward for the q-channel neglecting decoupling is given as

$$Y_{oqq-c} = \frac{Y_{oqq-o}}{1 + G_{cq}G_{cLqq-o}} \tag{3.6}$$

where Y_{oqq-o} is the open-loop output admittance and G_{cLqq-o} the open-loop inductor-to-current transfer function. As it can be deduced from the equation (3.6), as the bandwidth of the current-control increases the output admittance reduces. Conversely, it affects the output impedance inversely.

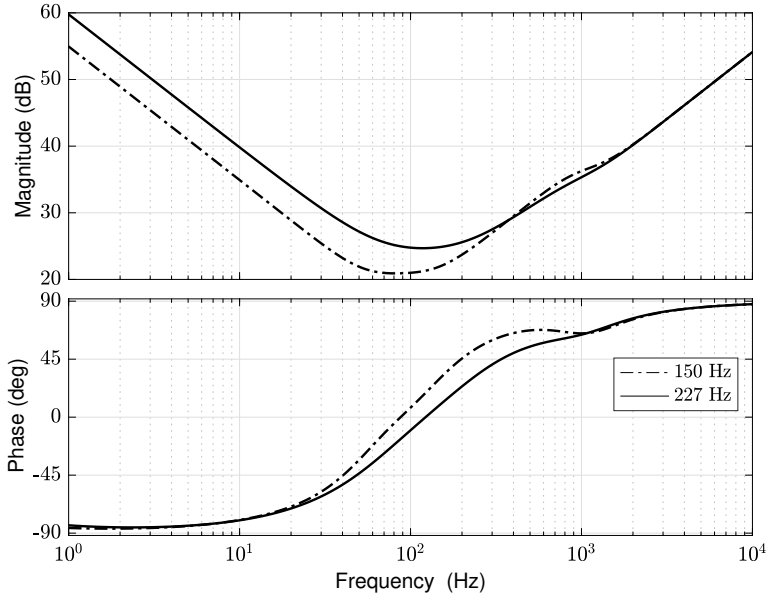


Figure 3.13. *Output impedance of a closed-loop model with ac current-control.*

As it is shown in Fig. 3.13 the impedance increased in magnitude with a wide bandwidth current-control. Thus, it can be deduced that as the bandwidth of the current-control increases, it makes the inverter act like an ideal current source.

3.2.4 Proportional Grid-Voltage Feedforward Term

In grid-connected converters the interaction between the grid input impedance and inverter output impedance has to satisfy Nyquist criterion as it is pointed in many literature works [24, 36, 39]. In stable operation, the inverter output impedance is greater than the grid impedance.

As has been shown above, the PI-controller is not able to track a sinusoidal reference without steady-state error. Thus, the use of feedforward terms is reported to improve the quality of current fed to the grid [24, 39, 42, 43]. The feedforward term became effective under distorted grid-voltage conditions because the feedforward term increases the output impedance of the inverter. Consequently, harmonic-rejection-ability of the current-control in dq-domain is essentially improved.

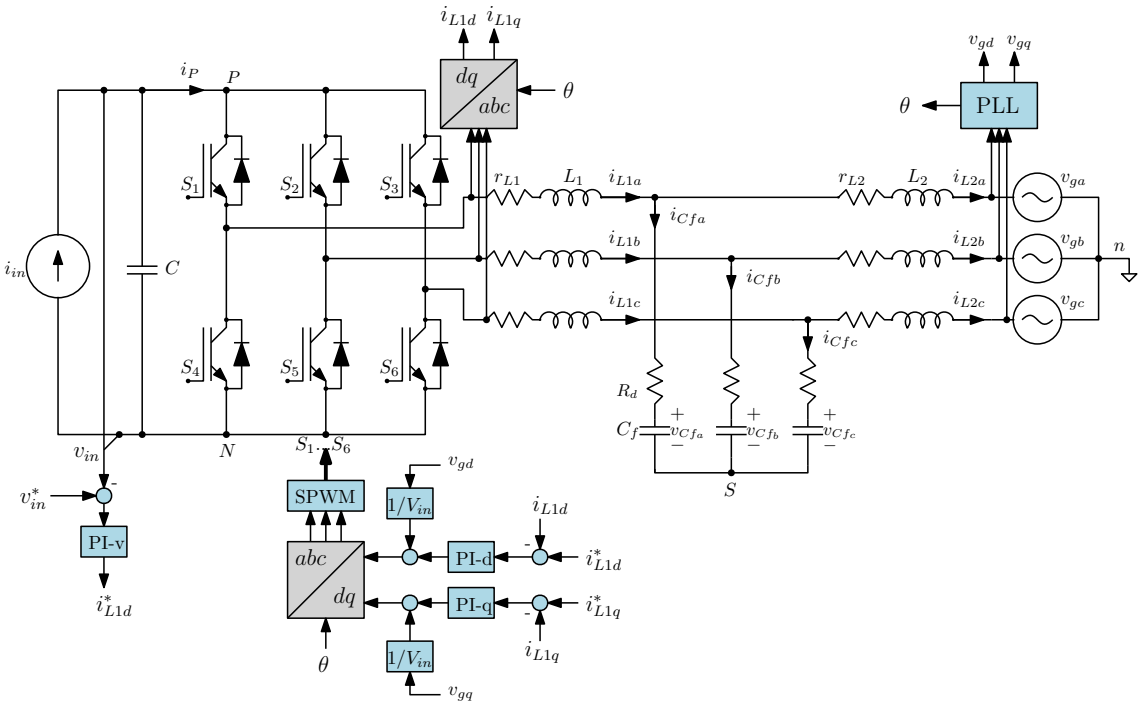


Figure 3.14. *Overview of the dq-control structure.*

The full-order model of the current-fed inverter with LCL-type filter in dq-domain is shown in Fig. 3.14. The inverter utilizes a cascaded control scheme where inverter side ac currents and dc-voltage are controlled. PLL is used generate the phase angle of the fundamental grid voltage. The grid voltage d and q-components for the formation of proportional grid-voltage feedforward are sensed from the PLL block.

The feedforward terms are chosen as in equation (3.7) according to [24]

$$G_{ff} = \begin{bmatrix} G_{ffd} & 0 \\ 0 & G_{ffq} \end{bmatrix} = \begin{bmatrix} \frac{1}{V_{in}} & 0 \\ 0 & \frac{1}{V_{in}} \end{bmatrix} \tag{3.7}$$

In Fig. 3.15 is shown the control block diagram for the inverter-side current-control. After solving the duty ratio from the block diagram, it is substituted back in (2.34) to include the PLL, feedforward and current-control in the closed-loop model. It should be noted that the PWM gains, sensing gains and decoupling gains are neglected for simplicity.

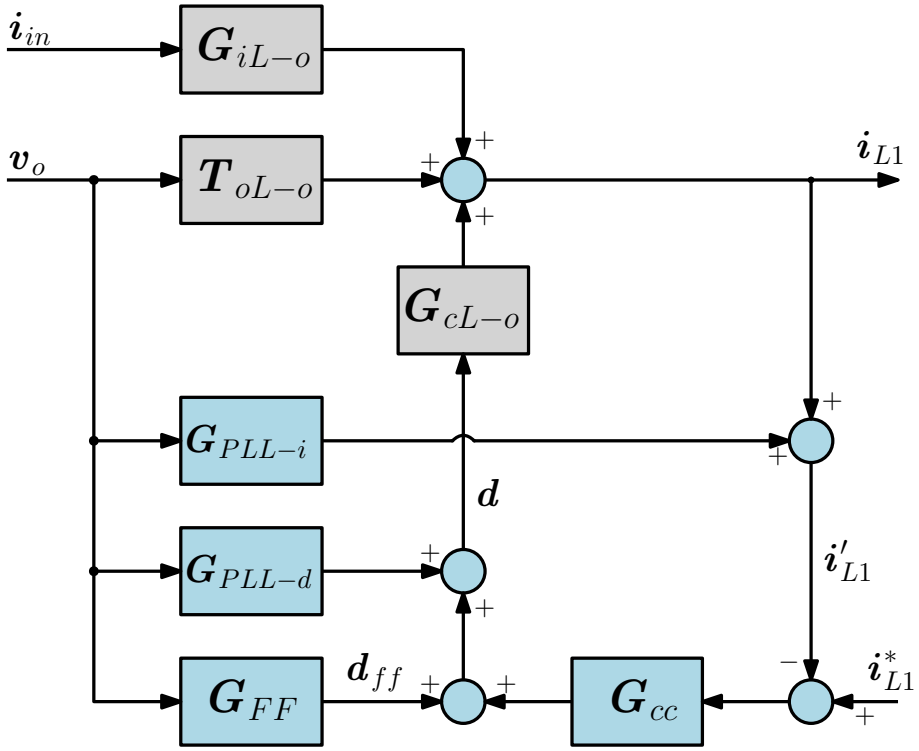


Figure 3.15. *current-control dynamics.*

The relevant transfer matrices to calculate the output impedance of the grid-connected converter can be given

$$\boldsymbol{T}_{oi-cc} = \boldsymbol{T}_{oi-o} - \boldsymbol{G}_{ci-o}(\boldsymbol{I} + \boldsymbol{L}_{cc})^{-1}(\boldsymbol{G}_{PLL} + \boldsymbol{G}_{FF} - \boldsymbol{G}_{cc}\boldsymbol{T}_{oL-o}) \tag{3.8}$$

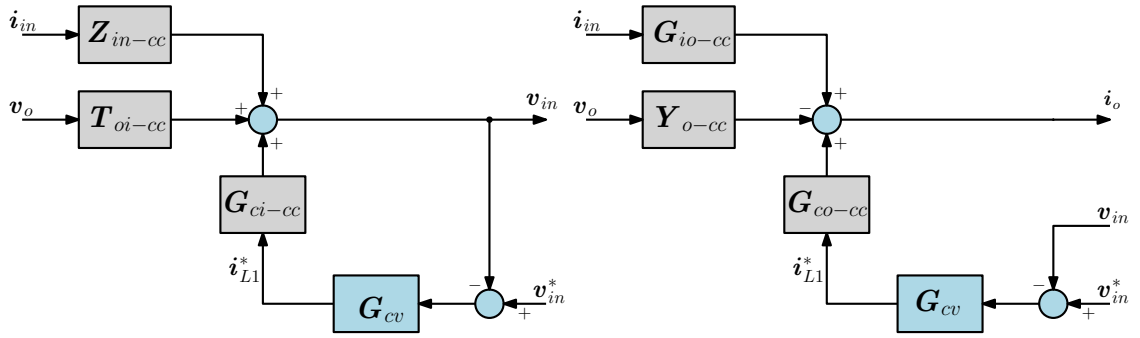
$$\boldsymbol{G}_{ci-cc} = \boldsymbol{G}_{ci-o}(\boldsymbol{I} + \boldsymbol{L}_{cc})^{-1} + \boldsymbol{G}_{cc} \tag{3.9}$$

$$\boldsymbol{Y}_{o-cc} = \boldsymbol{Y}_{o-o} - \boldsymbol{G}_{co-o}(\boldsymbol{I} + \boldsymbol{L}_{cc})^{-1}(\boldsymbol{G}_{PLL} + \boldsymbol{G}_{FF} - \boldsymbol{G}_{cc}\boldsymbol{Y}_{oL-o}) \tag{3.10}$$

$$\boldsymbol{G}_{co-cc} = \boldsymbol{G}_{co-o}(\boldsymbol{I} + \boldsymbol{L}_{cc})^{-1} + \boldsymbol{G}_{cc} \tag{3.11}$$

where the current-control loop gain is defindes as $\boldsymbol{L}_{cc} = \boldsymbol{G}_{cc}\boldsymbol{G}_{cL-o}$ and the PLL loop gain as $\boldsymbol{G}_{PLL} = \boldsymbol{G}_{PLL-d} - \boldsymbol{G}_{PLL-i}$. The current control, PLL loop gains and grid-voltage feedforward are given in the Appendix B.

The closed-loop output admittance matrix can be solved from Fig. 3.16 and can be



(a) *Input dynamics* ***(b)*** *Output dynamics*

Figure 3.16. *Input and output dynamics when the input voltage contol loop is closed*

presented as 3.12

$$\boldsymbol{Y}_{o-c} = \boldsymbol{Y}_{o-cc} - \boldsymbol{G}_{co-cc}\boldsymbol{G}_{c-in}(\boldsymbol{I} + \boldsymbol{L}_{in})^{-1} T_{oi-cc} \tag{3.12}$$

$$\boldsymbol{L}_{in} = \boldsymbol{G}_{ci-cc}\boldsymbol{G}_{cv} \tag{3.13}$$

where $\boldsymbol{G}_{cv}$ is the input voltage controller matrix.

Fig. 3.17 and 3.18 show the output impedances with and without the effect of the proportional grid-voltage feedforward term. As it can be evidenced from both figures, the grid-voltage feedforward has a significant effect on boosting the shape the inverter output impedance. The magnitude of the output impedance increases from the dc-voltage

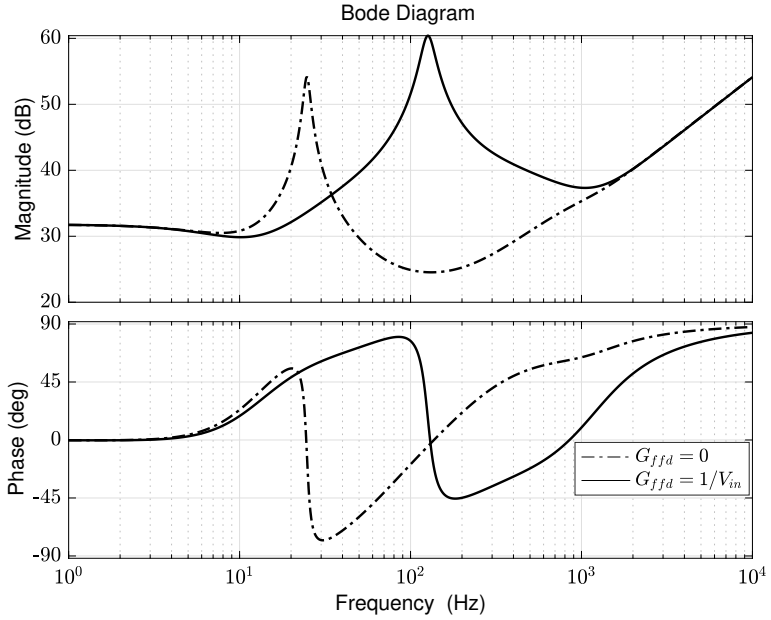


Figure 3.17. *D-component inverter output impedance.*

control bandwidth frequency to the resonant frequency of the LCL filter in both cases. However, as it can be seen from the figures, the feedforward term does not have any

effect on the shape of the impedances at frequencies over the resonant frequency. The direct effect the proportional feedforward has on the grid-side current quality will be shown in Chapter 5.

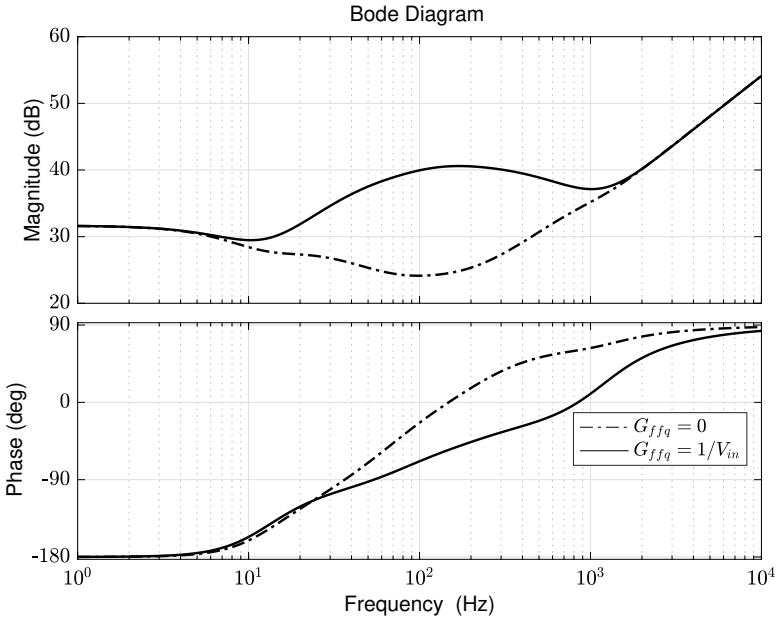


Figure 3.18. *Q-component inverter output impedance.*

The transfer functions used to plot the inverter output admittance are given in Appendix B. It should also be noted that due to the high number of poles and zeros MATLAB approximates the coefficients to infinite values. As a consequence, the transfer functions are converted to frequency-response data using the frd() MATLAB function to avoid inaccuracy problems.

3.3 Current Controller in Stationary Reference Frame

A proportional plus resonant controller is getting widely popular as current-control technique in grid-connected converters due to its simplicity and performance tracking reference in the stationary reference frame ($\alpha\beta$-frame)[27, 44, 45].

Control in the synchronous reference frame is quite complex, because it requires phase transformation from abc to dq quantities to utilize conventional PI-controllers. Moreover, the quantities have to transform back again to the stationary reference frame for execution. This by itself can introduce errors, if the phase transformation is not accurate. Zmood and et al. [46] developed proportional-resonant (PR) control for reference tracking in stationary frame from servo control system with the same transient and steady-state performances as PI-controllers used in synchronous reference frame for single and three-phase systems.

Teodorescu and et al. [45, 47] noted in there work that, and the proposed PR-controllers has the ability to enhance the shortcomings of the conventional PI-controllers such as the converter reference tracking. The current-control in stationary reference frame does not require as many phase transformations as in synchronous reference frame. Moreover, the control complexity in dq-reference frame is significantly reduced, since grid voltage feed-forward and cross-coupling terms are no longer needed.

3.3.1 PR Control Working Principle

The basic operational principle of PR-controller is quite simple. It introduces an infinite gain at a specific resonant frequency in order to mitigate steady-state error at the specific frequency [44, 45, 46]. As a result, the controller can be flexibly tuned selectively to compensate low-order harmonics using multiple PR-controllers simultaneously.

The PI-controller given in (3.2) can be transformed to ac compensatory working at ω. Thus, the controller can work in stationary reference frame without phase transformations. In order to do this, the integral part of the conventional PI-controller is shifted to both positive and negative fundamental frequencies to obtain the following term

$$\frac{1}{s} \rightarrow \frac{1}{s - j\omega} + \frac{1}{s + j\omega} = \frac{2s}{s^2 + \omega^2}. \tag{3.14}$$

As a result a resonant controller can be given as

$$G_{PR}(s) = K_p + K_i \frac{2s}{s^2 + \omega^2} \tag{3.15}$$

The proportional gain K_p and the integral gain K_i are tuned the same way as for the PI-controller. The proportional gain responsible to the system bandwidth, phase and gain margin. It should be noted also that the PR-controller given in (3.15) is ideal and sensitive to grid frequency. To overcome the stability problem related to infinite gain a damped PR-controller is used in practical applications. This controller is given by

$$G_{PR}(s) = K_p + K_i \frac{2\omega_c s}{s^2 + 2\omega_c s + \omega^2} \tag{3.16}$$

where $\omega_c << \omega$ is cutoff frequency. The cutoff frequency ω_c helps the controller from sensitivity towards frequency variation. The cutoff frequency is usually adjusted to be 5 - 15 rad/s in real applications to deal with different frequency variations [45]. In this thesis 8 rad/s is chosen.

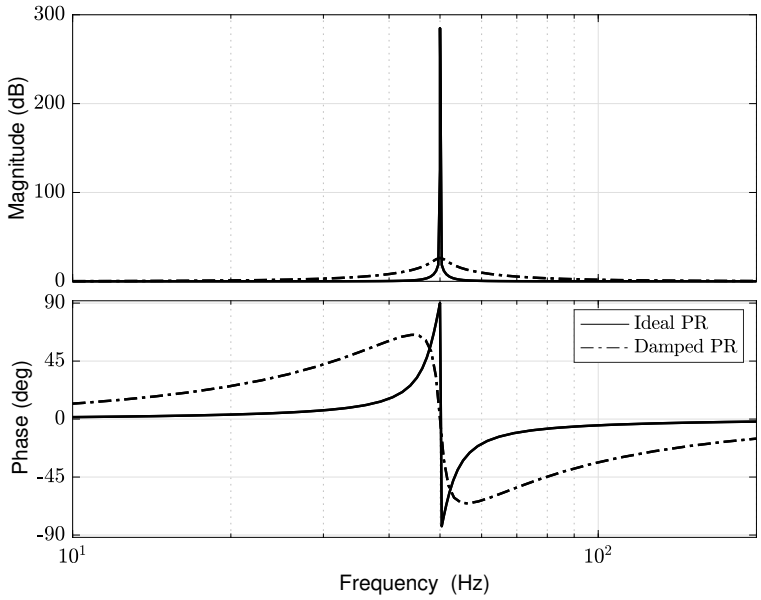


Figure 3.19. *Ideal and damped PR controller with* $K_p = 1$, $K_i = 20$ *and* $\omega_c = 8rad/s$.

3.3.2 PR Control and Harmonic Compensators

In the PR case, the output-current controller transfer function in stationary reference frame is given by

$$G_{PR-\alpha\beta}(s) = \begin{bmatrix} G_{PR-\alpha} & 0 \\ 0 & G_{PR-\beta} \end{bmatrix} = \begin{bmatrix} K_p + \frac{2K_i\omega_c s}{s^2+2\omega_c s+\omega^2} & 0 \\ 0 & K_p + \frac{2K_i\omega_c s}{s^2+2\omega_c s+\omega^2} \end{bmatrix} \tag{3.17}$$

where ω is the resonance frequency of the controller, K_p is the proportional gain, and K_i is the integral gain of the controller, which must be tuned to a high value for downsizing the steady-state error. The same controllers are used for the α and β components, which are denoted by $G_{PR-\alpha}$ and $G_{PR-\beta}$, respectively.

As it is mentioned above, selective harmonic compensation (HC) can be achieved by cascading several generalized integrators tuned to resonate at the desired low-order frequencies. Selective HC for maximum harmonic order (m) specified for attenuation is given as

$$G_{HC}(s) = \sum_{h=1}^{m} K_{ih} \frac{2s}{s^2 + (h\omega)^2} \tag{3.18}$$

where ω is the resonance frequency, h is the harmonics number and K_{ih} is the specific resonant gain. Because the harmonic compensator is able to work on both positive and negative sequences, one harmonic compensator is required to mitigate a harmonic order.

The damped selective HC can also be given as:

$$G_{HC}(s) = \sum_{h=1}^{m} K_{ih} \frac{2\omega_c s}{s^2 + 2\omega_c s + (h\omega)^2} \tag{3.19}$$

The integrator part of the resonant function for the fundamental in (3.16) and harmonic compensator in (3.19) can be implemented as a depicted Fig. 3.20. Notice that proportional K_p is add for the fundamental PR controller.

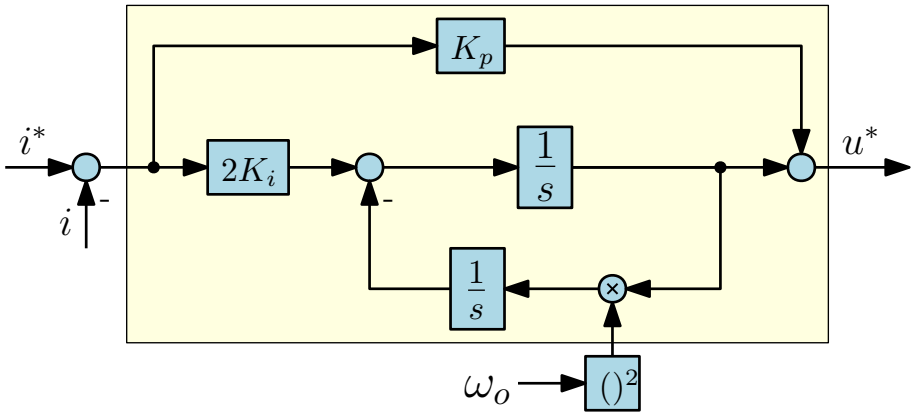


Figure 3.20. *Harmonic compensator implementation scheme.*

The PR controller can be implemented as depicted in Fig. 3.20. The controller was made adaptive to the frequency of the grid that is generated from the phase-locked-loop (i.e., ω_o). The HCs are being implemented in the same manner without the proportional gain (K_p) by tuning them to the harmonic orders that need to be rejected. PLL is responsible for generating the accurate phase and frequency information of the fundamental grid voltage. The working principle of PLLs will be discussed further in Chapter 4.

3.3.3 PR Control Design

As it is reported in [13, 48], it is reasonable to use the same method to design the parameters for PI and PR-controllers due to their similarity. The difference, however, is the PR controller is adapted to track reference in $\alpha\beta$-domain, which PI-controller cannot. Hence, the PR controller was designed using loop-shaping techniques as it was done in the dq-control. The proportional (K_p) and integral gain (K_i) of the PR-controllers are chosen to be equivalent to the control parameters used in dq-domain. The implementation of the harmonic compensators for the 5th, 7th, 11th and 13th are done correspondingly.

As shown in Fig. 3.21, adding HCs to the PR controller adds the resonant peaks at multiples of the fundamental frequency. The resonance peak existed only in the fundamental frequency the used PR controller cannot effectively compensate the grid current. However, together with HCs, the system will have enough gains in multiple harmonics and subsequently compensate the current effectively with the help of the HCs. In [49, 50], it

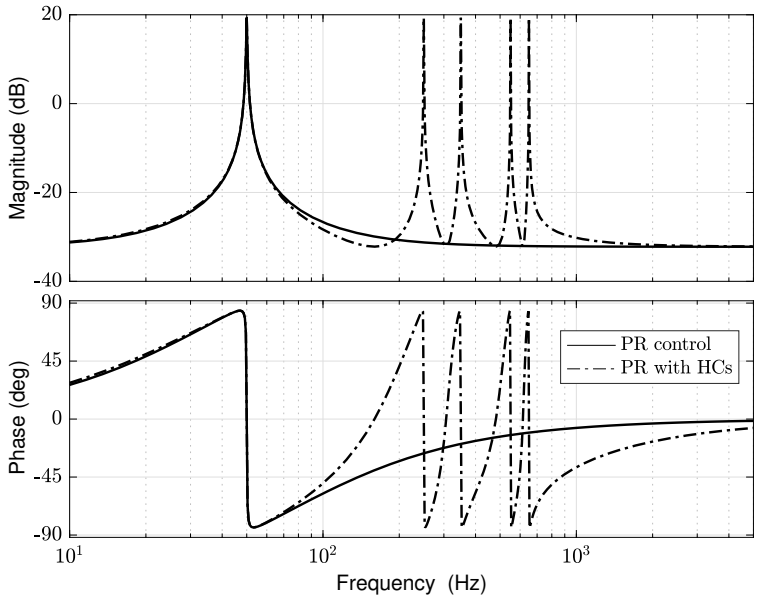


Figure 3.21. *Bode plot of PR controller and PR controller with HCs.*

was demonstrated that PR+HCs with enhancement of harmonic impedance for LCL-filter interfaced grid-connected converters. Subsequently, rejection of current distortion can be achieved.

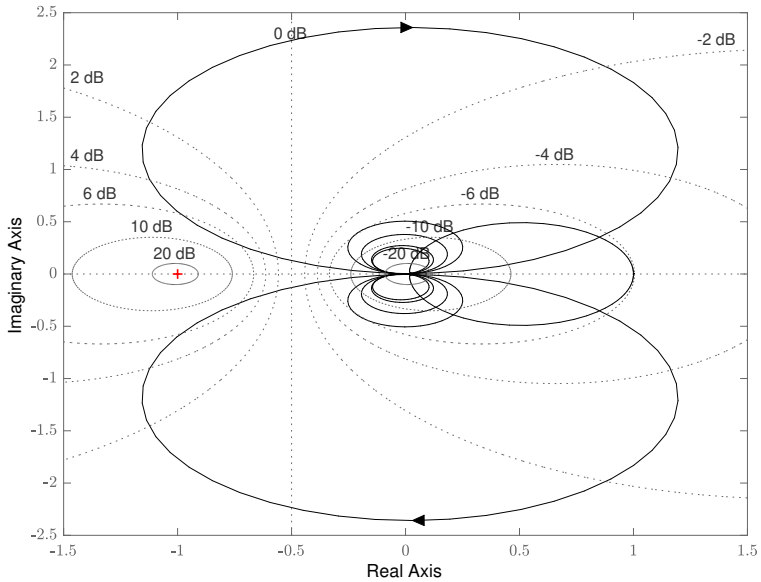


Figure 3.22. *Closed loop Nyquist plot of the designed PR controller with HCs.*

The bode plot of the system cannot easily tell whether the system is stable or not. In this case, the Nyquist plot becomes effective in dealing with these types of issues. Fig. 3.22 presents the Nyquist plot of the PR controller with HCs system including the LCL filter.

4 GRID SYNCHRONIZATION METHODS

In grid-connected converters, the current-control scheme requires the accurate phase and frequency information of the grid voltage fundamental component. Having the exact phase and frequency enables the inverter to inject current to the grid. In a real application, these crucial pieces of information are generated by a phase-locked-loop (PLL). PLL takes the grid voltage as its input and generates the appropriate information for the current-control scheme. Hence, proper synchronization is an essential part of grid-connected converters. In this chapter, the working principles of conventional synchronous reference frame PLL (SRF-PLL), delayed signal cancellation PLL (dqDSC-PLL) that improve the performance under unbalanced grid condition are presented. Moreover, the thesis also proposes an improved dqADSC-PLL [19], which can achieve twice the bandwidth of dqDSC-PLLs and it is rather quite simple to implement.

4.1 Synchronous Reference Frame Phase-locked-loop

In grid-connected applications, the PLLs are the most widely used synchronization techniques. According to Messo and et al. [24], the effect of the PLL can be analyzed from the small-signal angle difference between the grid reference frame and the control system reference frame. The linearized control system d and q-components can be given as a function of grid d and q-components by

$$\begin{aligned} \hat{x}_{d-c} &= \hat{x}_d + \Theta_\Delta \hat{x}_q + X_q \hat{\theta}_\Delta \\ \hat{x}_{q-c} &= \hat{x}_q - \Theta_\Delta \hat{x}_q - X_d \hat{\theta}_\Delta \end{aligned} \tag{4.1}$$

where Θ represents the steady-state phase difference between the systems and subscript c represents the reference frame of the control system. Consequently, utilizing (4.1) the grid variables can be described as a function of the angle difference and the control system variables as

$$\begin{aligned} \hat{v}_{gd} = \hat{v}_{gd-c}, \quad \hat{v}_{gq} &= \hat{v}_{gq-c} + V_{gd}\hat{\theta}_\Delta \\ \hat{i}_{L1d} = \hat{i}_{L1d-c}, \quad \hat{i}_{L1q} &= \hat{i}_{L1q-c} + I_{L1d}\hat{\theta}_\Delta \\ \hat{d}_d = \hat{d}_{d-c}, \quad \hat{d}_q &= \hat{d}_{L1q-c} + D_d\hat{\theta}_\Delta. \end{aligned} \tag{4.2}$$

However, in steady-state the error, grid voltage V_{gq}, q-component of the controlled current I_{L1q} and the q-component of the duty ratio D_q are assumed to be zero.

As can be deduced from (4.2) and assuming that the grid frequency is constant (i.e., $\hat{\theta}_\Delta = \hat{\theta}_c$), the linear control block diagram in frequency-domain to generate the small-signal angle $\hat{\theta}_c$ is depicted in Fig. 4.1. The reference grid voltage q-component v^*_{gq} is set to zero to synchronize the control system reference frame with the grid voltage space-vector.

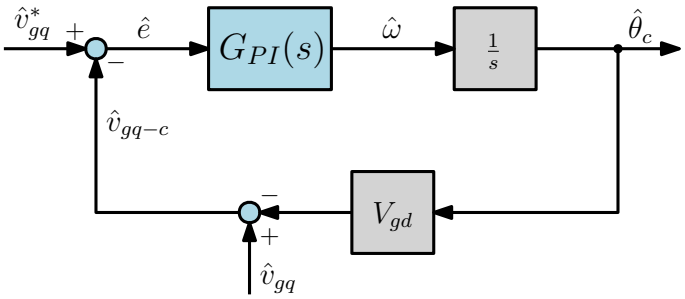


Figure 4.1. *Linearized control block diagram of the PLL.*

From Fig. 4.1, the small-signal angle can be solved and it is given by

$$\hat{\theta}_c = \frac{1}{V_{gd}} \cdot \frac{L_{PLL}}{1 + L_{PLL}} \hat{v}_{gq} \tag{4.3}$$

where

$$L_{PLL} = -\frac{V_{gd}}{s} G_{PI}(s). \tag{4.4}$$

Tuning the PLL is quite simple. The control bandwidth determines how fast the grid angle is synchronized. When the PLL utilizes higher bandwidth, it enables the PLL to have a faster response, but the loop gain amplifies any noise below the crossover frequency. Thus, higher bandwidth PLL is shown to increases instability when it connected to a weak grid as reported in [24, 36, 37].

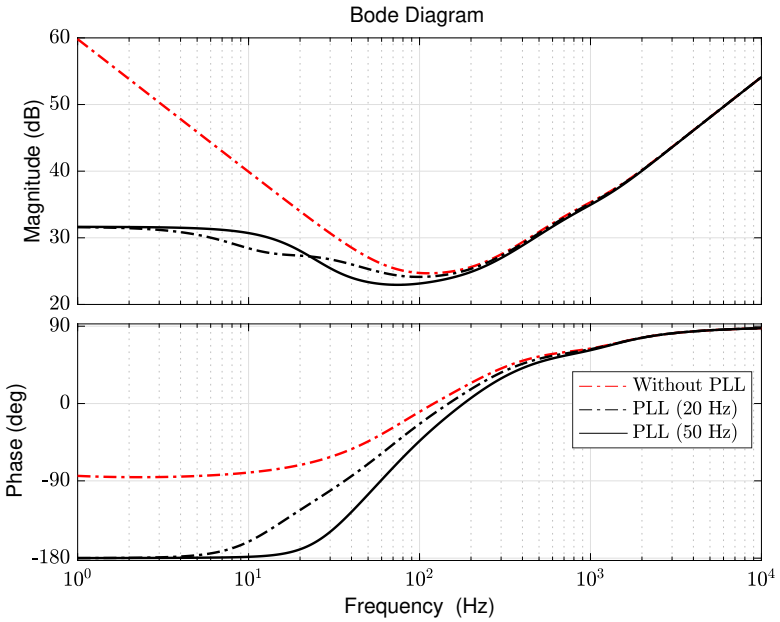


Figure 4.2. *The q-channel output impedance Z_{o-q} of a closed-loop model.*

Fig. 4.2 shows the output impedance of a closed-loop model under the influence of a phase-locked-loop. Here, because of the PLL, the phase of the closed-loop output impedances are shifted to -180 degrees making the systems prone to harmonic distortion or instability. Moreover, the wide-bandwidth PLL phase thrives close to -180 degrees which increase the susceptibility of the system to grid voltage unbalance and harmonic distortion.

To comprehend the operation and performance of the SRF-PLL, the simulation results under ideal three-phase grid voltage, Unbalanced and distorted grid conditions are pro-

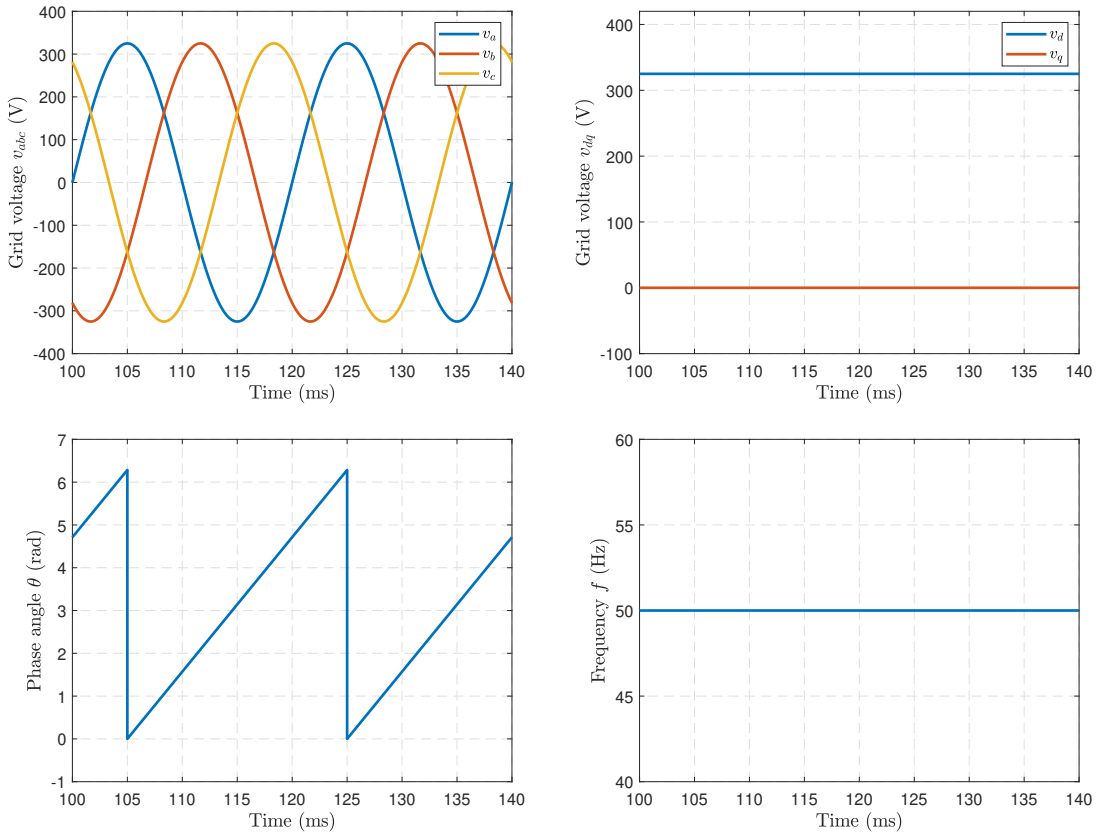


Figure 4.3. *SRF-PLL with ideal three-phase grid voltage.*

vided, respectively. The simulations results under ideal grid conditions are shown in Fig. 4.3. As it is depicted, the grid voltage is balanced and pure sinusoidal. The phase angle increases linearly and periodically from 0 to 2π rad within 20 ms. Moreover, the phase angle precisely follows the grid voltage. Furthermore, the grid voltage in synchronous frame is kept constant, indicating the proper alignment of the grid voltage with the d-axis. The frequency is also kept constant as 50 Hz.

As seen from Fig. 4.4, the unbalanced three-phase grid voltage degrade the performance of the SRF-PLL. The phase angle contains fluctuations and does not increase linearly as it does in an ideal three-phase grid voltage condition. Moreover, the grid voltage d- and q-axis components contain a fluctuation twice the fundamental frequency.

Likewise, as it can be evidenced from Fig. 4.5, the presence of 5th, 7th and 11th harmon-

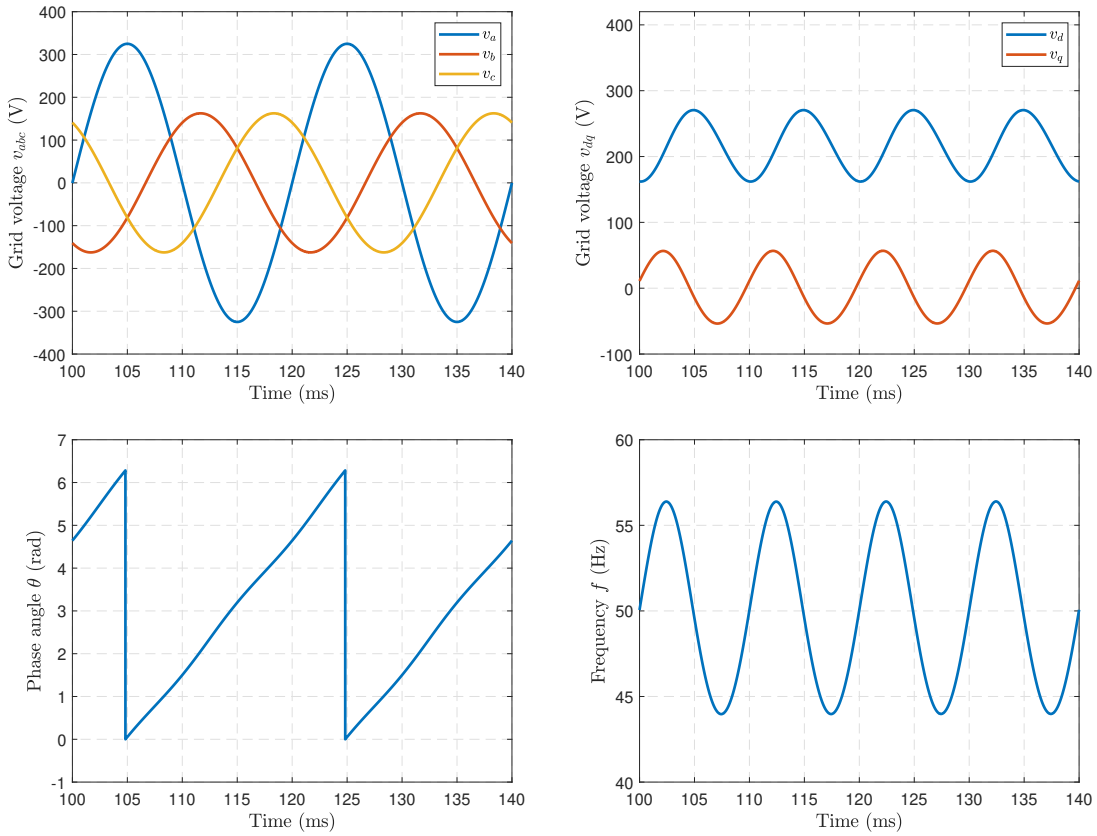


Figure 4.4. *SRF-PLL with unbalanced three-phase grid voltage.*

ics in the grid three-phase voltage, the grid voltage in synchronous reference frame and frequency are no longer constants. Moreover, the same can also be said for the phase angle.

The conventional SRF-PLL is a commonly used synchronization method due to its simplicity and robust performance. However, as it can be deduced from the simulation results, unbalanced and distorted grid conditions profoundly degrade its performance. To overcome this drawback, different advanced PLLs have been proposed in the literature [16, 17, 18].

4.2 Conventional Delayed Signal Cancellation PLL

A number of delayed-signal-cancellation (DSC) PLLs have been developed for microgrid applications to deal with these challenges [16, 17, 18]. The proposed PLLs eliminate the undesired harmonics from going into the PLL loop. Thus, the PLL control loop can be tuned to have a wider bandwidth. Subsequently, accurate and fast detection of the grid phase angle can be achieved.

As already mentioned PLL is a closed-loop feedback control system that tries to synchronize its output in frequency and phase with its input. Different researchers have proposed different strategies to perform under different scenarios. These methods can be clas-

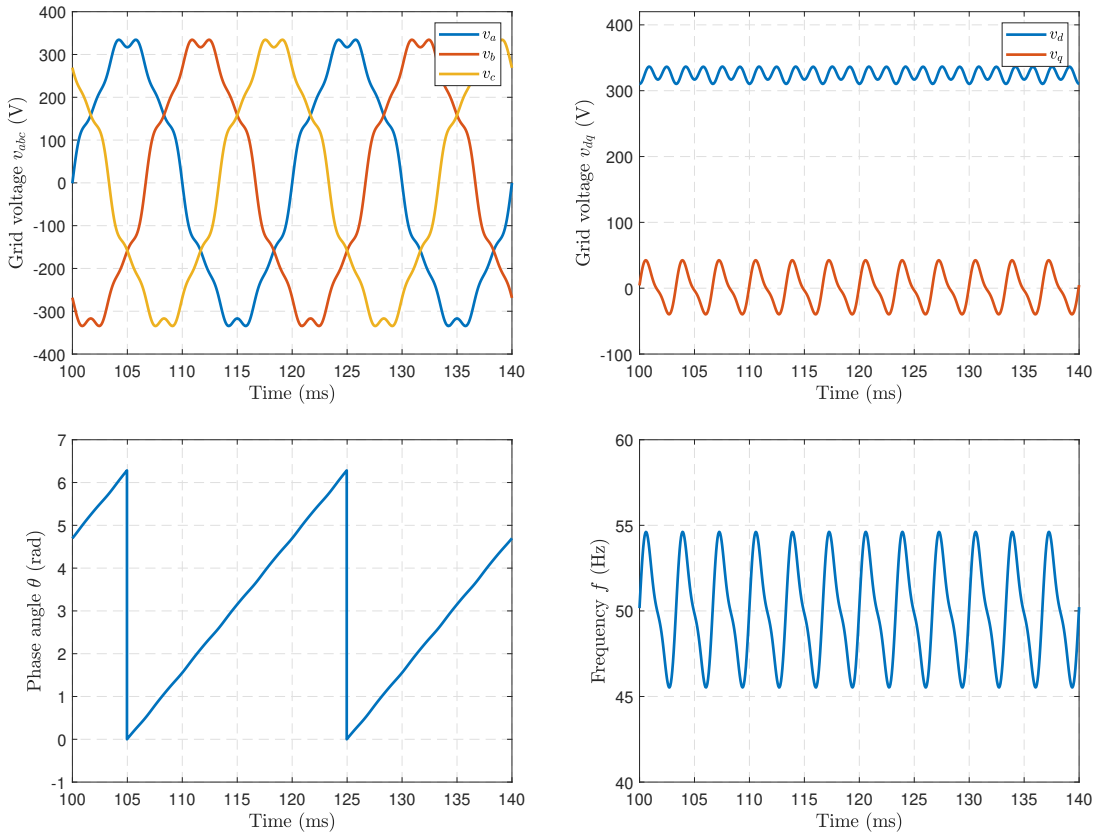


Figure 4.5. *SRF-PLL with distorted three-phase grid voltage.*

sied into two major categories, namely in-loop and pre-loop methods [51]. In this thesis, dqDSC-PLL and $\alpha\beta$DSC-PLL are studied. A cascaded version of the latter PLL type is used under distorted grid conditions as it can effectively be tuned to different harmonic frequencies. The contents in the next sections are for the most part from [19].

4.2.1 $\alpha\beta$DSC-PLL

A three-phase unbalanced grid voltage can be described using positive and negative sequence components according to

$$\begin{aligned} v_a(t) &= V^+ \cos(\omega t + \theta^+) + V^- \cos(\omega t + \theta^-) \\ v_b(t) &= V^+ \cos(\omega t - \frac{2\pi}{3} + \theta^+) + V^- \cos(\omega t - \frac{2\pi}{3} + \theta^-) \\ v_c(t) &= V^+ \cos(\omega t + \frac{2\pi}{3} + \theta^+) + V^- \cos(\omega t + \frac{2\pi}{3} + \theta^-) \end{aligned} \tag{4.5}$$

where ω is the fundamental angular frequency, V^+ and V^- are the amplitudes and θ^+ and θ^- the phase angles of the positive and negative sequence components, accordingly.

Applying the Clarke transformation transforms voltages in the $\alpha\beta$-coordinate system as

$$\begin{aligned} v_\alpha(t) &= V^+\cos(\omega t) + V^-\cos(\omega t) \\ v_\beta(t) &= V^+\sin(\omega t) - V^-\sin(\omega t) \end{aligned} \tag{4.6}$$

According to [52], the delayed signals in $\alpha\beta$-domain for a delay ($\frac{T_1}{n}$) is defined as

$$\begin{aligned} v_\alpha^d(t) &= \frac{1}{2}\Big(v_\alpha + v_\alpha\Big(t-\frac{T_1}{n}\Big)\cos\Big(\frac{2\pi}{n}\Big) - v_\beta\Big(t-\frac{T_1}{n}\Big)\sin\Big(\frac{2\pi}{n}\Big)\Big) \\ v_\beta^d(t) &= \frac{1}{2}\Big(v_\beta + v_\beta\Big(t-\frac{T_1}{n}\Big)\cos\Big(\frac{2\pi}{n}\Big) - v_\alpha\Big(t-\frac{T_1}{n}\Big)\sin\Big(\frac{2\pi}{n}\Big)\Big) \end{aligned} \tag{4.7}$$

In a conventional DSC-PLL, a fixed time delay is used to deal with established harmonic. A time delay of one-fourth of the fundamental $T_1/4$ corresponds to a $\frac{\omega T}{4} = \frac{\pi}{2}$ phase shift when the grid frequency is at its nominal value. The delay cancels out the negative component effectively while keeping the positive sequence component the same.

$$\begin{aligned} v_\alpha^d(t) &= \frac{1}{2}\Big(v_\alpha(t) - v_\beta\Big(t-\frac{T_1}{4}\Big)\Big) = V^+\cos(\omega t) \\ v_\beta^d(t) &= \frac{1}{2}\Big(v_\beta(t) + v_\alpha\Big(t-\frac{T_1}{4}\Big)\Big) = V^+\sin(\omega t). \end{aligned} \tag{4.8}$$

Since the delay works as a prefiltering technique, it does not degrade the internal dynamics of the PLL. Thus, the control loop gain of the this PLL is defined as SRF-PLL. The effect of unbalance can be eliminated using a decoupling network as shown in Fig. 4.6. It should be also noticed that multiple DSC blocks can be connected in series to cancel

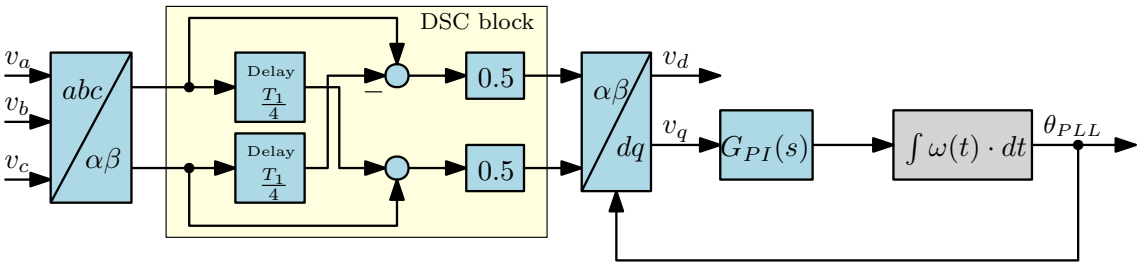


Figure 4.6. *Conventional DSC-PLL in statonary frame.*

out harmonics at different frequencies as it is proposed in the literature [51, 52, 53].

4.2.2 dqDSC-PLL

The unbalanced three-phase system given in (4.5) can be transformed to a synchronous reference frame which is aligned with the space-vector of positive sequence component. The d and q-components can be given as (4.9). As it can be seen clearly from the

equation, both the d and q-components oscillate with the second harmonic frequency

$$\begin{aligned} v_d^+ &= V^+ + V^- \cos(2\omega t + \theta^-) \\ v_q^+ &= -V^- \sin(2\omega t + \theta^-) \end{aligned} \tag{4.9}$$

In order to void the second harmonic oscillation from the q-component (i.e., which is used as a synchronization signal) a one-fourth of fundamental delay is used. The exclusive delay effectively cancels out the second harmonic oscillation. Delaying the second harmonic by $T_1/4$ as shown in Fig. 4.7 and adding the shifted signal with the original cancels out the effect of the negative sequence component. Furthermore, the summed signal is halved to keep the dc gain of the PLL unaffected.

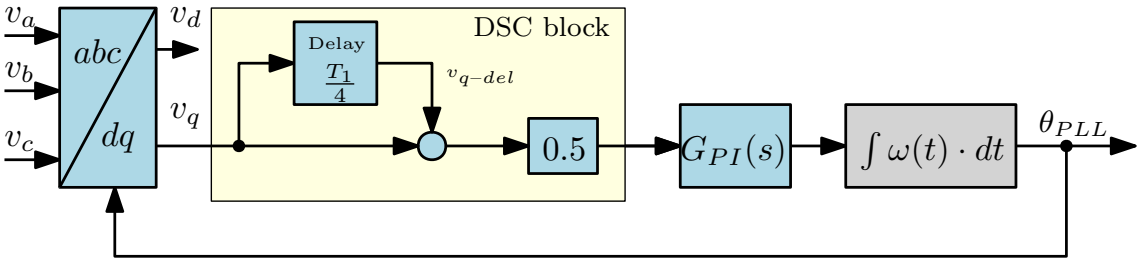


Figure 4.7. *Conventional DSC-PLL in synchronous reference frame.*

In frequency-domain, the loop gain of dqDSC-PLL can be described as

$$L_{PLL}^{dqDSC-PLL} = \frac{V_{gd}}{s} G_{PI}(s) e^{-\frac{T_1}{8}s}. \tag{4.10}$$

Since there are two paths for the q-component to pass through the DSC block, the delay is half of the actual delay. As can be deduced from the equivalent scheme, the q-component has one direct and one through the delay block paths. Thus, the effective delay in the loop gain is half of the actual delay.

4.3 Improved Delayed Signal Cancellation PLL

This thesis proposes an improved delayed signal cancellation PLL that is quite easy to implement compared to the other DSC-PLLs proposed in the literature [16, 17, 18]. As it was pointed out in [19], the proposed DSC-based PLL is implemented in the dq-domain. The synchronization method allows to reduce the internal delay down to one-eighth of the fundamental grid period. Therefore, the proposed PLL can have twice the bandwidth of dqDSC-PLL before becoming unstable.

As shown in Fig. 4.8, the improved delayed-signal PLL has a simple structure and requires only one delay element. In order to verify the model, the small-signal model, which allows a deterministic control design and the measured control loop gains are provided. As discussed in [19], the proposed improved DSC-PLL showed excellent performance

when tested under unbalanced voltage conditions. This is duet to the fact that as mentioned above, unbalanced grid voltages introduce more harmonics in grid currents when a conventional SRF-PLL is used.

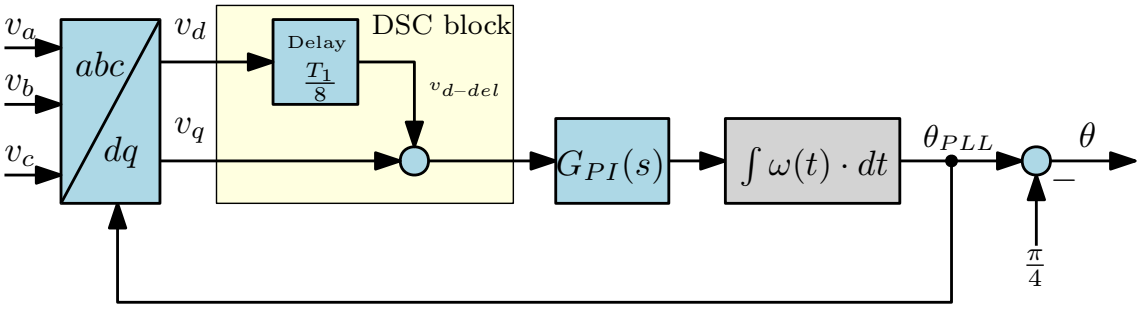


Figure 4.8. *Modified DSC-PLL in synchornous reference frame.*

In improved delayed signal cancellation [19], the grid voltage space vector can be given in the PLL reference frame according to

$$\boldsymbol{v}^{PLL} = \boldsymbol{v}^{grid} \cdot e^{j(-\delta+\theta)} = \boldsymbol{v}^{grid} \cdot e^{-j\delta} \cdot e^{j\theta} \tag{4.11}$$

where the angle δ is the constant 45-degree phase-shift and θ denotes a small variation in the angle difference between the two reference frames. Mapping the vector the complex plane gives

$$v_d^{PLL} + jv_q^{PLL} = (v_d^{grid} + jv_q^{grid})(\cos\delta - j\sin\delta)(\cos\theta + j\sin\theta) \tag{4.12}$$

Further linearizing (4.12) around the steady-state operating point give the small-signal representation of voltage d and q-components as

$$\begin{aligned} \hat{v}_d^{PLL} &= \frac{1}{\sqrt{2}}(\hat{v}_d^{grid} + \hat{v}_q^{grid} + V_d^{grid}\hat{\theta}) \\ \hat{v}_q^{PLL} &= \frac{1}{\sqrt{2}}(\hat{v}_d^{grid} + \hat{v}_d^{grid} + V_q^{grid}\hat{\theta}). \end{aligned} \tag{4.13}$$

The effective delay is approximated as half of the actual internal delay utilized in dqDSC-PLL, i.e., $T_1/16$. The loop gain has high gain due to the amplitude of the grid voltage. As it is given in (4.14) the loop gain is multiplied by $\sqrt{2}$ to include the effect of the grid voltage amplitude in the control design.

$$L_{PLL}^{dqADSC-PLL} = \frac{\sqrt{2}V_{gd}}{s} G_{PI}(s) e^{-\frac{T_1}{16}s} \tag{4.14}$$

The the performance of the dqADSC-PLL with the other DSC-based PLLs in mitigating the harmonic content of the grid-side current will be examined in Chapter 5. However, as will be shown in the next section, the improved DSC-based PLL is shown to reduce the settling time significantly compared to the existing methods, which makes it an attractive grid synchronization technique.

4.4 PLL Tuning

In this section the three PLLs presented are tuned in ordered to implement them in the simulation model MATLAB Simulink under different scenarios. Fig. 4.9 shows the loop gains given by the small-signal models (4.10) and (4.14). It is clear that the dqADSC-PLL yields twice higher bandwidth with the same phase margin as dqDSC-PLL.This is due to the smaller internal delay in DSC-block of the dqADSC-PLL.

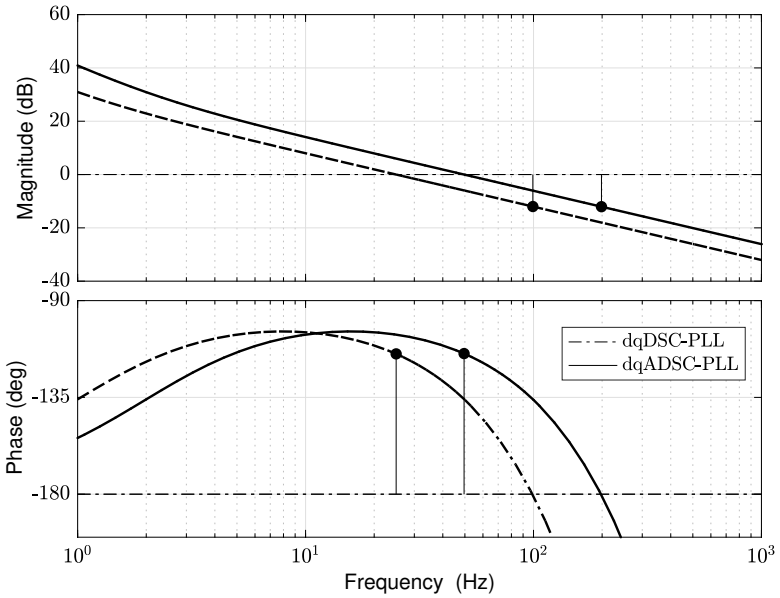


Figure 4.9. *Loop gains of the dqDSC (dotted) and dqADSC (solid) PLLs.*

Although, higher bandwidth PLL during grid disturbance is avoided in order to inject grid current with less current harmonic, the SRF-PLL and $\alpha\beta$CDSC-PLL were tuned to the same crossover frequency and phase margin as the improved delayed-signal cancellation (dqADSC-PLL) method to have a fair comparison. All the control parameters are given in Table 4.1.

Table 4.1. *PLL parameters.*

PLL	K_P	K_I	CF	T_{delay}
dqDSC-PLL	0.4823	3.0304	$25.0\ Hz$	$5\ ms$
dqADSC-PLL	0.6773	8.5114	$49.8\ Hz$	$2.5\ ms$
$\alpha\beta$DSC-PLL and SRF-PLL	0.8812	127.3503	$50.1\ Hz$	-

5 RESULTS AND PERFORMANCE EVALUATIONS

The aim of this chapter is to evaluate the performance of the two current-control techniques under different grid scenarios. To achieve this goal, the control techniques are implemented in MATLAB/Simulink environment using the parameters defined in Chapter 3. The scenarios examined are: distorted grid voltage, unbalanced grid voltage sag and dead-time effect. Moreover, during distorted and unbalanced grid voltage conditions the performance of the proposed delayed-signal cancellation PLLs are reviewed. To give a more general picture of the simulation results, a comparative analysis of grid current THD is presented. Finally, the experimental results are reviewed.

5.1 Distorted Grid Voltage

The performance of the current controllers under different grid conditions were examined with the control structures in Fig. 3.14 and 5.5 for synchronous and stationary reference frame, respectively.

The grid voltage is distorted with harmonics of order -5, +7, -11, and +13. The amplitude of these harmonics are given in Table 5.1. The values are the maximum allowed amplitudes of the harmonic components according to IEC 61000-3-2 and 61000-3-12 outline limits for harmonic emissions standards [54].

Table 5.1. *Grid voltage harmonic levels.*

Harmonic Order	Harmonic Voltage $\%$
5	6
7	5
11	3.5
13	3

In Fig. 5.1 is shown a grid voltage polluted with 5th, 7th, 11th and 13th harmonic components. The total harmonic distortion of the grid voltage in this test is about 9.07$\%$.

The grid current in LCL-type filter interfaced inverter can be easily distorted by grid voltage

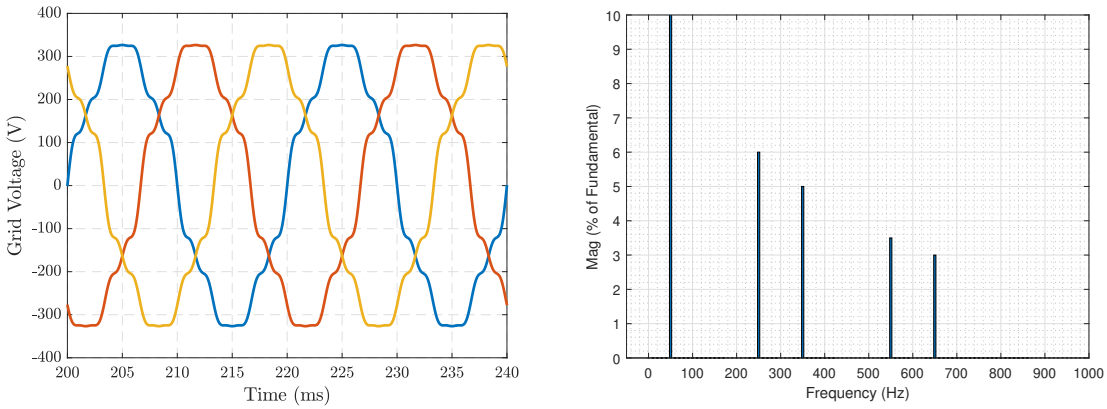
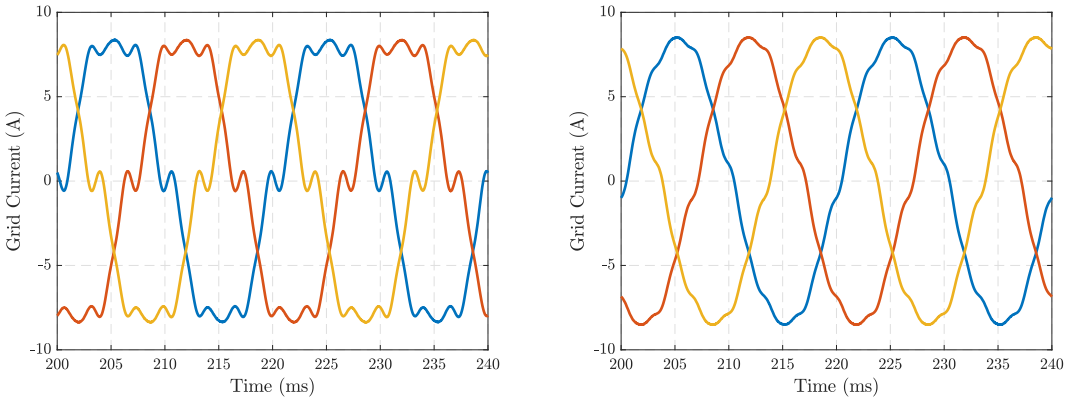


Figure 5.1. *Distorted grid voltage and its frequency component.*

harmonics, due to the low inductance feature of the filter. A proportional grid-voltage feedforward (GVFF) is shown to have effective harmonic attenuation when the LCL filter is considered as an L-type filter. However, in LCL filter interfaced inverter the inverter-side current feedback (ICF) can degrade the quality of the grid-side current especially under distorted grid voltage condition when the proportional GVFF in neglected.

In dq-control, the effect of the feedforward term is included in the simulation as it is shown in Fig. 3.14 to increase the output impedance of the inverter causing less harmonics in the current injected to the grid. Fig. 5.2 shows the grid-side currents with and without the effect of the proportional GVFF term. When the feedforward term defined in subsection (3.2.4) is activated, the grid current harmonic content reduced fro 14.61% to 4.24%.

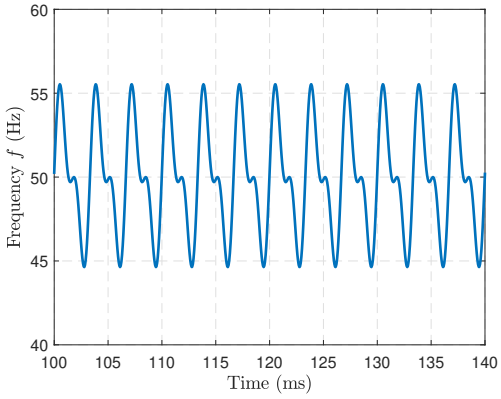


(a) *Without GVFF THD = 14.61%.* ***(b)*** *With GVFF THD = 4.24%.*

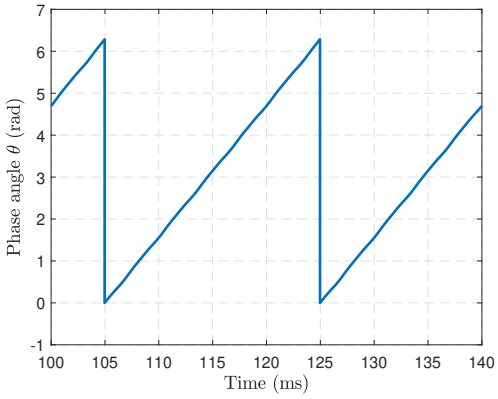
Figure 5.2. *Grid currents with and without GVFF.*

In order to obtain a better performance a synchronization method capable of accurately detecting the angle and frequency of utility grid should be used. According to Golestan and et al. [51], in a grid voltage polluted with harmonic orders of -5, +7, -11, and +13, a cascaded $\alpha\beta$DSC-PLL is shown to filter out the harmonics from affecting the PLL. This is realized by employing two cascaded $\alpha\beta$DSC12 (i.e., $T_1/12$) operators to block the first two harmonics and two cascaded $\alpha\beta$DSC24 (i.e., $T_1/24$) operators for the last two harmonic

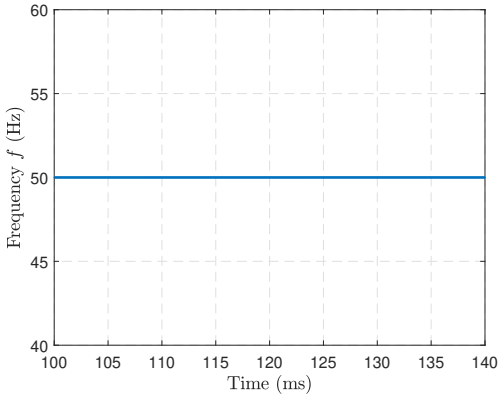
components, respectively.



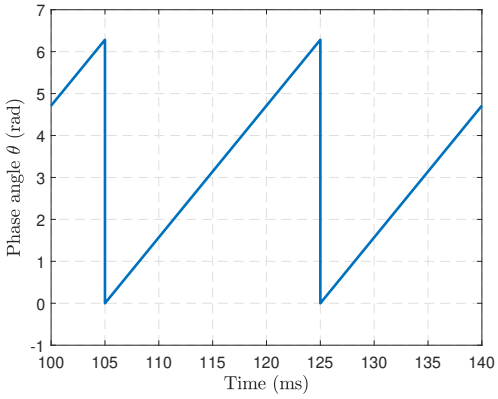
(a) *SRF-PLL.*



(b) *SRF-PLL.*



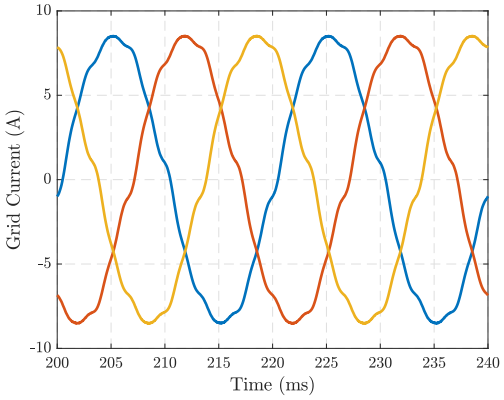
(c) $\alpha\beta$*CDSC-PLL*



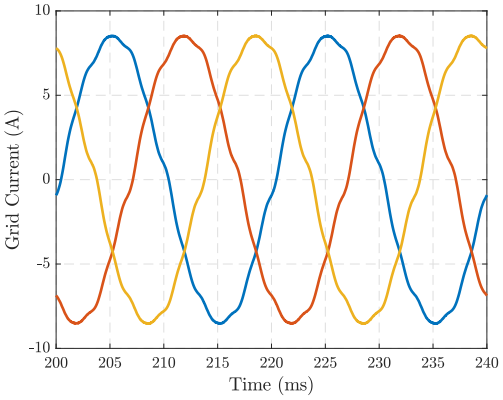
(d) $\alpha\beta$*CDSC-PLL*

Figure 5.3. *Simulation results from SRF-PLL and* $\alpha\beta$*CDSC-PLL.*

As shown in Fig. 5.3 a conventional PLL frequency (upper part) oscillates at the 6th and 12th harmonic. On the other hand, with the proposed $\alpha\beta$CDSC-PLL (lower part) neither the frequency nor output angle of the PLL experience oscillation.



(a) *SRF-PLL THD = 4.24%.*



(b) $\alpha\beta$*CDSC-PLL THD = 3.32%.*

Figure 5.4. *Grid currents with SRF-PLL and* $\alpha\beta$*CDSC-PLL.*

The obtained simulation results are shown in Fig. 5.4. It can be noticed that with the proposed PLL the current harmonic content reduced from 4.24% to 3.32%.

The simulations were also implemented in $\alpha\beta$-domain using PR controllers. Since the

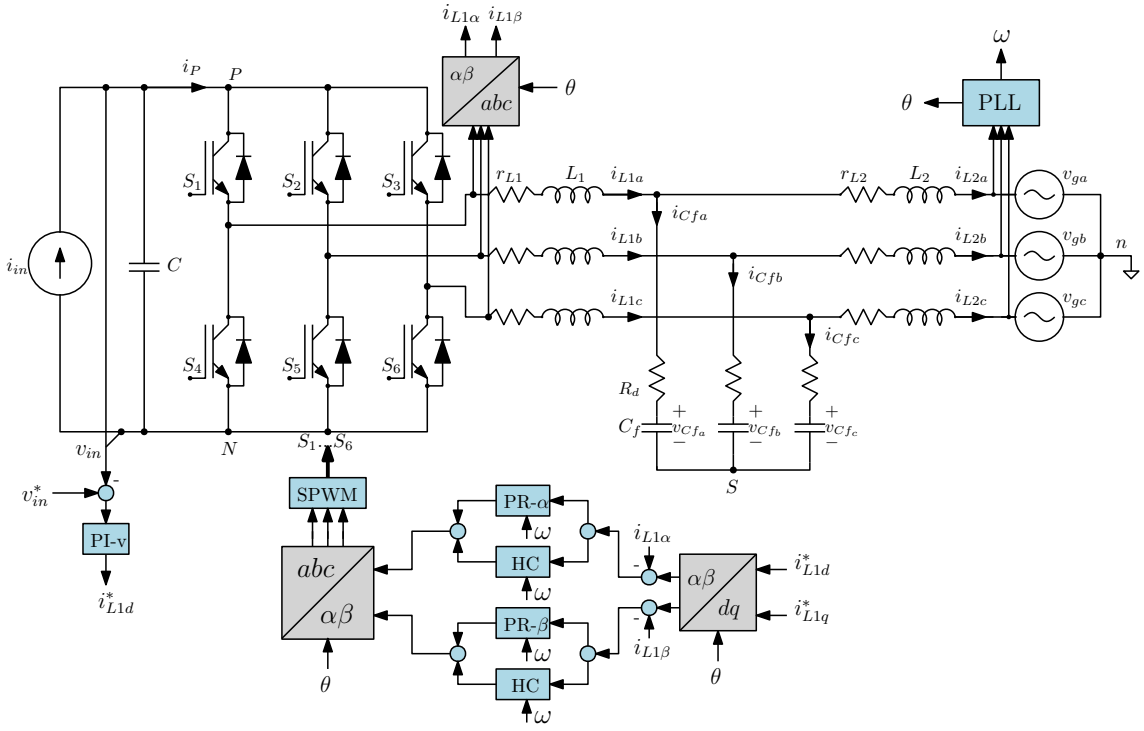
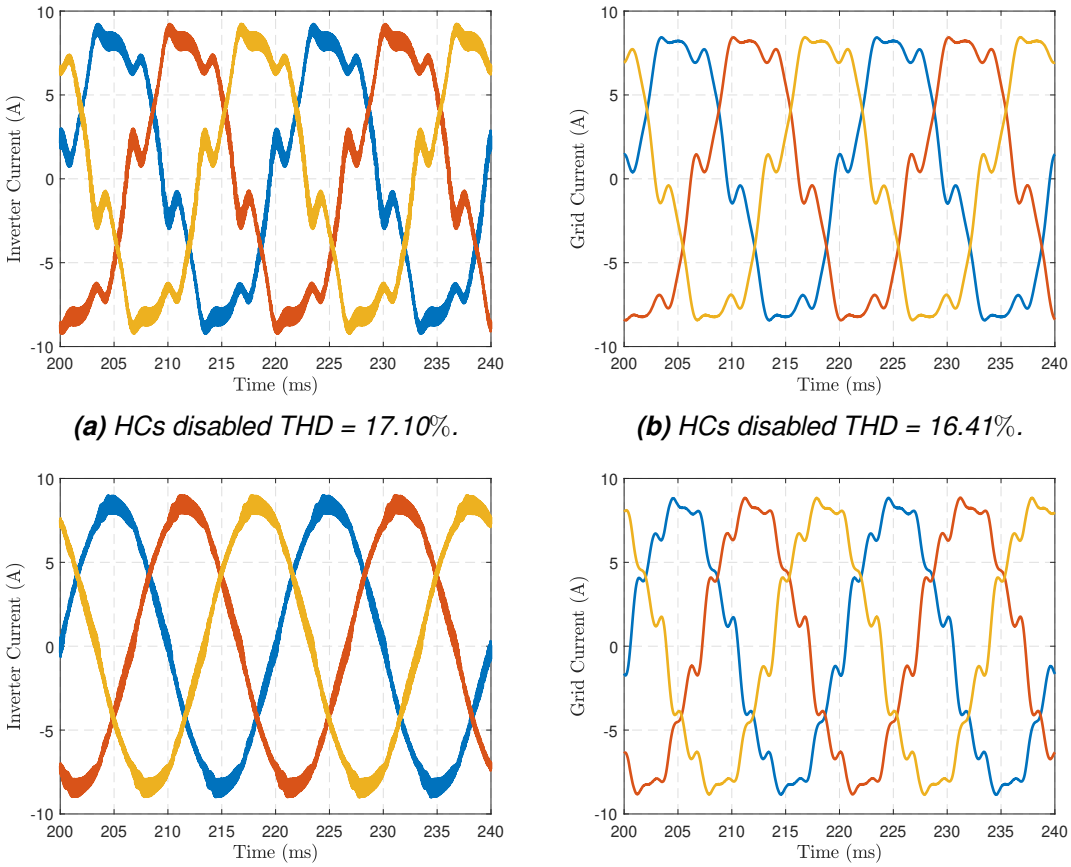


Figure 5.5. *Overview of the dq-control structure.*

PR controller operates at the fundamental frequency, the harmonic compensators were added to effectively compensate other frequencies that are critical from the grid point of view. Fig. 5.6 shows the simulation waveforms of the inverter and grid current when the HCs are enabled in the ICF control system. The differences are distinguishable for the inverter-side current. However, the HCs fail to mitigate the grid-side current distortions.

As it is clearly can be seen, the HCs improve the quality of both the inverter and grid-side currents. However, the inverter current shown in Fig. 5.6c has less harmonic components than the grid-side current Fig. 5.6d. It can be deduced from the figures, the inverter current contains no information of the harmonics from the grid-voltage, considering the controlled variable is the inverter-side current. Consequently, distorted grid current flows freely to the capacitor of the filter. Neither the harmonic compensators nor the PR controller is able to mitigate the harmonics from the grid-side current.

To overcome the issue above, a straightforward way is to make the current reference contain the full harmonic information by introducing a capacitor-current feedforward is proposed in the literature [15, 55]. The feedforward method is shown to effectively improve the grid-side current by generating infinite harmonic impedance at the working frequencies of the HCs. The working principle of the capacitor-current feedforward is the next subsection.



(a) *HCs disabled THD = 17.10%.*

(b) *HCs disabled THD = 16.41%.*

(c) *HCs enabled THD = 4.20%.*

(d) *HCs enabled THD = 11.15%.*

Figure 5.6. *PR controller with HCs.*

5.1.1 Capacitor-current feedforward

In distorted grid-voltage, a capacitor-current compensation generates infinite harmonic impedance. The idea is to adequately compensate the grid-side current by including the full capacitor-current in the ICF. This because the capacitor-current contains the harmonic information and the proposed method makes sure the ICF has all the harmonic information from the grid-side.

The implementation is utterly simple and does not require any extra sensor since the capacitor-current can be directly calculated from the capacitor voltage, which is also used for the grid synchronization. Therefore, the method can also be seen as cost-effective, because no capacitor-current measurement is required in the system.

The overview of grid-connected inverter LCL-type filter interfaced with capacitor-current compensation is depicted in Fig. 5.7. In the proposed scheme, the harmonic compensation loop is added to HCs to provide harmonic information from the grid side. Hence, the infinite impedance can only be introduced to HCs.

To generate the capacitor-current feedforward, a simple differentiator is proposed [15]. However, because traditional discretization method of the differentiator suffers from ei-

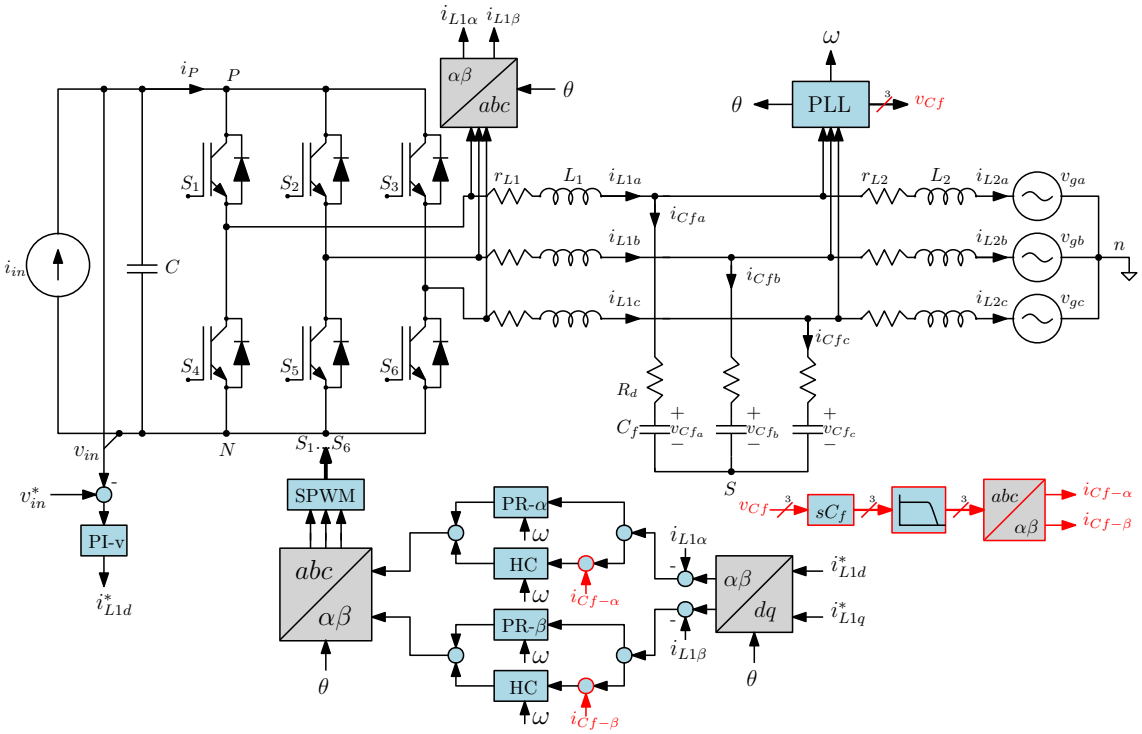
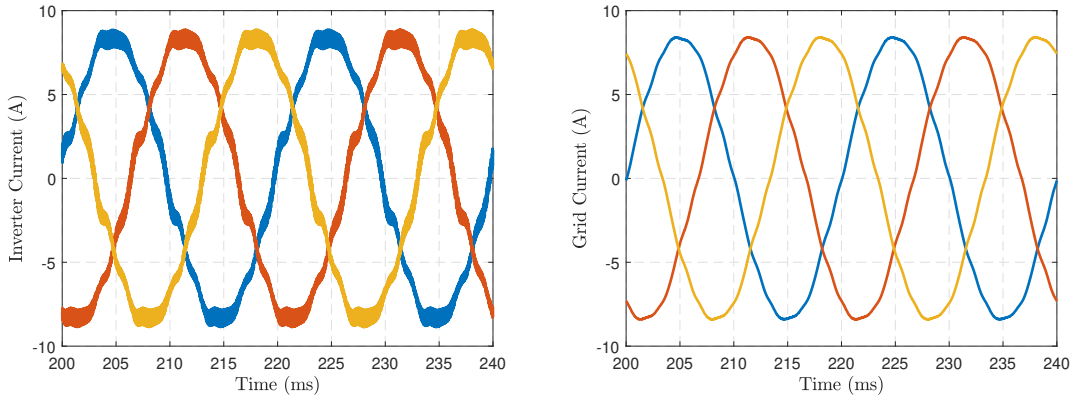


Figure 5.7. *Inverter with capacitor-current feedforward.*

ther large-phase error or noise amplification, a low pass filter is added to generate the capacitor-current feedforward. The optimum cutoff frequency for the low-pass filter, so that the feedforward term transfers the harmonic information is half of the switching frequency of the inverter, i.e., 5 KHz.

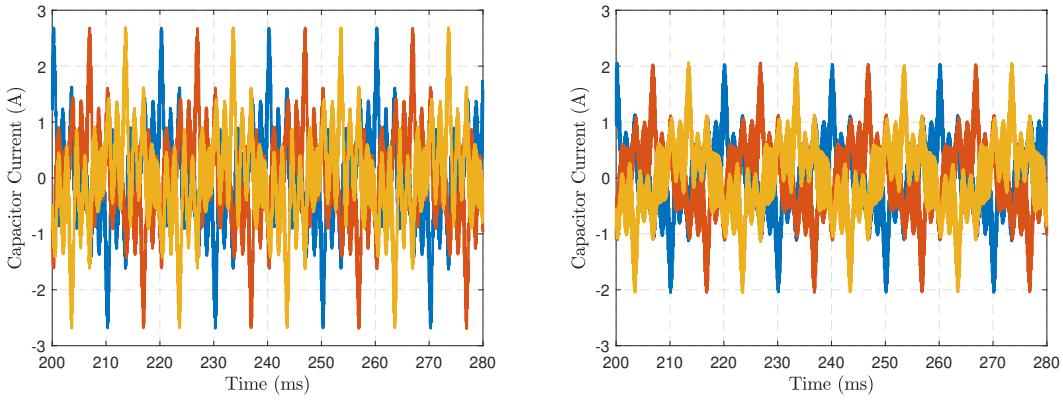


(a) *SRF-PLL THD = 5.66%.* ***(b)*** *SRF-PLL THD = 2.01%.*

Figure 5.8. *Simulation waveforms with capacitor-current feedforward.*

The simulation results with the proposed capacitor-current feedforward are shown in Fig. 5.8. Thanks to the proposed control, the grid-side current only contains slight low-order harmonics. It is seen from Fig. 5.8b that the THD of the grid current reduced from 10.04% to 2.01%. Moreover, as opposed to the inverter current in Fig. 5.6c, the inverter current in Fig. 5.8a has more harmonic components to be mitigated. In all, the effectiveness of the proposed method is shown to enhance the grid current quality.

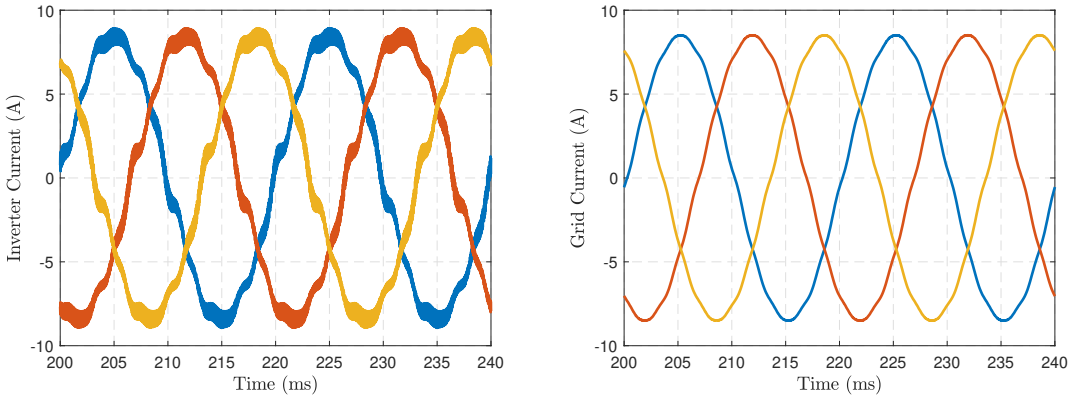
The current across the filter capacitor, when the inverter-side current is controlled by PR plus HCs and with the proposed capacitor-current feedforward are both shown in Fig. 5.9. Here, due to the information the ICF has, the harmonic content of the capacitor-current has reduced implying that the grid-side current has reduced as well.



(a) *Without capacitor-current feedforward.* ***(b)*** *With capacitor-current feedforward.*

Figure 5.9. *Filter capacitor-current.*

It must be mentioned that, in order to obtain a good performance of the adaptive-frequency PLL, the simulation was carried-out using $\alpha\beta$CDSC-PLL. As shown in Fig. 5.10b the grid-side current THD reduced from 2.01% to 1.43%.



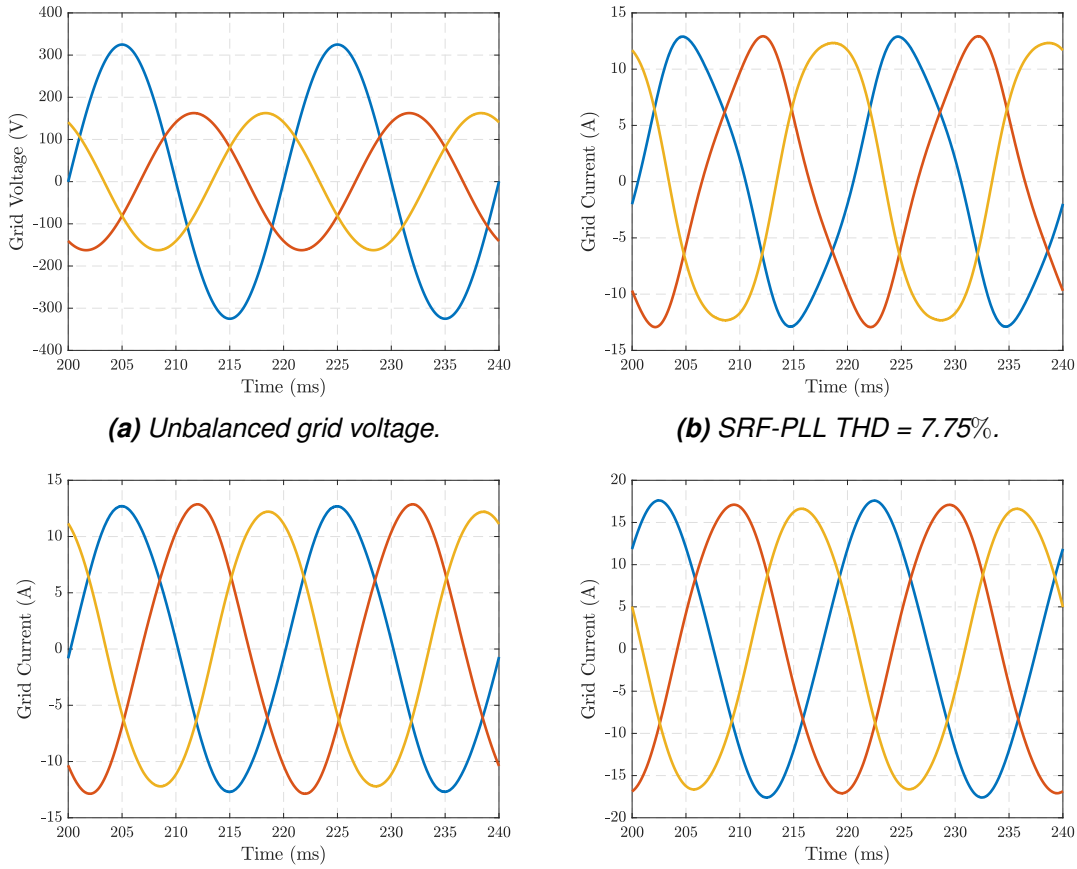
(a) *$\alpha\beta$CDSC-PLL THD= 6.33%.* ***(b)*** *$\alpha\beta$CDSC-PLL THD = 1.43%.*

Figure 5.10. *Grid currents with $\alpha\beta$CDSC-PLL.*

5.2 Unbalanced Grid Voltage sag

In order to demonstrate the robustness of the proposed current-control strategies, the simulations were also carried out under unbalanced grid voltage sag. The inverter operates in an unbalanced case where phase b and c amplitudes are reduced by 50%. The obtained results are shown in Fig. 5.11. In unbalanced grid voltage the SRF-PLL deteriorates the dynamic performance of the current controller, thus, increases the harmonic content of the grid current. To overcome this issue, a dqDSC-PLL is proposed in multiple works of literature as it is pointed out in Chapter 4.

The simulation results represented in Fig. 5.11d show that the proposed improved dqADSC-PLL can handle the unbalanced grid voltage. A grid current with less THD is achieved, which is much better than the conventional SRF-PLL shown in Fig. 5.11b. A conventional dqDSC-PLL shown to reduce the harmonic content of the grid current from 7.75% to 2.24%, which close to the performance offered by improved dqADSC-PLL (2.18%).



(a) *Unbalanced grid voltage.*

(b) *SRF-PLL THD = 7.75%.*

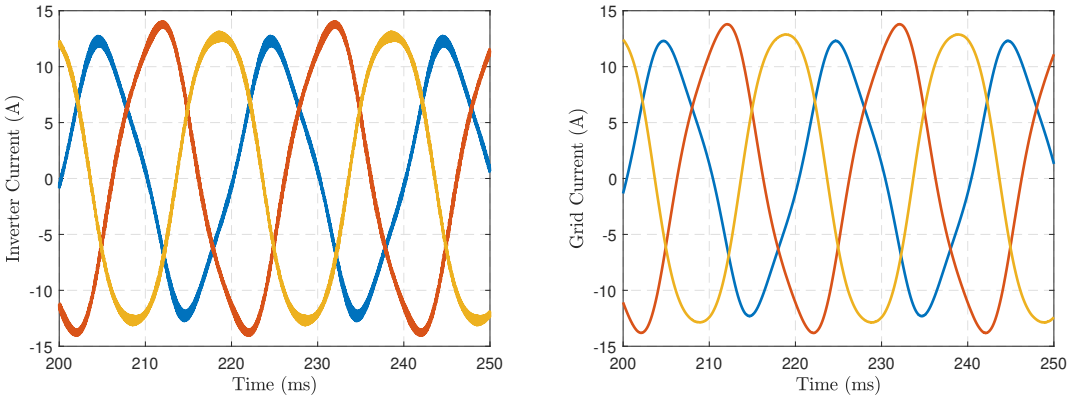
(c) *dqDSC-PLL THD = 2.24%.*

(d) *Improved dqADSC-PLL THD = 2.18%.*

Figure 5.11. *Grid currents with SRF-PLL and CDSC-PLL.*

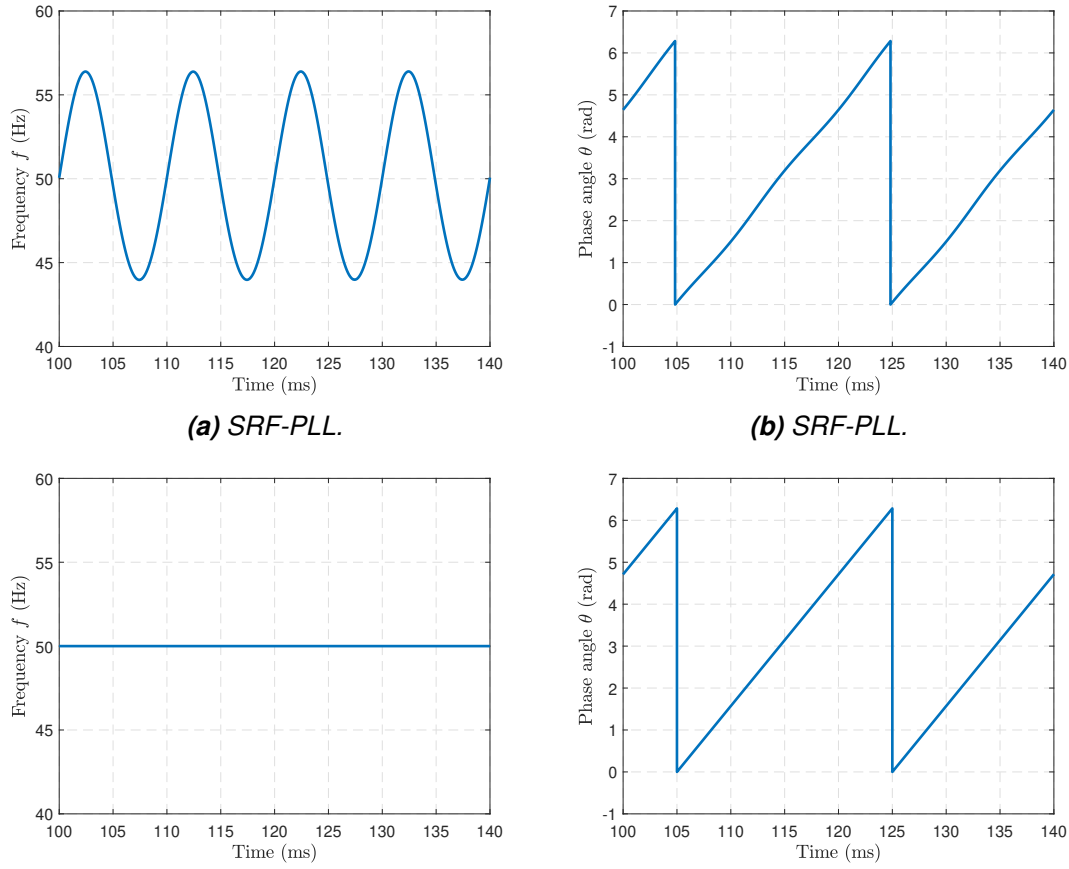
With the improved dqADSC-PLL the grid current contains much less third harmonic, which reduced from 7.75% to 2.18%. The remaining third harmonic is due to the dc-voltage control. This is due to the fact that capacitors make existing harmonics more visible.

In $\alpha\beta$-domain current control, the simulated wave forms using PR controller are shown in Fig. 5.12b. The grid-side current waveform is greatly distorted, thus, something has be done to keep the harmonic content below what grid-tied systems standards recommend.



(a) *SRF-PLL THD = 9.16%.* ***(b)*** *SRF-PLL THD = 9.06%.*

Figure 5.12. *Simulation results from PR-controller with 3rd HC.*



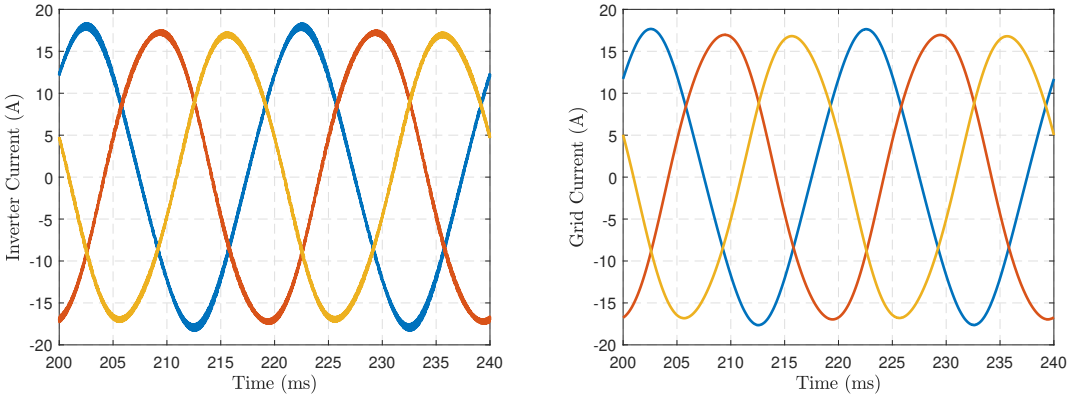
(a) *SRF-PLL.* ***(b)*** *SRF-PLL.*

(c) *dqADSC-PLL* ***(d)*** *dqADSC-PLL*

Figure 5.13. *Simulation results from SRF-PLL and dqADSC-PLL.*

Fig. 5.13 shows the grid frequency with conventional PLL (upper part) and proposed

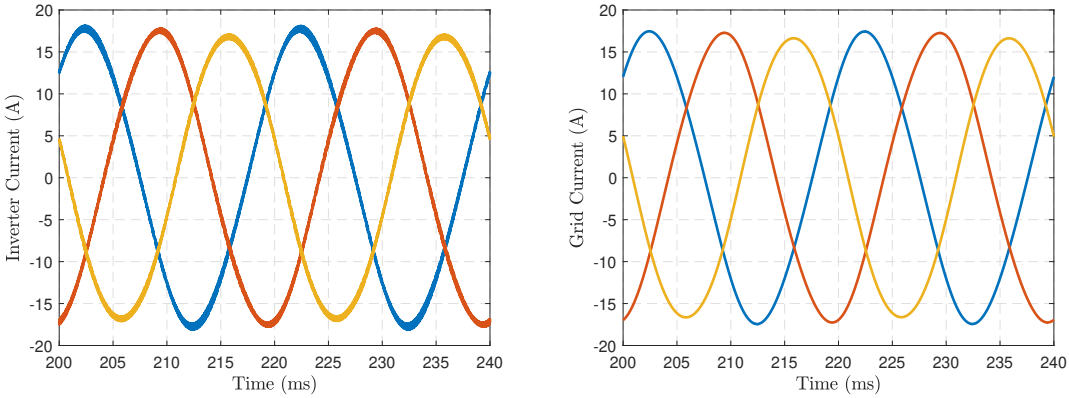
dqADSC-PLL (lower part) when the grid voltages are unbalanced. The conventional PLL experiences large oscillation at the second harmonic which subsequently distorts the output angle of the PLL. However, the proposed PLL is free of the oscillation.



(a) *Improved dqADSC-PLL THD = 2.69%.* ***(b)*** *Improved dqADSC-PLL THD = 2.46%.*

Figure 5.14. *Simulation results from PR-controller with improved dqADSC-PLL.*

Grid voltage unbalance is seen as 3rd harmonic in the grid current. Consequently, introducing a 3rd harmonic compensator to the PR controller and changing the SRF-PLL to the proposed improved dqADSC-PLL further reduces the grid current THD to 1.75% as it is evidenced from Fig. 5.15.



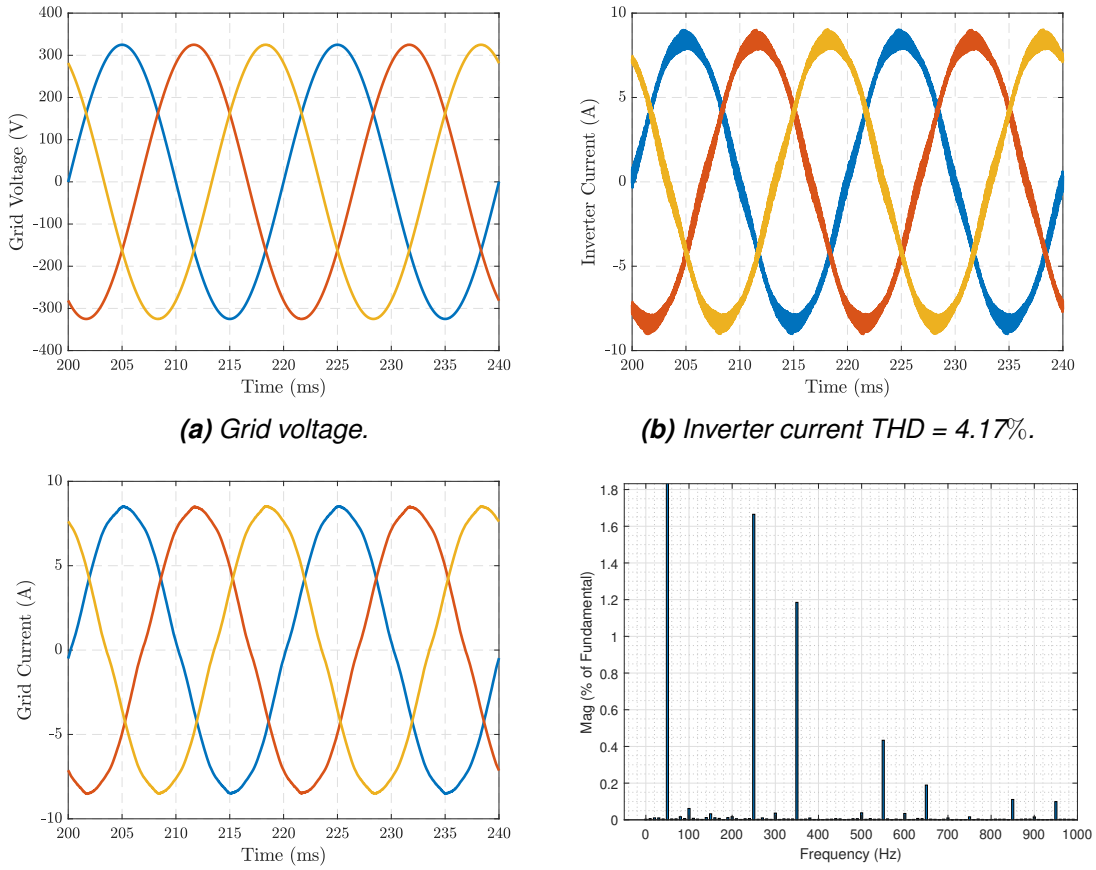
(a) *Improved dqADSC-PLL THD = 2.15%.* ***(b)*** *Improved dqADSC-PLL THD = 1.75%.*

Figure 5.15. *Simulation results from PR+HC with improved dqADSC-PLL.*

5.3 Dead-time effect

In most modulation techniques proposed in the literature, it is assumed that the semiconductor switches operate in an ideal manner. Thus, the upper and lower switches of the inverter leg turn on and off at the exact same time instants. In real applications, however, to prevent short-circuiting, the inverter legs due to non-ideal fall and conduction overlap, a small delay is added to the switch control logic. This time delay guarantees safe operation, by not allowing the lower and upper switches conducting simultaneously [56].

Since time delay is applied at every switching instants, it affects the performance of the inverter by decreasing the injected current quality (i.e., increasing the low-order harmonics). As it is pointed out in [57], a dead-time effect is added either in the hardware drivers of the semiconductor switches (i.e., IGBTs) or in the PWM scheme. In the simulations, the latter technique is utilized by applying $1\mu s$ delay time at the upper switches of the inverter.



(a) *Grid voltage.*

(b) *Inverter current THD = 4.17%.*

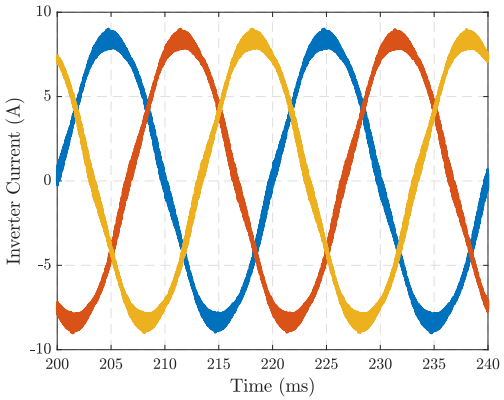
(c) *Grid Current THD = 2.10%.*

(d) *Grid current frequency component.*

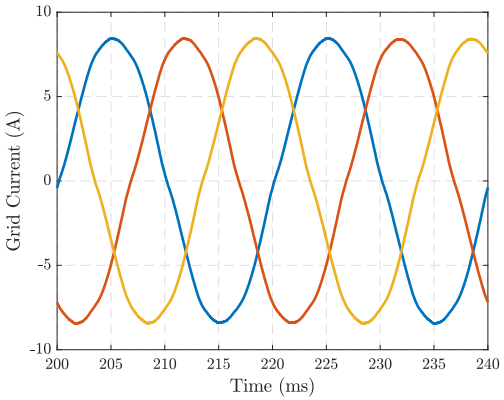
Figure 5.16. *Current-control in dq-domain with dead-time effect.*

The control bandwidth of the current controller in dq-domain affects the quality of the grid-side current. Higher current-control bandwidth reduces the harmonic content of the grid current as shown in Fig. 5.17. As it is evidenced from the THD of both the inverter and

grid current increased slightly as control bandwidth of the current-control reduced from 227 Hz to 150 Hz. Notice the grid voltage, in this case, is kept pure sinusoidal. ICF control system makes sure the grid current is free of distortion as long as the low-order harmonics have been eliminated from the inverter current before flowing into the grid.

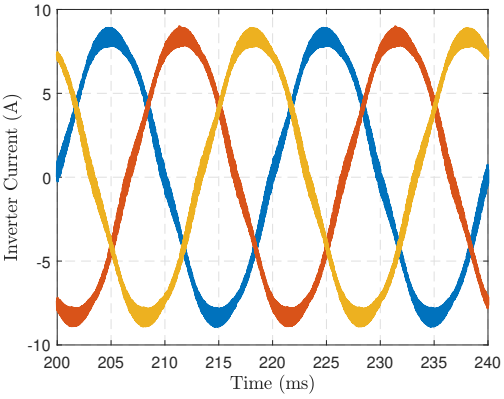


(a) *Inverter Current THD = 4.34 %.*

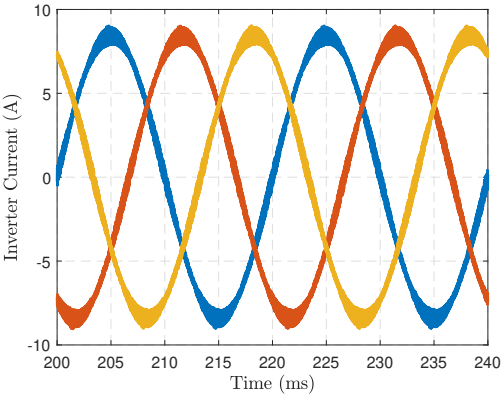


(b) *Grid Current THD = 2.52 %.*

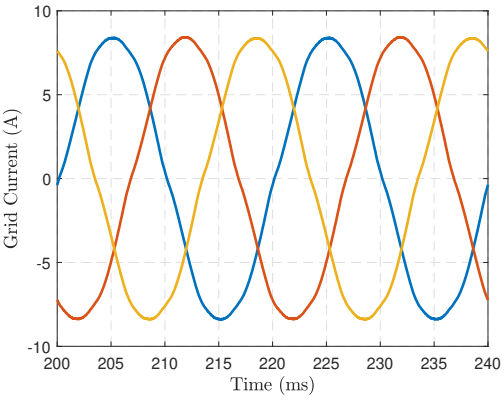
Figure 5.17. *Current-control in dq-domain with dead-time effect with lower bandwidth.*



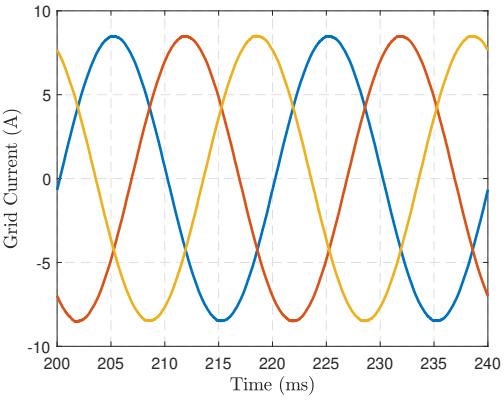
(a) *Inverter current without HCs THD= 4.49%.*



(b) *Inverter current with HCs THD= 3.76%.*



(c) *Grid current without HCs THD= 2.88%.*



(d) *Grid current with HCs THD= 0.21%.*

Figure 5.18. *current-control in $\alpha\beta$-domain with dead-time effect.*

As it is visualized in the simulation results of both PI and PR-control without HCs have

almost the same current harmonics reduction performance, the PI based current-control being a slightly better. Fig. 5.16 shows the results from current-control techniques in dq-domain. Here, the the THD of the grid current is 2.11%. Similarly, the results from the current-control in $\alpha\beta$-domain is depicted in Fig. 5.18. As it ca be clearly evidenced form the figure adding HCs to the PR control reduces the harmonic content significantly. Thanks to the HCs the THD of the grid current has reduced from 2.88% to 0.22%.

5.4 Comparative Analysis of the Grid Current THD

To give a more general comparison to the current-control techniques and the proposed grid synchronization techniques, the THD of the grid current under different scenarios are presented in Table 5.2. Notice also that the pure grid voltage condition is added here for a comparison. As it can be deduced from the THD values, the current-control techniques in both domains performed quite similarly in ideal grid voltage condition.

In distorted grid voltage case, the current-control in $\alpha\beta$-domain provided better results. however, merely PR+HCs suffered majorly from the harmonic distortion of the grid voltage. Hence, a capacitor-current feedforward must be utilized to inject pure sinusoidal current to the grid. Moreover, the use of $\alpha\beta$CDSC-PLL reduced the THD of the grid current in both current-control techniques.

Table 5.2. *Case studies and harmonic mitigation performance of the control techniques.*

Case study/ Controller	PI	PR	PR + HC	PR + HC + CCFFD
Pure Grid	0.08%	0.15%	0.15%	0.15%
Distorted Grid (SRF-PLL)	4.24%	16.41%	11.15%	2.01%
Distorted Grid ($\alpha\beta$CDSC-PLL)	3.32%	16.20%	9.14%	1.43%
Unbalanced Grid (SRF-PLL)	7.75%	9.06%	5.54%	-
Unbalanced Grid (dqADSC-PLL)	2.18%	2.42%	1.75%	-
Dead-time effect	2.10%	2.88%	0.21%	0.20%

In unbalanced grid voltage sag condition, the THD of the grid-current is less in dq-domain ICF when the grid synchronization utlized is SRF-PLL. A grid voltage unbalance is seen as 3rd harmonic in grid-side current. As a result, adding a 3rd harmonic compensator to the PR controller and utlizing dqADSC-PLL the harmonic content of the grid current reduced significantly with both current-control techniques.

When it comes to the dead-time effect scenario, the current-control in dq-domain offered the THD of the grid current is 2.10%. With merely PR controller in $\alpha\beta$-domain gave a THD of 2.88%. However, with the addition of harmonic compensators, the harmonic content reduced to 0.21%.

In all the scenarios examined, the current-control in $\alpha\beta$-domain using a PR controller with HCs provided better results in mitigating the THD of the grid-side current. This is due to the infinite impedance harmonic impedance provided by the HCs. Moreover, the capacitor-current feedforward in $\alpha\beta$-domain, which is equivalent to proportional grid-voltage feedforward in dq-domain must be used to give the ICF the full information of the grid side voltage.

All in all, the PR-based current-control techniques mitigated the low-order harmonics better. This can evidently be proved from the results provided in the table. Moreover, the delayed-signal cancellation based PLLs further attenuated the harmonic content of the grid-side current.

5.5 Experimental Results

In the laboratory, the operation of designed parameters for both dq-control and $\alpha\beta$-control are verified. The test bench that would enable to authenticate a three-phase converter model and control of an induction motor is shown in Fig. 5.19. The test bench is based on a real-time simulator dSPACE that supports the use of MATLAB Simulink and accessed from a PC. After loading the control system into the memory of the dSPACE, the parameters, for instance, the dc-voltage reference can be modified online using the Control Desk - program on the PC.

Figure 5.19. *Laboratory measurement setup.*

The laboratory test bench includes two 2.2 kW induction motors, two active three-phase two-level converters (four converters with diode bridges) and passively damped LCL-filter in the grid-side. The setup also includes measurement circuits for the grid converter, motor control and multiple components. The converters may operate as rectifier or in-

verter depending on the operation region of the motor. However, in default case, the grid-side converter operates as a rectifier and the motor side converter as an inverter that inverts the dc-link voltage to three-phase voltages to rotate the motor. The motor, which is controlled by a separate converter, has been used as a load for the converter and the amount of load current is regulated by adjusting the load torque of the electrical motor. In this thesis, the operation of the induction motor model and its control are omitted and understanding the operation principle of the active rectifier is the main focus.

In the simulation model, the dc-voltage controller is designed to have a bandwidth of 20 Hz with a phase margin 65 degrees, which is shown to have to ensure a stable operation. Similarly, the inner current controller loop was designed to have a bandwidth well below the resonance frequency in order to have a stable operation. In the laboratory measurements, however, the presence of startup transient would not allow the current controller to follow reference coming from the dc-voltage controller effectively. Thus, it was required to increase the crossover frequency of the current controller to have a bandwidth of 400Hz. This can be achieved easily by increasing the proportional gain of the current controller (i.e., K_p = 0.0531).

As shown in Fig. 5.20 the grid current contains excessive harmonics due to two main reasons. The first is that the dead-time effect due to the converters in the setup increases the harmonic distortion. Moreover, the converters are operating at partial load since the loads (motors) demand less power than the rated power of the converters. The rated power of the rectifier is 10 kW, whereas the rated power of the motors as already mentioned are 2.2 kW.

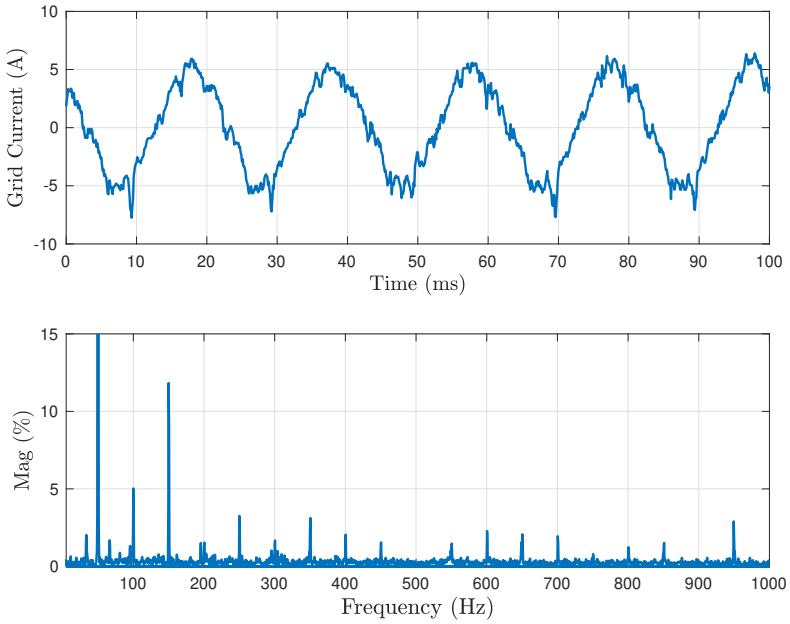


Figure 5.20. *Grid current and FFT with PI-control.*

The step response performance of the designed controller parameters in the synchronous

reference frame was tested. As shown in Fig. 5.21 the the cascaded control scheme is tested with a step change in the dc-link voltage from 600 to 650 V. The controller reacted to the step change very vast and it took less than 12 ms for the control system to reach to the new steady-state value. The grid current experienced the dc-link voltage step, but it did not became unstable.

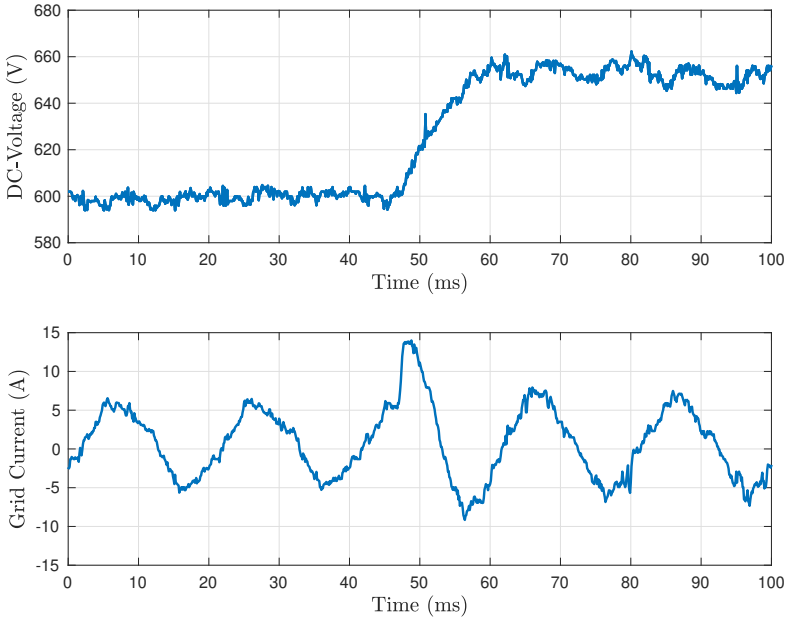


Figure 5.21. *A step change in dc-voltage from 600-650V with PI-control.*

The same testes were also carried out using adaptive PR-controller in $\alpha\beta$-domain. Like

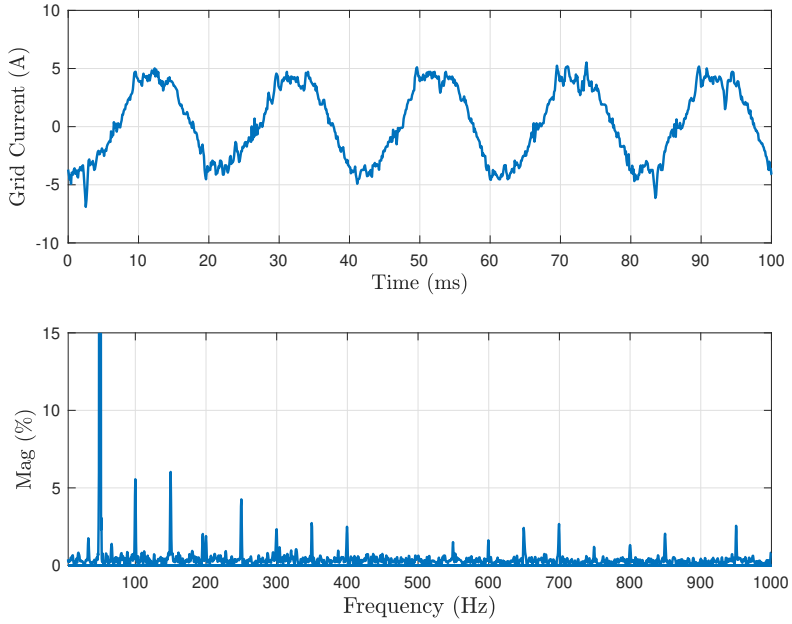


Figure 5.22. *Grid current and FFT with PR-control.*

the control scheme in current-control in dq-domain the cascaded control scheme worked as it should and the harmonic content the grid side current is less affected. The response obtained from the step rest is also better, the control system settles to its new reference frame faster.

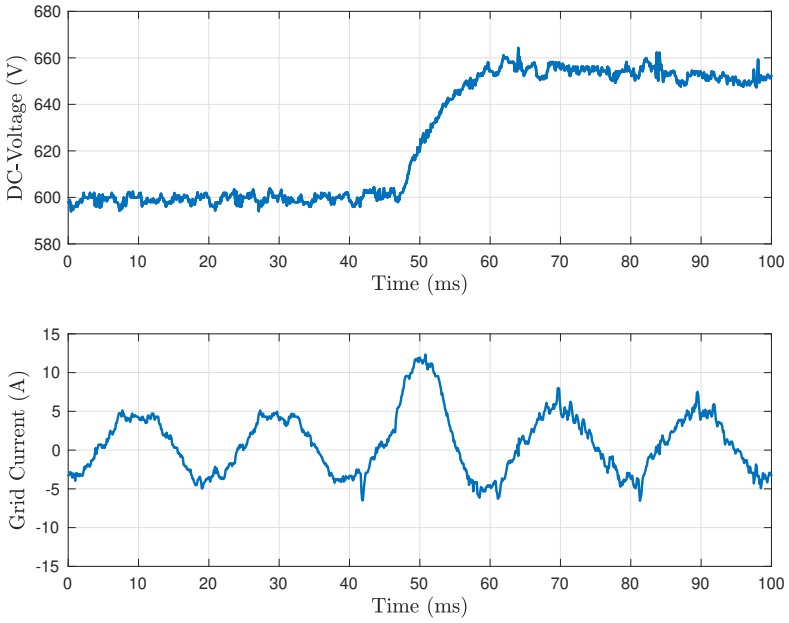


Figure 5.23. *A step change in dc-voltage from 600-650V with PR-control.*

The laboratory results from all the PLLs proposed in this thesis are provided in Appendix C. The enhancement made by the delayed signal cancellation based PLLs is almost invisible since the grid voltage has quite a small 5th and 7th harmonics. However, all the PLLs worked perfectly in synchronizing the grid voltage with the current produced by the inverter. Moreover, the effectiveness of the capacitor-current feedforward method for harmonic mitigation could not be verified in the laboratory since measuring the capacitor voltage is not possible in the laboratory setup. The effectiveness of the method will not be easy to witness due to the presence of nonidealities and the cleanness of the grid voltage.

6 CONCLUSION

The integration of renewable energy sources in distributed power generation is increasing. Inverters play an important role in coupling these sources with the utility grid. As a result, the number of grid-connected converters is increasing as well. Hence, reducing the harmonic content of the grid voltages and currents between the renewable energy source and the utility grid has become an important research area. The inverter should be able to produce current with less THD as possible even in the presence of distorted grid voltage, unbalanced grid voltage sag and dead-time effect. According to IEEE 1547 standards, the total harmonic distortion of the grid current shall be less than 5$\%$.

The aim of this thesis was to investigate the resonance phenomena observed in grid-connected inverters and the techniques utilized to suppress them. The thesis evaluated the performance of two current-control techniques under different grid voltage scenarios. The current-control techniques were proportional-integral (PI) controllers in dq-domain and proportional-resonant (PR) controllers in $\alpha\beta$-domain. To achieve this goal the control techniques were implemented in MATLAB/Simulink environment using designed parameters. The thesis also examined the enhancement made by proportional grid-voltage feedforward and capacitor-current feedforward terms in increasing the output impedance of the inverter. Thus, improve the harmonic-rejection-ability of the control system in a weak-grid condition. Moreover, during distorted and unbalanced grid voltage conditions the enhancement made by delayed-signal cancellation PLLs are tested. To have a fair comparison, each PLL is tuned to have the same bandwidth.

The simulation results validated that under different scenarios, the harmonic content of the grid-side current is kept below what standards recommend in both dq- and $\alpha\beta$-domains. In addition, the results obtained from the simulations correlated with what has been discovered in the past. These results tie well with previous studies wherein, the feedforward terms in both domains showed an excellent performance in suppressing the low-order harmonics from the current. Some crucial differences in the performances of the current-control techniques were also observed. PR+HCs provided better results than PI-based current controllers in mitigating low-order harmonic distortions from the grid-side current as have been observed in many works of literature. It has also been verified that using dqADSC-PLL and $\alpha\beta$CDSC-PLL current harmonic distortions were further reduced.

Finally, the operation of the designed current controllers were verified with a test bench that enables to authenticate a three-phase converter model and control of an induction

motor. Current-control methods in both domains worked well, even though, there were excessive harmonics observed in the grid-side current. The nonidealities such as partial loading and dead-time effects of the converters are the primary sources for the distortions observed. Despite the limitations, results from the laboratory provided evidence on the performance of current-control techniques in $\alpha\beta$-domain. The PR-controller mitigated current distortions better by reducing the harmonic content of the grid-side current.

The grid voltage in the laboratory is less affected by grid voltage distortion and unbalance. Hence, it turned out to be nearly impossible to see the improvements made by delayed-signal cancellation based grid synchronization techniques. With a better test bench, where also network emulator is used to create grid voltage distortion and unbalance, the feedforward terms and current-control techniques with the advanced PLLs could be validated. However, with the used setup, students can now design and test the operation of current-control techniques in dq- and $\alpha\beta$-domains on their converters design related courses.

Future studies could investigate the association between the quality of the current produced by inverters and AD-conversions. That is due to the fact that modern control schemes, for the most part, are implemented using digital controllers. Moreover, external expensive current sensing probes are utilized in the laboratory measurements. Thus, deployment of already installed current measurement units and their compensation can be one of the future works.

BIBLIOGRAPHY

[1] B. K. Bose. Global Warming: Energy, Environmental Pollution, and the Impact of Power Electronics. *IEEE Industrial Electronics Magazine* 4.1 (Mar. 2010), 6–17.

[2] T. Suntio, T. Messo, A. Aapro, J. Kivimäki and A. Kuperman. Review of PV Generator as an Input Source for Power Electronic Converters. English. *Energies* 10.8 (2017), 1076.

[3] B. K. Bose. Global Energy Scenario and Impact of Power Electronics in 21st Century. *IEEE Transactions on Industrial Electronics* 60.7 (July 2013), 2638–2651.

[4] L. Nousiainen, J. Puukko, A. Mäki, T. Messo, J. Huusari, J. Jokipii, J. Viinamäki, D. T. Lobera, S. Valkealahti and T. Suntio. Photovoltaic Generator as an Input Source for Power Electronic Converters. English. *IEEE Transactions on Power Electronics* 28.6 (2013), 3028–3038.

[5] F. Blaabjerg and S. B. Kjaer. Power electronics as efficient interface in dispersed power generation systems. *IEEE Transactions on Power Electronics* 19.5 (Sept. 2004), 1184–1194.

[6] R. Teodorescu, M. Liserre, P. Rodriguez and I. Books24x7. *Grid Converters for Photovoltaic and Wind Power Systems*. English. US: Wiley-IEEE Press, 2010;2011.

[7] A. Timbus, M. Liserre, R. Teodorescu, P. Rodriguez and F. Blaabjerg. Evaluation of Current Controllers for Distributed Power Generation Systems. English. *IEEE Transactions on Power Electronics* 24.3 (2009).

[8] D. Kumar and F. Zare. Harmonic Analysis of Grid Connected Power Electronic Systems in Low Voltage Distribution Networks. English. *IEEE Journal of Emerging and Selected Topics in Power Electronics* 4.1 (2016), 70–79.

[9] Z. Chen and E. Spooner. Grid power quality with variable speed wind turbines. *IEEE Transactions on Energy Conversion* 16.2 (June 2001), 148–154.

[10] S. W. Mohod and M. V. Aware. Grid Power Quality with Variable Speed Wind Energy Conversion. *2006 International Conference on Power Electronic, Drives and Energy Systems*. Dec. 2006, 1–5.

[11] J. Xu, S. Xie and T. Tang. Active Damping-Based Control for Grid-Connected LCL -Filtered Inverter With Injected Grid Current Feedback Only. *IEEE Transactions on Industrial Electronics* 61.9 (Sept. 2014), 4746–4758.

[12] X. Wei, L. Xiao, Z. Yao and C. Gong. Design of LCL filter for wind power inverter. English. IEEE, 2010, 1–6.

[13] N. F. Guerrero-Rodríguez, A. B. Rey-Boué and E. Reyes-Archundia. Overview and comparative study of two control strategies used in 3-phase grid-connected inverters for renewable systems. English. *Renewable Energy Focus* 19-20 (2017), 75–89.

[14] A. J. Xu, B. S. Xie, C. J. Kan and D. L. Ji. An improved inverter-side current feedback control for grid-connected inverters with LCL filters. *2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*. June 2015, 984–989.

[15] Z. Xin, P. Mattavelli, W. Yao, Y. Yang, F. Blaabjerg and P. C. Loh. Mitigation of Grid-Current Distortion for LCL-Filtered Voltage-Source Inverter With Inverter-Current Feedback Control. *IEEE Transactions on Power Electronics* 33.7 (July 2018), 6248–6261.

[16] S. Golestan, F. D. Freijedo, A. Vidal, A. G. Yepes, J. M. Guerrero and J. Doval-Gandoy. An Efficient Implementation of Generalized Delayed Signal Cancellation PLL. *IEEE Transactions on Power Electronics* 31.2 (Feb. 2016), 1085–1094.

[17] P. Rodriguez, J. Pou, J. Bergas, J. I. Candela, R. P. Burgos and D. Boroyevich. Decoupled Double Synchronous Reference Frame PLL for Power Converters Control. *IEEE Transactions on Power Electronics* 22.2 (Mar. 2007), 584–592.

[18] M. Rasheduzzaman and J. Kimball. Modeling and Tuning of an Improved Delayed-Signal-Cancellation PLL For Microgrid Application. *IEEE Transactions on Energy Conversion* (2018).

[19] T. Messo, J. Sihvo, D. Yang, X. Wang and F. Blaabjerg. Improved delayed signal cancellation-based SRF-PLL for unbalanced grid. *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*. Oct. 2017, 3103–3110.

[20] T. Suntio, T. Messo and J. Puukko. *Power electronic converters: dynamics and control in conventional and renewable energy applications*. English. Weinheim: Wiley-VCH, 2017.

[21] T. Geyer. *Model Predictive Control of High Power Converters and Industrial Drives*. English. Wiley, 2016.

[22] J. Puukko, T. Messo and T. Suntio. Effect of phoptovoltaic generator on a typical VSI-based three-phase grid-connected photovoltaic inverter dynamics. English. (2011).

[23] M. Liserre, F. Blaabjerg and S. Hansen. Design and control of an LCL-filter-based three-phase active rectifier. English. *IEEE Transactions on Industry Applications* 41.5 (2005), 1281–1291.

[24] T. Messo, J. Jokipii, A. Makinen and T. Suntio. Modeling the grid synchronization induced negative-resistor-like behavior in the output impedance of a three-phase photovoltaic inverter. English. IEEE, 2013, 1–7.

[25] A. Aapro, T. Messo, T. Roinila and T. Suntio. Effect of Active Damping on Output Impedance of Three-Phase Grid-Connected Converter. *IEEE Transactions on Industrial Electronics* 64.9 (Sept. 2017), 7532–7541.

[26] A. Aapro. Factors in active damping design to mitigate grid interaction in three-phase grid-connected photovoltaic inverters. English. PhD thesis. 2017.

[27] M. Parvez, M. F. M. Elias, N. A. Rahim and N. Osman. Current control techniques for three-phase grid interconnection of renewable power generation systems: A review. English. *Solar Energy* 135 (2016), 29–42.

[28] M. P. Kazmierkowski and L. Malesani. Current control techniques for three-phase voltage-source PWM converters: a survey. *IEEE Transactions on Industrial Electronics* 45.5 (Oct. 1998), 691–703.

[29] J. Scoltock, T. Geyer and U. K. Madawala. Model Predictive Direct Power Control for Grid-Connected NPC Converters. *IEEE Transactions on Industrial Electronics* 62.9 (Sept. 2015), 5319–5328.

[30] J. Rodriguez, M. P. Kazmierkowski, J. R. Espinoza, P. Zanchetta, H. Abu-Rub, H. A. Young and C. A. Rojas. State of the Art of Finite Control Set Model Predictive Control in Power Electronics. English. *IEEE Transactions on Industrial Informatics* 9.2 (2013), 1003–1016.

[31] IEEE Recommended Practice for Utility Interface of Photovoltaic (PV) Systems. *IEEE Std 929-2000* (Jan. 2000), 26.

[32] T. M. Blooming and D. J. Carnovale. Application of IEEE STD 519-1992 Harmonic Limits. *Conference Record of 2006 Annual Pulp and Paper Industry Technical Conference*. June 2006, 1–9.

[33] S. Kumar Peddapelli. *Pulse Width Modulation: Analysis and Performance in Multilevel Inverters*. English. Berlin: De Gruyter Oldenbourg, 2016;2017;

[34] D. G. Holmes and T. A. Lipo. *Pulse Width Modulation for Power Converters: Principles and Practice*. English. Vol. 18. United States: John Wiley and Sons, 2003.

[35] F. Blaabjerg. *Control of Power Electronic Converters and Systems*. English. Vol. 1. San Diego: Elsevier Science and Technology, 2018.

[36] J. Sun. Impedance-Based Stability Criterion for Grid-Connected Inverters. English. *IEEE Transactions on Power Electronics* 26.11 (2011), 3075–3078.

[37] C. Zhang, X. Wang, F. Blaabjerg, W. Wang and C. Liu. The influence of phase-locked loop on the stability of single-phase grid-connected inverter. English. IEEE, 2015, 4737–4744.

[38] M. Marjanen. Design and implementation of an induction motor drive test bench. English. 2015.

[39] T. Messo, A. Aapro, T. Suntio and T. Roinila. Design of grid-voltage feedforward to increase impedance of grid-connected three-phase inverters with LCL-filter. English. IEEE, 2016, 2675–2682.

[40] T. Messo, A. Aapro and T. Suntio. Generalized multivariable small-signal model of three-phase grid-connected inverter in DQ-domain. July 2015.

[41] D. Yang, X. Ruan and H. Wu. Impedance Shaping of the Grid-Connected Inverter with LCL Filter to Improve Its Adaptability to the Weak Grid Condition. English. *IEEE Transactions on Power Electronics* 29.11 (2014).

[42] A. Aapro, T. Messo and T. Suntio. Output impedance of grid-connected converter with active damping and feed-forward schemes. *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*. Oct. 2016, 2361–2366.

[43] T. Messo, A. Aapro, T. Suntio and T. Roinila. Design of grid-voltage feedforward to increase impedance of grid-connected three-phase inverters with LCL-filter. *2016*

IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia). May 2016, 2675–2682.

[44] Y. Liu, R. Bai, D. Wang, W. Ma and L. Wang. Proportional-resonant control method of three-phase grid-connected inverter. English. IEEE, 2014, 4797–4800.

[45] R. Teodorescu, F. Blaabjerg, M. Liserre and P. C. Loh. Proportional-resonant controllers and filters for grid-connected voltage-source converters. English. *IEE Proceedings: Electric Power Applications* 153.5 (2006), 750–762.

[46] D. N. Zmood and D. G. Holmes. Stationary frame current regulation of PWM inverters with zero steady-state error. English. *IEEE Transactions on Power Electronics* 18.3 (2003), 814–822.

[47] R. Teodorescu, F. Blaabjerg, U. Borup and M. Liserre. A new control structure for grid-connected LCL PV inverters with zero steady-state error and selective harmonic compensation. *Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2004. APEC '04.* Vol. 1. Feb. 2004, 580–586 Vol.1.

[48] F. Liu, Y. Zhou, S. Duan, J. Yin, B. Liu and F. Liu. Parameter Design of a Two-Current-Loop Controller Used in a Grid-Connected Inverter System With LCL Filter. *IEEE Transactions on Industrial Electronics* 56.11 (Nov. 2009), 4483–4491.

[49] T. Lee and S. Hu. Resonant current compensator with enhancement of harmonic impedance for LCL-filter based Active rectifiers. *2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*. Mar. 2011, 1538–1543.

[50] M. Schiesser, S. Wasterlain, M. Marchesoni and M. Carpita. A Simplified Design Strategy for Multi-Resonant Current Control of a Grid-Connected Voltage Source Inverter with an LCL Filter. English. *Energies* 11.3 (2018), 609.

[51] S. Golestan, J. M. Guerrero and J. C. Vasquez. Hybrid Adaptive/Nonadaptive Delayed Signal Cancellation-Based Phase-Locked Loop. *IEEE Transactions on Industrial Electronics* 64.1 (Jan. 2017), 470–479.

[52] Y. F. Wang and Y. W. Li. Grid Synchronization PLL Based on Cascaded Delayed Signal Cancellation. *IEEE Transactions on Power Electronics* 26.7 (July 2011), 1987–1997.

[53] Q. Huang and K. Rajashekara. An Improved Delayed Signal Cancellation PLL for Fast Grid Synchronization Under Distorted and Unbalanced Grid Condition. *IEEE Transactions on Industry Applications* 53.5 (Sept. 2017), 4985–4997.

[54] McGranaghan and Beaulieu. Update on IEC 61000-3-6: Harmonic Emission Limits for Customers Connected to MV, HV, and EHV. *2005/2006 IEEE/PES Transmission and Distribution Conference and Exhibition*. May 2006, 1158–1161.

[55] T. Abeyasekera, C. M. Johnson, D. J. Atkinson and M. Armstrong. Suppression of line voltage related distortion in current controlled grid connected inverters. *IEEE Transactions on Power Electronics* 20.6 (Nov. 2005), 1393–1401.

[56] S.-G. Jeong and M.-H. Park. The analysis and compensation of dead-time effects in PWM inverters. *IEEE Transactions on Industrial Electronics* 38.2 (Apr. 1991), 108–114.

[57] Y. Yang, K. Zhou, H. Wang and F. Blaabjerg. Harmonics mitigation of dead time effects in PWM converters using a repetitive controller. *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*. Mar. 2015, 1479–1486.

A MATLAB CODE FOR STEADY-STATE CALCULATION

```
%operating point
fsw = 10e3; Tsw = 1/fsw;
fs = 50; T = 1/fs; w = 2*pi*fs;
V_gd = 325; V_gq = 0; V_in = 700; I_in = 6; I_L2q = 0;

%passive components
C = 2*750e-6;   %input capacitor
C_f = 6.6e-6; %filter capacitor
L_1 = 4.1e-3; r_L1 = 100e-3;
L_2 = 8.1e-3; r_L2 = 300e-3;
R_d = 20; %damping resistance for the LCL filter

%define unknowns as symbolic variables
syms D_d D_q V_Cfd V_Cfq I_L1d I_L2d I_L1q

e1 = D_d*V_in-(r_L1+R_d)*I_L1d+w*L_1*I_L1q+R_d*I_L2d-V_Cfd==0;
e2 = D_q*V_in-w*L_1*I_L1d-(r_L1+R_d)*I_L1q+R_d*I_L2q-V_Cfq==0;
e3 = V_Cfd+R_d*I_L1d-(r_L2+R_d)*I_L2d+w*L_2*I_L2q-V_gd==0;
e4 = V_Cfq+R_d*I_L1q-(r_L2+R_d)*I_L2q-w*L_2*I_L2d-V_gq==0;
e5 = I_L1d-I_L2d+w*C_f*V_Cfq==0;
e6 = I_L1q-I_L2q-w*C_f*V_Cfd==0;
e7 = I_in -(3/2)*(D_d*I_L1d+D_q*I_L1q)==0;

%solve for capacitor voltage
VCfd2 = solve(e6,V_Cfd);
VCfq2 = solve(e5,V_Cfq);

%substitute back in original
e1 = subs(e1,[V_Cfd V_Cfq],[VCfd2 VCfq2]);
e2 = subs(e2,[V_Cfd V_Cfq],[VCfd2 VCfq2]);
e3 = subs(e3,[V_Cfd V_Cfq],[VCfd2 VCfq2]);
```

```
e4 = subs(e4,[V_Cfd V_Cfq],[VCfd2 VCfq2]);
e7 = subs(e7,[V_Cfd V_Cfq],[VCfd2 VCfq2]);

%intermediate
IL2d_m = solve(e3,I_L2d);

%substitute back result #1 in original
e1 = subs(e1,I_L2d,IL2d_m);
e2 = subs(e2,I_L2d,IL2d_m);
e4 = subs(e4,I_L2d,IL2d_m);
e7 = subs(e7,I_L2d,IL2d_m);

%intermediate result #2
IL1q_m = solve(e4,I_L1q);

%substitute back
e1 = subs(e1,I_L1q,IL1q_m);
e2 = subs(e2,I_L1q,IL1q_m);
e7 = subs(e7,I_L1q,IL1q_m);

%intermediate result #3
Dq_s = solve(e2,D_q);
e1 = subs(e1,D_q,Dq_s);
e7 = subs(e7,D_q,Dq_s);

%intermediate result #4
IL1d_s = solve(e7,I_L1d);
%change to (2,1) if req.
IL1d_s = simplify(IL1d_s(1,1));
%substitute back
e1 = subs(e1,I_L1d,IL1d_s);

%intermediate result #5
Dd_s = double(solve(e1,D_d));
e7 = subs(e7,D_d,Dd_s);

IL1d_s = double(solve(e7,I_L1d));
%check which solution makes sense & change to (2,1) if req.
IL1d_s = IL1d_s(1,1);

%substitute back
e2 = subs(e2,I_L1d,IL1d_s);
```

```
%Dq numerical value
Dq_s = double(solve(e2,D_q));

e4 = subs(e4,IL1d_s);
%IL1q numerical value
IL1q_s = double(solve(e4,I_L1q));
%substitute back
e3 = subs(e3,[I_L1d I_L1q],[IL1d_s  IL1q_s]);

%IL2d numerical
IL2d_s = double(solve(e3,I_L2d));
%substitute back
e6 = subs(e6,I_L1q,IL1q_s);
%VCfd numerical value
VCfd_s = double(solve(e6,V_Cfd));
%substitute back
e5 = subs(e5,[I_L1d I_L2d],[IL1d_s IL2d_s]);
%VCfq numerical value
VCfq_s = double(solve(e5,V_Cfq));

%final numerical value to characterize open-loop tf.s
D_d = double(Dd_s);
D_q = double(Dq_s);
I_L1d = double(IL1d_s);
I_L1q = double(IL1q_s);
I_L2d = double(IL2d_s);
V_Cfd = double(VCfd_s);
V_Cfq = double(VCfq_s);
```

B TRANSFER FUNCTIONS

$$\boldsymbol{G}(s) = \boldsymbol{C}(s\boldsymbol{I} - \boldsymbol{A})^{-1}\boldsymbol{B} + \boldsymbol{D} \tag{B.1}$$

Open-loop input dynamics

$$Z_{in-o} = \begin{bmatrix} \boldsymbol{G}(1,1) & 0 \\ 0 & 0 \end{bmatrix} \quad \boldsymbol{T}_{oi-o} = \begin{bmatrix} \boldsymbol{G}(1,2) & \boldsymbol{G}(1,3) \\ 0 & 0 \end{bmatrix} \quad \boldsymbol{G}_{ci-o} = \begin{bmatrix} \boldsymbol{G}(1,4) & \boldsymbol{G}(1,5) \\ 0 & 0 \end{bmatrix} \tag{B.2}$$

Inverter-sde open-loop dynamics

$$\boldsymbol{G}_{iL-o} = \begin{bmatrix} \boldsymbol{G}(2,1) & 0 \\ \boldsymbol{G}(3,1) & 0 \end{bmatrix} \quad \boldsymbol{T}_{oL-o} = \begin{bmatrix} \boldsymbol{G}(2,2) & \boldsymbol{G}(2,3) \\ \boldsymbol{G}(3,2) & \boldsymbol{G}(3,3) \end{bmatrix} \quad \boldsymbol{G}_{cL-o} = \begin{bmatrix} \boldsymbol{G}(2,4) & \boldsymbol{G}(2,5) \\ \boldsymbol{G}(3,4) & \boldsymbol{G}(3,5) \end{bmatrix} \tag{B.3}$$

Output dynamics

$$\boldsymbol{G}_{io-o} = \begin{bmatrix} \boldsymbol{G}(4,1) & 0 \\ \boldsymbol{G}(5,1) & 0 \end{bmatrix} \quad \boldsymbol{Y}_{o-o} = \begin{bmatrix} -\boldsymbol{G}(4,2) & -\boldsymbol{G}(4,3) \\ -\boldsymbol{G}(5,2) & -\boldsymbol{G}(5,3) \end{bmatrix} \quad \boldsymbol{G}_{co-o} = \begin{bmatrix} \boldsymbol{G}(4,4) & \boldsymbol{G}(4,5) \\ \boldsymbol{G}(5,4) & \boldsymbol{G}(5,5) \end{bmatrix} \tag{B.4}$$

Controller matrices

$$\boldsymbol{G}_{cc} = \begin{bmatrix} G_{PI-d} & 0 \\ 0 & G_{PI-q} \end{bmatrix} \quad \boldsymbol{G}_{vc} = \begin{bmatrix} G_{PI-v} & 0 \\ 0 & 0 \end{bmatrix} \tag{B.5}$$

The effect of PLL

$$\boldsymbol{G}_{PLL-d} = \begin{bmatrix} 0 & -\frac{D_q}{V_{gd}} \frac{L_{PLL}}{1+L_{PLL}} \\ 0 & \frac{D_d}{V_{gd}} \frac{L_{PLL}}{1+L_{PLL}} \end{bmatrix} \quad \boldsymbol{G}_{PLL-i} = \begin{bmatrix} 0 & \frac{I_{L1q}}{V_{gd}} \frac{L_{PLL}}{1+L_{PLL}} \\ 0 & -\frac{I_{L1d}}{V_{gd}} \frac{L_{PLL}}{1+L_{PLL}} \end{bmatrix} \tag{B.6}$$

The effect of feedforward term

$$\boldsymbol{G}_{FF} = \begin{bmatrix} G_{ffd} & 0 \\ 0 & G_{ffq}\left(1 - \frac{L_{PLL}}{(1+L_{PLL})}\right) \end{bmatrix} \tag{B.7}$$

C LABORATORY RESULTS USING DELAYED-SIGNAL CANCELLATION PLLS

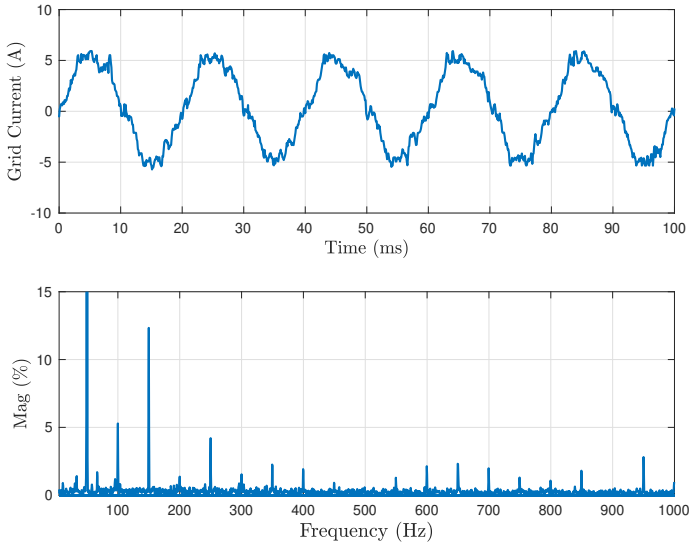


Figure C.1. *Dq-frame current-control with $\alpha\beta$CDSC-PLL.*

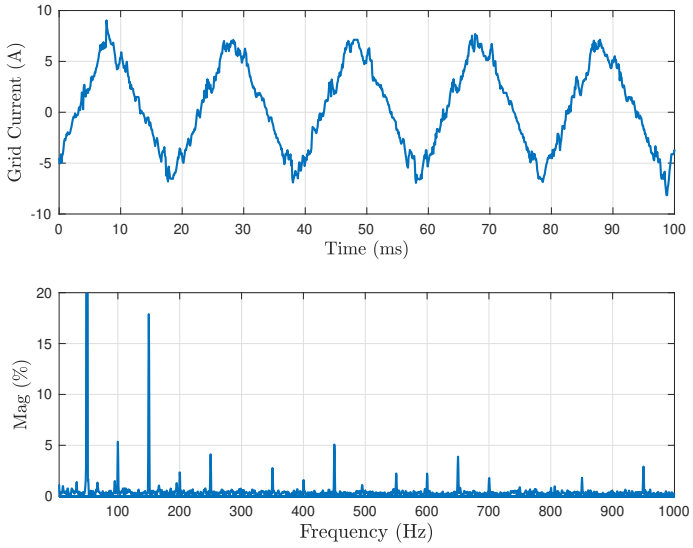


Figure C.2. *Dq-frame current-control with dqADSC-PLL.*

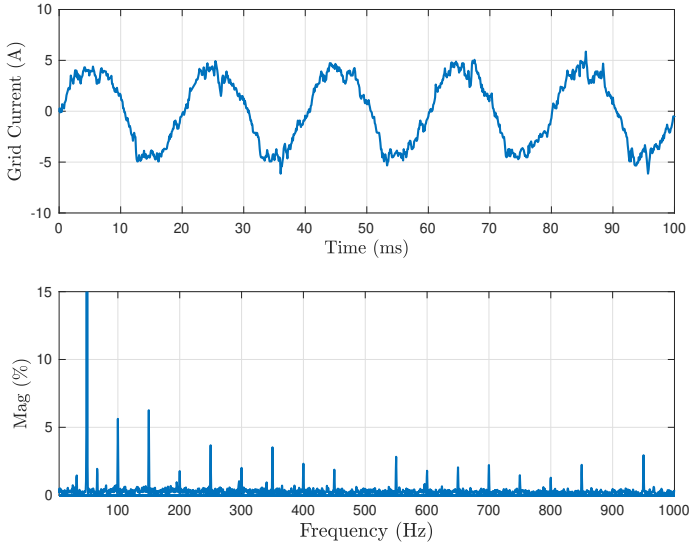


Figure C.3. *$\alpha\beta$-frame current-control with $\alpha\beta$CDSC-PLL.*

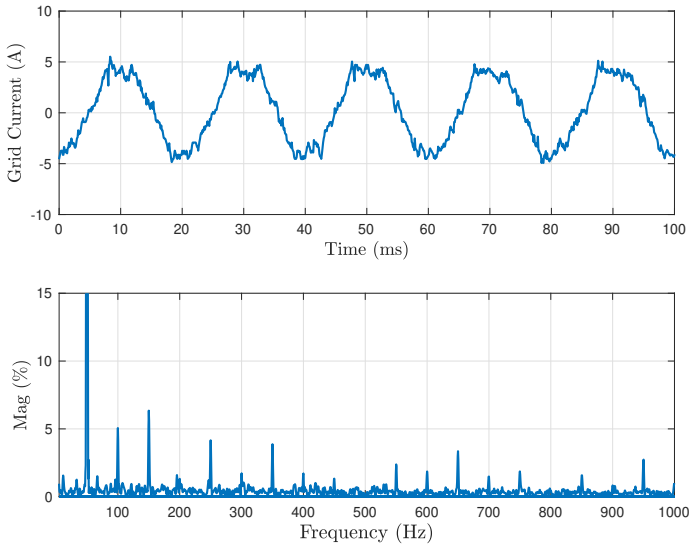


Figure C.4. *$\alpha\beta$-frame current-control with dqADSC-PLL.*