TAMPEREEN TEKNILLINEN YLIOPISTO
TAMPERE UNIVERSITY OF TECHNOLOGY

QIUTING WANG

DESIGN AND CONSTRUCTION OF A PLL SYSTEM FOR A 96-MHZ FM TRANSMITTER

Master of Science Thesis

Examiner: University Lecturer Olli-Pekka Lundén and Lecturer Jari Kangas
Examiner and topic approved by the Faculty Council of the Faculty of Computing and Electrical Engineering on 31st May 2017

ABSTRACT

QIUTING WANG: Design and Construction of A PLL System for A 96-MHz FM Transmitter
Tampere University of Technology
Master of Science Thesis, 54 pages, 3 Appendix pages
December 2017
Master's Degree Programme in Electrical Engineering
Major: Electronics
Examiner: University Lecturer Olli-Pekka Lundén and Lecturer Jari Kangas
Keywords: phase-locked loop, crystal oscillator, voltage-controlled oscillator, frequency divider, phase detector, loop filter

The phase-locked loop (PLL) is used as frequency synthesizer in numerous electronic devices. This thesis presents design and construction of a basic PLL system on solderless breadboard, using discrete components and integrated circuits (ICs). The circuitry is designed to synthesize a 96-MHz sinusoidal signal, which can be used as the carrier wave for an FM transmitter. The circuitry includes a 24-MHz crystal oscillator (XO), a 96-MHz voltage-controlled oscillator (VCO), two frequency dividers, a phase detector (PD), and a loop filter (LF). In addition, a buffer amplifier is placed before each frequency divider for diminishing spurious frequencies. The XO provides 24-MHz reference frequency while the VCO is tunable between 86 MHz and 100 MHz. The constructed PLL system is able to lock the VCO frequency to 96 MHz.

In this thesis, fundamental knowledge related to PLL is reviewed, and all building blocks of the PLL system are studied and analyzed. The challenges on utilizing IC chips are also discussed. Therefore this work provides a guide and reference for similar works and future study. For further research, the method of eliminating spurious frequencies and improving loop stability could be explored deeper to optimize the PLL performance.

PREFACE

Although this work took longer time than expected, I feel very glad that it was completed finally. I would like to thank my supervisors and examiners, Olli-Pekka Lundén and Jari Kangas, for offering me so many helpful suggestions and a variety of assistance, either on lab work or on thesis writing. I would also like to thank my parents and friends for always supporting and encouraging me.

Tampere, 20th December 2017

Qiuting Wang

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LIST OF ABBREVIATIONS AND SYMBOLS

PLL	phase-locked loop
VCO	voltage-controlled oscillator
FM	frequency modulation
XO	crystal oscillator
PD	phase detector
LF	loop filter
IC	integrated circuit
RF	radio frequency
RMS	root mean square
LPLL	linear phase-locked loop
DPLL	digital phase-locked loop
ADPLL	all-digital phase-locked loop
SPLL	software phase-locked loop
APLL	analog phase-locked loop
LO	local oscillator
IF	intermediate frequency
LPF	low-pass filter

$A_P\|_{\mathrm{dB}}$	power gain in dB
P_{in}	input power
P_L	load power
$A_V\|_{\mathrm{dB}}$	voltage gain in dB
V_{in}	input voltage RMS value
V_{out}	output voltage RMS value
$P\|_{\mathrm{dBm}}$	power in dBm
$P\|_{\mathrm{mW}}$	power in mW
V_{eff}	RMS value (effective value) of voltage
V_{pp}	peak-to-peak value of voltage
ω_i	reference (angular) frequency
ω_o	VCO output (angular) frequency
$\frac{\omega_o}{N}$	divided VCO output (angular) frequency
u_{pd}	phase detector output voltage
V_{ctrl}	VCO input control voltage
f_s	series resonant frequency of quartz crystal
f_p	parallel resonant frequency of quartz crystal
Z_{eq}	impedance of quartz crystal equivalent circuit

C_{var}	capacitance of varactor diode
ω_{max}	maximum VCO output frequency
ω_{min}	minimum VCO output frequency
K_v	VCO gain
$\Delta\omega_{VCO}$	VCO tuning range
K_n	frequency divider gain
θ_n	frequency divider output phase
θ_e	phase difference between two signals
$\bar{u}_{pd}$	average voltage of u_{pd}
K_d	phase detector gain
ω_c	cutoff frequency of low-pass filter
τ	time constant
K_f	loop filter gain
θ_i	XO output phase
θ_o	VCO output phase
ω_n	natural frequency
ζ	damping factor
ω_{cr}	lock range (capture range)
t_L	locking time (settling time)

1. INTRODUCTION

The phase-locked loop (PLL) is a feedback circuitry that can control an oscillator signal to track a reference signal by locking the phase difference between these two signals into a constant. The oscillator is commonly a voltage-controlled oscillator (VCO), and the phase difference is detected by a phase detector. [1, p.3]

The PLL was invented in 1930s [2, p.6] and it has been extensively utilized in many electronic fields, such as in wireless communication, microprocessor, and navigation. A PLL system can be found for example, in FM (frequency modulation) radios, televisions, computers, and cell phones [3, p.269].

The main applications of PLL system are reproduction of signals (as with noise reduction), modulation and demodulation, plus frequency synthesis. [1, p.3-4] [3, p.270-271]

A signal usually needs to be modulated before being sent out through a transmitter. The object of this work is to design and build a PLL circuitry, which can synthesize a 96-MHz carrier frequency for the purpose of frequency modulation. This PLL system is composed by five building blocks: a 24-MHz crystal oscillator (XO) which offers a reference signal, a 96-MHz VCO, two frequency dividers, a phase detector (PD), and a loop filter (LF). The whole circuitry is constructed on solderless breadboards with discrete components, except an IC (integrated circuit) chip CD4070BE used as PD and three IC chips 74AC74 used as dividers. The 96-MHz output signal can be used for an FM transmitter.

The PLL plays a preliminary but important role in radio frequency (RF) study. This thesis reviews the concept and mechanism of the PLL, presents the construction of each block and records their testing results, therefore providing a guide and reference for similar works and future study. The thesis also compares and discusses the applicability of some IC chips for the studied PLL.

This thesis is organized as follows. Chapter 2 introduces the reader to the fundamentals of PLL, including the development of PLL, the building blocks of PLL, and related control theory. Chapter 3 demonstrates the design of every block, also

presents their constructed circuits and measurement results. Chapter 4 analyzes some challenges on the phase detector and the frequency divider, presents the results of whole system, followed by conclusions in Chapter 5.

2. BACKGROUND

In this chapter, firstly some commonly used units are mentioned in Section 2.1. The development of phase-locked loop (PLL) is introduced in Section 2.2. Then each building block is explained separately in Section 2.3. Lastly the control theory of PLL is demonstrated in Section 2.4.

2.1 Commonly used units

Decibels (dB) are generally used when describing power and gain [4, p.7]. The power gain is expressed as:

$$A_P|_{\mathrm{dB}} = 10 \log \frac{P_L}{P_{in}}, \tag{2.1}$$

where P_{in} is the input power and P_L is the load power.

The voltage gain (assuming the input impedance equals the load impedance) is expressed as:

$$A_V|_{\mathrm{dB}} = 20 \log \frac{V_{out}}{V_{in}}, \tag{2.2}$$

where V_{in} is RMS (root mean square) value of input voltage and V_{out} is RMS value of output voltage.

A power level is converted into dBm as:

$$P|_{\mathrm{dBm}} = 10 \log \frac{P|_{\mathrm{mW}}}{1\,\mathrm{mW}}, \tag{2.3}$$

where $P|_{\mathrm{mW}}$ is a power value in mW.

The RMS value (or effective value) of voltage V_{eff} across 50-Ω load can be converted into power value as:

$$P|_{\mathrm{dBm}} = 10 \log \frac{(V_{eff}|_{\mathrm{V}})^2}{50\,\Omega \times 10^{-3}\ \mathrm{W}}, \tag{2.4}$$

while for a sinusoidal signal, the relationship between V_{eff} and peak-to-peak value of voltage V_{pp} is described as:

$$V_{pp} = 2\sqrt{2}\, V_{eff}. \tag{2.5}$$

2.2 The development of PLL

This section presents the history and classification of PLL.

2.2.1 The History of PLL

In 1932, a French engineer named *Henri de Bellescize* published a paper in the French periodical *L'Onde Electrique*, presenting the first PLL circuit in the world. This PLL was built based on two vacuum tubes, for the purpose of receiving signals synchronously. However, his work failed to attract public attention at that time. [2, p.6-7]

After about twenty years, the PLL began to be applied as a synthesizer due to the development of color televisions. The popularity of computers also promoted the innovation of PLL. Nowadays, PLL has been utilized in a variety of electronic devices. [2, p.7][5, p.8-9]

2.2.2 The classification of PLL

There are primarily four types of PLL at present: linear PLLs (LPLLs), digital PLLs (DPLLs), all-digital PLLs (ADPLLs), and software PLLs (SPLLs). [2, p.8]

LPLLs are also referred as analog PLLs (APLLs), constructed purely by analog components. DPLLs have gradually replaced LPLLs, since 1970's, due to their advantages in system stability. In DPLLs, some parts of the circuitry utilize digital elements. The third type, ADPLLs do not include any analog components. Finally, SPLLs are implemented by software and the PLL function is realized based on programs. [2, p.8]

This work is focusing on DPLLs, hence the following PLLs in this thesis mainly refer to digital PLLs.

2.3 The building blocks of PLL

A primary block diagram of PLL is depicted in Figure 2.1. It consists of a crystal oscillator (XO), a voltage-controlled oscillator (VCO), a frequency divider, a phase detector (PD), and a loop filter (LF).

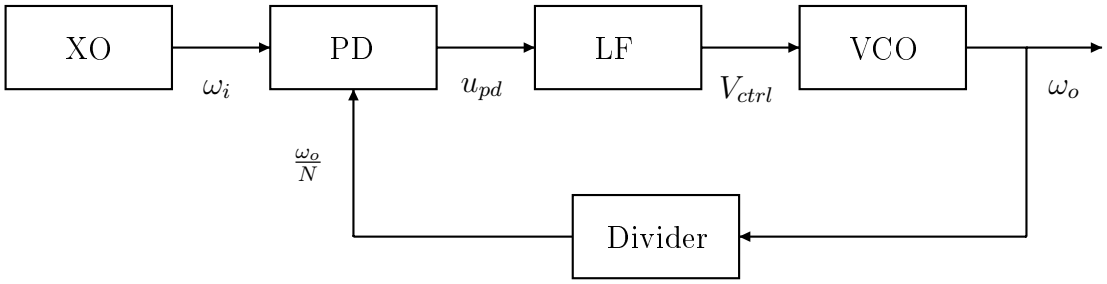


Figure 2.1 *A block diagram of PLL.*

The XO provides a stable reference (angular) frequency ω_i. During the test, it can be replaced by other signal generators. The VCO creates a signal at frequency ω_o, which could be several times greater than ω_i. This ω_o will be divided by N (the division number) through the divider, such that ω_i and divided frequency $\frac{\omega_o}{N}$ are close to each other. The PD compares the phase difference between ω_i and $\frac{\omega_o}{N}$, outputting a beat signal of voltage u_{pd}. After the LF, the filtered u_{pd} becomes V_{ctrl} that controls the operation of VCO. Eventually, ω_o will be adjusted to be identical to $N\omega_i$ due to this negative feedback loop.

Each block is shortly clarified in the following sections.

2.3.1 Crystal oscillators

Oscillator circuits are currently applied in almost every electronic device to offer a specific and steady frequency [6]. Figure 2.2 shows the concept of most electronic oscillators.

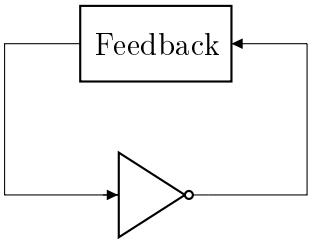


Figure 2.2 *The concept of most electronic oscillators.*

Basically, a oscillator can be regarded as a closed-loop circuit that consists of an amplifier and a feedback network [7, p.12-13]. The feedback part provides positive feedback and works as a frequency-selective network. It determines the oscillation frequency. The signal at selected frequency is amplified by the amplifier, meanwhile the signals at other undesired frequencies attenuate. Due to the positive feedback, the wanted signal will be amplified repeatedly, until its amplitude reaches the limitation and does not increase any more.

There are two necessary requirements for generating stable sinusoid. Firstly, the total phase shift of loop equals 360°. Usually the amplifier provides 180° phase shift and the feedback network provides another 180° phase shift. Secondly, the closed-loop gain must be 1, which means the amplifier gain compensates fully for the signal attenuation in the feedback path. [4, p.502-506] [7, p.10-13]

According to the components of feedback network, oscillators can be basically divided into RC oscillators, LC oscillators, crystal oscillators, and other oscillators. The one used in this project is a crystal oscillator.

The crystal oscillator appeared in 1920's [7, p.1]. It is usually used for creating a reference signal at a precise frequency because it usually has better frequency stability than an RC or LC oscillator. Figure 2.3 presents a picture of quartz (SiO_2) crystal and its electronic symbol. Both two opposite sides of the thin piece of quartz are metalized for electrical contact. Because of the piezoelectric effect, the quartz vibrates in its thickness direction and finally generates an alternating current at its resonant frequency. Thinner quartz has higher resonant frequency, thereby the physical thickness of a quartz restricts its frequency upper limitation. Commonly, the resonant frequency of a quartz crystal is made from several tens of kHz to several tens of MHz. [7, p.3]

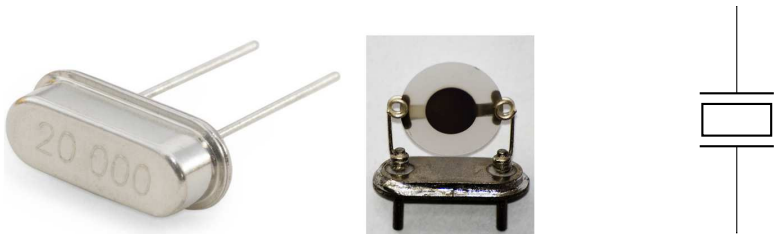


Figure 2.3 *(a) A quartz crystal and (b) the electronic symbol of quartz crystal.*

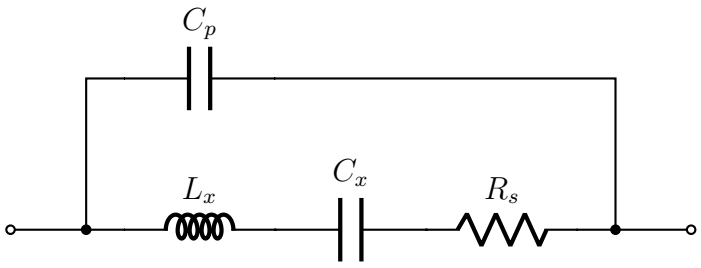


Figure 2.4 *An equivalent circuit of quartz crystal.*

As shown in Figure 2.4, an equivalent circuit of quartz crystal includes an inductor L_x and a capacitor C_x, that make the crystal strongly frequency-selective. There is also a parallel capacitor C_p representing the parasitic capacitance of the metal

platings, the package, and the leads. A series resistor R_s representing the mechanical and electrical losses. Crystal exhibits two different resonant frequencies: one is the series resonant frequency (f_s) caused by L_x and C_x, the other is the parallel resonant frequency (f_p) caused by L_x, C_x and C_p. These two frequencies can be calculated from:

$$f_s = \frac{1}{2\pi\sqrt{L_x C_x}}, \tag{2.6}$$

$$f_p = \frac{1}{2\pi\sqrt{L_x \frac{C_x C_p}{C_x + C_p}}}. \tag{2.7}$$

Supposing $L_x = 4.2$ H, $C_x = 0.006$ pF, $R_s = 260\ \Omega$, $C_p = 3.4$ pF (values from [7, p.5]), f_s and f_p can be obtained as approximately 1.00258 and 1.00346 MHz respectively, from Equation 2.6 and 2.7. The impedance of this equivalent circuit Z_{eq} can be calculated from:

$$Z_{eq} = (-j2\pi f C_p) \;//\; (j2\pi f L_x - j2\pi f C_x + R_s) \tag{2.8}$$

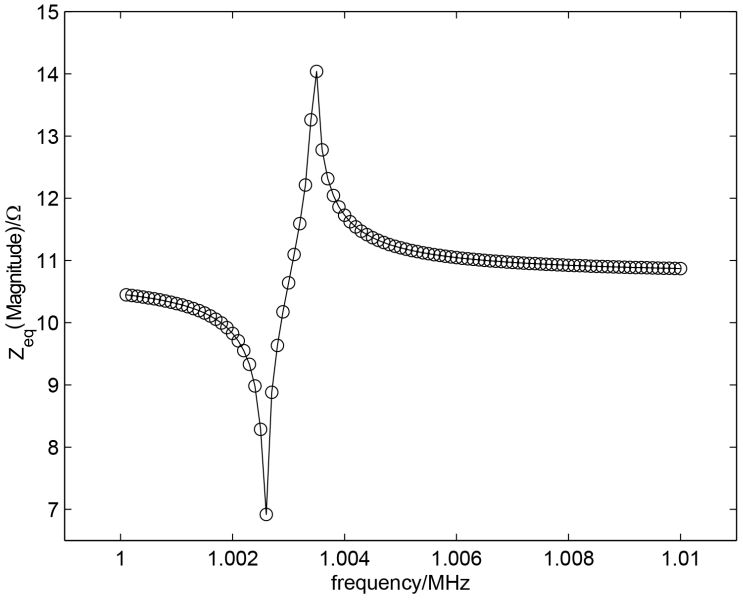


Figure 2.5 *The magnitude of Z_{eq} as a function of frequency f (generated by Matlab).*

Figure 2.5 plots the magnitude of Z_{eq} as a function of frequency f. The circuit presents low impedance at its series resonant frequency (1.00258 MHz) and high impedance at parallel resonant frequency (1.00346 MHz). Crystal oscillators work at the series resonant frequency. However, according to the connecting ways of crystal, the oscillator circuits can be divided into series-resonant circuits and parallel-

resonant circuits. In a series-resonant oscillator, the crystal impedance is low at the oscillation frequency while in a parallel-resonant oscillator, the crystal impedance is high at the oscillation frequency. [7, p.9]

Pierce crystal oscillator (see Figure 2.6) has simple structure and good frequency stability. Consequently, it was selected for this project. Pierce oscillator circuit was derived from Colpitts oscillator, a parallel-resonant circuit (see Figure 2.7), by George W. Pierce. [7, p.25-27,45-51]

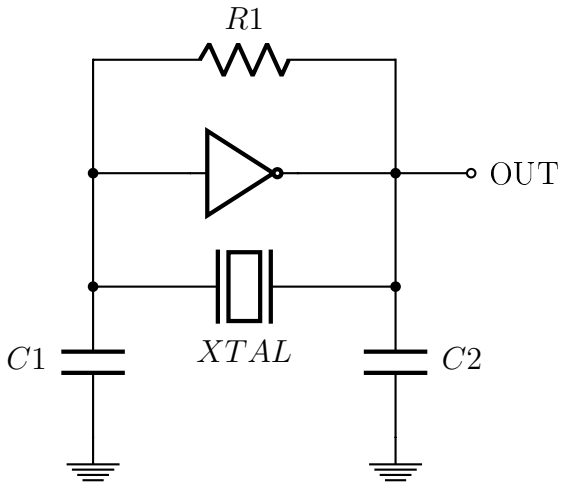


Figure 2.6 *A typical Pierce crystal oscillator circuit.*

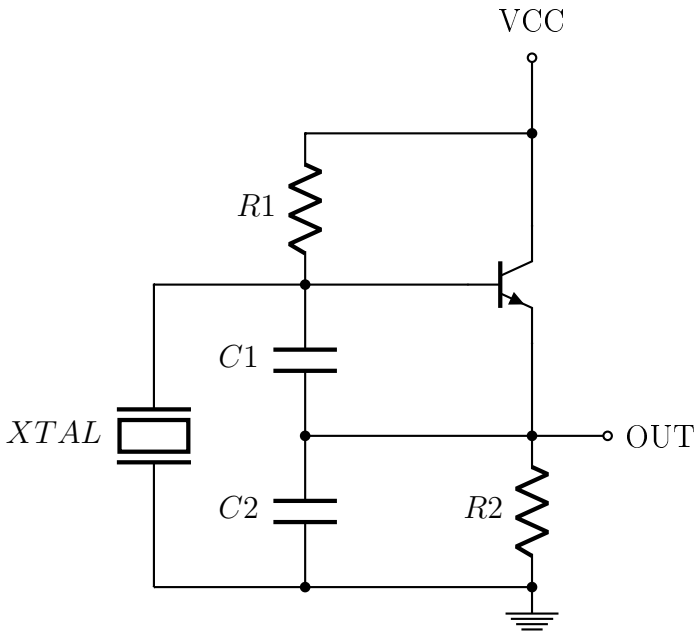


Figure 2.7 *A simple crystal oscillator with transistor.*

In a Pierce crystal oscillator, it is the quartz crystal and two capacitors that form the feedback network, determine the resonant frequency and provide 180° phase shift.

2.3.2 Voltage-controlled oscillators

The frequency of a voltage-controlled oscillator (VCO) can be tuned by a input voltage within a range. It is a necessary part in PLL loop.

A high-frequency VCO circuit for PLL is usually built by adding a varactor diode into an LC resonant oscillator. Its tunability is realized through the variable capacitance of varactor diode. It can provide more linear gain over other VCOs. [2, p.38-42]

Most LC oscillators use the topology called "three-point" type. The three-point oscillator contains a transistor and a LC tank. The three terminals of transistor are connected to three nodes of the LC tank respectively. [8, p.749-750]

According to Razavi [4, p.517], three-point oscillators can be divided into three different groups: with gate (or base) grounded, with drain (or collector) grounded, and with source (or emitter) grounded, as shown in Figure 2.8.

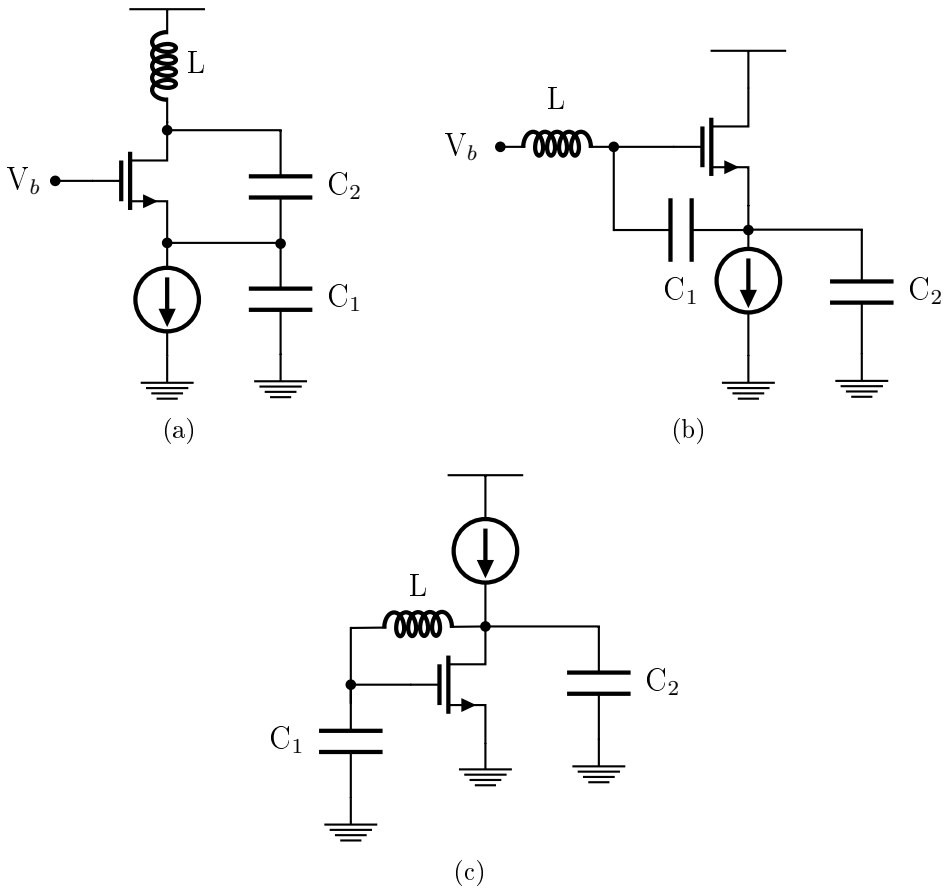


Figure 2.8 *The topology of three-point oscillator (using MOSFET), (a) with gate grounded, (b) with drain grounded, (c) with source grounded.*

The Clapp oscillator [9, p.605], which is a common choice for VCO design, has its

drain (or collector) grounded, as shown in Figure 2.9(a). The tunable oscillator is obtained by replacing the capacitor C_0 with a varactor diode (see Figure 2.9(b)). [9, p.606-607]

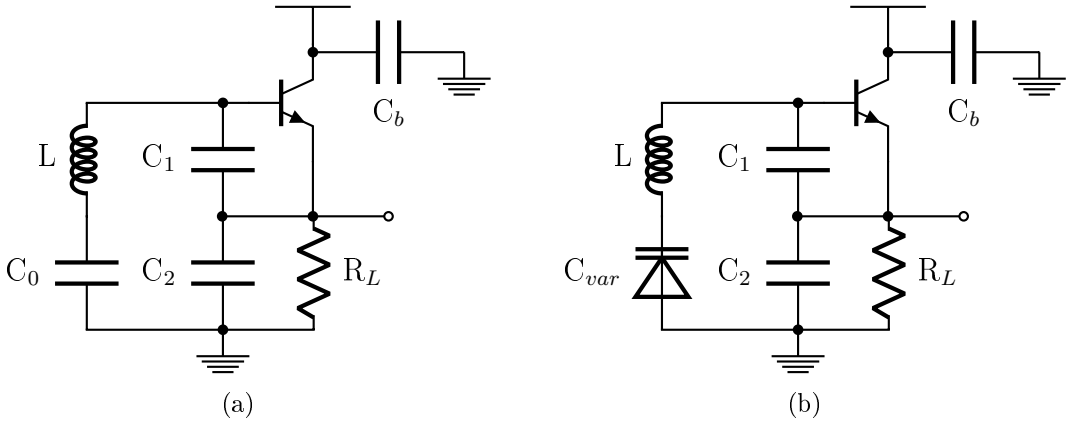


Figure 2.9 *(a) A Clapp oscillator and (b) a Clapp VCO circuit.*

The capacitance of a varactor diode C_{var} decreases as its reverse-biasing voltage increases, which can be described as followed:

$$C_{var} = C_{V0}\left(1 - \frac{V_{ctrl}}{V_{diff}}\right)^{(-1/2)}, \tag{2.9}$$

where C_{V0} is the original capacitance of diode without any applied voltage, V_{ctrl} is the applied reverse-biasing voltage, and V_{diff} is the barrier voltage of the pn-junction. [9, p.307-308]

The resonant frequency ω_o of clapp VCO in Figure 2.9(b) is calculated from:

$$\omega_o = \sqrt{\frac{1}{L}\left(\frac{1}{C_{var}} + \frac{1}{C_1} + \frac{1}{C_2}\right)}. \tag{2.10}$$

Thereby, the maximum output frequency ω_{max} is calculated from:

$$\omega_{max} = \sqrt{\frac{1}{L}\left(\frac{1}{C_{var\_min}} + \frac{1}{C_1} + \frac{1}{C_2}\right)}, \tag{2.11}$$

and the minimum output frequency ω_{min} is calculated from:

$$\omega_{min} = \sqrt{\frac{1}{L}\left(\frac{1}{C_{var\_max}} + \frac{1}{C_1} + \frac{1}{C_2}\right)}. \tag{2.12}$$

The ω_o can be described as a function of input control voltage V_{ctrl} after a locally

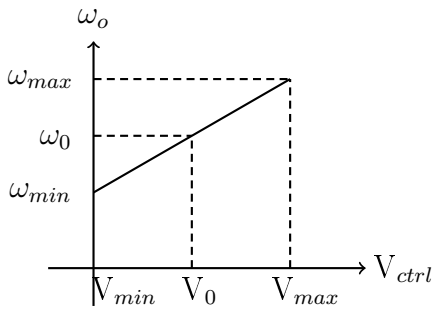


Figure 2.10 *The characteristic of VCO output frequency.*

linearized approximation, as plotted in Figure 2.10:

$$\omega_o = K_V V_{ctrl} + \omega_{min}, \tag{2.13}$$

where K_V is the slope of function, called the VCO gain and expressed in rad/s/V:

$$K_V = \frac{\Delta \omega_o}{\Delta V_{ctrl}} \approx \frac{\omega_{max} - \omega_{min}}{V_{max} - V_{min}} \text{ rad/s/V}. \tag{2.14}$$

For typical varactors V_{min} can be zero and V_{max} several volts or even tens of volts.

The difference between ω_{max} and ω_{min} is called the tuning range $\Delta \omega_{VCO}$:

$$\Delta \omega_{VCO} = \omega_{max} - \omega_{min}, \tag{2.15}$$

while the angular center frequency ω_0 is the center point between ω_{max} and ω_{min}.

In time domain, phase θ_o is obtained by integrating instantaneous angular frequency ω_o over time:

$$\theta_o(t) = \int_0^t \omega_o(\tau) d\tau + C. \tag{2.16}$$

On the other hand, the Laplace transform of integration is division by s [4, p.607]. Therefore, the Laplace domain phase of a VCO is given by:

$$\theta_o = \frac{\omega_o}{s}. \tag{2.17}$$

$\Delta \theta_o$ can be written as:

$$\Delta \theta_o = \frac{\Delta \omega_o}{s} = \frac{K_V \cdot \Delta V_{ctrl}}{s} = \underbrace{\frac{K_V}{s}}_{\text{VCO gain}} \cdot \Delta V_{ctrl}. \tag{2.18}$$

2.3.3 Frequency dividers

A frequency divider divides an input frequency usually by an integer. There are analog dividers and digital dividers: analog dividers are targeted at very high frequencies, while digital dividers are commonly used in IC chips. [4, p.655-661]

The flip-flop divider is a digital divider. Flip-flops [10, p.142] are bistable circuits meaning that it can flip between state "0" (logic low level) and "1" (logic high level) under the effect of its input signal. Flip-flop dividers have the advantages of simple structure, low power consumption, and low cost. [10, p.143-145]

The D flip-flop (data flip-flop, or delay flip-flop) is popular for frequency division. It is an edge triggered flip-flop, which means the stored state will flip at the positive edge or the negative edge of input clock signal.

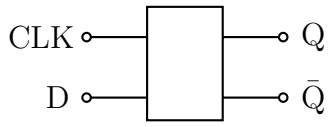


Figure 2.11 *D flip-flop symbol.*

As shown in Figure 2.11, a D flip-flop has two input nodes and two output nodes: data input D, clock input CLK, output Q and its complement $\bar{Q}$. Q and $\bar{Q}$ are opposite to each other. A D flip-flop can be made by connecting logic gates in the way shown in Figure 2.12, using four NAND gates with one NOT gate.

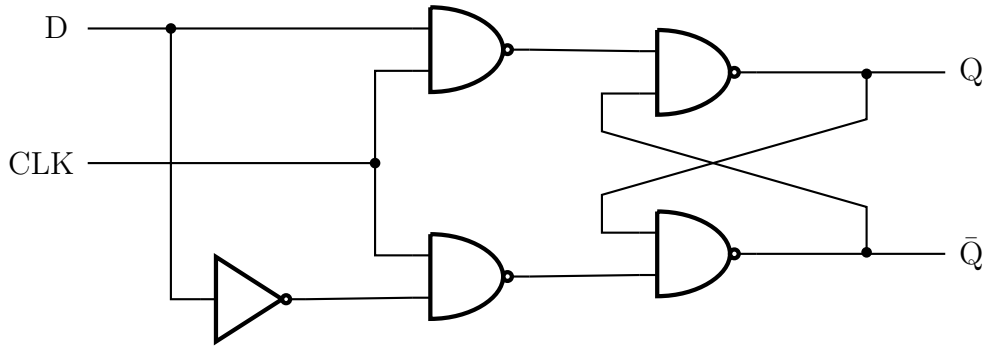


Figure 2.12 *A D flip-flop composed by logic gates.*

Table 2.1 shows the truth table of a positive edge-triggered D flip-flop. Q_n is the previous state of Q_{n+1}. In brief, the output Q takes the state of data input only when CLK jumps from low to high. In any other cases, Q and $\bar{Q}$ remain their previous value no matter which state D is, because the stored memory is latched. If the flip-flop is negative triggered, the output values will flip at negative edges. This edge triggered flip-flops help to reject the interference and reduce the possibility of

error, because the output will hold its state except the moment of triggering even if there are interferences at input D.

Table 2.1 *The truth table of a positive triggered D flip-flop.*

CLK	D	Q_{n+1}	$\bar{Q}_{n+1}$
$\uparrow$	0	0	1
$\uparrow$	1	1	0
$\downarrow$	$\times$	Q_n	$\bar{Q}_n$
0	$\times$	Q_n	$\bar{Q}_n$
1	$\times$	Q_n	$\bar{Q}_n$

Figure 2.13 shows an example sequence diagram of a positive edge-triggered D flip-flop, designed with Xilinx ISE (a VHDL design tool).

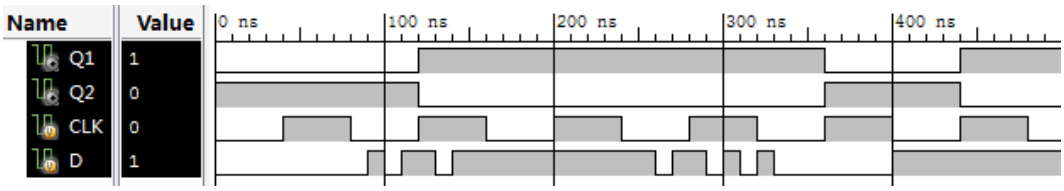
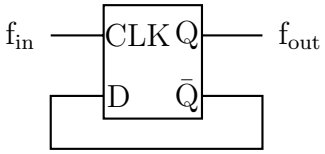
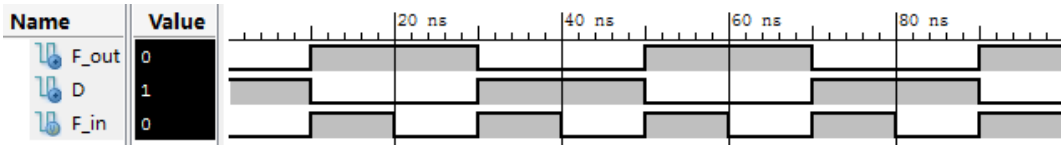


Figure 2.13 *An example sequence diagram of a positive edge-triggered D flip-flop.*

A by-2 divider can be obtained by connecting the $\bar{Q}$ of D flip-flop to its D. Figure 2.14 presents a by-2 divider and its corresponding sequence diagram created with Xilinx ISE.



(a)



(b)

Figure 2.14 *(a) The diagram of a by-2 divider and (b) the sequence diagram of by-2 divider.*

Similarly, a by-4 divider can be implemented by cascading two D flip-flop, as depicted in Figure 2.15(a). The input signal goes into the CLK pin of first flip-flop, then its Q is connected to the CLK of second flip-flop.

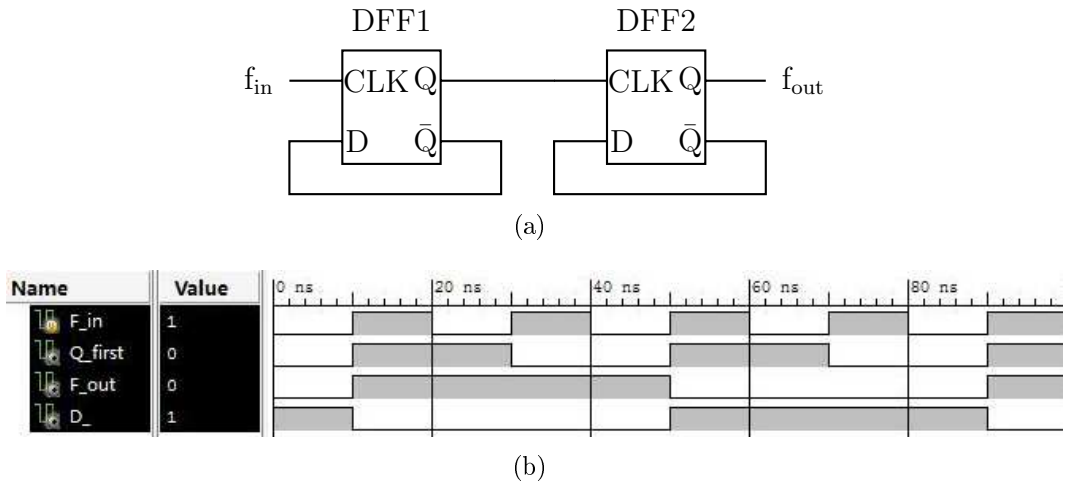


Figure 2.15 *(a) The diagram of a by-4 divider and (b) the sequence diagram of by-4 divider.*

From Figure 2.15(b), it can be seen that Q_1 changes from its previous state to the opposite at each positive edge of f_{in}, having a frequency of $f_{in}/2$. At the same time, Q_2, which is the desirable output signal f_{out}, flips its state at every positive edge of Q_1 (CLK_2), having a frequency of $Q_1/2$. Therefore, f_{out} equals a quarter of f_{in}.

Likewise, a divide-by-N circuit can be made up of M D flip-flops while $N = 2^M$. The gain of the by-N divider is:

$$K_n = \frac{\theta_n}{\theta_o} = \frac{\frac{\omega_o/s}{N}}{\omega_o/s} = \frac{1}{N}, \tag{2.19}$$

where θ_n is the phase of divided signal.

2.3.4 Phase detectors

A phase detector generates an output signal that is proportional to the phase difference between two input signals. There are several means for realizing the function of phase detection [2, p.15]. In this section, two types of phase detectors are introduced: the double-balanced diode mixer and the Exclusive-OR (XOR) gate.

Double-balanced diode mixer

A double-balanced diode mixer contains four end-to-end diodes and two transformers (see Figure 2.16). In down conversion operation LO (local oscillator) and RF (radio frequency) are input ports while IF (intermediate frequency) is output port.

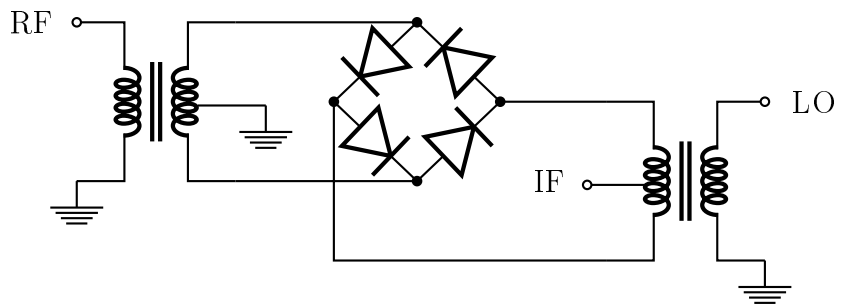


Figure 2.16 *A double-balanced diode mixer.*

Two input ports are fed with strong enough square waves at same frequency. When LO signal is positive, the upper two diodes conduct current and lower two diodes are off. Therefore, RF signal flows from the upper terminal of its secondary side into IF, which means the IF reproduce the signal of RF. When LO signal is negative, there is the opposite situation. The lower two diodes conduct current instead, and RF signal flows from the lower terminal into IF. In this case, the IF signal is the negative of RF. Figures 2.17 - 2.21 illustrate how the double-balanced mixer detects two square waves.

When LO and RF are in phase, the phase difference between them is 0 ($\theta_e = 0$), the result of mixer is a square wave with 100% duty cycle, see Figure 2.17.

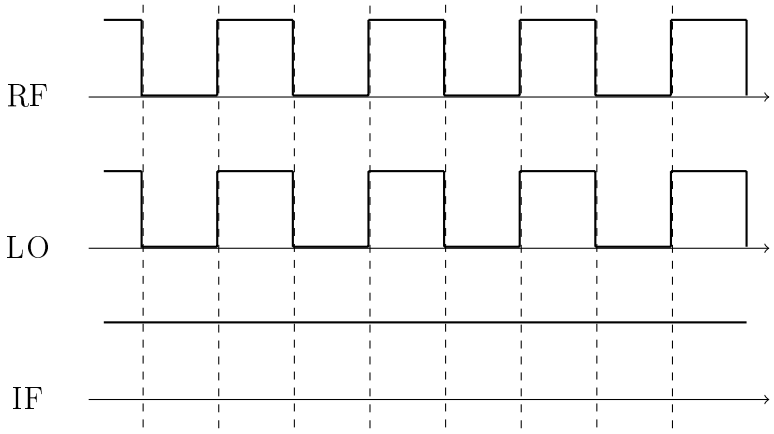


Figure 2.17 *The input and output waveforms of double-balanced diode mixer when* $\theta_e = 0$.

When the phase difference between LO and RF is higher than 0 but lower than $\pi/2$ ($0 < \theta_e < \frac{\pi}{2}$), the duty cycle of the output wave is between 100% and 50%, as shown in Figure 2.18.

When the phase difference between LO and RF is exactly $\pi/2$ ($\theta_e = \pi$), the result of mixer is a square wave with 50% duty cycle, as shown in Figure 2.19.

When the phase difference between LO and RF is higher than $\pi/2$ but lower than π

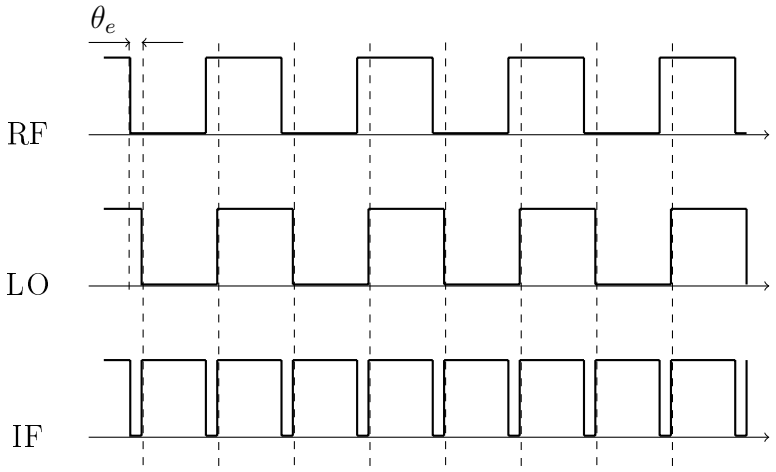


Figure 2.18 *The input and output waveforms of double-balanced diode mixer when* $0 < \theta_e < \frac{\pi}{2}$.

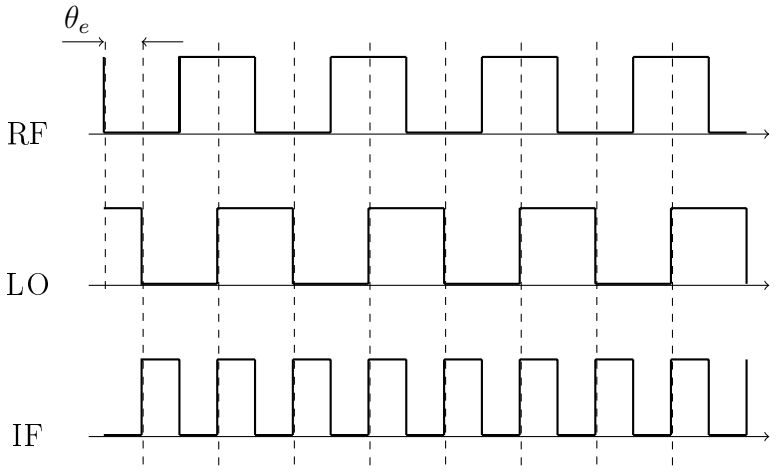


Figure 2.19 *The input and output waveforms of double-balanced diode mixer when* $\theta_e = \pi$.

($\frac{\pi}{2} < \theta_e < \pi$), the duty cycle of the output wave is between 50% and 0%, as shown in Figure 2.20.

When LO and RF are completely out of phase, $\theta_e = \pi$, the result of mixer is a square wave with 0% duty cycle, as shown in Figure 2.21.

Overall, the output signal u_{pd} at IF port is a square wave that has identical frequency with input signals. The duty cycle of u_{pd} is inversely proportional to θ_e:

$$\text{Duty cycle} = (1 - \frac{\theta_e}{\pi}) \times 100\%. \tag{2.20}$$

And the average voltage of u_{pd} is proportional to the duty cycle:

$$\bar{u}_{pd} = V_{pd} \times \text{Duty cycle}, \tag{2.21}$$

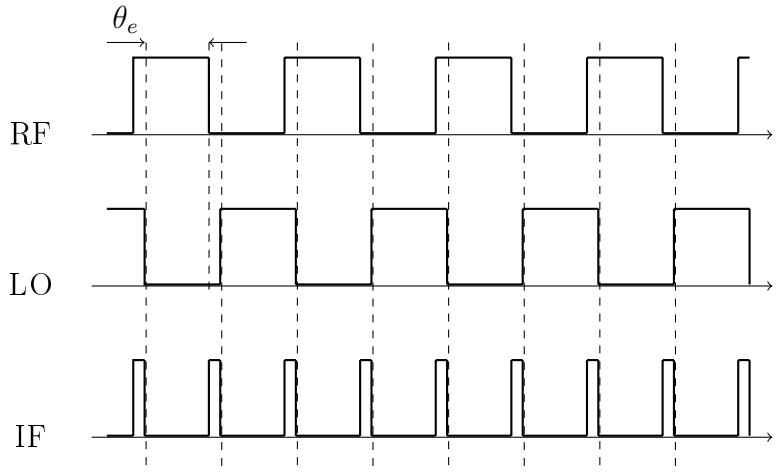


Figure 2.20 *The input and output waveforms of double-balanced diode mixer when* $\frac{\pi}{2} < \theta_e < \pi$.

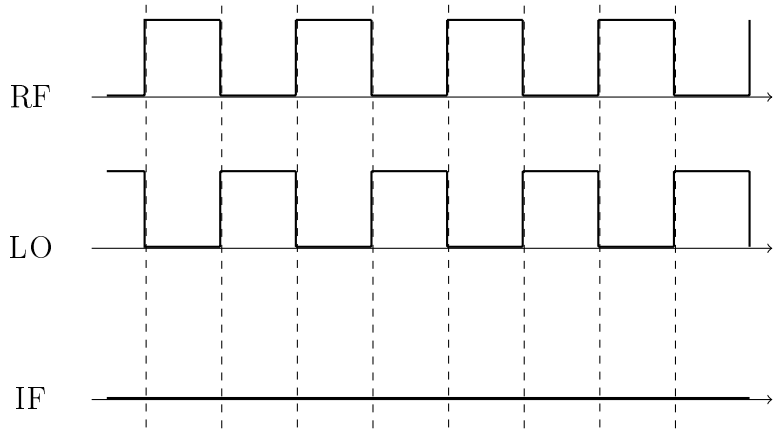


Figure 2.21 *The input and output waveforms of double-balanced diode mixer when* $\theta_e = \pi$.

where V_{pd} is the amplitude of u_{pd}.

Therefore, $\bar{u}_{pd}$ can be written as a function of θ_e:

$$\bar{u}_{pd} = V_{pd} \times (1 - \frac{\theta_e}{\pi}). \tag{2.22}$$

The relationship between θ_e and $\bar{u}_{pd}$ is plotted in Figure 2.22. It is a periodical triangle wave with period of 2π. The slope at $-\frac{\pi}{2}$ is also called the gain of this phase detector, which is calculated from:

$$K_d = \frac{\Delta\ \bar{u}_{pd}}{\Delta\ \theta_e} = \frac{V_{pd}}{\pi}. \tag{2.23}$$

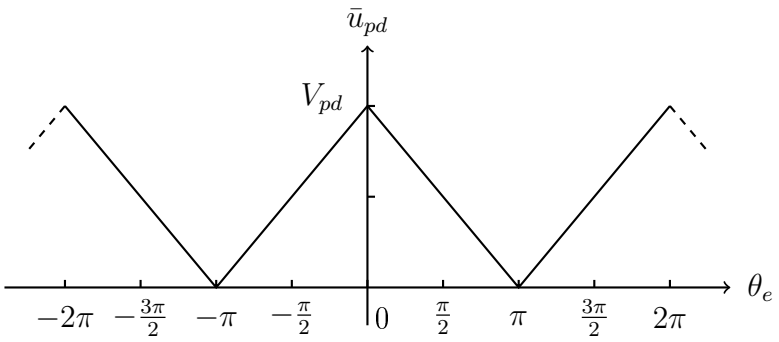


Figure 2.22 *The $\bar{u}_{pd}$ as a function of θ_e for double-balanced mixer.*

Exclusive-OR gate

The Exclusive-OR (XOR) gate is a simple logic gate, usually represented as shown in Figure 2.23. According to its truth table shown in Table 2.2, if input A and B are different, the XOR gate generates a logic "1", otherwise the output Q will be logic "0".

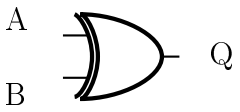


Figure 2.23 *Schematic symbol an XOR gate.*

Table 2.2 *The truth table of an XOR gate.*

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

Figures 2.24 - 2.28 depict the output waveforms of XOR gate when comparing two square waves of identical frequency. Basically, they are opposite to the results of double-balanced mixer. [2, p.52-55]

When $\theta_e = 0$, the result of XOR gate is shown in Figure 2.24. The duty cycle of square wave equals 0%.

When $0 < \theta_e < \frac{\pi}{2}$, see Figure 2.25, the duty cycle of the output is lower than 50%.

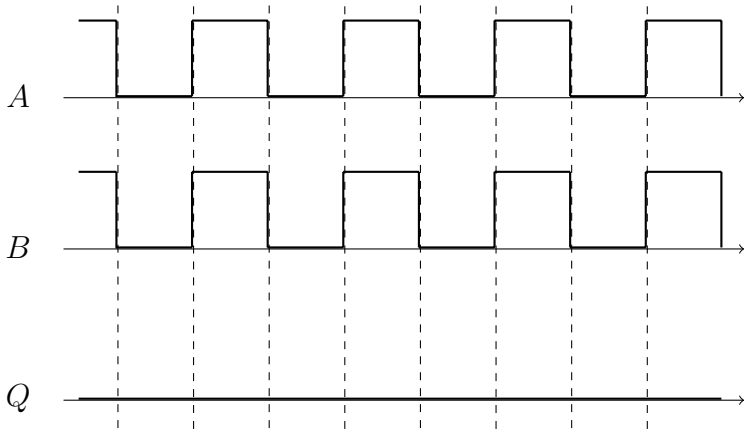


Figure 2.24 *The input and output waveform of XOR gate when* $\theta_e = 0$.

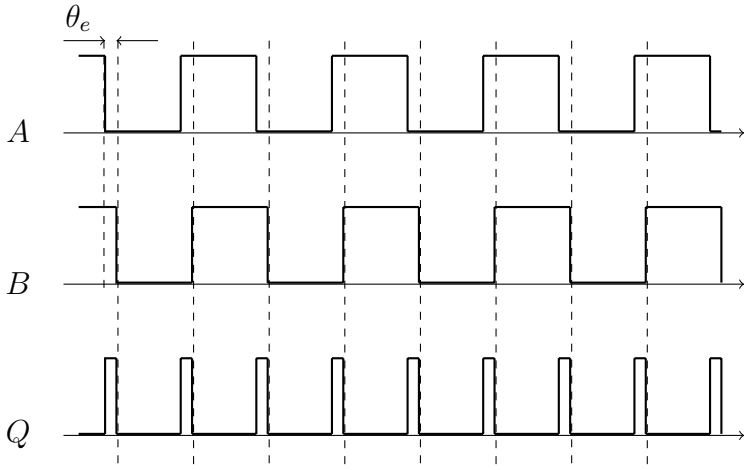


Figure 2.25 *The input and output waveform of XOR gate when* $0 < \theta_e < \frac{\pi}{2}$.

When $\theta_e = \pi/2$, the result of XOR gate is shown in Figure 2.26. The duty cycle of square wave is exactly 50%.

When $\frac{\pi}{2} < \theta_e < \pi$, see Figure 2.27, the duty cycle of the output is higher than 50%.

When $\theta_e = \pi$, two input signals are completely out of phase, the waveform is shown in Figure 2.28. The duty cycle of square wave reaches 100%.

The relationship between $\bar{u}_{pd}$ and θ_e can be described as:

$$\bar{u}_{pd} = V_{pd} \times \frac{\theta_e}{\pi}. \tag{2.24}$$

Figure 2.29 presents the $\bar{u}_{pd}$ as a function of θ_e for XOR gate. Maximum $\bar{u}_{pd}$ is achieved when input waves are out of phase by π, and minimum $\bar{u}_{pd}$ is obtained

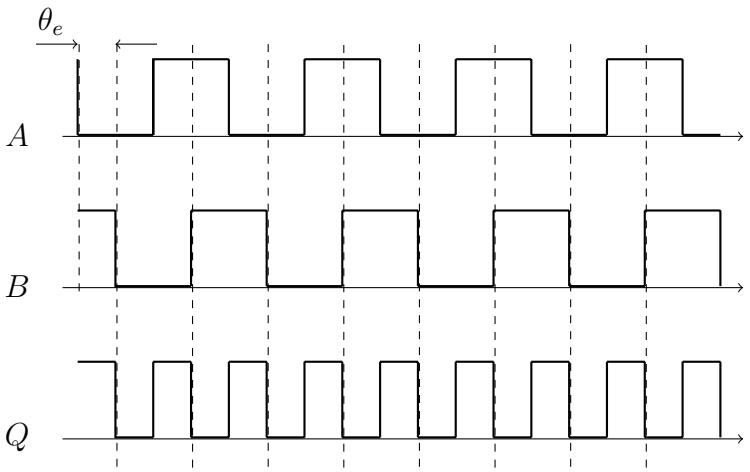


Figure 2.26 *The input and output waveform of XOR gate when* $\theta_e = \pi/2$.

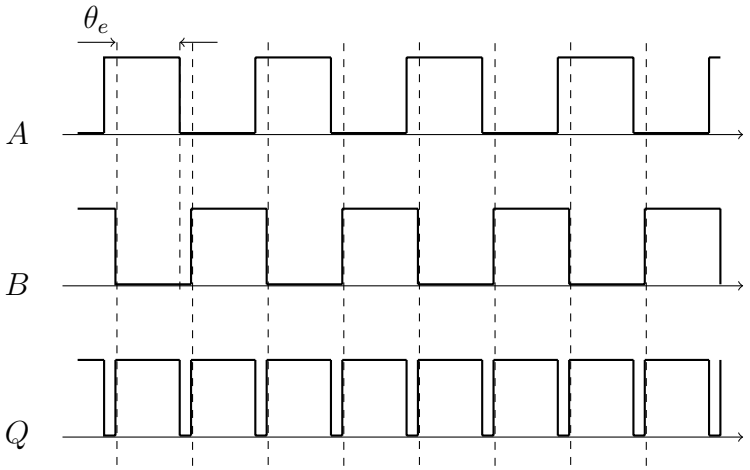


Figure 2.27 *The input and output waveform of XOR gate when* $\frac{\pi}{2} < \theta_e < \pi$.

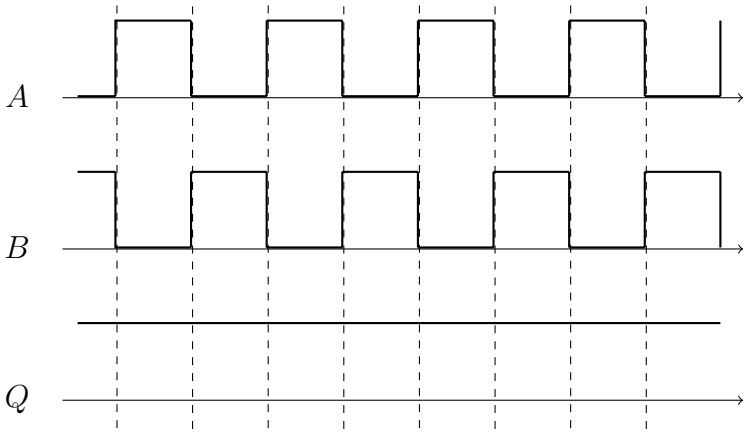


Figure 2.28 *The input and output waveform of XOR gate when* $\theta_e = \pi$.

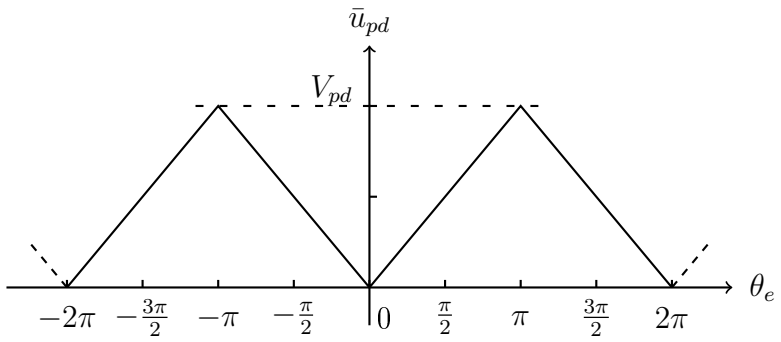


Figure 2.29 *The $\bar{u}_{pd}$ as a function of θ_e for XOR gate.*

when input waves are in phase. The slope at $\frac{\pi}{2}$ equals phase detector gain K_d:

$$K_d = \frac{\Delta\ \bar{u}_{pd}}{\Delta\ \theta_e} = \frac{V_{pd}}{\pi}. \tag{2.25}$$

2.3.5 Loop filters

The loop filter (LF) is invariably a low-pass filter (LPF). It is driven by the phase detector output u_{pd}, allowing frequencies that are lower than the cutoff frequency pass and filtering out undesired high frequency components. After passing the LPF, u_{pd} becomes the input control voltage of VCO. [2, p.33-34]

The order of a LPF equals the number of poles to its transfer function. Higher-order LPFs provide better performance in filtering, however on the other hand, lower-order system could be more stable. For real applications nowadays, second-order LPFs are mostly used. [2, p.60]

This work utilizes an RC low-pass filter, which is one of the simplest first-order LPFs [9, p.210]. It consists of a series resistor and a shunt capacitor, as shown in Figure 2.30. The corresponding transfer function can be obtained from:

$$\begin{aligned} H(j\omega) &= \frac{V_{out}}{V_{in}} = \frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}} \\ &= \frac{1}{1 + j\omega RC} \\ &= \frac{1}{1 + j\omega\tau}, \end{aligned} \tag{2.26}$$

where $\tau = RC$ is the time constant. The cutoff frequency $\omega_c = 1/\tau$ is defined as the point where the gain through the filter drops 3 dB. [11, p.386]

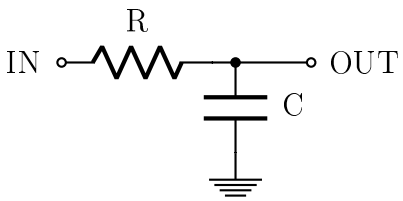


Figure 2.30 *An RC low-pass filter.*

Therefore the gain of LPF $K_f(s)$ in frequency domain is presented as:

$$K_f(s) = \frac{1}{1 + s\tau}, \tag{2.27}$$

where $s = j\omega$.

2.4 The control theory of PLL and key parameters

The gain of each block has been introduced in previous sections. Therefore, this closed-loop PLL system can be modeled as shown in Figure 2.31.

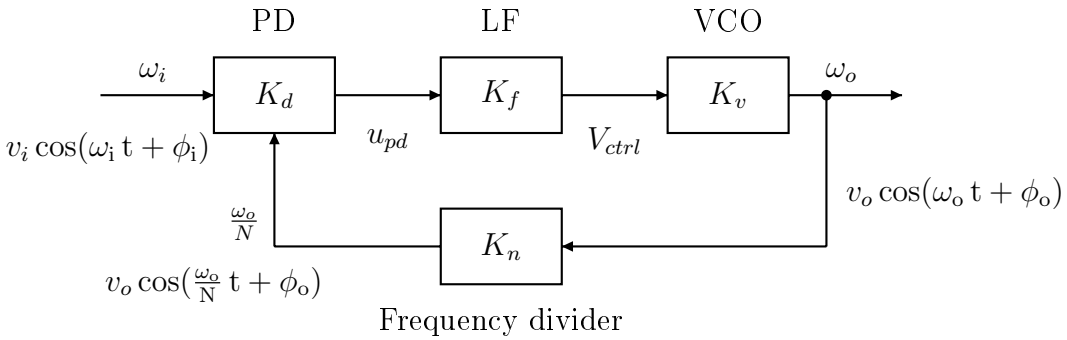


Figure 2.31 *The modeled PLL loop showing voltages and angular frequencies.*

Supposing that the reference signal is a wave with amplitude at v_i, angular frequency at ω_i and initial phase at ϕ_i, and the divided VCO output is another signal with amplitude at v_o, angular frequency at $\frac{\omega_o}{N}$ and initial phase at ϕ_o. As explained in Section 2.3.4, the phase detector compares the instantaneous phase of these two input signals, generating an AC signal u_{pd} of which average voltage is proportional to the phase difference θ_e. They can be expressed as:

$$\theta_i = \omega_i t + \phi_i, \tag{2.28}$$

$$\frac{\theta_o}{N} = \frac{\omega_o}{N} t + \phi_o, \tag{2.29}$$

$$\theta_e = \theta_i - \frac{\theta_o}{N} = (\omega_i - \frac{\omega_o}{N}) t + (\phi_i - \phi_o), \tag{2.30}$$

$$u_{pd} = K_d \theta_e. \tag{2.31}$$

After passing LF, u_{pd} is filtered and integrated, becoming a DC signal V_{ctrl}, provided that ω_i equals ω_o/N. It tunes the VCO and determines the output frequency ω_o.

$$V_{ctrl} = K_f\, K_d\, \theta_e, \tag{2.32}$$

$$\omega_o = K_v\, K_f\, K_d\, \theta_e + \omega_{min}. \tag{2.33}$$

If there is a difference in ω_i and $\frac{\omega_o}{N}$ at the beginning, θ_e would change from 0 to 2π periodically, therefore making V_{ctrl} also beat between V_{max} and V_{min}. It causes the ω_o swing between ω_{max} and ω_{min}. Meanwhile this variation of ω_o is fed back to phase detector, changing θ_e and tuning the VCO again continuously. Eventually the VCO generates an exactly same frequency as $N\omega_i$, θ_e becomes a constant, and the loop achieves locked state at this time.

There are two necessary requirements for locking the loop: $\frac{\omega_o}{N}$ equals ω_i and θ_e reaches a proper constant. During the settlement process, if frequency $\frac{\omega_o}{N}$ is equal to ω_i but θ_e is improper, ω_o may keep changing. The loop would not be locked until both two requirements are met. [4, p.604-605]

In this project, θ_e is supposed to equal $\pi/2$ when PLL is locked, because only at this time the control voltage V_{ctrl} reaches the center point, making the VCO create its center frequency, which is about 96 MHz.

As final constant θ_e is independent of the initial phases ϕ_i and ϕ_o, it can be assumed that both ϕ_i and ϕ_o are equal to 0, so that the reference signal becomes $v_i\, cos(\theta_i)$ while the VCO output becomes $v_o\, cos(\theta_o)$. The loop block diagram is then modified as shown in Figure 2.32.

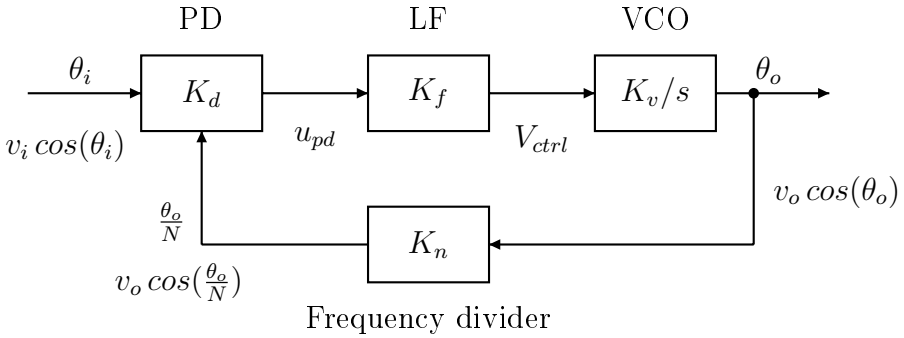


Figure 2.32 *The modeled PLL loop focused on phases.*

Hence, the output phase of VCO is obtained as:

$$\theta_o = \frac{K_v}{s}\, K_f\, K_d\, (\theta_i - K_n\, \theta_o), \tag{2.34}$$

and the closed-loop transfer function is given by:

$$H(s) = \frac{\theta_o}{\theta_i} = \frac{K_d\, K_f\, K_v}{s + K_n\, K_d\, K_f\, K_v}, \tag{2.35}$$

where the gains of the phase detector, the filter, the VCO and the divider are:

$$K_d = \frac{\Delta V}{\pi}\ \text{V/rad}, \tag{2.36}$$

$$K_f = \frac{1}{1 + s\tau}, \tag{2.37}$$

$$K_v = \frac{\Delta\,\omega}{\Delta V}\ \text{rad/s/V}, \tag{2.38}$$

$$K_n = \frac{1}{N}. \tag{2.39}$$

When the loop is locked, the divided frequency tracks the reference frequency, that is to say:

$$\frac{d\,\theta_i}{d\,t} = \frac{d\,K_n\,\theta_o}{d\,t}. \tag{2.40}$$

In order to analyze the stability of this system, the poles of closed-loop can be found from:

$$\begin{aligned} s + K_n\, K_d\, K_f\, K_v &= 0 \\ \Rightarrow s &= -\frac{\frac{1}{1+s\tau}\, K_d\, K_v}{N} \\ &= -\frac{1}{2\tau} \pm \sqrt{\left(\frac{1}{2\tau}\right)^2 - \frac{K_d\, K_v}{\tau\, N}}\ \text{rad/s}. \end{aligned} \tag{2.41}$$

According to the Nyquist stability criterion, the loop is unstable if the number of poles located in the right-half complex plane is not equal to zero.

The order number of a PLL equals the order number of the loop filter plus 1. This work applies simple first-order loop filter, hence it is a second-order PLL system, which is to say, the loop has two poles: one from LPF and the other one from VCO. Both two poles are supposed to be in the left-half plane.

The corresponding natural frequency ω_n and damping factor ζ are obtained from:

$$\omega_n = \sqrt{\frac{K_d\, K_v\, \omega_c}{N}}\ \text{rad/s}, \tag{2.42}$$

$$\zeta = \frac{\omega_c}{2\,\omega_n}. \tag{2.43}$$

Normally, ζ is selected to be between $1/\sqrt{2}$ and 1, to avoid damped or over-damped problems. [4, p.608]

Lock range ω_{cr} (also known as capture range) and locking time t_L (also known as settling time) are important parameters for analyzing this kind of traditional PLL system. The lock range means the loop is able to get locked rapidly within this frequency range. The lock time refers to the time that system needs to achieve locked state. [2, p.70-72]

Values of ω_{cr} and t_L are calculated from [2, p.101]:

$$\omega_{cr} = \sqrt{N\, K_d\, K_v\, \omega_c} \ \text{rad/s}, \tag{2.44}$$

$$t_L \approx \frac{2\pi}{\omega_n}\,\text{s}. \tag{2.45}$$

3. BLOCK DESIGN, CONSTRUCTION AND TESTING

Figure 3.1 shows the block diagram of this project. A 24-MHz sine-wave from crystal oscillator (XO) is divided by 4, while the output signal of 96-MHz voltage-controlled oscillator (VCO) is divided by 16. Two divided frequencies are compared by phase detector (PD), generating a signal that is proportional to the phase difference. This signal is then filtered by low-pass filter (LPF) and becomes the input control voltage of VCO.

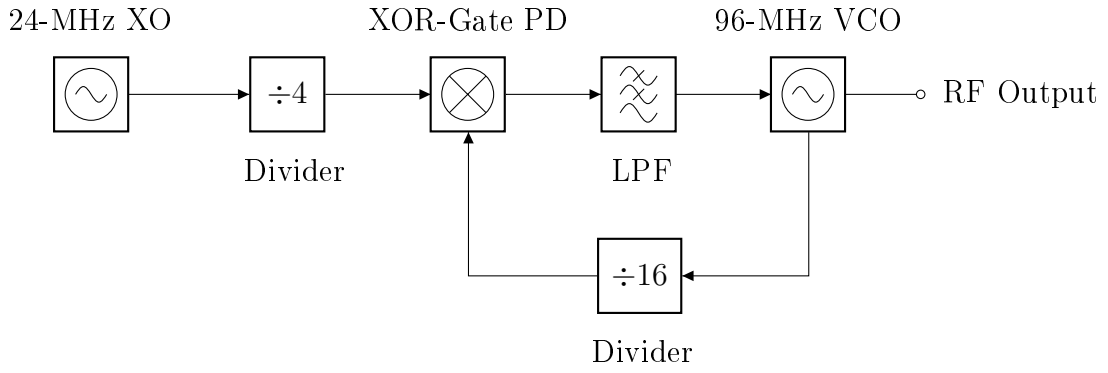


Figure 3.1 *The block diagram of PLL system for this project.*

The detailed design, construction and testing for each block are discussed in this chapter. The information on measurement setups can be found in Appendix.

3.1 Crystal oscillator design, construction and testing

A 24-MHz quartz crystal oscillator circuit is chosen for providing a stable reference signal at around 24 MHz. The circuit (see Figure 3.2) is designed based on Pierce oscillator (see Figure 2.6 in Section 2.3.1). An NPN-type bipolar junction transistor KSP10 works as the inverting amplifier, providing 180° phase shift. A 24-MHz quartz and capacitors C_1 and C_2 work as the feedback network, providing another 180° phase shift. Potentiometer R_b and resistor R_c are used for transistor biasing. Capacitor C_b is used for DC block.

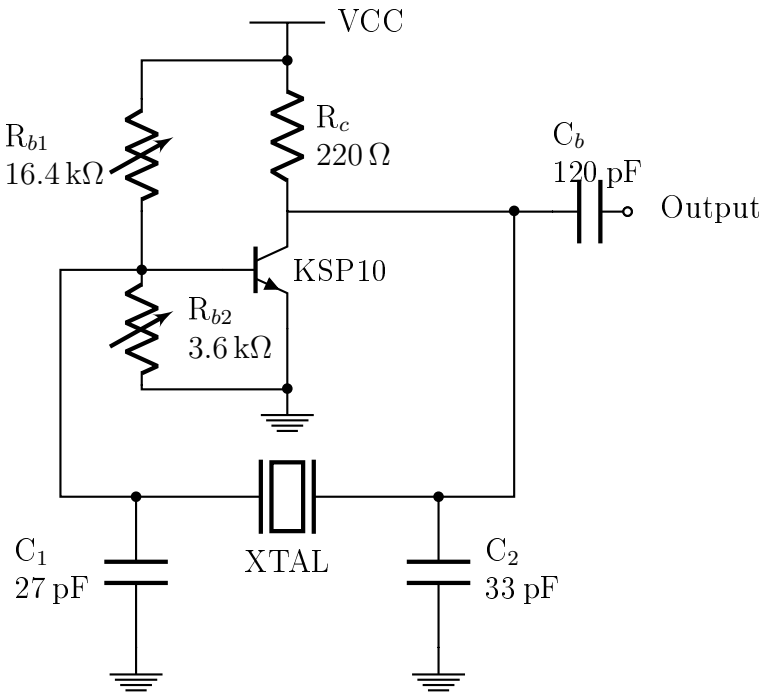


Figure 3.2 *The designed 24-MHz crystal oscillator circuit.*

The Pierce oscillator can work either at or slightly beyond the series resonant frequency of quartz crystal. Decreasing the value of C_1 and C_2 makes the operating frequency approach resonant frequency [12, p.249], and helps to improve the output power of oscillator. However, there is a lower bound for capacitors' value. The circuit does not oscillate any more if the value of capacitors are lower than this bound. [13, p.90]

Hence, the value of C_1 and C_2 must be selected carefully. Basically, their initial values can be calculated from an empirical formula [12, p.250]:

$$C_1 = C_2 = \frac{2000 \times 10^{-12}}{1 + 10^{-6} f} \text{ F}, \tag{3.1}$$

where f is the desired operating frequency in Hz. After trying and comparing different combinations of C_1 and C_2, the most proper group (C_1 =27 pF, C_2 =33 pF) is determined to be used for this oscillator.

By redrawing the circuit above, the final oscillator can be obtained as shown in Figure 3.3.

The constructed circuit shown in Figure 3.4 is tested under 6-V battery pack. The output signal observed through oscilloscope and spectrum analyzer are presented in Figure 3.5. The corresponding parameters are measured as shown in Table 3.1.

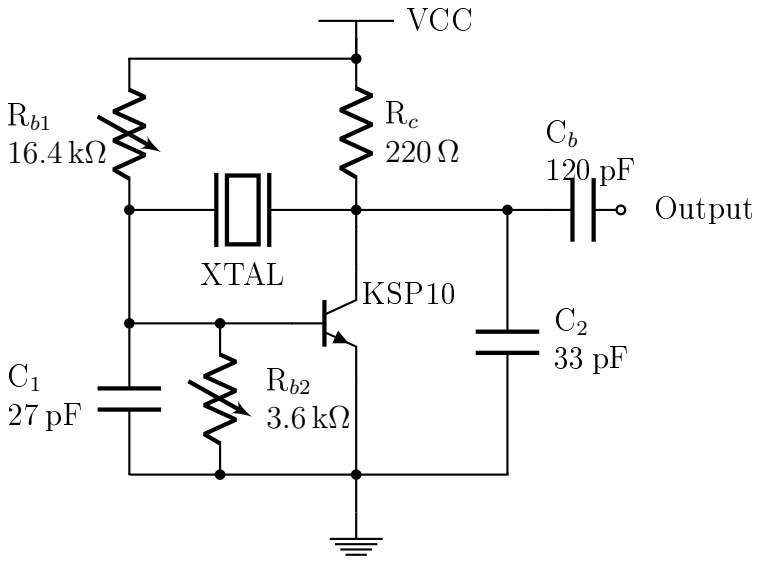


Figure 3.3 *The redrawn crystal oscillator circuit.*

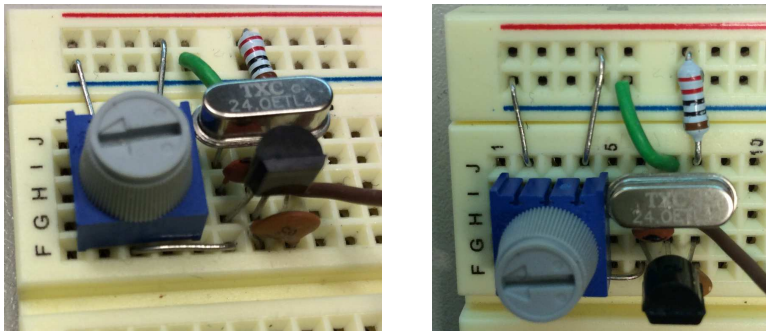
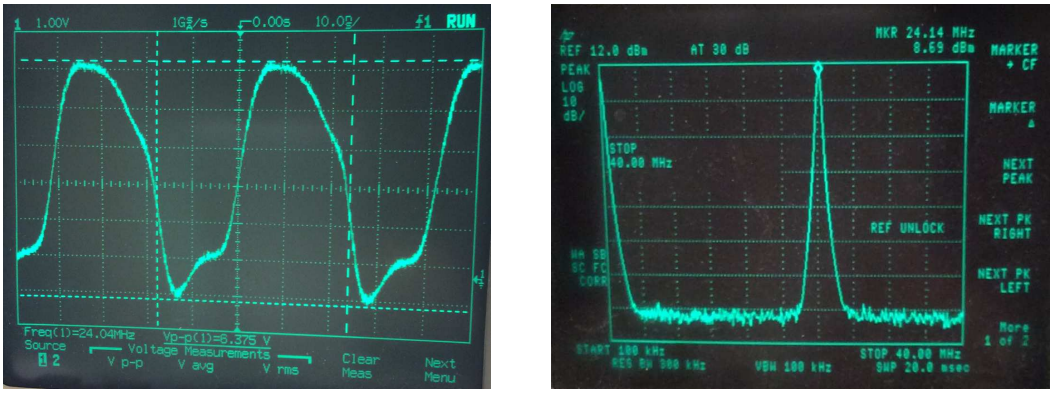


Figure 3.4 *The constructed 24-MHz crystal oscillator circuit.*



(a) (b)

Figure 3.5 *(a) The output signal of XO observed through oscilloscope and (b) observed through spectrum analyzer.*

Table 3.1 *Measured parameters of 24-MHz crystal oscillator circuit.*

Parameter	Value
f (Frequency)	24.04 MHz
V_{pp} across open circuit	6.375 V
V_{pp} across 50-Ω load	1.72 V
Current consumption	11.24 mA

3.2 Voltage-controlled oscillator design, construction and testing

The VCO circuit (drawn in Figure 3.6) is designed based on Clapp VCO (see Figure 2.9(b) in Section 2.3.2). The increase of input control voltage V_{ctrl} will cause a linear decrease of varactor capacitance, thereby result in the growth of output frequency.

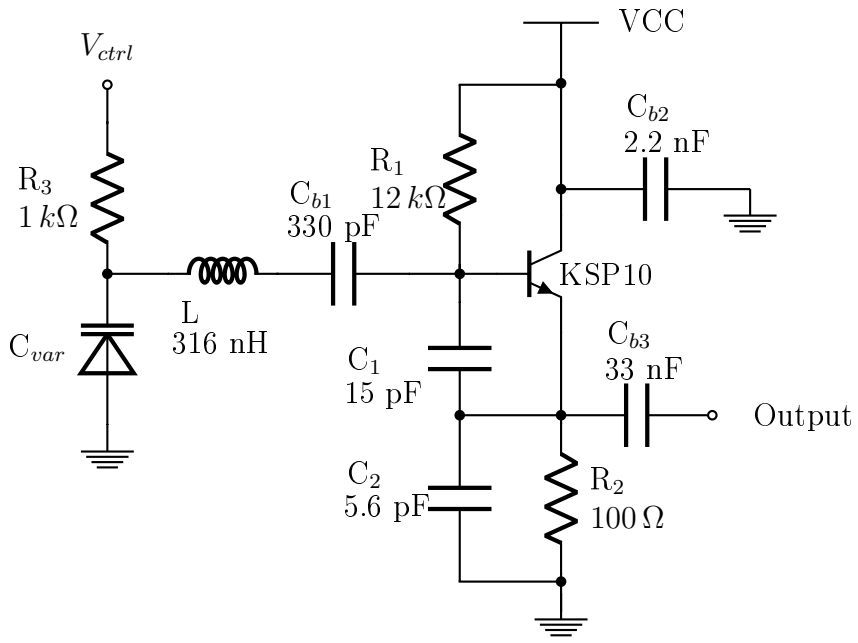


Figure 3.6 *The designed 96-MHz VCO circuit.*

A varactor BYV26C is used as the variable capacitor C_{var}, in series with an air-wound coil inductor L. Resistors R_1 and R_2 are used for biasing, while R_3 is used for limiting current. Capacitors C_{b1}, C_{b2}, and C_{b3} are used as DC blocks, C_1 and $C2$ help to construct the frequency selective network. The transistor KSP10 is selected

again as amplifier.

To determine the value of capacitors and inductor, it is required to decide the minimum output frequency ω_{min} and maximum output frequency ω_{max} at first. In this case the desired center frequency is 96 MHz, which is to say, the ideal VCO circuit is supposed to generate a signal at frequency between 86 MHz and 106MHz if the bandwidth could reach 20 MHz.

BYV26C is a diode with glass passivated junction, its reverse voltage can reach 600 V [14, p.1]. The capacitance of diode changes from approximately 36 pF to 15 pF when reverse voltage increases from 0 to 6 V, as shown in Figure 3.7 [14, p.3].

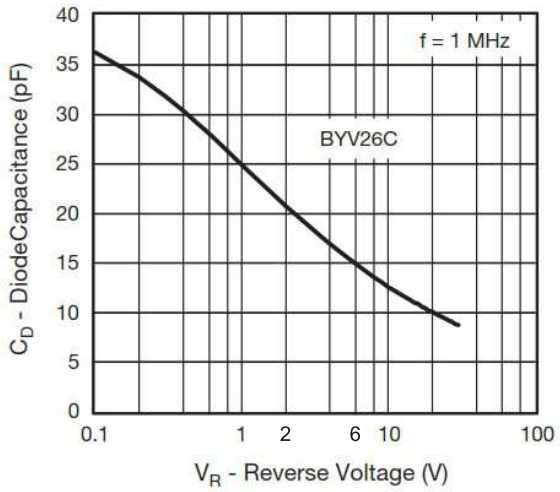


Figure 3.7 *The diode capacitance of BYV26C as a function of its reverse voltage.*

For stable oscillation, C_1 and C_2 should be much larger than C_{var}. However, in practice the output power optimization requires low values for C_1 and C_2. Like in crystal oscillator design, they need to be adjusted according to the practical circuit. [9, p.606-607]

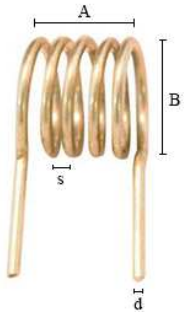


Figure 3.8 *An air-wound coil.*

Air-wound coil inductors are widely used at frequencies between 10 MHz and 1 GHz [15, p.217-218]. It can be made from wounding a wire, as shown in Figure 3.8. The

value of coil inductor L can be computed from Equation 2.11 and 2.12 (see Section 2.3.2), when capacitors are known. Then the inductor size can be decided based on the Wheeler Equation 3.2 [15, p.218].

$$L = \frac{B^2 n^2}{0.45B + A}, \tag{3.2}$$

where L is the inductance of coil in nH, B is the average diameter of coil in mm, n is the number of turns, A is the length of coil in mm. For the coil inductor applied in this work, $A = 11$, $B = 10$, $n = 7$, so the calculated L equals 316 nH.

However, an air-wound coil also has parasitic capacitance as other types of inductors, which is supposed to be taken into consideration. As discussed in [15, p.219], the distributed capacitance C in pF per turn is calculated from:

$$C \approx \frac{B\epsilon_{eff}}{11.45 \cosh^{-1} \frac{s}{d}}, \tag{3.3}$$

where ϵ_{eff} is the effective dielectric constant between turns, s is the spacing between turns at wire centers in mm, and d is the diameter of wire in mm. For the inductor in this work, $s = 2.2$, $d = 0.7$, $\epsilon_{eff} \approx 8.85 \times 10^{12}$ F/m. The calculated capacitance per turn is about 0.09 pF.

Nevertheless, the total parasitic capacitance is not simply the series of each C because of the existing of coupling among nonadjacent turns [15, p.219]. Consequently, it is hard to obtain an accurate real parasitic capacitance. This parasitic capacitance will result in the decrease of VCO output frequency ω_o. For this reason, the values of C_1 and C_2 may have to be tuned in the actual circuit. In the end, C_1 was 15 pF and C_2 was 5.6 pF.

The constructed 96-MHz VCO circuit shown in Figure 3.9 is powered from a 5-V DC power supply. The output frequency f_o is recorded when input control voltage V_{ctrl} ranges from 0 to 6V, as depicted in Figure 3.10. Recorded results are listed in Appendix, and the characteristic is plotted in Figure 3.11.

This VCO is tunable between 86 MHz and 100 MHz with maximum 6-V V_{ctrl}. In addition, the gain of VCO (K_v) slightly decreases during the growth of V_{ctrl}. The desired center frequency 96 MHz is obtained with 2.7-V V_{ctrl} (see Figure 3.12). Figure 3.13 presents a clean output waveform observed through oscilloscope. The measured parameters are listed in Table 3.2.

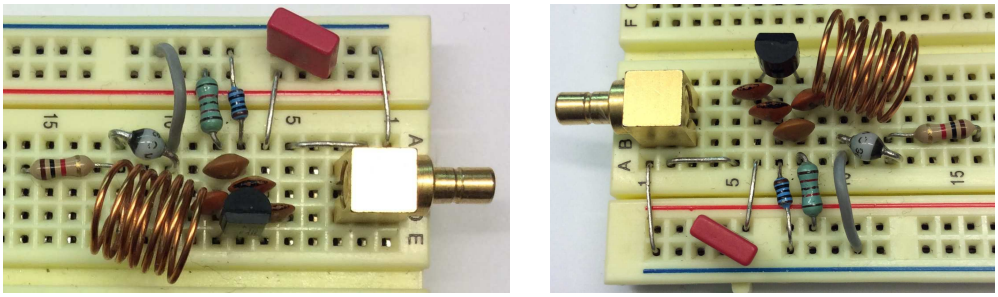


Figure 3.9 *The constructed 96-MHz VCO circuit.*

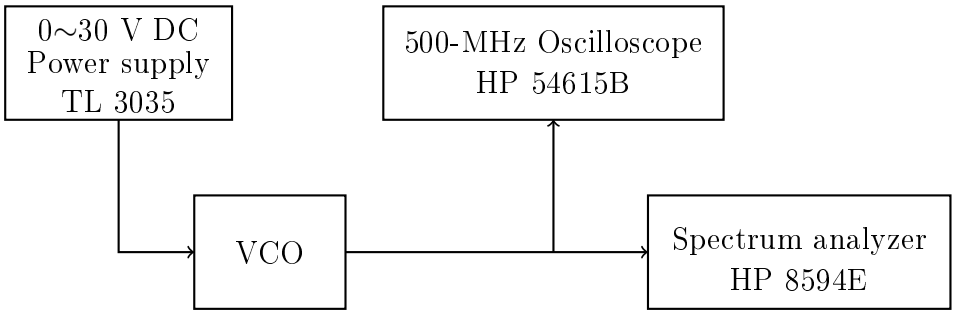


Figure 3.10 *Measurement setup for VCO test.*

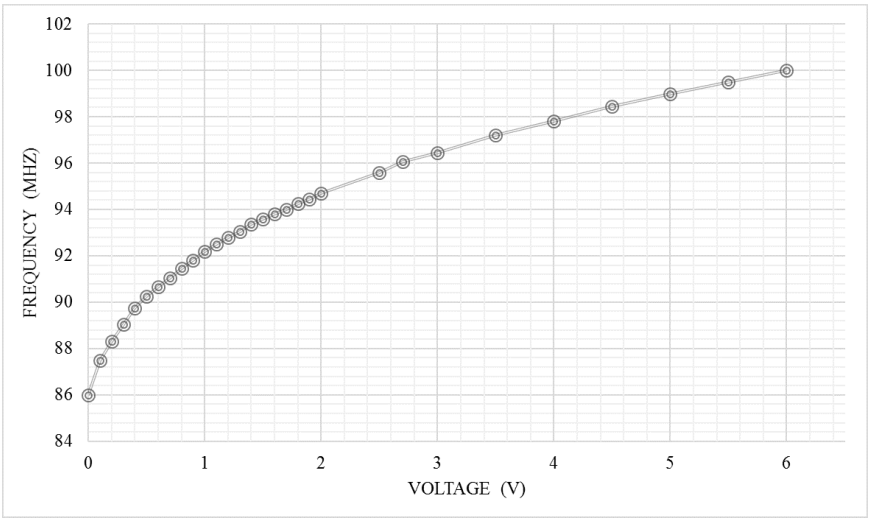


Figure 3.11 *The output frequency of the VCO (f_o) as a function of input control voltage (V_{ctrl}).*

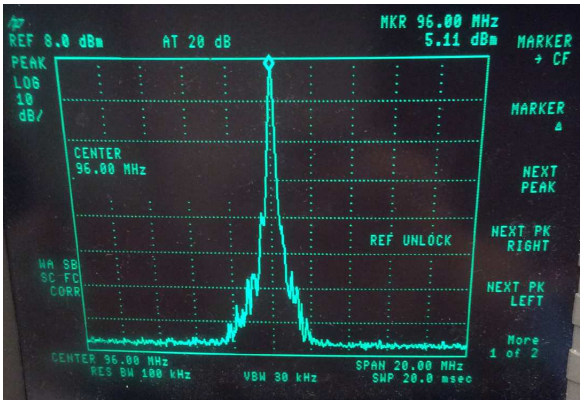


Figure 3.12 *The VCO output measured by spectrum analyzer with 2.7-V V_{ctrl}.*

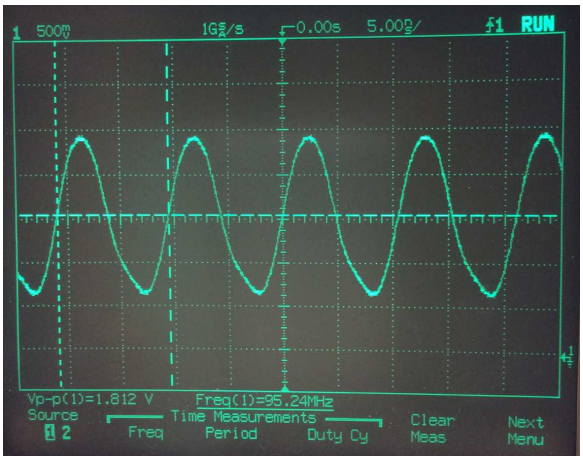


Figure 3.13 *The output waveform of 96-MHz VCO circuit observed through oscilloscope.*

The average VCO gain $\bar{K}_v$ is computed from:

$$\bar{K}_v = \frac{\Delta\,\omega}{\Delta V} = \frac{2\pi \cdot 14\,\text{MHz}}{6\,V} = 2\pi \cdot 2.33\,\text{MHz/V}. \tag{3.4}$$

The maximum K_v is obtained from:

$$K_v|_{0\sim0.5V} = \frac{\Delta\,\omega}{\Delta V} = \frac{2\pi \cdot 4.25\,\text{MHz}}{0.5\,V} = 2\pi \cdot 8.5\,\text{MHz/V}. \tag{3.5}$$

The K_v around center point is obtained from:

$$K_v|_{2.5\sim3V} = \frac{\Delta\,\omega}{\Delta V} = \frac{2\pi \cdot 0.85\,\text{MHz}}{0.5\,V} = 2\pi \cdot 1.7\,\text{MHz/V}. \tag{3.6}$$

Table 3.2 *Measured parameters of 96-MHz VCO circuit.*

Parameter	Value
ω_{min}	2π·86 MHz
ω_{max}	2π·100 MHz
V_{pp} across open circuit	1.812 V
V_{pp} across 50-Ω load	1.11 V
Current consumption	13 mA

3.3 Frequency divider design, construction and testing

74AC74 is an IC chip that integrates two D-type positive edge-triggered flip-flops. As shown in Figure 3.14, it has 14 pins in total, containing two data inputs D_1, D_2, two clock pulse inputs CP_1, CP_2, four outputs Q_1, $\bar{Q}_1$, Q_2, $\bar{Q}_2$, two direct clear inputs $\bar{C}_{D1}$, $\bar{C}_{D2}$ and two direct set inputs $\bar{S}_{D1}$, $\bar{S}_{D2}$, which enable the chip. Table 3.3 presents its truth table. The clear and set inputs are connected to logic high during the test. [16]

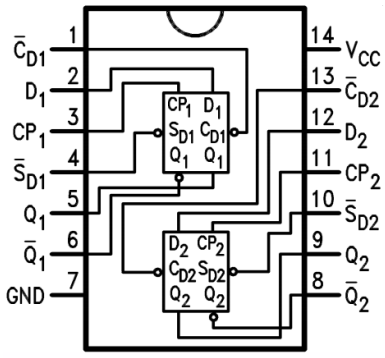


Figure 3.14 *The pin diagram of 74AC74.*

As mentioned in Section 2.3.3, a divide-by-2^N circuit can be realized by cascading N D flip-flops. In this work, two 74AC74 ICs are cascaded to divide VCO output by 16 while another 74AC74 is used to divide XO output by 4. Figures 3.15 and 3.16 present the connection diagrams. R_1 and R_2 are used to ensure that the DC level of input signals equals the center point of supply voltage, otherwise the IC may be unable to work.

The maximum clock frequency of 74AC74 under 5-V power supply is expected to

Table 3.3 *The truth table of 74AC74.*

$\bar{S}_D$	$\bar{C}_D$	CP	D	Q_{n+1}	$\bar{Q}_{n+1}$
L	H	×	×	H	L
H	L	×	×	L	H
L	L	×	×	H	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	×	Q_n	$\bar{Q}_n$

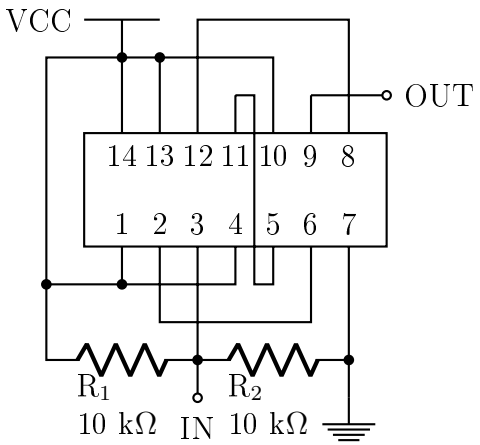


Figure 3.15 *The connection diagram of by-4 divider.*

reach 125 MHz [16]. When powered by 5-V DC voltage, a by-4 divider is able to handle input frequencies from about 930 kHz to 125 MHz, except 12∼13 MHz. According to the test results, the recommended input power of clock signal for driving the divider is above 12 dBm (approximately 2.5-V peak-to-peak). The chip can handle most clock frequencies lower than 125 MHz with such amplitude. Higher input power would be required if clock frequency approaches the limitation. In addition, the measured current consumption of one IC is 11.5 mA.

It is noticeable that all input signals in previous tests are sinusoidal waves. The divider would present better performance, for instance, covering greater frequency range and requiring lower input power when it is fed by a clean square wave, because square wave spends shorter time to transit from logic low to high.

The constructed divide-by-4 and divide-by-16 circuits shown in Figure 3.17 are tested under 6-V battery pack. The upper left pin is connected to power supply and lower right pin is connected to ground for all chips. In by-16 divider, two 10-nF

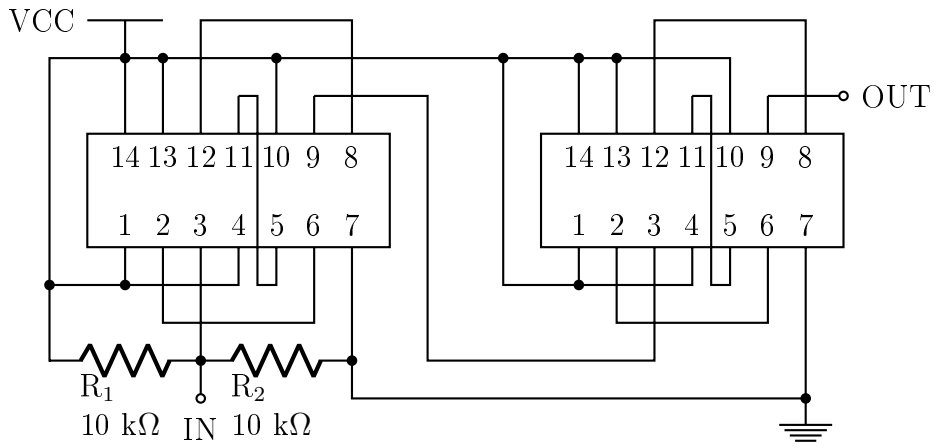
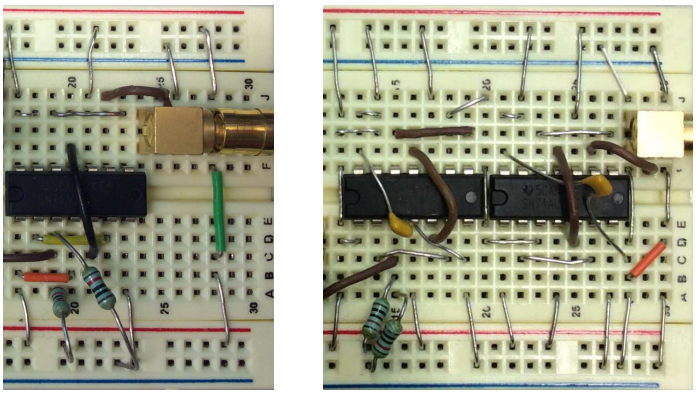


Figure 3.16 *The connection diagram of by-16 divider.*

capacitors are placed between power supply pin and ground pin for filtering.



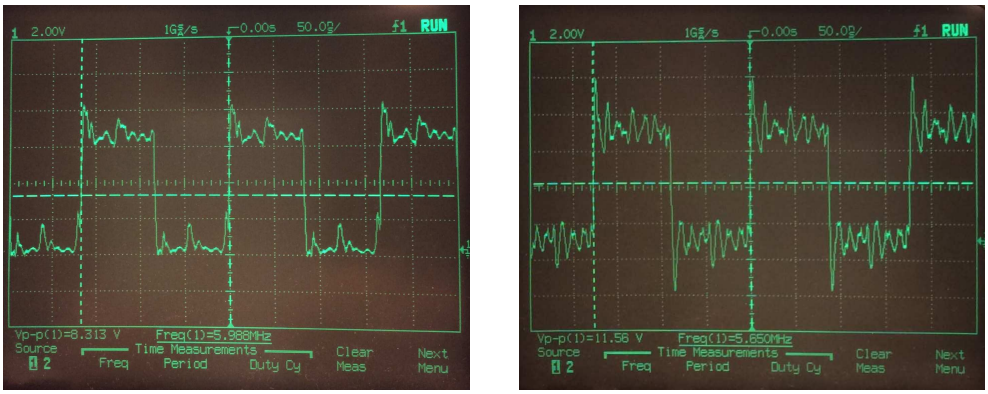
(a) (b)

Figure 3.17 *(a) The constructed by-4 divider for XO and (b) the constructed by-16 divider for VCO.*

As presented in Figure 3.18, both the divided XO output and VCO output have correct frequency, though containing high-frequency harmonies.

3.4 Phase detector design, construction and testing

The phase detector plays a vital role in PLL circuits. As mentioned in Section 2.3.4, there are several options for realizing phase detection. In this project, both double-balanced mixer and Exclusive-OR (XOR) gate have been tested, and the XOR gate is selected in the end. The detailed comparison will be discussed in Chapter 4. In brief, the average voltage of double-balanced mixer output signal has limited range, while the XOR gate has the drawback of frequency limitation.



(a) (b)

Figure 3.18 *(a) Divided XO signal and (b) divided VCO signal.*

The simulation of detecting two different frequencies by XOR gate is done with Multisim. The schematic is shown in Figure 3.19 and a part of waveforms is presented in Figure 3.20. The XOR gate compares a 100-Hz square wave and a 90-Hz square wave, which are indicated by green and light blue waves respectively in the figure. The red wave represents the output of XOR gate before RC low-pass filter while the dark blue wave represents the filtered output. It is obvious that the red one is a periodical signal of which frequency equals the difference between two inputs (10 Hz). In addition, the duty cycle of square wave changes regularly from 0% to 100% then back to 0%, causing the instantaneous voltage of filtered signal beat between maximum and minimum slowly.

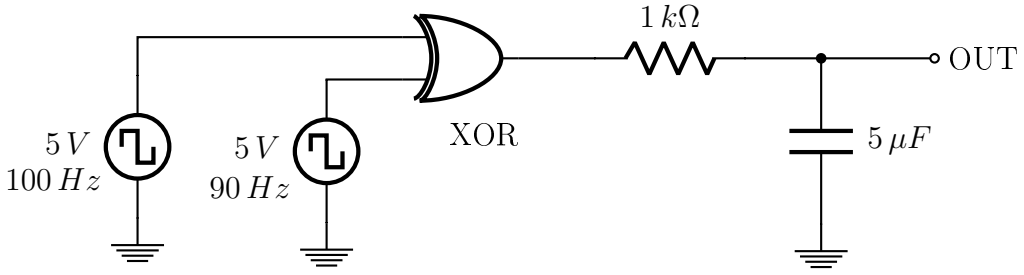


Figure 3.19 *The schematic for phase detector testing.*

The final design for this project is to detect two 6-MHz input signals using a chip CD4070BE. CD4070 Series (manufactured by Texas Instruments) are cheap and usual CMOS IC chips. The package of CD4070BE is PDIP, suitable for breadboard. As shown in Figure 3.21(a), it has 14 pins, contains 4 XOR gates in total. However, only one XOR gate is used in this project.

The IC is connected as presented in Figure 3.21(b). The capacitors are used for filtering and resistors help maintain a proper DC level. Pin 14 and pin 7 are connected to VCC and GND respectively. Pin 5 and pin 6 are connected to input while

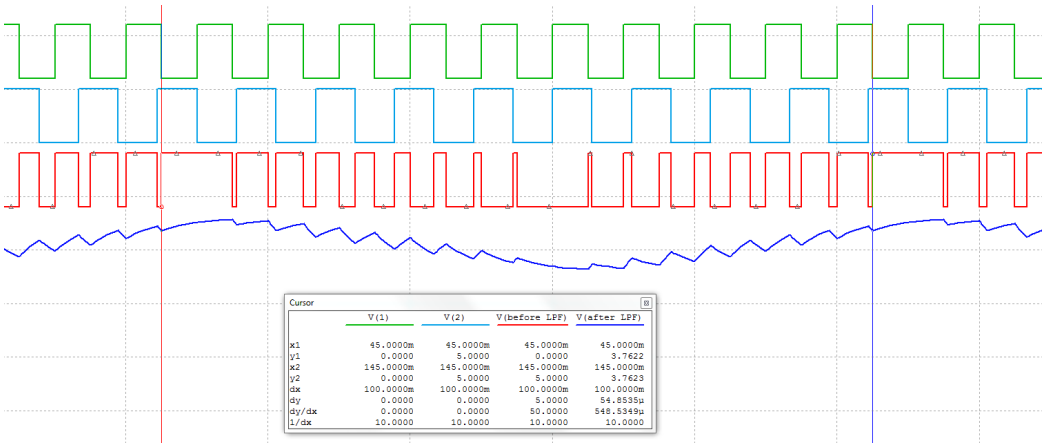


Figure 3.20 *The input and output waveform of phase detector.*

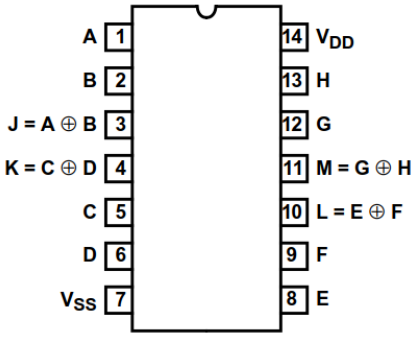
pin 4 is the output. Other pins are not connected. [17]

The constructed phase detector shown in Figure 3.22 is powered by 6-V DC power supply. The upper left pin is connected to supply voltage and lower right pin is connected to ground. A 4.7-μF capacitor is placed between these two pins for filtering.

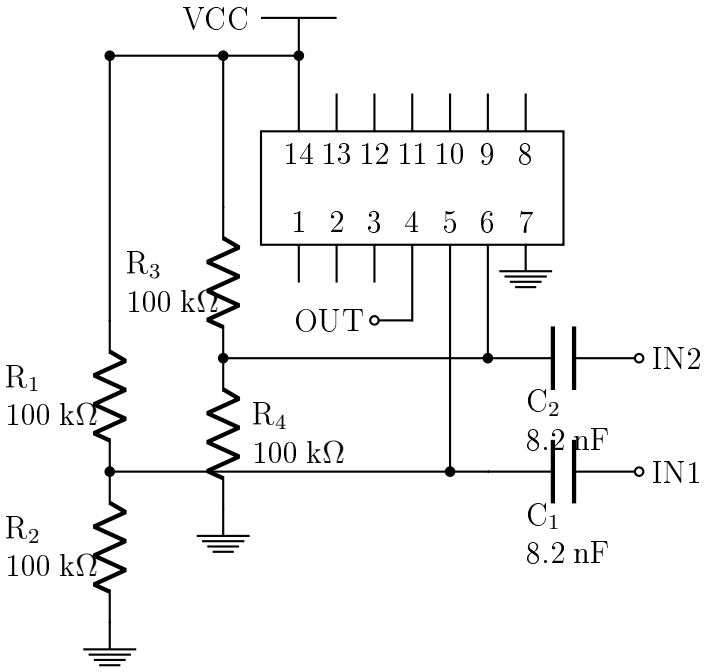
The output waveform of detecting two signals of 6 MHz is shown in Figure 3.23. It appears as a sine-wave more than square wave at around 6 MHz.

For comparison, much lower frequencies are detected. Figure 3.24 shows the output waveform of detecting two signals of 10 kHz, it is approaching a square wave. It can be concluded that the transition and propagation delay of internal circuitry may influence the performance of IC, determine the upper limitation of its operating frequency as well.

The gain K_d is measured by means of changing the phase difference θ_e and recording the corresponding average output voltage $\bar{u}_{pd}$, as shown in Figure 3.25. Two input waves are obtained by splitting a signal from function generator to ensure the frequencies are identical. Different electrical lengths of the cable results in different phase, so θ_e can be modified by changing the length of cable or changing the source frequency. The output waveform of detecting two square waves at about 4.8 MHz are presented in Table 3.4. The reason why 6-MHz signals were not used but 4.8-MHz signals, instead, was a 50-m long cable provides around 90° phase difference at 4.8 MHz.



(a)



(b)

Figure 3.21 *(a) The pinouts of CD4070BE and (b) the connection way of CD4070BE in this project.*

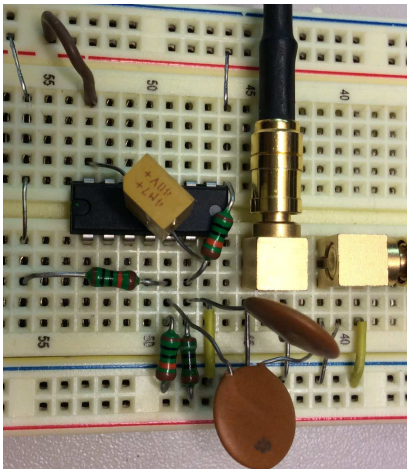


Figure 3.22 *The constructed phase detector.*

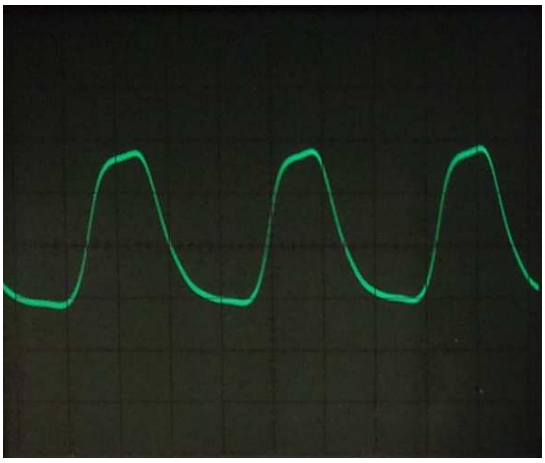


Figure 3.23 *The output waveform of detecting two signals of 6 MHz (seconds/division 50 ns, volts/division 2 V).*

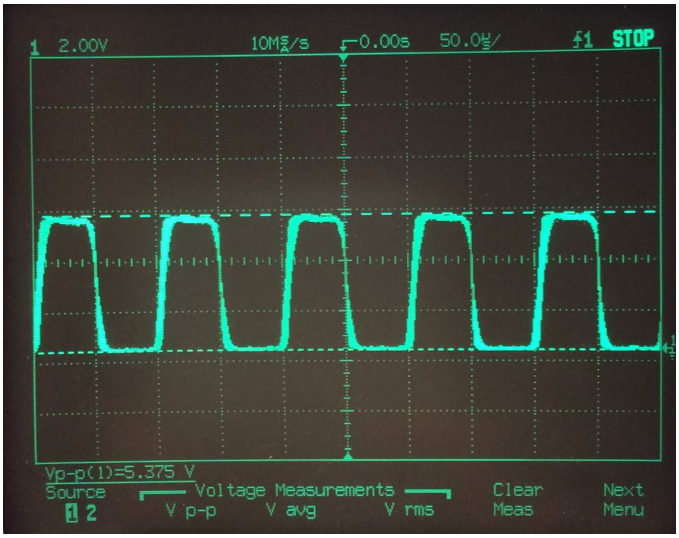


Figure 3.24 *The output waveform of detecting two signals of 10 kHz (seconds/division 50 µs, volts/division 2 V).*

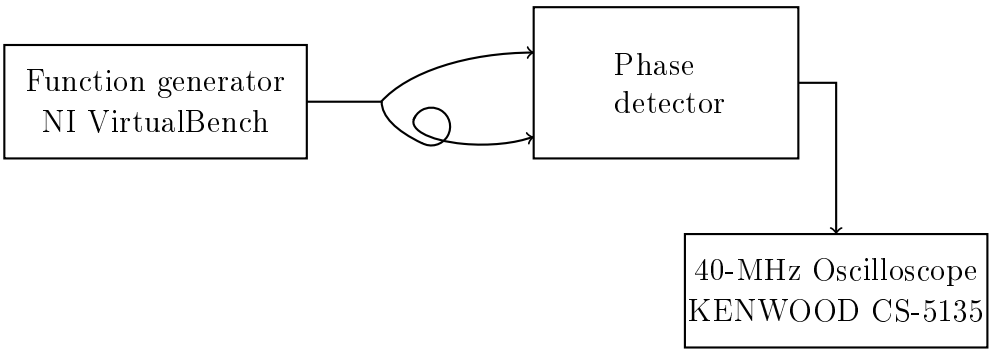


Figure 3.25 *Measurement setup for measuring K_d.*

Table 3.4 *The result of detecting two 4.8-MHz square waves.*

θ_e (in Degrees)	$\bar{u}_{pd}$ (in Volts)
87	1.8
88	2.4

Therefore K_d is computed from:

$$\begin{aligned} K_d &= \frac{\Delta\,\bar{u}_{pd}}{\Delta\,\theta_e}\ \text{V/rad} \\ &= \frac{2.4-1.8}{88-87}\cdot\frac{180}{\pi}\ \text{V/rad} \\ &\approx 34\ \text{V/rad} \end{aligned} \tag{3.7}$$

During the test, it is also found that the amplitude of input signals should keep the same level with supply voltage, otherwise the IC will work improperly. The measured current consumption of CD4070BE is about 9 mA under 6-V power supply.

3.5 Loop filter design, construction and testing

The simple first-order RC low-pass filter (LPF) is selected for this work to filter unwanted high-frequency components and let low frequency pass.

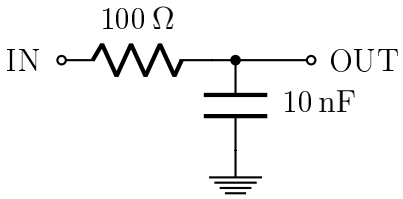


Figure 3.26 *The RC low-pass filter.*

The resistor R and capacitor C may be changed according to the practical circuitry to achieve a best performance for PLL loop. The final decided components for this filter are a 100-Ω resistor and a 10-nF capacitor.

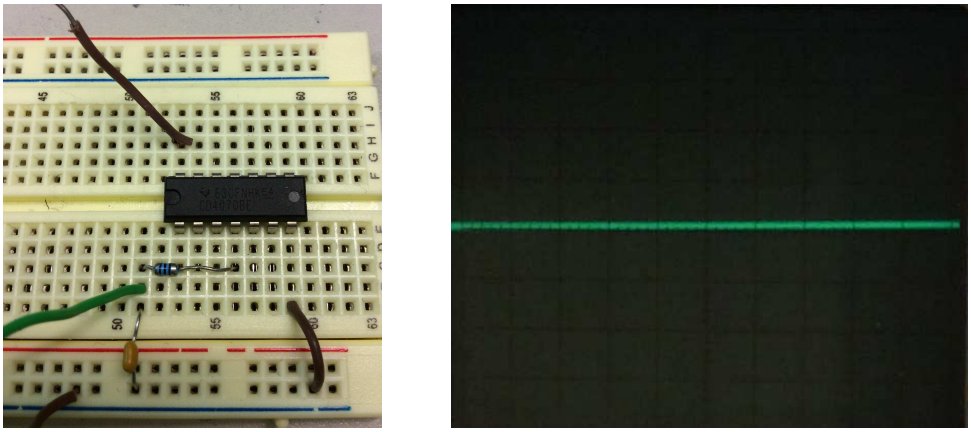
The cutoff frequency ω_c of designed LPF in Figure 3.26 and its gain are given by:

$$\omega_c = \frac{1}{RC} \text{ rad/s} = 1 \text{ MHz}, \tag{3.8}$$

$$f_c = \frac{1}{2\pi RC} \text{ Hz} \approx 159 \text{ kHz}, \tag{3.9}$$

$$K_f = \frac{1}{1 + s \cdot 10^{-6}}. \tag{3.10}$$

The constructed LPF is presents in Figure 3.27(a), the resistor is placed between output of phase detector and a shunt capacitor. The waveform shown in Figure 3.23 is transformed to a 2.1-V DC signal shown in Figure 3.27(b) after passing the LPF.



(a) (b)

Figure 3.27 *(a) The constructed LPF circuit and (b) the output waveform of LPF (volts/division 500 mV, lowest line as ground level).*

4. RESULTS AND ANALYSIS

This chapter discusses the challenges encountered during this work and corresponding solutions to them, and presents the measurement results. Sections 4.1 and 4.2 provide the analysis on the phase detector and the frequency divider, respectively. Section 4.3 shows the results of whole system. The information on measurement setups is presented in Appendix.

4.1 Analysis of the phase detector

The initial idea is to divide the VCO output by 4, obtaining a frequency which is tunable between around 21.5 MHz and 25 MHz. The XOR gate phase detector is expected to compare this divided signal directly with 24-MHz XO output. As shown in Figures 2.24 - 2.28, XOR gate is supposed to generate a square wave of which duty cycle changes between 0% and 100%. However, the IC CD4070BE has a drawback of insufficient operation speed. Even though its datasheet does not present the information related to its maximum operating frequency, the parameters of transition time and propagation delay time can be found, as presented in Table 4.1 [17, p.5].

Table 4.1 *Transition time and propagation delay time of CD4070BE.*

Parameter	V_{DD}(V)	Typical	Maximum	Units
t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	ns
	15	40	80	ns
t_{PHL}, t_{PLH}	5	140	280	ns
	10	65	130	ns
	15	50	100	ns

V_{DD} is the supply voltage of IC, t_{THL} and t_{TLH} represent the required time that output signal transits between logic high and low, t_{PHL} and t_{PLH} represent the

required time that the signal propagates from input to output. Besides, input t_r and t_f represent the time that input signal changes between logic high and low. They are specified to be 20 ns. Basically the propagation delay time t_{PHL} and t_{PLH} are not taken into consideration, because it does not affect the shape of output waveform. Supposing the output signal falls down as soon as it rises up, becoming a triangle wave. The output frequency under 5-V supply voltage is:

$$f = 1/T = 1/200 \text{ ns} = 5 \text{ MHz}, \tag{4.1}$$

based on *typical* value of transition time. The upper limitation frequency would fall down to 2.5 MHz if transition time reaches its *maximum*. This frequency can be improved with higher supply voltage. However, it may not exceed 10 MHz even under 10-V supply voltage. Obviously, it is impossible to handle 24-MHz signal for this XOR gate.

Therefore, an IC named SA602A is considered for replacing XOR gate. It integrates a double-balanced mixer and some parts of a crystal oscillator, as shown in Figure 4.1 [18, p.2]. The double-balanced mixer creates similar results as XOR gate, see Figure 2.17 - 2.21. The input frequency of this mixer could reach 500-MHz [18, p.8]. In addition, the entire circuitry is simplified due to the integration of this chip.

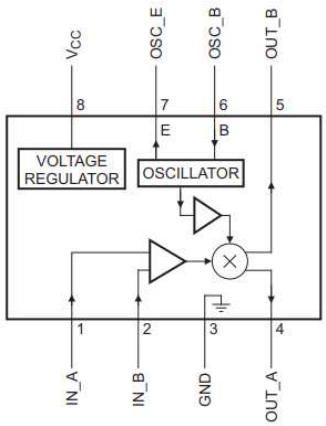


Figure 4.1 *The diagram of SA602A.*

In order to test this mixer, the IC is connected as shown in Figure 4.2, and powered by 5-V DC voltage supply. Two input sinusoidal signals at 1 MHz are fed from separate signal generators.

The output signal observed through oscillator presents a slowly changing waveform when two input frequencies are pretty close to each other. Figure 4.3 shows some states of the output. The problem is that the average voltage of output is limited between about 0.8 V and 2.8V, consequently causing the decreasing of VCO tuning

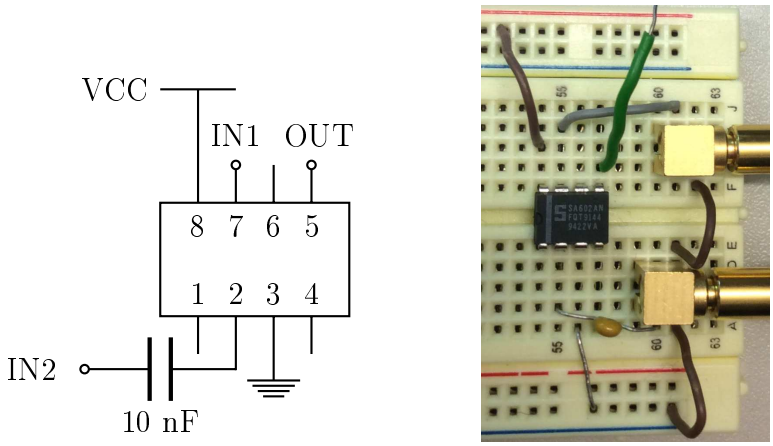


Figure 4.2 *(a) The connection way of SA602A for testing, and (b) the constructed circuit of SA602A for testing.*

range. This result is independent on either supply voltage or input amplitude.

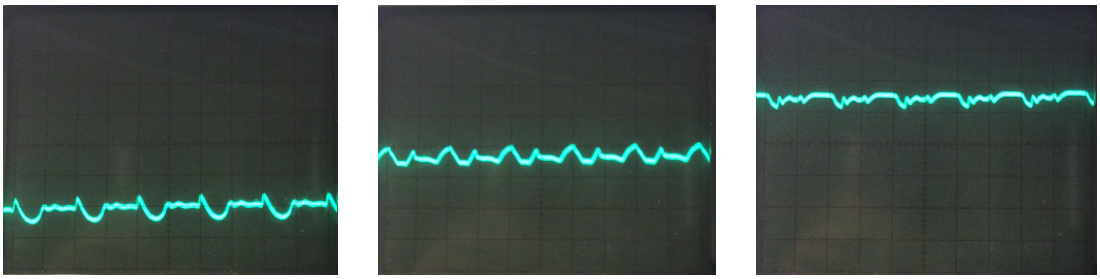


Figure 4.3 *The output waveforms of SA602A when detecting two 1-MHz signals (volts/-division 0.5 V, seconds/division 0.5 μs, lowest line as ground level).*

Another idea is to keep using CD4070BE, but adding additional frequency dividers to scale both XO frequency and VCO frequency down to 6 MHz.

Two 1-MHz sinusoidal waves are fed from signal generators into CD4070BE for testing. As presented in Figure 4.4, the duty cycle slowly changes from 0 to 100% then back to 0, therefore the average output voltage is changeable between 0 V and around 7V under 7-V supply voltage.

However, since 6-MHz is close to upper limitation frequency of chip, the performance is not as good as at lower frequency. As can be seen from Figure 3.23 and 3.24, when duty cycle is around 50%, the output waveform at 10 kHz looks more like a square wave than at 6 MHz. The reason is that the frequency of 6 MHz is too high to allow the output maintain logic high or low for longer time. The slope at point of $\theta_e = \pi/2$ gets steeper, and correspondingly, K_d is increased, as plotted in Figure 4.5. Nonetheless, it is not wise to add more frequency dividers because more

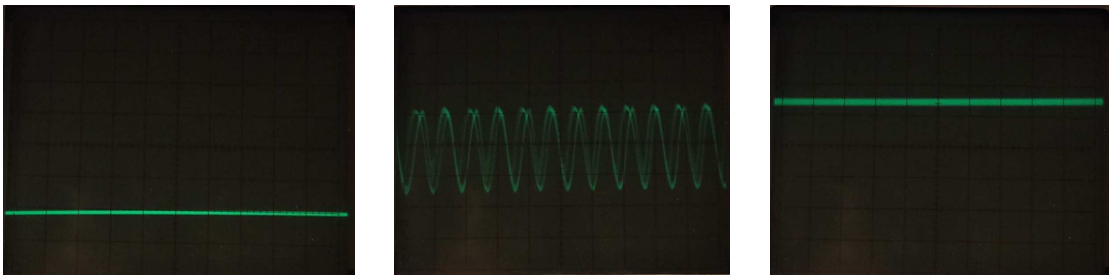


Figure 4.4 *The output waveforms of CD4070BE when detecting two 1-MHz signals (volts/division 2 V, seconds/division 1 μs, lowest line as ground level).*

spurious frequencies will be introduced.

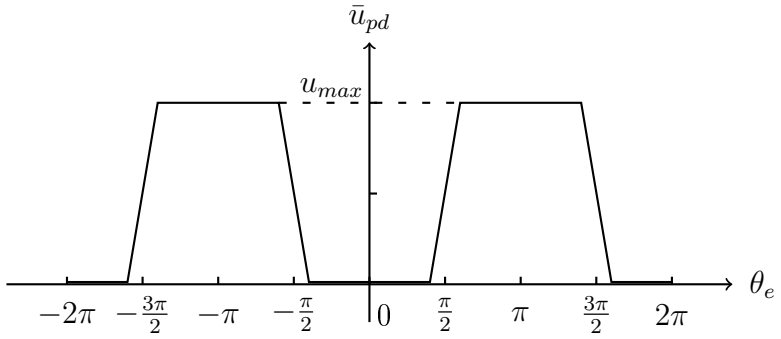


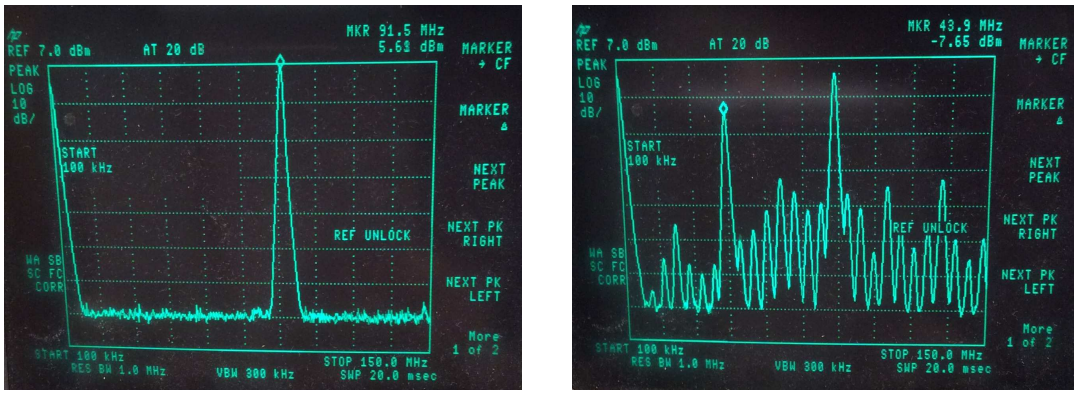
Figure 4.5 *The average voltage $\bar{u}_{pd}$ as a function of phase error θ_e for CD4070BE.*

Either CD4070BE or SA602A has drawback for this PLL system. Although the CD4070BE is decided to be applied as final design in this work, it cannot be recommended for frequency detection above 2.5 MHz.

4.2 Analysis of the frequency divider

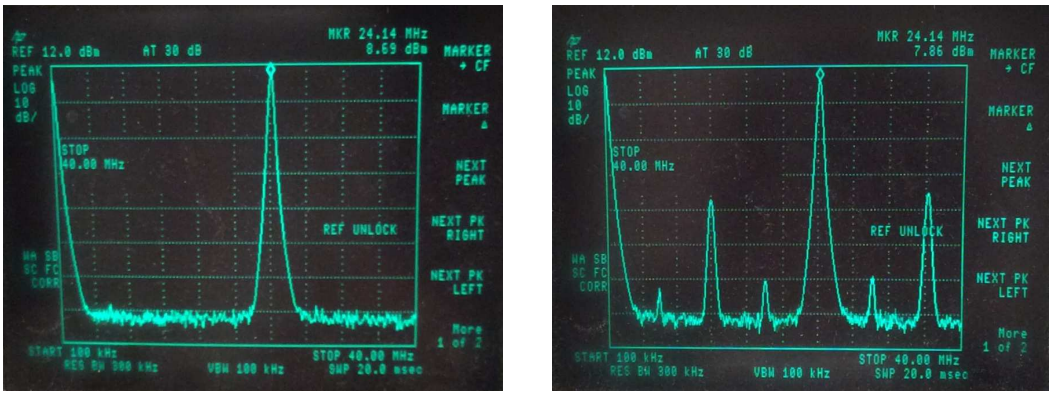
When the VCO block was connected with divide-by-16 circuit, it was found that the divider brought VCO output signal spurious frequencies, as shown in Figure 4.6. Similar problem happened with the by-4 divider. The spectrum of crystal oscillator output had single frequency component, while additional spurious components were introduced after being connected with divide-by-4 circuit, see Figure 4.7.

Several ways has been tried for the purpose of solving this problem. For example, each block was enclosed by foils for preventing electromagnet interference. However it was proved to be useless for eliminating the noise. Finally, these spurious signals were suppressed by means of putting cascaded simple amplifiers as buffers at the forward path of dividers. This method prohibits signals leak from dividers back to previous circuit. The design of buffer circuits are presented in Figure 4.8 while the



(a) (b)

Figure 4.6 *(a) The spectrum of VCO output when VCO works independently and (b) the spectrum of VCO output when VCO works with divide-by-16 circuit.*



(a) (b)

Figure 4.7 *(a) The spectrum of XO output when XO works independently and (b) the spectrum of XO output when XO works with divide-by-4 circuit.*

constructed circuits are shown in Figure 4.9. In VCO's buffer, the series connected 2.2-μH inductor, 330-pF capacitor and 100-Ω resistor are placed before the output port, in order to stabilize the operation of its previous transistor.

The XO output presents better frequency spectrum after adding the buffer circuit, as shown in Figure 4.10. The maximum of spurious decreases from -25 dBm (about 0.036 V V_{pp}) to -48 dBm (about 0.003 V V_{pp}).

Similarly, Figure 4.11 compares the output spectrum of VCO when it works without and with the buffer circuit. The maximum of spurious decreases from -7.65 dBm (about 0.262 V V_{pp}) to -46 dBm (about 0.003 V V_{pp}).

Both XO and VCO output signals are amplified after passing their buffer circuits, as presented in Figure 4.12.

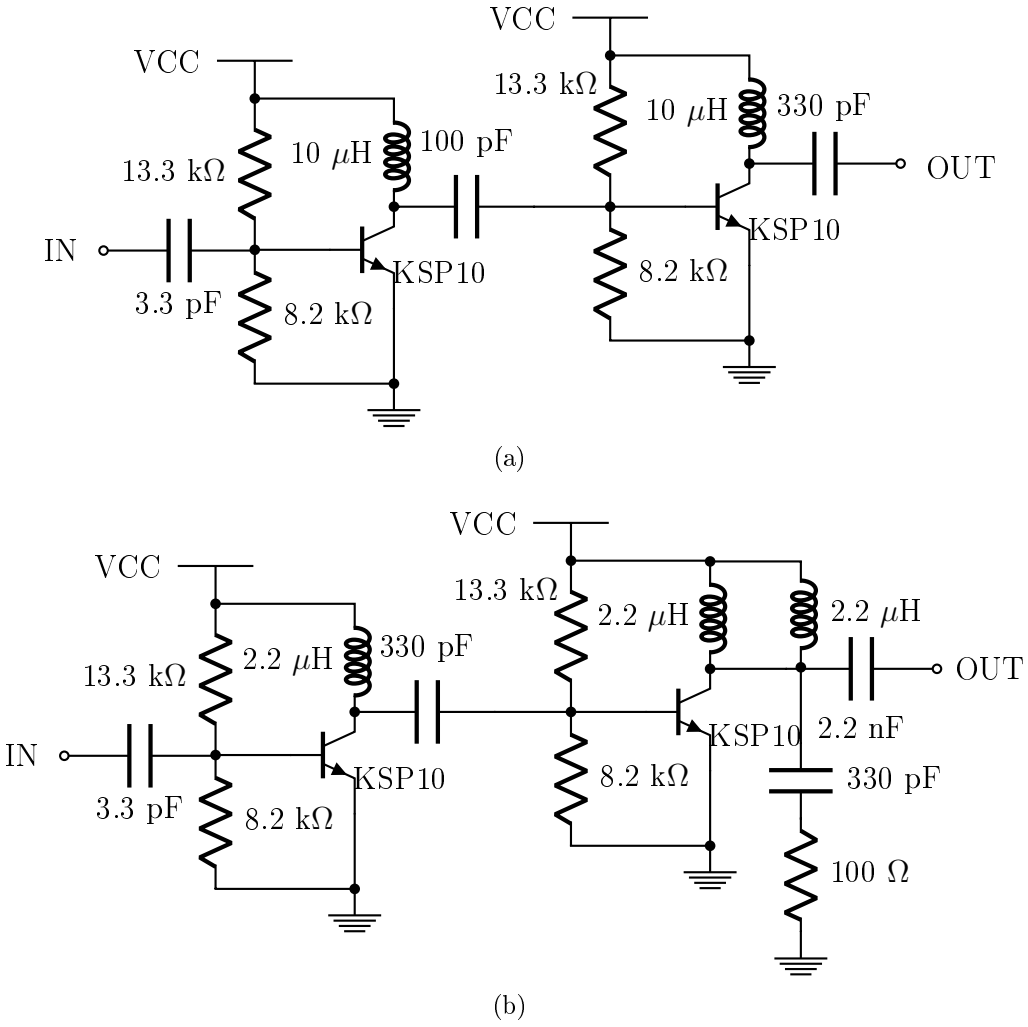
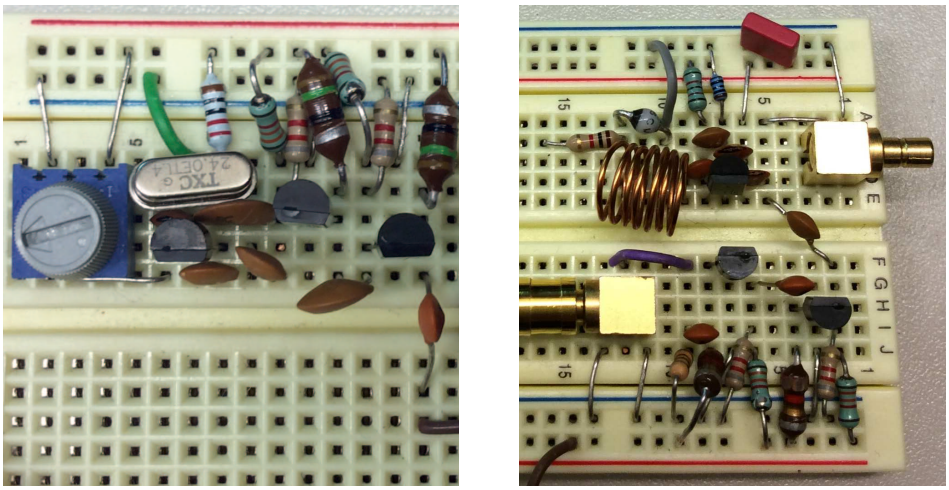
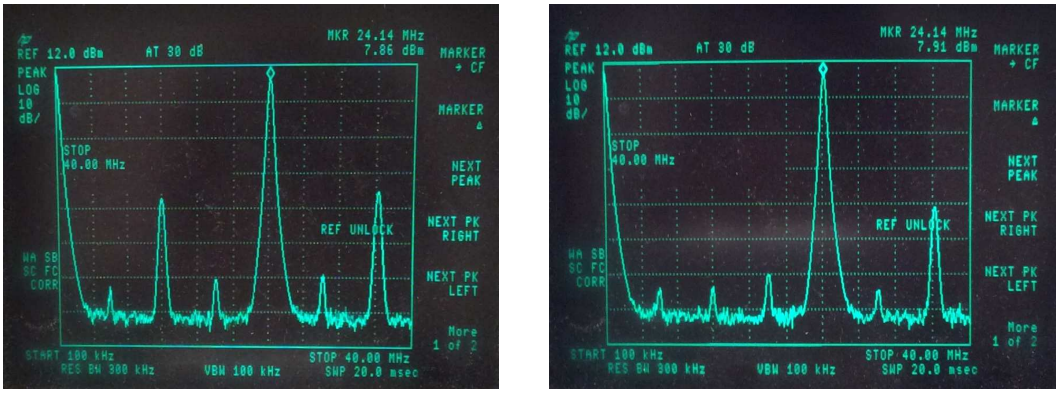


Figure 4.8 *(a) The buffer circuit for XO and (b) the buffer circuit for VCO.*



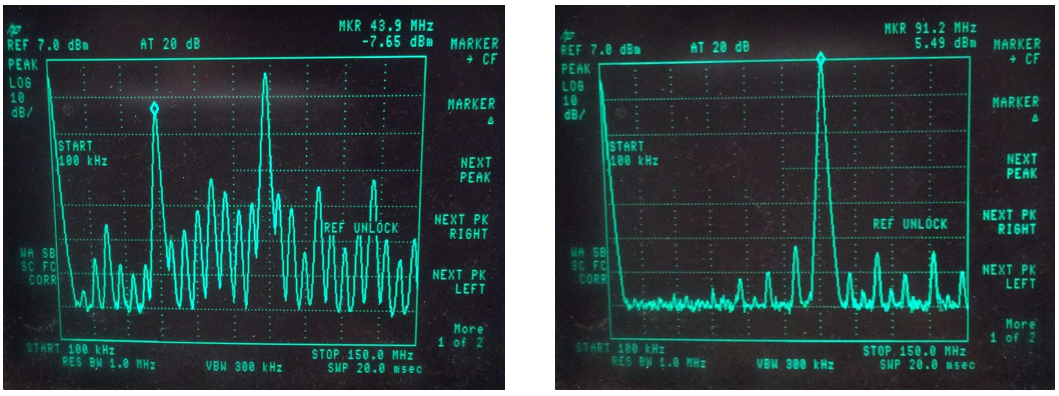
(a) (b)

Figure 4.9 *(a) The XO with its buffer and (b) the VCO with its buffer.*



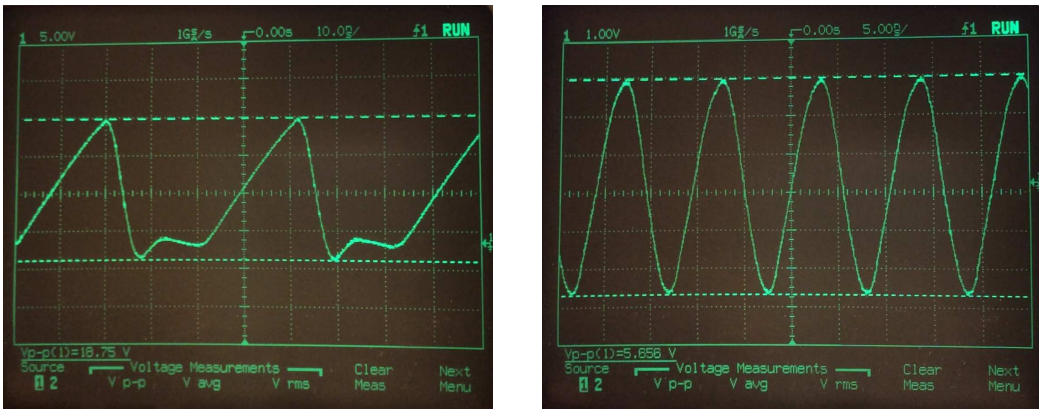
(a) (b)

Figure 4.10 *(a) The spectrum of XO working without buffer and (b) the spectrum of XO working with buffer.*



(a) (b)

Figure 4.11 *(a) The spectrum of VCO when working without buffer and (b) the spectrum of VCO when working with buffer.*



(a) (b)

Figure 4.12 *(a) The amplified XO output and (b) the amplified VCO output.*

4.3 Measurement results

The complete PLL system is obtained by combining all building blocks, as presented in Figure 4.13.

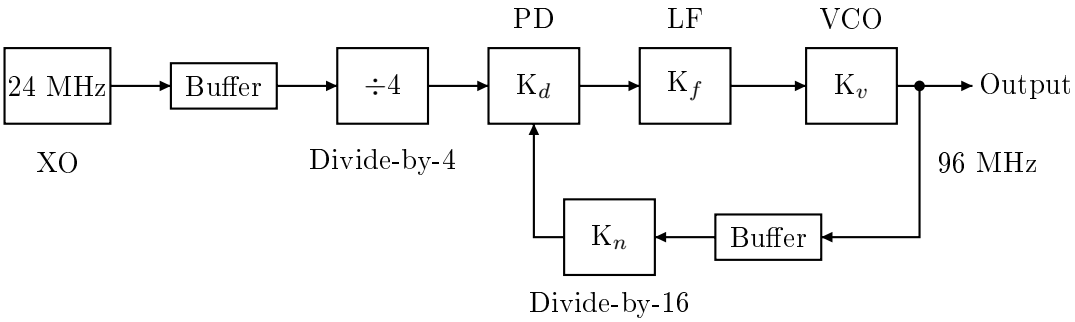


Figure 4.13 *The block diagram of whole PLL system.*

In order to avoid interference between high-frequency signals, each building block is constructed and tested on separate breadboard, powered by different voltage sources, and connected through wires or coaxial cables, as shown in Figure 4.14.

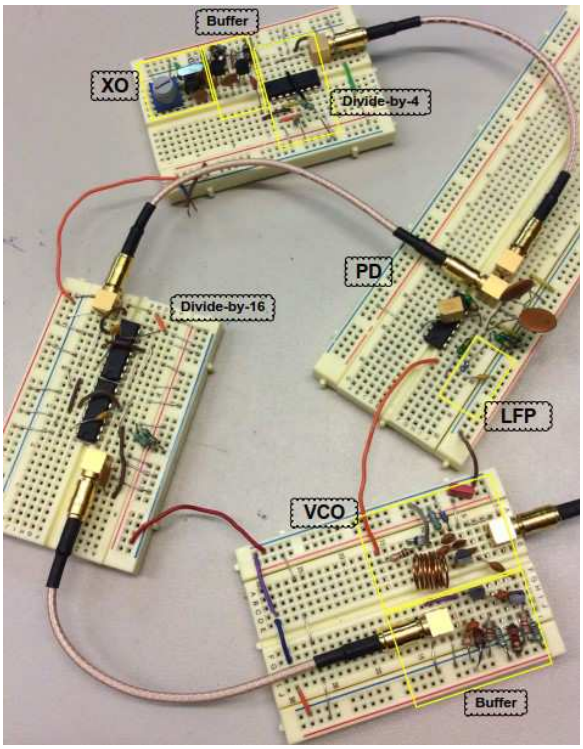
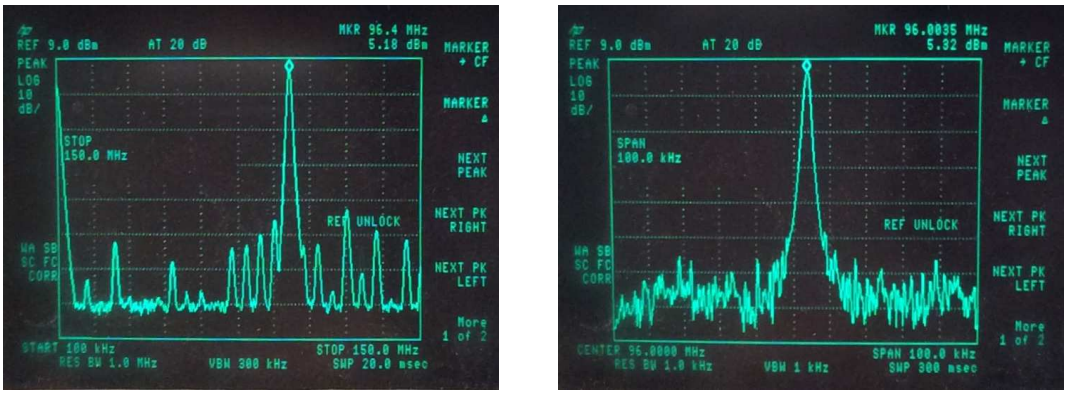


Figure 4.14 *The completed PLL circuitry.*

The spectrum of VCO output at locked state is shown in Figure 4.15. The frequency is locked to 96.0035 MHz.



(a) (b)

Figure 4.15 *The spectrum of VCO output at locked state: (a) with 150-MHz span and (b) with 100-kHz span.*

The gain of each block are listed as:

$$K_d = 34 \text{ V/rad} \tag{4.2}$$

$$K_f = \frac{1}{1 + s \cdot 10^{-6}} \tag{4.3}$$

$$K_v = 2\pi \cdot 8.5 \text{ MHz/V} \tag{4.4}$$

$$K_n = 1/16 \tag{4.5}$$

To determine the stability of loop, poles are calculated from:

$$\begin{aligned} s &= -\frac{1}{2 \times 10^{-6}} \pm \sqrt{\left(\frac{1}{2 \times 10^{-6}}\right)^2 - \frac{K_d\, K_v\, K_n}{10^{-6}}} \text{ rad/s} \\ &\approx (-0.5 \pm j10.7) \times 10^6 \text{ rad/s} \end{aligned} \tag{4.6}$$

Two poles are located in left-half complex plane, hence the loop is stable.

The calculated natural frequency ω_n and damping factor ζ are:

$$\omega_n = \sqrt{\frac{K_d\, K_v\, K_n}{10^{-6}}} \text{ rad/s} \approx 10.71 \times 10^6 \text{ rad/s}, \tag{4.7}$$

$$f_n \approx 1.7 \text{ MHz}, \tag{4.8}$$

$$\zeta = \frac{\omega_c}{2\,\omega_n} \approx 0.047. \tag{4.9}$$

The damping factor ζ is a tiny value, therefore there is a high possibility that the system is under-damped, which would cause the overshoot problem and the risk of

instability. The best way to improve damping factor in this case could be decrease the phase detector gain K_d.

The approximate values for lock range ω_{cr} (also known as capture range) and locking time t_L (also known as settling time) are:

$$\omega_{cr} = \sqrt{\frac{K_d\, K_v\, \times 10^6}{K_n}}\ \text{rad/s} \approx 171.4 \times 10^6\,\text{rad/s}, \tag{4.10}$$

$$f_{cr} = \frac{\omega_{cr}}{2\pi} = 27.28\ \text{MHz}, \tag{4.11}$$

$$t_L \approx \frac{2\pi}{\omega_n}\,\text{s} \approx 0.587\ \mu\text{s}. \tag{4.12}$$

5. CONCLUSIONS

A PLL system was designed and built on breadboard in this work, for the purpose of synthesizing a stable carrier wave at 96 MHz. The system contains five building blocks: a 24-MHz crystal oscillator (XO), a 96-MHz voltage-controlled oscillator (VCO), two frequency dividers, a phase detector (PD), and a loop filter (LF). The XO offers a 24-MHz sine-wave as the reference signal. The VCO output frequency can be tuned from 86 MHz to 100 MHz. The XO frequency is divided by 4 into 6 MHz, meanwhile the VCO frequency is divided by 16. The divided VCO frequency varies accordingly between 5.375 MHz and 6.25 MHz. Two divided frequencies are compared by a phase detector, creating a signal that is proportional to phase difference of these two input signals. After filtered by low-pass filter, the output of phase detector becomes the input control voltage of VCO. The VCO frequency is tuned to be more and more close to quadruple frequency of XO, eventually locking exactly to 96 MHz.

During the lab work, some problems of applying IC chips are discovered and studied. Their solutions are also presented. Additional dividers are used to decrease the input frequency of phase detector CD4070BE, to compensate its insufficient operation speed. However, this XOR gate IC is problematic for frequencies above 2.5 MHz. On the other hand, the divider 74AC74 introduces a large amount of spurious to its previous circuit. The buffer circuit which is composed by two cascaded amplifiers is placed at the forward path of frequency divider, in order to limit spurious frequencies.

The constructed loop circuitry can lock to 96 MHz as expected, though there exists a possibility of overshoot. For further research, the method of eliminating spurious frequencies could be explored deeper to improve the practical results. Other divider IC chips could be applied instead of 74AC74, for example, a prescaler SAB6456 can divide a frequency by 256. It provides a larger division number than a 74AC74, and is more compact so that it saves space. It also generates purer output waveform. Besides, other phase detectors with higher operation speed could be implemented instead of CD4070BE, to decrease the gain of phase detector, consequently improving the stability of system and preventing under-damped problem.

REFERENCES

[1] William F. Egan, *Phase-Lock Basics, Second Edition*, John Wiley & Sons, 2008.

[2] Roland E. Best, *Phase-Locked Loops: Design, Simulation, and Applications, Sixth Edition*, McGraw-Hill Education, 2007.

[3] Karl D. Stephan, *Analog and Mixed-Signal Electronics, First Edition*, John Wiley & Sons, 2015.

[4] Behzad Razavi, *RF Microelectronics, Second Edition*, Person Education, 2012.

[5] Stanley J. Goldman, *Phase-Locked Loop Engineering Handbook for Integrated Circuits*, Artech House, 2007.

[6] Martin Snelgrove, *Oscillator*, AccessScience, McGraw-Hill Education, 2014.

[7] Robert J. Matthys, *Crystal Oscillator Circuits, Revised Edition*, Krieger Publishing Company, 1992.

[8] Richard C. Li, *RF Circuit Design*, John Wiley & Sons, 2012.

[9] Reinhold Ludwig, Gene Bogdanov, *RF Circuit Design: Theory & Applications, Second Edition*, Person Education, 2009.

[10] Brian Holdsworth, Clive Woods, *Digital Logic Design*, Elsevier Science, 2002.

[11] Marc Thompson, *Intuitive Analog Circuit Design*, Elsevier Incorporated, 2006.

[12] Randall W. Rhea, *Oscillator Design and Computer Simulation, Second Edition*, SciTech Publishing, 1995.

[13] Olli-Pekka Lundén, Kristian Konttinen, Masoumeh Hasani, *A simple closed-form analysis of clapp oscillator output power using a novel quasi-linear transistor model*, 2014 IEEE Radio and Wireless Symposium (RWS), 2014.

[14] *BYV26C Data Sheet*, Vishay Semiconductors, 2017.

[15] Peter Vizmuller, *RF Design Guide: Systems, Circuits and Equations*, Artech House, 1995.

[16] *74AC74 Data Sheet*, Fairchild Semiconductor Corporation, 1988.

[17] *CD4070B Data Sheet*, Texas Instruments Incorporated, 2003.

[18] *SA602A Data Sheet*, NXP Semiconductors, 2014.

APPENDIX A. MEASUREMENT SETUPS

The information on measurement setups are presented as follow.

For Figures 3.5, 3.18: measurement setup type A is applied.

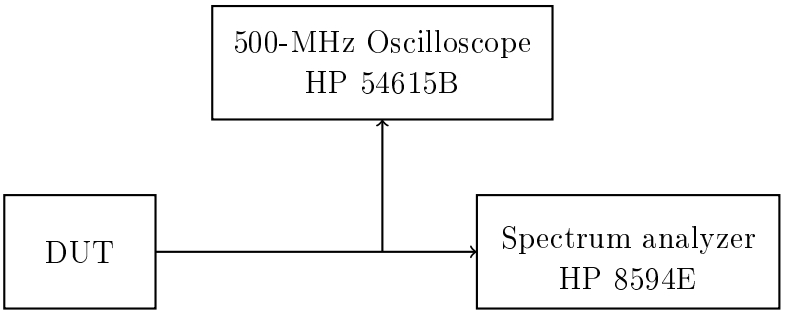


Figure A.1 Measurement setup type A.

For Figures 3.23, 4.3, 4.4 : measurement setup type B is applied.

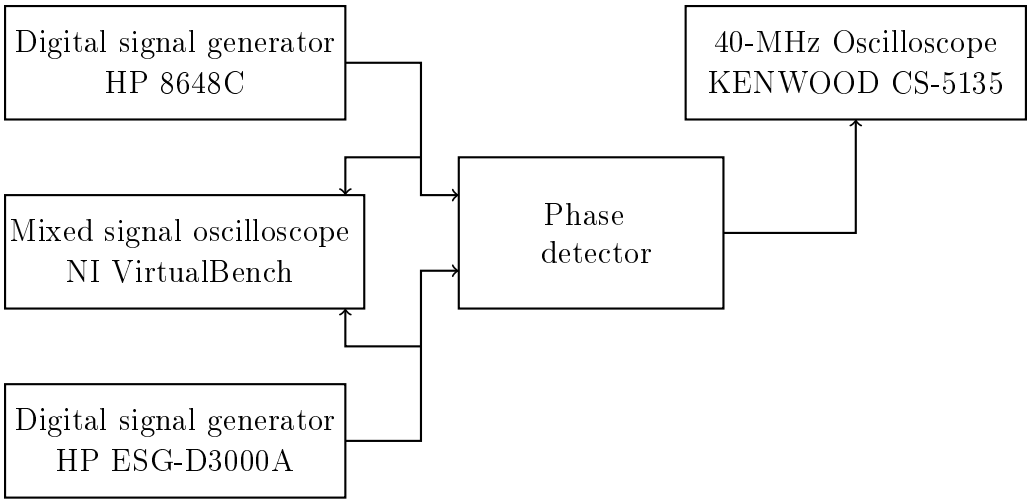


Figure A.2 Measurement setup type B.

For Figure 3.24, : measurement setup type C is applied.

For Figure 3.27(b) : measurement setup type D is applied.

For Figures 4.6, 4.7, : measurement setup type E is applied.

For Figures 4.10, 4.11, 4.12: measurement setup type F is applied.

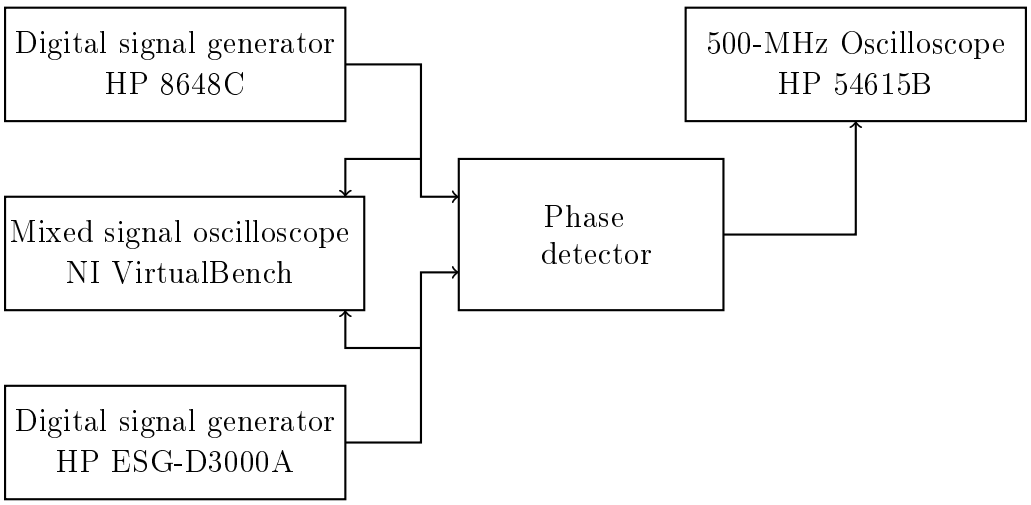


Figure A.3 Measurement setup type C.

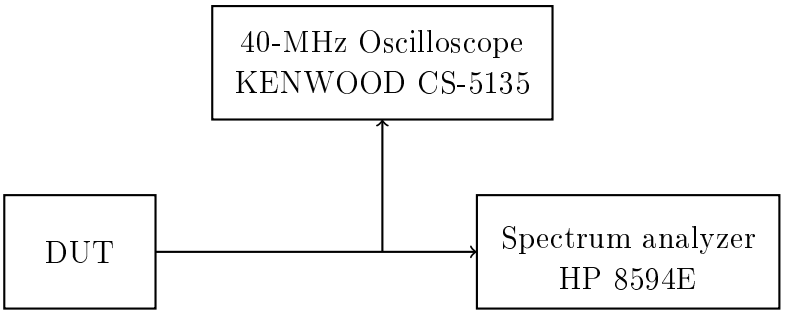


Figure A.4 Measurement setup type D.

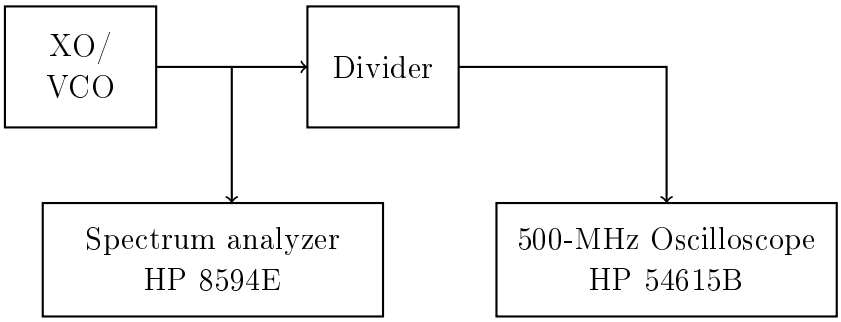


Figure A.5 Measurement setup type E.

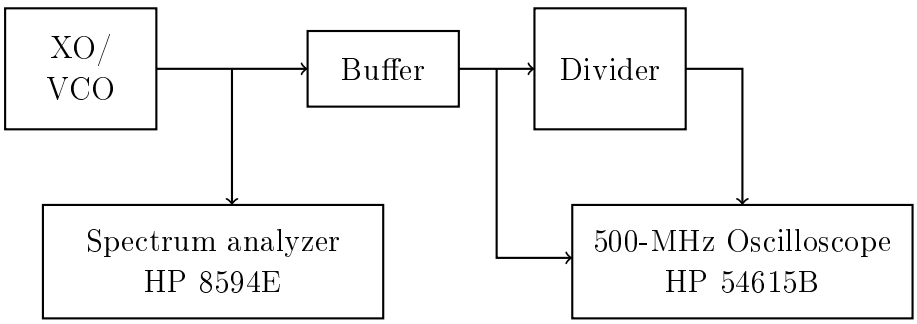


Figure A.6 Measurement setup type F.

APPENDIX B. VCO TUNING RANGE

Table 1 The measured tuning range of 96-MHz VCO circuit.

V_{ctrl} (V)	f_o (MHz)
0	86
0.1	87.5
0.2	88.3
0.3	89.05
0.4	89.75
0.5	90.25
0.6	90.65
0.7	91.05
0.8	91.45
0.9	91.8
1.0	92.2
1.1	92.5
1.2	92.8
1.3	93.05
1.4	93.35
1.5	93.6
1.6	93.8
1.7	94.0
1.8	94.25
1.9	94.45
2.0	94.7
2.5	95.6
2.7	96.0
3.0	96.45
3.5	97.2
4.0	97.8
4.5	98.45
5.0	99.0
5.5	99.5
6.0	100