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LYDIA LEPPÄNEN

BENDABILITY OF FLIP-CHIP ATTACHMENT ON SCREEN PRINTED INTERCONNECTIONS

Master of Science thesis

Examiners: Assoc. Prof. Matti Mäntysalo and Dr. Tech. Laura Frisk

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ABSTRACT

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The world is heading towards the IoE (Internet of Everything) where everything will be connected to each other. New flexible, light-weight and low-cost electronic devices are needed to add intelligence everywhere in our surroundings. Conventional silicon-based manufacturing is not the best solution because silicon is mechanically rigid and expensive. One way to manufacture these devices cost-effectively in a very large scale is by roll-to-roll screen printing on flexible substrates. However, due to the low calculation performance of current printed electronics, silicon ICs are still needed to act as brains of the devices. Many studies about chip-on-flex or chip-on-film (COF) attachments are available but information about the integration of a silicon chip directly on a screen printed substrate is needed. This thesis investigates bare chip attachment on printed flexible circuitry and evaluates its subsequent level of bendability.

The chip was attached on the high-density rotary screen printed circuitry using a flip chip technique with anisotropic conductive adhesives (ACP and ACF). A selection of chips was stud bumped with gold. Chips without bumps were more challenging to bond due to the surface roughness of the screen printed lines and a small marginal of the suitable bonding pressure. A chip should be exactly parallel with the substrate while bonding so that the pressure is correct on all pads. After finding the suitable bonding parameters, approximately 90 % of the ACP bonded and 96 % of the ACF bonded interconnections worked without bumps. Stud bumping increased the yield almost to 100 % and decreased the contact resistances approximately 75% making the contacts more reliable. Calendering was tested for printed lines to increase their uniformity and decrease the pad height deviation by heating and pressing them with high force. Calendering reduced the line heights by approximately 1 μm and decreased the surface roughness, but following this process there still existed at least a 2 μm variation in the line heights (nominal line height 5 μm). Bending reliability of the chip attachments on flexible plastic substrates was determined using a self-built bending test set-up which bends the sample between two rigid plates. All chip attachments studied withstood at least a 2.5 cm bending radius.

The main results of this thesis were to demonstrate bare die integration on screen printed circuitry and to show its suitability for flexible hybrid electronic applications. Still further development of the bonding process and materials are needed to achieve more reliable long-term solutions.

TIIVISTELMÄ

LYDIA LEPPÄNEN: Silkkipainetuille johtimille toteutetun flip-chip-liitoksen taivutettavuus
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Maailma on menossa kohti digitalisaatiota. Käsite ”Internet of Everything (IoE)” eli ”kaiken internet” on luotu kuvaamaan skenaariota, jossa kaikki ympärillämme olisi kytketty langattomasti toisiinsa. Jotta älykkyyttä saataisiin lisättyä ympäristöömme, tarvitaan uusia taipuisia, kevyitä ja halpoja elektroniikkalaitteita, jotka voidaan kiinnittää pintoihin. Yksi tapa valmistaa näitä laitteita suuressa mittakaavassa, on rullalta rullalle silkkipainatus taipuisille muovi-alustoille. Tämän päivän printatun elektroniikan laskentatehokkuus ei kuitenkaan mahdollista täysin painamalla valmistettuja laitteita, jonka takia piipohjaisia mikrosiruja tarvitaan vielä. Tutkimustietoa sirujen liittämisestä taipuisille alustoille tai kalvoille löytyy, mutta piisirun integroiminen suoraan silkkipainetulle piirille on uutta. Tämä diplomityö tutkii paljaan sirun liittämistä taipuisalle silkkipainetulle piirilevylle sekä valmiin liitoksen taipuisuutta.

Siru liitettiin silkkipainetulle alustalle käyttäen flip-chip -tekniikkaa ja anisotrooppisesti johtavia liimoja. Osa siruista oli nystytetty kullalla. Ilman nystyjä sirut olivat hankalampia liittää painetuille hopeajohtimille, koska painojälki oli epätasaista ja sirun piti olla tarkasti samansuuntaisesti liitettävään pintaan nähden, jotta liittämispaine olisi optimaalinen joka osassa sirua. Kun toimivat parametrit liittämisprosessissa oli löydetty, 90 % anisotrooppisesti johtavalla pastalla (ACP) liitetyistä ja 96 % anisotroopppisesti johtavalla kalvolla (ACF) liitetyistä kontakteista toimivat. Nystytys lisäsi liitosprosessin saantoa lähes 100 %:iin ja pienensi kontaktiresistanssia keskimäärin 75 % tehden liitoksista luotettavampia. Painetuille alustoille testattiin kalanterointia eli kiillotusta puristamalla korkeassa lämpötilassa, jotta painojäljestä tulisi tasaisempaa. Kalanterointi vähensi vetojen korkeutta keskimäärin 1 µm:n ja pienensi niiden pinnan karheutta. Kuitenkin vähintään 2 µm:n korkeuseroja havaittiin johtimissa kalanteroinnin jälkeenkin. (Vetojen pitäisi olla 5 µm:n paksuisia.) Liitosten taivutettavuus määritettiin käyttäen itse suunniteltua testilaitteistoa, jossa liitosta taivutetaan kontrolloidusti kahden metallilevyn välissä. Kaikki testinäytteet selvisivät taivutuksen vähintään 2,5 cm:n asti.

Tämä diplomityö demonstroi paljaan sirun integroimisen tiheään painetulle muovikalvolle sekä osoitti, että liitokset soveltuvat taipuisan elektroniikan sovelluksiin. Kuitenkin liittämisprosessia ja materiaaleja on edelleen kehitettävä, jotta pystyttäisiin valmistamaan luotettavia liitoksia, jotka kestävät pidemmässäkin käytössä.

PREFACE

This Master's thesis was carried out at Department of Electronics and Communications Engineering at Tampere University of Technology. The work was funded by the Tekes strategic opening project: "The Naked Approach: Nordic perspective to gadget-free hyperconnected environments" (funding decision 40337/14).

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Tampere, 31.3.2016

Lydia Leppänen

CONTENTS

LIST OF FIGURES

LIST OF SYMBOLS AND ABBREVIATIONS

ACA	Anisotropic conductive adhesive
ACF	Anisotropic conductive film
ACP	Anisotropic conductive paste
CMOS	Complementary Metal Oxide Semiconductor
COB	Chip-on-Board
COF	Chip-on-Flex or Chip-on-Film
COG	Chip-on-Glass
CTE	Coefficient of thermal expansion
HySiF	Hybrid System in Film
IC	Integrated Circuit
ICA	Isotropic conductive adhesive
ICF	Isotropic conductive film
ICP	Isotropic conductive paste
IGZO	Indium-gallium-Zinc-oxide
IoE	Internet of Everything
IoT	Internet of Things
LCD	Liquid Crystal Display
NCA	Non-conductive adhesive
NCF	Non-conductive film
NCP	Non-conductive paste
NMOS	N-type Metal Oxide Semiconductor
OLED	Organic Light Emitting Diode
OPV	Organic Photovoltaics
OTFT	Organic Thin Film Transistor
ROM	Read-only Memory
PCB	Printed Circuit Board
PEN	Polyethylene naphthalate
PET	Polyethylene terephthalate
PI	Polyimide
PMOS	P-type Metal Oxide Semiconductor
RFID	Radio Frequency Identification
R2R	Roll-to-roll
SMT	Surface-mount technology
TFT	Thin Film Transistor
TUT	Tampere University of Technology
UTM	Universal Tensile Machine
UV	Ultraviolet
VTT	fin, Valtion teknillinen tutkimuskeskus, Technical research center of Finland
WORM	Write Once Read Many

dL	length change
F	*force*
h	thickness
L	length
T	Temperature
r	radius

1. INTRODUCTION

Advanced silicon-based microelectronics has enabled various different applications, from mobile phones to self-flying airplanes. The continuous miniaturization of the electronic circuits has caused the decrease in the manufacturing costs. However, silicon has couple of weaknesses: it is rigid and large amount of silicon is expensive. Silicon-based electronics cannot be placed on large area curved surfaces or it cannot interact with human body directly. Therefore different approaches for flexible electronics have been studied.

One approach to achieve the flexibility is to use printed electronics. It means that electronics components and circuits are printed on a substrate on the same way than manufacturing conventional printed products, such as newspapers. That can enable to add intelligence to the applications which traditionally have not been seen as electronics applications and revolutionize the use of electronics. Possible examples could be clothes and walls. That could result to an environment where every surface is connected on internet known as Internet of Everything (IoE). Printing is an additive, cheap and simple process to fabricate electronics. By choosing a flexible substrate and flexible inks, it is possible to manufacture flexible electronics. Unfortunately, the calculation performance of printed electronics is currently not as good as the performance of silicon electronics due to the lower mobility of organic semiconductors [1] and larger gate length [2]. A technique to combine both the benefits involved in printed and silicon-based electronics is known as hybrid electronics.

Hybrid electronics consist of both printed and silicon electronic components and take the advantages of both technologies. Typically, a hybrid electronic device includes a silicon microprocessor and radio frequency circuit due to their fast and affective calculation. Also separate memory can be provided by silicon based component. Other components, including antennas [3,4], energy harvesters [5-7], batteries [8,9], sensors [10,11], displays [12,13] and wiring [14,15] can be fabricated with printing techniques because they require large area. The key point of the hybrid electronics is to have a good and reliable interface between the printed and silicon-based components. This thesis will study the reliability of interconnections between a silicon chip and printed circuitry on flexible substrate when the device is being bent. The idea of using a bare silicon die without any package or interposer is to maximize the bendability and minimize the thickness of the system. Printed devices with silicon microprocessors could then be placed on curved surfaces everywhere around us.

The main objective of this thesis is to determine the bendability of silicon chip attachments on screen printed interconnections. For that purpose, a suitable bending test method has to be defined and a test set-up has to be built. The attachments are fabricated with flip-chip technique using anisotropic conductive adhesives. Ideally the chips would be bonded without any bumps to keep the amount of process steps small. However, a selection of the chips is stud bumped with gold to observe the effect of bumping on bonding and bending reliability. This thesis should give essential information for the chip attachment of an energy autonomous sensor system which is planned to fabricate later in this research project. That system is a flexible hybrid device which consists of printed components: PV (Photovoltaic) cell, supercapacitor, display and radio frequency energy harvester as well as silicon IC (Integrated Circuit) chip.

The next chapter tells more about hybrid electronics. After that in chapter three, flexible electronics and bending tests are discussed. Chapter four describes the experiments and chapter five discusses and analyzes the results of them. In the end, chapter six summarizes the most important aspects of the thesis.

2. HYBRID ELECTRONICS

Ideally every electronic device can be printed with low-cost and simple manufacturing processes. Unfortunately, the speed of electrons in printed materials is low compared to silicon. The best printed complementary circuit logic delays are 30 µs [16]. Comparing to propagation delays of silicon circuits (order of 100 ps), they still are very large. A microprocessor made from today's printed transistors would take a very large area. That is why flexible electronics still need silicon microcontrollers. The integration of printed and silicon electronics is called hybrid technology.

A hybrid electronic device consists of a silicon IC which includes the logic the device needs in its application. Other components are aimed to be manufactured with printing technologies but they can also be silicon-based. An example of a hybrid electronic device is shown in Figure 1. It is a flexible, wireless multifunctional sensor which can be placed on existing houses [17].

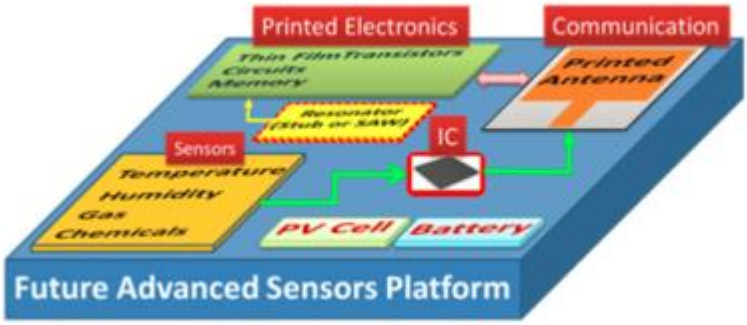

Figure 1. *A hybrid electronics device: a multifunctional sensor platform for smart buildings [17].*

2.1 Silicon-based electronics

Silicon is the second most abundant material on earth and it is found in sand. However, the treatments demanded for silicon when it is used in electronics, are complex and expensive. Next the advantages of silicon electronics as well as the comparison to the printed electronics are discussed.

2.1.1 Advantages of silicon-based electronics

The answer why silicon electronics is fast is due to its high charge carrier velocity. The charge carriers are electrons and holes which create the current by moving from one place to another. The charge carrier mobility of silicon depends on the doping level, but electron mobilities 100-1400 $cm^2/(V \cdot s)$ are common [18]. The high mobility of charge carriers enables high switching frequencies in microprocessors. That makes silicon electronics fast.

The widely used technology in microprocessors is CMOS-technology (Complementary Metal Oxide Semiconductor). CMOS-logic consists of a PMOS (P-type Metal Oxide Semiconductor) and a NMOS (N-type Metal Oxide Semiconductor) blocks. One of them is conducting always meaning that circuit consumes almost no power in static situations. Other advantages are large noise margin and far developed design and manufacturing methods [19].

It is not yet possible to manufacture good printable microprocessors using CMOS technology. The main reason for that is the limited availability of good n-type inks [20]. Good n-type ink with good electron mobility and solubility is hard to create [21] while good p-type inks are widely available which has at first led to the use of a PMOS technology in printed electronics applications. Recently good n-type semiconductor inks have been developed and CMOS-technology is possible [21].

Table 1 gathers the features of silicon-based and printed electronics. As the characteristics of silicon and printed electronics are very different, they are suitable for different electronic applications. In a summary, printable and silicon electronics are not usually competing in the same markets. On the other hand, conventional electronics manufacturers are also interested in printing technologies.

Table 1. *Comparison of silicon and printed electronics, adapted from [22].*

Silicon electronics	**Printed electronics**
very short switching times	long switching times
high integration density	low integration density
small areas	large areas
rigid substrates	flexible substrates
sophisticated fabrication	simple fabrication
high fabrication costs	low fabrication costs

2.1.2 Manufacturing process

The success of microelectronics is based on its advanced handling of silicon crystals [1]. Silicon chip manufacturing is a long process and it requires multiple steps. First silicon has to be purified. Nearly 100 % purity is necessary that the chips function as intended [23]. Pure silicon is heated until it is melted. Then a seed is drop into the molten silicon. A seed is a perfectly formed solid silicon piece which physical structure is specified. When the seed is slowly pulled out of the molten silicon rolling it at the same time, the molten silicon cools and solidifies around the seed. The new silicon gets the same specified crystal structure as the seed. That method is called a Czochralski growth process [24]. After Czochralski process, the formed silicon bar is sawed into wafers. Generally, the wafer diameters are 200 mm or 300 mm [23]. In the end, the wafers need to be polished.

Chips are next created on to the wafers. In order to get the transistors in the silicon, tiny areas of different semiconductor types are processed. To get p- and n-type silicon, some impurities are douped to the silicon using methods, such as diffusion and ion implantation [23]. In addition, deposition techniques are used when layers from other materials are needed. Wanted patterns of the materials are formed using photolithography.

The photolithography process is shown later in Figure 5. First the wanted patterning material is coated on the substrate. After that, a photoresist is covered on top of it. Next the patterned mask is placed and the sample is exposed on UV-light (Ultaviolet). The part of the photoresist which is not under the mask is exposed. If negative photoresist is used (as in Figure 5), UV-exposed photoresist is dissolved to the developer. Using positive photoresist, the unexposed photoresist is etched. Finally, the remaining photoresist is cleaned and the wanted patterning has been formed.

When the chips have been formed to the wafer as in Figure 2, the wafer has to be cut in pieces, where each chip is located. These chips can then be packed on different packages or used as a bare dies.

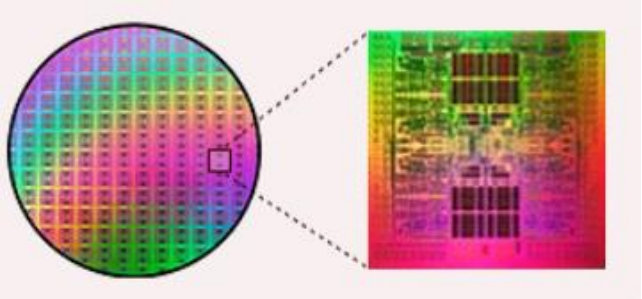

Figure 2. *Chips on a wafer [25].*

2.2 Printable electronics

Printing is not a new idea. The first printing revolution began already in the 1440's when Johannes Gutenberg started to print the Bibles. The first printed transistor was made in 2003 [20], the first printed circuit in 2004 [26]. However, separate other components and interconnects were already printed before that.

There will be huge potential markets for printable and organic electronics in the future. In Figure 3, IDTechEx has estimated the global market value for printed electronics. As can be seen, the growth of the market will be significant. On other hand, compared to the over 200 billion USD $ business of consumer electronics only in US [27], the printed electronics market is still moderate.

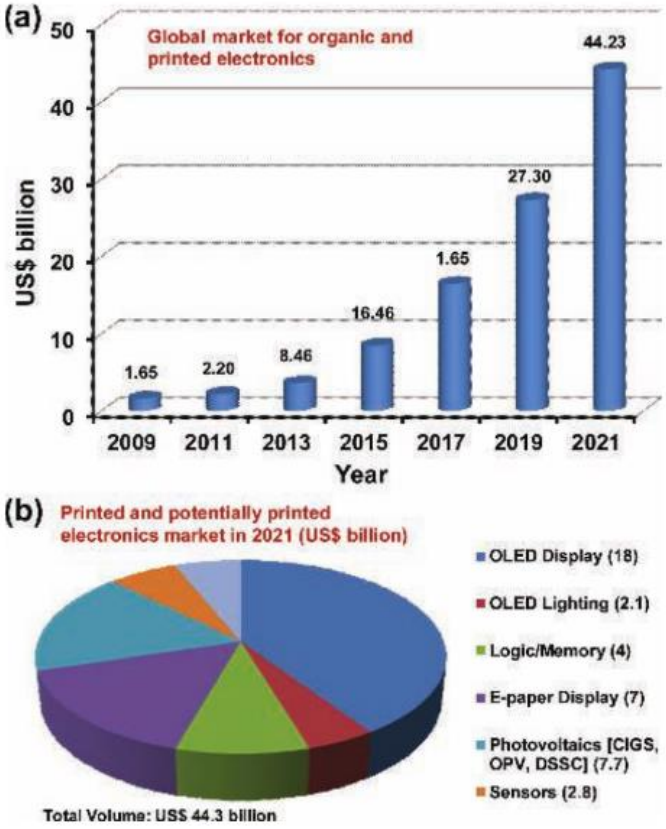

Figure 3. *Market for printed electronics [28].*

2.2.1 Applications

Typical printed electronics applications do not need high performance in the calculation point of view. They are more high volume products. Low weight, large area and mechanical flexibility are also typical features of printed electronics products.

Followed is the list of typical printed electronics applications. Each of them will be discussed shortly. Example pictures of each application can be found in Figure 4.

- solar cells
- flexible displays
- e-textiles
- sensors
- memory
- flexible batteries
- radio frequency identification (RFID) -tags

The energy, which a **photovoltaic** cell produces, depends directly on the cell area. Silicon is expensive, which is what makes printing the solar cell with organic inks a good solution for large-area applications. Organic photovoltaic cell consists of two electrodes and different functional layers between them. The current originates from the electron movement between the electrodes which is caused by sun light. OPVs have already taken root in the market. In year 2015 the market for OPVs was 300,000 US$ according to IDTechEx [29]. Life-time and effectiveness of printed photovoltaics need still development [26].

Flexible and OLED (Organic Light Emitting Diode) **displays** are other large-area electronics applications. OLED has similar structure than normal LED: anode, emitting layer and cathode. These layers can be printed when they are made from organic materials. Also the control circuit of large displays, backplane, is reasonable to manufacture from OTFTs (Organic Thin Film Transistors) using printing. Also very flexible, paper-like displays have been developed [30].

One increasing business is **electro-textiles** or wearable electronics on the other name. They are clothes with electronics. They can for example measure body parameters. E-textiles face stretching and bending when they are on human body. That is the reason why printing with flexible inks is an attractive manufacturing method for these applications.

Flexible **sensors** are needed for e-textiles and other applications. When they can be printed in a cheaper way, they will make the Internet of Things (IoT) possible collecting mass of data. For instance organic temperature, pressure and photodiode sensors are developed [26].

Thin and flexible **batteries** are already commercially available. Still further improvement in their printability, cost and ease of integration are needed [26]. Especially development of low-cost, printable supercapacitors are done [9,31]. Supercapacitors are electrochemical capacitors which have high capacitance values. That means that they charge and discharge energy fast.

Memories are needed everywhere. Memory units use the same structure and they are needed in huge amounts. R2R-printing (Roll-to-roll) of memories would cut the costs. ROM (Read-only Memories) and WORM (Write Once Read Many) memories have already printed in identity cards [26]. The application where flexible and thin memories are needed is particularly identification and smart cards.

RFID –tag (Radio Frequency Identification) is a thin and low-weight tag which includes an IC and an antenna. It responds contactless to radio waves which are transmitted from the RFID reader [32]. RFID-tags are used to identification in many cases, such as controlling the access to buildings and tracking goods. For that reason they need to be manufactured in a cheap way. One tag can only costs less than one or two cents [33]. The part of RFID-tag which has originally printed is antenna. Printed antennas are already common in conventional silicon based RFID-tags [26]. In addition the whole RFID-tags can be printed.

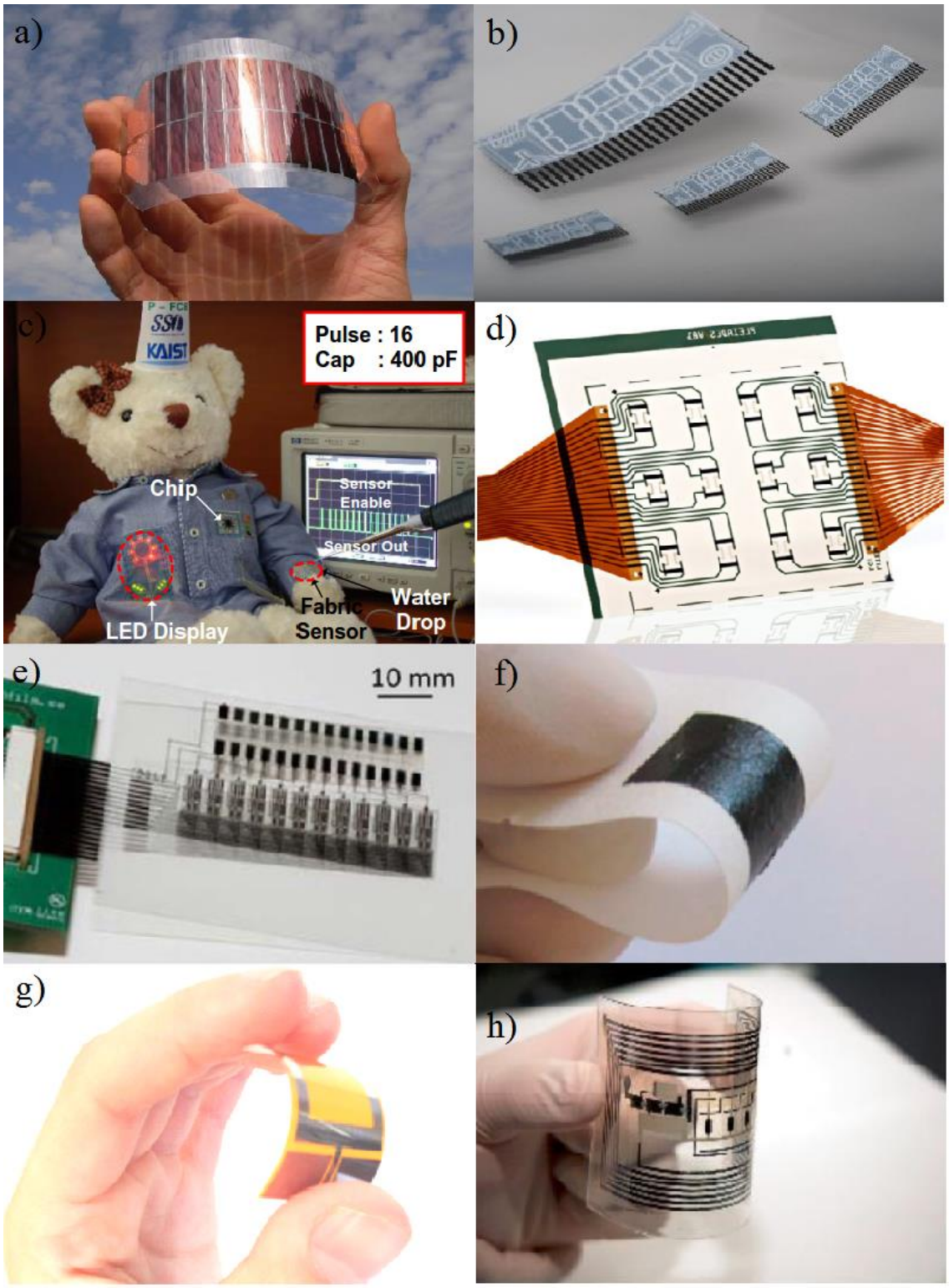

Figure 4. *Printed electronics applications: a) OPV [34], b) organic display [35], c) e-textile: a sweat monitoring system [36], d) temperature sensor [37], e) memory array [38], f) supercapacitor on a paper [8], g) flexible antenna [39], h) RFID-tag [40].*

2.2.2 Manufacturing methods

The main advantage of printed electronics is its simple manufacturing. Manufacturing printed electronics, a printing machine prints ink to the desired substrate. Ink can be a polymer or a paste that consists of a solvent and a material that contains the functionality. If conductive layer is needed, some metal atoms (e.g. silver), are added to the solvent. When printing is completed, solvent will evaporate and a conductive layer will form. Comparing to the subtractive technologies used in silicon-based manufacturing of electronics, printing has fewer process steps what makes it cheaper (Figure 5). In addition, the additive nature of printing means less waste of materials.

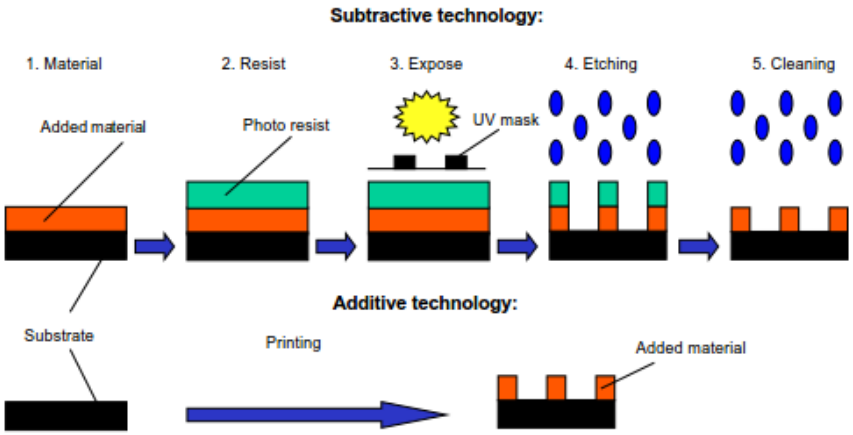

Figure 5. *Printing as an additive technology [41].*

There are many manufacturing techniques used for printing electronics. Some of them are analog and others digital. The difference between the mentioned techniques is a printing form, also called a printing master. In analog printing techniques the master is physical and permanent. Then the printing master has to be manufactured before printing. In the digital printing techniques the printing master is only computer code and easily changeable. Digital printing techniques include inkjet (Figure 6 A), xerography and laser transfer while screen printing (Figure 6 B), flexography (Figure 6 C) and gravure printing (Figure 6 D) are analog printing techniques.

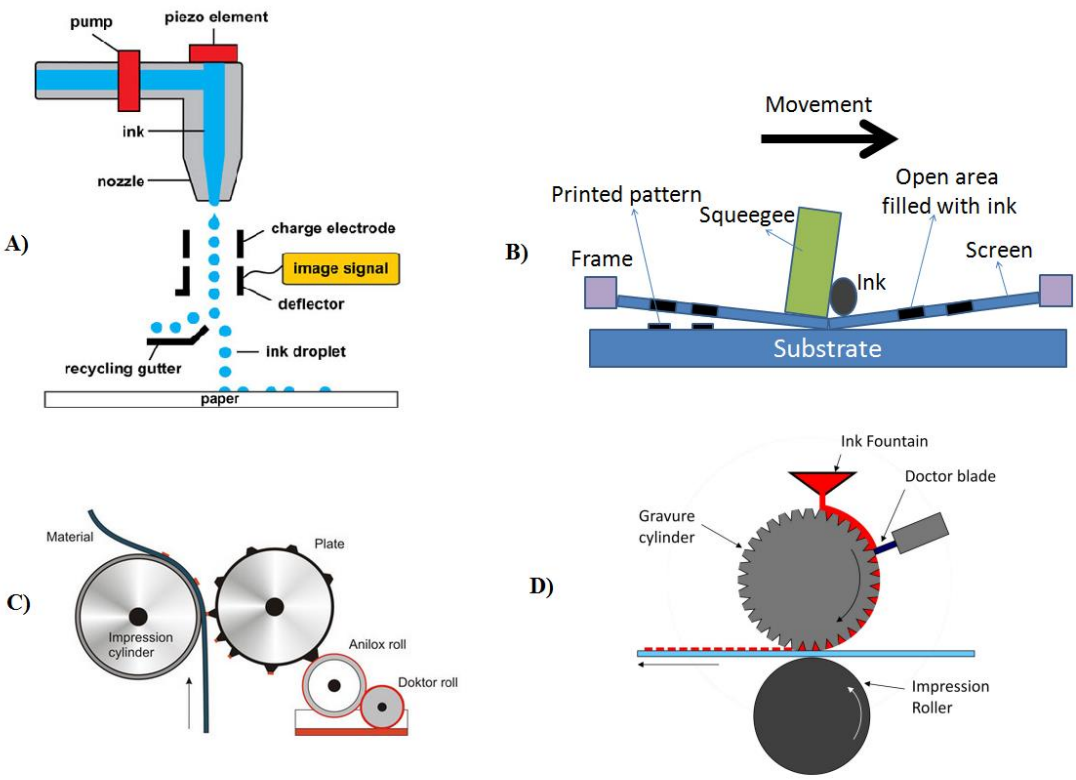

Figure 6. *Printing techniques: A) inkjet [42], B) screen printing [39], C) flexography [43], D) gravure [44].*

In **inkjet** printing, the ink is stored in cartridges and then transferred from them to the substrate using a nozzle. There are two types of inkjet printing techniques: continuous inkjet and drop-on-demand inkjet [45]. Continuous inkjet printer (Figure 6 A) ejects ink drops all the time. The drops are charged by electrode and positioned to the substrate according to the wanted picture [45]. Remaining ink drops are collected to the recycling gutter [45]. Drop-on-demand inkjet printer ejects ink drops only when they are needed to form the wanted picture. Best inkjet printers can print wires with width of 10 µm [17].

In **screen printing**, the ink is transferred to the substrate through a printing form which is a screen mask. The screen has little holes which are manufactured so that they form the wanted picture when the ink is transferred through the screen. Ink is pressed through the screen using a squeegee. Screen printing is a simple way to manufacture large amount of products and it is easy to use with R2R-processes. However, the resolution of screen printed products is typically about 100 µm [45] which is not compatible with digital printing techniques. Also the layer thickness is more challenging to control and layer thicknesses under 10 µm are difficult to achieve with screen printing [45].

Using **flexography**, the printing master is a rubber cylinder which has the embossing of the wanted picture. The cylinder works like a pressure stamp. The cylinder is wetted to the ink with the help of another cylinder and then pressed to the substrate. Resolution

under 20 μm as well as thin layers (< 1 μm) are possible to achieve with flexography [45].

Gravure works opposite way than flexography. There the printing form has little wells, where the ink is seized when the printing form is dipped to ink. When the wells are touching the substrate, the ink from well is transferred to substrate. The thickness of the formed patterns depends on the size of the wells. Quite high resolution pictures (< 20 μm) can be printed with gravure printer [45].

The offset forms of gravure and flexography are also possible. In that case, the ink is transferred to the printing form through an extra cylinder. Also coating techniques can be used for the large area electronics which do not require patterning. A good example of that includes large area solar cells.

Resolution, possible layer thicknesses and large-scale printability of the presented printing techniques are collected in Table 2. A designer has to choose the best available printing technique for each application. Inkjet is commonly used in prototypes and in research. The printing layout is easily changeable and small inkjet printers are cheap compared to large-scale printing machines.

Table 2. *Summary of the printing techniques, adapted from [45].*

	inkjet	**screen printing**	**flexography**	**gravure**
resolution	high	low	high	high
layer thickness	thin layers possible	thick layers	thin layers possible	broad thickness range
large-scale printability	for prototypes	R2R-manufacturable	R2R-manufacturable	R2R-manufacturable

2.3 Attachment of a microchip

A key issue is to have reliable interconnections between the silicon chip and the printed wiring on flexible substrate in order to have reliable hybrid technology. Conventional silicon electronic industry mostly uses reflow soldering to attach SMT (Surface-Mount Technology) components on circuit board. In reflow soldering a solder paste first attach components to their pads temporarily. When all components have been attached the device goes to the reflow oven. In the oven the solder melts and connects the joints.

Reflow soldering is not an option, when flexible polymer substrates, such as PET (polyethylene terephthalate) are used. The main reason is the high (over 200 °C) temperature which is needed in reflow-soldering. PET starts to melt temperatures between

200 - 260 °C depending on the PET-type [46]. The glass transition temperature of PET is only 70 - 78 °C [46] which means that some deformations in PET starts to happen already then. Therefore, flip-chip bonding with anisotropic conductive adhesives is mostly used with PET [47] because it can be done in lower temperatures than soldering.

2.3.1 Adhesives

There are three types of adhesives used in the electronic attachments: non-conductive adhesives (NCA), isotropic conductive adhesives (ICA) and anisotropic conductive adhesives (ACA). Electrically conductive adhesives (ACA and ICA) are based on non-conductive polymer binders, which are typically made from epoxy [48]. The conductivity of the adhesives is created by adding conductive filters, typically silver, nickel or gold metal particles or metal coated polymer particles [48,49].

The working principles of the adhesives are shown in Figure 7. ICAs are conductive in every direction meaning that it needs to be placed only between the bumps and pads. Residual area between the component and substrate needs to be covered with underfill.

ACAs conduct only in one direction. When ACA is heated, the particles, which face pressure between the pads and bumps, deform causing them to conduct. That causes the conduction only to the vertical direction. The benefit of the one direction conductivity is that the current from the chip leg goes only down to the pad and precision of the component placement control does not need to be so high.

Using NCA, the pads and bumps are pressed towards each other in a way that they are in direct physical contact. Then the NCA functions only as a support and attach the component on the substrate.

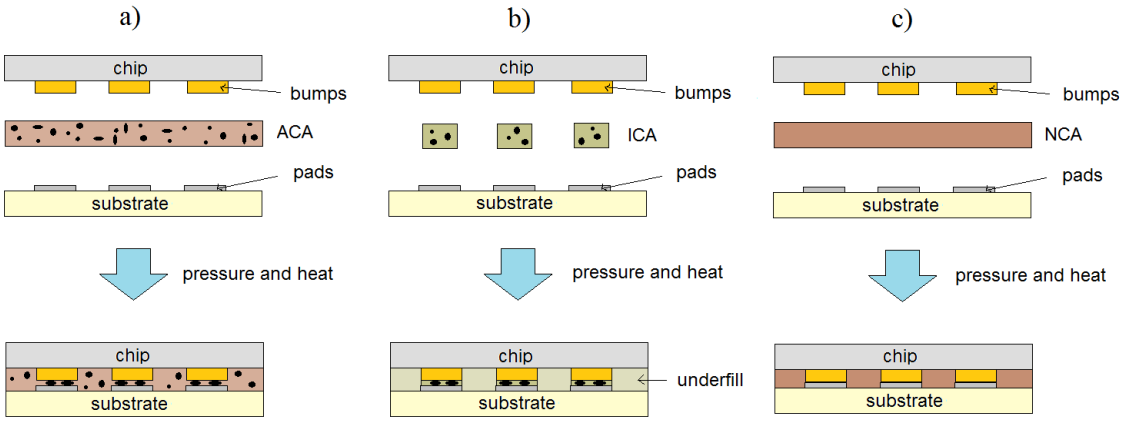

Figure 7. *Attaching principles with a) ACA, b) ICA and c) NCA.*

Adhesives are available in two forms: paste and film. Non-conductive, anisotropic conductive and isotropic conductive pastes are shortly called NCP, ACP and ICP and non-conductive, anisotropic conductive and isotropic conductive films are called NCF, ACF, ICF. The advantages of films are shorter curing times and easier handling [50]. In addition, the conductive particles are distributed more uniformly in film than in paste.

ACA is considered more reliable option for the fine pitch attachments. However, there are multiple facts that support the use of NCA. NCA is cheaper and it creates a larger contact area which leads to the smaller contact resistance [49]. The NCA bonding does not have the short circuit problem where adjacent pads are connected through particles [49]. NCA bonding is, however, more sensible to bump height variations than ACA bonding [49].

There are multiple advantages of using ACA with flip chip bonding instead of reflow soldering also for those applications where it is not the only option:

- lower curing temperatures
- high resolution capacity due to smaller particle size enables lower pitch sizes
- higher mechanical flexibility = less sensitive to thermomechanical stresses
- simple processing due to less process steps, no need for underfill
- no lead = environmentally friendly [51,52].

All the advantages of ACA make it perfect choice for flexible electronics and for the miniaturization of electronics. A remarkable thing is that there is no need for underfill which reduces process steps. Disadvantages of ACAs compared to soldering are higher contact resistance and lower current capability [53]. Furthermore, the contact alignment needs to be more accurate because there is no self-alignment as with solder.

2.3.2 Flip-chip bonding

Flip-chip bonding is a common method for attaching SMT component or bare die on substrate in electronic industry. The conventional flip-chip process goes according to the following steps. First solder bumps are created top of the chip pads. Then the chip is turned on and picked up to the tool. The tool aligns the pads and bumps and presses the chip on the substrate. After heating, the joints are formed. Using solder or ICA the protective underfill still needs to be dispensed.

Solder bumps are not placed when using flip-chip bonding with adhesives. When adhesive films are used, film has to be first pre-laminated on a substrate before component placement using some pressure and heat. The flip-chip assembly process with adhesive films is shown in Figure 8. Pastes can be dispensed, screen printed or stencil printed on a substrate before the placement of a chip.

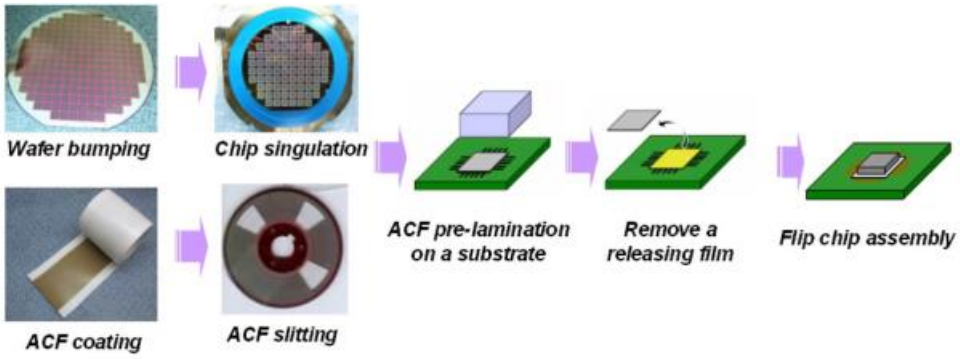

Figure 8. *Flip-chip assembly process using ACF [54].*

Currently, ACFs have been widely used for flat-panel display module packages, such as liquid crystal displays (LCD), plasma display panel, and organic electroluminescence display, and flip-chip module packages, such as chip-on-glass (COG), chip-on-film (COF) and chip-on-board (COB) [55]. Chip-on-film or chip-on-flex (COF) is a fabrication technology that was first applied in liquid crystal module of small panel [56]. There driver chips were attached on a film using flip-chip bonding. The substrate film was typically two-layer structure (copper and silicon). After that, multiple studies of COF have been performed [57-61] . When the easiest way to fabricate conductive patterns on foils is printing, flip-chip bonding on printed interconnections has been tested. Van den Brand et al. [62] bonded 100 μm pitch chips on screen printed PEN with ACP. However, they used embedded circuitry what means that they made grooves where the ink was printed. That provides a smooth contact area for the ACP particles. Van den Brandt [47] also bonded 300 μm chips on screen printed circuitry using ACP.

3. FLEXIBLE ELECTRONICS

A clear advantage of hybrid electronics is the possibility to manufacture flexible and stretchable electronic devices. This chapter will present the fundamentals and background of flexible electronics and after that concentrate on the bendable electronics and their bending tests.

3.1 Introduction to flexible electronics

The development of flexible electronics started 1960s when first flexible solar cell arrays were made [63-64]. In 1980s the researchers started to development flexible displays and backplane TFT-circuits (Thin Film Transistor) for them [19]. Since then, the flexible electronics is closely linked to large-area electronics because the main flexible electronic products have been solar cells and displays.

Typically, a flexible large-area electronic device is composed of substrate, backplane electronics, frontplane and encapsulation [19]. All of them have to be flexible. Two approaches have been applied: (1) transferring completed circuits to a flexible substrate or (2) fabricating them directly on the flexible substrate [19]. The first approach covers the idea of hybrid flexible electronics. Printing methods are used for the second approach.

Flexibility of a material depends on its thickness. Thin layers are more flexible than thick layers. Conventionally the material used in electronics is silicon in its crystalline form. It is mechanically fragile and cannot be bent. Amorphous silicon (a-Si) is more flexible and for that reason widely used for flexible electronics [65,66]. Also other semiconductors, such as indium-gallium-zinc-oxide (IGZO) in their amorphous form are used [67]. In addition, rigid semiconductors are thinned in order to make them more flexible. According to van den Brand et al [47], thickness under 25 μm makes silicon chips flexible.

Another approach to achieve the flexibility is to use naturally elastic materials, for instance plastics. Electronics from plastics are possible to manufacture using printing technologies with flexible inks and substrates. That is a cost-efficient way to create flexible electronics with roll-to-roll processes. Polymers have the possibility to be very flexible and rather cheap material and that is why many plastic types, including polyethylene terephthalete (PET), polyimide (PI) and polyethylene naphthalete (PEN) are used in flexible electronics. They are also good isolators which is important for an electronic substrate. Unfortunately, the melting temperature of polymers is low which creates challenges for some processes.

Flexibility can also mean many different things for different people and applications. There are multiple degrees of flexible electronics: bendable, rollable, conformally shaped and elastically stretchable. In some applications, the whole device must not be flexible; it is enough if some part of it is.

A promising technology to manufacture high performance flexible systems is a Hybrid System in Film (HySiF) [68]. There the organic printed electronics and ultra-thin silicon chips are embedded into one system which is manufactured partly inside a foil [69]. That idea combines flexible and hybrid electronics.

3.2 Bending tests

The bending stress to the device can be caused from internal or external causes. Different coefficients of thermal expansion (CTE) of the used materials cause internal stress when the ambient temperature is changing. The external bending stress is mainly caused by someone or something that is bending the device.

The bending stress caused by different CTEs usually occurs when the device is in high temperatures and then disappears when the loading is removed. However, materials which are plastically deformed, as polymers are, may still contain stress when they are unloaded [70]. The stress can damage the device.

There are two types of stress on bending: compressive and tensile stress as shown in Figure 9. On compressive bending, the chip is inside the bending circle and on tensile bending the component is outside the circle. The bending curvature, when the device fails, can be very different in both situations.

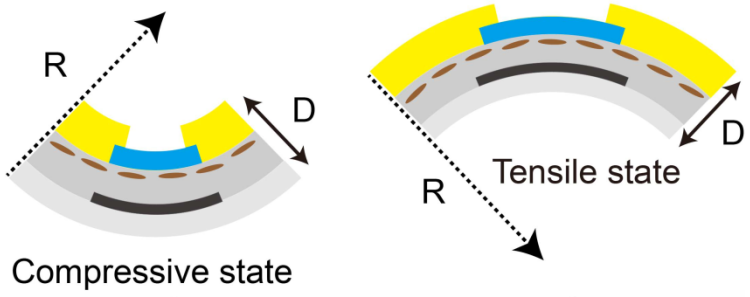

Figure 9. *Compressive and tensile stress on bending [71].*

3.2.1 Test methods and standards

Because the field of printed electronics is so new, there are no certified standard test methods yet to test the flexibility of printed electronic devices. Each researcher has chosen his own method and mostly they have built the test devices themselves.

There are two fundamental ways to perform a static bending test. First one is just to bend the device in certain bending radius, for example around a circular item, and see if it functions after it. Other way is to investigate what is the minimum bending radius by bending the device little by little and measuring it all the time. Dynamic bending tests include many bending cycles in order to evaluate the long-term bending reliability of the device.

In the field of mechanics and materials, the three- and four point bending tests are popular. Also the flexibility of conventional printed circuit boards (PCB) are tested with those tests for example according to JEDEC JESD22-B113 standard [72]. In the test, the test sample is placed on two rigid supports and then a one or two loading points are bending the device according to the Figure 10. However, the flexible electronics substrates such as PET and PEN –foils, are very flexible. When the foil has been bent once, it will not get up. Therefore 3- and 4-point test methods are not suitable for this purpose.

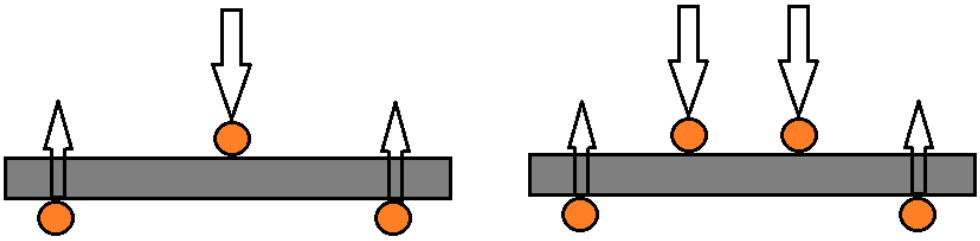

Figure 10. *3- and 4- point bending tests.*

The mechanical strength and reliability of conventional PCBs are also studied using ball drop simulation [73]. Its aim is to simulate the impact loading into one point of the board.

Bending tests with folding a flexible device in two parts are relatively easy to perform. Josh et al. [74] folded supercapacitors according to the Figure 11. The flexible supercapacitor was attached to two rigid supports and bent to the chosen bending angle. The repeatability of this test is good but the actual bending angle in the device is hard to define. It depends on the device attachment mechanism on the support.

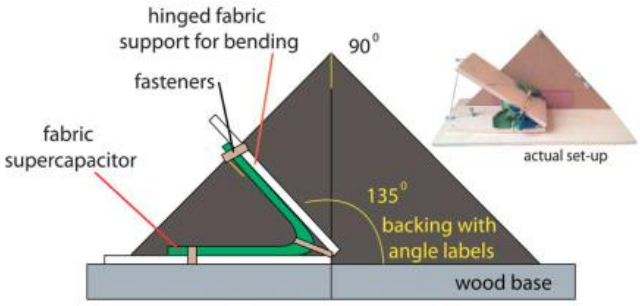

Figure 11. *Folding test set-up [74].*

If dynamic bending tests are wanted to flexible electronics, a rolling test (used in [75,76]) is a possible way to perform it. The principle of the test is shown in Figure 10. The sample attached between two plates and moving the other plate the sample rolls.

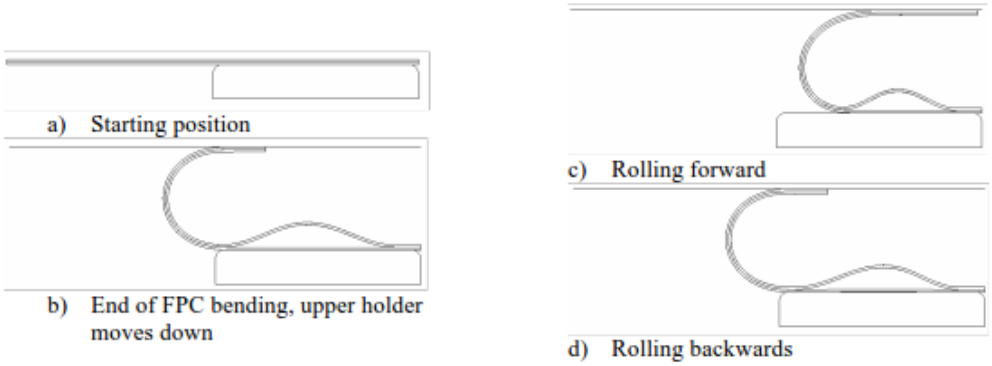

Figure 12. *A rolling test principle [77].*

In paper industry, test equipment, such as taber tester, is used to measure the stiffness of paper. They are so called X-Y-θ –systems. The test sample is fixed on the other end and another end is bent according to the Figure 13. That could be good style to test the bendability of film-based printed electronics. Unfortunately, the commercial paper stiffness testers usually are able to go only until 90° of bending angle. For that reason, buying that kind of quite expensive machine for bendability tests for flexible electronics might not be reasonable.

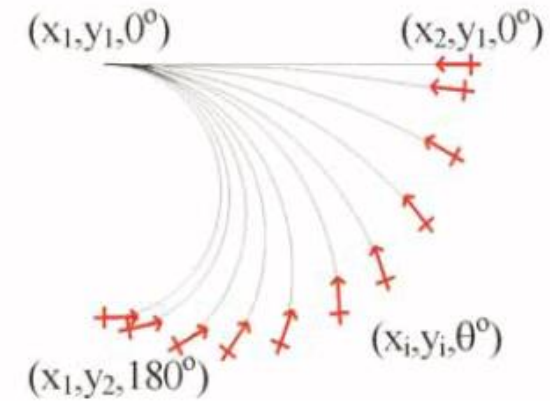

Figure 13. *X-Y-θ bending system [78].*

Some of the researchers have used two rigid support plates and bent the film between them according to the Figure 14 a) [79]. The lower plate is static and the upper plate position can be controlled to choose the right bending radius. With that method, it is then possible to determine the minimum bending radius which the device can stand. The plates are possible to attach any kind of device which can control the movement of the other plate. Burns et al. [79] have done this with a Universal Tensile Machine (UTM).

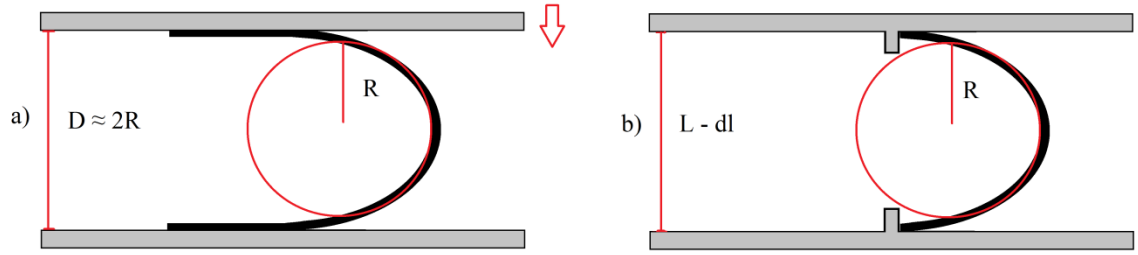

Figure 14. *Bending test principles.*

However, this method bends the device more sinusoidal than to round curve. In order to find out the exact bending radius, the correction term needs to be defined:

$$r = \frac{L}{2\pi\sqrt{\frac{dL}{L} - \frac{\pi^2 h^2}{12L^2}}} \quad (1)$$

where L is the initial length of the specimen, dL the rate of change of the length and h is the thickness of the whole specimen [80]. Although this correction term has planned for the bending test method in Figure 14 b). In Figure 14 a), the length of that part of the sample which is being bent is decreasing with the bending radius because the both end of the samples are not fixed as in Figure 14 b). The sides of the samples cannot be horizontal way attached to the plates using the correction term. The actual length of the bent sample should be measured in each point of the bending radius to determine the actual bending radius according to formula (1). That is why it is hard to determine the exact bending radius when the device is bent according to Figure 14 a). However, a good approximation of the radius can be calculated dividing the distance between the plates to half.

3.2.2 Previous studies

Various bendability studies of printed interconnections on flexible substrates have been made [15,76,81-84]. Flexible inks are already available and in case of hybrid flexible electronics, the printed circuitry is not the first one to cause problems. More challenging is to get the other components and their interconnections to the printed circuitry reliable in a way that they do not break on bending the device.

Bending tests for flexible displays are already widely performed. Chen et al. [30] bent flexible e-paper display to bending curvature of 15 mm without any degradation and Burns et al. [79] bent their e-paper display to bending curvature of 5 mm without degradation.

Other far developed flexible electronics field: RFID-tag industry, has studied the flexibility of their products. Usually, silicon ICs are used in RFID-tags which makes their

studies interesting also for the hybrid electronics point of view. Cai et al. [32] bent the chip on PET on a mandrel which diameter was 20 mm. However, the chips used in RFID industry are large and their pitch is also large meaning that they are not good examples of fine-pitch applications.

Some bending tests for chip interconnections on flexible substrate have performed. Jokinen and Ristolainen [85] have studied the interconnections of a chip on PEN substrate. They bonded thick and thin (50 μm) chips. The used chips had 250 μm pitch and 25 μm high gold stud bumps. They made the interconnections with flip chip technique using anisotropic conductive film with particle size of 3 μm. They investigated the bending reliability of the structure using 3 cm bending radius with some samples in the environmental stress tests. With bending, little higher resistance on interconnections was measured but it had no effect on reliability of the interconnections.

Lu et al. [86] performed static bending tests with curvature of 15 mm and 25 mm to 50 μm thin chip (10 mm x 3 mm) on PI substrate. The bending curvature of 25 mm did not change the contact resistance after 1000 hours but the joints failed after 24 hours with curvature of 15 mm. They also performed cyclic bending tests with 0.25 Hz bending frequency. The bending amplitudes were 10 mm and 15 mm. All test samples survived 500 cycles without any significant increase in resistance. Because the bending mechanisms of the static and cyclic tests were different, any correlation between the tests cannot be seen.

4. EQUIPMENTS AND METHODS

In this chapter, the materials and methods used in experiments are discussed. That includes the test sample manufacturing as well as describing the bending tests.

4.1 Test samples

A test sample consists of a silicon microchip and printed wiring on PET substrate. The test samples were prepared jointly at VTT Technical Research Center of Finland (Valtion teknillinen tutkimuskeskus) and TUT (Tampere University of Technology). VTT screen printed the wiring and fabricated the bare dies, with the bonding of the chip performed at TUT.

4.1.1 Test chips

Bare silicon chips without any interposer or package was chosen to bond. One reason is the minimization of the process steps which decreases the costs as well. Other reason is the maximization of the bendability. The hypothesis is that the rigid areas have to keep as small as possible to achieve good bendability of the device.

Two different test chips were fabricated. They are both square and have 80 I/Os; 20 in the each edge. A test chip #1 had two daisy-chain structures meaning that every second pad was connected inside the chip. When the chip has been attached on the substrate, it is easy then to measure if there are faulty connections by measuring the resistance between two adjacent pads. If they are connected, there is a short circuit somewhere. A test chip #2 has two adjacent pads always connected. The connections of the chips can be seen in Figure 15.

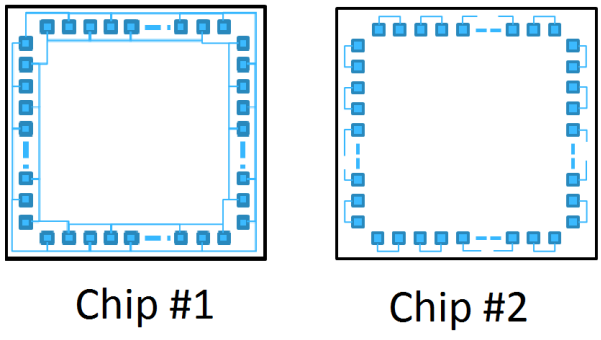

Figure 15. *Test chip connections.*

The test chip #1 is used to find the suitable bonding parameters and the test chip #2 for bending reliability tests. The distance from the center of a chip pad to the center of its adjacent pad is called a pitch. Three versions of both chips with different pitches were ordered in order to study the dependence of pitch and chip size on the reliability. The sizes of the chips can be seen in the Table 3. Since the number of IOs is the same for these three chips which have different pitch, the chips have different dimensions.

Table 3. *Chip dimensions.*

pitch	length of a side (21·pitch)	chip area
150 µm	3.15 mm	9.9 mm^2
175 µm	3.68 mm	13.5 mm^2
200 µm	4.20 mm	17.6 mm^2

Chips have 60 µm x 60 µm aluminum pads. When the aluminum is in contact with air, a thin aluminum oxide layer is formed on top of the aluminum. That layer is insulating.

Usually gold or nickel/gold bumps are fabricated on top of the pads to make the bonding easier. Gold stud bumps were ordered on top of the chip contact areas for selection of the chips. Stud bumps were fabricated with high precision wire bonder cutting the gold thread to the balls.

4.1.2 Screen printed substrates

The wiring on PET was printed with a rotary screen printer. The thickness of the PET foil is 125 µm. The used ink was Asahi silver conductive paste LS-411AW. The printed test structure for the test chip #1 can be seen in Figure 16. It includes 80 test pads, where the connection of the chip and wiring can be evaluated. Every second pad should be short circuited after the chip has been bonded. In order to find out if, for instance, connection number 3 works, two resistance measurements will be done. If pads 1 and 3 or 3 and 5 are short circuited, then the connection 3 between the chip and substrate works.

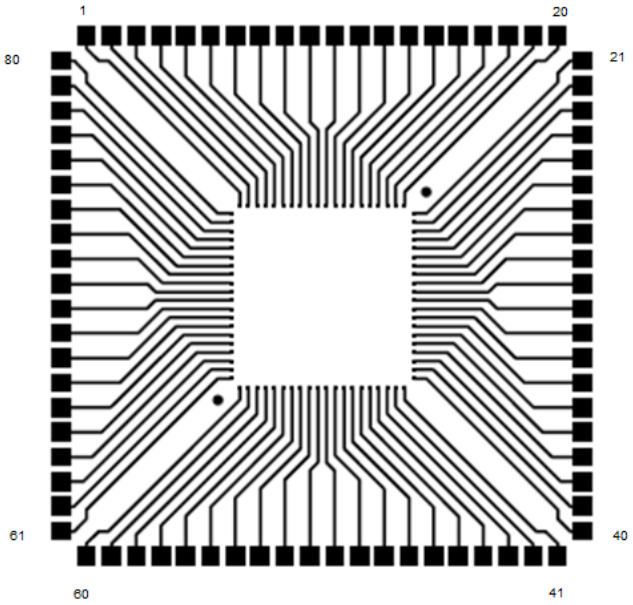

Figure 16. *Printed wiring structures for test chip #1.*

First the minimum possible line width and spacing between the printed lines had to be solved. In order to do this, 16 different line width and pitch combinations in Table 4 for test structure #1 were fabricated. Also four different screens: Stork S305, Stork S355, Gallus KMS and Gallus KF were tested at VTT Oulu.

Table 4. *Nominal line width and pitch combinations.*

column number	pitch (P) (µm)	nominal line width (L) (µm)
1	150	50
2	175	50
3	200	50
4	250	50
5	150	75
6	175	75
7	200	75
8	250	75
9	150	100
10	175	100
11	200	100
12	250	100
13	150	125
14	175	150
15	200	150
16	250	150

Test patterns in Table 4 were sent to conductivity measurements in order to find out the best line width and pitch combinations. Resistance of every line was measured to see if the line is continuous. Also the short circuits between two adjacent lines were checked to see if they are connected.

According to the optical and electrical observations, the Stork S305 screen was working best. Other screens have problems with line spreading; the lines were in a contact with their adjacent lines. Patterns with pitch 150 µm and line width 125 µm as well as patterns with pitch 175 µm and line width µm 150 included lots of short circuits due to the small 25 µm gap between the lines. The failures of other patterns with Stork S305 screen can be seen in Figure 17. Most of the failures were open circuits meaning that the lines were broken somewhere.

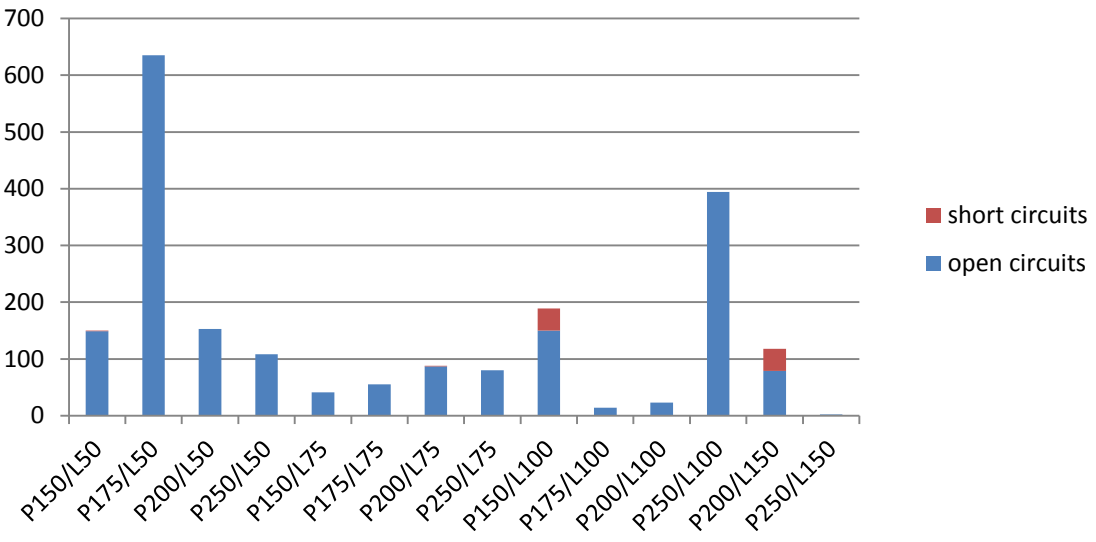

Figure 17. *Failures in printed circuitry measurements.*

From the Figure 17 can be seen that the P175/L100 and P200/L100 seem to be the most reliable options. However, it is more beneficial to use as small pitch as possible. In addition, the effect of the pitch on the bonding and bending wanted to be evaluated choosing three different pitches: P150, P175 and P200 for the following tests. When only one line width was chosen for the following print trials, 75 µm was the best option due to the smallest amount of failures. Printing with L75 produced 184 failures while L50 made 938 and L100 produced 226 failures. That is why the combinations P150/L75, P175/L75 and P200/L75 were chosen to fabricate for the following bonding tests.

After the good line width and pitch combinations were found, layouts for bonding and bending tests were fabricated with those combinations. The picture of the printed wiring structure for bonding tests is shown in Figure 18.

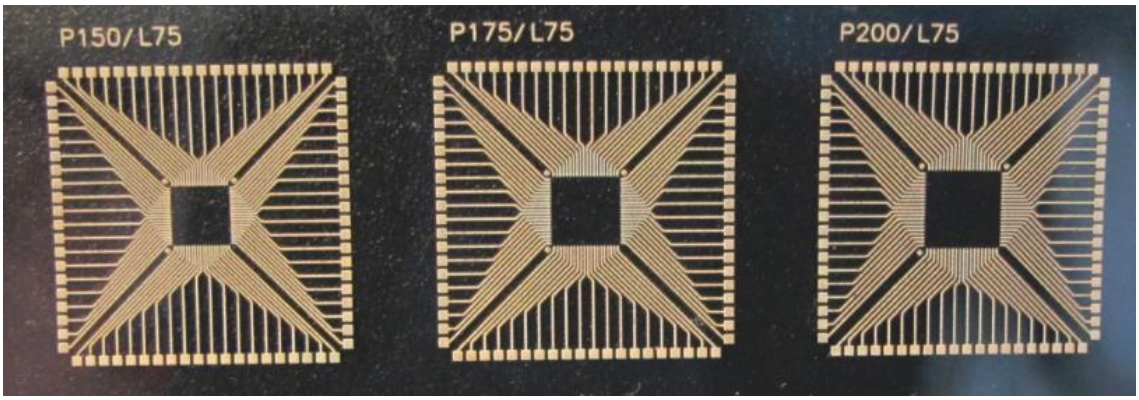

Figure 18. *Screen printed test layouts for bonding tests.*

Two wiring structures were designed for the bending tests. One according to the Figure 19 and another otherwise similar but the chip has turned 45°. Both of the structures were designed for three different sizes of the chip. That wiring structure forms 8 daisy chains around the chip, two for each edge. They are now called sectors. Measuring the resistance from the eight sectors, the breaking place of the connections on bending can be determined.

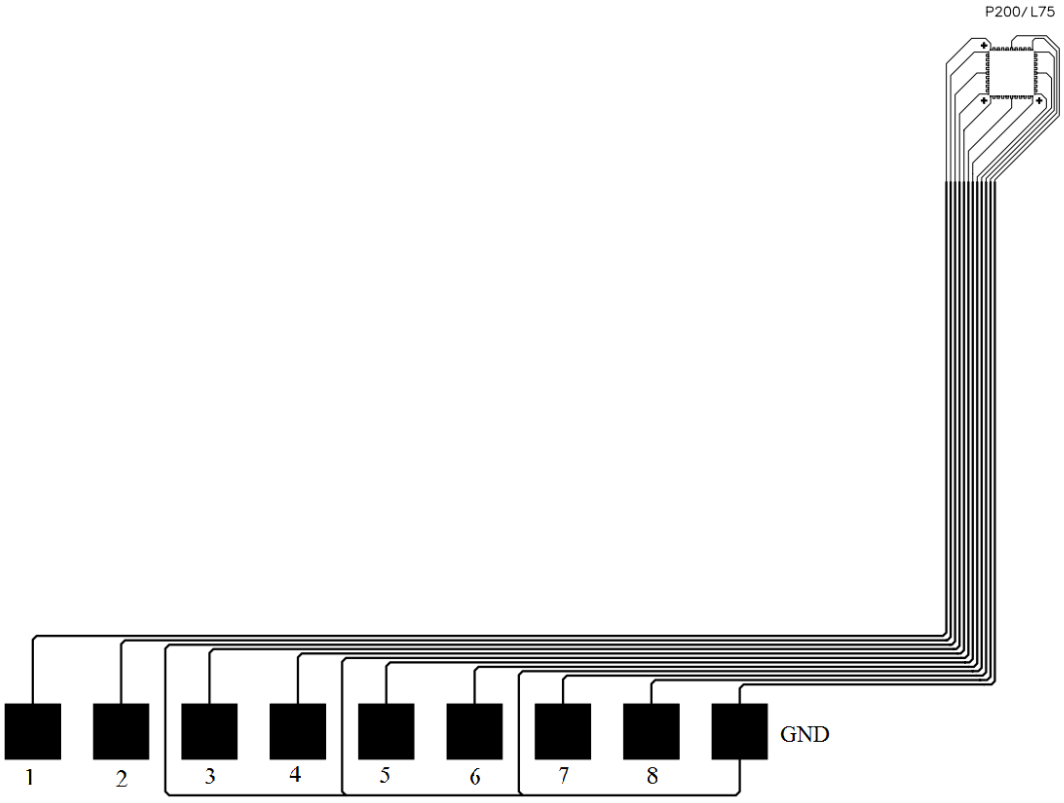

Figure 19. *Wiring structure for bending tests (P200/L75 version).*

4.1.3 Bonding of the chip

The flip-chip bonding was performed manually using a Finetech fineplacer. The picture of the fine placer is in Figure 20.

Figure 20. *Fineplacer.*

First, adhesive is placed on the screen printed substrate and then the substrate is placed on to the plate. Paste adhesives are in a syringe and they are dispensed on a substrate through a needle using a dispenser. The right amount of the paste needs to be found out experimentally. If film is used, the right area of the roll needs to be cut and then pressed on the substrate. Film needs a pre-bonding phase, where it is attached to the substrate. In pre-bonding a glass piece is placed on the film and then the film is pressed and heated.

When the adhesive is on substrate, the chip is picked up to the tool the active side down. The alignment of the chip on to the substrate pads is done manually moving the plate under the substrate and seeing the both parts in a microscope. Finally the chip is pressed on to the substrate with the wanted force and the heating is started. The heat comes from the tool and the plate under the substrate. Both temperature profiles can be set from the computer. A pressing force can be chosen to be 0.1-20 N. After heating, the tool is lifted up and an attachment is ready.

Three different adhesives for bonding were tested: two anisotropic conductive adhesives and a non-conductive adhesive. The details of the adhesives can be seen in the Table 5.

Table 5. *Used adhesives.*

	ACF	ACP	NCP
form	film (thickness 40um)	paste	paste
conductive particle	Au/Ni coated polymer (5 μm)	Ni-Au particle (2.5 μm)	no particles
recommended bonding temperature and time	190 °C, 15 s	150 °C, 5 s	180 °C, 8 s
recommended pressure	100g /bump	-	-

In conclusion, the whole test sample fabrication process is described In Figure 21. Two different kinds of samples were fabricated: one with test chip #1 on a substrate for it and another with test chip #2 on its substrate.

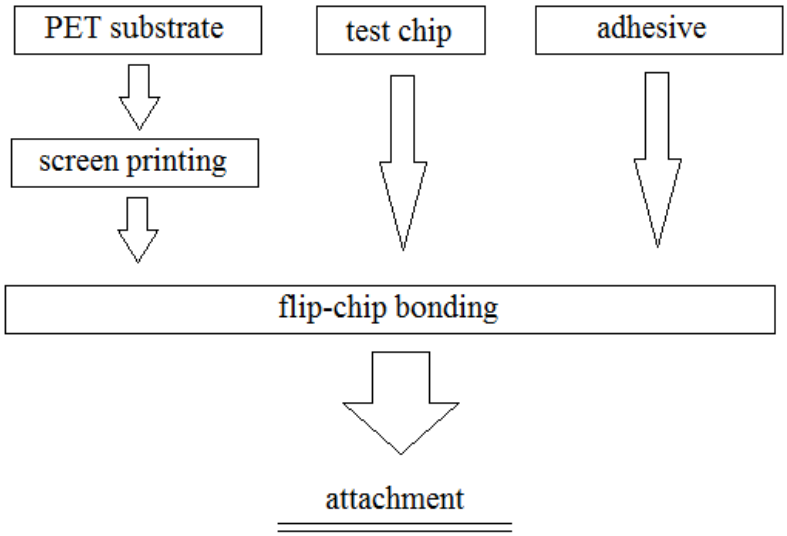

Figure 21. *The process flow chart of test sample fabrication.*

4.2 Bending test set-up

The bending test method what was chosen to these measurements was the plate-test described in the previous chapter 3.2.1. The test apparatus is self-built.

The test set-up for bending tests consists of an Instron 4411 Universal Tensile Machine (UTM) which works as a bending device and an 8-channel resistance measurement system in Figure 22. Special tools for the tester were ordered. They function as plates and between them the sample is bent.

The resistance measurement system includes 3D-printed contact clips, 8-channel measurement card, virtual bench -device and computer with LabVIEW-program. LabVIEW controls the Virtual Bench which drives the measurement card. The measurement card measures the resistances of each channel one at a time and a time before each loop. The frequency, in which the virtual bench changes the channel, can be controlled from LabVIEW. However, the measurement card is quite slow and with high frequencies it is less reliable. That reason the measuring frequency is good to be low. Also the bending speed can be chosen from the UTM.

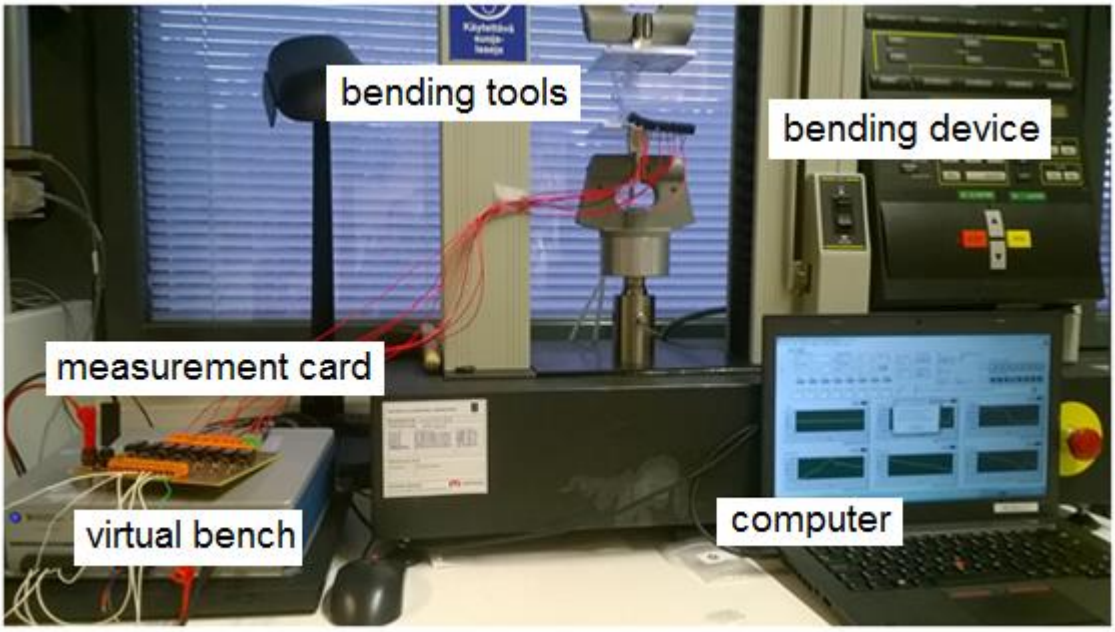

Figure 22. *Bending test set-up.*

At first, some preparation for the bending tests has to be done. First the jigs are installed to the UTM using a compressed air pedals which press the tools to be still in their places. The levelness of the tools is measured with a level. The plates have to be as parallel as possible. After that, the wires are attached to the T#2 substrate measurement pads using 3D-printed clips. Now the sample is ready to be placed between the jigs. The sample is curved a slightly and taped both of its end to the plates.

The starting point of the bending test is the distance between the plates. It is measured with a slide gauge and recorded. The control program of the Instron is opened and a compressive test type is chosen. The wanted bending speed is pre-determined. Then the resistance measurement from LabVIEW is started at the same time with the bending program and the measurement starts. When all channels are broken or the bending cannot be performed anymore, measurements are stopped.

The output data of the test is a text-file including the time and resistance vectors from the eight channels. Matlab-program is used to combine the resistance data with the distance between plates and find out the breaking radii of the samples. In Appendix A is presented a Matlab-code what was made for drawing the resistances of the measurement channels as a function of the bending radius and helping to find out the breaking points.

Manufacturer of the ink promises conductivity degradation under 10 % after 10 cycles of 360° bending [87]. In these bending tests only one bending cycle was meant to do and after one bending cycle of 360°, the resistance of the printed lines remains unchangeable. Therefore, the only remarkable resistance change comes from the junctions when the sample is being bent as in Figure 23.

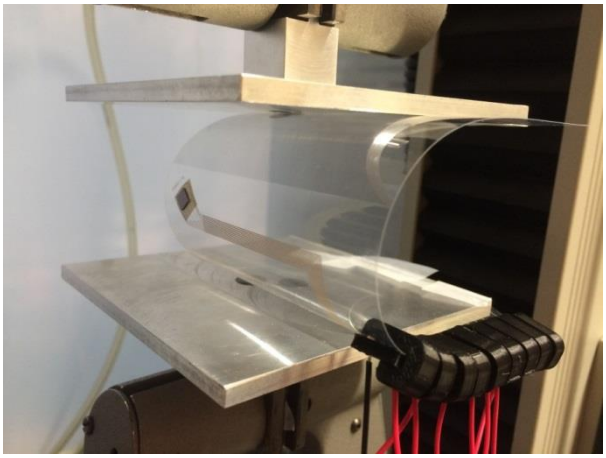

Figure 23. *Sample is being bent.*

Sampling frequency of the measurement card is set to 0.42 Hz meaning that the resistance values from every eight channels are measured in 2.4 s. The bending speed can be decided to be enough slow for this sampling rate. The bending diameter, which is between the two plates in Figure 23, is measured with the accuracy of 1 mm. This leads to the result that the measurement system has to measure the resistances more than once at the 1 mm movement of the plate. It was chosen that the system should measure the resistance of the channels at least 10 times in that distance. To be in a safe area, the speed was chosen to be 2 mm/min. Then the device measures the resistances approximately 12.5 times in a 1 mm distance of bending.

The starting point of the bending test is possible to be measured with the accuracy of 1 mm. There are two reasons for this accuracy. First, the tools are waving lightly when it

is touched which makes the measuring challenging. Secondly, the tools are not infinite planar. The height difference between plate edges is still under 1 mm. Comparing to this accuracy, the 12.5 data points in 1 mm distance is much and the sampling rate is not limiting the accuracy of the measurement.

Since the bending diameter is possible to determine with an accuracy of 1 mm, the bending radii has a 0.5 mm accuracy. The bending radius is not exactly a circle but still called as a bending radius and that has to be remembered.

The samples are bent according to the axis on the Figure 24. The idea is to concentrate only to this type of bending for this study. The channels of the resistance measurements sectors are numbered to the Figure 24.

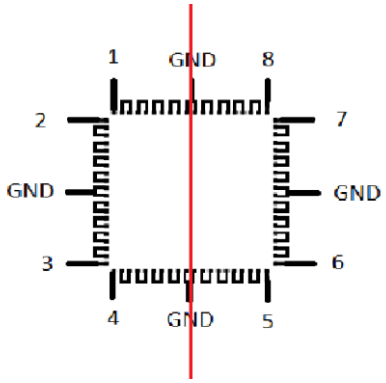

Figure 24. *Bending axis versus the channels.*

Overall 27 samples were bent and they are classified in Appendix B. All the samples were bonded using ACP. Two different-sized chips were used in the bending tests; chips with 150 µm pitch and chips with 175 µm pitch. Most of the samples have stud bumps.

4.3 Analyzing methods

This chapter describes the methods which are used to analyze the samples and results in the next chapter. The electrical connections of the attachments were measured with FLUKE 87 true RMS multimeter.

Cross-section pictures of the attachments were prepared in order to observe the quality of the attachments. The cross-section figures were fabricated by moulding the samples and then cutting the mould in the correct place. First the PET substrate including the attachment was cut in a small piece that it would fit in the mould. The substrate has to be cut exactly parallel to the wanted cross-section line. After that, a sample holder is attached to the sample and the sample is placed to the mould with the wanted cross-section surface down. Epoxy is mixed and injected into the mould. After eight hours of drying the mould was finished.

The epoxy cylinder including the sample was then grinded in order to achieve the wanted cross-section depth. It was done with sandpaper grinding machine grinding the sample little by little and checking it under the microscope between grinding steps. When the chip bumps/pads started to see in the microscope, the right depth was achieved. After that, the cross-section surface needs polishing. Polishing is done first with fine sand paper and after that with diamond granules.

Many optical microscopes were used to investigate the polished cross-sections of the attachments and to observe the bonding results. PET-substrate is transparent which allows the observing of the attachment alignments through the substrate. That is a large advantage. Many pictures were taken with microscopes to analyze the findings further.

Wyko NT1100 surface profilometer was used to analyze the screen printed lines. It measures the distance to the surface optically and gives the 3D images of the surface as well as the 2D data of it. The profilometer data was analyzed with Vision 4 program from Veeco instruments Inc. It calculates the average roughness and average height -values of the chosen areas. Matlab-program in Appendix C was written and used to set the x-axis to zero level in the cross-section figures that the Vision-program created and to draw better figures.

Matlab program was used to draw pictures about the results from the bending tests and analyze the data. Minitab program helped with the statistical analysis of the bending and bonding results.

5. RESULTS AND DISCUSSION

This chapter reports the results of the tests described in the previous chapter 4. It also analyses and discusses them.

5.1 Bonding results

The bonding trials are described in this chapter. Bonding was performed according to the chapter 4.1.3.

5.1.1 Bonding with ACAs

The recommended heating in bonding was 15 s at 190 °C with ACF. However, it takes time to heat the tool and chip, thus some extra seconds are needed to add to the heating phase. In addition, the actual temperature is lower than the set temperature, meaning that the temperature has to be set to be larger than the recommended temperature.

The first challenge in bonding was proven to be the sensitivity of the printed lines. They did not survive 20 seconds when the tool temperature was set to 210 °C and plate temperature 100 °C. The wires peeled off the substrate and bent according to the Figure 25. The temperature was clearly too much for them. Reducing the tool temperature with multiple trials to 150 °C or shortening the bonding time did not help. Instead, setting the plate temperature to be only 40 °C helped and bonding was performed more successfully. Then the majority of the heat comes from up and the heating of the substrate is minimized. That should prevent the adhesion problems with the silver ink and substrate on heating.

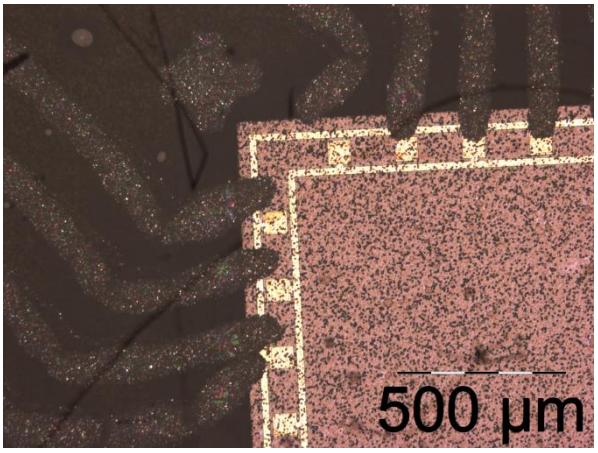

Figure 25. *Damaged wires after bonding (T_{tool} = 180 °C, T_{plate} = 100 °C, t = 20 s).*

Another challenge is to get right bonding pressure all over the chip. The bonding pressure is very accurate because the aluminium pads are thin and the printed pads rough. The pressure has to be high enough to press particle in ACA and get them to conduct. As the cross-section picture of one ACP bonded sample (Figure 26) can be seen, there is too much space between the pads in that sample and no particle is conductive. That means that the bonding pressure was not enough. On other hand, when the pressure is too high, also other particles that are not under the pads are pressed and they will conduct leading to short circuits.

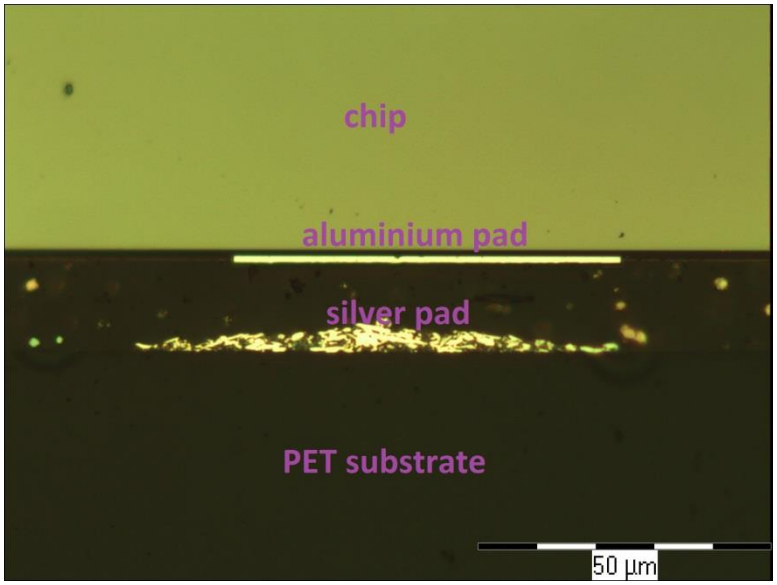

Figure 26. *Microscopic image about the cross-section of the sample with too low bonding pressure (800 g).*

In order to get the same pressure all over the chip, the chip and the substrate have to be physically parallel when the chip is pressed. The angle θ (in Figure 27) between the surfaces can only be very small. The particle size of the ACF is 5 µm and the particle size of the ACP is 2.5 µm. If the printed pads are assumed to be similar, the height difference between the two opposite sides of the pads has to be less than the particle size. For the chip which side is 3.68 mm, and particle size 5 µm, the angle is 0.08°. If the particle size is only 2.5 µm, the angle is 0.04°. The thickness of the printed pads is about 5 µm. From this simple calculation, it is to be concluded that the height control has to be accurate.

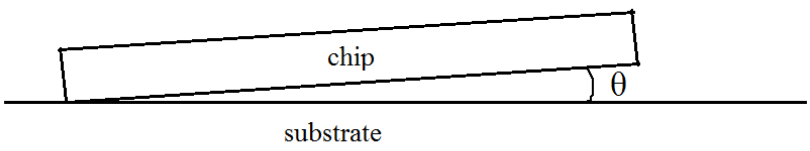

Figure 27. *The principle of height difference on bonding.*

Unfortunately, the height control with the fine placer is not that accurate. It is done manually rolling the rolls and every time when bonding is done, it has to be again. Also the levelness of the tool may not be optimal since the tool is already old. The inaccurate levelness of the bonding was noticed in a way that the connections were working good on one side or corner and not at all on the opposite side or corner. The process to get the tool levelled was slow because the contacts of one sample have to be first measured in order to know which side is good. After that one roll is turned a little and the bonding and measurement circle is performed again.

However, working contacts were able to produce. The yield is still relatively poor but the failures are divided around the chip. Seven test #1 samples with paste with same height control settings and nine samples with film and same height control settings were able to manufacture. Bonding parameters were:

- paste: T_{tool} = 150 °C, T_{plate} = 60 °C, t = 5 s, F = 20N
- film: T_{tool} = 150 °C, T_{plate} = 40 °C, t = 20 s, F = 20N

The results of the bonding trials are gathered in the Table 6. One of the ACF bonded samples was all around short circuited and that is not marked on the Table 6. The cause for it is unknown because the contacts had good alignment when the sample was observed under the microscope.

Table 6. *Working contacts (out of 80) of the ACA bonding trials.*

Sample	1	2	3	4	5	6	7	8
ACP	75	75	76	65	73	71	71	
ACF	76	75	75	80	77	79	78	77

The mean values of the working contacts are 72.3 for the ACP and 77.1 for the ACF. Film seems to work a little better in this application. However, the amount of the samples is quite small and more precise conclusions would require larger amount of samples. It is possible that the bonding parameters and other variables were only better optimized for the film. On the other hand, the samples show that it is possible to make working contacts with good repeatability.

One challenging thing is to define a working contact. Contacts, which daisy chain resistances were below 500 ohms, were marked as working contacts. The resistance measurements from the test #1 attachments include two 6-7 mm long silver traces, the contacts and a short distance on a chip. The majority of the actual resistance should be caused by the silver lines on the substrate. The resistance of the lines is somewhere between 7 and 11 ohms, as known from the measurements done for the printed wirings. The measured contact resistances of the worked contacts are shown in Figure 28.

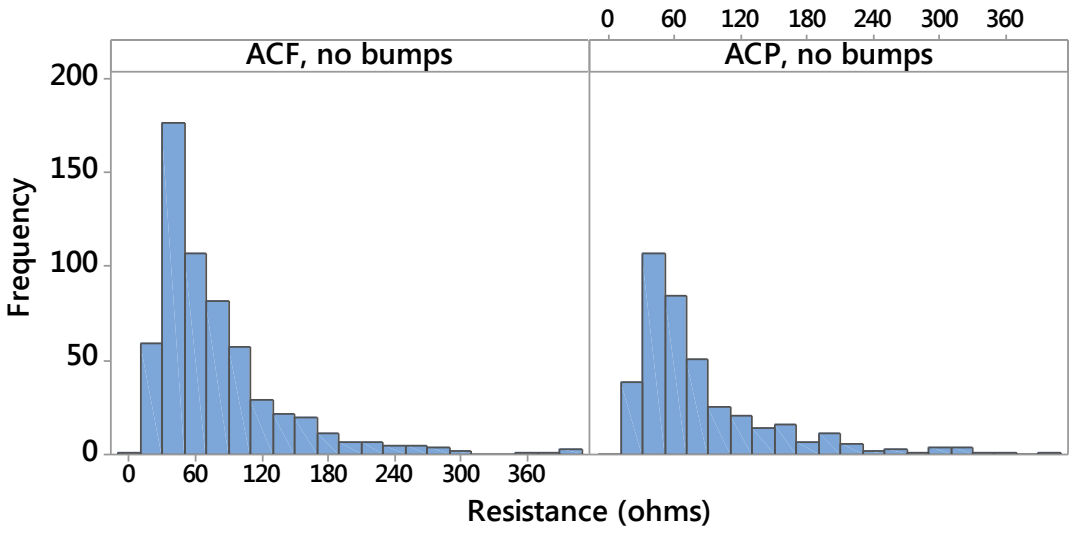

Figure 28. *Histogram of contact resistances of the test #1 attachments with ACAs.*

As can be seen, the deviation of the contact resistances is large and the mean values (78.4 Ω for ACF and 82.9 Ω for ACP) are much larger than the resistance of a printed silver line. In addition, the exact value of one contact resistance was changing every time when it was measured. For example after one day, the contact resistance can be a lot different. That indicates the unreliability of the contacts.

Cross-section images of the attachments were prepared in order to know the quality of the attachment. One example of a working contact is in Figure 29. There is clearly a conductive path for the current but the roughness of the silver pad is affecting. It cannot be known are the particles deformed and really conductive or is the conductivity caused by the silver flakes of the traces which are in a contact with aluminium pads of the chip.

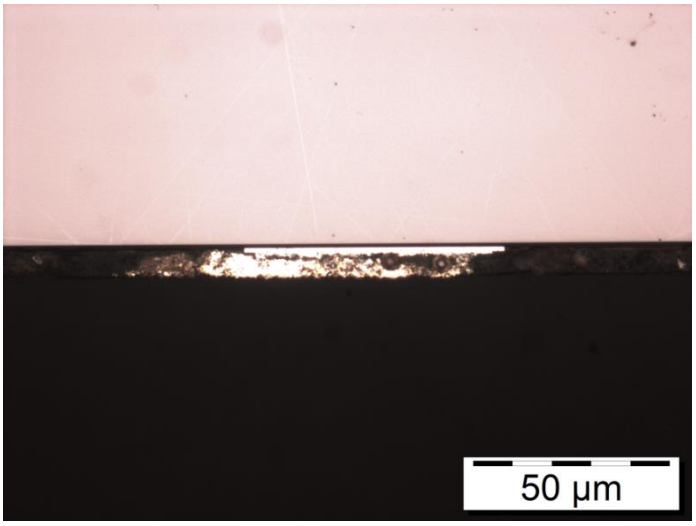

Figure 29. *Microscopic image about the cross-section of a working contact made with ACF.*

In addition, the height variations between different pads of the test structure and also between different test structures effect on the reliability and the yield. If there are some chip pads which are more flat, they more likely fail on bonding due to the larger gap between the chip and substrate. To make the bonding easier, chips with gold stud bumps were also tested.

5.1.2 Stud bumping

Samples with stud bumps were ordered to see if the bonding would be easier and more reliable results would be achieved. However, the wire bonder left a sharp tip to every bump as shown in Figure 30. Some of the bumps had a very long tail. They cause problems on bonding. A sharp tip can penetrate through the silver pad and even to the substrate on bonding. A sharp tip also provides a small and poor contact area to the particles to deform. A good way to increase the contact area and get the bump surfaces flat is coining. The coining was done with fine placer pressing the bumps with its maximum force 20 N. The coined bumps are in Figure 30 b.

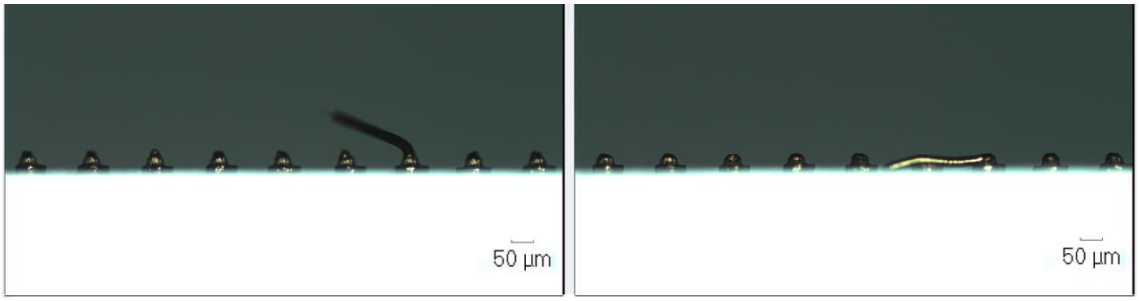

Figure 30. *Microscopic image about the side profile of a stud bumped chip a) before coining, b) after coining.*

As you can be seen from the Figure 30 b, the long tailed bump can cause problems after coining. If the tail goes towards the next bump, it causes a short circuit as in Figure 30 b). That is why every chip was checked after coining.

As from the figure Figure 30 can be seen, the height of the stud bumps is still large, between 40 µm and 80 µm. It would be good to use even more pressure than 20 N to press the bumps flat. Flat bumps should decrease the contact resistance and the amount of adhesive between the chip and substrate would be smaller. In addition, the contact area would increase. Unfortunately, there was no controlled method available to perform that.

The contact areas are smaller when bumps are used instead of aluminium pads. That affects the used force on bonding. The bump diameter is a little more than 2/3 of the chip pad edge l resulting that the bump radius r is 1/3 of the chip edge. The friction of the bump contact area of the chip pads is

$$\frac{\pi \cdot r^2}{l^2} = \frac{\pi \cdot \left(\frac{1}{3} \cdot l\right)^2}{l^2} = \frac{\pi}{9} \approx 0.35$$

That makes 0.35*20 N = 7 N for bonding. To be a little safer area, 8 N of force was chosen when bonding the stud bumped chips.

Finally when the bonding has done, the attachment looks like in Figure 31. That is a working contact. The bump penetrates a little to the silver pad and presses it, but still forms a good contact. Sometimes the bump went completely through the silver pad transferring the silver away from it. Then the bump touches mostly only the substrate and silver pads only in the edges. In some cases that may be the problem why the contact did not work.

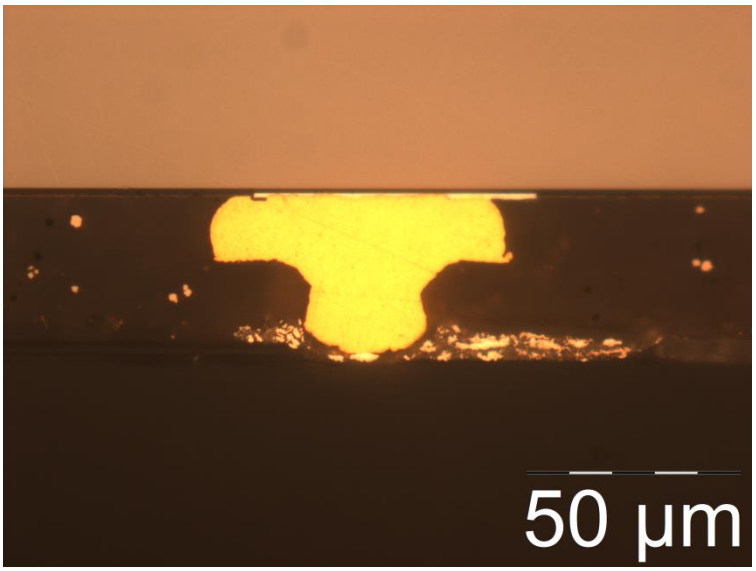

Figure 31. *Microscopic image about the cross-section of a stud bumped sample with ACP.*

The working attachments were done with ACP. When ACF was tested, the stud bumps or silver pads melted or there were air bubbles left between the chip and the substrate. That is shown in Figure 32. The reason for this can be the higher temperature of ACF bonding. The gold bumps are good heat conductors. The air bubbles can be caused by the large height of the bumps. The film has the same thickness all over it and it needs high temperature to melt and move away from the bumps. The used 40 µm film could not also be optimum choice for the bumped chips since the bumps were mostly higher than it. However, some extra adhesive was gushed under the chip. With paste this is simpler because it is ready to move away right after the chip is pressed. However, similar effects appeared also for the ACP bonded, stud bumped samples. That refers that the silver traces or bumps can be melting.

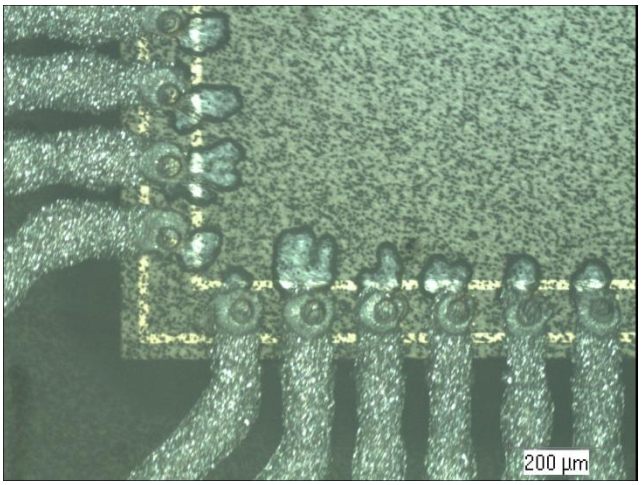

Figure 32. *Microscopic image from down of ACF bonded stud bumped chip.*

After all, stud bumping increased the yield and reliability of the attachments. In a 7 samples series, 6 samples worked perfectly (all of the contacts worked) and 1 was completely short circuited. That is a large development compared to the results on the Table 6. There was found no reason for the short-circuiting of one sample. If it is left out, the yield of the working contacts was 100 %. In addition, the contact resistances decreased remarkably as can be seen in Figure 33.

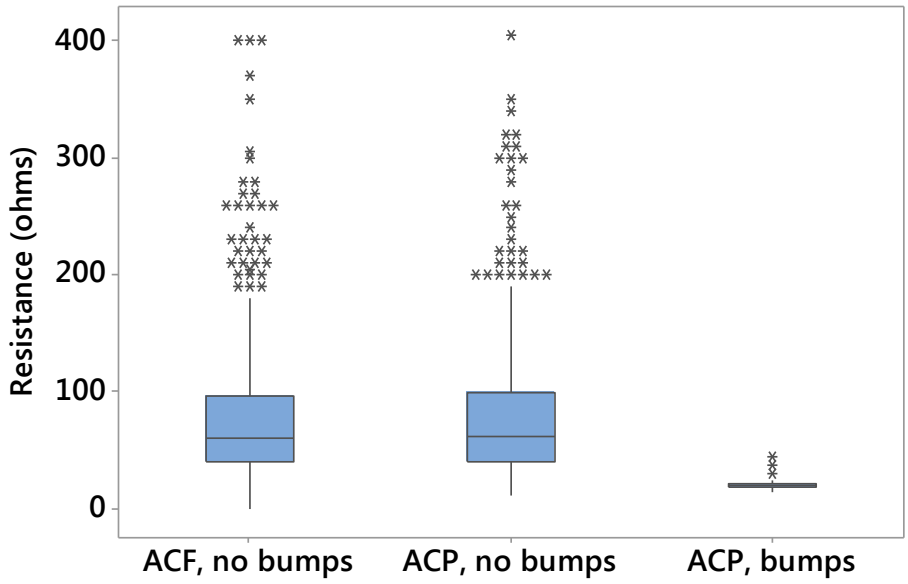

Figure 33. *Difference in contacts resistances.*

In the Figure 33 are shown the mean values as well as the deviation of the resistance values for bonded samples. The mean value of the resistances for stud bumped samples is 20.3 Ω which is a quarter of the mean values of the non-bumped samples. The deviation of the resistance values is also small when bumps were used.

When the resistance of the printed line was between 7 and 11 ohms, the added resistance of the attachments with bumps is about the same size. That feels an acceptable level. In addition, the variation of the contact resistances can mostly be result from the variation of the resistances of the printed lines since the length of the lines varies in the test substrates.

5.1.3 Analysis of the bonding and quality of the contacts

The holes of the silver traces are relatively large. Theoretically ACA particles could be trapped in those gaps. On the other hand, silver ink is quite soft and the ACA particles could even sink on the silver. It was very challenging to get the particles deform. From the cross-section figures (Figure 29 and Figure 31), it looks like that the silver ink is deforming when it is pressed and all the contacts are direct meaning that no particle is conductive.

For that reason, a non-conductive adhesive was tested to clarify this hypothesis. This kind of direct contacts would be fabricated cost-efficiently using NCAs. However, this is not an ideal way to perform bonding. Direct contacts are more likely to break on bonding and when the temperature changes.

One sample with stud bumps and NCP was bonded. The used bonding force was the same 8 N than bonding with ACAs. One corner was not working, but other contact resistances were similar than bonding with ACP. In addition, three samples without stud bumps were bonded with 20 N of bonding force. The amount of working contacts of those samples was 24, 26 and 32. That is less than in the previous bonding results with ACF and ACP (in Table 6). That might be only because the bonding parameters as well as the levelness of the tool were not optimized as good as bonding with ACAs.

Successful bonding with non-conductive adhesive proves that direct contacts without the help of any conductive particles are formed with that specific force. If the mechanic and elastic properties of the adhesives are otherwise similar, the 20 N of bonding force should be enough to form direct contacts also when ACAs are used. That hypothesis includes that the conductive particles are not remarkably resisting the silver traces to contact the aluminium pads.

When the aluminium pads of the chip have a thin insulating oxidation layer, a relative large pressure is needed that the particles of ACAs go through it and form a conductive path. On the other hand, large pressure could press the soft and rough silver traces to be a direct contact with the aluminium areas as mostly happened. The correct bonding pressure is therefore hard to determine. The particle size of the adhesive should be large to equalize the surface variations of the silver traces. 2.5 μm particles were not large enough as well as 5 μm particles.

Furthermore, the other parameters affect also much for the bonding results. Next are listed the critical parameters for the attachments which have noticed to have effect on bonding:

- bonding parameters:
    - temperature and its profile
    - time
    - pressure
    - levelness of the tool and substrate
    - height of the tool
    - chip and substrate alignment
- substrate variations:
    - curing time and -temperature of the ink
    - thickness variations of the printed lines
    - adhesion between ink and substrate
- adhesive:
    - particle size and hardness
    - particle amount and distribution.

Each of them has an effect. In order to know more about their relevance, systematic study with large sample size should be prepared and tested. In addition, a small movement of the chip on bonding caused problems.

5.2 Surface roughness and calendering

The particle size in adhesive A is about 5 μm, adhesive B 2.5 μm. If the silver line surface has gaps which are more than the particle size, particles will seize in those holes and do not feel the pressure. That can already be noticed from the Figure 26 where the silver pad is rough and curved. In addition, the surface height variations causes the particles feel different bonding pressure. Then all of the particles cannot work ideally at the same bonding pressure. The roughness of one pad can be seen in the following profilometer cross-section Figure 34. In that pad, there is a gap which is approximately 2.5 μm.

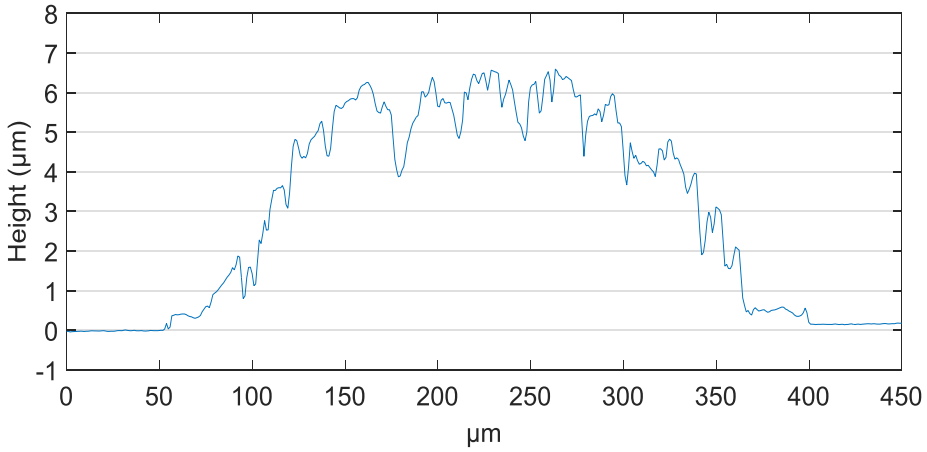

Figure 34. *Cross-section of the printed pad surface.*

The height variations between different screen printed lines are relatively large. That is caused by the ink drops which go through mesh openings. The mesh size is 40 µm. Then the 75 µm line has only one ink droplet side by side when the openings cover 21 % of the mesh area. Ideally ink droplets should spread smoothly but in real life some thickness differences on the lines are shown as can be seen from the profilometer image Figure 35.

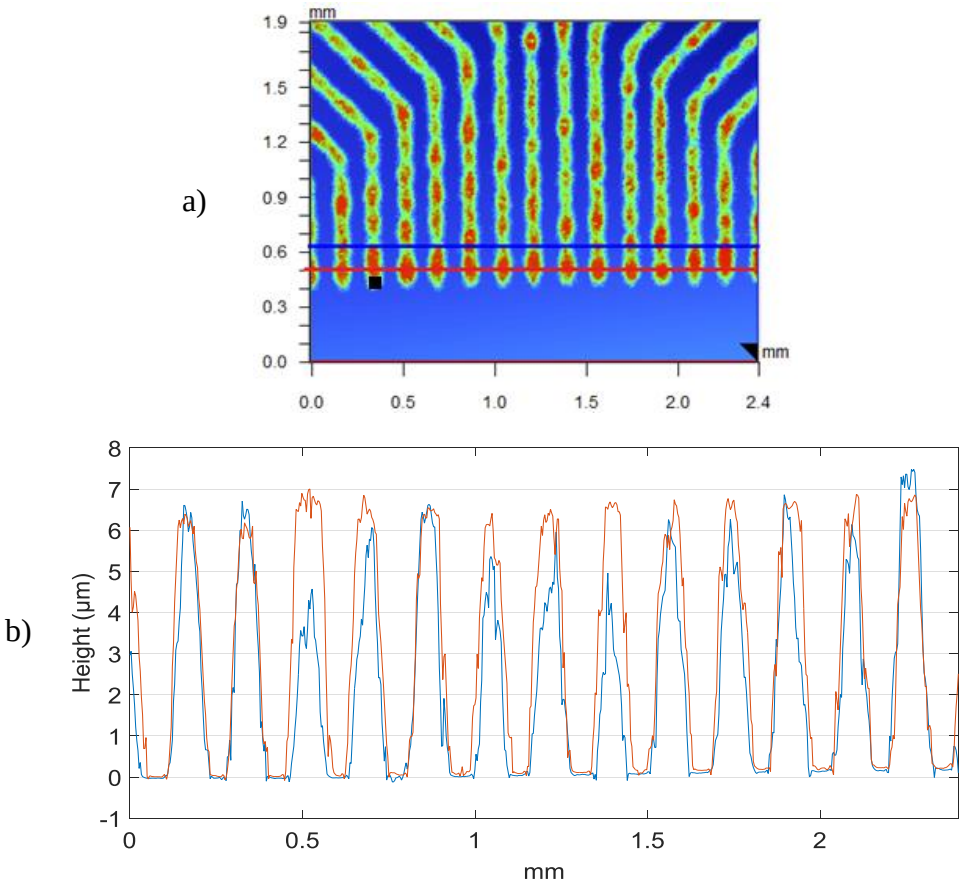

Figure 35. *Line height variations (un-calendered substrate): a) 2D profilometer picture, b) cross-sections of the lines.*

In Figure 35 b) are the cross-section profiles of a sample. The places where the cross-sections pictures have been taken are shown in Figure 35 a). Places, where has been a mesh opening and the ink has been gone through, are higher than the others. Also the line ends are higher. The height differences are at least 3 µm. However, they are only local variations and the chip pads are 60 µm wide. It is more reasonable to observe that size of areas.

The screen printed lines are just enough long in the centre to cover the pads of the chips. That can be seen in Figure 32. The edge of the line is naturally round. It takes approximately 70 µm that the line is on its full thickness. When the 60 µm long chip pads are in the end of the lines (as the black square in the third line in the Figure 35), they are not in the ideal place. For that reason, the lines should be designed longer for the future screen layouts. That would also make the alignment of the chip on bonding easier.

A solution to decrease the surface roughness and the height differences between different lines is calendering. Calendering means a compressing the substrate under pressure and heat [88]. That was performed for the substrates in a R2R-process at VTT where the temperature of the embossing cylinder was 120 °C and the pressure 15 bar.

The purpose of calendering is to equalize the height variations and surface roughness of the silver traces. The hypothesis is that when the silver pads would be more flat and their height would be more equal, the bonding would be done more reliable. The aim is to avoid open contacts which could be due to the more flat pads on the substrate.

The surface roughness of the un-calendered and calendered substrates was measured with an optical profilometer. The focus was on the inner sides of the lines where the chip will be attached. In Figure 36 are presented the line heights of calendered and un-calendered samples.

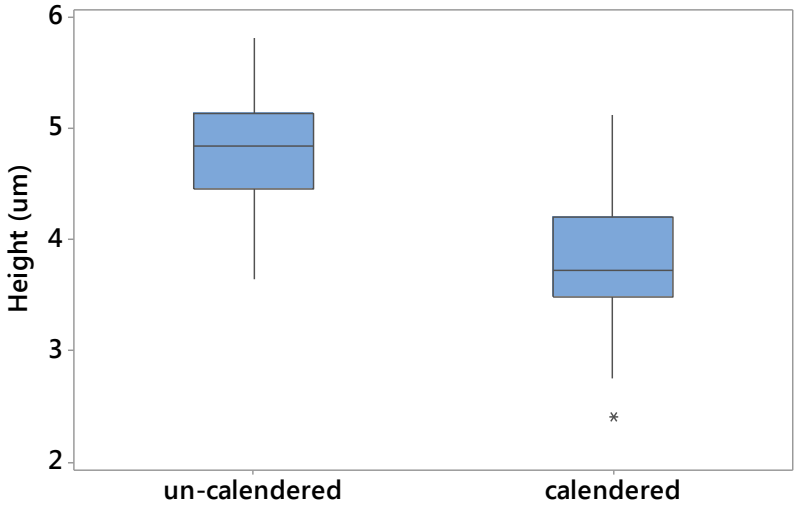

Figure 36. *Thickness of the screen printed lines.*

Line heights were measured from an area of 49 µm x 300 µm of the inner line ends. Four profilometer pictures of each edges of two un-calendered and two calendered samples were analysed. Average line heights from 189 pieces of 49 µm x 300 µm areas were calculated.

As can be seen, the un-calendered lines are higher. Calendering did approximately 1 µm reduction to the average line height. Similar effect can also be seen when comparing the Figure 35 and Figure 37.

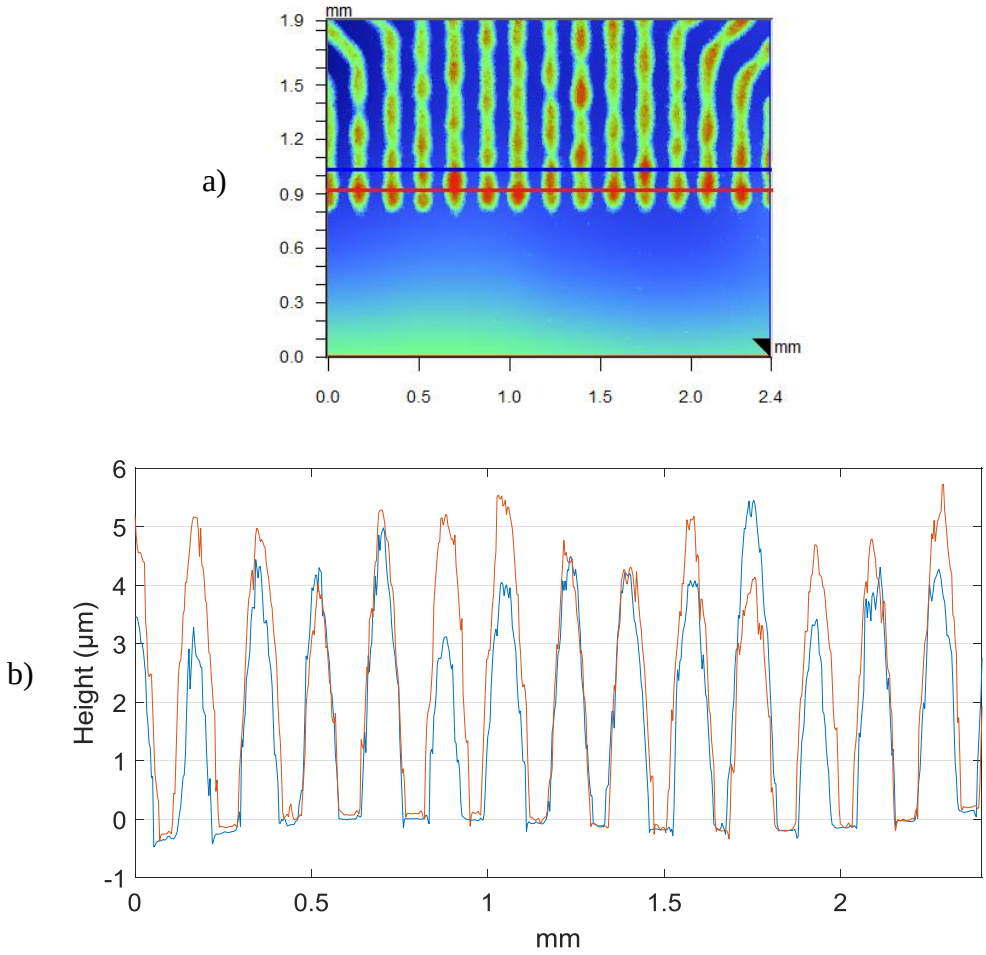

Figure 37. *Line height variations (calendered substrate) a) 2D profilometer picture, b) cross-sections of the lines.*

Calendering smoothened surface roughness of the screen printed interconnections. That can already be noticed when comparing the Figure 35 a) to Figure 37 a). In the pictures, red means high area and green low area. There are no more that high red spikes in the profilometer 2D-images after calendering. That results to the lower average surface roughness. The surface roughness of 49 µm x 600 µm areas from the lines of one calendered and one un-calendered sample was analysed. The results are shown in Figure 38. With those samples, calendering reduced the surface roughness approximately 0.3 µm.

However, more accurate conclusions would require more test samples. According to Jansson et al. [88] similar calendering process with same ink decreased 72 % the roughness of silver conductors.

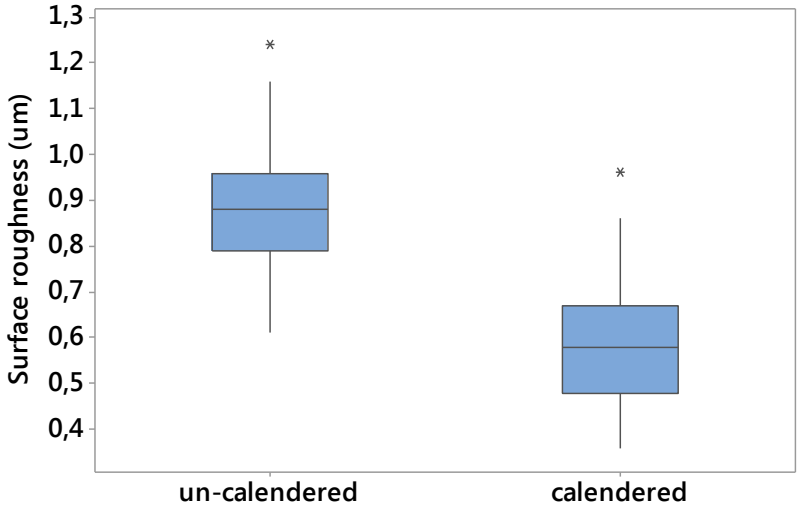

Figure 38. *Surface roughnesses for un-calendered and calendered sample.*

Calendered substrates were tested to bond with ACP. The height control on bonding was challenging also in this case but when the pressure was enough, contacts were formed. However, the results are not comparable to the previous results with un-calendered substrates due to the different height control settings. More reliable way to manufacture attachments need to be found before studying the effect of calendering on the yield.

5.3 Bending results

This chapter describes the results for the bending tests described in the chapter 4.2. The numerical results of tests are collected in Appendix B. First the bending results of each different sector and after that the results from the whole samples are discussed. In addition the effects of different pitch and bump of the samples are presented.

5.3.1 Minimum bending radii of the sectors

The initial resistance values of the sectors were mostly between 100 and 120 ohms. The interconnections were calculated broken when the resistance was increased more than 100 % on bending. When a sample was being bent, its resistance typically increased a little before the sample broke. In Figure 39 are shown the sector resistances (1st – 8th) of a sample with bumps and 150 µm pitch when it was bent.

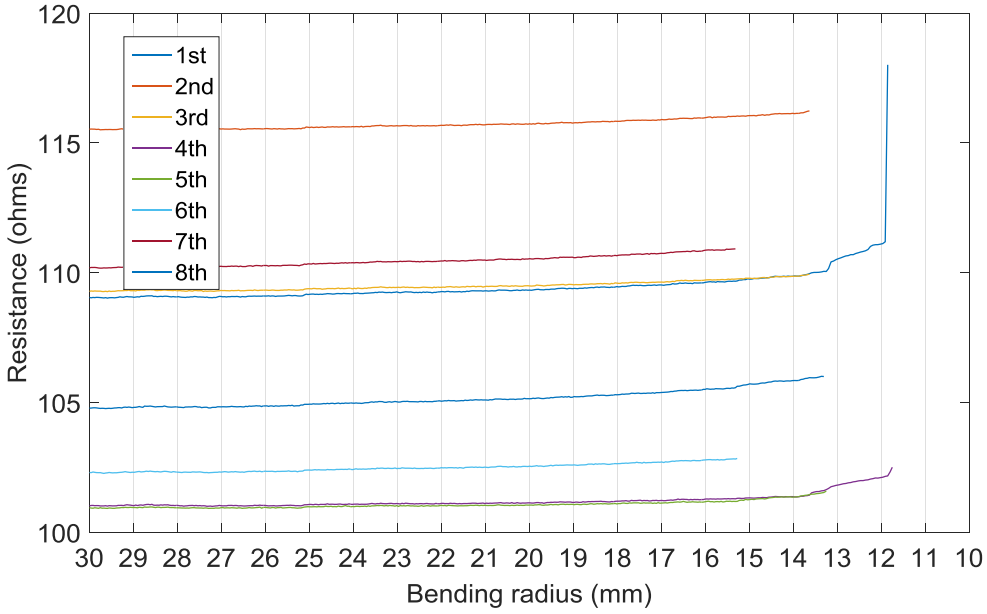

Figure 39. *Sector resistances as a function of bending radius*

As can be seen from the Figure 39, the resistances increased only couple of percent when the sample was bent. The peeling of the chip from the substrate was happening suddenly and rapidly, when the adhesive could not anymore keep the substrate under the chip. Then also the joints were broken fast and no significant increase in resistance was happening.

Many times the sample peeled off from the other side and it remained to hang on with the other side until the end. Then the sectors 2 and 3 or 6 and 7 never broke in the bending test when the test was able to go until the bending curvature of 8 mm. The results of the channels, which never broke in the tests, are not calculated in the following analysis where the minimum bending radii of the sectors are analyzed.

As could be predicted already before tests, the outer sectors 2, 3, 6, and 7 (see Figure 24) are more likely to break when the attachment is being bent. That can be seen in Figure 40 where the breaking points of the each sector for all bent samples are plotted.

The medians of the sectors 1, 4, 5, and 8 are remarkable smaller than the medians of the middle sectors 2, 3, 6 and 7. Also the 50 % of the data points for sectors 1, 4, 5 and 8 are smaller than the 50 % of the data points for the sectors 2, 3, 6 and 7 despite of the 0.5 mm overlap of sectors 3 and 5 in their boxes. What is to be remembered is that the non-breaking sectors where not included which makes the outer edge sectors look worse than they really are.

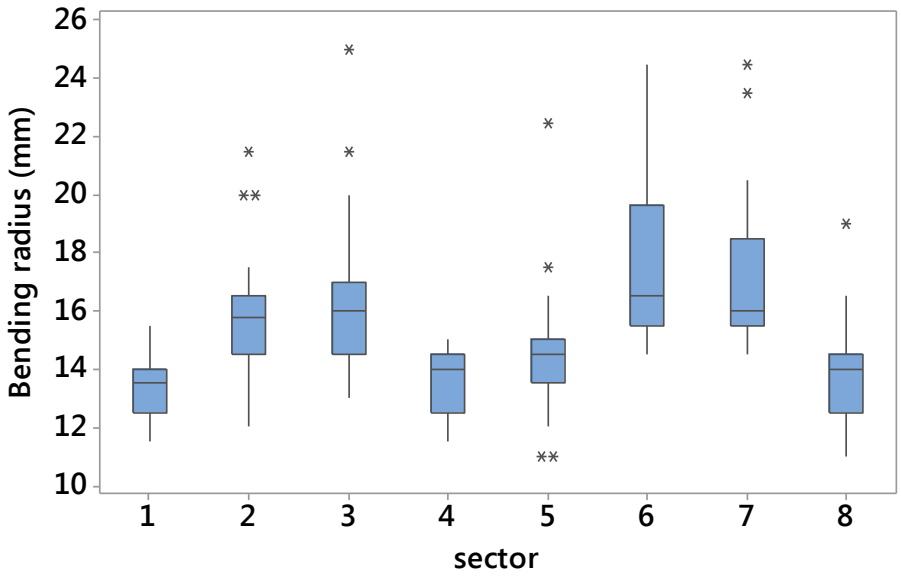

Figure 40. *Boxplot of the breaking points for each channel.*

Another interesting thing is to study how the breaking points of the all sectors are divided with the samples. The histograms of the breaking points for all sectors are shown in Figure 41. Samples with different pitches are separated for two cases. The statistics does not show standard deviation and the results are divided similarly in both cases. Approximately 14-15 mm of bending radius is the most common place to break.

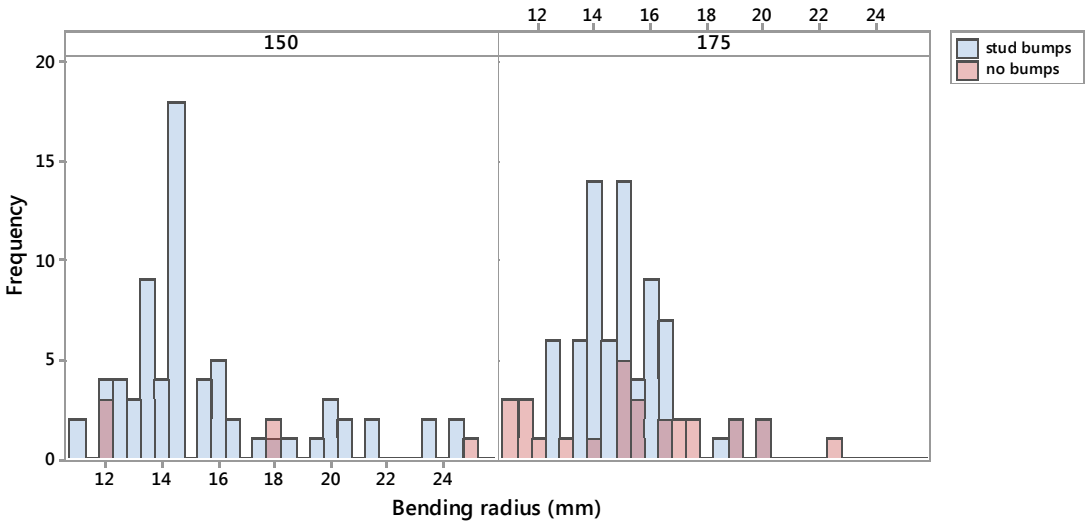

Figure 41. *Breaking radii of the sectors.*

5.3.2 Effects of the pitch and bumps

Bending radii for smaller chip (pitch 150 µm) are divided more widely but the radii look approximately same. The mean value for pitch 150 µm is 15.6 mm and for pitch 175 µm 15.1 mm which are shown in Figure 42.

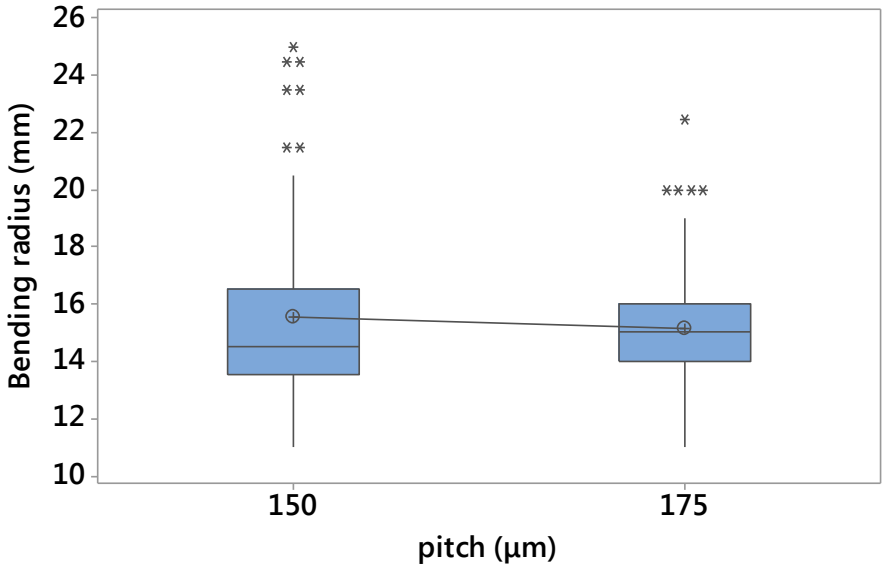

Figure 42. *Effect of the chip size on the bending radius.*

A Student's t-test is a test used in statistical analysis. It is used to determine if two data sets are similar or they differ significantly. If the hypothesis is that the data sets for both pitches are similar, Minitab-program gives the t-test t-value 0.99 and P-value 0.32. P-value tells that the distribution of the data points is not exactly standard. The t-value of 0.99 tells that it cannot be determined if the populations are different. That can already be seen in Figure 42 where the mean values are close to each other.

It seems that the size of the chip does not have a huge effect. The difference in mean values is the same than the accuracy of the measurement. Therefore no conclusions about the chip size influence on minimum bending radius can be drawn. However, the difference in chip sizes was 0.53 mm which is approximately same than the difference in mean values of the bending radii. It would make sense, if the difference of the bendability would be roughly the same amount than the difference in the chip size. If chips with larger size difference could have been used, the size might have a larger effect on the minimum bending radius. Then the difference in bendability could have been noticed easily with the bending test set-up used in this thesis. On the other hand, larger chips are more difficult to attach using fine placer due to larger height difference in the edges. Already the largest chip in bonding test (pitch 200 µm) was challenging to get working on its every edges and corners.

Another feature which may have an effect on the minimum bending radius is the used stud bumps in the chip attachment. Five samples (pitch 175 µm) without bumps were fabricated for the bending tests. Two of them have all sectors working before bending tests. A boxplot of the breaking points of the sectors divided for bumped and non-bumped samples is presented in Figure 43. All of the samples have the pitch of 175 µm.

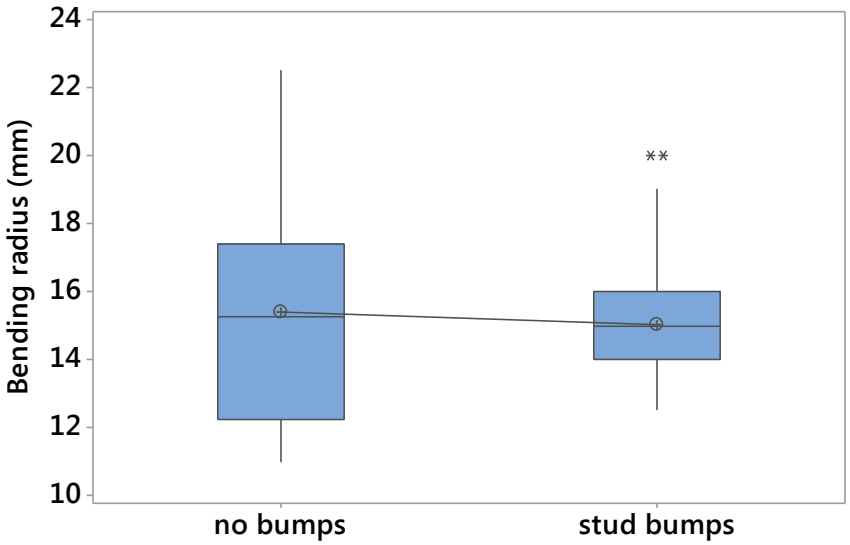

Figure 43. *The effect of bumps on bending radius.*

The mean value of the samples with gold stud bumps is 15.0 mm and the mean value for samples without stud bumps is 15.4 mm. The difference is statistically insignificant. A t-test t-value is 0.54 but the insecurity of the t-test results is large due to the small sample size and abnormally distributed deviation.

The quality of the joints seems to have a quite small influence on the minimum bending radius. That has something to do with the breaking mechanism.

5.3.3 Minimum bending radii of the samples

Sometimes the whole device has to work and if one joint is broken, then there is no use of that device anymore. The first breaking points of the samples are shown in the next Figure 44. Only the samples which all sectors were working were calculated in. In addition, all samples are stud bumped.

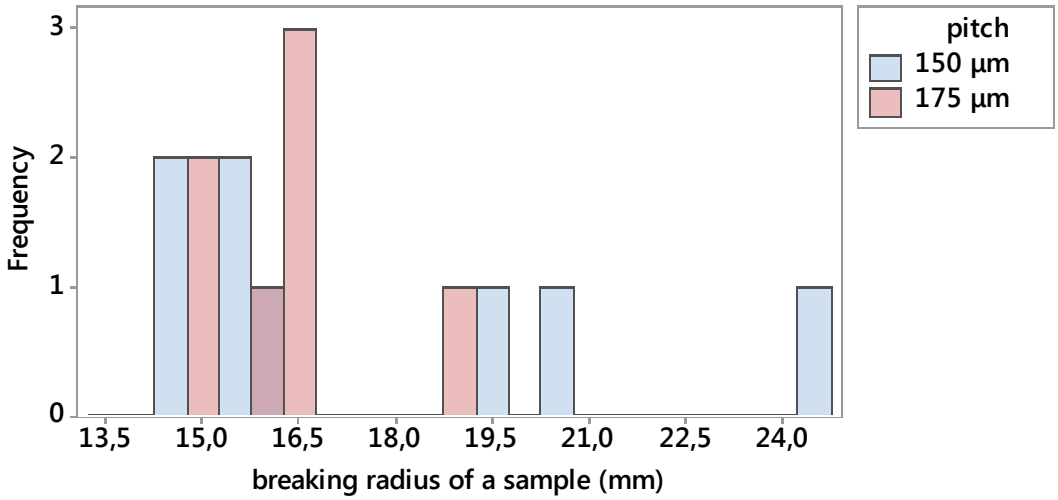

Figure 44. *Breaking radii of the samples.*

The mean values of the breaking points are 17.6 mm for pitch 150 µm and 16.4 mm for pitch 175 µm. The deviation of the breaking points is from 14.5 mm to 24.5 mm which is large. That can be explained from the bad joints. Also the sample attachment can have an effect. Sometimes it was not perfect and the foil had some minor extra waves on bending when the real bending radius could be smaller than the calculated one.

From the Figure 44 can be concluded that a 2.5 cm of bending radius is okay to these attachments. However, it cannot be said that the samples survive on a rounded surface which radius is 2.5 cm. The long term bending reliability has to be studied separately.

5.3.4 Breaking mechanism and long-term reliability

The breaking mechanism of the samples is the peeling of the adhesive from the substrate. That can be seen in Figure 45. Even the screen printed silver patterns are peeling from the substrate. That means that the adhesion between the chip and adhesive is better than the adhesion between the adhesive and substrate.

To make the adhesion between the adhesive and PET better, the adhesive and its curing need to be optimized. In addition, some extra mechanical strength from different adhesive which is put in the middle of the chip might help. In practice, that would be challenging to implement because the extra adhesive cannot mix with the ACA.

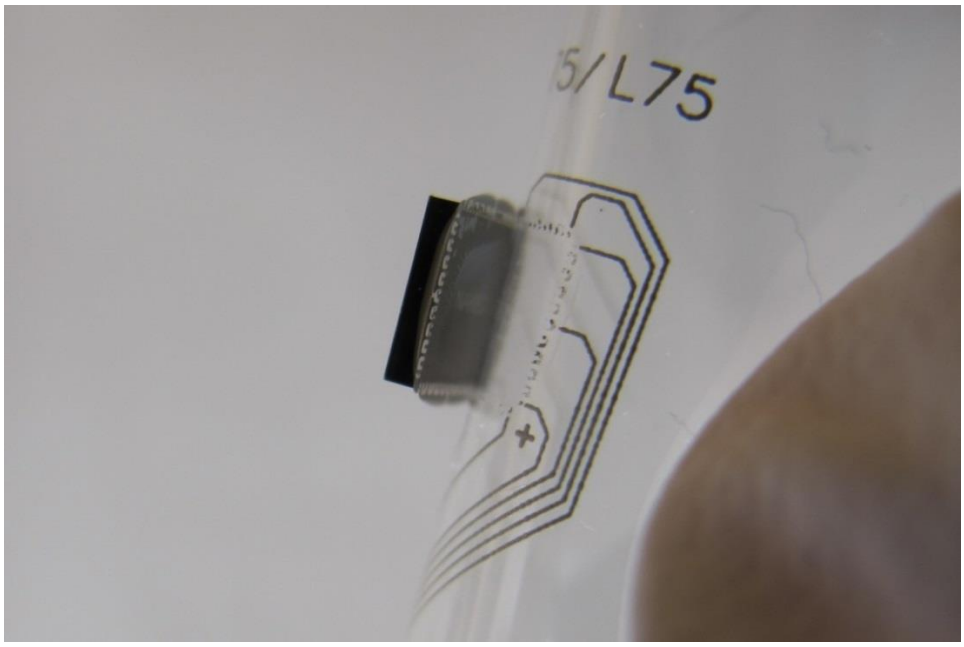

Figure 45. *The peeling of the chip on bending.*

To see if the contacts are really reliable in the long term, environmental stress tests are needed in addition to bending tests. To see how the attachments withstand moisture, samples were put to the test chamber. The humidity in the chamber was 85 % of relative humidity and temperature 85 °C. That is called a 85/85-test. Totally 9 samples were measured before putting them to the chamber and after 500 hours in the chamber. The results are shown in Figure 46. Contacts with bumps seem to work good also after 85/85-test. More degradation was happening in the samples which had no bumps. ACF lost more working contacts than ACP.

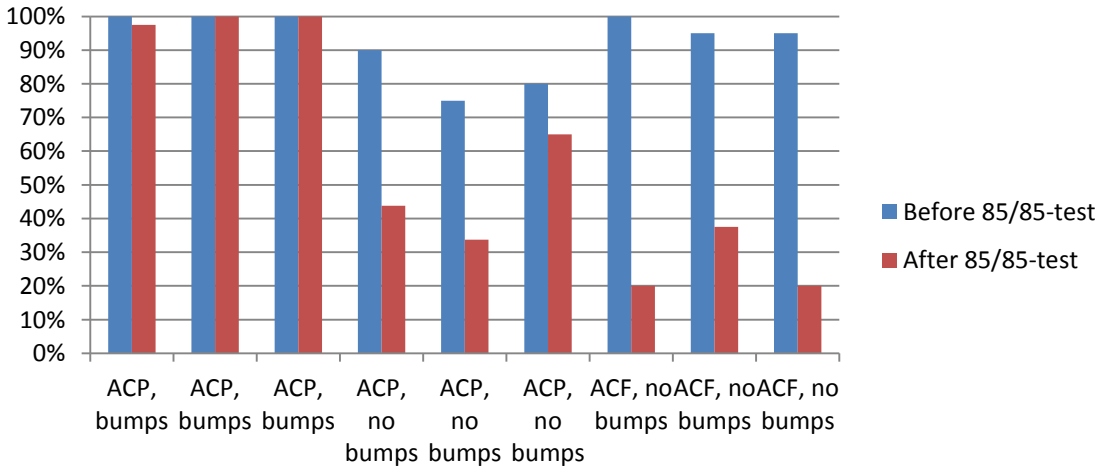

Figure 46. *Working contacts before and after 85/85 test.*

That 85/85 –test can be the starting point of future reliability tests of the flip-chip attachments on screen printed substrate. Some proposals for the future work are discussed in the next chapter.

5.4 Future work

The bonding of a silicon bare die on the screen printed high pitch substrate needs still further development. Ideally, the bonding would be done without any bumps when the number of process steps is minimized. Bumping is also an expensive step and could invalidate the advantage of low-cost screen printing. At least in the first phase, bumping seems to be essential. Very thin and smooth bumps for the chips would be ideal to order. Gold could be the best material for bumps because the hardness of gold is smaller than other metals [86]. Therefore gold bumps would act as soft joints between IC and the substrate when the device is meant to be flexible.

Furthermore, the adhesive selection needs to be planned carefully. The particle size should be large (larger than the tested 5 μm) and its hardness should be enough to break the aluminum oxide on the aluminum pads if no bumps are used. However, the particle should deform easily before the whole silver pad is pressed to the bump or aluminum pad forming a direct contact. In addition, the hardness of the printed silver lines would be good to measure in order to know how easily the particles sink in the silver lines.

Calendering reduced the surface roughness. If calendering would be done with higher pressure, the lines could be even smoother. In addition, many chips should be bonded on the un-calendered and calendered substrates with same parameters and settings in order to know if the different surface roughnesses have any significant effect on bonding.

When bonding is performed better and higher yield is achieved, environmental stress tests are needed to study the reliability of the joints. Tests, where the temperature varies are good to observe the quality of the joints: how easily they will break due to the tensions of different materials used in attachments. These kind of hybrid devices are meant to attach everywhere on our surroundings, also under the sun-light and moist environments. That is why moisture and UV-tests are good to see the long-term reliability of the devices.

Other R2R-capable techniques to manufacture interconnections would be interesting to study as well. For instance with etching processes, it would be possible to fabricate flat surfaces with certain accurate thickness instead of rough and rounded pads made by screen printing. Ahn and Guo [89] presented high-speed R2R nanoimprint lithography process where flexible plastic substrates can be used. They were able to manufacture nano-scale patterning of polymers. However, this would also invalidate the largest advantage of using screen printing: the simple and low-cost manufacturability with few process steps when etching needs removal of material. On the other hand, if the reliability and reproducibility of the attachment would increase using etched substrates, the advantages of etching would be more than the disadvantages. Manufacturing large amounts of devices, yield and reliability have very large effects.

6. CONCLUSIONS

The main goal of the thesis was to determine the bending reliability of a silicon chip which is attached on rotary screen printed circuitry. This included the finding of a suitable bending test method, building the test set-up and fabricating the test samples. Before preparing the test samples, suitable bonding parameters had to be determined.

Test samples were bonded using a flip-chip technique and anisotropic conductive adhesives. The idea of using a bare die without any interposer or package is that the attachment would be more bendable when it is smaller. Two different ACAs were used: film with 5 μm particles and paste with 2.5 μm particles. The optimization of the bonding process and finding suitable parameters were challenging due to the roughness and height variations of printed lines. However, working contacts were possible to produce through low-temperature processing. Approximately 90 % of the ACP bonded and 96 % of the ACF bonded interconnections worked. Stud bumping of the chips increased the yield almost to 100 % and decreased contact resistances. Without bumps, half of the measured contact resistances were between 40 - 100 Ω. When stud bumps were used, the same numbers were 19 – 21 Ω. However, the conducting mechanism seems to be direct meaning that the screen printed wires are in a direct contact with bumps or chip pads without the help of conductive particles. That does not indicate reliable contacts. Calendering was performed to the printed lines which reduced the surface roughness making the surfaces smoother. However, 2 μm variations on the line heights were observed after calendering.

The bending test set-up worked well for its purpose of use. All of the tested samples survived at least a 2.5 cm of bending radius. Stud bumps or the 0.53 mm difference in the chip size did not seem to have any significant effect on the minimum bending radius with the used measurement accuracy. Attachments were bendable in a way that they can survive one bending cycle. The long-term bending reliability of the attachments still needs to be solved. In addition, the reliability of the attachments needs to be studied using environmental stress tests.

According to the results of this thesis, bonding of the chips on screen printed circuitry was proven to be possible despite of the height variations of the printed pads. However, further development and adhesive optimizations are needed to achieve higher reliability. In addition, the attachments were proven to be bendable. If hybrid electronics are becoming common and they are placed also on curved surfaces, studies about the bendability of different components of the hybrid devices are needed. This thesis provides a firm starting point for further development.

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APPENDIX A: MATLAB-CODE FOR PRESENTING THE SECTOR RESISTANCES AS A FUNCTION OF BENDING RADIUS

```
%Made by Lydia Leppänen, last change: 31.3.2016

%This template is for the bending tests. It draws the measured
%resistances as a function of the bending radius.

%You need to add the result matrix from the text-file which the
%Labview-program created. The matrix must have . as a decimal
%separator and inf when the resistance is infinitive (= replace NaN).
%In addition, the used speed and starting distance of the plates need
%to be added.

%add the result matrix from text-file between the square brackets:
A = [
    ];

%add the used speed in mm/min:
speedmin = ;

%add the starting point (mm):
startvalue = ;

%-----------------CODE-------------------------------------------------

%calculating the time and resistance vectors:

time = A(:,1);
first = A(:,3);
second = A(:,4);
third = A(:,5);
fourth = A(:,6);
fifth = A(:,7);
sixth = A(:,8);
seventh = A(:,9);
eight = A(:,10);

%solving the radius-vector which matches with the resistance vectors:

l = length (time);
onevector = ones (l, 1);
start = startvalue*ones;
speed = speedmin/60;
distance = start - speed*time;
radius = distance/2;

%drawing the resistances as a function of bending radius:

plot (radius, first);
set(gca,'XDir','reverse');
hold on;
plot (radius, second);
hold on;
plot (radius, third);
hold on;
plot (radius, fourth);
```

```
hold on;
plot (radius, fifth);
hold on;
plot (radius, sixth);
hold on;
plot (radius, seventh);
hold on;
plot (radius, eight);
hold on;

legend('1st','2nd', '3rd', '4th', '5th', '6th', '7th', '8th');
xlabel('bending radius (mm)');
ylabel('resistance (ohms)');
```

APPENDIX B: RESULTS FROM THE BENDING TESTS

Table 7. *The table shows minimum bending radii for each sector (mm) and the minimum bending radius of the whole sample (min r.) which is the bending radius when the first contact of the sample has broken. When there is a text "broken" the channel was broken already before the bending test. Line shows that the sector survived for the whole bending test without breaking.*

sample	pitch (µm)	bump	sector 1	sector 2	sector 3	sector 4	sector 5	sector 6	sector 7	sector 8	min. r
1	150	gold	13,0	20,0	20,0	13,5	16,5	24,5	24,5	16,5	24,5
2	150	gold	12,0	broken	16,0	12,0	14,5	20,0	18,0	14,5	18,0
3	150	gold	13,5	13,0	13,0	12,5	12,5	20,5	20,5	12,5	20,5
4	150	gold	14,0	16,0	16,0	14,0	14,5	19,5	18,5	14,5	19,5
5	150	gold	broken	21,5	21,5	broken	17,5	23,5	23,5	broken	23,5
6	150	gold	13,5	-	-	13,5	14,5	14,5	14,5	14,5	14,5
7	150	gold	12,0	13,5	13,5	12,0	13,5	15,5	15,5	13,5	15,5
8	150	gold	13,5	14,5	14,5	13,5	11,0	16,0	16,0	11,0	16,0
9	150	gold	14,0	-	-	14,0	14,5	14,5	14,5	14,5	14,5
10	150	gold	14,5	15,5	15,5	15,4	14,5	-	-	14,5	15,5
11	150	no	broken	broken	25,0	12,0	12,0	18,0	18,0	12,0	25,0
12	175	gold	14,0	16,0	16,0	14,0	14,0	16,0	16,0	14,0	16,0
13	175	gold	15,0	14,5	14,5	15,0	15,0	19,0	19,0	15,0	19,0
14	175	gold	14,0	16,5	16,5	14,0	15,0	16,5	15,5	14,0	16,5
15	175	gold	14,0	-	-	14,0	14,0	15,0	15,0	14,0	15,0
16	175	gold	broken	14,5	14,5	14,0	14,0	broken	18,5	14,0	18,5
17	175	gold	12,5	broken	broken	broken	broken	15,5	15,5	12,5	15,5
18	175	gold	12,5	16,5	16,5	12,5	12,5	15,0	15,5	12,5	16,5
19	175	gold	broken	16,0	16,0	14,5	16,0	20,0	20,0	broken	20,0
20	175	gold	broken	broken	broken	broken	broken	16,0	16,0	broken	16,0
21	175	gold	13,0	15,0	15,0	13,5	13,5	16,5	16,5	13,5	16,5
22	175	gold	15,0	15,0	15,0	15,0	13,5	-	-	13,5	15,0
23	175	no	15,5	20,0	20,0	15,0	15,0	19,0	19,0	15,0	20,0
24	175	no	broken	broken	16,5	broken	11,0	15,5	15,5	11,0	16,5
25	175	no	broken	16,5	broken	broken	broken	broken	broken	11,0	16,5
26	175	no	broken	17,5	17,5	15,0	15,0	broken	broken	14,0	17,5
27	175	no	11,5	12,0	13,0	11,5	22,5	17,0	17,0	11,5	22,5

APPENDIX C: MATLAB-CODE FOR REMOVING THE OFFSET-LEVEL IN PROFILOMETER FIGURES

```
%Made by Lydia Leppänen, 3.3.2016

%This code is for profilometer analysis to put the surface of the PET-
%foil to on zero-level in the figures from Vision-program.

%add the offset value:
offset = ;

%add the 2D-data matrix:
A =[
    ];

number = numel (A)/2;
Xaxis = A(:,1);
Yapu = A(:,2);

x = 1;

while x < number + 1
    Yaxis(x) = offset*(-1) + Yapu(x);
    x = x + 1;
end;

plot (Xaxis, Yaxis);

xlabel('mm');
ylabel('height (um)');
```