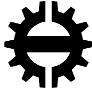

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TAMPERE UNIVERSITY OF TECHNOLOGY

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SiC MOSFET UPGRADE OF A POWER CONVERTER

Master of Science thesis

Examiner: prof. Karri Palovuori
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ABSTRACT

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Power semiconductor devices are at the heart of modern power electronics due to their ability to control large amounts of power with relatively low power dissipation. This feature of the semiconductor switches results in efficient power systems. Today the power semiconductor devices are dominated by silicon (Si) technology. However, Si semiconductor switches are approaching their material limitations in terms of blocking voltage, operation temperature, and conduction and switching characteristics. Wide band gap semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN), promise to revolutionize next generation power electronics with their superior material properties. This thesis studies the effects of upgrading a power converter that is designed with Si insulated-gate bipolar transistors (IGBT) with novel SiC metal-oxide-semiconductor field-effect transistors (MOSFET) and if the upgrade is achievable with minor changes on the original power converter. The upgrade is executed for the three-phase active rectifier section of the power converter that also includes power factor correction.

The switching waveforms of the semiconductor switches are compared and analysed, and the effects of the upgrade on the efficiency of the power converter is examined. Also the possibility of increasing the switching frequency of the upgraded section and its effects on converter efficiency is studied. The measurements in this thesis work include reference measurements that were performed with the original power converter and comparison measurements with the upgraded power converter. Switching waveforms were measured at the rated switching frequency of 40 kHz. Efficiency measurements of the upgraded converter were performed at 40 kHz, 80 kHz, and 120 kHz switching frequencies. Efficiency of the entire power converter was measured in forward and in reverse operation modes at different loading conditions. Also the efficiency of the upgraded section of the power converter was measured separately in forward operation.

The measurements in this thesis work show promising results that a power converter designed with Si IGBTs can be upgraded with SiC MOSFETs with somewhat small changes on the original design and with moderate workload. The measurements also show that the upgrade is beneficial even at higher switching frequencies. However, more testing, designing, and optimizing is required before the upgraded power converter could be ready for use. It must be considered, if the higher cost of the new switching components and the work hours needed to achieve the complete upgraded power converter are worth the gained efficiency improvements.

TIIVISTELMÄ

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Puolijohdekytkimet ovat modernin tehoelektroniikan keskiössä, sillä ne pystyvät käsittelemään suuria tehomääriä suhteellisen pienillä häviöillä. Tämä ominaisuus mahdollistaa tehoelektroniikan laitteiden toteuttamisen hyvällä hyötysuhteella. Puolijohdekomponenttien materiaalina on pääosin käytetty piitä, jonka valmistustekniikkaa on kehitetty pitkään ja ominaisuudet tunnetaan hyvin. Pii-pohjaiset puolijohdekytkimet lähestyvät kuitenkin materiaalin rajoituksia estosuuntaisen jännitteen, toimintalämpötilan sekä johtavuus- ja kytkentäominaisuuksien osalta. Suuren energia-aukon puolijohdemateriaalit, kuten piikarbidi ja galliumnitridi, voivat erinomaisilla materiaaliominaisuuksillaan mahdollistaa seuraavan sukupolven tehoelektroniikan kehityksen. Tässä diplomityössä tutkitaan mahdollisuutta päivittää pii-puolijohdekytkimillä (Si IGBT) suunniteltu tehomuunnin piikarbidi-puolijohdekytkimillä (SiC MOSFET) mahdollisimman pienillä muutoksilla alkuperäisen tehomuuntimen toteutukseen. Päivitys suoritetaan tehomuuntimen kolmivaiheiseen aktiiviseen tasasuuntaajaan, joka sisältää tehokertoimen korjauksen.

Työssä vertaillaan ja analysoidaan puolijohdekytkimien aaltomuotoja kytkentätilanteissa sekä tutkitaan päivityksen vaikutuksia tehomuuntimen hyötysuhteeseen. Työssä tutkitaan myös mahdollisuutta nostaa päivitetyn osion kytkentätaajuutta ja suuremman kytkentätaajuuden vaikutusta hyötysuhteeseen. Mittaukset koostuvat alkuperäisellä tehomuuntimella suoritetuista referenssimittauksista sekä vertailumittauksista päivitetyllä tehomuuntimella. Kytkentätilanteiden aaltomuodot on mitattu tehomuuntimen nimellistaajuudella 40 kHz. Päivitetyn tehomuuntimen hyötysuhdemittaukset on suoritettu 40 kHz:in, 80 kHz:in sekä 120 kHz:in kytkentätaajuuksilla. Tehomuuntimen kokonaishyötysuhde mitattiin myötä- ja vastakkaissuuntaisessa toimintatilassa eri kuorma-arvoilla. Myös pelkän päivitetyn osion hyötysuhde myötäsuuntaisessa toimintatilassa mitattiin erillään koko tehomuuntimen hyötysuhteesta.

Diplomityön tulokset ovat lupaavia ja osoittavat, että Si IGBT:illä suunniteltu tehomuunnin voidaan päivittää SiC MOSFET:eillä melko pienillä muutoksilla alkuperäisen tehomuuntimen toteutukseen sekä kohtuullisella työmäärällä. Mittaukset osoittavat, että päivitys parantaa hyötysuhdetta jopa suuremmilla kytkentätaajuuksilla. Kuitenkin tarvitaan lisää testausta, suunnittelua ja optimointia ennen kuin päivitetty tehomuunnin on valmis tuotantoon ja käyttöön. Sovelluskohtaisesti täytyy harkita, onko uusien kytkinkomponenttien suurempi hinta ja päivitykseen vaadittavat työtunnit niillä saavutettavan hyötysuhteen kasvun arvoisia.

PREFACE

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LIST OF SYMBOLS AND ABBREVIATIONS

A_{core}	transformer core area
A_{Cu}	transformer winding area
A_p	transformer area product
BJT	bipolar junction transistor
B_{pk}	peak flux density
C	collector terminal
$C_{dc\text{-}link}$	dc-link storage capacitor
C_{ds}	drain-source capacitance
C_f	diode junction capacitance
C_{gd}	gate-drain capacitance
C_{gs}	gate-source capacitance
C_{iss}	input capacitance of a semiconductor switch
C_{JD}	drain junction depletion capacitance
C_{JS}	source junction depletion capacitance
C_{OD}	gate-drain overlap capacitance
C_{OS}	gate-source overlap capacitance
C_{oss}	output capacitance of a semiconductor switch
C_{oss1}	output capacitance of the upper switch
C_{oss2}	output capacitance of the lower switch
C_{rss}	reverse transfer capacitance of a semiconductor switch
D	drain terminal
di/dt	current slew rate
D_n	electron diffusion constant
D_N	negative side diode
D_p	hole diffusion constant
D_P	positive side diode
dv/dt	voltage slew rate
E	emitter terminal
E_{crit}	critical electric field
E_g	bandgap energy
$E_{loss,rr}$	reverse recovery energy loss
EMI	electromagnetic interference
E_{off}	MOSFET turn-off energy loss
E_{on}	MOSFET turn-on energy loss
E_{rec}	reverse recovery energy
E_t	defect state energy
FET	field effect transistor
FWD	freewheeling diode
G	gate terminal
GaN	gallium nitride
g_m	transconductance
i_{ac}	alternating current
I_C	collector current
I_D	drain current
i_D	diode current
i_{dc}	dc-link current
I_{dc}	dc-level of inductor current
i_{DP}	positive side diode current

IGBT	insulated gate bipolar transistor
I_l	load current
i_L	inductor current
I_O	output current
i_{ph}	phase current
I_{pk}	inductor peak current
I_{rr}	reverse recovery current
I_S	maximum continuous forward current rating
i_S	switch current
i_{SN}	negative side transistor current
$i_s(t)$	system current
i_T	transistor current
I_1	transformer primary side current
I_2	transformer secondary side current
ΔI	inductor ripple current
j	current density
JFET	junction field-effect transistor
J_s	*pn*-junction leakage current
K_u	copper fill factor
L_{ac}	AC-side inductor
L_D	drain inductance
L_{dc}	DC bus inductance
L_{dcr}	DC bus return inductance
L_f	freewheeling diode parasitic inductance
L_G	gate inductance
L_n	electron diffusion length
L_P	power loop inductance
L_p	hole diffusion length
L_S	source inductance, common mode inductance
m_n	effective electron mass
m_p	effective hole mass
MESFET	metal-semiconductor field-effect transistor
MISFET	metal-insulator-semiconductor field-effect transistor
MOSFET	metal-oxide-semiconductor field-effect transistor
n_i	intrinsic carrier density
n_n	electron density
n_p	hole density
N_1	primary winding turns
N_2	secondary winding turns
P_{core}	transformer core loss
P_{Cu}	transformer copper loss
PF	power factor
PFC	power factor correction
P_{in}	input power
$p_{in}(t)$	instantaneous input power
P_{loss}	power loss
$P_{loss,buck}$	power loss of buck dc-dc section of a power converter
$P_{loss,PFC}$	power loss of PFC rectifier section of a power converter
$P_{loss,tot}$	total power loss of a power converter
$P_{on,MOSFET}$	MOSFET on-state loss

P_{out}	output power
PV	photovoltaic
PWM	pulse width modulation
r	current ripple ratio
R_{BD}	body-drain resistance
R_{BS}	body-source resistance
R_D	drain resistance
$R_{DS(on)}$	drain-source on-state resistance
R_f	freewheeling diode resistance
R_g	gate resistance
$R_{g,off}$	negative gate supply resistance
$R_{g,on}$	positive gate supply resistance
R_S	source resistance
R_1	primary side copper wire resistance
R_2	secondary side copper wire resistance
S	source terminal
Si	silicon
SiC	silicon carbide
SiO_2	silicon oxide
S_N	negative side transistor
S_P	positive side transistor
S_1	upper switch
S_2	lower switch
T	temperature
t_c	crossover time
$t_{d(off)}$	turn-off delay time
$t_{d(on)}$	turn-on delay time
t_{fi}	MOSFET current fall time
t_{fi1}	IGBT first current fall time
t_{fi2}	IGBT second current fall time
t_{fv1}	first drain-source or collector-emitter voltage fall time
t_{fv2}	second drain-source or collector-emitter voltage fall time
T_j	junction temperature
t_{ri}	current rise time
t_{rr}	reverse recovery time
t_{rv}	IGBT voltage rise time
t_{rv1}	MOSFET first voltage rise time
t_{rv2}	MOSFET second voltage rise time
UVLO	undervoltage lockout
V_{acc}	IGBT accumulation voltage
V_{CE}	collector-emitter voltage
$V_{CE(on)}$	collector-emitter on-state voltage
V_{ch}	IGBT channel resistance
V_{core}	transformer core volume
V_D	drain voltage
V_{dc}	source voltage
$V_{dc\text{-}link}$	dc-link voltage
V_{drift}	IGBT drift layer voltage
V_{drop}	drain-source voltage drop during current rise period
V_{DS}	drain-source voltage

$V_{DS(on)}$	drain-source on-state voltage
V_{FWD}	freewheeling diode on-stage voltage drop
V_G	gate voltage
V_{GE}	gate-emitter voltage
V_{GG}	gate supply voltage
V_{GS}	gate-source voltage
$V_{GS,IO}$	Miller plateau voltage
V_{LP}	induced voltage in power loop inductance
V_{LS}	induced voltage in common mode stray inductance
V_{MOD}	fundamental voltage of the pulse width modulation pattern
V_{MOSFET}	voltage of the MOSFET section of an IGBT
V_{p+n}	IGBT collector junction voltage
V_{ref}	reference voltage
V_{SD}	diode forward voltage rating
$v_s(t)$	system input voltage
v_{sat}	saturated electron drift velocity
V_{th}	threshold voltage
$V_{transistor}$	voltage of the FET section of an IGBT
V_1	primary side voltage
Q_f	fixed oxide density
Q_g	total gate charge
Q_{gc}	gate-collector charge
Q_{gd}	gate-drain charge
Q_{ge}	gate-emitter charge
Q_{gs}	gate-source charge
Q_{tot}	total additional charge
h	Boltzman’s constant
k	Planck’s constant
η	electrical system efficiency
σ	drift region conductivity
λ	thermal conductivity
τ	channel transition time
ε_S	semiconductor permittivity
μ_n	electron mobility
μ_p	hole mobility
Ψ_B	surface potential
ϕ_{ms}	metal-semiconductor work function

1. INTRODUCTION

Power semiconductor devices are at the heart of modern power electronics. History of power electronics is much connected to the development of switching devices and the field has grown in parallel with the growth of the power semiconductor device technology. The need to utilize semiconductor switches in power electronic applications is their ability to control large amounts of power from the input to the output with a relatively low power dissipation, hence resulting in an efficient power system. Efficiency is considered as an important figure of merit. Low efficiency implies large amounts of power being dissipated in a form of heat, which reduces component reliability, increases the cost of energy due to increased consumption, and requires additional components, such as heat sinks, resulting in low power density. The improvements in semiconductor processing technology along with manufacturing and packaging techniques has allowed power semiconductor development for high voltage and high current ratings and fast turn-on and turn-off characteristics. Also, the availability of devices with different characteristics and ratings makes it possible to cover many power electronics applications. [42]

Today the power semiconductor devices are dominated by the well-established *silicon* (Si) technology that has gone through several generations of development in the last 50 years. However, Si power semiconductor devices are approaching their material limitations in terms of blocking voltage, operation temperature, and conduction and switching characteristics. These physical limits of the silicon technology have become a barrier to achieve higher performance of power conversion. Wide band gap semiconductor devices promise to revolutionize next generation power electronics converters with their high breakdown electric field, low on-resistance, fast switching speed, and high junction temperature capability. *Silicon carbide* (SiC) and *gallium nitride* (GaN) devices are wide band gap devices that are under rapid development. [23]

This thesis studies the effects of upgrading a power converter that is designed with Si *insulated-gate bipolar transistors* (IGBT) with novel SiC *metal-oxide-semiconductor field-effect transistors* (MOSFET). The switching waveforms of the semiconductor switches are analysed and the effects of the upgrade on the efficiency of the power converter is examined. It is studied, if the upgrade is achievable with minor changes on the original power converter and if the switching frequency of the upgraded section can be increased. The structure and operation, switching characteristics, and typical power losses of the switching components are presented in Chapter 2.1 for the MOSFET and in Chapter 2.2 for the IGBT. The differences between silicon and silicon carbide technologies and the challenges of SiC devices are introduced in Chapter 2.3. Chapter 3

addresses the non-ideal effects of SiC MOSFETs. The operating principle and different sections of the power converter that is studied in this thesis are presented in Chapter 4. The process of selecting the new switching components and comparison of the semiconductor switches are presented in Chapter 5. Results and analysis are presented in Chapter 6: Chapter 6.1 focuses on the measurement setups, 6.2 on the results from the measurements of the switching waveforms, 6.3 on the results from the efficiency measurements, and 6.4 on the analysis of the results from the measurements. Conclusions of this thesis work are presented in Chapter 7.

2. SEMICONDUCTOR SWITCHES

The advancements in semiconductor technology and in power semiconductor devices have led to the growth of the power electronics field [42] and enabled the growth of power electronics technology toward higher efficiency, higher power density and more integrated systems [48]. Semiconductor *pn*-junctions have two dominant features: injection of minority carriers with forward bias and a variation of depletion width with reverse bias. These *pn*-junction properties are used in *bipolar junction transistors* (BJT) and in *field-effect transistors* (FET) that are two important types of transistors in switching applications. [49]

Semiconductor transistors are used in power electronics as power switches to enable electrical power conversion from the source to the load. Ideally, a power switch operates either fully on or fully off, which minimizes the power loss of the transistor. [36] Electrical power conversion from the source to the load can also be performed without switching devices, with transistors that operate in their linear region. However, in these linear applications a large amount of energy is lost within the circuit before the processed energy reaches the output. Semiconductor switches are needed in power electronic circuits due to their ability to control and manipulate very large amounts of power with relatively low power dissipation. [42]

Improvements in semiconductor processing technologies along with manufacturing and packaging techniques has allowed the development of semiconductor switches for high voltage and high current ratings as well as fast turn-on and turn-off characteristics. Nowadays the availability of different switching devices with varying switching speeds, power handling capabilities and cost make it possible for semiconductor switches to cover many power electronics applications. [42] There are several forms of the BJTs and the FETs depending on the device structure. BJTs, especially the *insulated gate bipolar transistor* (IGBT), are discussed in Chapter 2.2. FETs are discussed in Chapter 2.1, focusing on the structure and operation of the *metal-oxide-semiconductor field-effect transistor* (MOSFET).

The advancements in semiconductor technology has been primarily driven by silicon (Si) power devices. However, Si switches are approaching their performance limits. In recent years semiconductor switches based on wide bandgap materials, such as silicon carbide (SiC) and gallium nitride (GaN), has been introduced to overcome the limitations of Si power devices. [48] SiC technology and material properties are discussed in Chapter 2.3.

2.1 Metal-Oxide-Semiconductor Field-Effect Transistor

Field-effect transistors are unipolar devices in which only one type of charge carriers, electrons or protons, participate in the conduction process [50]. Because of this, they are called *majority carrier devices*. In an *n*-type material, where there is a relatively large number of conduction band electrons due to semiconductor doping, electrons are majority charge carriers and holes are *minority carriers*. On the contrary, in a *p*-type material holes are majority carriers and electrons are minority carriers. [49]

FETs are voltage-controlled devices. They are well suited for controlled switching between a conducting state and a non-conducting state. There are several different forms of the FET. In a *junction FET* (JFET), the control voltage of the semiconductor switch varies the depletion width of a reverse-biased *pn*-junction. In a *metal-semiconductor FET* (MESFET) the *pn*-junction is replaced by a metal contact called the Schottky barrier. The control terminal can also be separated from the semiconductor by an insulator as in a *metal-insulator-semiconductor FET* (MISFET). Special case of the MISFET is the *metal-oxide-semiconductor FET* (MOSFET) that uses an oxide layer as the insulator. [49] This chapter focuses to study the structure and operation of the MOSFET (Chapter 2.1.1) as well as its switching characteristics (Chapter 2.1.2) and power losses (Chapter 2.1.3).

2.1.1 Structure and operation

The MOSFET has four terminals: gate (*G*), drain (*D*), source (*S*) and body [50]. The body of the MOSFET is often connected to the source terminal, making it a three-terminal device. The gate terminal is isolated from the device substrate by an insulator. The substrate and the insulator forms a high-quality capacitor. [36] Most MOSFETs are made of silicon for the semiconductor, oxides like silicon oxide (SiO_2) for the insulator and metal for gate terminal [49]. The MOSFET has a metal-oxide-semiconductor structure as shown in Figure 1.

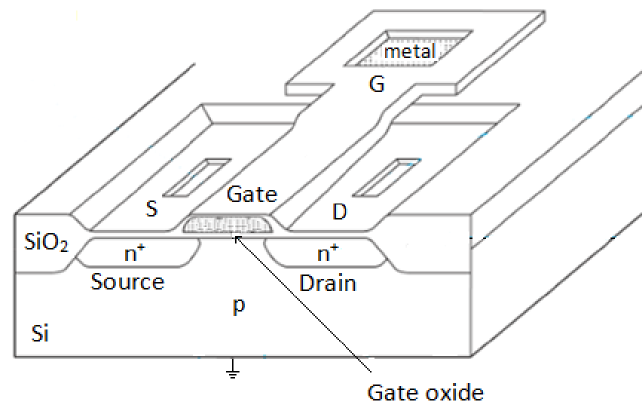

Figure 1. *Cross-section of an n-type MOSFET. Gate metal is isolated from the semiconductor substrate by an isolating oxide layer. Adapted from [49].*

The MOSFET shown in Figure 1 is an *n*-channel device that is formed on a *p*-type silicon substrate. Electron mobility in silicon is larger than the mobility of holes and therefore the *n*-channel type is commonly preferred in devices with Si substrate. When no voltage is applied to the gate terminal, there is a potential barrier for an electron to travel from the source terminal to the drain terminal. This potential barrier corresponds to the built-in potential of the *pn*-junctions in the substrate. [49]

When a positive voltage is applied to the gate, positive charges are deposited on the gate metal. The positive charge on the gate terminal causes positive charges in the substrate move further away from the gate. In response, the positive gate charge attracts electrons from the underlying substrate and a thin surface region containing mobile electrons is formed below the gate oxide. A *depletion region* is formed in the substrate for the area where all free charge carriers have been diffused away. [49] The induced electrons under the gate terminal form an *n*-channel, which connects the source and the drain terminals and allows current to flow between them [50]. If the potential barrier between the source and the drain is reduced sufficiently by applying a gate voltage more than what is known as the *threshold voltage* (V_{th}), there is a significant current flow from the source to the drain. V_{th} is the minimum gate voltage (V_G) value required to build up the conducting channel. [49] The conductivity of the channel can be adjusted by varying the gate voltage as Figure 2 illustrates [50].

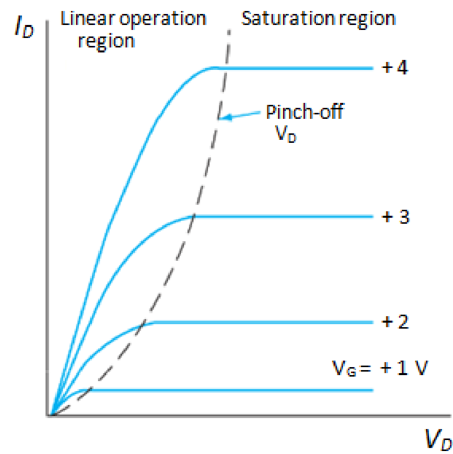

Figure 2. *Current-voltage characteristics of a MOSFET drain as a function of gate voltage. Adapted from [49].*

In the *linear operation region* of the MOSFET, drain current (I_D) is proportional to drain voltage (V_D). The conducting channel acts as a resistance, thus I_D increases linearly with increasing V_D, as shown in Figure 2. As V_D increases, it reaches a point at which the width of the channel is reduced to zero. This is called the *pinch-off point*. [50] The number of charge carriers arriving at the pinch-off point, hence the current flowing from drain to source, remains constant. After the pinch-off point, I_D does not increase significantly with increasing drain voltage and the device is operating in *saturation region*. [49] Figure 3 (b) shows the MOSFET cross-section during the formation of pinch-off.

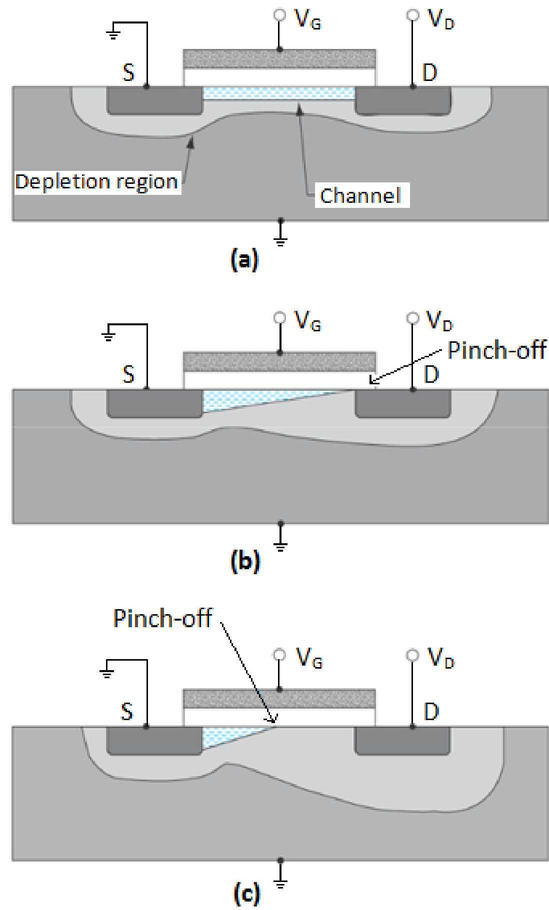

Figure 3. *MOSFET cross-section in (a) linear region, (b) onset of saturation at pinch-off and (c) strong saturation. Adapted from [49].*

The voltage difference between the gate and the channel reduces from the gate voltage value near the source terminal to $V_G - V_D$ near the drain end. Once the drain current is increased to the point where $V_G - V_D = V_{th}$, the channel is pinched off and threshold is maintained near the drain end. [49] As can be seen from Figure 3 (c), increasing V_D causes the point at which the channel gets pinched off to move closer to the source end.

The MOSFET structure includes several parasitic capacitive and resistive components. These equivalent components of the MOSFET are illustrated in Figure 4.

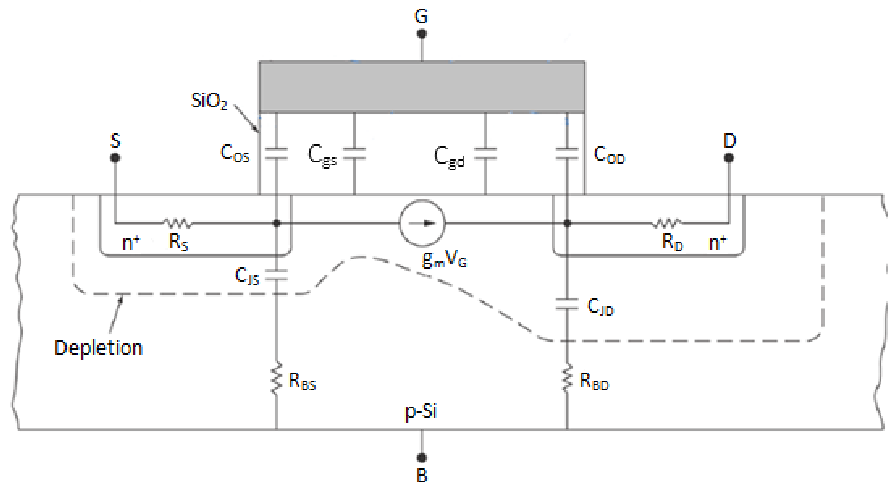

Figure 4. *Parasitic capacitive and resistive components presented in the MOSFET cross-section. Adapted from [49].*

In the MOSFET cross-section shown in Figure 4, the four capacitances below the gate terminal represent the *input capacitance* (C_{iss}). C_{iss} is the sum of the parasitic capacitances from gate to source (C_{gs}) and from gate to drain (C_{gd}). [49] Gate capacitances C_{gs} and C_{gd} vary with the voltage across them, since part of their capacitance is contributed by the voltage dependent depletion layer [22]. Overlap capacitances from gate to source (C_{OS}) and from gate to drain (C_{OD}) are results of gate electrode overlapping to the source and drain junctions. C_{OD} is also known as the *Miller overlap capacitance* [49]. The Miller capacitance develops an undesirable feedback path between the input and the output of the MOSFET [50]. The MOSFET structure also has *pn*-junction depletion capacitances associated with the source (C_{JS}) and the drain (C_{JD}). [49]

Resistances R_S and R_D demonstrate the parasitic source and drain resistances, respectively. The resistances between the substrate and the drain and the source regions are illustrated as R_{BD} and R_{BS}, respectively. The drain current can be modelled as a voltage-controlled current source $I = g_m V_G$, where g_m is the transconductance of the device. [49] The MOSFET structure includes several parasitic components that lead to non-ideal operation of the MOSFET. Also, the component packaging and layout can produce parasitic effects. These parasitic components and their effects on the operation of the MOSFET are discussed in chapters 3.1 *SiC MOSFET parasitic components* and 3.2 *Switching oscillation*.

A power MOSFET is a semiconductor device that is comprised of several MOSFET cells connected in parallel on the surface of a silicon die [22]. A cross-section of one power MOSFET cell is illustrated in Figure 5 (a).

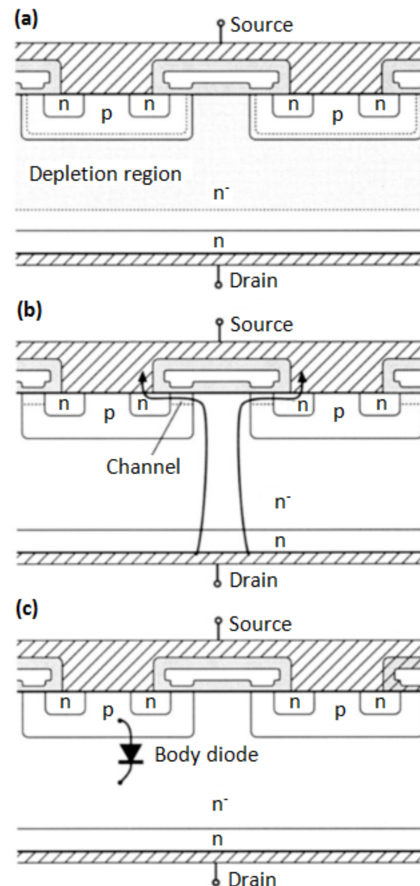

Figure 5. *Power MOSFET cross-section showing (a) off-state, (b) on-state and (c) the body diode. Adapted from [22].*

In a power MOSFET, current flows vertically through the device. The drain connection is in the bottom of the silicon die while the source connection and the gate terminal are on the top surface. The n^--region is often called the drift region. When the power switch is off and the voltage between the drain and the source terminals (V_{DS}) is $V_{DS} \geq 0$, *pn*- and pn^--junctions shown in Figure 5 (a) are reverse-biased and no current flows through the device. With a gate-source voltage (V_{GS}) larger than the threshold voltage of the device, a conducting channel forms at the surface of the *p*-region, as shown in Figure 5 (b). Drain current flows through the drain contact, the *n*-substrate, the n^- drift region, the conducting channel, the *n*-region, and through the source contact. The on-resistance of the device is the sum of the resistances in the conducting channel, source and drain contacts, and in all the semiconductor regions. MOSFET losses are discussed in Chapter 2.1.3. [22]

The pn^--junction of the power MOSFET forms an effective diode called the *body diode* in parallel with the MOSFET channel, as illustrated in Figure 5 (c) [22]. During the device switching from on-state to off-state, the body diode produces *reverse recovery current* (I_{rr}). I_{rr} is due to high concentrations of injected carriers that are stored in the drift region during conduction. [32] As the device switches from on-state to off-state, the diode charge distribution must change [27]. The injected carriers are swept away from the drift region,

which results in reverse current [32]. In some cases, such as a SiC diode, the charge distribution difference is caused by the device junction capacitance rather than by injected charge carriers [27]. I_{rr} leads to additional power loss during the switching process. However, the body diode of the MOSFET can be utilized to conduct reverse currents in inductive hard switching, when external anti-parallel diodes are avoided. [32]

2.1.2 Switching characteristics

The switching characteristics of a power MOSFET are investigated with a simple circuit shown in Figure 6.

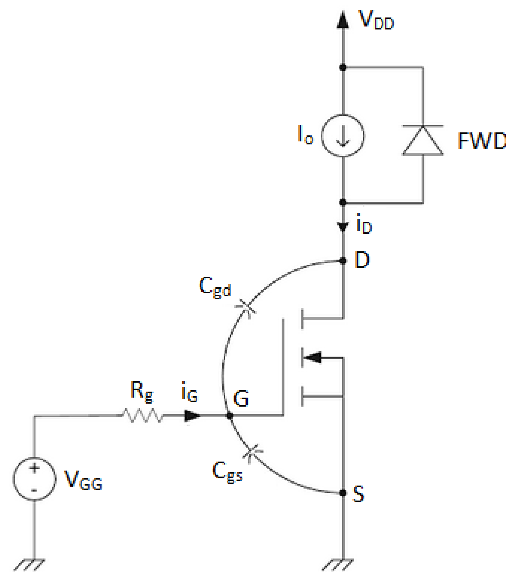

Figure 6. *Simplified equivalent circuit used to examine the switching behavior of MOSFET. Adapted from [42].*

Load inductance is assumed to be very large, so the current through it can be modelled with a constant current source that equals the output current (I_O). The MOSFET equivalent model includes parasitic capacitances C_{gs} and C_{gd} and parasitic gate resistance (R_g). Other non-idealities, that the MOSFET and the diode might have, are ignored in this model. *Freewheeling diode* (FWD) conducts the load current while the MOSFET is in off-state. [42]

The turn-on process of the MOSFET begins as gate voltage steps from zero to gate supply voltage (V_{GG}). The turn-on waveforms of the power MOSFET are shown in Figure 7.

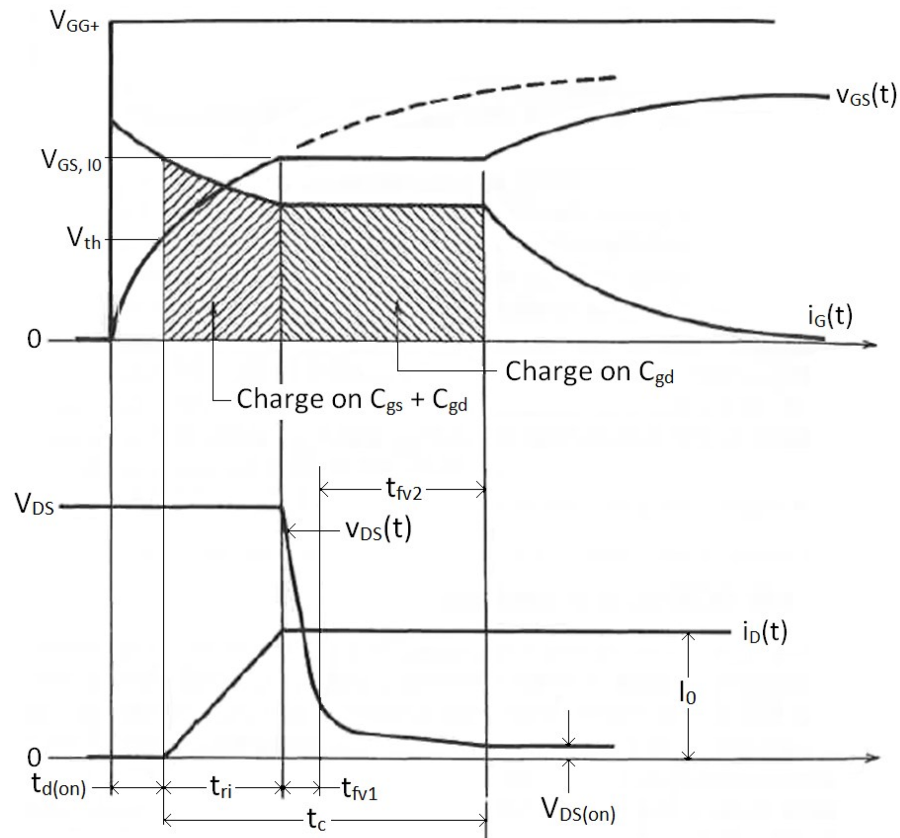

Figure 7. *MOSFET turn-on voltage and current waveforms. Adapted from [36].*

The turn-on process can be divided into three time intervals: turn-on delay time ($t_{d(on)}$), current rise time (t_{ri}) and drain-source voltage fall time (t_{fv1}, t_{fv2}). During the turn-on delay time, the gate current flows through the gate resistor and charges the parasitic capacitances C_{gs} and C_{gd}. Gate-source voltage increases from zero to threshold voltage. [36]

As V_{GS} reaches V_{th} at the beginning of the current rise period, the conducting channel is formed under the gate terminal of the MOSFET. Drain current begins to increase linearly from zero and the MOSFET operates in linear region. The gate-source voltage continues to rise. [36] As long as I_D remains less than I_O, the freewheeling diode conducts current and V_{DS} equals its off-state value [42].

V_{DS} fall time can be divided into two time intervals: t_{fv1} and t_{fv2}. During the first interval t_{fv1}, the MOSFET is carrying full load current, but still operates in the linear region. V_{GS} becomes clamped at $V_{GS,IO}$, which is also known as *Miller plateau voltage*. This is the V_{GS} value that is required to maintain $I_D = I_O$. The first time interval of V_{DS} fall time corresponds to the passing of the linear region and the second time interval corresponds to the completion of the transient to the saturation region. [36]

As V_{DS} has completed its drop to the on-state value ($V_{DS(on)}$), V_{GS} becomes unclamped and continues to grow towards V_{GG}. Gate current decays towards zero with the same time

constant that V_{GS} grows. [36] $V_{DS(on)}$ value is determined by the on-state resistance ($R_{DS(on)}$) according to $V_{DS(on)} = R_{DS(on)} I_O$. $R_{DS(on)}$ results from the resistivity of the channel and from the MOSFET structure. [42]

The turn-off process of the MOSFET involves the same events that occurred during the turn-on process, but in reverse sequence. MOSFET turn-off waveforms are presented in Figure 8.

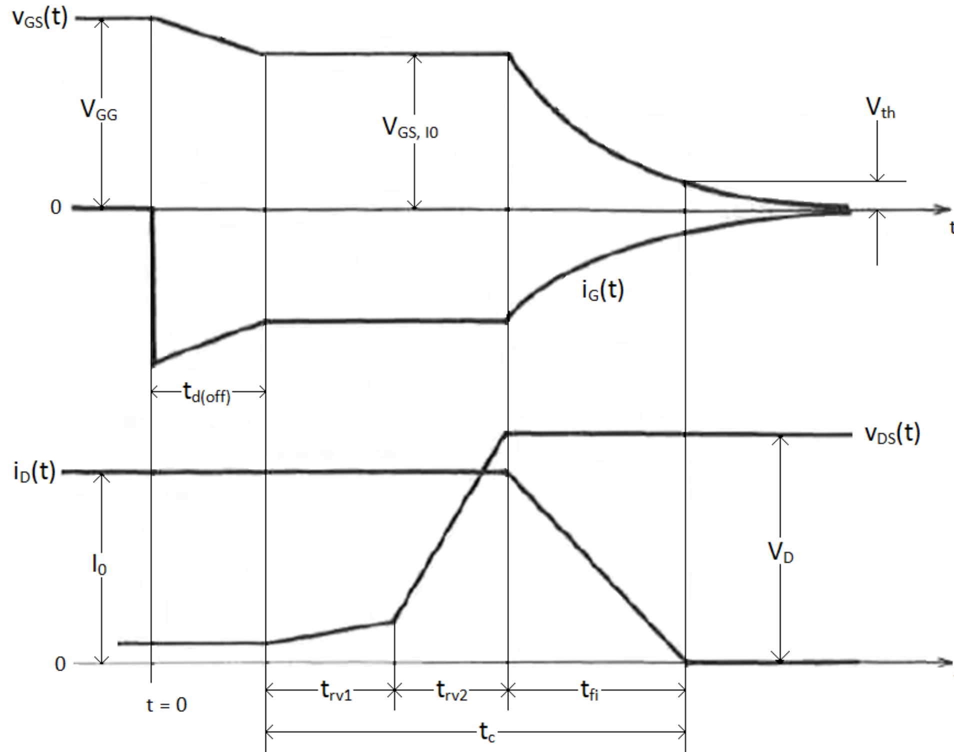

***Figure 8.** MOSFET turn-off voltage and current waveforms. Adapted from [36].*

Similar to turn-on, the turn-off process can be divided into three time intervals: turn-off delay ($t_{d(off)}$), voltage rise time (t_{rv1}, t_{rv2}) and current fall time (t_{fi}). The turn-off process begins as the gate drive voltage steps down from V_{GG} to zero. During $t_{d(off)}$ the parasitic capacitances C_{gs} and C_{gd} begin to discharge through the gate resistance and V_{GS} declines towards $V_{GS,IO}$. [36]

Voltage rise period begins as V_{GS} reaches the Miller plateau voltage. Voltage rise can be divided into two intervals (t_{rv1}, t_{rv2}), during which the MOSFET enters linear region from saturation region. [26]

During the current fall period, I_D is transferred from MOSFET channel to the FWD and V_{DS} has reached its initial value. Drain current I_D begins to decrease towards zero as the conducting channel is removed from the MOSFET structure. [42]

2.1.3 MOSFET losses

During the MOSFET turn-on and turn-off processes, power loss occurs primarily during the crossover time (t_c), shown in figures 7 and 8. During t_c, the device operates in linear region in which both the drain-source voltage and the drain current are high, which results in high power loss (P_{loss}) according to $P_{loss} = V_{DS}I_D$. [36]

Conduction losses occur when the device operates at on-state. The on-state power dissipation is given by

$$P_{on,MOSFET} = I_O^2 R_{DS(on)}. \quad (1)$$

Figure 9 shows the resistive components that comprise the on-state resistance in MOSFET cross-section. [36]

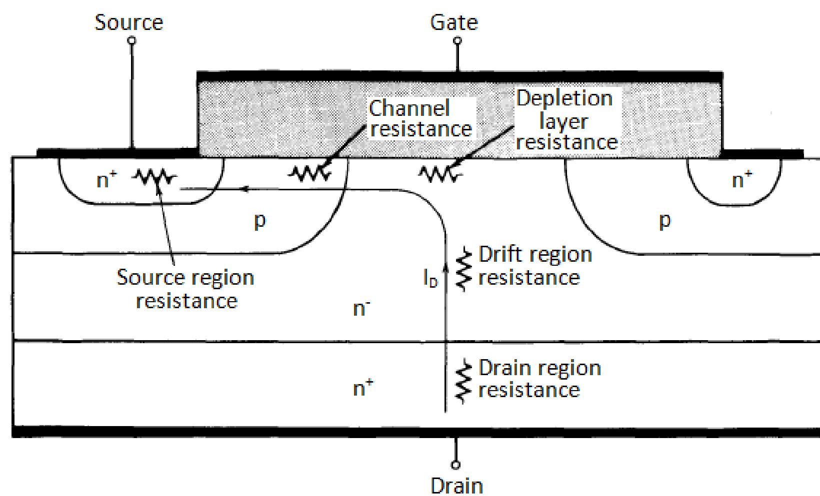

Figure 9. *On-state resistive components in an n-channel MOSFET structure. Adapted from [36].*

Channel and depletion layer resistances are affected by the gate-source voltage value as well as doping and dimensional considerations. Larger V_{GS} value will lower these resistances. For high breakdown voltage ratings, the drift region resistance dominates the on-state resistance. $R_{DS(on)}$ increases significantly with increasing junction temperature. The positive temperature coefficient arises from the decrease of charge carrier mobility as the temperature of the semiconductor increases. [36] MOSFETs have higher $R_{DS(on)}$ values than bipolar transistors. However, BJT parameters are even more sensitive to junction temperature when compared to the MOSFET. [42]

2.2 Insulated Gate Bipolar Transistor

In contrast to field-effect transistors, bipolar junction transistors operate by the injection and collection of minority carriers [49], thus both electrons and holes participate in the conduction process [50]. Power BJTs are current-controlled devices that require base

drive circuits to provide base current during the on-state. BJTs have good on-state characteristics but the base current increases the power loss in BJT control electrode. [42]

When compared with MOSFETs, the BJTs have lower conduction losses during the on-state, but longer switching times especially at the turn-off [36]. The on-state resistance of the MOSFET increases with increasing breakdown voltage. Higher voltage rating also increases the reverse recovery characteristics of the MOSFET body diode and leads to greater switching losses. [42] Because of these features, the breakdown voltage of a Si MOSFET is limited to approximately 600 V.

The low on-state conduction losses of the BJTs and the fast switching processes of the MOSFETs have been combined into the insulated gate bipolar transistor [36] that was introduced in the early 1980s. The IGBT can be controlled through the gate voltage similarly to MOSFETs, but it has lower on-state resistance since most of the output current is handled by the BJT section of the device. [42]

2.2.1 Structure and operation

An IGBT is a four-layer and three-terminal semiconductor device, which comprises of a *p-n-p-n* diode and an insulated gate, as illustrated in Figure 10 [36].

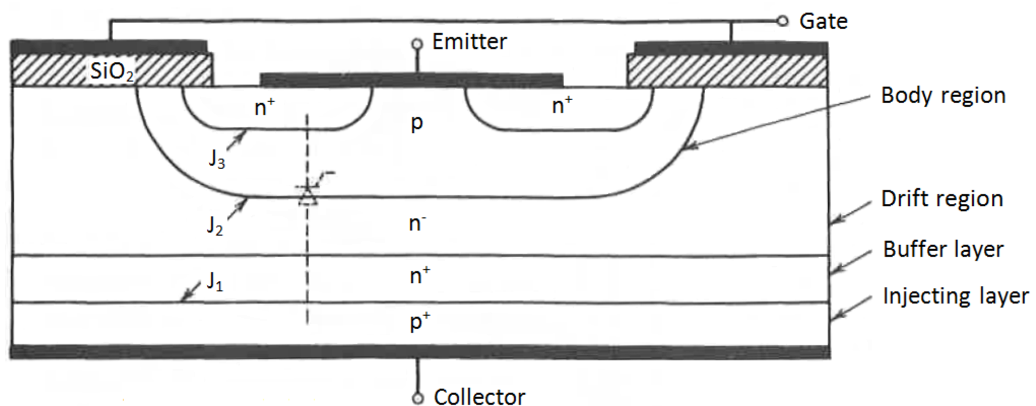

Figure 10. *Cross-section of an n-channel IGBT. Adapted from [36].*

Main difference between the structure of a MOSFET and an IGBT is the p^+-layer that forms the collector (C) of the IGBT. The added p-layer is called the injecting layer. It allows minority carrier injection into the n-layer while the device operates at on-state. [42] The injecting layer forms a pn-junction, labelled as J_1 in Figure 10. Junction J_2 between the n^-- and p-layers blocks away reverse voltages when the IGBT operates in off-state. [36]

Like the MOSFET, the IGBT is controlled between its on- and off-states by the gate voltage. When the gate-emitter voltage (V_{GE}) is less than the V_{th} of the device, there is no conductive channel to connect the device collector to the emitter (E). The applied V_{GE} is

dropped across the voltage blocking junction J_2 and only small leakage current flows through the device. [36]

When V_{GE} exceeds the threshold value, a conductive channel begins to form beneath the gate terminal. This channel connects the n^- drift region to the upper n^+ region, as shown in Figure 11.

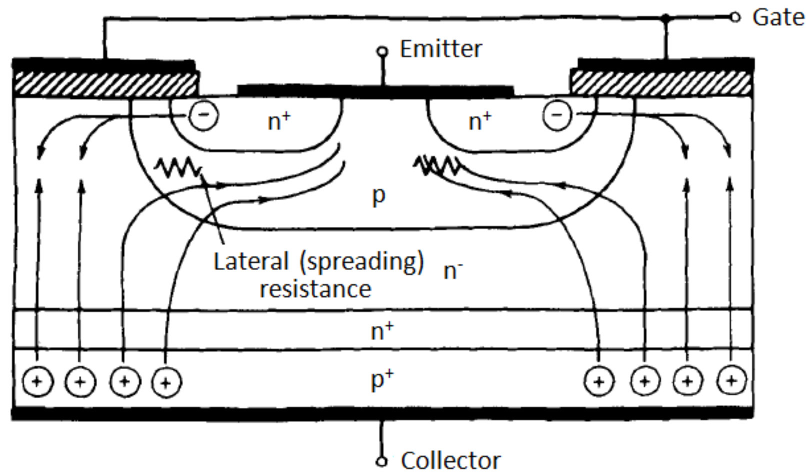

Figure 11. *A cross-section of an IGBT showing charge carrier flow paths during the on-state. Adapted from [36].*

As V_{GE} reaches V_{th}, the junction J_1 is forward biased and holes are injected from the p^+ substrate into the n^- drift region. The injected minority carriers in the drift region cause conductivity modulation, which reduces the on-state resistance of the n^--region and allows the device to have low on-state voltage drop. Electrons in the drift region recombine with the injected holes. [42] The remaining holes move by drift and diffusion through the drift region. As soon as the holes reach the *p*-type body region, their charge attracts electrons from the emitter metallization and the excess holes are recombined. Junction J_3 is collecting the diffused holes and can be considered as the collector of a *pnp*-transistor in the IGBT structure, shown in Figure 10. [36] Equivalent circuit modeling the IGBT structure and parasitic components is shown in Figure 12.

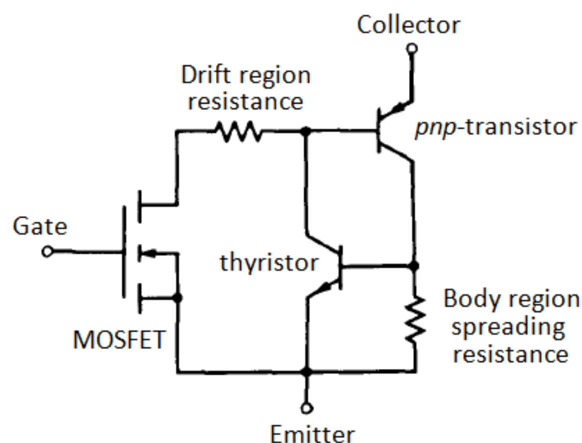

Figure 12. *Equivalent circuit of the IGBT showing the structural MOSFET, thyristor and pnp-transistor. Adapted from [36].*

The current-voltage output characteristics for the IGBT are shown in Figure 13. The output *I-V* characteristics are similar to those of a MOSFET. However, the current of the IGBT begins to increase after an offset voltage of ~0.7 V unlike in a MOSFET. During this offset period, the *pn*-junction J_1 is forward biased, but all the injected charge carriers recombine in the n^--region. [49]

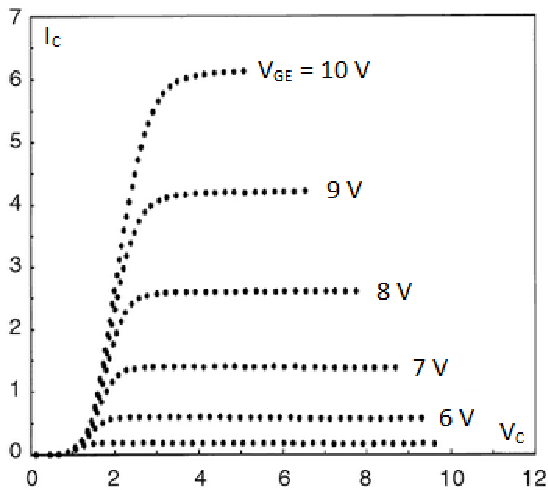

Figure 13. *Output current-voltage output characteristics of an IGBT as a function of gate-emitter voltage. Adapted from [42].*

After the offset period, the collector current begins to increase as more holes are injected to the drift region and all the injected carriers are not recombined by electrons. The current caused by hole injection acts as the base current of the *pnp*-junction. This is the preferred operation mode of the IGBT. [49] If V_{GE} is large enough, a large number of electrons are injected from the emitter to the body region and the parasitic thyristor can be turned on. This state, when both the parasitic thyristor and the *pnp*-transistor are turned on, is called the *latch-up* of the IGBT. Once the device is in latch-up, the gate has no control over the emitter current and the IGBT can be destroyed by the excessive power dissipation. [36]

2.2.2 Switching characteristics

The turn-on waveforms of the IGBT are similar to those of a MOSFET, as can be seen from Figure 14.

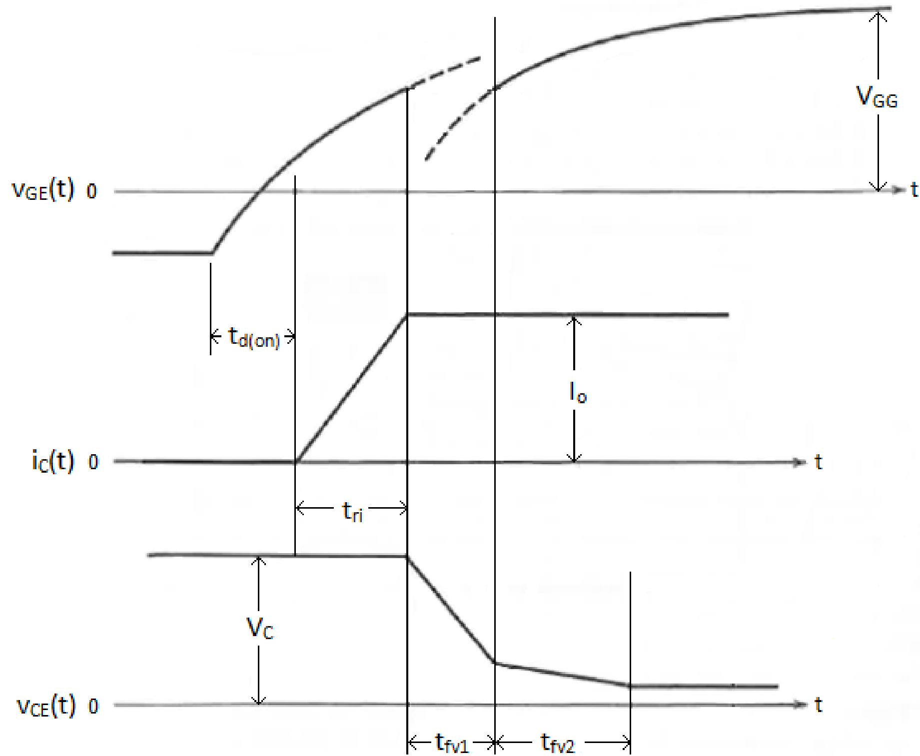

Figure 14. *IGBT turn-on voltage and current waveforms. Adapted from [36].*

The turn-on process can be divided into four intervals: turn-on delay time ($t_{d(on)}$), current rise time (t_{ri}), and collector-emitter voltage (V_{CE}) fall time (t_{fv1}, t_{fv2}). During $t_{d(on)}$ the gate current charges the parasitic junction capacitances of the IGBT and V_{GE} increases with a constant slope towards the threshold voltage. The current rise period begins after V_{GE} has reached V_{th}, and a conducting channel forms beneath the gate of the IGBT, connecting the upper n^+-region and the n^- drift region. Collector current (I_C) increases linearly to its steady-state value. [42]

As V_{GE} reaches the value that will support the steady-state collector current, V_{CE} starts to decrease. V_{CE} fall time can be divided into two time intervals: t_{fv1} and t_{fv2}. V_{CE} drops rapidly during t_{fv1} as the gate-drain capacitance of the MOSFET section of the device discharges. [42] The *pnp*-transistor section of the IGBT traverses from its saturation region to linear region during the time interval t_{fv2} [36]. V_{GE} begins to rise to its on-state value [42].

Turn-off waveforms of the IGBT are shown in Figure 15. The turn-off process begins as the gate voltage is removed [42].

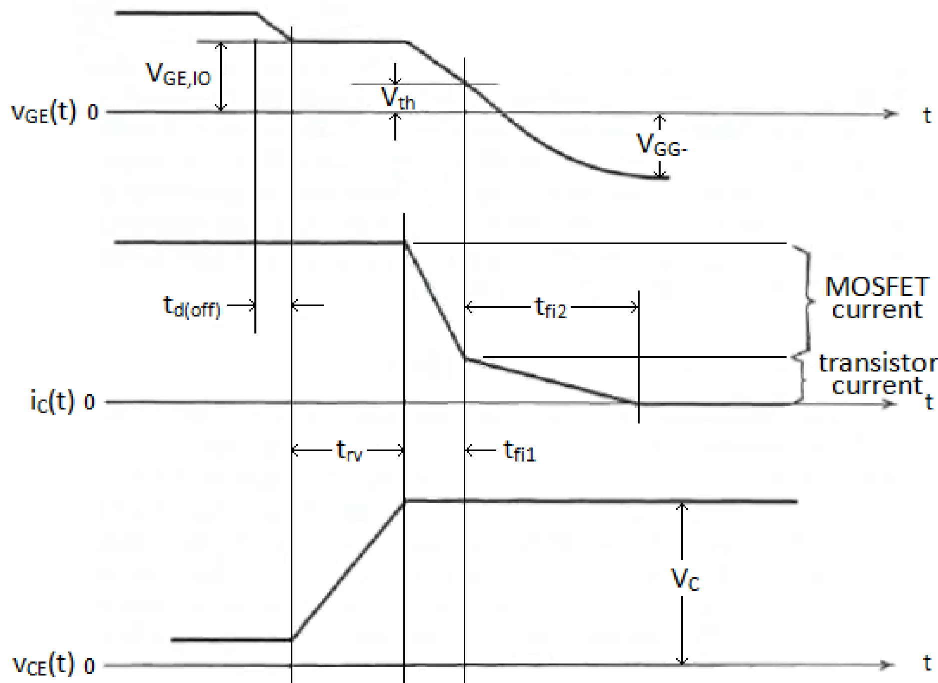

Figure 15. *IGBT turn-off voltage and current waveforms. Adapted from [36].*

The turn-off process of the IGBT can be divided into three time intervals: turn-off delay ($t_{d(off)}$), voltage rise time (t_{rv}) and current fall time (t_{fi1}, t_{fi2}). Contrary to the MOSFET turn-off process, where voltage rise time was divided into two time intervals t_{rv1} and t_{rv2}, the IGBT current fall time can be divided into two intervals t_{fi1} and t_{fi2}. [36]

As the turn-off process begins, V_{GE} decreases as the parasitic capacitances discharge during the turn-off delay phase. Voltage rise time begins as V_{GE} reaches the $V_{GE,IO}$, that is the value that is required to keep the collector current constant. V_{CE} begins to rise at a rate that is determined by the gate resistance. At the beginning of the current fall time V_{CE} has reached its final value and the conducting channel is removed. [42]

Collector current decreases rapidly during t_{fi1}, as the channel is cut [42]. After the MOSFET section of the device is turned off, the IGBT still has some excess carriers stored in the n^- drift region. These charge carriers can be removed only through recombination. During on-state, it is desirable to have large excess-carrier lifetime in order to achieve greater conduction modulation in the drift region and reduced on-state voltage drop. However, the longer excess-carrier lifetime results in longer duration of t_{fi2}. The slow decrease in collector current is called *current tailing*. [42]

2.2.3 IGBT power losses

As was discussed in previous chapters, the on-state resistance of the IGBT is significantly reduced of that of a MOSFET. When a positive voltage is applied to the gate terminal, holes are injected to the n^- drift region from the p^+ substrate. These excess carriers reduce

the resistivity of the drift region thus reducing the on-state voltage drop. The resistive components that result in on-state power loss of an IGBT are illustrated in Figure 16. [42]

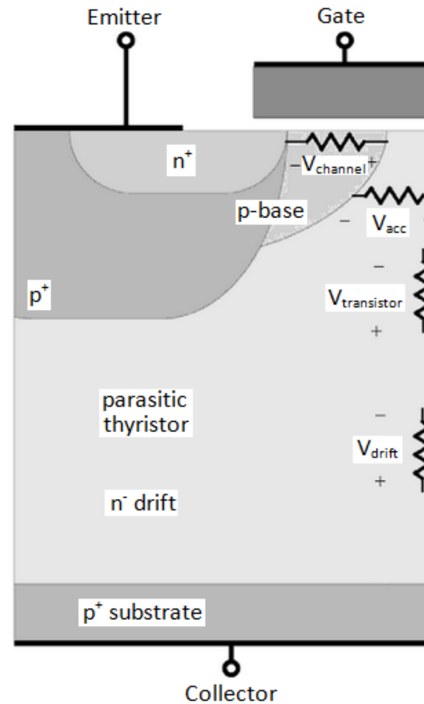

Figure 16. *On-state resistive components in the structure of an IGBT. Adapted from [42].*

The on-state voltage drop of an IGBT is given as $V_{CE(on)}$ on most IGBT datasheets. It can be calculated as

$$V_{CE(on)} = V_{p^+n} + V_{drift} + V_{MOSFET}, \quad (2)$$

where V_{p^+n} is the voltage drop across the collector junction, V_{drift} is the drift layer voltage drop and V_{MOSFET} is the voltage drop across the MOSFET section. V_{MOSFET} composes of voltage drops across the channel resistance (V_{ch}), the field-effect transistor resistance ($V_{transistor}$), and the accumulation resistance (V_{acc}). [42]

When the excess-carrier lifetime in the drift region is large, the gain of the *pnp*-transistor is high. This results in larger collector current at the *pnp*-transistor section than in the MOSFET section of the device, thus the voltage drop across the MOSFET section is small compared to total losses of the IGBT. If lifetime control techniques are used to increase the switching frequency of the device, the current gain of the *pnp*-transistor is reduced and a larger portion of the current flows through the MOSFET section. The resistance of the MOSFET section can be reduced by using a trench IGBT shown in Figure 17. [42]

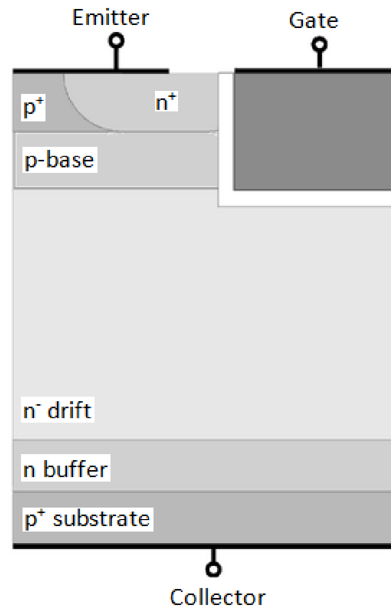

Figure 17. *Cross-section of a trench IGBT. Adapted from [42].*

By extending the gate terminal below the *p*-base and the n^- drift region, a channel is created between the n^+ emitter and n^- drift region, eliminating the accumulation layer resistance from the IGBT structure. [42]

Although the IGBT has lower on-state resistance compared to the power MOSFET, current tailing during the turn-off process limits the operating frequency of the IGBT. There is also a significant power loss during current tailing. Lifetime control techniques can be used to reduce the minority carrier lifetime in the n^- drift region. However, smaller minority carrier lifetime results in weaker conduction modulation and greater on-state losses. There is a tradeoff between smaller on-state losses and faster switching times. As a result, higher speed IGBTs usually have lower current ratings. [42]

2.3 Silicon carbide semiconductors

Power technology tends to move towards higher efficiency, higher power density and more integrated systems. Improvements in power semiconductor devices have been primarily driven by Si power devices over the past 50 years. Si MOSFETs dominate the market in applications that have voltage ratings below 600 V. Si IGBTs are developed for applications from 600 V to 6.5 kV. However, Si power devices are approaching their performance limitations. [48] In addition to Si device voltage limitations, their internal parasitic parameters, IGBT tail losses, and large reverse recovery charge limit the operation frequency of the switching components to less than 100 kHz and even less in the case of Si IGBT. Also the narrow band gap of Si limits the device temperature below 125°C. [44] *Wide bandgap semiconductors*, such as silicon carbide (SiC), can operate at high voltage, high temperature and at high switching frequencies, thus offering potential replacement for the matured Si devices [51].

The conductivity in semiconductors is based on excitation of electrons from lower energy band (valence band) to higher energy band (conduction band). The amount of energy required for an electron to move to conduction band is called the *bandgap energy* (E_g). [49] Silicon is considered as an *indirect semiconductor*. In an indirect semiconductor an electron in the conduction band minimum cannot fall directly into the valence band maximum. Indirect semiconductors require a change of momentum for the electron in a transition. [50] Electrons may go through some defect state E_t within the bandgap, as illustrated in Figure 18 (a). Part of the energy E_g is given up as heat to the semiconductor lattice. [49]

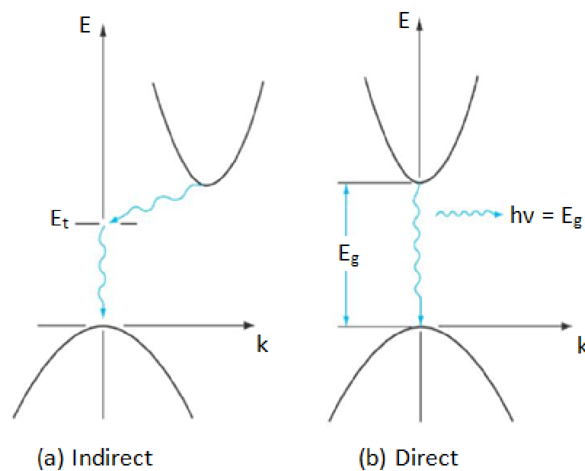

Figure 18. *Indirect and direct electron transitions in semiconductors: (a) indirect transition through a defect state (b) direct transition with photon emission. Adapted from [49].*

In *direct semiconductors*, such as SiC, the conduction band minimum and valence band maximum are at the same momentum value against each other, as shown in Figure 18 (b). An electron on the conduction band minimum can fall directly to an empty state in the valence band. The transition does not require a change in crystal momentum for the electron and it can give off the energy difference E_g as a photon. [49]

2.3.1 Differences between Si and SiC

SiC devices have remarkable advantages in conductivity, breakdown voltage and in high frequency and high temperature operation [41]. The physical properties that explain the differences between Si and SiC materials are listed in Table 1.

Table 1. *Physical properties of Si and SiC [41, 49].*

Property	Si	SiC
Bandgap energy, E_g (eV at 300K)	1.11	2.86
Critical electric field, E_{crit} (V/cm)	2.5 * 10^5	2.2 * 10^6
Thermal conductivity, λ (W/cm*K at 300K)	1.5	3-4
Saturated electron drift velocity, v_{sat} (cm/s)	1 * 10^7	2 * 10^7
Electron mobility, μ_n (cm^2/V*s)	1350	950
Hole mobility, μ_p (cm^2/V*s)	480	120

A perfect semiconductor crystal is called an *intrinsic* semiconductor. An intrinsic material has no impurities or lattice defects, and there are no charge carriers at 0 K. Electron-hole-pairs, that are generated as electrons are excited thermally across the bandgap, are the only charge carriers in an intrinsic material. At a given temperature there is a certain concentration of electron-hole-pairs, which are measured as the intrinsic carrier density (n_i). [49] The bandgap energy affects the intrinsic carrier density according to

$$n_i(T) = \left(\frac{2\pi kT}{h^2}\right)^{\frac{3}{2}} (m_n m_p)^{\frac{3}{4}} e^{-\frac{E_g}{2kT}}, \quad (3)$$

where k is the Planck's constant, h is the Boltzman's constant, T is the absolute temperature and m_n and m_p are the electron and hole effective masses respectively. As can be noticed from Table 1, SiC has higher bandgap energy (2.86 eV) compared to that of Si (1.11 eV). According to Equation 3, a lower intrinsic carrier density can be achieved with higher bandgap energy. n_i is also affected by the temperature. [41]

The intrinsic carrier density affects the leakage current (J_s) of a *pn*-junction as given by

$$J_s = qn_i^2 \left(\frac{D_p}{L_p n_p} + \frac{D_n}{L_n n_n}\right), \quad (4)$$

where D_p and D_n are the diffusion constants, L_p and L_n are the diffusion lengths and n_p and n_n are the carrier densities for holes and electrons respectively. Higher bandgap energy and thus lower intrinsic carrier density will reduce the leakage current of a *pn*-junction. [41]

The intrinsic carrier density also affects the surface potential (Ψ_B) of a semiconductor, according to

$$\Psi_B = \frac{kT}{q} ln\left(\frac{n_n}{n_i}\right). \tag{5}$$

Surface potential has an influence on the threshold voltage of the material, according to

$$V_{th} = \phi_{ms} - \frac{Q_f}{C_{ox}} + 2\Psi_B + \frac{\sqrt{4\varepsilon_s q n_n \Psi_B}}{C_{ox}}, \tag{6}$$

where ϕ_{ms} is the work function between a metal and a semiconductor and Q_f is the fixed oxide density. Lower intrinsic carrier density results in higher surface potential and thus in higher threshold voltage value. [41]

As can be noticed from Table 1, SiC has 10 times greater critical electric field (E_{crit}) ($2.2^{*}10^{6}$ V/cm) than Si ($2.5^{*}10^{5}$ V/cm). This makes high-voltage power devices achievable with SiC. [49] The breakdown voltage of the MOSFET is dependent of E_{crit} according to

$$V_{BD} = \frac{\mu_n \varepsilon_s E_{crit}^2}{2\sigma}, \tag{7}$$

where ε_s is the permittivity of the semiconductor and σ is the conductivity of the drift region. As can be seen from Equation 7, with a higher critical electric field, the drift region can be adjusted to achieve higher conductivity at the same breakdown voltage value. [41]

The main advantage of wide band gap semiconductors for power device applications is their very low on-state resistance even at high voltages. The on-state resistance is dependent of the breakdown voltage and given by

$$R_{DS(on)} = \frac{4V_{BD}^2}{\mu_n \varepsilon_s E_{crit}^2}. \tag{8}$$

The specific on-resistance of Si and 4H-SiC devices are compared in Figure 19 as a function of breakdown voltage. [16]

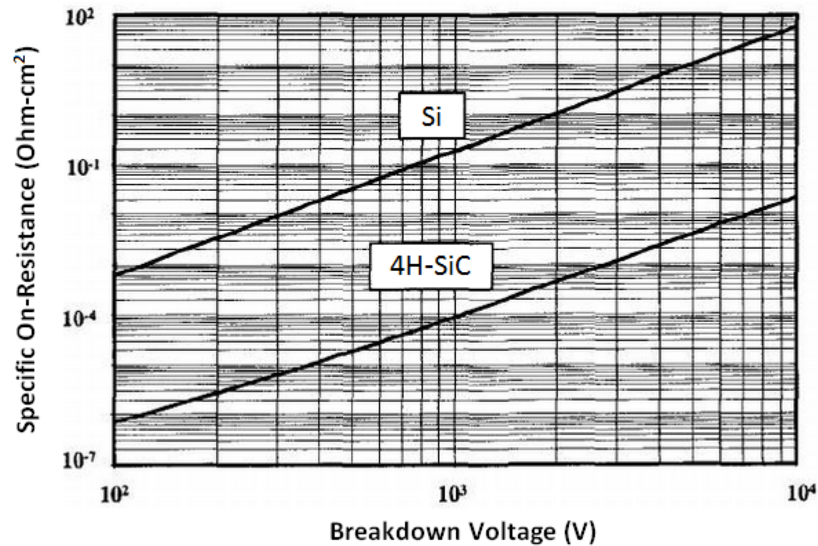

Figure 19. *Specific drift region on-resistances in Silicon and 4H-SiC as a function of breakdown voltage. Adapted from [16].*

From Figure 19 can be seen that the on-resistance values of 4H-SiC are approximately 2000 times smaller than those for Si devices with the same breakdown voltage. [16]

Also, the electron saturation velocity (v_{sat}) for SiC is higher ($2^{*}10^{7}$ cm/s) compared to that of Si ($1^{*}10^{7}$ cm/s). If charge carriers are travelling at their saturation drift velocity in a channel with length of L, the channel transition time (τ) is given by

$$\tau = \frac{L}{v_{sat}}. \tag{9}$$

A higher transition frequency can be achieved with a higher saturation velocity. [41]

Thermal conductivity (λ) of SiC is 2-3 times higher than the thermal conductivity of Si. High thermal conductivity promises a low thermal resistance. This property gives SiC great heat dissipation capability. [41] Smaller thermal resistance allows SiC devices to be smaller, which leads to lower parasitic capacitances and enables higher switching speeds [48]. The SiC MOSFET die size can be 50% smaller than the die of a Si device with similar ratings. Also, the junction temperature of SiC can be above 150°C. High junction temperature reduces the thermal management system volume and increases the reliability of the system. [44]

The lower charge carrier mobility in SiC MOSFET results in higher channel resistance when compared to that of the Si devices [11]. Therefore the SiC MOSFETs with the present technology need to be driven with a higher gate voltage than the typical Si IGBTs and Si MOSFETs [57].

The effects of the physical properties of SiC and Si on the performance of switching devices are listed in Table 2.

Table 2. *The effect of physical properties of Si and SiC on semiconductor device performance [16, 41, 48]*

Property	Si	SiC	Effect
Bandgap energy, E_g (eV at 300K)	1.11	2.86	Lower n_i, reduced leakage current, increased V_{th}
Critical electric field, E_{crit} (V/cm)	2.5 * 10^5	2.2 * 10^6	Higher conductivity with the same breakdown voltage, smaller $R_{DS(on)}$, smaller on-state losses
Thermal conductivity, λ (W/cm*K at 300K)	1.5	3-4	Low thermal resistance, reduced power loss, smaller devices, high temperature operation, increased reliability
Saturated electron drift velocity, v_{sat} (cm/s)	1 * 10^7	2 * 10^7	Higher transition frequency
Electron mobility, μ_n (cm^2/V*s)	1350	950	Lower charge carrier mobility results in higher channel resistance
Hole mobility, μ_p (cm^2/V*s)	480	120	

Before the development of SiC devices, MOSFETs have usually been chosen for applications with voltages less than 600 V. At these voltages, the on-state voltage drop of the MOSFET is still competitive with the voltage drop in minority carrier devices and their switching speed is significantly faster. At voltages greater than 600 V, minority carrier devices have been preferred due to their lower on-state losses. [22] SiC technology has enabled the usage of MOSFETs also with high-voltage applications since they have 10 times larger critical electric field compared to Si devices [48].

Compared with IGBTs, the MOSFETs have significantly lower switching losses due to their majority carrier conduction mechanism [48]. Majority carrier devices do not have minority carriers in the device structure that need to be stored during the turn-on process and removed through recombination during the turn-off process. Since majority carrier devices do not suffer from minority carrier storage effects, they have higher switching speeds and higher cut-off frequencies than bipolar devices. [50] The turn-off switching time of the IGBT is significantly longer than that of the MOSFET due to current tailing [22]. The only delays during the turn-on and turn-off processes of a MOSFET are due to charging and discharging the device parasitic capacitances [56]. The parasitic components in the MOSFET structure are discussed in Chapter 3.1.

2.3.2 SiC device challenges

Although SiC devices show promising advantages, many challenges exist in device and application perspectives. Faster switching, higher temperature and smaller size raise new design challenges.

SiC allows the usage of higher frequencies, which is desirable in many applications. However, higher switching speed together with parasitic capacitances and inductances of the device results in substantial *electromagnetic interference* (EMI). High-frequency applications will require advanced EMI filters and innovative EMI shielding techniques. [48] The internal parasitic components cannot be completely avoided and therefore it is important to try to avoid all external parasitics that can impact the switching performance of the power devices at fast switching frequencies. [23]

Low voltage SiC devices from 400 V to 1700 V are commercially available. However, high voltage SiC devices for 3.3 kV and above are still in development stages. One of the reasons why high voltage SiC devices are not commercially available is their very limited current ratings. Therefore, SiC based power modules that combine several SiC dies in parallel are currently necessary for high power conversion system. [23]

For small and fast SiC devices the short circuit withstand capability is challenging. The short circuit withstand time of a SiC MOSFETs is approximately 1 μs when the traditional Si devices have a short circuit withstand time greater than 10 μs. This sets challenges to protection circuits that are required to have a faster response time when compared to Si IGBTs and Si MOSFETs. [23]

The smaller size of the SiC components and their corresponding higher loss density pose new challenges for thermal design. Although SiC devices can operate at higher temperatures, most of the external components such as the package materials, capacitors, and control electronics are rated for lower operation temperatures. [48] High temperature technologies need to cover all aspects of the packaging, including die attach, substrate, encapsulant, and interconnection structure. Advanced packaging techniques are also required for minimizing the parasitic components and for reducing the weight and size of the device. [23]

As was discussed in Chapter 2.3.1, the higher critical electric field of SiC also affects the threshold voltage by increasing it, thus SiC devices require higher gate voltage for on-state operation than Si devices. This makes the traditional gate driver incompatible with the SiC MOSFET. Also, the higher switching frequency sets challenges for the gate drive design. [48]

It is expected that SiC devices and their related technologies will mature over time. This will result in devices with lower cost, higher current ratings, better reliability, better gate drive, and high temperature packaging. Many of these advances are under rapid

development. One barrier to overcome for wide bandgap technologies is to train engineers to utilize these new components. [23] Integrating SiC technology into the electrical systems requires deep understanding of system design, including EMI and thermal issues. The limited knowledge of the new technology causes non-recurring engineering costs that might be a concern for many potential SiC users. Also, the absolute cost of SiC devices is higher than the cost of Si devices. The savings with SiC components may come from smaller passive components, lower cooling requirements and higher absolute power ratings. [48]

3. NONIDEAL EFFECTS OF THE SiC MOSFET

Silicon carbide components are smaller than silicon devices. Their die size can be 50% smaller than that of a Si device with similar rating. The smaller component size leads to much smaller parasitic components that enable higher switching speeds. However, internal parasitics from the device package and external parasitics induced by the circuit board are inevitable. Combined with extremely fast switching speeds, these parasitic inductances and capacitances can cause overshoot and oscillation in device voltages and currents. [44] SiC MOSFET parasitic components are discussed in Chapters 3.1.1 *Parasitic capacitances*, 3.1.2 *Power loop inductances*, and 3.1.3 *Common mode stray inductance*. The effects of these parasitic elements on device switching are studied further in Chapter 3.2 *Switching oscillation*.

3.1 SiC MOSFET parasitic components

SiC MOSFET has superior material properties that allow five to ten times faster switching compared to most advanced Si IGBTs. However, the high switching frequency, high current and voltage slew rates (*di/dt* and *dv/dt*, respectively) together with device parasitic inductances and capacitances create high frequency oscillations and overshoots in the voltages and currents of the device. [38] The switching behavior of the MOSFET is also nonlinear due to varying voltage-dependent parasitic capacitances [51]. Parasitic components from device packaging, printed circuit board and bus bar do not play such a critical role when a power converter is designed with Si switches, as they switch at a much slower rate than SiC MOSFETs. [38] The parasitic components of a SiC MOSFET are illustrated in Figure 20 for component packaging, equivalent circuit, and device cross section.

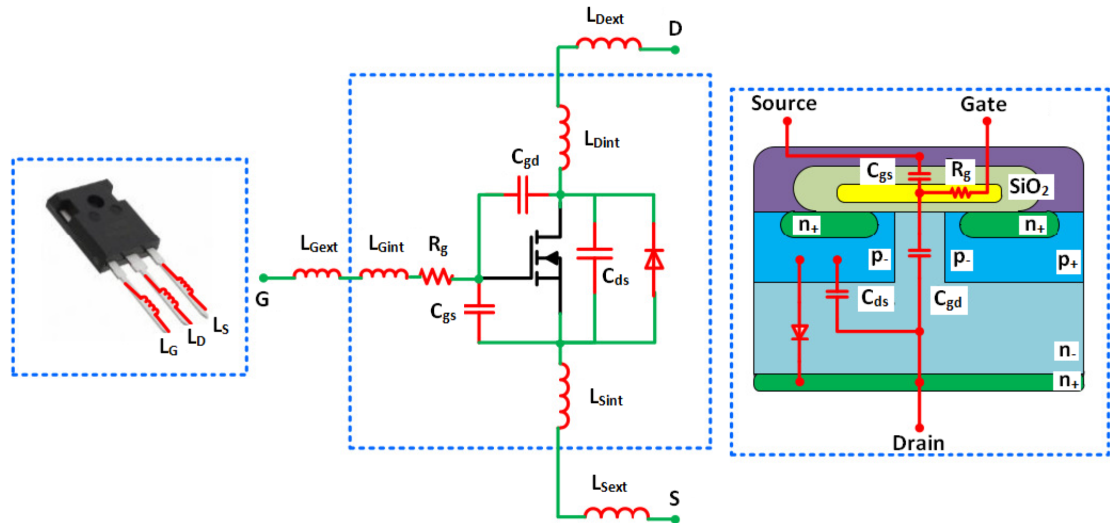

Figure 20. *Parasitic components of a SiC MOSFET presented in the package, equivalent circuit and simplified cross section of the device. Adapted from [38].*

The SiC MOSFET can be presented with three parasitic capacitances between its terminals: gate-drain capacitance (C_{gd}), gate-source capacitance (C_{gs}), and drain-source capacitance (C_{ds}). The parasitic inductances presented in Figure 21 consist of internal and external lead inductances. Figure 21 also shows external inductances that are relevant in the study of MOSFET switching behavior.

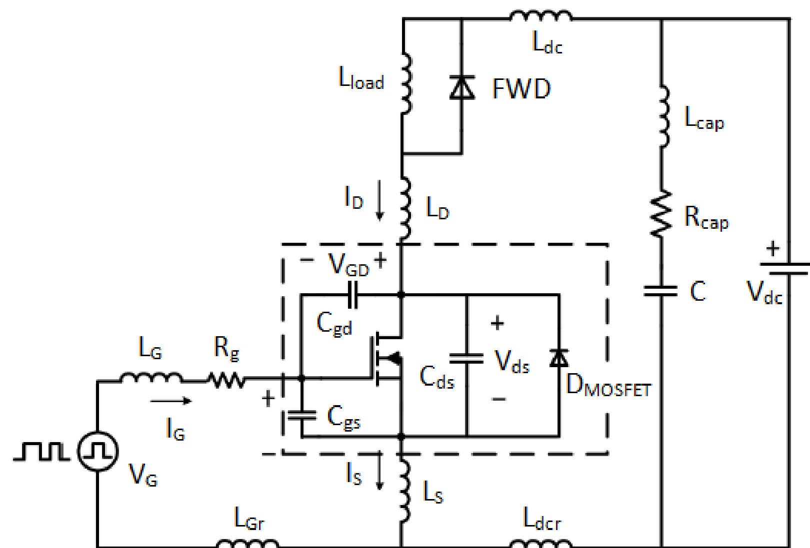

Figure 21. *Test circuit of a MOSFET with internal and external parasitic inductances and parasitic capacitances. Adapted from [38].*

The equivalent circuit shown in Figure 21 can be divided into two loops: power and gate loop. The power loop consists of source voltage (V_{dc}), DC bus inductance (L_{dc}), drain inductance (L_D), the MOSFET, DC bus return inductance (L_{dcr}) and source inductance (L_S). The gate loop comprises of gate voltage (V_G), gate resistance (R_g), gate inductance

(L_G), gate return inductance (L_{Gr}) and source inductance (L_S). Source inductance exists in both loops and is also referred to *common mode stray inductance*. [38]

3.1.1 Parasitic capacitances

During the turn-on process the input capacitance of the MOSFET is charged to threshold voltage and before the device begins to turn off it is discharged to plateau voltage value. The impedance of the driver circuit and the input capacitance have a direct relationship to the turn-on and turn-off delays. The output capacitance (C_{oss}) of a MOSFET is important in soft switching applications since it can affect the resonance of the circuit. C_{rss} is the reverse transfer capacitance that equals the gate-drain capacitance. C_{rss} if often called the Miller capacitance and it is one of the major parameters affecting the voltage rise and fall times during switching. C_{iss}, C_{oss} and C_{rss} can be expressed as:

$$C_{iss} = C_{gs} + C_{gd}$$

$$C_{oss} = C_{ds} + C_{gs}$$

$$C_{rss} = C_{gd}.$$ [21]

C_{gd} and C_{ds} vary as a function of V_{DS} and therefore also the capacitances C_{iss}, C_{oss} and C_{rss} vary as a function of voltage. C_{gs} is constant and does not depend on the drain-source voltage value. [35]

Gate charge values reflect the charge stored on the device capacitances [21]. Component datasheets usually report total gate charge (Q_g), gate-source charge (Q_{gs}) and gate-drain charge (Q_{gd}) values for MOSFETs. The time that is required to turn-on a switching device equals the time it takes to inject Q_{gs} and Q_{gd} into the gate terminal. Q_{gs} is the charge required to bring V_{GS} from zero to plateau value and Q_{gd} is the charge required to bring V_{GS} through the plateau region. [35]

3.1.2 Power loop inductances

As was discussed in Chapter 3.1, DC bus inductance, drain inductance and DC bus return inductance constitutes the power loop together with common mode stray inductance. The three inductances L_{DC}, L_D, and L_{DCR} have similar effects in the switching characteristics and are therefore referred as *power loop inductance* (L_P). L_P causes oscillations in V_{DS} and I_D during the turn-on and turn-off processes. During the turn-on process L_P resonates with the junction capacitance of the freewheeling diode and during the turn-off process it resonates with the output capacitance C_{oss}. [38]

During the turn-on process a rapid current change (*di/dt*) with a large L_P value causes a voltage drop in V_{DS}. This voltage drop equals the induced voltage in the power loop

inductance (V_{LP}) given as $V_{LP} = L_P \frac{di}{dt}$. The drop in V_{DS} causes reduction in turn-on loss (E_{on}). The reduction in E_{on} increases with increased L_P value as illustrated in Figure 22 for L_P = 50 nH and L_P = 200 nH. [38]

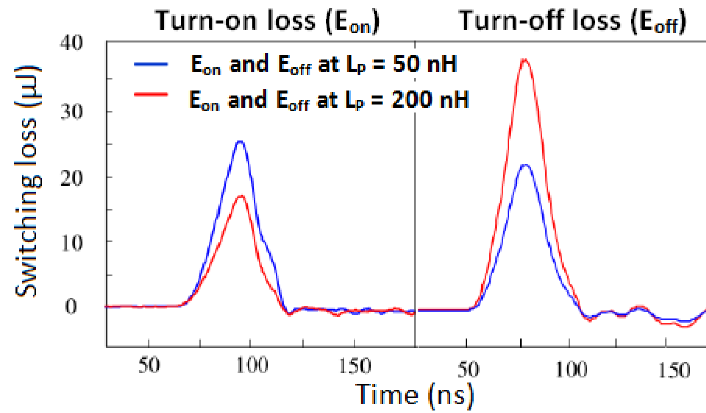

Figure 22. *The effect of increased power loop inductance L_P on turn-on and turn-off loss. Adapted from [38].*

However, as can be seen from Figure 22, the higher L_P value results in higher turn-off loss during the turn-off process. During the turn-off process L_P resonates with C_{oss} and causes oscillation and overshoot in V_{DS}. [38]

Although the higher value of L_P reduces the turn-on loss, the reduction in E_{on} is less compared to the increase in turn-off loss (E_{off}) and the total loss of the device increase. L_P must be taken into consideration in optimum utilization of SiC MOSFET. However, the common mode parasitic stray inductance affects the switching performance the most out of all the parasitic inductances. The effects of L_S on the switching processes are discussed in the next chapter. [38]

3.1.3 Common mode stray inductance

Almost all the commercial transistors are three-pin devices. The MOSFET is vulnerable to unwanted interaction between its power supply and the sensitive input signal that is utilized for driving the MOSFET. In a three-pin device, the stray inductance of the source wire bonding is coupled with the fast current variation and current slope. The fast current slope induces a voltage in L_S that is opposite to the driving signal of the MOSFET. This opposing signal slows down every switching cycle, which in turn increases the cycle by cycle switching loss. [18]

As was discussed in Chapter 2.1.2, during the turn-off process V_{GS} starts to decrease from its maximum value to plateau voltage and voltage rise period begins as the drain-source voltage begins rising After the V_{DS} rise period, I_D starts to decrease. The rapid change in I_D induces a voltage over the parasitic inductance L_S (V_{LS}) according to $V_{LS} = L_S \frac{dI_D}{dt}$. This

voltage across L_S can increase the gate-source voltage above the plateau value and can result in a false turn-on of the MOSFET. [38] L_S causes delay to device turn-off and correspondingly increases the turn-off power dissipation [18].

During the turn-on process V_{GS} and I_D increase, causing an increase in the voltage over the inductance L_S according to $V_{LS} = -L_S \frac{dI_D}{dt}$. The induced voltage reduces V_{GS} value and the system behaves as a negative feedback system. As V_{GS} is reduced, it takes more time for V_{DS} to come down to its saturation value $V_{DS(on)}$. [38] The voltage over L_S results in turn-on delay and in increased turn-on switching loss. Also, the effective value of V_{GS} is reduced and the actual voltage across the gate and the source is less than the fixed value required to turn on the device. [18]

With a *Kelvin source contact* and an added fourth pin to the device, the power path and the driving signal path of the MOSFET can be separated. With the utilization of the fourth pin it is possible to obtain a driving signal that is immune to any disturbance that the fast current variation in the power path could produce. The utilization of a Kelvin source reduces the overall power losses within the MOSFET, which leads to lower operation temperature and potentially to more reliable and longer lasting power systems. Lower working temperature also offers the opportunity to use smaller heat sinks, thus less area would be occupied from the circuit board. [18]

3.2 Switching oscillation

Since the SiC MOSFETs can operate at high switching frequencies, they allow designing fast-switching electronic devices. However, the fast-switching characteristics can lead to undesirable voltage and current overshoots and oscillations that are the result of high *dv/dt* and *di/dt* rates coupled with the parasitic components of the circuit. [44] Voltage and current overshoot and oscillation may cause damage to the device, increase power losses and introduce EMI noise. [51] The origins of switching oscillations are covered in Chapter 3.2.1 for the turn-on process and in Chapter 3.2.2 for the turn-off process. The equivalent circuit used to investigate the switching processes of a SiC MOSFET is presented in Figure 23.

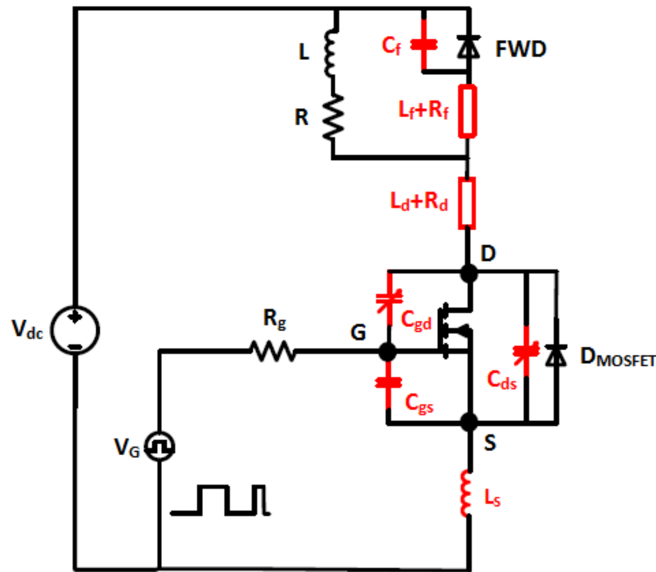

Figure 23. *Equivalent circuit of a SiC MOSFET with parasitic components. Adapted from [26].*

The parasitic components are shown in red color in Figure 23. The inductive load L can be assumed to be a constant current source with an inner resistance R [26]. This current is carried either by the MOSFET, or the FWD, or by both, depending on the phase of the MOSFET switching cycle [51]. Junction capacitance of the freewheeling diode is considered as a parallel parasitic capacitance C_f. Also, the parasitic inductance L_f and resistance R_f are presented in the freewheeling loop. [26]

The SiC MOSFET is modelled with three terminal capacitances C_{gd}, C_{gs}, and C_{ds}. Parasitic capacitances C_{gd} and C_{ds} are voltage-dependent and nonlinear. As was discussed in Chapter 3.1.1, C_{gd} is a function of the drain-source voltage V_{DS}. The equivalent circuit also considers the parasitic inductance and resistance of the drain terminal (L_D and R_D respectively) and the common mode source inductance. The parasitic inductance of the gate terminal (L_G) is ignored in the equivalent circuit, as its influence on the switching behavior is insignificant compared to the domination of L_S. [26]

3.2.1 Switching oscillation during turn-on process

The turn-on process of a SiC MOSFET with parasitic components is divided into four phases: turn-on delay, current rise period, current ringing and full conduction [26]. These phases of the turn-on process are shown in Figure 24.

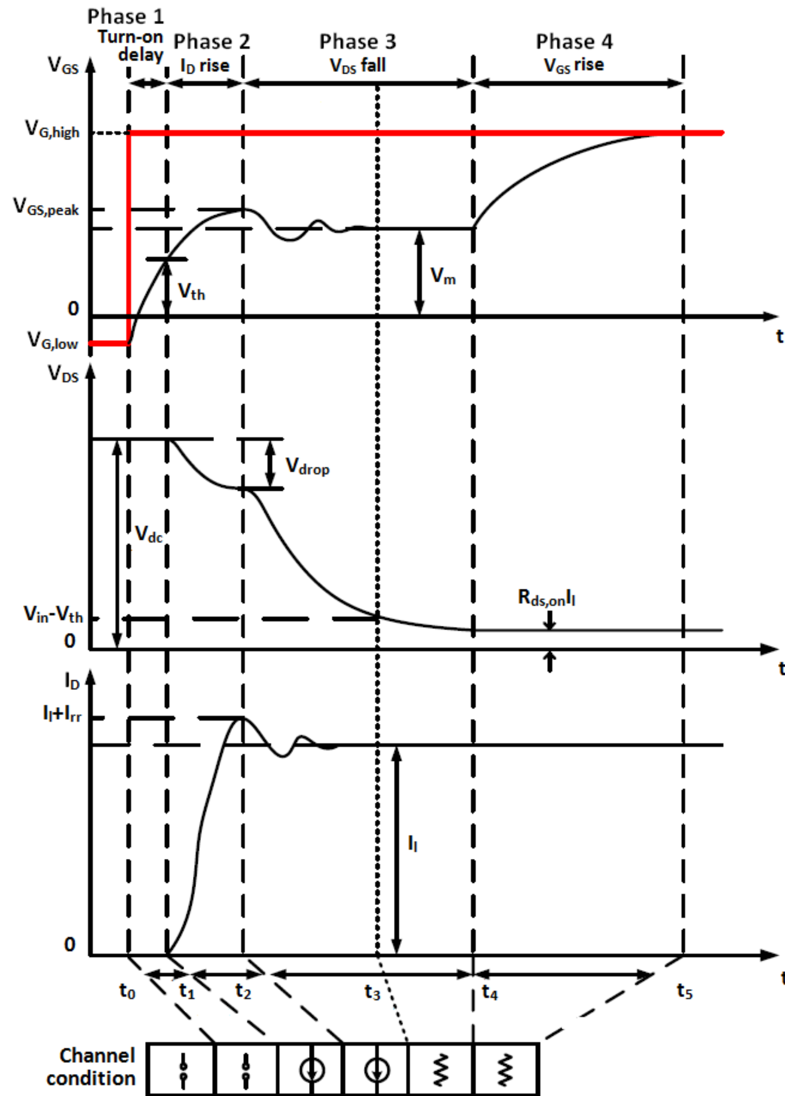

Figure 24. *Switching waveforms of the SiC MOSFET during the turn-on process, with parasitic components. Adapted from [26].*

Similarly to the ideal MOSFET turn-on process, the turn-on delay (Phase 1, t_0-t_1) begins as the gate voltage steps from its low value ($V_{G,low}$) to high value ($V_{G,high}$). A gate current flows through the gate resistor and charges the input capacitances C_{gs} and C_{gd} and V_{GS} begins to rise. The MOSFET channel is open and not conducting during this phase. [26]

The current rise period (Phase 2, t_1-t_2) starts as V_{GS} reaches the threshold voltage. The MOSFET channel forms and allows channel current to flow between the source and drain terminals. The MOSFET enters saturation region. The drain-source terminal blocks V_{dc} as long as the freewheeling diode is conducting. The junction capacitance of the FWD discharges and adds to I_D causing a drain current spike according to equation $I_D = I_l + I_{rr}$, where I_{rr} is the reverse recovery current caused by the discharge of C_f and I_l is the load current. [26] The additional power loss caused by the reverse recovery current during the turn-on process can be estimated from the area of the current spike in the current

waveform. The surface area of the current spike equals the total additional charge (Q_{tot}) during the turn-on process. The power losses caused by the reverse recovery current ($E_{loss,rr}$) can be calculated as

$$E_{loss,rr} = f * V_{dc} * Q_{tot}. \text{ [2]} \tag{10}$$

In half-bridge applications, where another MOSFET is utilized in the same leg to achieve synchronous rectification, I_{rr} is the reverse recovery current of the body diode of the synchronous MOSFET [27]. During the current rise period V_{DS} decreases the amount V_{drop}, since the rapid change in I_D induces voltages across L_s and L_D according to $V_{drop} = (L_S + L_D)\frac{dI_D(t)}{dt}$ [14].

Current ringing phase (Phase 3, t_2-t_3) begins after the drain current reaches its peak value and the FWD starts to share V_{dc} with the MOSFET. MOSFET channel is still in the linear region. The resonance of the FWD junction capacitance and the power loop inductance causes current ringing. This ringing occurs at a natural frequency that can be denoted as $\omega_n = 1/\sqrt{(L_S + L_D + L_f)C_f}$. Oscillation frequency is constant for constant parasitic inductances and capacitances in a system. Equivalent circuit of the current ring phase is shown in Figure 25.

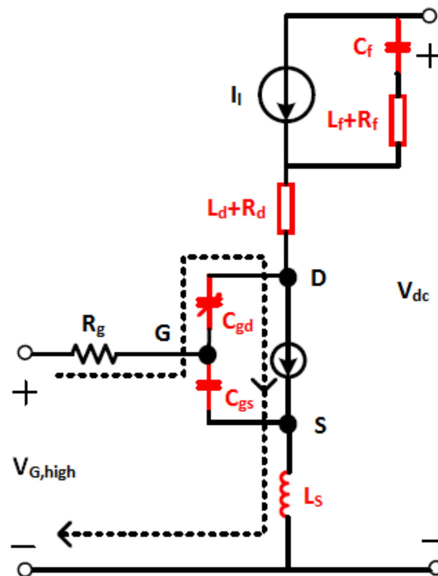

Figure 25. *Equivalent circuit of a SiC MOSFET during the turn-on current ringing phase. Adapted from [26].*

The current ringing phase can be divided into two intervals during which the device switches over from linear region to saturation region. At the end of Phase 3, after the MOSFET has entered the saturation region, V_{GS} equals the Miller plateau voltage and drain current has settled to load current value. [26]

During full conduction (Phase 4, t_4-t_5) the channel is complete and V_{DS} equals the voltage drop over the channel resistance, according to $V_{DS} = R_{DS(on)} * I_l$. $V_{G,high}$ must be higher than the Miller plateau voltage to provide fully open channel and low enough channel resistance. Therefore, C_{gs} is charged to $V_{G,high}$ during Phase 4. [26]

Current ringing can be attenuated by controlling $V_{G,high}$ to a lower value during the turn-on process. Lower $V_{G,high}$ value will suppress the peak current. The relationship between di_D/dt and $V_{G,high}$ can be found

$$\frac{dI_D}{dt} = \frac{V_{G,high} - \left(\frac{I_D}{g_m} + V_{th}\right)}{R_g \frac{C_{iss}}{g_m} + L_S} \quad [26]. \tag{11}$$

From Equation 10 can also be noticed that increasing the gate resistor value will slow down the di_D/dt rate and thus suppress the resonance between C_f and the power loop inductance.

3.2.2 Switching oscillation during turn-off process

Similar to the turn-on process, the turn-off process of the unideal MOSFET can be divided into four phases: turn-off delay, voltage rise, current fall and V_{GS} fall [26]. These phases of MOSFET turn-off are illustrated in Figure 26.

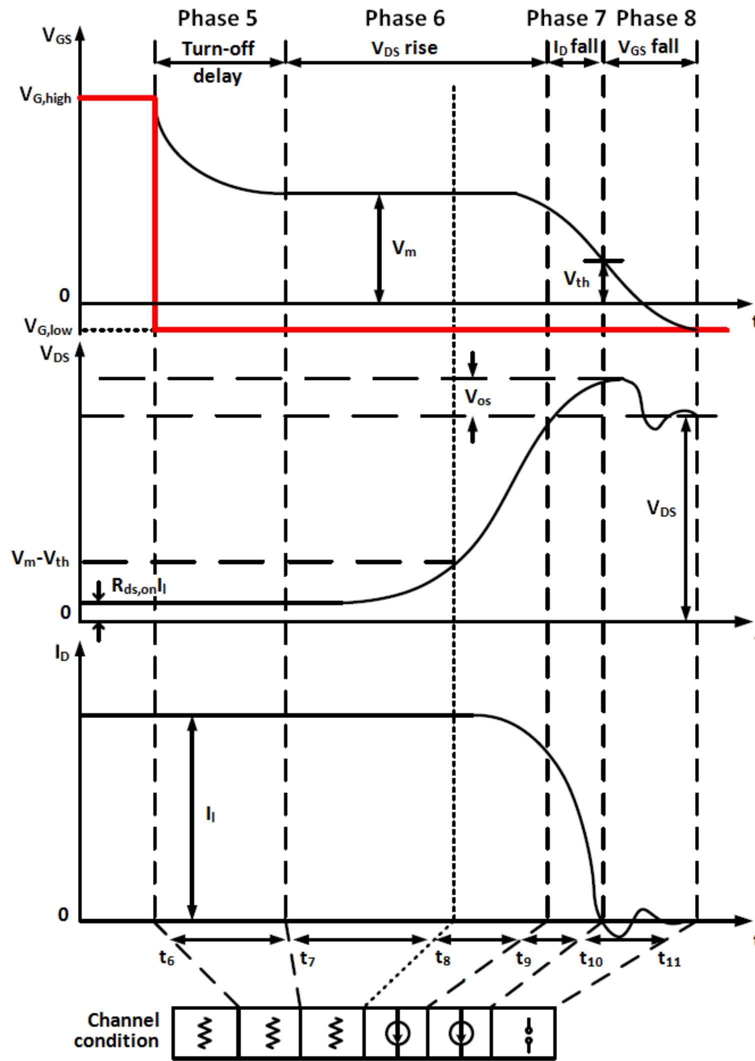

Figure 26. *SiC MOSFET switching waveforms with parasitic elements during turn-off process. Adapted from [26].*

Turn-off delay (Phase 5, t_6-t_7) begins as the gate voltage steps from its high value to $V_{G,low}$. The parasitic output capacitances C_{gs} and C_{gd} begin to discharge. [26]

Voltage rise period (Phase 6, t_7-t_9) starts when V_{GS} reaches the Miller plateau value. This phase can be divided into two intervals (t_7-t_8 and t_8-t_9), during which the MOSFET enters linear region from saturation region. [26]

During the current fall period (Phase 7, t_9-t_{10}), I_D is transferred from the MOSFET channel to the FWD that begins to conduct as V_{DS} reaches V_{dc}. The device is still in the linear region. A voltage overshoot can be observed during this period. V_{DS} can be expressed as

$$V_{DS} = V_{dc} - \left(L_S + L_D + L_f\right)\frac{dI_D}{dt} + V_{FWD} + R_f I_l - \left(R_D + R_f\right)I_D, \tag{12}$$

where V_{FWD} is the on-state voltage drop of the FWD. [26] The high di_D/dt rate during the turn-off transient induces voltage spikes on L_s and L_D, which causes the overshoot in V_{DS}.

[44] The amplitude of the voltage overshoot is closely related to di_D/dt, as can be seen from Equation 15

$$\frac{dI_D}{dt} = \frac{V_{G,low}+\frac{I_D}{g_m}+V_{th}}{R_g\frac{C_{iss}}{g_m}+L_s}. \quad (13)$$

By adjusting $V_{G,low}$ to higher value, the current slew rate di_D/dt can be slowed down similarly to the turn-on process. [26] Current slew rate can also be slowed down by selecting a higher value for the external resistor R_g [57].

The turn-off process finishes at the end of current fall period, as the channel is cut and no channel current flows inside the device. However, the input capacitance will continue to discharge during the V_{GS} fall period (Phase 8, t_{10}-t_{11}). [26] The equivalent circuit during Phase 8 is shown in Figure 27.

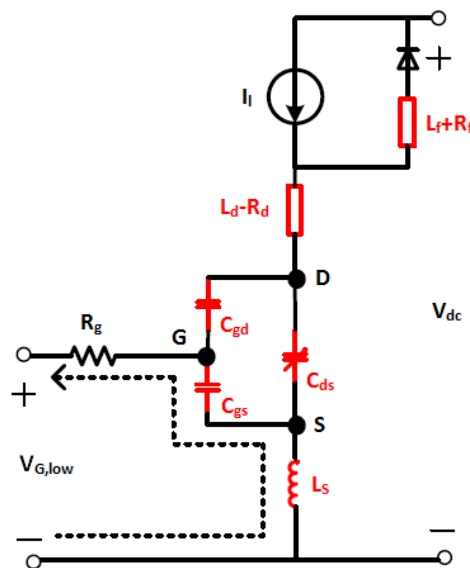

Figure 27. *SiC MOSFET equivalent circuit during turn-off voltage ringing phase. Adapted from [26].*

The inductances L_s and L_D resonate with C_{ds}, which causes the drain-source voltage to oscillate [44]. Oscillation occurs at a natural frequency that can be calculated as $\omega_n = 1/\sqrt{(L_S + L_D + L_f)C_{ds}}$ [26].

The MOSFET does not exhibit a tail current while turning off and this it can be switched off faster than the IGBT. However, the tail current of an IGBT provides natural snubbing during the turn-off, which works to reduce ringing. [29]

4. THE POWER CONVERTER

Power electronics utilize electronic circuits to control the flow of electrical energy. Most common power electronic circuits are rectifiers, DC-AC inverters and AC-DC converters. All these circuits require the usage of large semiconductor devices as switches, magnetic components for energy storage, and special control methods. [42] Power electronics is nowadays seen in many industrial and commercial products. This has been enabled by the rapid development in semiconductor technology and in power switches. [25]

Power electronics evolution has moved towards higher efficiency, higher power density and more integrated systems. Wide bandgap semiconductors have allowed to design devices with faster switching speeds, higher switching frequencies, and for higher temperatures than has been possible to achieve with the conventional Si switches. [48] Higher operation frequency makes it possible to utilize smaller and lighter transformers, filter inductors, and capacitors [42]. However, the fast semiconductor switches and non-linear loads can lead to poor power quality. Poor power quality affects the stability, continuity, and reliability of a power system. [19]

This chapter presents the basic operation of the power converter that is being studied in this thesis and explains how an AC-input voltage is modified in each section of the device in order to achieve a DC-output voltage to feed a bidirectional load. Also, the considerations in driver circuit and magnetic component design are being discussed in Chapters 4.2 and 4.3, respectively. Chapter 4.4 addresses electrical system efficiency.

4.1 Operation of the converter

The purpose of this thesis is to execute a SiC MOSFET upgrade for a power converter that has an output voltage of 370 V_{DC} and output power of 9.6 W. The power module has a three-phase voltage input of 380 – 280 V_{AC} and it comprises of an input filter, an active three-phase rectifier with *power factor correction* (PFC), a buck dc-dc converter, gate drivers, and measurement circuits. The power module feeds a bidirectional load and therefore the active three-phase rectifier with PFC and the buck dc-dc converter operate in both forward and reverse directions. The original version of the device has Si IGBTs as the active components in the PFC rectifier and in the dc-dc converter. The purpose of this thesis is to upgrade the PFC rectifier section of the converter with SiC MOSFETs and to increase the switching frequency in this section.

Simplified block diagram of the device is shown in Figure 28.

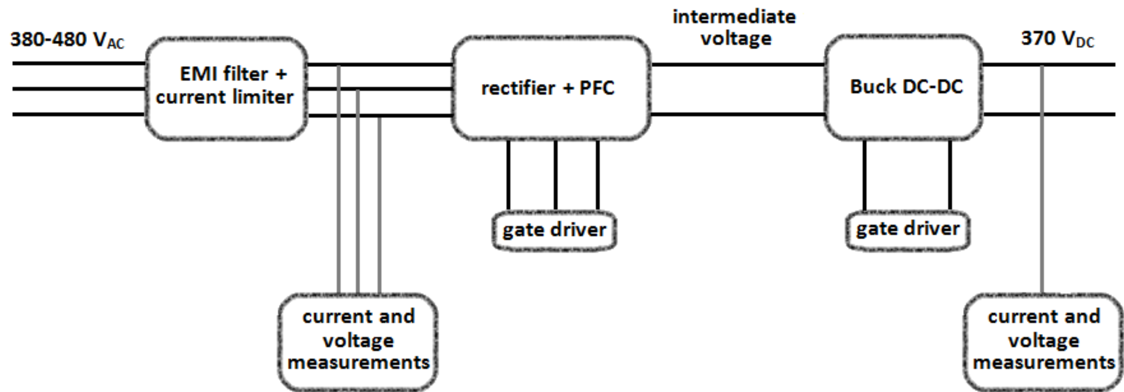

Figure 28. Block diagram of the power module studied in this thesis.

The input section of the power module includes an EMI filter and a current limiter. The active rectifier bridge acts as an AC-DC converter and produces a high intermediate voltage, which is also called the dc-link voltage. This voltage is utilized to charge capacitors that ensure safe operation of the device if the main power is suddenly shut down. The three-phase active rectifier also operates as a PFC and regulates the input current of the device. The buck dc-dc converter regulates the output voltage to the desired level of 370 V_{DC}. The operation principles of power factor correction, active rectifier and buck dc-dc converter are discussed in Chapters 4.1.1–4.1.3.

4.1.1 Power factor correction

Electric power quality is measured by the variation of voltage, current and frequency in a power system [19]. Ideally, the power device presents a load that is purely resistive and the device draws only the minimum real power that is required for its operation from the supply line. [53] In an ideal power device, the system voltages and currents are expected to have pure sinusoidal waveforms of a single frequency [19]. The current of the device would be a replica of its input voltage and exactly in phase with it [53].

However, in actual power systems the voltage and current waveforms of the system comprise of a fundamental component of certain frequency as well as several harmonic components of different frequencies. The harmonic components are called harmonics and they are generated in the power system for several reasons, such as non-linearity, excessive amount of semiconductor switches, and different design constrains. [19] Switched-mode power supplies present a non-linear impedance to the supply line and therefore draw harmonics and apparent power from it [53]. Harmonic components do not deliver any real power to the load and therefore the current harmonics lead to inefficient use of equipment capacity. For example, harmonics can increase the conduction and iron loss in transformers. Harmonics can also cause EMI, insulation failure and mistriggering of relay protection. [42]

Power systems that contain harmonics are said to have poor *power factor* (PF). Power factor gives a measure of how effective the utilization of real power is in a system as well as represents the measure of distortion in the line voltage and current and the phase shift between them. [42] Power factor is given by

$$PF = \frac{real\ power}{apparent\ power} cos\theta, \tag{14}$$

where θ is the phase shift angle between the system current and voltage [42, 53]. Power factor value is 1 if both current and voltage are sinusoidal and in phase. If voltage and current are sinusoidal but not in phase, the power factor is the cosine of the phase angle. [53]

In a power electronic system, the active switching devices cause non-linear behavior and the input voltage ($v_s(t)$) and the system current ($i_s(t)$) have a phase shift between them. Phase shift between $v_s(t)$ and distorted $i_s(t)$ is illustrated in Figure 29. [42]

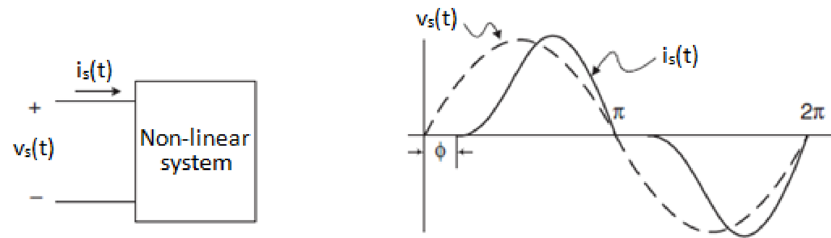

Figure 29. *Phase shift between the system current and the input voltage of a non-linear power system with active switching devices. Adapted from [42].*

Power factor correction seeks to force the input current to be sinusoidal as well as in phase with the input voltage [40]. It shapes the input current in order to maximize the real power available from the power line [53]. The purpose of the PFC is also to generate well-regulated dc output voltage [40]. The PFC circuit usually stores the excessive input energy in inductive and capacitive components of the circuit when the instantaneous input power ($p_{in}(t)$) is larger than the average input power (P_{in}) of the power system. Correspondingly, the PFC releases the stored energy when $p_{in}(t)$ is less than P_{in}. The PFC studied in this thesis operates in a *two-stage scheme*. The operation principle of the two-stage scheme PFC is illustrated in Figure 30. [42]

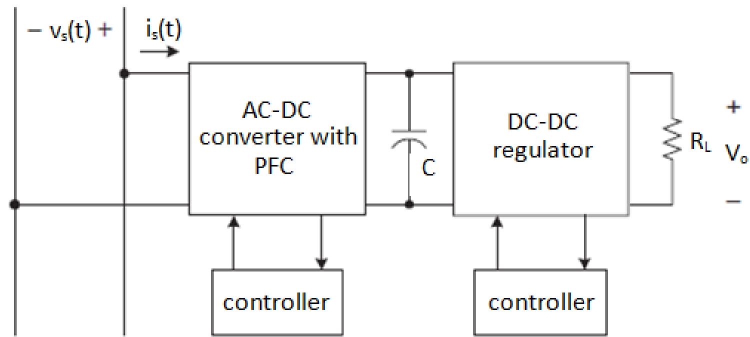

Figure 30. *Two-stage scheme PFC configuration of a power supply. Adapted from [42].*

In the two-stage scheme, a non-isolated PFC converter is connected to the supply line to create an intermediate dc bus voltage. This bus voltage is typically full of harmonic ripple and a dc-dc regulator is cascaded with the PFC to provide electrical isolation and tight voltage regulation to the load. These two power stages can be controlled separately and thus both converters can be optimized individually. The two-stage scheme has quite low efficiency, since it processes the input power twice and has complex control circuits, higher cost and low reliability. Other common system configurations are *one-stage scheme*, that combines the PFC circuit and the power conversion circuit in one stage, and *parallel scheme*, where the power from the supply line flows to the load through two parallel paths. One-stage scheme and parallel scheme are not studied further in this thesis. [42]

Power factor correction can be achieved through both active and passive circuits. Active PFC circuits include active components, such as transistors and integrated circuits, while passive PFC circuits can attenuate the current spikes and spread the current out well enough with a single inductor. The effects of passive and active PFC on the input current waveform are shown in Figure 31. [53]

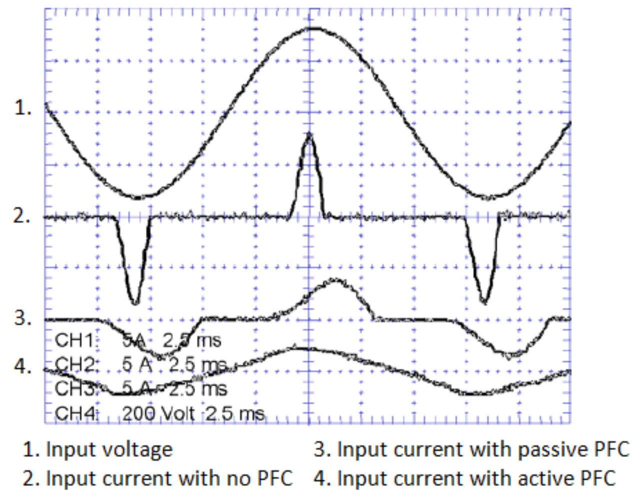

Figure 31. *Input waveform characteristics of a power supply with different PFC types. Adapted from [53].*

Waveform 1 in Figure 31 shows the input voltage of a power supply and waveform 2 presents the input current of the device without power factor correction. The input circuit of a power supply usually consists of a rectifier that is followed by a storage capacitor. The storage capacitor can maintain the peak voltage of the input sine wave until the next peak comes to recharge the capacitor. As can be seen from Figure 31, current is drawn from the supply line only at the peaks of the input waveform. This current pulse must contain enough energy to sustain the load until the next peak. In the case shown in Figure 31, the input current and voltage are in phase, but the current waveform has significant distortion. [53]

Waveform 3 shows the input current waveform with passive PFC. Passive methods in PFC design have been used in power supplies where large size and weight of the inductive components are not critical. At higher power levels the utilization of these large inductors becomes impractical and active PFC is preferred. Waveform 4 in Figure 31 shows the input current waveform with active PFC. The peak current level in passive PFC (waveform 3) is 33 % higher than the peak current with active PFC (waveform 4). Active PFC has been favored in recent years due to market trends, such as rising cost of copper and magnetic core material as well as falling costs of semiconductors. [53]

4.1.2 Active rectifier

The power electronics supply from the three-phase ac supply voltage is usually carried out in two stages: the mains AC-voltage is first rectified into a dc-voltage and then adapted to the desired load voltage level with a dc-dc converter. The rectification can be achieved by simple unidirectional three-phase diode rectifiers with capacitive smoothing of the output voltage. This *passive rectification* utilizes no control, sensors, auxiliary supplies or EMI filtering, thus having low complexity and high robustness. Passive rectifiers have an unregulated output voltage that is directly dependent on the mains

voltage level. With *active rectifier* systems, the output DC-voltage of the rectifier can be controlled to a constant value independent of the actual mains voltage. Active voltage regulation can be achieved with a six-switch converter structure that is presented in Figure 32. The six-switch AC-DC bridge circuit is often applied for supplying the DC-link voltage of variable speed drives. [31]

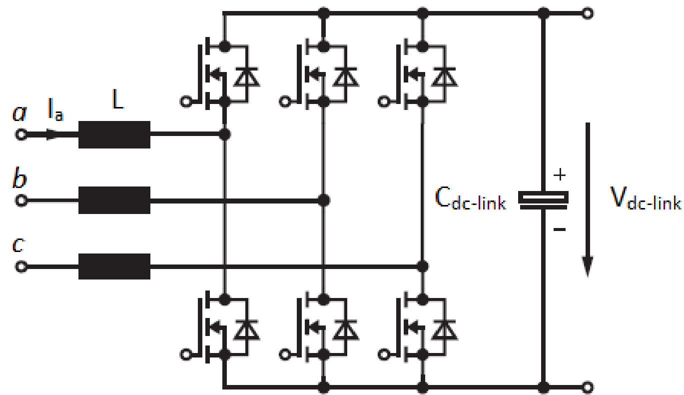

Figure 32. *A bidirectional active PFC rectifier. Adapted from [31].*

The semiconductor switches that are utilized in the six-switch rectifier can be turned to on-state or to off-state whenever required. The commutation of the switches and their gate-turn-off capability allows full control of the converter. [42] These controlled rectifiers can be implemented for reversal operation, where the circuit operates as an inverter and feeds energy back into the mains. The inverter operating mode is often utilized in variable speed drives during braking. [31]

There are two types of controlled rectifiers: current source and voltage source rectifiers. In a current source rectifier, the power reversal is achieved by reversing the voltage, while in a voltage source rectifier the power reversal is achieved by reversing the current. The voltage source rectifier is most widely utilized and also addressed in this thesis. [42] The voltage source rectifier keeps the dc-link voltage at the desired level by using a feedback control loop. For the feedback the dc-link voltage ($V_{dc\text{-}link}$) is measured at the capacitor and compared with a reference voltage (V_{ref}). The error between $V_{dc\text{-}link}$ and V_{ref} is applied to drive the rectifier switches on or off. [42] Current paths in the voltage source rectifier are illustrated in Figure 33 for the rectifier operation mode.

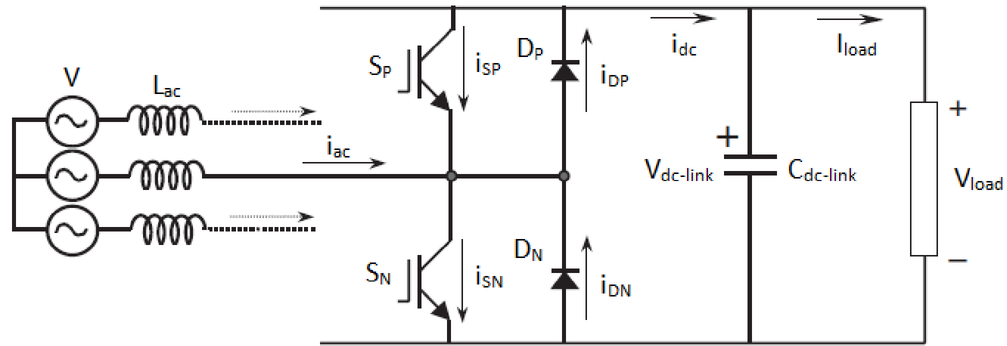

Figure 33. *Current paths presented for one phase of a six-switch active rectifier. Adapted from [42].*

The circuit operates in rectifier mode when the DC-link current (i_{dc}) is positive and the capacitor $C_{dc\text{-}link}$ is being discharged. During the rectifier operation, the error signal asks the control block for more power from the supply line according to the difference between $V_{dc\text{-}link}$ and V_{ref}. The required power is taken from the supply line by generating appropriate drive signals for the six semiconductor switches. As a result more current flows from the AC-side (i_{ac}) and the capacitor is charged again. During the inverter operation mode, current i_{dc} is negative and $C_{dc\text{-}link}$ is overcharged. The error signal asks the feedback loop to discharge the capacitor and to return power to the mains. [42]

The switches are controlled with periodical *pulse width modulation* (PWM) signals. The error signal between $V_{dc\text{-}link}$ and V_{ref} is used to generate a template waveform that produces the PWM signal. The template should be a sinusoidal waveform with the same frequency of the mains. The fundamental of the PWM pattern is a voltage (V_{MOD}) with the same frequency of the template. By controlling the magnitude and phase of V_{MOD} with respect to the mains, the operation of the rectifier can be controlled. Changing V_{MOD} through the PWM pattern is illustrated in Figure 34. [42]

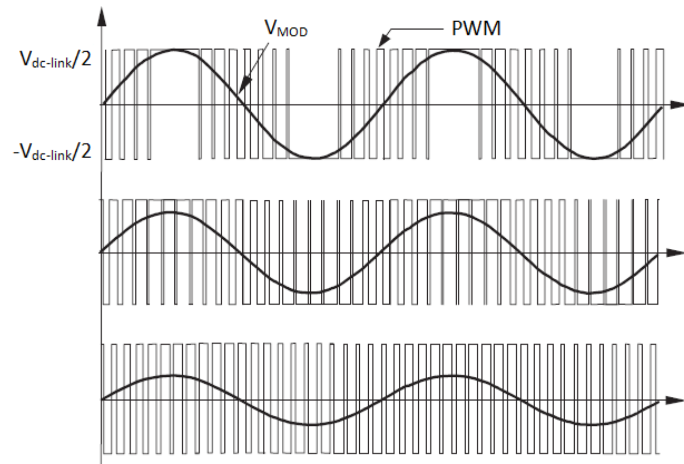

Figure 34. *Example of changing the V_{MOD} through the PWM pattern. Adapted from [42].*

As can be seen from Figure 34, changing the PWM pattern modifies the magnitude of V_{MOD}. The phase of V_{MOD} can be modified by displacing the PWM pattern. [42]

During the positive half cycle of V_{MOD} the negative side transistor S_N shown in Figure 34 is switched on and i_{ac} begins to flow through the transistor (i_{SN}). This current returns to the mains and comes back to the switches, closing a loop with another phase and passing through diode D_N that is connected to the same negative terminal. The current can also go to the load and return through the positive side transistor (S_P). When the transistor S_N is switched off, the current path is interrupted and begins to flow through the positive side diode (D_P, i_{DP}). i_{dc} charges the capacitor $C_{dc\text{-}link}$ and allows the rectifier to produce dc-voltage. Inductance L_{ac} is important for the rectifier process, because it generates an induced voltage that allows the diode D_P to conduct. The current waveforms for the positive V_{MOD} half cycle are presented in Figure 35. [42]

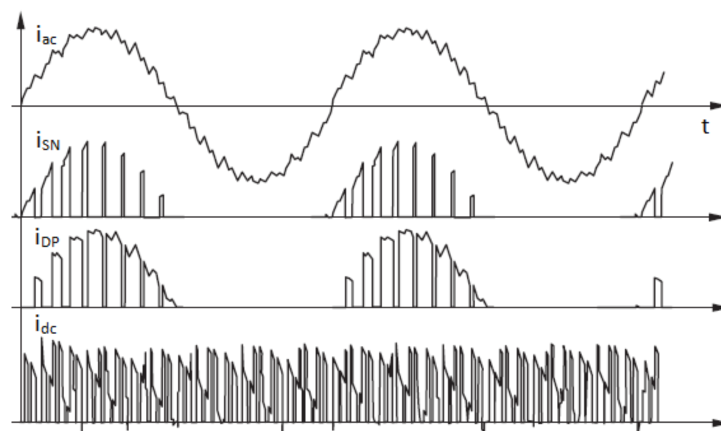

Figure 35. *Six-switch active rectifier current waveforms through the mains, the switches and the DC-link. Adapted from [42].*

As can be seen from Figure 35, the dc-side current is composed by controlling the negative and positive side switches on and off according to the changes in the AC-side

current. Similar operation occurs during the negative half cycle of V_{MOD}. During the negative half cycle the current flows either through S_P or D_N. [42]

When the rectifier operates in inverter mode the currents flowing through the transistors come mainly from $C_{dc\text{-}link}$. In order to have full control over the rectifier, the six diodes must be polarized negatively at all voltage supply values. Negative polarization is achieved by ensuring a dc-side voltage that is higher than the peak dc-voltage generated by diode rectification. This way the diodes will conduct only when at least one of the transistors is switched on. [42]

PWM control can manage both real and apparent power, which allows voltage source controlled rectifier to operate as a PFC circuit. Since also the current and voltage waveforms of the rectifier can be modulated through PWM control, the AC-current waveforms can be maintained almost sinusoidal, which reduces harmonics to the mains. [42] Active rectifiers are often preferred in applications that operate in regenerative mode such as cranes, elevators or wind turbines. The field of applications for the active rectifiers is limited by the high cost of power switches and control software. Also, the high switching frequency increases the control complexity of the system. [33]

4.1.3 Bidirectional buck DC-DC converter

DC-DC converters are utilized to convert a dc input voltage into a lower or higher dc output voltage, to regulate the dc output voltage against load and line variations, and to reduce the ac voltage ripple on the dc output voltage. The DC-DC converter can also provide isolation between the input and the load thus protecting the supplied system and the input source from EMI. [42]

In the power system that is studied in this thesis, a buck converter is implanted after the three-phase rectifier with PFC to regulate the output voltage to a desired level. This converter operates in both forward and reverse directions. Operation in reverse direction is utilized during regenerative breaking. The converter operates in buck mode when the power flow is towards the load and in boost mode when the power flow reverses towards the mains.

The buck converter is also called a step-down converter as it produces lower output voltage compared to the input voltage. Boost converter creates an output voltage that is always greater than the input voltage and is often called a step-up converter. With a step-down/step-up converter it is possible to create an output voltage that is either higher or lower than the input voltage respectively. [36] Simplified schematic of a bidirectional boost converter is presented in Figure 36.

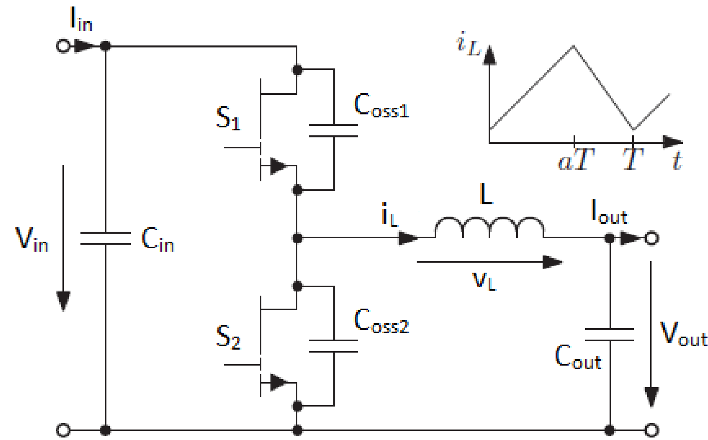

Figure 36. *Bidirectional buck converter topology. Adapted from [45].*

The buck converter illustrated in Figure 36 operates in buck mode when the upper switch S_1 is conducting. Voltage across inductor L is positive according to $V_L = V_{in} - V_{out}$ and the inductor current (i_L) will increase linearly. Power flow is towards the load. When S_1 turns off, i_L continues to increase and charges the capacitor C_{oss1}. When voltage across S_1 is decreased to zero at time interval aT, i_L reaches its maximum value. [20]

After aT, the body diode of the lower switch S_2 turns on naturally and the voltage over S_2 is clamped to zero. Voltage across the inductor L equals V_{out} and i_L begins to decrease linearly. Power flow is towards the mains and the converter operates in boost mode. S_2 is turned on and i_L continues to decrease until it becomes negative and S_2 turns off. After S_2 is turned off, the inductor current begins to charge C_{oss2}. When the voltage across S_2 is decreased to zero at time interval T, i_L reaches its minimum value. After the boost period is over, the body diode of S_1 turns on naturally and the voltage over S_1 is clamped to zero. S_1 is turned on and the converter comes into next switching period. [20]

In order to avoid short circuits of the voltage source, a *dead tim*e is required between the signals that control the switches on and off. During the dead time none of the switches are conducting and current flows through one diode. Dead time influences the relationship between output voltage, input voltage and duty cycle. [15]

This thesis does not focus on the operation of the buck DC-DC converter as the semiconductor switches and the switching frequency of this part of the device are kept unchanged.

4.2 Driver circuit

A driver circuit is required to switch a semiconductor switch from its off-state to on-state and vice versa. It is desirable that the switching device traverses rapidly through the linear operation region, where both the drain-source voltage and the drain current of a MOSFET are high and the instantaneous power dissipation is large. [36] Ideally the semiconductor

switches would operate only in cut-off or saturation regions and the turn-on and turn-off times would be minimized. Gate driver supplies the gate charge needed for the power device to turn-on and off. Voltage controlled devices, such as IGBTs and MOSFETs, also require a constant voltage on the gate terminal in order to remain the conducting channel. [42]

The driver circuit is an interface between the control PWM signal and the power semiconductor switch. It amplifies the control signal and provides electrical isolation between the sensitive logic-level signals and higher power levels. [36] In analog driver circuits the isolation can be achieved through optical isolation or transformer isolation [42]. IC gate drivers apply silicon isolation technology [5].

As both Si IGBT and SiC MOSFET have the MOS-gate structure, the gate driver of the Si IGBT can be exploited for the SiC MOSFET. However, the differences in device physics need to be considered during the gate driver development. SiC MOSFETs have lower total gate charge Q_g, which permits lower power consumption in the gate driver. [47] As was discussed in Chapter 2.3.1 ,the channel resistance in the SiC MOFET is larger than in the Si device, thus the SiC MOSFET needs to be driven with a higher gate voltage [57]. SiC devices are often physically smaller compared to Si IGBTs with similar ratings. This means that the driver circuit has less time to detect and interrupt a short circuit condition safely. Driving the SiC MOSFET at high voltage levels minimizes switching losses and improves the surge current rating for the device, but it also puts a greater voltage stress on the gate terminal. This can affect the long-term reliability of the device. [29]

SiC MOSFETs have usually low gate threshold voltages. In high-speed applications the parasitic components together with fast current and voltage rates can cause switching oscillations at the gate terminal during the turn-off process. This oscillation can cross the rated V_{th} of the SiC MOSFET and result in unwanted conduction while the device is switching off. The SiC MOSFETs are often provided with negative gate voltage during the turn-off process to prevent the false turn-on. The negative gate voltage also improves the switching device's noise immunity during the off-state. [39]

The turn-on and turn-off characteristics of a power switch can be controlled by external gate resistances $R_{g,on}$ and $R_{g,off}$ of the driver circuit. As was discussed in chapter 3.2, the rapid current change during the turn-on and turn-off processes cause oscillations and overshoot as the rapidly changing current is coupled with the parasitic inductances of the device and the driver circuit. Current slew rate can be slowed down by selecting higher values of $R_{g,on}$ and $R_{g,off}$, which results in lower surge voltages and in limited voltage ringing. However, as *di/dt* is slowed down also the turn-on and turn-off delay times increase, which results in higher switching losses. [57] Figures 37 and 38 show the turn-off waveforms of a SiC MOSFET with two different gate resistor values.

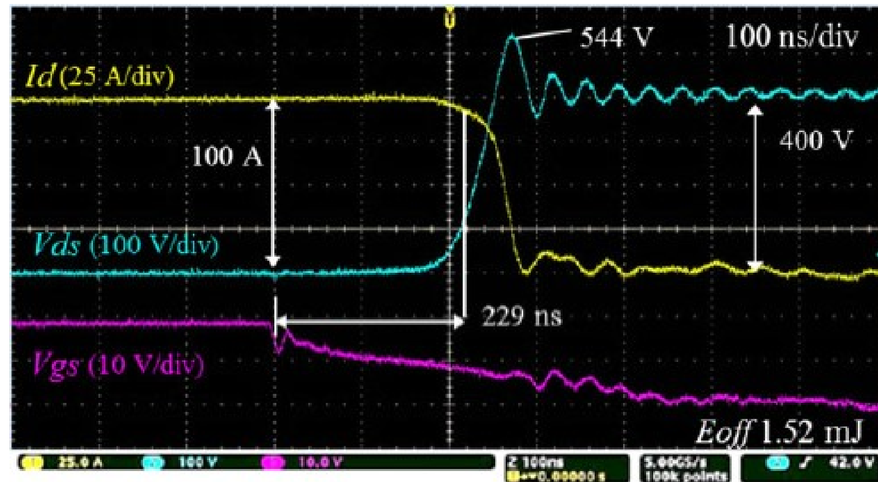

Figure 37. *Turn-off waveforms of a SiC MOSFET with $R_{g,off}$ = 6.2 Ω. High gate resistance value results in moderate surge voltage and in limited ringing. Turn-off delay is 229 ns. [57]*

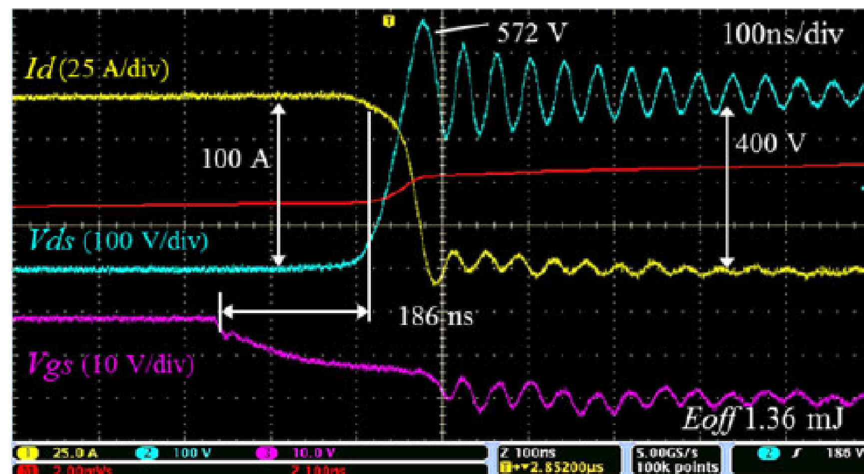

Figure 38. *Turn-off waveforms of a SiC MOSFET with $R_{g,off}$ = 3.9 Ω. Low gate resistance value results in fast switching, higher surge voltage and in current and voltage oscillations. Turn-off delay is 186 ns. [57]*

Figures 37 and 38 show the turn-off waveforms of a SiC MOSFET with a conventional analog gate drive method for two different $R_{g,off}$ values. Figure 37 shows the turn-off waveforms for a higher gate resistor value (6.2 Ω) and Figure 38 for a lower gate resistor value (3.9 Ω). It can be noticed, that the turn-off process proceeds slower with a higher gate resistor value. The turn-off delay with a higher $R_{g,off}$ value is 229 ns and 186 ns with a lower $R_{g,off}$ value. The difference in turn-off delays is 43 ns. There is also a notable difference in the surge voltages of the devices. The drain-source surge voltage is 28 V lower with $R_{g,off}$ = 6.2 Ω (544 V) than with $R_{g,off}$ = 3.9 Ω (572 V). It can also be noticed, that the voltage fluctuation is limited with a higher gate voltage value. There is a clear tradeoff between the switching losses and EMI challenges of a power device that should be carefully studied in order to optimize the driver design [29]. Gate driver design is

critical so that the full potential benefits of SiC devices in an actual converter can be utilized [23].

In high-frequency applications the parasitic components of the gate driver circuit have a significant impact on power device switching together with the parasitic components of the semiconductor device. Stray inductances from the driver circuit can be minimized with proper layout. The driver circuit should be located very close to the MOSFET. A Kelvin source connection is recommended for the switching device, since the high drain current *di/dt* can couple back into the gate drive through any common source inductance. This can cause significant ringing in the gate loop. The gate and source paths should ideally both be copper planes on opposing layers in order to minimize the stray inductance. [29]

4.3 Magnetic components

Magnetic components, inductors and transformers, are an important part of most power electronics converters. They are often designed and constructed for a particular application. [36] The trend in power supplies is towards miniaturization. The ability to manufacture small and efficient magnetic components is critical in order to achieve high power density since high-frequency transformers determine approximately 25% of the overall device volume and 30% of the overall weight. Reduction in the size of magnetic components is often achieved by high frequencies in switching circuits. [25]

The volume of a transformer could be reduced significantly by increasing the switching frequency. The product of transformer core area (A_{core}) and winding area (A_{Cu}) is a stand for transformer volume. Area product (A_p) is often used instead of volume when the transformer size is optimized. The area product can be calculated as $A_p = A_{core} * A_{Cu}$. [25]

The cross-section area of the transformer core is obtained by Faraday's law

$$A_{core} = \frac{V_1}{2\pi N_1 f B_{pk}}, \tag{15}$$

where V_1 is the primary voltage, N_1 is the number of primary turns and B_{pk} is the peak flux density of the magnetic material. The cross-sectional areas of primary and secondary copper windings are determined by choosing a current density (j) that is assumed to be equal at both windings. The winding area can be calculated as

$$A_{Cu} = \frac{N_1 I_1 + N_2 I_2}{K_u j}, \tag{16}$$

where N_1 and N_2 are the numbers of primary and secondary turns respectively, I_1 and I_2 are the primary and secondary currents respectively, and K_u is the copper fill factor which depends on the wire type and size, insulation requirement, and winding technique. [54]

Combining (17) and (18) yields

$$A_p = \frac{E_1 I_1 + E_2 I_2}{K j f B_{pk}}, \quad (17)$$

where $K = 2\pi K_u$ [25]. From (16) can be seen that increasing the switching frequency will decrease the area product and thus decrease the transformer volume. The relationship between the transformer area product and operating frequency can be evaluated by (16) as long as B_{pk} and j are known. B_{pk} and j should be chosen according to transformer size in order to meet overall efficiency and temperature rise since B_{pk} is directly related to core loss density and j to copper loss density. [54]

Transformer core loss (P_{core}) is a result of three loss mechanisms: hysteresis, eddy current and stray losses. All these core losses are a function of frequency and peak flux density. Therefore, they can be approximated by

$$P_{core} = c V_{core} f^x B_{pk}^y, \quad (18)$$

where V_{core} is the volume of the core and c, x and y are coefficients relating to materials. [25] Figure 39 shows the dependence of core losses on the peak flux density for several switching frequencies. The core that is studied in Figure 39 is a MnZn ferrite core.

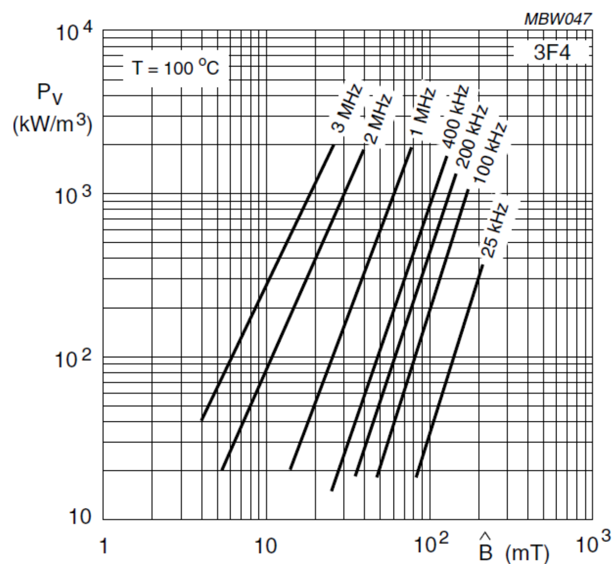

Figure 39. *Core power loss as a function of peak flux density for several switching frequency values [12].*

It can be clearly noticed from Figure 39 that increasing the peak flux density of a transformer increases the core loss significantly. P_V is the specific power loss for the volume of the core. Higher peak flux density values with low core loss can be achieved with higher switching frequencies.

Transformer copper losses (P_{Cu}) can be approximated by

$$P_{Cu} = R_1 I_{rms1}^2 + R_2 I_{rms2}^2, \tag{19}$$

where R_1 and R_2 are copper wire resistances at primary and secondary windings respectively. [25]

Figure 40 shows transformer core volume as a function of switching frequency for three MnZn ferrite cores 3C96, 3F4 and 3F45.

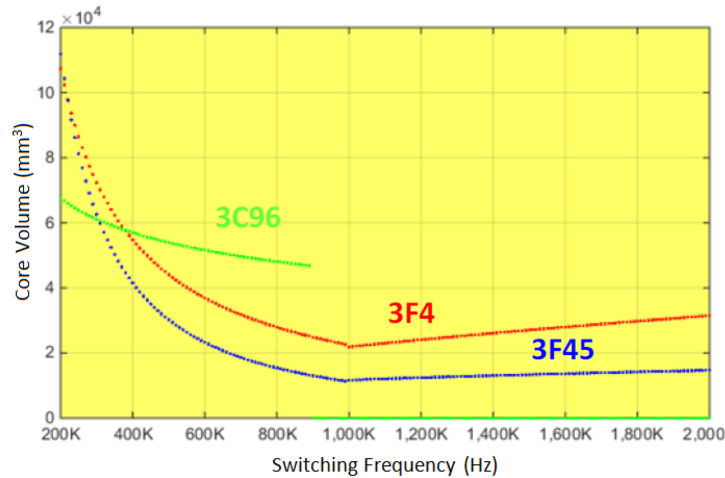

Figure 40. *Transformer core volume as a function of switching frequency. Adapted from [44].*

It can be noticed from Figure 40 that for 3F4 and 3F45 the core volume decreases rapidly with increasing frequency especially at switching frequencies from 200 kHz to 600 kHz. Core volume decreases until the switching frequency is increased to 1000 kHz. After this point the core size must be increased in order to obtain efficiency and thermal limits since both core and copper loss increase with frequency.

Higher switching speed allows smaller size also with other magnetic components than transistors, such as in filter inductors. If everything in the electrical system is kept unchanged and the switching frequency is doubled, the durations of the on-time (t_{on}) and off-time (t_{off}) will halve. Voltseconds is the applied voltage multiplied by the time that it is applied for: $voltseconds = V_{on} * t_{on}$. This means that if t_{on} and t_{off} halve, also the voltseconds will halve. [17]

Inductor ripple current (ΔI) is defined by

$$\Delta I = \frac{V\Delta t}{L}. \tag{20}$$

From Equation (19) can be seen that ΔI is defined as voltseconds per inductance, thus inductor current ripple will also halve if the switching frequency is doubled. The inductor current has also an average DC-level (I_{dc}) around which the current ripple swings. If the system input or output voltages do not change, changes in the inductance, switching

frequency, or duty cycle does not affect I_{dc}. Inductor current ripple and DC-level current builds up the inductor peak current (I_{pk}) according to $I_{pk} = \Delta I + I_{dc}$. [17]

Current ripple ratio (r) is a geometrical ratio that compares the inductor current ripple to its associated DC-value according to

$$r = \frac{\Delta I}{I_L} = \frac{I_{ac}}{I_{dc}}. \quad (21)$$

Further, since I_{dc} does not change when the frequency is changed, but ΔI will halve if the frequency is doubled, r will also halve. For example, if we have started off with $r = 0.4$, we would now have $r = 0.2$. If the current ripple ratio is returned to the calculated optimum value of $r = 0.4$, ΔI needs to be doubled to its original value. According to Equation (19), this can be achieved by halving the inductance. Therefore, it can be generally stated that inductance is inversely proportional to frequency. As a result, r, I_{dc}, and ΔI are unchanged. [17]

The size of an inductor can be thought of being proportional to its energy-handling capability that must be at minimum the energy that is needed to be stored in the power system. It can be calculated as

$$\textit{Energy-handling capability} = \frac{1}{2} * L * I_{pk}^2. \quad (22)$$

As a conclusion, if the switching frequency is doubled, I_{pk} is unchanged, and L is halved, the energy-handling requirement that roughly corresponds to the size of the inductor has halved. It must be noted that since the peak current is unchanged, also the required current rating of the inductor is independent of the frequency. [17]

The progress in wide bandgap semiconductors will lead to a further miniaturization of power electronic systems [24]. The optimum choice of magnetic core material is not straight forward since it is influenced by several design parameters associated with the converter topology as well as core material properties, such as frequency, current ripple, saturation flux density, and operating temperature. Magnetic materials that are currently applied in power converters include silicon steel, ferrite, iron powder and tape wound amorphous/nanocrystalline materials. [13] However, for example the standard MnZn ferrite cores are limited by their dominating eddy current losses and the resulting heat dissipation. The increase in switching frequencies requires also improved ferrite materials with lower losses and transformer design with unique construction technologies. [24]

4.4 Efficiency

The development of power supplies has been driven by a constant demand for power density increase and a decrease in relative costs over the last few decades. The challenges in the development of new systems are in maintaining and improving a previously

attained power density while simultaneously assuring high efficiency over the entire range of output power. [30]

Electrical system efficiency (η) is defined as a ratio of output power *(P_{out})* to the input power (P_{in}) according to

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out}I_{out}}{V_{in}I_{in}} \text{ [42].} \tag{23}$$

Figure 41 shows the development of the rated power efficiency of telecom rectifier modules and photovoltaic (*PV*) inverter systems over the last two decades.

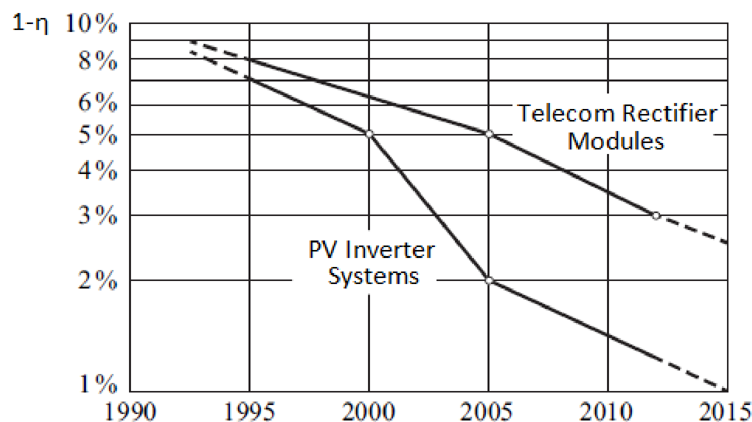

Figure 41. *Development of the rated power efficiency of telecom power supply modules and PV inverters since 1995. Adapted from [30].*

As can be seen from Figure 41, raising the efficiency has become a primary development goal in the power supply industry. Telecom rectifier modules are reaching efficiency of 0.97 and PV inverter systems are rapidly reaching 0.99 efficiency. [30]

Typically, three loss components are occurring for a power electronic system: $P_{V,0}$ that is independent of the output power, $P_{V,1}$ that is linearly dependent on the output power and $P_{V,2}$ that is current dependent. The loss component $P_{V,0}$ is caused by the power consumption of auxiliary systems, such as measuring and control electronics, and blowers for cooling. There are also contributions from capacitive switching losses of the power semiconductors and from core losses of the input inductor. $P_{V,1}$ is linearly dependent of the output power and is caused by power semiconductors with largely current independent forward voltage drop (bipolar semiconductors) and by approximately linearly current dependent switching losses. The loss component $P_{V,2}$ describes the ohmic loss components. Typical examples of the ohmic losses are MOSFET conduction losses, winding losses of the magnetic components, and losses in electrolytic capacitors. [30] SiC MOSFET conduction losses can be expected to be lower than the Si IGBT conduction losses due to the lower $R_{DS(on)}$ value [16]. Also, MOSFETs can be assumed to have lower switching losses than the bipolar IGBT devices since they do not have any minority carriers stored in the device structure that would slow down the switching processes [36].

Besides the low switching loss, the remarkable advantage for SiC MOSFETs in bidirectional three-phase rectifiers is that the conduction loss of the freewheeling diode, which carries most of current in rectifier circuit models, can be largely improved with SiC MOSFET channel reverse conduction. [46] In reverse conduction, a reverse channel of a SiC MOSFET is turned on when $V_{gs} > 0$, $V_{ds} < 0$, and $I_d < 0$. In this operation mode a reverse drain current can flow through the MOSFET channel. Also, the MOSFET body diode conducts reverse current from the source terminal to the drain terminal. However, conducting capability of the body diode is much weaker than the reverse channel conducting capability due to its higher on-state voltage drop and on-state resistance. The utilization of the body diode is unavoidable since dead time is required between the upper and the lower switches. [55]

In a three-phase active rectifier system, the phase current (i_{ph}) is below zero during half of the fundamental period. This means that when the control signal of the rectifier leg is set high, the current of the upper switch becomes negative. In a bidirectional IGBT circuit, this reverse current flows through the freewheeling diode. SiC MOSFETs show a reverse conduction capability, which means that the reverse current of the switch is shared between the FWD and the reverse conducting transistor. The distribution of the forward and reverse currents between the switching transistor and the FWD are illustrated in Figure 42 for a Si IGBT and a SiC MOSFET. [28]

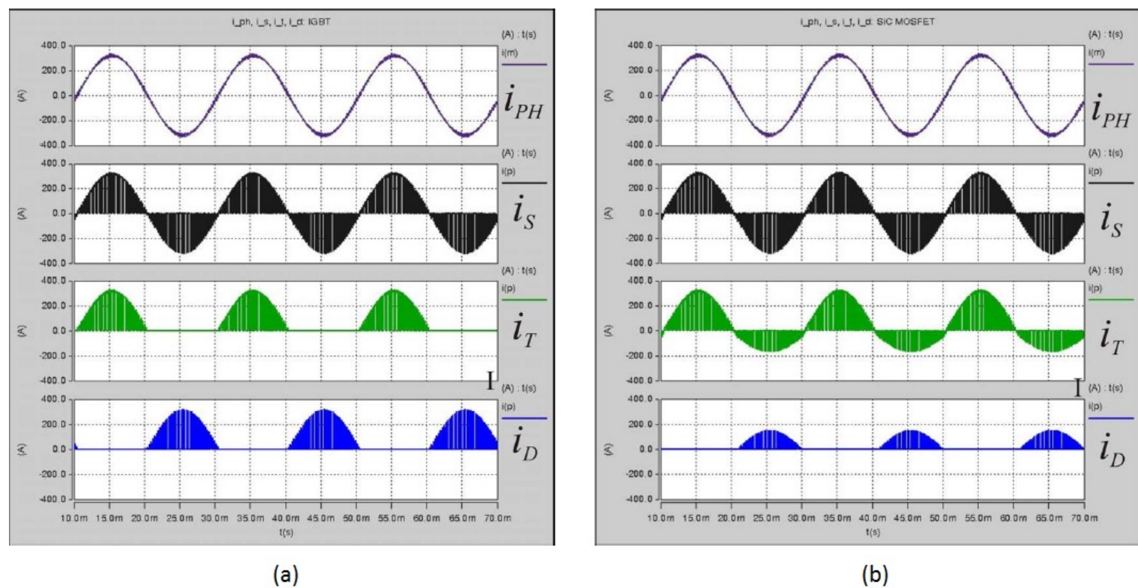

Figure 42. *Simulated current waveforms of a Si IGBT (a) and a SiC MOSFET rectifier (b). Adapted from [28].*

Figure 42 shows the phase current (i_{ph}), switch current (i_S), transistor current (i_T) and FWD current (i_D) of a rectifier leg. Figure 42 (a) presents the current waveforms with Si IGBT switches and Figure 42 (b) with SiC MOSFETs. During the period that the current in the switch is positive, only the semiconductor switch is conducting half of the fundamental period in both cases. The power losses are due to the channel resistance of

the power switches during this period. Second phase occurs when the switch current turns negative. In the Si IGBT circuit the FWD begins to conduct the reverse current. In the SiC MOSFET circuit the voltage drop across the reverse conducting transistor is lower than the threshold voltage of the FWD and the diode current remains zero. In the third phase, the threshold voltage of the FWD is exceeded in the SiC MOSFET circuit, and the switch current is shared between the diode and the transistor. Figure 42 (b) shows that the FWD dissipates conduction power losses only in the third phase for short periods of time. [28] However, the reverse recovery behavior of the SiC MOSFET is a small portion of the switching losses in a rectifier system [55].

Main properties that can be assumed to have an impact on the device efficiency when Si IGBTs are replaced by SiC MOSFETs are collected in Table 3.

Table 3. *Effects on device efficiency when Si IGBTs are replaced by SiC MOSFETs [16, 28, 29, 36, 41].*

Property	Si IGBT	SiC MOSFET	Effect on efficiency, when Si IGBTs are replaced by SiC MOSFETs
$R_{DS(on)}$ value		2000 smaller than for Si for the same breakdown voltage	Higher efficiency: smaller on-state conduction losses
Charge carrier type	Bipolar device, minority carriers need to be removed through recombination and stored again during the switching processes	Unipolar device, the only charges that need to be removed in the switching processes are from device parasitic capacitances	Higher efficiency: faster switching, lower switching losses
Thermal conductivity	1.5 W/cm*K	3-4 W/cm*K, better heat dissipation, smaller components and heat sinks	Higher efficiency: smaller parasitic elements, higher switching speeds, less cooling elements
Reverse conduction	Only through an external freewheeling diode	In bidirectional operation part of the reverse current can go through the MOSFET channel in reverse direction	Higher efficiency: reverse current shared between the diode and the transistor
Switching frequency	Limited	Higher than with Si IGBT. Smaller inductive components, smaller inductor losses. Parasitic elements can affect significantly the switching waveforms.	Higher efficiency: smaller inductor losses Lower efficiency: tradeoff between slower switching times and EMI challenges

In this thesis work, only the effects of replacing Si IGBTs with SiC MOSFETs and the effects of increased switching frequency on the power converter efficiency are being studied. External structures such as gate resistors, input inductors or device layout are not optimized from the original converter.

5. SELECTING THE COMPONENTS

The main advantage of wide band gap semiconductors is their low on-resistance even when they are designed for high voltages [16]. SiC devices are able to work at high temperature, voltage, and frequency while they produce less power losses than the conventional Si power switches. SiC MOSFETs enable designing high-voltage and high-frequency converters. [52]

The original power converter studied in this thesis was executed with Si IGBTs as the power switches. During the thesis work, the Si IGBTs in the three-phase rectifier with PFC were replaced by SiC MOSFETs. The effects of this upgrade on switching waveforms and on the total efficiency of the converter were studied. The efficiency of the converter was also studied with increased switching frequencies. The driver IC of the switching components needed to be changed since the SiC MOSFETs require a larger gate voltage than the original Si IGBTs and a negative gate voltage during the off-state.

5.1 SiC MOSFET

The Si IGBTs were replaced with the SiC MOSFETs with minimal changes made to the original converter. In the original three-phase rectifier the switching components were Si IGBTs *IRGP30B120* from International Rectifier. This component is a three-pin device in a TO-247 package. It was desirable that the SiC MOSFETs would have the same package than the Si IGBTs. However, also a four-pin TO-247 package was an option, since the additional Kelvin source connection would reduce the common mode inductance of the power switch.

The voltage rating of the SiC MOSFET had to correspond the voltage rating of the Si IGBT ($V_{CE} = V_{GE} = 1200$ V) and the rated drain current of the SiC MOSFET needed to be between 20 and 40 A, since the collector current of the Si IGBT was rated at 25 A at room temperature.

All the SiC MOSFETs that were available with these ratings were listed and their datasheet values, availability and price was compared. SiC MOSFETs from five manufactures (Cree, ROHM, Microsemi, ON Semiconductor and Infineon) were selected for further comparison. Datasheet values of the Si IGBT and the SiC MOSFETs are compared in Chapters 5.1.1 *Basic information and maximum ratings*, 5.1.2 *Switching characteristics*, and 5.1.3 *Body diode characteristics*. Argumentation for the final selection of the SiC MOSFET is given in Chapter 5.1.4 *Selecting the SiC MOSFET*.

5.1.1 Basic information and maximum ratings

The package, breakdown voltage and rated current were the first features that limited the selection of the SiC MOSFETs. Suitable components were found from five manufacturers: Cree, ROHM, Microsemi, ON Semiconductor and Infineon. SiC MOSFETs *APT25SM120B* from Microsemi, *SCT3080KL* from ROHM, and *C3M0075120K* from Cree were selected for further comparison and evaluation. The properties of the SiC MOSFETs were also compared with the original Si IGBT *IRGP30B120* from International Rectifier. SiC MOSFETs from ON Semiconductor and Infineon were still under development, thus their datasheets were confidential and could not be shared in this thesis work.

Basic device information and some maximum ratings of the selected SiC MOSFETs are listed in Table 4. Symbols before the slash (/) in the symbol column implies for the Si IGBTs. Symbols after the slash implies for the SiC MOSFETs.

Table 4. *Basic information and maximum ratings of the switching components. Values are measured at 25°C. [1, 4, 7-9]*

	IGBT, Infineon, *IRGP30B120KD*	MOSFET, ROHM, *SCT3080KL*	MOSFET, Microsemi, *APT25SM120B*	MOSFET, Cree, *C3M0075120K*	MOSFET, Cree, *C2M0080120D*
V_{CE}/V_{DS}	1200 V	1200 V	1200 V	1200 V	1200 V
I_C/I_D	25 A	31 A	25 A	30 A	36 A
$V_{CE(on)}$	2.28 V	-	-	-	-
$R_{DS(on)}$	-	80 mΩ	140 mΩ	75 mΩ	80 mΩ
T_J	-55°C to +150°C	-55°C to +175°C	-55°C to +170°C	-55°C to +150°C	-55°C to +150°C
Package	TO-247	TO-247	TO-247	TO-247-4	TO-247

As can be seen from the component information in Table 4, all the selected components have a breakdown voltage of 1200 V and their rated I_D is between 20 and 40 A. All the components have operating junction temperatures (T_J) from -55°C to at least +150°C. SiC MOSFETs from ROHM and Microsemi have even higher maximum operating junction temperatures of +175°C.

$V_{CE(on)}$ is the voltage drop between the collector and the emitter of the IGBT and $R_{DS(on)}$ is the on-state resistance of the MOSFET. *APT25SM120B* from Microsemi has

significantly higher on-state resistance (140 mΩ) than the other SiC MOSFETs (75 mΩ and 80 mΩ) and is therefore left out from further evaluation. However, all of the compared SiC components have significantly lower $R_{DS(on)}$ values than what would be achieved with Si technology with the same breakdown voltage. For example, the Si MOSFET *FQD2N100* from Fairchild Semiconductor has $R_{DS(on)}$ value of 9 Ω with 1000 V breakdown voltage [10]. Similarly the Si MOSFET *IPAN80R450P7* from Infineon has $R_{DS(on)}$ value of 450 mΩ with 800 V breakdown voltage [3].

C3M0075120K from Cree has a kelvin source connection and it is in a four-pin TO-247 package. All the other components have a three-pin TO-247 package.

5.1.2 Switching characteristics

IGBT and MOSFET manufacturers provide three capacitance values on their component datasheets: C_{iss}, C_{oss} and C_{rss}. The input capacitance (C_{iss}) is charged during the turn-on process and needs to be discharged before the component can turn off. Therefore, C_{iss} has a direct relationship to the turn-on and turn-off delays. The output capacitance (C_{oss}) is important in soft switching applications. C_{rss} is the reverse transfer capacitance that is equal to the gate-drain capacitance of a MOSFET and to the gate-collector capacitance of an IGBT. It is one of the major parameters affecting voltage rise and fall times during switching. [21]

Gate charge values reflect the charge stored on the device capacitances [21]. The time that is required to turn-on a switching device is the time it takes to inject the gate-emitter charge (Q_{ge}) and the gate-collector charge (Q_{gc}) of an IGBT, and Q_{gd} and Q_{gs} of a MOSFET into the gate [35]. Table 5 shows the capacitance and gate charge values for the Si IGBT and for the selected SiC MOSFETs according to their datasheets.

Table 5. *Capacitance and gate charge values of the selected components. Measured at 25°C. [1, 5-7]*

	IGBT, Infineon, IRGP30B120KD	MOSFET, ROHM, SCT3080KL	MOSFET, Cree, C3M0075120K	MOSFET, Cree, C2M0080120D
C_{iss}	2200 pF	780 pF	1350 pF	950 pF
C_{oss}	210 pF	75 pF	58 pF	80 pF
C_{rss}	85 pF	35 pF	3 pF	7.6 pF
Q_g	169 nC	60 nC	51 nC	62 nC
Q_{ge}/Q_{gs}	19 nC	15 nC	14 nC	15 nC
Q_{gc}/Q_{gd}	82 nC	25 nC	21 nC	23 nC

As can be seen from Table 5, the input and output capacitances of the Si IGBT are approximately 2-3 times higher than those of the SiC MOSFEETs. Even the highest SiC MOSFET input capacitance value (*C3M0075120K*, 1350 pF) is 850 pF smaller than the C_{iss} value of the Si IGBT (2200 pF). Also, the highest SiC MOSFET output capacitance value (*C2M0080120D*, 80 pF) is 130 pF smaller than the C_{oss} value of the Si IGBT (210 pF). C_{rss} of the Si IGBT is considerably larger than that of the SiC MOSFETs. C_{rss} values vary a lot between the SiC MOSFET from ROHM (35 pF) and the two SiC MOSFETs from Cree (3 pF and 7.6 pF).

There is not a clear difference in Q_{ge}/Q_{gs} values between the Si IGBT and the SiC MOSFETs. However, the total gate charge and Q_{gc}/Q_{gd} values are approximately three times larger for the Si IGBT. The gate charge values between the selected SiC MOSFETs are almost equal.

The higher capacitance and gate charge values of the Si IGBT predict slower turn-on and turn-off times and higher switching losses when compared to the selected SiC MOSFETs. Also, since the IGBT is a bipolar device with current tailing, it should have notably longer turn-off time and turn-off losses when compared to unipolar MOSFETs. The MOSFET can turn off as soon as the parasitic junction capacitances are discharged while the IGBT turns fully off after all the minority carriers are recombined. Table 6 shows the turn-on and turn-off energies and times for the Si IGBT and for the selected SiC MOSFETs.

Table 6. *Switching energies and switching times of the components. Measured at 25°C unless otherwise specified. [1, 5-7]*

	IGBT, Infineon, IRGP30B120KD	MOSFET, ROHM, SCT3080KL	MOSFET, Cree, C3M0075120K	MOSFET, Cree, C2M0080120D
E_{on}	1066 µJ	132 µJ	275 µJ	265 µJ
E_{off}	1493 µJ	18 µJ	70 µJ	135 µJ
$t_{d(on)}$	50 ns (at 125°C)	15 ns	22 ns	11 ns
t_r	25 ns (at 125°C)	22 ns	11 ns	20 ns
$t_{d(off)}$	210 ns (at 125°C)	29 ns	33 ns	23 ns
t_f	60 ns (at 125°C)	24 ns	11 ns	19 ns

As was predicted, the turn-on loss of the Si IGBT is approximately 4-8 times larger than that of the SiC MOSFETs. The difference is even higher for the turn-off loss because of the minority carriers in the IGBT structure. The turn-off loss of the SiC MOSFET *SCT3080KL* (18 µJ) is 1475 µJ smaller when compared to that of the Si IGBT *IRGP30B120KD* (1493 µJ). Also, the turn-off losses of the SiC MSOFETs from Cree are 11-17 times smaller than that of the Si IGBT.

The turn-on and turn-off times between the Si IGBT and the SiC MOSFETs differ remarkably. The turn-on time of the Si IGBT (50 ns) is 2 times longer than that of the slowest SiC MOSFET (*C3M0075120K*, 22 ns). Even more significant is the differences in the turn-off times. The turn-off time of the Si IGBT (210 ns) is over 170 ns greater than the turn-off time of any of the selected SiC MOSFETs (23-33 ns). Out of the selected SiC MOSFETs, the $t_{d(on)}$ and $t_{d(off)}$ times are the longest for Cree's *C3M0075120K* (22 ns and 33 ns, respectively). However, as was discovered previously, all the SiC MOSFETs have extremely fast switching times when compared with the original Si IGBT.

Different manufacturers provide their component information at different temperatures. The switching energies of Cree's *C3M0075120* was informed at 150°C in the datasheet's table of electrical characteristics, while all the other selected components had their switching energies measured at room temperature (25°C). Often the manufacturers also provide graphs that show the relationships between different values and junction temperature. In Figure 43 is shown the graphs of switching loss as a function of junction temperature for Cree's *C3M0075120K* and *C2M0080120D*.

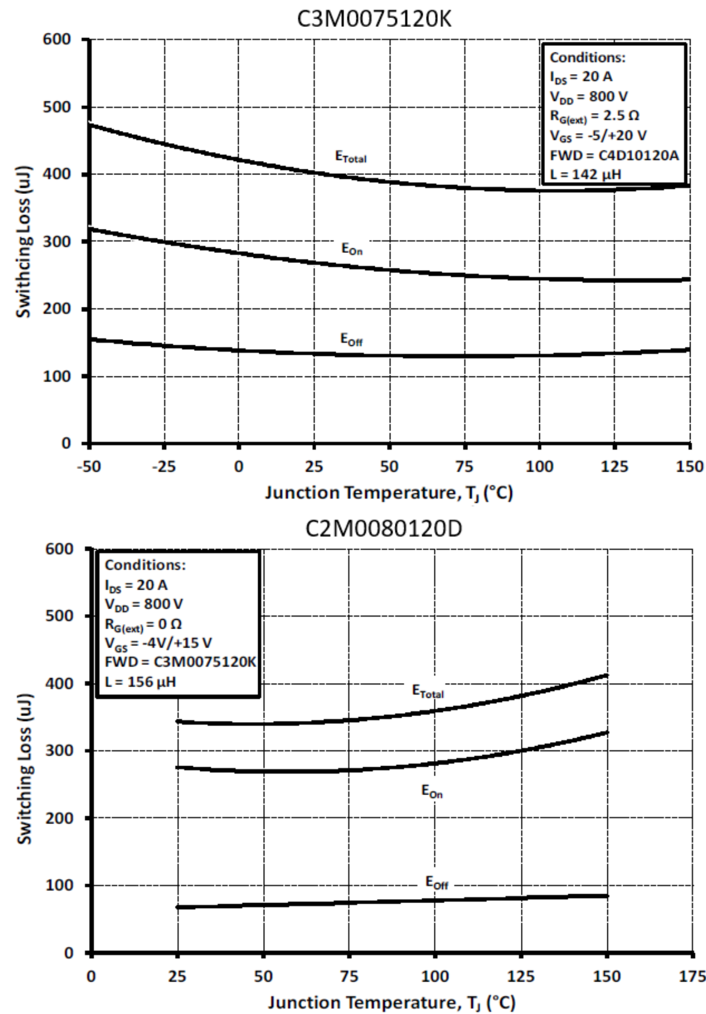

Figure 43. *Switching energies as a function of junction temperature for Cree's SiC MOSFETs C3M0075120K and C2M0080120D. Adapted from [1, 6].*

As can be seen from Figure 43, the turn-on loss of *C3M0075120K* increase with an increasing junction temperature while the turn-on loss of *C2M0080120D* decreases with an increasing junction temperature. To be able to compare the switching losses of the selected components, the turn-on and turn-off loss of *C3M0075120K* at room temperature were looked from the graph provided on the datasheet.

It should be noticed, that the switching times and energies are strongly affected by stay inductances in the circuit, as has been discussed in earlier chapters. Switching time and energy values that are provided in the datasheets may vary from observed results in an actual power device. [21]

5.1.3 Diode reverse recovery characteristics

The *pn*$^-$-junction of the power MOSFET forms an effective body diode in parallel with the MOSFET channel, as was discussed in Chapter 2.1.1. Also, the Si IGBTs utilized in the original power converter include antiparallel soft recovery diodes in the same package

to carry current in opposite direction. Characteristics of the body diode influence the performance and reliability of the converter as well as the characteristics of the MOSFETs and the IGBTs. The reverse recovery characteristics affect the peak current ratings, turn-on transition times, and turn-on switching loss of the switching components. [43] Information of the reverse recovery characteristics of the selected components are gathered on Table 7.

Table 7. *Reverse recovery characteristics of the switching components. Measured at 25°C unless otherwise specified. [1, 5-7]*

	IGBT, Infineon, IRGP30B120KD	MOSFET, ROHM, SCT3080KL	MOSFET, Cree, C3M0075120K	MOSFET, Cree, C2M0080120D
V_{SD}	1.76 V	3.2 V	4.5 V	3.3 V
I_S	-	31 A_{max}	22.4 A_{max}	36 A_{max}
t_{rr}	300 ns (at 125°C)	17 ns	18 ns (at 150°C)	32 ns
Q_{rr}	-	50 nC	220 nC (at 150°C)	192 nC
E_{rec}	1820 µJ (at 125°C)	-	-	-
I_{rr}	34 A (at 125°C)	6 A	19 A (at 150°C)	10 A

V_{SD} is the forward voltage rating of the diode and I_S is the maximum continuous forward current rating of the diode. t_{rr} is the reverse recovery time, Q_{rr} the reverse recovery charge, E_{rec} the reverse recovery energy, and I_{rr} the peak reverse recovery current of the diode.

As can be seen from the t_{rr} values on Table 7, the antiparallel diode of the Si IGBT from Infineon has remarkably longer reverse recover time (300 ns) than the body diodes of the SiC MOSFETs (17 ns - 32 ns). The antiparallel diode of the IGBT *IRGP30B120KD* is a soft recovery diode. Soft recovery diodes are utilized for lower *dv/dt* rates during the turn-off process of the diode. Lower *dv/dt* rate can decrease oscillation losses and EMI in the circuit. However, the reverse recovery time of a soft recovery diode is long and will cause more losses in the diode. [27]

Q_{rr} is the amount of charge that is stored in the diode structure during its on-state and needs to be removed through recombination before the diode turns off. Hence I_{rr} is the reverse current that results from recombination, there is a straight relationship between these values. This can also be seen from the Q_{rr} and I_{rr} values on Table 7. The SiC MOSFET *C3M0075120K* from Cree has the highest Q_{rr} value (220 nC) and I_{rr} (19 A)

value, while the SiC MOSFET *SCT3080KL* has the lowest Q_{rr} and I_{rr} values (50 nC and 6 A, respectively). I_{rr} values of all the selected SiC MOSFETs are moderate when compared to the I_{rr} value of the Si IGBT *IRGP30B120KD* (34 A).

Minority carrier concentration increases with temperature, thus I_{rr} and t_{rr} also increase with temperature [56]. Temperature dependence should be noticed when the reverse recovery characteristics are compared based on the datasheet values. t_{rr}, Q_{rr}, and I_{rr} values of the SiC MOSFET *C3M0075120K* are given at 150°C and t_{rr}, E_{rec}, and I_{rr} values of the Si IGBT *IRGP30B120KD* are given at 125°C while the reverse recovery characteristics of other components are given at room temperature. *C3M0075120K* and *IRGP30B120KD* might have smaller t_{rr} and I_{rr} values at room temperature. However, the Si IGBT has significantly higher t_{rr} and I_{rr} values even when compared to the SiC MOSFET *C3M0075120K* values that are also measured at high temperature.

5.1.4 Selecting the SiC MOSFET

SiC MOSFETs from five manufacturers Cree, ROHM, Microsemi, ON Semiconductor and Infineon were considered to replace the original Si IGBTs. SiC MOSFETs *APT25SM120B* from Microsemi, *SCT3080KL* from ROHM, and *C3M0075120K* from Cree were selected for further comparison and evaluation. SiC MOSFETs from ON Semiconductor and Infineon were still under development, thus their datasheets were confidential and could not be shared in this thesis work. All the selected SiC MOSFETs fulfilled the basic requirements that were set based on the design of the power converter. However, the SiC MOSFET *APT25SM120B* from Microsemi had significantly higher on-state resistance (140 mΩ) than the other SiC MOSFETs (75 mΩ and 80 mΩ) and was therefore left out from further evaluation.

All SiC MOSFETs had significantly lower capacitance and gate charge values when compared to those of the original Si IGBT. Also, the switching energies and switching times were remarkably smaller than those of the original Si IGBT, especially during the turn-off process. This was expected since unlike the bipolar transistors, the MOSFET does not suffer from minority carrier storage effects during the turn-off. There were small differences in the capacitance values of the SiC MOSFETs. *C3M0075120K* from Cree had the largest C_{iss} value (1350 pF) but the lowest C_{oss} value (58 pF). C_{rss} value varied a lot between the SiC MOSFET *SCT3080KL* from ROHM (35 pF) and the two SiC MOSFETs *C3M0075120K* and *C2M0080120D* from Cree (3 pF and 7.6 pF respectively). There were only minor differences in the gate charge values between the compared SiC MOSFETs. The switching energies E_{on} and E_{off} were the smallest for *SCT3080KL* from ROHM (132 µJ and 18 µJ, respectively), while *C3M0075120K* had the largest E_{on} value (275 µJ) and *C2M0080120D* had the largest E_{off} value (135 µJ). Cree's *C3M0075120K* also had the longest $t_{d(on)}$ and $t_{d(off)}$ times out of the compared SiC MOSFETs.

Also, the reverse diode characteristics of the SiC MOSFETs were superior compared to those of the original Si IGBT. *C2M0080120D* form Cree had the longest t_{rr} time (32 ns) and *C3M0075120K* from Cree had the largest I_{rr} (19 A) out of the compared SiC MOSFETs.

Since the availability of the SiC MOSFETs under development from ON Semiconductor and Infineon was uncertain, these components were not selected to replace the original Si IGBT. All the SiC MOSFETs had superior switching and reverse diode characteristics when they were compared with the Si IGBT utilized in the original converter. Although the SiC MOSFET *C3M0075120K* from Cree had the largest C_{iss}, E_{on} and I_{rr} values, it was considered more important to have a Kelvin source connection and to avoid any additional stray inductance effects in this application. Therefore, *C3M0075120* with a Kelvin source connection was selected to replace the original Si IGBT *IRGP30B120KD*.

5.2 Driver component

The selected SiC MOSFET required new driver components. As was discussed in Chapter 4.2, although the SiC MOSFET and the Si IGBT both have the MOS-gate structure, the gate driver for the SiC MOSFET might not be directly utilized from the original power converter.

The gate driver in the original power converter was *Si8238* from Silicon Labs. Silicon Labs also provides drivers with high drive voltage values and the new driver component was selected from their *Si827x* drivers. The gate driver *Si8273* had the same input and output terminals as the original driver and therefore it was selected in order to avoid major changes on the converter design. There were two variants of *Si8273* with the same *undervoltage lockout* (UVLO) value than the original driver had. *Si8273DBD* had an integrated deglitcher and *Si8273DB* had a low jitter feature. Electrical characteristics of the original driver and of the selected drivers are listed on Table 8.

Table 8. *Electrical characteristics of the driver components [5, 6].*

	Si8238, Silicon Labs	Si8273DB, low jitter, Silicon Labs	Si8273DBD, integrated deglitcher, Silicon Labs
Input Supply Voltage	2.7 - 5.5 V	2.5 - 5.5 V	2.5 - 5.5 V
Driver Supply Voltage	6.5 - 24 V	4.2 - 30 V	4.2 - 30 V
Common Mode Transient Immunity	45 kV/μs	300 kV/μs	350 kV/μs

As can be seen from the listed electrical characteristics on Table 8, the two compared drivers can use the same input supply voltage than the original driver, but they can supply 6 V higher gate voltage to the switching components.

Si8273DBD has an integrated deglitcher to remove glitches from the circuit. *Si8273DB* has a low-jitter feature, which is utilized to remove signal jitter from the gate control signals. Jitter is always present in digital systems and it introduces wideband noise to the converters' power output [34]. Neither one of these special features were not considered significant for this application. The selection was done based on the different common mode transient immunity values that were provided on the datasheet. *Si8273DBD* had a common mode transient immunity of 350 kV/µ that was 50 kV/µ higher than that of *Si8273DB* (300 kV/µ). Therefore, *Si8273DBD* was selected as the driver component for the previously selected SiC MOSFETs.

All though the *Si8273DBD* had the same input and output terminals as the original gate driver, its pin order was slightly different and required some modifications on layout of the original converter. No other changes were made on the original driver circuit.

6. RESULTS AND ANALYSIS

In this thesis, the effects of upgrading a power converter with SiC MOSFETs on switching waveforms and on converter efficiency was being studied. It was also studied, if the Si IGBTs of the PFC rectifier section of the original power converter could be directly replaced with SiC MOSFETs with minimal changes on the design of the converter and if the switching frequency of the PFC rectifier section could be increased.

The test setups, measurement equipment and measurement results are introduced in Chapter 6.1. The results from the switching waveform measurements are presented in Chapter 6.2 and the results from the efficiency measurements in Chapter 6.3. These results are analyzed in Chapter 6.4.

6.1 Measurement setups

The measurements were performed for a power converter that was fed by a three-phase power supply. The output of the converter was connected to a load that could be adjusted to a desired load current level through its software and could operate in both forward and reverse directions. Reference measurements were performed with the original power converter that had Si IGBTs as the switching components. Comparison measurement were performed with the same converter, of which PFC rectifier section was upgraded with SiC MOSFETs.

The PFC rectifier of the power converter consists of three legs and each leg has two semiconductor switches, similarly than was expressed in Figure 33 in Chapter 4.1.2. The upper power switch is called the high-side switch and the lower power switch is called the low-side switch. Switching waveforms were measured from the low-side switch on one of the rectifier legs. Measurements were performed with an oscilloscope from Teledyne LeCroy. The measured waveforms were V_{CE} and I_C from the original power converter and V_{DS} and I_D from the updated converter. Also the waveforms of the gate voltage and the converter input current were observed during the measurements but are not presented in this thesis.

The efficiency of the power converter was measured and calculated at 40 kHz switching frequency for the original converter and at 40 kHz, 80 kHz, and 120 kHz for the upgraded converter. The input power was viewed from the precision power analyzer PPA5530 from N4L, separately for the three phases. The power values of the three phases were summed in order to gain the total input power. The output power was calculated from output voltage and current values that were measured with two multimeters from Fluke. The input power values and the output voltage and current values were recorded by taking pictures of the test setup. Efficiency of the entire power converter was measured in

forward and reverse operation at different loading conditions. Also the efficiency of the PFC rectifier section was measured separately in forward operation.

6.2 Switching waveforms

The upgrade of the power converter was performed with minimal changes on the original converter. When the Si IGBTs and their driver components were replaced with the selected SiC MOSFETs and the new driver components, the drain-source voltage of the SiC MOSFET oscillated significantly during the turn-off process in the test measurements. This oscillation in V_{DS} is shown in red in Figure 44. The measurement presented in Figure 44 was carried out with a lower voltage than the rated operating voltage of the device.

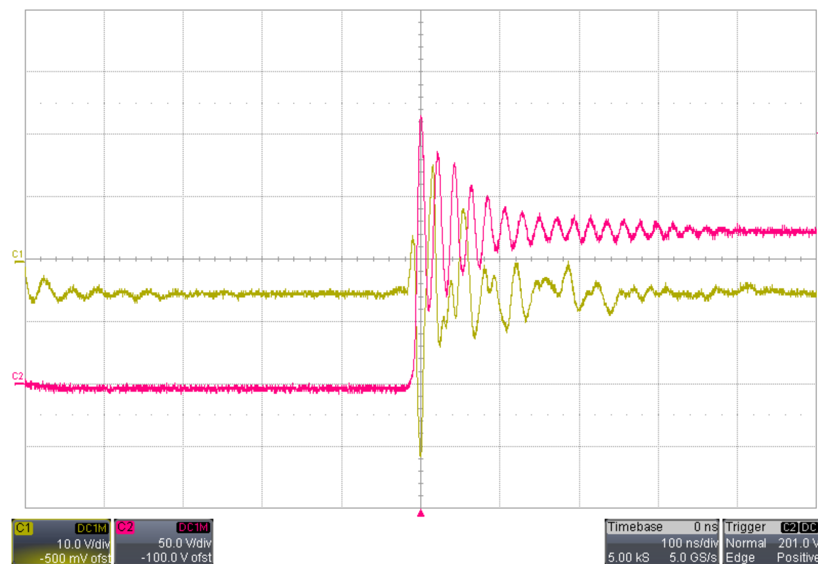

Figure 44. *Drain-source voltage oscillation of the SiC MOSFFET with 3.4 Ω gate resistor shown in red color.*

As can be seen from Figure 44, the voltage overshoot during the oscillation was 90 V and the oscillation continued for 400 ns. This oscillation was unacceptable and could cause damage to the converter at higher voltages. The measurements could not be continued with the rated operating voltage until the oscillation and the voltage overshoot would be suppressed.

Since all changes on the layout of the original power converter were avoided, the modifications needed to assemble the SiC MOSFETs and the new drivers were accomplished with jumping wires. It was taken into consideration that these additional wires could increase the stray inductance of the circuit and cause excessive noise. Also, the probes of the oscilloscope and their ground leads were fairly long. Long wires in the measuring probes could increase ringing in the circuit. However, the jumping wires and the measuring circuits were as optimized as possible.

As was discussed in Chapter 4.2, the turn-on and turn-off characteristics of a power switch could be controlled by changing the magnitude of the external gate resistors. During the turn-off process, the rapidly changing current is coupled with the parasitic inductances of the circuit and causes oscillation. By increasing the gate resistance, the current slew rate could be slowed down, which could result in lower surge voltages and limited voltage ringing. It was assumed that the ringing in the low-side switch during the turn-off is partly a result from the fast turn-on and rapid current change of the high-side switch. Therefore, the external gate resistor value was changed only for the positive gate voltage supply that drives the switches to on-state. The original gate resistances in the gate driver circuits were 3.4 Ω. The gate resistance for the positive gate voltage was increased to 5.5 Ω. Figure 45 shows V_{DS} of the low-side SiC MOSFET during the turn-off process with the increased $R_{g,on}$ at the rated operating voltage (~ 650 V).

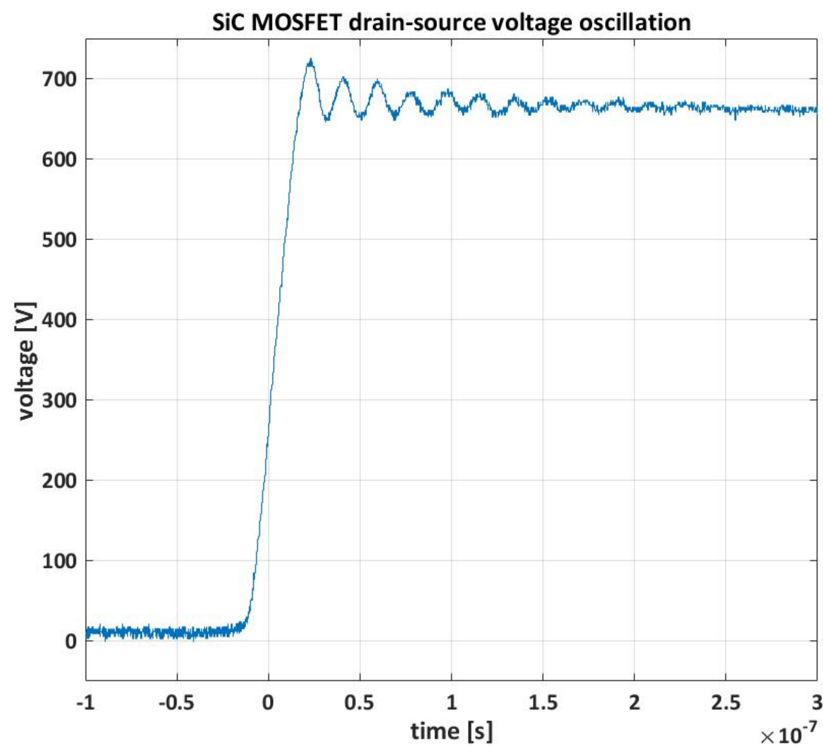

Figure 45. *Drain-source voltage oscillation of the SiC MOSFET with 5.5 Ω gate resistor.*

As can be seen from the drain-source voltage presented in Figure 45, increasing the gate resistor value from 4.3 Ω to 5.5 Ω suppressed the voltage overshoot to 61.6 V and abbreviated the duration of the voltage oscillation to 233 ns. The voltage overshoot decreased 28.4 V and the duration of the oscillation decreased by 167 ns. However, as was discussed in Chapter 4.2, as the current slew rate is slowed down during the turn-on process, also the turn-on delay time increases, which results in higher switching losses. In this thesis work, slowing down the current slew rate was essential in order to suppress the voltage oscillation.

The switching waveforms of the semiconductor switches were studied in operating conditions where significant voltage or current stress was applied on the power switches. First, the reverse recovery currents were studied through current waveforms. Also the entire turn-on process was examined through voltage and current waveforms. Figure 46 shows the collector current of the Si IGBT and the drain current of the SiC MOSFET during the turn-on process.

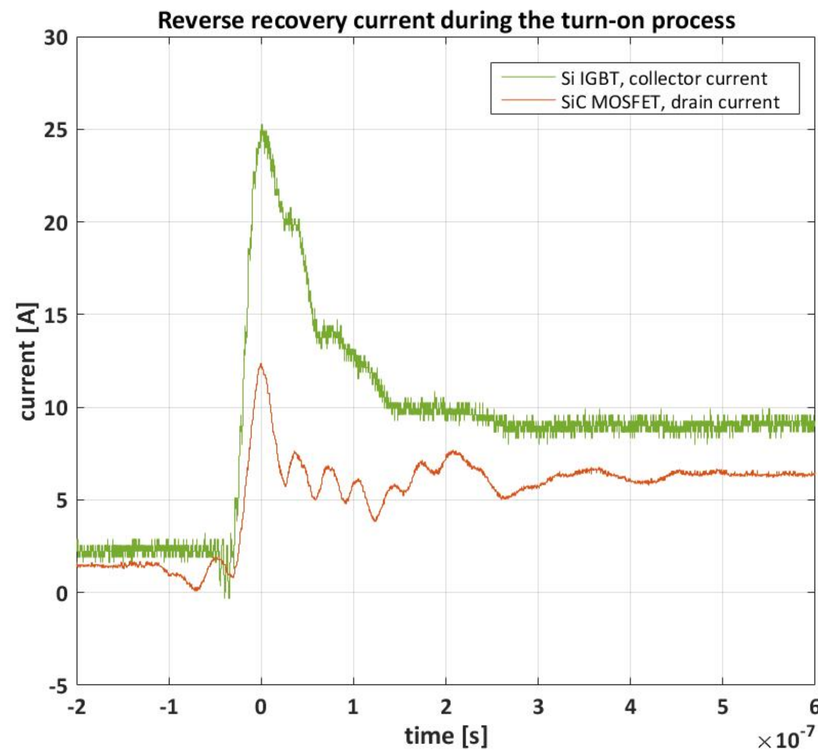

Figure 46. *Reverse recovery current of the Si IGBT and the SiC MOSFET during the turn-on process.*

Figure 46 shows I_C of the low-side Si IGBT in green and I_D of the low-side SiC MOSFET in red. Both currents are measured during the turn-on process. The waveforms in Figure 46 have a small offset from the measuring oscilloscope and therefore the current waveforms differ from 0 A before the turn-on process begins. The offset is approximately 2 A. The current waveforms show that the power converter was feeding a smaller load during the measurements of the updated power converter with SiC MOSFETs than during the reference measurements of the Si IGBT: I_D of the SiC MOSFET levels to 6.3 A while I_C of the Si IGBT levels to 9.3 A. As can be seen from Figure 46, a spike occurs in both current waveforms before the current waveforms level to on-state values. The spike in I_C of the Si IGBT is 16.3 A and the spike in I_D of the SiC MOSFET is 5.95 A when the maximal current value is compared to the final on-state current level.

As was discussed in Chapter 3.2.1, the spikes that occur in I_C and I_D of the low-side switch during the turn-on process are caused by the reverse recovery current of the high-side

switch and will increase turn-on power losses. Additional current and power loss caused by the reverse recovery current can be estimated by the surface area of the current spike in the current waveform, which shows the total additional charge Q_{tot}. Figure 46 shows the difference between the reverse recovery currents of the SiC MOSFET's body diode and the Si IGBT's freewheeling diode. Also the junction capacitances of the switching components cause reverse recovery current. The current spike in I_C of the Si IGBT is 10.4 A higher than that in I_D of the SiC MOSFET. Although the current waveforms were measured at different loading conditions, the load current value should not have significant impact on the magnitude of the reverse recovery current.

The turn-on processes of Si IGBT and SiC MOSFET were compared through their voltage and current waveforms- Figure 47 (a) shows V_{CE} and I_C of the Si IGBT and Figure 47 (b) shows V_{DS} and I_D of the SiC MOSFET during the turn-on process. The current waveforms I_C and I_D are the same waveforms that were compared in Figure 46.

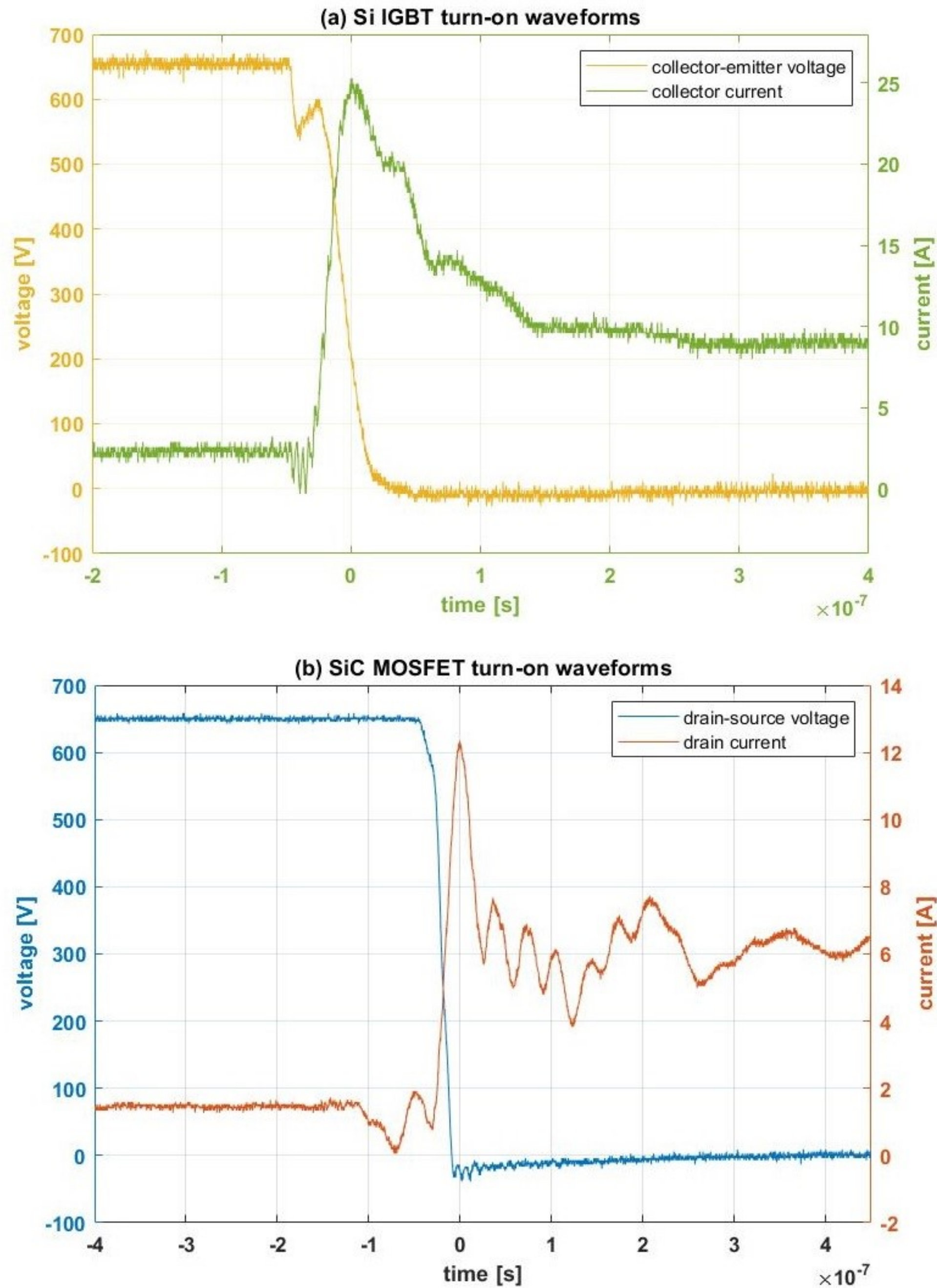

Figure 47. *Turn-on waveforms of (a) the Si IGBT and (b) the SiC MOSFET.*

Figures 47 (a) and (b) show how the current waveforms of the semiconductor switches begin to rise and the voltage over the switches decrease rapidly after the gate voltage has been set to its high value. Both figures show a voltage drop in V_{CE} and in V_{DS} before the voltage waveforms start to decrease steadily towards zero. This voltage drop (V_{drop}) is caused by the fast change in current that induces voltages across the parasitic inductances L_s and L_D, as was discussed in Chapter 3.2.1.

Figure 47 (a) shows that V_{CE} of the Si IGBT decreases from 651 V to zero in 0.772 ns. Voltage slew rate of the Si IGBT is 842 V/ns during the turn-on process. According to

Figure 47 (b), V_{DS} of the SiC MOSFET decreases from 655 V to zero in 0.36 ns. During the turn-on process, *dv/dt* of the SiC MOSFET is 1 819 V/ns, which is 977 V/ns faster than that of the Si IGBT. Faster turn-on process results in lower turn-on power losses, as was discussed in Chapter 2. Also the reverse recovery current spike of the SiC MOSFET was 10.4 A lower than that of the Si IGBT, which also promises lower turn-on power loss for the upgraded power converter. However, V_{DS} of the SiC MOSFET has oscillation for 0.68 ns after it has decreased below zero and the drain current has remarkable fluctuation before leveling to its on-state value. These oscillations cause excessive stress and power losses over the switching device.

Secondly, the turn-off process was studied by comparing the voltage waveforms V_{CE} of the Si IGBT and in V_{DS} of the SiC MOSFET during the turn-off process. These voltage waveforms are presented in Figure 48.

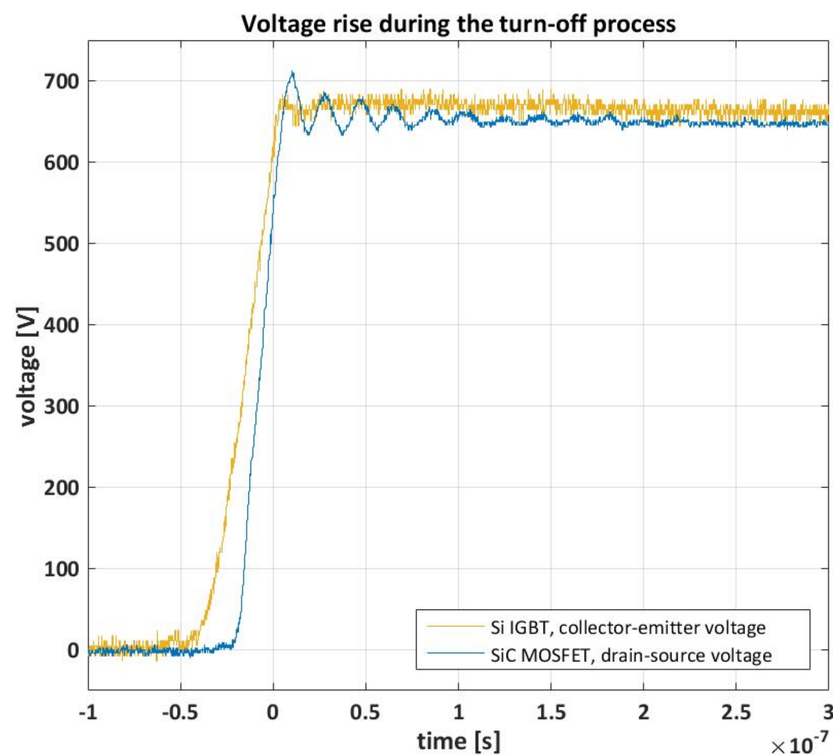

Figure 48. *Voltage rise waveforms of the Si IGBT and the SiC MOSFET during the turn-off process.*

As can be seen from Figure 48, the rise time of V_{CE} of the Si IGBT (0.53 ns) is 0.2 ns longer than that of V_{DS} the SiC MOSFET (0.33 ns). The Si IGBT has a voltage slew rate of 12.68 V/ns while the voltage slew rate of the SiC MOSFET is 21.42 V/ns. *dv/dt* rate of the Si IGBT is 8.74 V/ns slower than that of the SiC MOSFET. Longer turn-off delay time and slower *dv/dt* rate of the Si IGBT results in larger turn-off losses, as was discussed in Chapter 4.2. However, V_{DS} of the SiC MOSFET has oscillation for 233 ns

and voltage overshoot of 61.6 V. Voltage overshoot and oscillation may cause damage to the switching device, increase power losses and introduce EMI noise.

Lastly, the turn-off processes of the Si IGBT and the SiC MOSFET were compared through their voltage and current waveforms. Figure 49 (a) shows V_{CE} and I_C of the Si IGBT and Figure 49 (b) shows V_{DS} and I_D of the SiC MOSFET during the turn-on process. The voltage waveforms V_{CE} and V_{DS} are the same waveforms that were compared in Figure 48.

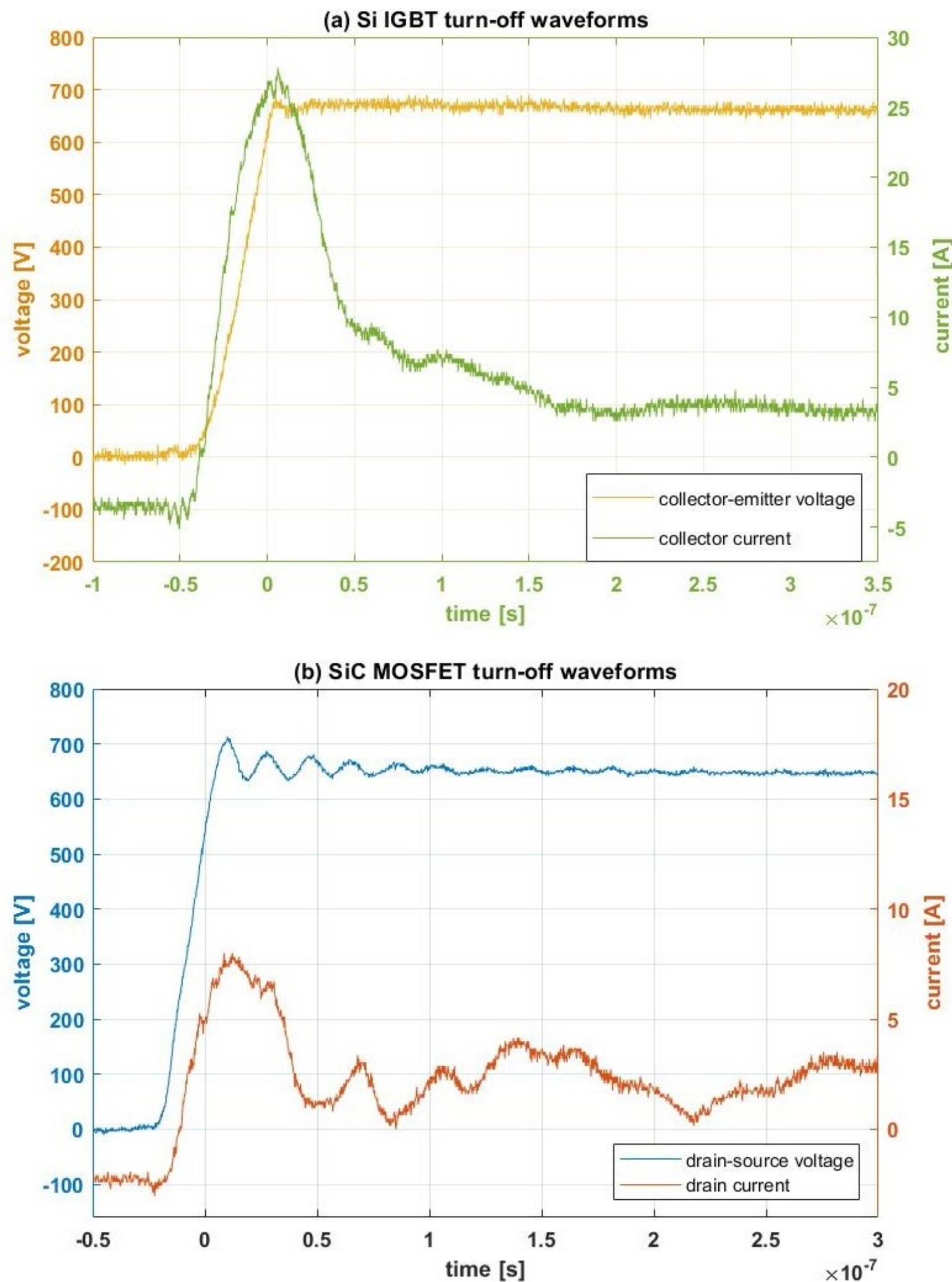

Figure 49. *Turn-off waveforms of (a) the Si IGBT and (b) the SiC MOSFET.*

Figures 49 (a) and (b) show the turn-off waveforms of the switching devices under hard switching. In the beginning of the turn-off process, the current of the lower leg of the

converter goes through the freewheeling diode of the low-side switch. The current that is measured at the semiconductor switch before the turn-off process is therefore negative. Hard switching of the high-side switch forces the entire current to run through the high-side switch and the low-side switch turns off. Similarly to the turn-on current waveforms, also the turn-off current waveforms have offset from the measuring oscilloscope for approximately 2 A. As can be seen from Figures 49 (a) and (b), the reverse recovery spike occurs in I_C and I_D also during the forced turn-off process. The current spike in I_D of the SiC MOSFET is 5.6 A and the current spike in I_C of the Si IGBT is 23.8 A, when the maximum current value is compared to the final off-state current level. The additional current spike of the Si IGBT is 18.2 A greater than that of the SiC MOSFET. As was previously discussed, reverse recovery current during the turn-off process increase turn-off power losses. Additional power loss caused by the reverse recovery current can be estimated by the surface area of the current spike in the current waveform.

Observations from the voltage and current waveforms presented in Figures 45 - 49 are gathered on Table 9.

Table 9. *Observations from the turn-on and turn-off waveforms of the Si IGBT and the SiC MOSFET.*

	Si IGBT, *dv/dt*	**SiC MOSFET, *dv/dt***	**difference**	**observations**
Turn-on process	842 V/ns	1 819 V/ns	977 V/ns	Minor ringing in V_{DS} of the SiC MOSFET
Turn-off process	12.68 V/ns	21.42 V/ns	8.74 V/ns	Oscillation in V_{DS} of the SiC MOSFET for 233 ns and voltage overshoot 61.6 V
	Si IGBT, I_{rr} overshoot	**SiC MOSFET, I_{rr} overshoot**	**difference**	**observations**
Turn-on process	16.3 A	5.95 A	10.4 A	Fluctuation in I_D
Turn-off process	23.8 A	5.6 A	18.2 A	Fluctuation in I_D

6.3 Efficiency measurements

As was introduced in Chapter 6.1, the input power of the power converter was viewed from a power analyzer for the three phases and summed in order to gain the total input

power. Output power was calculated from output voltage and output current according to $P_{out} = V_{out} * I_{out}$. V_{out} and I_{out} were measured with two multimeters. The efficiency of the power converter in forward operation mode was measured with 14 output load values from 740 W to 10 360 W. In reverse operation mode the efficiency was measured with 10 output load values from -628 W to -7 640 W. The reference measurements with the original power converter were performed at the rated 40 kHz switching frequency. Efficiency of the upgraded power converter was measured with 40 kHz, 80 kHz, and 120 kHz switching frequencies at the PFC rectifier section.

During the reference measurements, the intermediate voltage broke through the Si IGBTs of the buck DC-DC converter. These first measurements were performed by constantly increasing the output load after the previous load step was recorded. After the voltage breakdown we learned that the power converter did not have any load protection and it was designed to withstand the rated maximum load only for approximately 3 seconds. This time constraint made the measurements more difficult, since 3 seconds was just enough for the power analyzer and for the multimeters to level after the load step. This made the measurements less reliable. Only the Si IGBTs of the buck DC-DC converter broke during the voltage breakdown and the efficiency measurements could be continued after the damaged components were replaced. Efficiency was calculated as the ratio of the output power and the input power, according to Equation (23) in Chapter 4.4. The calculated efficiency of the original converter and of the upgraded converter with different output load values and switching frequencies are presented in Table 10 in Appendix A.

From the efficiency values in Table 10 can be noticed that the efficiency of the updated power converter at row 9. with 120 kHz switching frequency and with P_{out} = 6 660 W is 1.0455. The efficiency of the power converter cannot be over 1, thus it is assumed that there is an error in this measurement caused by the time constraint. This measurement point is ruled out from further studies. The efficiency curves for the power converter in forward operation mode are presented in Figure 50.

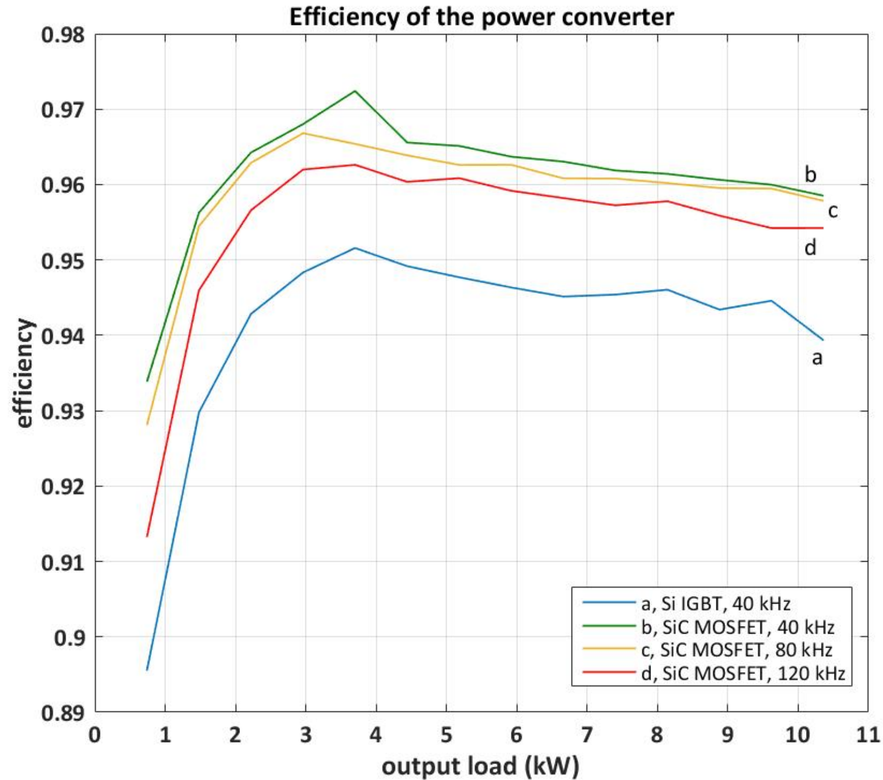

Figure 50. *Efficiency curves of the power converter with (a) Si IGBTs and with (b-d) SiC MOSFETs in the PFC rectifier section.*

As can be seen from the efficiency curves in Figure 50, the efficiency of the power converter increased notably by changing the switching components. The increase in efficiency was approximately 2.1 percentage points between the original power converter and the upgraded power converter at 40 kHz switching frequency. Even with higher switching frequencies the increase in efficiency with SiC MOSFETs is visible. When the switching frequency was increased, also the switching losses increased since the switches turned on and off more often. The increase in efficiency was approximately 1.9 pp at 80 kHz switching frequency and 1.4 pp at 120 kHz switching frequency. These measurements demonstrate that the efficiency of the converter could be considerably increased with SiC MOSFETs even when the switching frequency is tripled.

The efficiency of the power converter was also studied at reverse operation by feeding negative values to the output load. The calculated efficiency of the original converter and of the upgraded converter with different output load values and switching frequencies are presented in Table 11 in Appendix A for reverse operation. It should be noticed that in order to obtain the correct efficiency value, the output and the input power are reversed in the calculations in relation to forward operation. The efficiency curves for the power converter in reverse operation mode are presented in Figure 51.

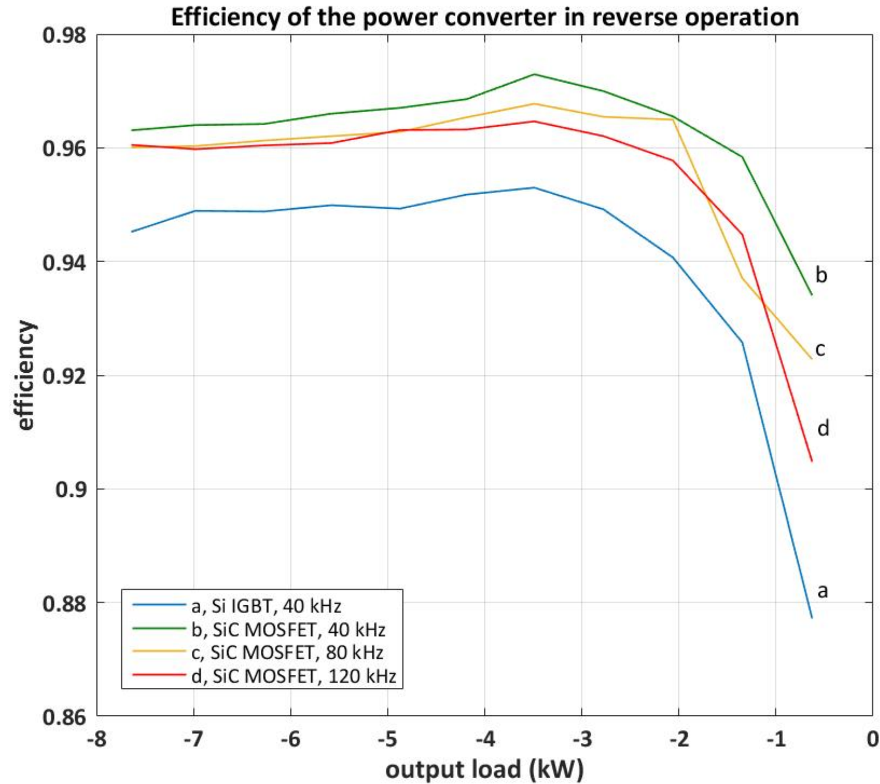

Figure 51. *Efficiency curves of the power converter in reverse operation with (a) Si IGBTs and with (b-d) SiC MOSFETs in the PFC rectifier section.*

Since the power converter was operating in reverse direction, thus feeding power to the supply line, the output load was considered negative. Therefore, the output load value increases from right to left on the efficiency curves in Figure 51. The efficiency curves in reverse operation resemble those of forward operation and show a similar increase in efficiency with the upgraded power converter. It should be noticed that the maximum output load in reverse operation was less than during the efficiency measurements in forward operation. The increase in efficiency was approximately 2.4 pp between the original power converter and the upgraded converter at 40 kHz switching frequency during reverse operation. The increase in efficiency was approximately 1.8 pp at 80 kHz switching frequency and 1.5 pp at 120 kHz switching frequency.

After measuring the efficiency of the entire power converter in forward and in reverse operation modes, losses of the buck DC-DC section were diminished from total losses in order to define the efficiency of the PFC rectifier section separately. First, the efficiency of the buck DC-DC section was measured with different load values. The total losses of the converter ($P_{loss,tot}$) with Si IGBTs and SiC MOSFETs at different switching frequencies were calculated according to $P_{loss,tot} = \frac{P_{out}}{\eta} - P_{out}$. Also the losses of the buck DC-DC section ($P_{loss,buck}$) were calculated similarly and diminished from the total losses to gain the losses of the PFC rectifier section ($P_{loss,PFC}$) according to $P_{loss,PFC} =$

$P_{loss,tot} - P_{loss,buck}$. The calculated losses $P_{loss,buck}$ and $P_{loss,PFC}$ are presented in Table 12 in Appendix A. The efficiency of the PFC section was calculated according to $\eta_{PFC} = \frac{P_{out}}{(P_{out}+P_{loss,PFC})}$. The calculated efficiency values for the buck DC-DC section and for the PFC rectifier section with Si IGBTs and with SiC MOSFETs at different switching frequencies are presented in Table 13 in Appendix A. Corresponding efficiency curves are presented in Figure 52.

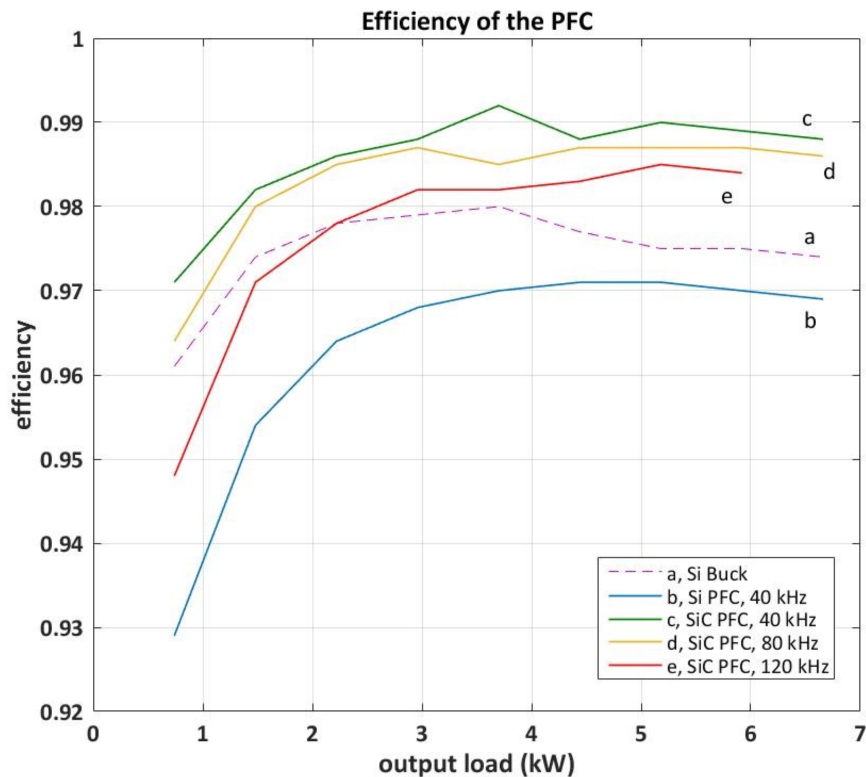

Figure 52. *Efficiency curves of (a) the buck DC-DC section, (b) the PFC rectifier section with Si IGBTs, and (c-e) the PFC rectifier section with SiC MOSFETs.*

As can be seen from the efficiency curves on Figure 52, the efficiency of the PFC rectifier section increased significantly with the SiC MOSFET upgrade. The efficiency of the PFC rectifier increased approximately 2.4 pp from the average of 0.96 to the average of 0.99 at 40 kHz switching frequency. The efficiency also increased at higher switching frequencies. At 80 kHz switching frequency the increase in efficiency was approximately 2.2 pp and at 120 kHz approximately 1.5 pp. The efficiency curve (e) at Figure 52 finishes at the output load of 5 920 W since the measurement point at P_{out} = 6 660 W was ruled out from the results.

6.4 Analysis

The switching waveform measurements in Chapter 6.2 show that it is possible to upgrade the power converter, that is designed with Si IGBTs, with SiC MOSFETs with minimal changes on the original converter design. Oscillation and voltage overshoot that occurred during the turn-off process in the first tests were successfully suppressed by increasing the gate resistor value in the positive gate supply. By increasing $R_{g(on)}$ the current slew rate was slowed down during the turn-on process, thus the turn-on delay time was increased. Even with a higher $R_{g(on)}$ value, the turn-on process of the SiC MOSFET was 977 V/ns faster than that of the Si IGBT. The turn-off process of the SiC MOSFET was 8.74 V/ns faster than that of the Si IGBT during hard-switching of the high-side switch.

One of the major differences between the switching curves of the Si IGBT and the SiC MOSFET were in the reverse recovery currents. During the turn-on process, the reverse recovery current of the high-side switch and its body diode or freewheeling diode caused current spikes that would increase switching losses in the low-side switch. The SiC MOSFET had 10.4 A lower I_{rr} overshoot than the Si IGBT. Also during the turn-off process the I_{rr} overshoot of the SiC MOSFET was 18.2 A lower than that of the Si IGBT.

From the switching waveforms it was expected that the upgraded power converter with SiC MOSFETs would have lower switching losses during the turn-on and the turn-off processes than with Si IGBTs due to the faster *dv/dt* rates and significantly lower reverse recovery current values. However, there was notable oscillation and overshoot in V_{DS} of the SiC MOSFET and fluctuation in I_D that could cause some additional power losses and produce excessive stress over the switching components. The reliability and durability of the SiC MOSFETs need to be further investigated and the layout of the power converter needs to be optimized for the new components and for higher switching frequencies. However, these measurements show promising results that power converters designed with Si IGBTs can be upgraded with SiC MOSFETs with somewhat small changes and with moderate workload.

The efficiency measurements in Chapter 6.3 illustrate that a significant increase in converter efficiency can be achieved by upgrading the switching components in the PFC rectifier section. The efficiency curves (a) and (b) in Figure 52 show that in this power converter the original PFC rectifier section has lower efficiency (0.96) than the buck DC-DC section (0.97) with Si IGBTs and with the same switching frequency. By upgrading the Si IGBTs of the PFC rectifier section with SiC MOSFETs, the efficiency of the PFC rectifier increased 2.2 pp at 40 kHz switching frequency. This increase equals approximately 30-50 W smaller power losses at low output load values (P_{load} of 740-2 220 W) as can be calculated from the power loss values presented in Table 12. The smaller power losses were expected since the selected SiC MOSFETs had faster *dv/dt* rates and significantly lower reverse recovery current values when compared with the original Si IGBTs, as was discovered in the measurements in Chapter 6.2. Even though

the IGBTs generally have smaller on-state losses when compared with MOSFETs, the SiC MOSFETs can have significantly lower $R_{DS(on)}$ values and thus lower on-state losses than the conventional Si MOSFETs, as was discussed in Chapter 2.3.1.

Switching losses increase as the switching frequency is increased, since the switching components turn on and off more often. Therefore, it was expected that the efficiency of the upgraded power converter would decrease as the switching frequency was increased. Even when the switching frequency of the PFC rectifier section was tripled, the efficiency was approximately 1.5 pp greater than that of the original PFC rectifier. This increase equals approximately 16-33 W smaller power losses at low output load values (P_{load} of 740 - 2 220 W) as can be calculated from the power loss values in Table 12.

The increase in efficiency of the upgraded PFC rectifier affected positively the overall efficiency of the power converter, as could be seen from the efficiency curves in forward operation mode in Figure 50 and in reverse operation mode in Figure 51. Efficiency of the power converter increased in forward operation mode from the average of 0.94 to 0.96 at 40 kHz switching frequency. The increase of 2.1 pp in efficiency is significant as the efficiency of the original power converter is already high. Even at higher switching frequencies the increase in efficiency was notable. Efficiency in reverse operation mode showed a similar increase in efficiency with the upgraded power converter.

The drive for increasing the switching frequency of the PFC rectifier section was to be able to reduce the size and weight of the large magnetic components of the power converter. It was not possible to design new filter inductors and transformers for the upgraded power converter within this thesis work, but according to Equations (17) and (22) in Chapter 4.3 both the transformer volume and the filter inductor size could be decreased with increased switching frequency. Magnetic components are designed individually for most power applications. Further current measurements, calculations, and comparison of available magnetic core materials are required for optimizing the magnetic components of the upgraded power converter.

The performed efficiency measurements are estimations of the efficiency. The measurement devices and the test setup were not optimized, and the measurement results have a wide margin of error due to the time limitation of 3 seconds. This time constraint was barely enough for the measurement devices to level after a load step and it affects the reliability of the measurements greatly. It was considered if the measurements could be performed with a thermographic camera in order to achieve exact measurements, but the switching components that would have been measured were located inside the converter and could not be exposed. However, all the efficiency curves presented in Figures 50-52 show a similar increase in converter efficiency. It can be assumed that these efficiency curves give a correct estimation of the efficiency, even though the individual measurement points are not comparable.

7. CONCLUSIONS

Si IGBTs combined with silicon-based freewheeling diodes are commonly used in power applications [37]. However, these silicon-based components are approaching their performance limits as power electronics move towards higher efficiency, higher power density and more integrated systems. Wide bandgap semiconductors, such as silicon carbide, allow designing devices with faster switching speeds, higher switching frequencies and for higher temperatures than has been achieved with the conventional Si components. [48] Higher operation frequency makes it also possible to utilize smaller and lighter transformers, filter inductors, and capacitors [42]. Compared with IGBTs, the MOSFETs have significantly lower switching losses due to their majority carrier conduction mechanism [48]. At voltages greater than 600 V, MOSFETs have been preferred since their switching speeds are significantly faster than that of the IGBTs and their on-state voltage drop has still been competitive with the voltage drop in minority carrier devices. [22] SiC technology has enabled the usage of MOSFETs also in high-voltage applications since they have 10 times larger critical electric field values when compared with Si devices and they have very low on-state resistances even at high voltages [48].

In this thesis work, it was studied if a power converter that was designed with Si IGBTs as the switching components could be upgraded with SiC MOSFETs with minimal changes on the original converter design. The upgrade was performed for the active three-phase rectifier of the converter that also has power factor correction. The effects of the upgrade on switching waveforms and on converter efficiency was examined. Also the possibility of increasing the switching frequency of the PFC rectifier section and its effects on converter efficiency was studied.

In the original three-phase rectifier the switching components were Si IGBTs *IRGP30B120* from International Rectifier. It was desirable that the SiC MOSFETs would have the same TO-247 package, corresponding voltage rating of 1 200 V, and similar rated current between 20 and 40 A than the original Si IGBTs had. However, also a four-pin TO-247 package was an option, since the additional Kelvin source connection would reduce the common mode inductance of the power switch. SiC MOSFETs from five manufacturers Cree, ROHM, Microsemi, ON Semiconductor and Infineon were considered to replace the original Si IGBTs. All the SiC MOSFETs had superior switching and reverse diode characteristics when they were compared with the Si IGBT utilized in the original converter. It was considered most important to have a Kelvin source connection in order to avoid any additional stray inductance effects in this application. Therefore, *C3M0075120* from CREE with a Kelvin source connection was selected to replace the original Si IGBT. The selected SiC MOSFET required new driver

components to achieve greater gate voltage level. The gate driver in the original power converter was *Si8238* from Silicon Labs. Silicon Labs also provides drivers with higher voltage values and *Si8273DBD* from Silicon Labs was selected as the driver components for the previously selected SiC MOSFETs.

The measurements in this thesis work included reference measurements that were performed with the original power converter that had Si IGBTs as the switching components, and comparison measurements that were performed with the same converter, of which PFC rectifier section was upgraded with SiC MOSFETs. Switching waveforms were measured from the low-side switch on one of the rectifier legs. The efficiency of the power converter was measured and calculated at 40 kHz switching frequency for the original converter and at 40 kHz, 80 kHz, and 120 kHz for the upgraded converter. Efficiency of the entire power converter was measured in forward and reverse operation at different loading conditions. Also the efficiency of the PFC rectifier section was measured separately in forward operation.

The switching waveform measurements showed that it is possible to upgrade the power converter that is designed with Si IGBTs with SiC MOSFETs with minimal changes on the original converter design. The SiC MOSFETs had faster switching times and significantly lower reverse recovery currents when compared to those of the Si IGBTs, as was to be expected also from the datasheet comparison of these components and based on the theory study. From the switching waveforms it was expected that the upgraded power converter with SiC MOSFETs would have lower switching losses during the turn-on and the turn-off processes than with Si IGBTs due to the faster *dv/dt* rates and significantly lower reverse recovery current values.

The efficiency measurements illustrated that a significant increase in converter efficiency can be achieved by upgrading the switching components in the PFC rectifier section. By upgrading the Si IGBTs of the PFC rectifier section with SiC MOSFETs, the efficiency of the PFC rectifier increased 2.2 pp at 40 kHz switching frequency from the average of 0.94 to the average of 0.96. The smaller power losses corresponded the expectations made based on the switching waveform measurements and on the theory study. It was expected that the efficiency of the upgraded power converter would decrease as the switching frequency was increased since the witching losses increase as the switches are turned on and off more often. Even when the switching frequency of the PFC rectifier section was tripled, the efficiency was approximately 1.5 pp greater than that of the original PFC rectifier. The increase in efficiency of the upgraded PFC rectifier section affected positively the overall efficiency of the power converter in forward operation mode and in reverse operation mode. Efficiency of the power converter increased in forward operation mode from the average of 0.94 to 0.96 at 40 kHz switching frequency. The increase of 2.1 pp in efficiency is significant as the efficiency of the original power converter is already high. Even at higher switching frequencies the increase in efficiency was notable.

Efficiency in reverse operation mode showed a similar increase in efficiency with the upgraded power converter.

The performed efficiency measurements are estimations of the efficiency, since the test setup was not optimized, and the measurement devices had barely enough time to level after a load step due to the time constraint of 3 seconds. The efficiency measurements would have been more reliable, if the efficiency of the switching components would have been measured with a thermographic camera. This was not possible since the semiconductor switches were located inside the converter and could not be exposed. However, it can be assumed that these efficiency curves give a correct estimation of the efficiency, even though the individual measurement points are not comparable. Also the switching waveform measurements are directional, since the new switching components and drivers were assembled via jumping wires and the probes of the oscilloscope had fairly long wires, that could increase the stray inductance and affect the switching waveforms.

Based on this study, it is plausible and beneficial to upgrade a power converter with SiC MOSFETs. The possibility to increase the switching frequency of the PFC rectifier section allows to design smaller and lighter magnetic components that will considerably reduce the overall size and weight of the power converter. However, much work needs to be done before the upgraded power converter could be ready for use. Within this thesis work we did not study the reliability of the SiC MOSFETs or EMI issues that can result from the higher switching frequency, oscillation in voltage waveforms and fluctuation in current waveforms, that need to be still examined. Also the converter design and layout needs to be optimized and the new magnetic components must be designed. It must be considered, if the higher cost of the new switching components and the work hours needed to achieve the complete upgraded power converter are worth the gained efficiency improvement and the smaller size and weight. Nevertheless, these measurements show promising results that power converters designed with Si IGBTs can be upgraded with SiC MOSFETs with somewhat small changes and with moderate workload.

REFERENCES

[1] C3M0075120K Datasheet, CREE, 2017.

[2] Calculation of turn-off power losses generated by an ultrafast diode, AN5028 Application not, ST Microelectronics, Rev 1, 2017, 20 p.

[3] IPAN80R450P7 Datasheet, Infineon, Rev. 2.0, 2016, 13 p.

[4] SCT3080KL Datasheet, ROHM Semiconductor, 2016.

[5] Si823x Datasheet, Silicon Labs, 2016, 56 p.

[6] Si827x Datasheet, Silicon Labs, 2016, 41 p.

[7] APT25SM120B Datasheet, Microsemi, 2015.

[8] C2M0080120D Datasheet, CREE, 2015.

[9] IRGP30B120KD-EP Datasheet, International Rectifier, 2014, 13 p.

[10] FQD2N100/FQU2N100 Datasheet, Fairchild Semiconductor, Vol. Rev. C0, 2013, 9 p.

[11] SiC Power Devices and Modules, Application Note, ROHM semiconductor, Rev. 001, 2013, 39 p.

[12] 3F4 Material specification, Ferroxcube, 2008.

[13] A. Hilal, B. Cougo, Optimal inductor design and material selection for high power density inverters used in aircraft applications, International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC) 2016, pp. 1-6.

[14] M.R. Ahmed, R. Todd, A.J. Forsyth, Analysis of SiC MOSFETs under hard and soft-switching, 2015 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 2231-2238.

[15] B. Bidoggia, R. Maheshwari, R. Nielsen, S. Munk-Nielsen, F. Blaabjerg, Steady-state analysis of dead-time effect on bidirectional buck converters, IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society, pp. 792-797.

[16] B.J. Baliga, Silicon Carbide Power Devices, World Scientific Publishing Company, River Edge, 2006, 528 p.

[17] Power Sources and Supplies - World Class Designs, Elsevier.

[18] C. G. Stella, M. Laudani, A. Gaito, M. Nania, Advantage of the use of an added driver source lead in discrete Power MOSFETs, 2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014, pp. 2574-2581.

[19] S. Chattopadhyay, M. Mitra, S. Sengupta, Electric Power Quality, Springer Netherlands, 2011, 182 p.

[20] Cheng Song, Zhang Yingchao, Lu Jiaxin, Zhan Tianwen, Li Long, Qian Xisen, A ZVS bidirectional buck converter applied to hybrid energy storage system, 2014 IEEE Conference and Expo Transportation Electrification Asia-Pacific (ITEC Asia-Pacific), pp. 1-6.

[21] J. Dodge, J. Hess, IGBT Tutorial, Advanced Power Technology, Application Note APT0201, Rev. B, 2002, pp. 1-15.

[22] R.W. Erickson, D. Maksimovic, Fundamentals of Power Electronics, Springer US, 2001, 883 p.

[23] F. F. Wang, Z. Zhang, Overview of silicon carbide technology: Device, converter, system, and application, CPSS Transactions on Power Electronics and Applications, Vol. 1, Iss. 1, 2016, pp. 13-32.

[24] H. Jungwirth, M. Schmidhuber, M. Baumann, Next generation ferrite material for SiC & GaN applications, 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 887-889.

[25] H. R. Karampoorian, G. Papi, A. Zadehgol, Volume and loss optimization of high frequency transformer for compact switch mode power supply considering corrected waveform factor, 2006 IEEE Power India Conference, pp. 6.

[26] H.Huang, X. Yang, Y. Wen, Z. Long, A switching ringing suppression scheme of SiC MOSFET by Active Gate Drive, 2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), pp. 285-291.

[27] P. Haaf, J. Harper, Understanding Diode Reverse Recovery and its Effect on Switching Losses, Fairchild Semiconductor Power Seminar, 2007, pp. 23-33.

[28] J. Rabkowski, T. Platek, Comparison of the power losses in 1700V Si IGBT and SiC MOSFET modules including reverse conduction, 2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe), pp. 1-10.

[29] J. Rice, J. Mookken, SiC MOSFET gate drive design considerations, 2015 IEEE International Workshop on Integrated Power Packaging (IWIPP), pp. 24-27.

[30] J. W. Kolar, F. Krismer, Y. Lobsiger, J. Muhlethaler, T. Nussbaumer, J. Minibock, Extreme efficiency power electronics, 2012 7th International Conference on Integrated Power Electronics Systems (CIPS), pp. 1-22.

[31] J. W. Kolar, T. Friedli, The Essence of Three-Phase PFC Rectifier SystemsPart I, IEEE Transactions on Power Electronics, Vol. 28, Iss. 1, 2013, pp. 176-198.

[32] K. Peng, S. Eskandari, E. Santi, Characterization and modeling of SiC MOSFET body diode, 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 2127-2135.

[33] M. Liserre, A. Dell'Aquila, F. Blaabjerg, Design and control of a three-phase active rectifier under non-ideal operating conditions, Conference Record of the 2002 IEEE Industry Applications Conference. 37th IAS Annual Meeting (Cat. No.02CH37344), pp. 1181-1188.

[34] M. Mauerer, A. Tüysüz, J. W. Kolar, Low-Jitter GaN E-HEMT Gate Driver With High Common-Mode Voltage Transient Immunity, IEEE Transactions on Industrial Electronics, Vol. 64, Iss. 11, 2017, pp. 9043-9051. Available (accessed ID: 1):.

[35] R. McArthur, Making Use of Gate Charge Information in MOSFET and IGBT Data Sheets, Advanced Power Technology, Application Note APT0103, 2001, pp. 1-8.

[36] N. Mohan, T.M. Undeland, W.P. Robbins, Power electronics: converters, applications, and design, John Wiley & Sons, 2003, 824 p.

[37] M. Nawaz, K. Ilves, Replacing Si to SiC: Opportunities and challenges, 2016 46th European Solid-State Device Research Conference (ESSDERC), IEEE.

[38] P. Nayak, M. V. Krishna, K. Vasudevakrishna, K. Hatua, Study of the effects of parasitic inductances and device capacitances on 1200 V, 35 A SiC MOSFET based voltage source inverter design, 2014 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), pp. 1-6.

[39] P.V. Pol, S.L. Patil, S.K. Pandey, A simple and novel technique for driving silicon carbide power MOSFETs with unipolar supply voltage, 2016 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), IEEE, pp. 1-6.

[40] A.I. Pressman, Switching Power Supply Design, McGraw-Hill, 1998, 682 p.

[41] F. Qi, L. Fu, L. Xu, P. Jing, G. Zhao, J. Wang, Si and SiC power MOSFET characterization and comparison, 2014 IEEE Conference and Expo Transportation Electrification Asia-Pacific (ITEC Asia-Pacific), IEEE, pp. 1-6.

[42] M.H. Rashid, Power Electronics Handbook, Elsevier Science, 2011, 1362 p.

[43] S. C. Das, G. Narayanan, Reverse recovery characteristics of the IGBT anti-parallel diode with variation in operating conditions: An experimental study, 2016 7th India International Conference on Power Electronics (IICPE), pp. 1-5.

[44] S. Guo, L. Zhang, Y. Lei, X. Li, W. Yu, A. Q. Huang, Design and application of a 1200V ultra-fast integrated Silicon Carbide MOSFET module, 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 2063-2070.

[45] S. Kloetzer, U. Mueter, S. Fahlbusch, K. F. Hoffmann, Compact Diode-less Bidirectional GaN Based Buck Converter for Mobile DC-DC Applications, PCIM

Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, pp. 1-8.

[46] S. Mao, T. Wu, X. Lu, J. Popovic, J. A. Ferreira, Three-phase active front-end rectifier efficiency improvement with silicon carbide power semiconductor devices, 2016 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 1-8.

[47] S. Yin, K. J. Tseng, P. Tu, R. Simanjorang, A. K. Gupta, Design considerations and comparison of high-speed gate drivers for Si IGBT and SiC MOSFET modules, 2016 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 1-8.

[48] X. She, A.Q. Huang, O. Lucia, B. Ozpineci, Review of Silicon Carbide Power Devices and Their Applications, IEEE Transactions on Industrial Electronics, 2017, pp. 8193-8205.

[49] B. Streetman, S. Banerjee, Solid State Electronic Devices, Global Edition, Pearson Education Limited, 2015, 616 p.

[50] S.M. Sze, Semiconductor devices, physics and technology, Wiley, 1985, 582 p.

[51] T. Liu, R. Ning, T. T. Y. Wong, Z. J. Shen, Modeling and Analysis of SiC MOSFET Switching Oscillations, IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 4, Iss. 3, 2016, pp. 747-756.

[52] T. Zhao, J. Wang, A. Q. Huang, A. Agarwal, Comparisons of SiC MOSFET and Si IGBT Based Motor Drive Systems, 2007 IEEE Industry Applications Annual Meeting, pp. 331-335.

[53] Turchi Joel, Dalal Dhaval, Wang Patrick, Jenck Laurent, Power Factor Correction (PFC) Handbook, ON Semiconductor, 2014, 118 p.

[54] W. J. Gu, R. Liu, A study of volume and weight vs. frequency for high-frequency transformers, Power Electronics Specialists Conference, 1993. PESC '93 Record., 24th Annual IEEE, pp. 1123-1129.

[55] X. Hou, D. Boroyevich, R. Burgos, Characterization on latest-generation SiC MOSFET's body diode, 2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), pp. 247-252.

[56] X. Li, L. Zhang, S. Guo, Y. Lei, A. Q. Huang, B. Zhang, Understanding switching losses in SiC MOSFET: Toward lossless switching, 2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA), pp. 257-262.

[57] K. YAMAGUCHI, J. MAGOME, Y. SASAKI, Fast and Low Loss Gate Driver for SiC-MOSFET, Electronics and Communications in Japan, Vol. 99, 2016, pp. 13-23.

APPENDIX A: EFFICIENCY MEASUREMENT DATA

Table 10. *Efficiency of the power converter with Si IGBTs and with SiC MOSFETs in the PFC rectifier section.*

Line number	Load power (W)	Efficiency with Si IGBT, 40 kHz	Efficiency with SiC MOSFET, 40 kHz	Efficiency with SiC MOSFET, 80 kHz	Efficiency with SiC MOSFET, 120 kHz
1.	740	0.8955	0.9338	0.9281	0.9132
2.	1 480	0.9298	0.9563	0.9545	0.9460
3.	2 220	0.9428	0.9642	0.9629	0.9566
4.	2 960	0.9483	0.9680	0.9668	0.9620
5.	3 700	0.9516	0.9724	0.9654	0.9626
6.	4 400	0.9492	0.9656	0.9639	0.9604
7.	5 180	0.9477	0.9651	0.9626	0.9608
8.	5 920	0.9463	0.9637	0.9626	0.9592
9.	6 660	0.9451	0.9630	0.9608	*1.0455*
10.	7 400	0.9454	0.9619	0.9608	0.9572
11.	8 140	0.9469	0.9614	0.9602	0.9578
12.	8 880	0.9434	0.9606	0.9585	0.9559
13.	9 620	0.9446	0.9600	0.9595	0.9542
14.	10 360	0.9393	0.9585	0.9578	0.9542

Table 11. *Efficiency of the power converter in reverse operation with Si IGBTs and with SiC MOSFETs at the PFC rectifier section.*

Line number	Load power (W)	Efficiency with Si IGBT, 40 kHz	Efficiency with SiC MOSFET, 40 kHz	Efficiency with SiC MOSFET, 80 kHz	Efficiency with SiC MOSFET, 120 kHz
1.	-628	0.8773	0.9340	0.9228	0.9048
2.	-1 348	0.9368	0.9584	0.9371	0.9447
3.	-2 062	0.9407	0.9655	0.9649	0.9577
4.	-2 778	0.9492	0.9700	0.9655	0.9620
5.	-3 490	0.9530	0.9730	0.9677	0.9646
6.	-4 185	0.9518	0.9686	0.9654	0.9632
7.	-5 580	0.9499	0.9660	0.9620	0.9608
8.	-6 273	0.9488	0.9642	0.9613	0.9604
9.	-6 979	0.9489	0.9640	0.9603	0.9598
10.	-7 640	0.9452	0.9631	0.9601	0.9605

Table 12. *Losses of the buck section with Si IGBTs and losses of the PFC rectifier section with Si IGBTs and SiC MOSFETs.*

Line number	Load power (W)	Losses of buck with Si IGBTs (W)	Losses of PFC with Si IGBTs (W),40 kHz	Losses of PFC with SiC MOSFETs (W), 40 kHz	Losses of PFC with SiC MOSFETs (W), 80 kHz	Losses of PFC with SiC MOSFETs (W), 120 kHz
1.	740	29.987	56.354	22.451	27.352	40.310
2.	1 480	40.023	71.777	27.648	30.549	44.521
3.	2 220	51.034	83.563	31.281	34.551	49.707
4.	2 960	63.218	98.041	34.592	38.398	53.749
5.	3 700	75.689	112.59	29.279	56.948	69.006
6.	4 440	106.12	131.65	52.184	60.303	77.164
7.	5 180	132.73	153.13	54.477	68.502	78.378
8.	5 920	154.37	181.27	68.643	75.556	97.629
9.	6 660	175.96	210.63	79.609	95.587	

Table 13. *Efficiency of the buck section with Si IGBTs and efficiency of the PFC rectifier section with Si IGBTs and SiC MOSFETs.*

Line number	Load power (W)	Efficiency of buck	Efficiency of PFC with Si IGBT, 40 kHz	Efficiency of PFC with SiC MOSFET, 40 kHz	Efficiency of PFC with SiC MOSFET, 80 kHz	Efficiency of PFC with SiC MOSFET, 120 kHz
1.	740	0.9611	0.9292	0.9705	0.9644	0.9483
2.	1 480	0.9737	0.9538	0.9817	0.9798	0.9708
3.	2 220	0.9776	0.9637	0.9861	0.9847	0.9781
4.	2 960	0.9791	0.9679	0.9885	0.9872	0.9822
5.	3 700	0.9800	0.9705	0.9921	0.9848	0.9820
6.	4 440	0.9767	0.9712	0.9884	0.9866	0.9829
7.	5 180	0.9750	0.9713	0.9896	0.9870	0.9851
8.	5 902	0.9756	0.9703	0.9885	0.9874	0.9838
9.	6 660	0.9743	0.9693	0.9882	0.9859	