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HIGH-SPEED CAMERA SERIAL INTERFACE VERIFICATION

Master of Science Thesis

Examiners:  
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## ABSTRACT

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During the last decade, cameras have become a standard part of many personal devices such as mobile phones, personal computers, and tablets. General camera sensor development has been really fast. Picture quality has increased significantly and mobile imaging is getting closer to compact cameras. Technically many camera features such as the resolution, frame rates and application features are improved. This continuous change has an impact for the needed system bandwidth.

This thesis focuses on the D-PHY interface verification defined by the international MIPI alliance. The interface is a commonly used standard in the mobile camera and display interface and most of the component suppliers directly support that standard. The current standard revision is the third approved version. When the first standard version supported 1 Gbps per lane, the current version supports lane-speed up to 2.5 Gbps.

The increase in bandwidth has brought new needs for the signal integrity verification. During the past years, the camera signal integrity has not been a critical design parameter. Nowadays, the interface performance is often close to its electrophysical limits and many design parameters need to be considered during the system design phase.

The purpose of this thesis is to create a reliable verification environment for the D-PHY camera interface verification. The target for quality is to build a reference level measurement environment. The system will replace manual measurements which take a lot of resources. The system will be used in verification, but as important as the verification is to understand better the current and incoming challenges and practical limits in system design.

## TIIVISTELMÄ

TAMPEREEN TEKNILLINEN YLIOPISTO

Signaalinkäsittely ja tietoliikennetekniikka

**PUSKALA, JOONAS:** High-Speed Camera Serial Interface Verification

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Kamerat ovat reilussa kymmenessä vuodessa tulleet kiinteäksi osaksi monia henkilökohtaisia laitteita, kuten matkapuhelimia, tietokoneita ja tabletteja. Samalla kameroiden yleinen kehitys on ollut nopeaa ja tekniset ominaisuudet, kuten kuvanlaatu ovat parantuneet. Samanaikaisesti kuvan resoluutiot ja latenssivaatimukset ovat kasvaneet merkittävästi, mikä on johtanut väylänopeuksien kasvuun.

Tässä työssä on keskitytty kansainvälisen MIPI Alliancen määrittelemän D-PHY -rajapinnan verifiointiin. Sitä käytetään yleisenä standardina mobiililaitteiden kamera- ja näyttöväylissä. Standardi on kehittynyt viime vuosina merkittävästi ja väylän suurin mahdollinen siirtonopeus on kasvanut ensimmäisen hyväksytyn standardiversion 1 Gbps kaistanleveydestä nykyiseen 2.5 Gbps kaistanleveyteen.

Siirtonopeuden kasvu on tuonut uudenlaisen tarpeen kameraväylän verifiointiin ja koko suunnitteluajatteluun. Aiemmin käytetyillä väylänopeuksilla signaalin laatu ei ole ollut kriittinen tekijä tuotesuunnittelussa, kun taas nykyisillä nopeuksilla lähestytään väylänopeuden sähköfysikaalisia rajoja. Tarvittava signaalin laatu voi siten yhtenä keskeisenä tekijänä ohjata jopa koko laitteen suunnittelua.

Työn tarkoituksena on ollut luoda kameran sensoreiden D-PHY -rajapinnan verifiointiin luotettava ja helppokäyttöinen ympäristö. Laadullisena tavoitteena on referenssitason mittausjärjestelmä. Se tulee korvaamaan käsin tehtävät mittaukset, jotka vievät hyvin paljon resursseja. Järjestelmää tullaan hyödyntämään kameroiden verifiointissa, mutta yhtä tärkeää on se, että järjestelmän avulla voidaan ymmärtää paremmin nykyisiä ja tulevaisuuden haasteita komponenttien tuotekehityksessä sekä tuoteintegroinnissa.

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## LIST OF SYMBOLS AND ABBREVIATIONS

A/D	Analog to Digital Converter
AF	Auto Focus
APS	Active-Pixel Sensor
BUJ	Bounded Uncorrelated Jitter
CCI	Camera Control Interface
CCP	Compact Camera Port
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CSI	Camera Serial Interface
DC	Direct Current
DCD	Data Cycle Distortion
DDJ	Data Dependent Jitter
DDR	Double Data Rate
DJ	Deterministic Jitter
DSI	Display Serial Interface
DUT	Device Under Test
EMC	Electromagnetic Compatibility
FF	Fixed-Focus
FPGA	Field-Programmable Gate Array
Gbps	Gigabit Per Second
GHz	Gigahertz
Hi-Res	Hi-Resolution
HS	High-Speed
I2C	Inter-Integrated Circuit
IBIS	Input/Output Buffer Information Specification
IC	Integrated Circuit
IF	Interface
ISI	Intersymbol Interference
ISP	Image Signal Processor
Low-Res	Low Resolution
LP	Low-Power
Mbps	Megabit Per Second
MHz	Megahertz
MIPI	Mobile Industry Processor Interface
Mpix	Mega Pixel
PHY	Physical Layer
PLL	Phase Locked Loop
RGB	Red Green Blue
RF	Radio Frequency
RJ	Random Jitter

SI	Signal Integrity
SJ	Sinusoidal Jitter
SMIA	Standard Mobile Imaging Architecture
SoC	System-on-Chip
TDR	Time-Domain Reflectometer
TLIS	Transmission-Line-Interconnect-Structure
$U_{inst}$	Unit Interval time.
VGA	Video Graphics Array
VNA	Vector Network Analyzer
XTAL	Crystal
$\lambda$	Wave Length
$\Omega$	Impedance Unit (ohm)
$\Delta z$	Length Unit
$C_0$	Speed of Light in Vacuum
$c$	Characteristic Capacitance per Length Unit
$C$	Capacitance
$D+ / Dp$	Positive Differential Line
$D- / Dn$	Negative Differential Line
$\epsilon_r$	Permittivity
$f$	Frequency
$f_{BW}$	Bandwidth
$I$	Current
$l$	Characteristic Inductance per Length Unit
$L$	Inductance
$m$	Meter
$\rho_L$	Reflection Coefficient
$\mu_r$	Permeability
$U$	Voltage
$v_p$	Phase Velocity
$Z_0$	Characteristic Impedance
$\omega$	Angular Velocity



# 1 INTRODUCTION

Nowadays, a high quality digital camera is a standard feature in all smart phones. The history began from the first widely commercial camera phone, which was the Nokia 7650. The phone contains a 0.3Mpix camera sensor with VGA (640x480) resolution. The quality of mobile imaging has taken giant steps during the last couple of years and outstrips traditional digital cameras in many technology areas, like the camera sensor resolution and advanced technologies like the Nokia Pureview. Today, the highest resolution is 41 Mpix, which sets quite different requirements for the data paths and digital imaging processing.

Parallel with the resolutions, also frame rates and other feature requirements need more system bandwidth. During the last years, the bandwidth has mainly grown by adding more parallel data-lanes without significant frequency increase. The supported maximum data-lane amount in the specification is reached and a way to increase the bandwidth is to increase the frequency.

Higher frequencies bring new challenges for the signal integrity and system design quality. So far, the frequencies used, have not been critical for the system design, but on the other hand, it is known that frequencies are close to their electrophysical limits. The D-PHY interface specification states the same: the maximum frequencies and required timings are defined, but at the same time the specification states that the maximum achievable bit rate frequency is dependent on the performance of the transmitter, the interconnection and the receiver design quality.

This thesis focuses on the camera serial interface test environment development and signal integrity verification. The used standard is the MIPI D-PHY CSI-2 (Mobile Industry Processor Interface D-Physical Layer Camera Serial Interface 2), which is a commonly used camera serial interface standard in mobile devices.

The main objective is to build a high quality and reliable camera module verification environment. The target of the environment is to set the reference quality for the camera serial interface verification. The setup will help to understand better which interface signal integrity factors are critical for the future projects, and what are the practical limits for the interface.

## 2 MOBILE CAMERA SYSTEM DEVICES

This chapter gives a short overview of the mobile phone camera sub-system architecture and the used interfaces.

Most of the mobile device manufacturers and component suppliers have joined the Mobile Industry Processor Interface (MIPI) alliance. It is an international forum which specifies the general standards commonly used in mobile devices, ranging from smartphones to wireless-enabled devices and netbooks. The standards specified by the MIPI Alliance may impact both hardware and software. The main purpose is to create general standards which are freely available for all the alliance members. The common standards guarantee that the components and chipsets are compatible with each other and the same components can be used in different platforms. [1]

Standard Mobile Imaging Architecture (SMIA) was originally Nokia Corporation's, nowadays Microsoft Corporation's, standard for mobile cameras. The standard generations are SMIA and SMIA++, which is an upgrade from the SMIA standard. The main features are backwards compatible, but the SMIA++ includes also some new features and technologies, such as the MIPI D-PHY CSI-2 interface support, which allows higher data bandwidth through the transmission lines. [2]

The SMIA++ standard can be divided into two parts: the electrical part which contains the supported electrical standards, and the functional part where all the software and performance related features are described. These functional features are, for example, operating modes, generic performance capabilities, output formats, control interface, and register mapping. [2]

The main objective is to be able to connect any SMIA++ standard based camera to any SMIA++ compliant host system. This will ensure the camera module compatibility across a wide range of host chipset processors, camera modules as well as research and development tools [2].

The SMIA++ standard does not overlap with the MIPI alliance interface standards. It only specifies which general standards are to be used with the SMIA++ and in the mobile devices which follow the standard.

## 2.1 Camera subsystem

A typical mobile smartphone contains two digital cameras; a high-resolution rear camera for high-quality photographing and a lower resolution front camera for video calls and selfies. The cameras together with a processor form a camera subsystem. Additionally, the camera subsystem may contain an integrated flash driver circuit and a flash module.

The camera subsystem is an integrated part of the mobile device. A basic structure is represented in Figure 2.1.

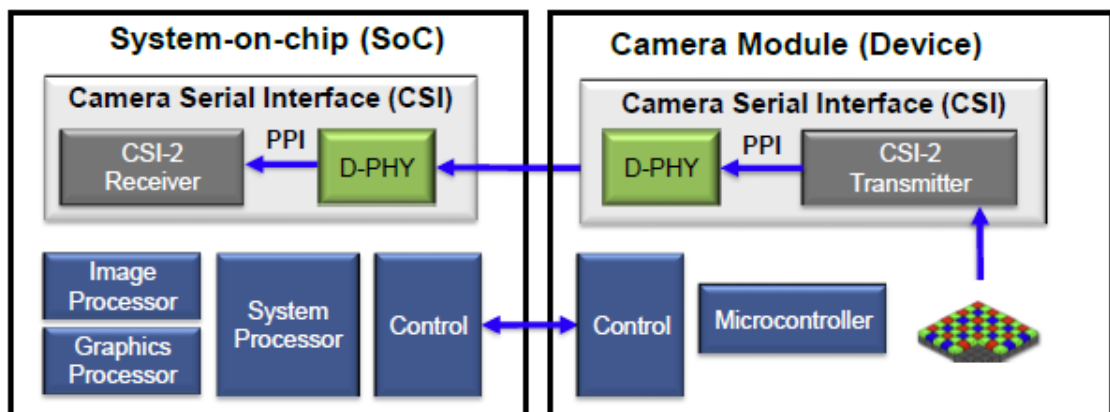


Figure 2.1. Camera sub-system structure [3]

A digital camera sensor is an integrated electronic component, which converts visible light to a data format. Currently the commonly used camera sensors are based on the CMOS APS (Complementary Metal–Oxide Semiconductor – Active Pixel Sensor) technology. [4]

Technically the camera sensor contains millions of small light sensitive sensors. Each of the sensors are sensitive to some of the three RGB-colors (Red, Green, Blue). The final pixel information contains color information from all of these color channels to present any visible color. A single sensor converts the light to an analog voltage. Depending on the amount of the received light, the sensor generates corresponding voltage level, which is converted in an A/D-converter to a digital format. [4,5]

The camera sensor picture data is transferred from the camera module to the processor and further to the Imaging Signal Processor (ISP) over the Camera Serial Interface 2 (CSI2). The physical layer standard used is the D-PHY, which defines the electrical characteristics for the interface. [2,6]

The Imaging Signal Processing unit is often a System-on-Chip (SoC) with a multi-processor architecture. It is an optimized sub-processor to process the imaging data and algorithms. The purpose of the processing is to process the RAW-picture data from the

sensor to compressed format. A second important feature is to optimize the picture quality. As a final result, it converts the captured picture data to some commonly used and packed format, such as the JPG (Video Graphics Array), stores the image to the system memory or generates a preview stream via the graphics processor to the display.

## 2.2 Electrical camera interfaces

The interface can be divided into different types of signals: a system clock, a control signal over CCI/I<sup>2</sup>C, generic I/O-control signals, a high-speed data interface and power sources. The electrical requirements for the different types of cameras are the same. [2]

A basic camera connection diagram with one differential data pair to the host system with the typical interfaces is presented in Figure 2.2.

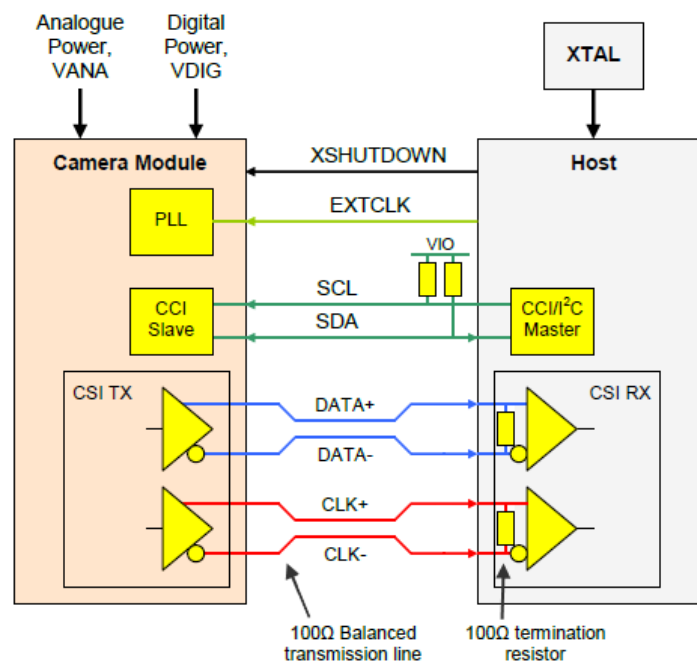


Figure 2.2 Simplified SMIA++ camera subsystem diagram [2]

The camera does not contain a system crystal (XTAL) to generate internal clocks. The camera sensor clocks are generated from an external clock generated by the system processor. All of the internal camera sensor clocks are generated from this clock in PLL's (Phase Locked Loop). The common clock source synchronizes the system, which is important especially in order to keep the high-speed data bus transmitter and the receiver synchronized. The clock quality requirements, such as jitter and voltage levels, are specified in the SMIA++ specification. [2]

The Camera Control Interface (CCI) is used as a control link between the system processor and the camera module. The standard is I<sup>2</sup>C compatible which is a 2-wire bi-directional interface including data and clock signals. The bus supports several devices,

one of the devices is a master (host unit) and others, like the cameras and the flash drives, are slaves [2,7].

Cameras use the Camera Serial Interface 2 (CSI-2) standard over the D-PHY physical layer. The interface is a high-speed data link designed for camera use by the MIPI Alliance. The interface allows the use of 1-4 differential data-lane pair(s), which makes the link bandwidth scalable to correspond to system and camera module requirements. Typically a low-end camera modules support only 1-2 data-lanes, when high-end modules support the full 4 data-lane configuration. [2,8]

Additionally, the system needs power resources. The power supply regulators are integrated to the Power Management Integrated Circuit (PMIC), which is a shared resource with the other system and peripherals. It offers the needed power and different voltage levels for the whole system. The power supplies are typically software controllable. [2]

### 2.3 Camera Serial Interface 2

The camera Serial Interface 2 (CSI-2) is the standard to identify standard interface between the camera peripheral and the host processor for high-speed mobile applications. It defines the application-, protocol and PHY layers. [6]

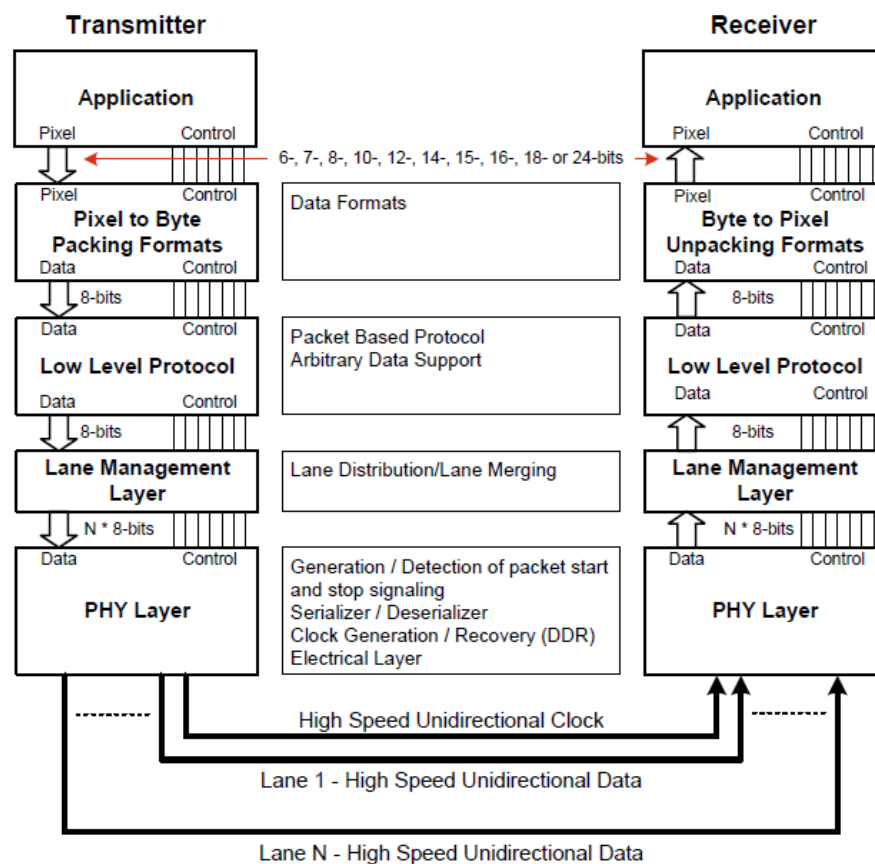


Figure 2.3 CSI-2 layer definitions [6]

- **PHY-layer:** The PHY layer specifies the physical layer for the data transmission. Such as the electrical definitions for the input and output circuitry, timings and clocking requirements, package serializer / deserializer and package detections. [6]
- **Protocol layer:** The protocol layer consists of several layers which have independent tasks in the protocol stack. The main purpose of the protocol layer is to define how multiple data streams are tagged and interleaved to ensure that each data streams can be properly reconstructed. [6]
- **Application layer:** The higher-level encoding and interpretation of data contained in the data stream. The CSI-2 specification describes the mapping of the pixel values to bytes. [6]

### 2.3.1 D-PHY layer interface

The purpose of the D-PHY layer is to provide a flexible, low-cost, high-speed and low-power solution for mobile applications. The same MIPI D-PHY layer is commonly used in both camera- (CSI) and display serial interface (DSI) applications. The prefix “D” means 500 in roman numerals, which was the maximum lane frequency in the first approved D-PHY layer specification. [6,8]

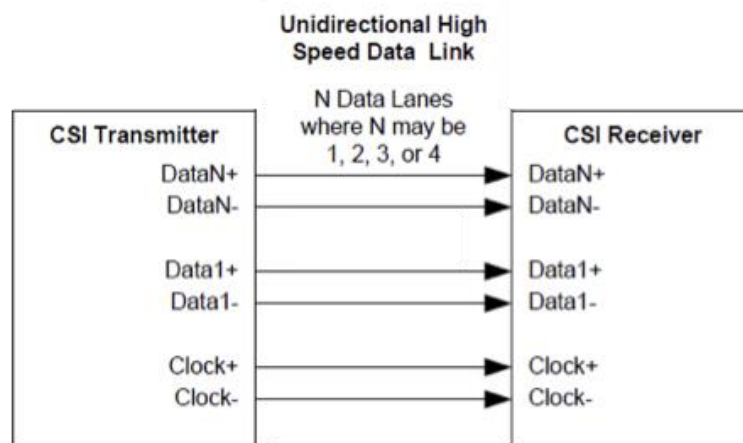


Figure 2.4 D-PHY unidirectional configuration with 2 data pairs. [6]

A basic D-PHY configuration includes one clock pair and the 1-4 data pairs depending on the application bandwidth requirements (Figure 2.4). The clock and data pairs use differential signaling. [6,8]

The first approved D-PHY layer specification version (v1.0) specifies the data rates per lane in high-speed mode up to 1 Gbps (500 MHz) and the total bandwidth of 4 Gbps with 4 data-lanes. In the next version (v1.1), maximum data rate was increased to 1.5 Gbps and the total bandwidth up to 6 Gbps. The current specification version (v1.2) supports up to 2.5 Gbps lane-speed and a total of 10 Gbps bandwidth. The specifications are mainly backwards compatible with some differences in the timing requirements. The



which case the current leakage from the transmitter to the receiver is zero. The state can be also used to disable the transmitter and receiver functional blocks in order to save energy. [8]

### 2.3.2 C-PHY layer interface

The next generation of physical interfaces under the CSI-2 specification is the C-PHY. Instead of the differential pair configurations, the C-PHY uses differential trios. Electrically it is backwards compatible with D-PHY devices. This means that the same host processors and receiver can support the D-PHY and C-PHY layers. [10]

One of the main differences compared to the D-PHY is the embedded clock. Because the trio states changes with every unit interval (UI), a separate clock pair or trio is not needed and the minimum configuration needs only three wires. The maximum system configuration is six trios or eighteen wires. [10]

The most important advantage of the C-PHY is the increased bandwidth. Sixteen bit words can be encoded to 7 channel symbols, meaning approximately 2.3 bits per symbol. Compared to the D-PHY data wire, the C-PHY effectivity per data wire is about double depending slightly from the interface configuration size. The maximum defined bandwidth is 17.1 Gbps when the full configuration is used. [10]

Figure 2.7 demonstrates the CSI2 D-PHY and C-PHY configurations and the total bandwidths. From the system point of view only the physical layer is changed and the other CSI2 layers are the same. A notable update for the picture is the channel rate increase in the D-PHY specification version 1.2. With the channel rate of 2.5 Gbps the total bandwidth is 10 Gbps.

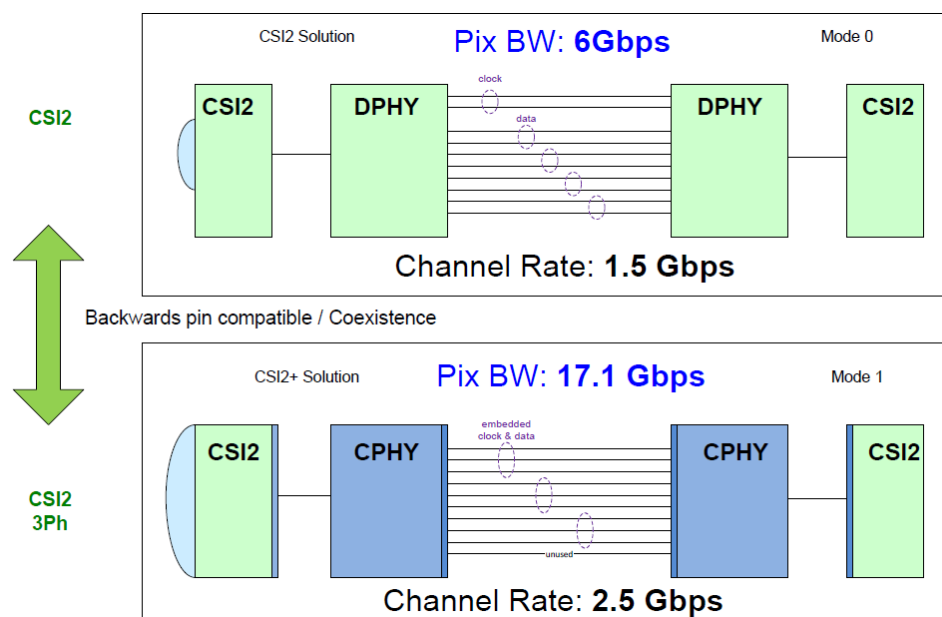


Figure 2.7 D-PHY (specification version 1.1) vs C-PHY bandwidth comparison [11]



The C-PHY layer supports six physical layer states. Figure 2.8 demonstrates the basic configuration structure and one of the possible trio states “100”. In the C-PHY trio output states are always a combination of the logical 0 and 1, which means that the trio states “000” and “111” are not possible, and the possible output combinations are limited to six. This is also one of the key parameters to define the symbol rate per clock. [10]

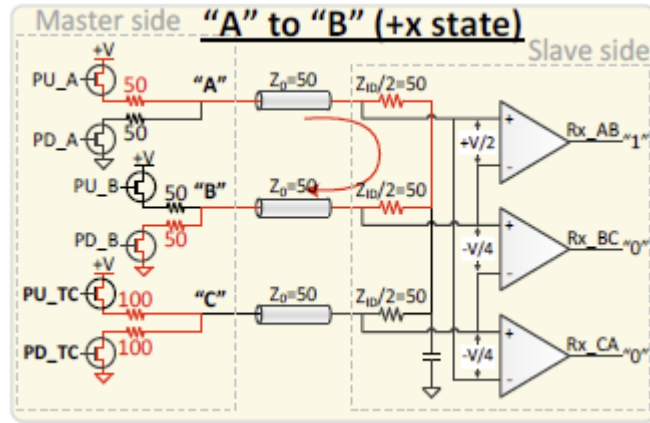


Figure 2.8 C-PHY 3-phase configuration demonstrates one of the six possible states [10]

When the D-PHY device (differential pair) needs to be connected to the differential trio receiver, only the Rx\_AB and Rx\_CA ends are used and the Rx\_BC is left unconnected. The configuration ensures the backwards technology compatibility between the C-PHY and D-PHY interfaces. [10]

## 3 THEORETICAL BACKGROUND

Signals can be transferred over a transmission line or a radio frequency link. Common for the both transmission types are the electromagnetic waves, which carry the signal. Even if the target is to send only digital bit values, high or low states in digital terms, in practice all of the digital signal transmission systems are based on analog technology. This thesis handles only the transmission over the transmission line. Usually a line is defined as a transmission line when the line is longer than the signal wave length. Deeper theory of the transmission line is based on telegraph equations. [12]

High frequency and an analog signal make a system more complex to understand. Analog signals and non-linear system generate several harmonic frequency components, which may behave differently from the nominal frequency depending on the transmission line features. [12]

In practical implementations, a non-ideal behavior of the signal is often handled under a term called signal integrity. It measures the quality of the transferred electrical signal. All analog signals always contain noise, loss or distortion. The typical signal integrity terms are described in this chapter. [13]

Any electrical network can be modelled by using network parameters. In this thesis, the network models are handled by using S-parameters, which are particularly useful for high frequencies and matched loads.

### 3.1 Transmission line theory

The dielectric transmission lines, such as the coaxial cables, the striplines and the microstrips, always have characteristic inductance and capacitance. These are related to the materials used, the permittivity and permeability of the dielectric medium and the transmission line's physical structure and dimensions. These define many transmission line factors, such as the characteristic impedance ( $Z_0$ ), the propagation delay, the wave length, the attenuation and the reflections. [13,14]

In order to understand the transmission line model, it needs to be first divided into infinite short slides ( $\Delta z$ ). The characteristic capacitance ( $c$ ) and the characteristic inductance ( $l$ ) are presented per length unit H/m or F/m (Figure 3.1). [13,14]

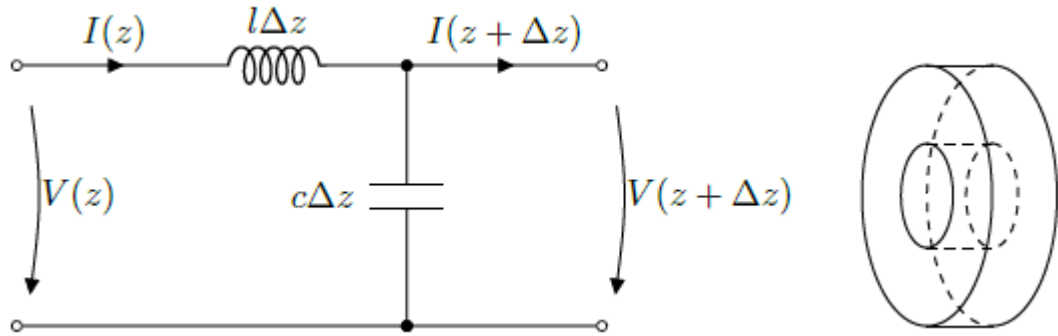


Figure 3.1 Model of lossless transmission line per length unit [14]

In practice, analog signals consist of several frequencies which behave differently in the transmission line. This is easy to understand when the capacitance  $C$  and the inductance  $L$  frequency relationship  $j\omega$  is added to the transmission line model (Figure 3.2). For example, due to the parallel capacitance, the signal loss for the high frequencies is higher than with the lower frequencies. [13,14]

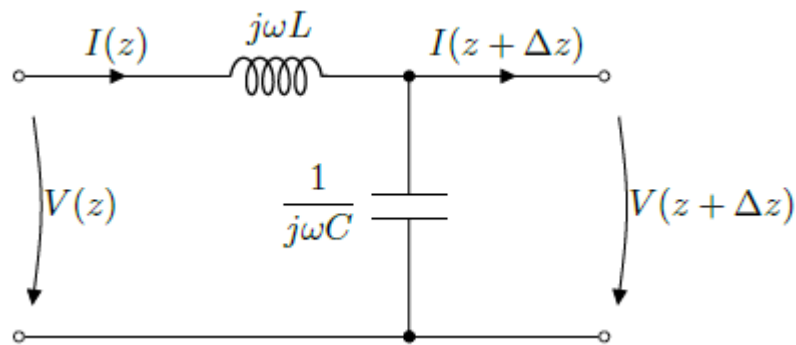


Figure 3.2 Impedances when input is sinusoidal at angular frequency of  $\omega$  [14]

### 3.1.1 Telegraph equations

Typically a length unit ( $\Delta z$ ) (Figure 3.2) is to be considered as an infinite short slide. This is because the transmission line features may vary over the line length. However, in theory if the detailed structure and parameters of the transmission line are known, the voltage and current over the transmission line can be defined in any single point by using the following telegraph equations. [14]

The voltage change over the inductor:

$$U(z + \Delta z) = U(z) - l\Delta z \cdot \frac{\partial I(z)}{\partial t} \quad (1)$$

The Equation (1) in simplified format:

$$\frac{\partial U}{\partial z} = U(z) - l \frac{\partial I}{\partial t} \quad (2)$$

The current change over the capacitor:

$$I(z + \Delta z) = I(z) - c\Delta z \cdot \frac{\partial U(z+\Delta z)}{\partial t} \quad (3)$$

The Equation 3 in a simplified format:

$$\frac{\partial U}{\partial z} = U(z) - l \frac{\partial I}{\partial t} \quad (4)$$

Telegraph equations for the lossless transmission line can be deduced by combining the Equations 2 and 4:

$$\frac{\partial^2 I}{\partial z^2} = lc \frac{\partial^2 I}{\partial t^2} \quad (5)$$

$$\frac{\partial^2 U}{\partial z^2} = lc \frac{\partial^2 U}{\partial t^2} \quad (6)$$

### 3.1.2 Characteristic impedance

One of the critical design parameters in high-speed design is the characteristic impedance  $Z_0$ . It is defined as a ratio of voltage and current along the transmission line and follows the Ohm's law (Equation 7). The unit for characteristic impedance is  $\Omega$ . [13,14]

$$U = Z_0 \cdot I \quad (7)$$

For the lossless transmission line, the characteristic impedance can be defined as

$$Z_0 = \sqrt{\frac{l}{c}} \quad (8)$$

where  $l$  is the inductance and  $c$  is the capacitance per unit length ( $\Delta z$ ). Because the value is defined as per length unit, the characteristic impedance is not line length depended. By contrast, the parameters  $c$  and  $l$  depend on the structure and the materials used in the transmission line. [13,14]

### 3.1.3 Signal reflections

Ideally the characteristic impedance over the transmission line is constant. However, in practical designs, the system includes many interfaces such as connectors. Very often the characteristic impedance is not exactly the same across these electrical discontinuity points. These signal mismatches cause reflections. [12]

The characteristic impedance and signal continuation are very important for the signal integrity. The signal reflections in a situation where the signal reflects back and forth between the two interfaces are causing attenuation, because finally the reflected signal energy is totally absorbed to the transmission line's resistive part. Secondly, a signal in some specific point in the transmission line is always the sum of the signals in the line. For this reason, the reflected signals may gain and attenuate the original signal, which may cause interference to the systems. [12]

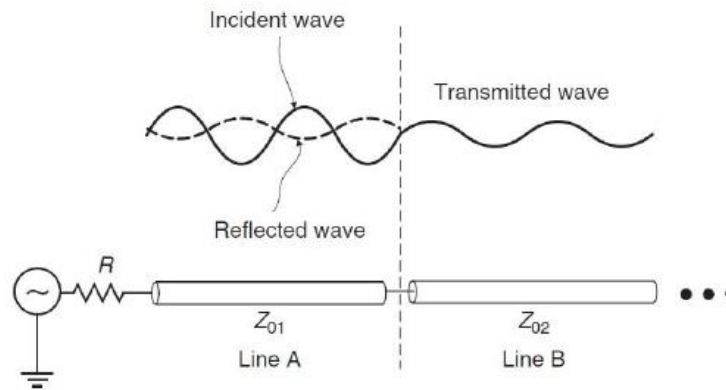


Figure 3.3 Discontinuity of electromagnetic wave [12]

The principle of reflection is presented in Figure 3.3. If the characteristic impedance  $Z_{01}$  is different from  $Z_{02}$ , some or all signal energy is reflected from the interface. The rest of the signal energy penetrates the interface called a transmitted wave in the figure. The quantity of the reflected signal depends on the reflection coefficient  $\rho_L$ , which is defined as. [12]

$$\rho_L = \frac{Z_{02} - Z_{01}}{Z_{02} + Z_{01}} \quad (9)$$

The reflection coefficient can be used to calculate voltage amplitudes.

$$\rho_L = \frac{V_{\text{reflected wave}}}{V_{\text{incident wave}}} \quad (10)$$

Similarly, the currents can be calculated by using the Ohm's law (Equation 7), when the voltage amplitude and the characteristic impedance of the transmission line are known. [12,14]

### 3.1.4 Propagation delay

The theoretical maximum speed of the electromagnetic wave is defined as the speed of light in a vacuum. For that reason, the propagated signal from the transmitter to receiver is always delayed. In the electrical transmission lines, the speed of the propagated signal is defined as phase velocity  $v_p$ . [12,14]

$$v_p = \lambda f = \frac{1}{\sqrt{lc}} = \frac{c_0}{\sqrt{\mu_r \epsilon_r}} \quad (11)$$

where  $\lambda$  is the wavelength,  $f$  is the frequency,  $l$  is the characteristic inductance and  $c$  is the characteristic capacitance,  $c_0$  is the speed of light in vacuum,  $\mu_r$  is the relative magnetic permeability of dielectric and  $\epsilon_r$  is the relative permittivity of the dielectric. [12,14]

As a conclusion from the equation (11), only the materials used affect the signal propagation speed  $v_p$ . In other words, the transmission line structure or dimension does not affect the phase velocity. [12, 14]

### 3.2 S-parameters

Scattering parameters, often called shortly the S-parameters, are used to express the properties of linear electrical networks. Other known network parameters are the Y-parameters, the Z-parameters, the H-parameters, the T-parameters and the ABCD-parameters. [12]

The S-parameters are especially used in RF-frequencies. The main difference from other formats is that the S-parameters are defined against matched load, typically 50  $\Omega$  but any other reference impedance can be used as well. Other parameters are defined against open or short circuits. The matched reference load is important with high frequencies, where practically short or open circuits do not exist, due to the parasitic capacitance and inductance. For this reason, the S-parameters are to be used for modelling high-speed transmission lines. [12]

When defining the S-parameters, any electrical network or transmission line can be regarded as a black box including passive RLC-components or an active circuit such as an amplifier. The parameters define the relationship of one or more black box ports, when the voltage is supplied to one port and measured from the another port. [12]

The S-parameters are typically presented in a square matrix format. The simplest matrix format is 1 x 1 (one-port model) but the matrix size can be N x N and contain  $N^2$  elements. The matrix elements include a voltage gain value and a phase angle or similarly the matrix can be presented in a complex number format. [12]

Because the RLC-network behavior always has a dependency to the used frequency, it is highly important to understand that a wideband system needs to be modelled in the whole frequency band. This means that the S-parameters must be sampled over that band. [12]

### 3.2.1 Two-port model

The two-port model can be used to model any two port linear network, such as a cable or transmission line. Typically one port includes a signal path and a ground plane or a cable shield. The arrows and symbols in Figure 3.3 present the power directions inserted or removed from the network. [12]

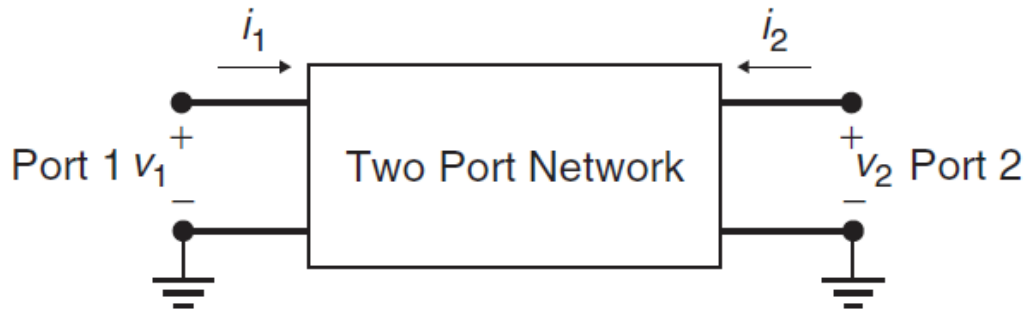


Figure 3.4 Two-port network model [12]

The two-port S-parameter matrix consists of four elements:

$$S = \begin{bmatrix} S_{11} & S_{21} \\ S_{12} & S_{22} \end{bmatrix} \quad (12)$$

where

- $S_{11}$  reflection coefficient or reflection loss of input port 1
- $S_{21}$  Insertion loss or forward voltage gain from port 1 to port 2
- $S_{12}$  Isolation or reverse voltage gain from port 2 to port 1
- $S_{22}$  Reflection coefficient or reflection loss of output port 2

The relationship of the ports can be calculated by using the S-matrix:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{21} \\ S_{12} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad (13)$$

where

- $a_i$  is a stimulation to port  $i$
- $b_j$  is a response from port  $j$

The model can be used to define the test fixture S-parameters. [12]

### 3.2.2 Four-port mixed-mode model

Four port models contain sixteen S-parameter elements. Two different models can be used: standard four-port model for single ended signals or mixed-mode model for the differential signals. In Figure 3.5, the lines can be considered as positive and negative differential lines.



Figure 3.5 Four port differential DUT model

In the balanced signal, such as the differential lanes, the mixed-mode S-parameter model is to be used. The differential-mode and the common-mode parameters need to be defined to each port. The matrix parameters present the differential-mode ( $d_i$ ) and the common-mode signals' ( $c_i$ ) relationships (Equation 14).

$$S = \begin{bmatrix} Sd_1d_1 & Sd_1d_2 & Sd_1c_1 & Sd_1c_2 \\ Sd_2d_1 & Sd_2d_2 & Sd_2c_1 & Sd_2c_2 \\ Sc_1d_1 & Sc_1d_2 & Sc_1c_1 & Sc_1c_2 \\ Sc_2d_1 & Sc_2d_2 & Sc_2c_1 & Sc_2c_2 \end{bmatrix} \quad (14)$$

where [12]

- Sdd: Driver and receiver are differential.
- Scc: Driver and receiver are common mode.
- Sdc: Driver is common mode and receiver is differential.
- Scd: Driver is differential mode and receiver is common mode.

The upper left corner ( $S_{didj}$ ) in the matrix describes the system performance with a differential stimulus and response. The others describe for example the cross-talk effect between the differential lines. Logically the mixed-mode parameters can be used as any other S-parameters. The first  $d_x$  or  $c_y$  parameter corresponds to the port response and the second one is the port stimulation source. For example the  $S_{c1d2}$  presents the port1 common-mode response stimulated by the differential-mode port2. [12,15]

### 3.2.3 One-port model

The one-port model is the simplest model. The model only defines the single port reflection coefficient or reflection loss called the S11 parameter. In practice it measures the termination quality against the ideal 50  $\Omega$  pure resistance.

$$S = [S11] \quad (15)$$

The model can be used to define the reflections from a receiver or a transmitter. [12]

## 3.3 Differential and single-ended signaling

Slow speed bus interconnections are typically implemented by using single-ended connections. The maximum reachable data rate per single-ended line is approximately 1 to



2 Gbps. With higher speeds, the signal integrity becomes challenging because the high-speed systems are often very noisy. [12]

Figure 3.6 demonstrates the effects of a single-ended line noise. The signal received is clearly corrupted compared to the received ideal signal. The receiver needs to detect the received bit value, logical 0 or 1, based on the reference voltage value. If the received signal is very noisy, it may cause bit detection errors for the received data. [12]

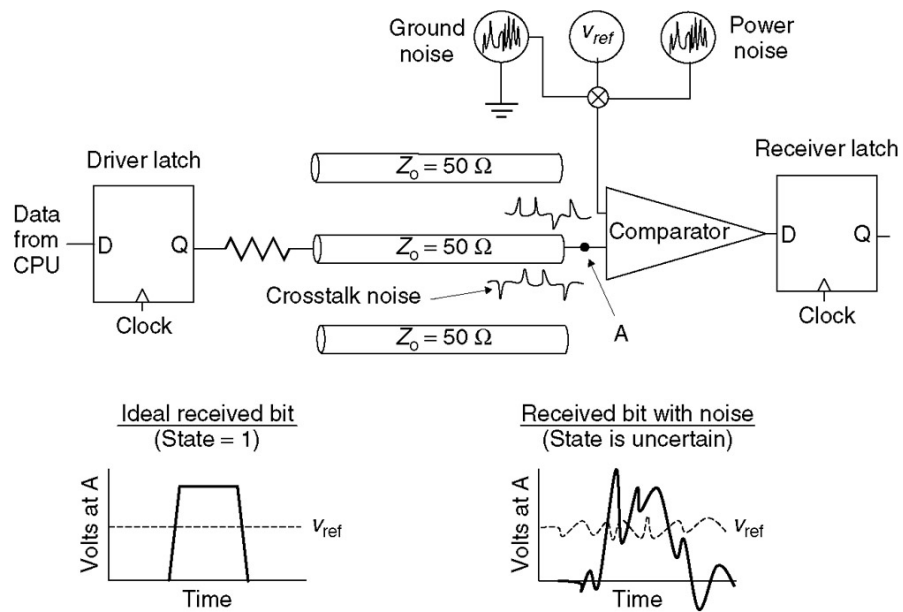


Figure 3.6 Principle of the single-ended transmission line [12]

Differential signaling is used with higher data rates or when a more reliable data transmission method is needed. It is based on a technique where two transmission lines D+ and D- (Figure 3.7.) drive the same signal data 180° out of phase. The difference of the received voltage is used to recover data at the receiver end by a differential amplifier. [12]

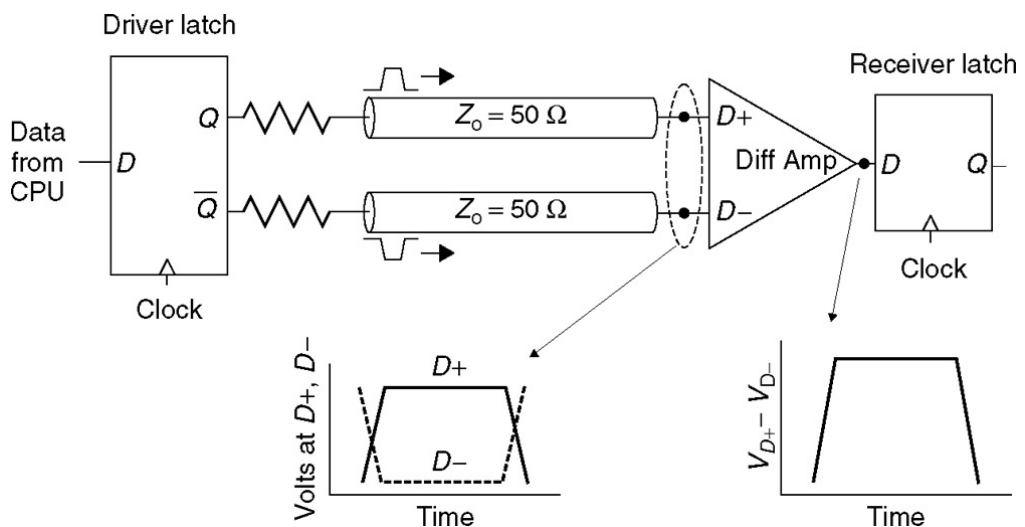


Figure 3.7 Principle of the differential transmission line [12]

The advantage of differential signaling is the ability to reject common-mode noise. The idea is based on data lines which are routed as pairs close to each other. For that reason, the noise on the D+ and the D- lines is approximately the same and the noise can be rejected. [12]

Equation 16 and Figure 3.8 demonstrate the differential common-mode noise rejection theory and behavior. [12]

$$V_{diff} = (V_{D+} + V_{noise}) - (V_{D-} + V_{noise}) = V_{D+} - V_{D-} \quad (16)$$

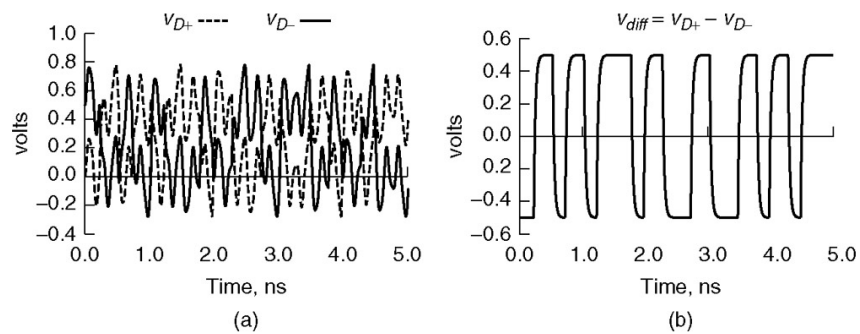


Figure 3.8 Rejection of common mode noise with differential signaling [12]

### 3.4 High-speed signal integrity

Signal integrity is a set of different measures to define the quality of the transmitted signal. Ideally, when an analog voltage signal is transmitted over a transmission line, it can be received without any distortion. In the real world, many things affect the signal which limits the bandwidth and the maximum transmission line distance.

In theory, the ideal system in digital communications has a wide bandwidth without errors. A typically used quality parameter for system reliability is the bit error rate (BER), which can be considered as the amount of errors per total number of bits during a time period. To ensure a low or error free BER value, the signal integrity (SI) needs to be considered as a system design parameter. [12]

#### 3.4.1 Attenuation

When a signal is transmitted over the electric material, some signal energy will always be absorbed to the transmission line or radiated out from the system. This is also called a signal insertion loss. The two-port S-parameters  $S_{ij}$  directly represents this behavior.

The attenuation is not typically a major issue in short transmission lines, such as in mobile devices. However, the attenuation parameter is always a frequency dependent and it is not constant over the frequency range. That may cause some distortion to the received signal. [12]

### 3.4.2 Jitter

In theory, ideal clocks are stable and the variation of the clock pulse period is zero. However, in practice any clock always includes a frequency domain variance, called jitter. In other words, frequency is not stable, which causes timing variation. The jitter affects signal timings and is a limiting factor for the bandwidth in the digital communications. Commonly used method to see the jitter effect is a measure signal eye-diagram (Figure 3.9). [12]

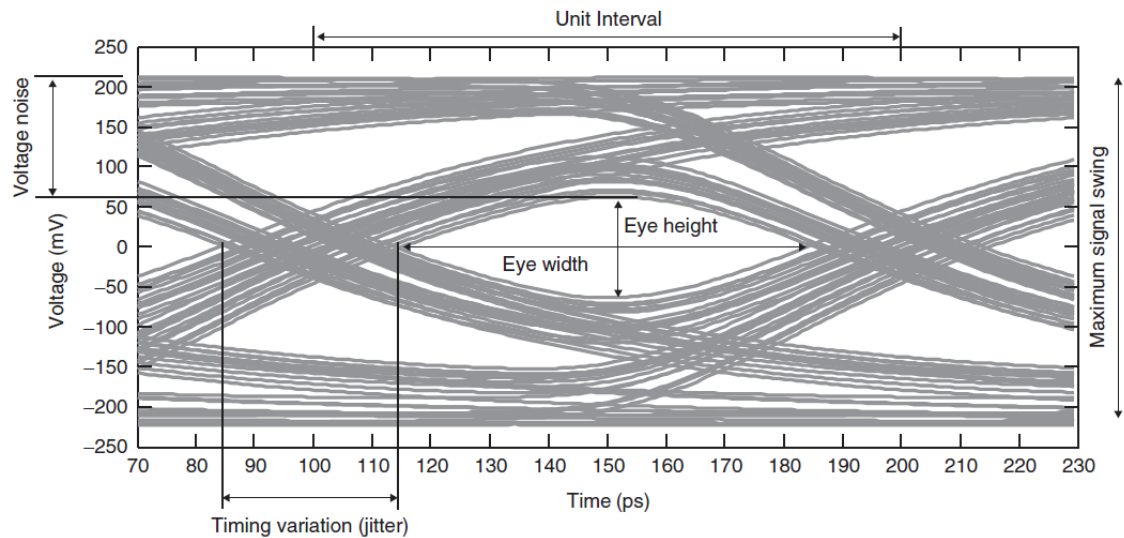


Figure 3.9 Jitter in Eye-diagram [12]

Jitter can be divided into two main classes; random and deterministic jitters. Additionally, deterministic jitter can be divided into several source types. [12]

- Random Jitter (RJ), caused by thermal and noise effects. Typically Gaussian distribution.
- Deterministic Jitter (DJ) sources
  - Sinusoidal Jitter (SJ), periodic frequency components
  - Data Dependent Jitter (DDJ)
    - Duty Cycle Distortion (DCD), caused by voltage offsets between differential inputs and differences between transition times within a system.
    - Intersymbol Interference (ISI), caused by long / short bit cycles
    - Bounded Uncorrelated Jitter (BUJ), caused by cross-talk

### 3.4.3 Cross-talk

Cross-talk means a situation where a signal transmitted through the transmission line or any other system part causes an unwanted effect to some other system part. For example, in differential lines which are routed as pairs, positive and negative lines may cause

interference to each other. The cross-talk can be generated inductively via magnetic fields or capacitively through electrical fields between two system parts.

When the signal propagates in a dielectric transmission line, it always carries a current, which creates a magnetic field around the transmission line. If the two lines are close enough of each other, the magnetic fields cause unwanted interference to the another line. In other words, the magnetic field causes current to the another line.

A second common cross-talk mechanism is the capacitance between system parts. In that case, the energy from one to another system part is transferred via electric field. [12]

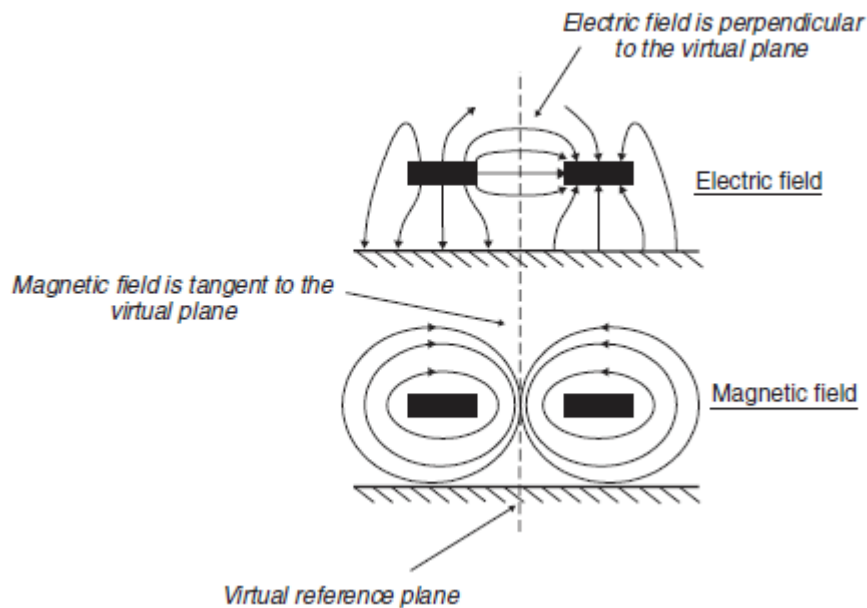


Figure 3.10 Differential Cross-talk [12]

#### 3.4.4 SKEW

Skew represents the signal clock and data lane timing offset. The reasons for skew are jitter, different signal propagation delay in dielectric material between the signal lines, different signal trace lengths, and transmitter-end clock and data timing variation. [12]

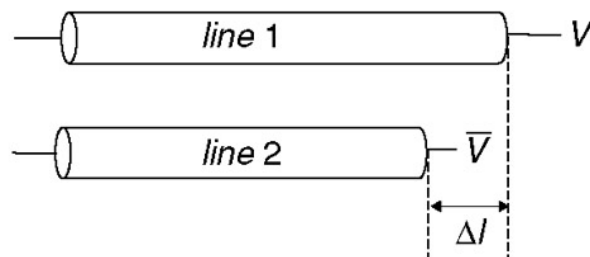


Figure 3.11 Routing length difference ( $\Delta l$ ) in differential data-pair [12]

In the double data rate (DDR) technology, such as used in the MIPI D-PHY, the data read speed is double compared to the system frequency. The data lane states are read every time when the differential clock lane changes the state and the data lane state changes are synchronized into the middle of the clock UI-period. For reliable system functionality, the signal needs to fill a timing budget. These timing parameters are called  $t_{\text{setup}}$  and  $t_{\text{hold}}$  times and the parameters have a direct relationship to the skew parameter, which is defined as the clock and data deviation from the ideal timing. The basic functionality and timing diagram is presented in Figure 3.11. [8]

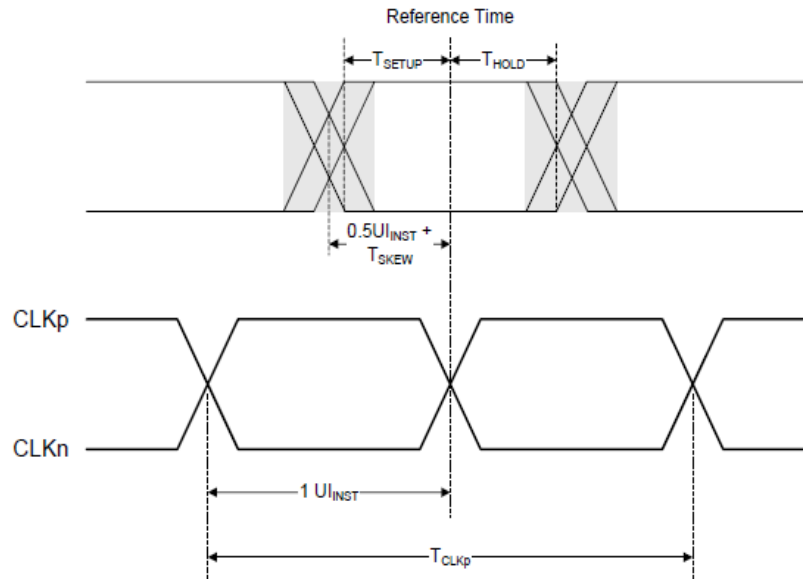


Figure 3.12 DDR signal skew definition [8]

In the MIPI D-PHY specifications all values are specified the same way:

$$t_{\text{SKEW}} = t_{\text{SETUP}} = t_{\text{HOLD}} = 0,2 \cdot \text{UI}_{\text{INST}} \quad (17)$$

where  $\text{UI}_{\text{INST}}$  is the Unit Interval time.

## 4 MEASUREMENT SYSTEM

The measurement system precision works as the weakest link in the chain. For that reason, it is very important that all of the test fixtures are well designed and the measurement tools are suitable to handle the high speed signals without distorting the actual measured signal. The test fixtures must pass a differential high speed signal without significant insertion loss or impedance mismatches on the data path [8]. Otherwise, the measured signal could be distorted and the measured results are not valid. The test fixture is presented in Chapter 4.1.

Valid measurement devices and tools are as important as the test system itself. In high speed signals, the sampling rate is one of the key features. Fast signals include several harmonics frequencies which are important for the final signal waveform. The fastest rise and fall times can be used in order to define the needed sampling rate. This ensures the required bandwidth. Third thing is to minimize the load which is caused from the probes to the device under testing. These factors are defined in Chapter 4.2.

### 4.1 Verification environment

In order to measure high-speed signals, the verification system needs to be well specified, designed and built by using high-quality components. The MIPI D-PHY signal path is built by using two test fixtures, a termination board, cables and additionally a test control unit to control the camera and to supply the needed powers. A setup block diagram is presented in Figure 4.1.

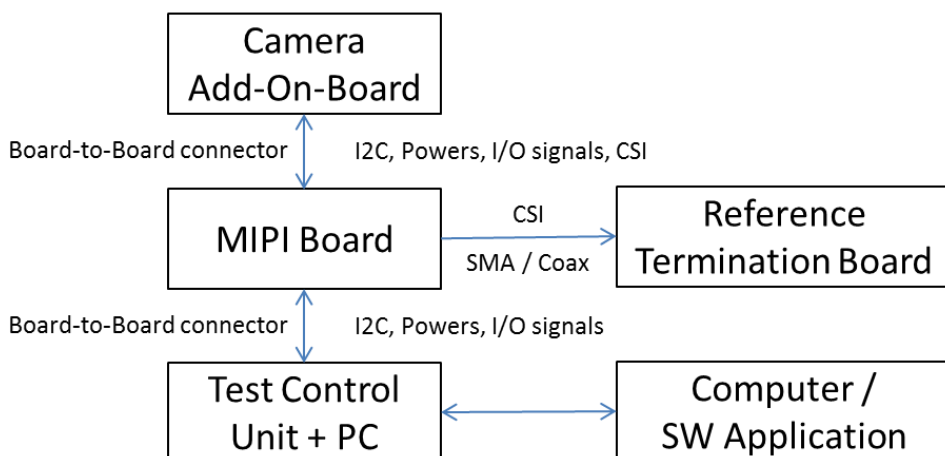


Figure 4.1: MIPI D-PHY test system block diagram

- Camera Add-On-Boards (AOB) to connect camera to the system.
- MIPI camera adapter board to pass camera CSI signals to the RTB board.
- SMA-cables to connect the MIPI boards.
- MIPI D-PHY Reference Termination Board (RTB) for the CSI2 signal termination.
- PC and the SW application

In a normal case, the control unit is directly connected to the camera add-on-board and terminates the CSI-signal. In the MIPI D-PHY verification setup, the MIPI adapter board is used to route the CSI-signals from the camera add-on-board to the SMA-connectors and to pass the signal to the reference termination board.

#### 4.1.1 Camera Add-on-Boards

Camera add-on-boards (AOB) connect the camera to the test system. Typical connection methods are sockets and flexes. The socket is a metallic camera holder for the module assembly. The contact to the camera bottom is implemented by using pogo pins. Most of the high-end cameras use flexes due to a flexible product design and camera module size. The board-to-board connectors are used to connect the camera to the test system or boards which give a better signal integrity performance than the pogo pins.

The board-to-board connector interfaces in the test system are specified up to 8 GHz / 16 Gbps differential lane-speed.

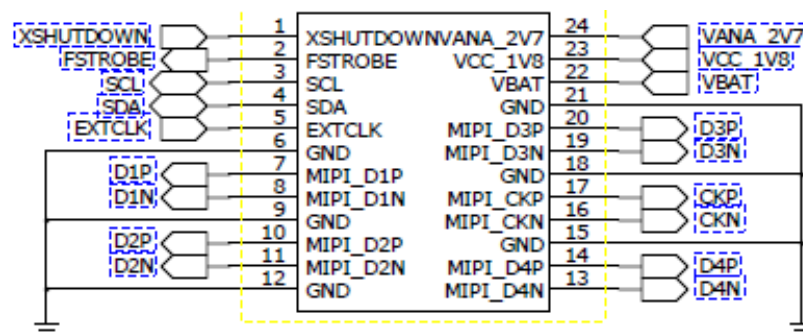


Figure 4.2: Typical four lane camera connector pinout

On the camera add-on-board, the CSI-signals are routed as pairs without ground isolation between the positive and the negative differential lines (Figure 4.2). The pairs are isolated with ground planes from the other pairs or signals. All of the differential signal line lengths are matched to avoid propagation delay difference and skew timing issues.

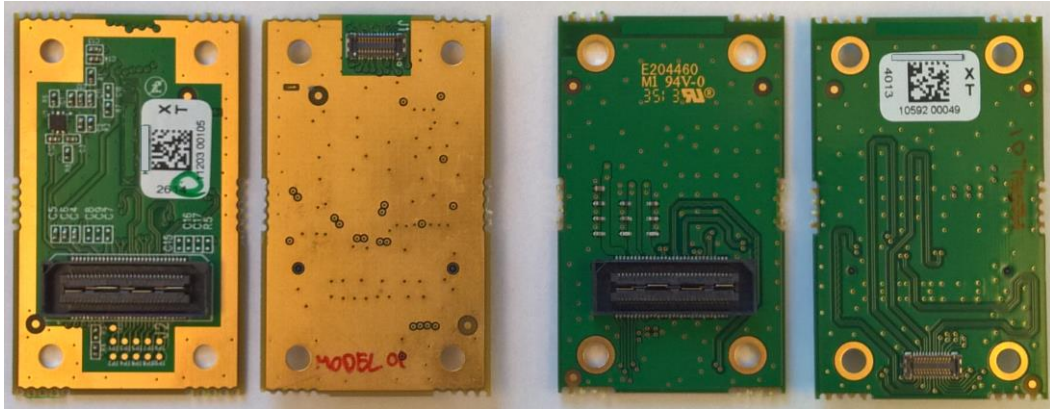


Figure 4.3 Camera Add-On-Boards. Four and two layer designs

Examples of the board designs are presented in Figure 4.3. Both, a stripline and microstrip signal routing can be used in the design and the same level of signal integrity quality can be achieved with both options. The left-hand side board layout uses a four layer design and the both design types are used. The advantage of the design is a ground plane on the top side. The target of the design is to use the same boards also in the camera module EMC verification. The right-hand side layout design uses only two layers and microstrips. Additionally, configuration options, power source PSSR filters and power regulators can be added to the camera add-on-boards when needed.

#### 4.1.2 MIPI camera test board

The MIPI test board is a test fixture to connect the camera add-on-boards to the MIPI D-PHY reference termination board (RTB) and the test control unit. The purpose of the MIPI camera test board is to route the differential CSI lines to the SMA connectors.

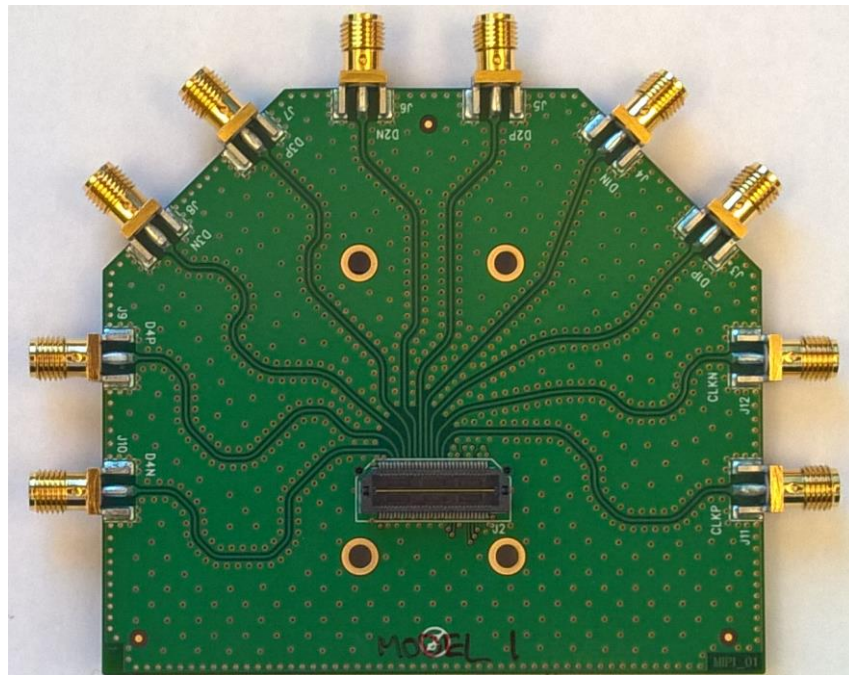


Figure 4.4 MIPI adapter board



The board is assembled between the test control unit and the camera add-on-board. The camera control I/O-signals and powers are routed through the board from the test control unit to the camera module. The differential signals are routed only from the camera connector to the SMA-connectors, not to the control unit end. This ensures the maximum signal integrity.

In board layout design, the microstrips are used for the CSI-trace routing. The lines are clearly visible on the board in Figure 4.3. All of the line lengths are matched to avoid propagation delay issues. Another design consideration is the signal isolation. The spacing between the lines is enough to avoid crosstalk between the lines. Additionally, the lines are matched to nominal 50 ohm differential impedance. These three are the main design rules which ensure the high quality signal integrity.

#### 4.1.3 MIPI D-PHY Reference Termination Board

The MIPI D-PHY Reference Termination Board (RTB) is a reference termination test fixture for the MIPI D-PHY signaling measurements. The board emulates the standard receiver end termination in the High-Speed (HS) and the Low-Power (LP) modes. The test fixture is designed for repeatable and consistent measurements in order to verify the MIPI D-PHY transmitter performance. The test fixture is commonly used and publicly available. [16]

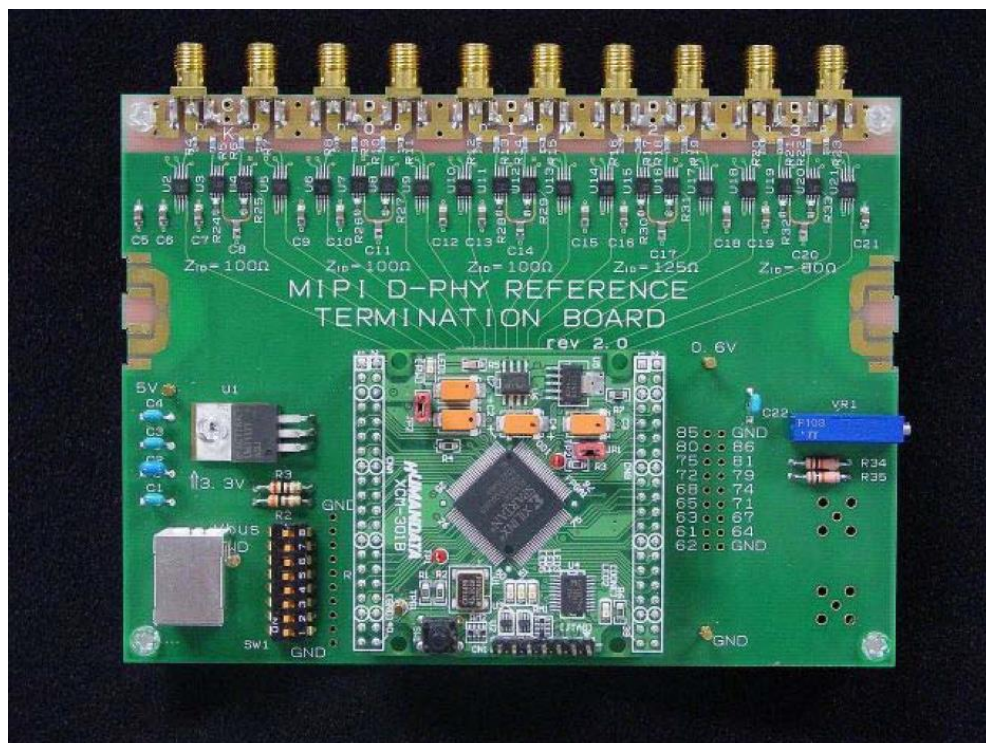


Figure 4.5: MIPI D-PHY Reference Termination Board (RTB) [16]

The board offers an ideal resistive 100  $\Omega$  termination and in the worst case 80  $\Omega$  and 125  $\Omega$  terminations, which are the D-PHY specification limits. The clock input and two of the data lines are terminated with the ideal 100  $\Omega$  resistance and two others with the

limit values  $80 \Omega$  and  $125 \Omega$ . The termination is controlled by a FPGA according to the MIPI D-PHY LP-signaling protocol. [16]

The signal is to be measured as close as possible to the termination resistors to avoid possible reflections in the measured signal. For the best performance, it is recommended to use solderable active probe heads.

#### 4.1.4 Test control unit

A test control system is a research and development tool, which is designed to control the camera sensor and capture picture data. The system parts include the physical device and the PC control software.



Figure 4.6 Scooby2 platform unit for Image sensor analysis [14]

The device works as a host control unit, such as the camera sub-system in mobile devices, including: a processor, I/O interfaces, power regulators and a CSI receiver. The unit is able to control the camera, supply the needed powers, receive sensor picture data and pass data to a PC. The camera add-on-boards and sensor can be directly connected to the Scooby2 unit or alternatively in the MIPI D-PHY interface verification use cases, it works only as a control unit, where the CSI data is routed to the termination board.

The software application is used to control the test system and camera sensor. All of the camera parameters used can be set in that application. The application used is compatible with the SMIA standard control features. [17]

### 4.1.5 Coaxial cables

Standard 50  $\Omega$  coaxial cables with SMA-connectors can be used. However, it is highly recommended to use high-quality shielded cables and connectors to avoid impedance discontinuation and reflections which may cause distortion for the signal integrity and results.

The used cable length should not be longer than 0,25 m. The maximum total transmission line length 0,3 m is defined in the MIPI D-PHY specification. All coaxial cable lengths need to be phase matched. Differences in the cable lengths cause propagation delay difference and affect the signal timings [8].

## 4.2 Measurement devices

For accurate measurements, it is essential to understand the measurement device requirements. Measurement devices affect the results and optimal devices give the best results. For the laboratory engineers, this is not often well known or understood.

One of the key parameters is the system bandwidth. The calculations are not as simple as Dr. Nyquist defines them. The optimal bandwidth requirement can be mathematically calculated based on the specification data. [18, 19]

Another important feature is to understand the load caused by the measurement device to the signal under testing. All probes or tools are not suitable for accurate measurements.

### 4.2.1 Required measurement device bandwidth

In theory, an ideal signal is a sine wave which consists of only one frequency component. In practice, the signal wave always includes several harmonic frequencies, which are mandatory to build and present the final signal wave.

Nyquist's sampling theory defines that the sampling rate needed for accurate measurement must be greater than twice the maximum signal frequency. However, for the digital signals, where the edges are very fast, harmonic frequency components play a big role. For that reason, a significantly higher sampling rate and bandwidth are needed than Nyquist has defined. [18,19]

Oscilloscopes over 1 GHz bandwidth typically use a maximally-flat frequency response filter. Lower than 1 GHz oscilloscopes use a Gaussian type filter. The filter responses are presented in Figure 4.4. [20]

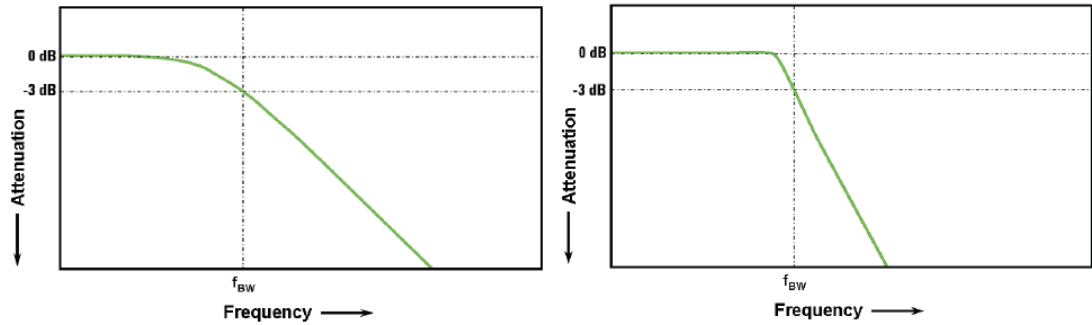


Figure 4.7: Oscilloscopes with Gaussian and maximally-flat frequency responses [20]

The advantage of oscilloscopes with maximally-flat frequency response, is that the scope attenuation for frequencies near the bandwidth limit is better than in the Gaussian type filter, where the signal starts to attenuate earlier from the 3 dB point than with the maximally-flat response.

For the analog signals a basic rule of thumb for the oscilloscope bandwidth, is that the measured signal contains frequency components up to the fifth harmonic. [20]

$$f_{BW} = 5 \cdot f_{CLK} \quad (18)$$

However, for the digital signals the more critical rule to define the needed bandwidth is the fastest edges such as the signal rise ( $t_r$ ) and fall ( $t_f$ ) times. The MIPI D-PHY specification v1.1 supports lane speed up to 1.5 Gbps (750 MHz). The minimum rise and fall time in the MIPI D-PHY specification is defined as 100 ps. [8,20]

The fastest required edges can be used to calculate the knee frequency. It defines the highest practical frequency component which is needed to present signal without distortion. [20]

$$f_{knee} = \frac{0.4}{RT(20\%-80\%)} = \frac{0.4}{100 \text{ ps}} = 4 \text{ GHz} \quad (19)$$

where  $f_{knee}$  is the needed test system bandwidth and RT is the definition of signal rise and fall times. The calculated knee frequency is 4 GHz.

Furthermore, the knee frequency can be used to define the needed oscilloscope bandwidth and accuracy of the measurement. Based on the Equations (19), the needed oscilloscope bandwidth can be defined as a function of accuracy. The calculations are presented in Table 4.1. [20]

Table 4.1: Oscilloscope bandwidth requirement [16]

Required Accuracy	Maximally-flat response	Required Bandwidth $f_{knee} = 4 \text{ GHz}$
20%	$f_{BW} = 1,0 \cdot f_{knee}$	4,0 GHz
10%	$f_{BW} = 1,2 \cdot f_{knee}$	4,8 GHz
3%	$f_{BW} = 1,4 \cdot f_{knee}$	5,6 GHz

Based on the MIPI D-PHY specification v1.1, the needed minimum oscilloscope bandwidth in order to measure accurate results is 6 GHz.

#### 4.2.2 Oscilloscope

The selected oscilloscope can be any model which fulfils the requirements presented in Table 1. In this reference setup, the used oscilloscope model is Agilent Infiniium DSA90804A.

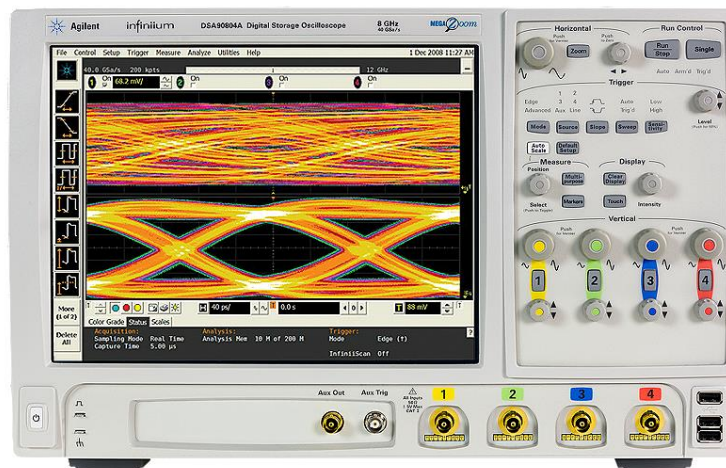


Figure 4.8: Agilent DSA90804A [21]

Agilent Infiniium DSA90804A key feature parameters are: [21]

- 8 GHz bandwidth
- 40 GSA/s on each of 4 analog channels
- 50 Mbps memory per channel
- Noise floor 2,22 mV at 100 mV/div
- Support for several test and debug applications such as the MIPI D-PHY compliance application

#### 4.2.3 Oscilloscope probes

When measuring high speed signals, active probes must be used. A traditional passive probe's usable bandwidth is generally limited around 1 GHz and is not suitable in high-speed applications. The active probes can handle signals up to 30 GHz. [22]

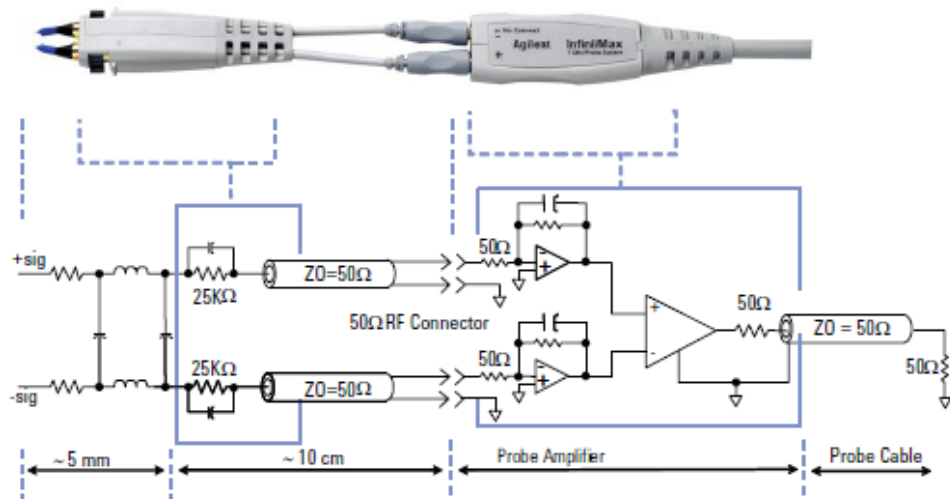


Figure 4.9: Agilent Infiniimax active probe architecture [23]

The dimensions of the connection circuit under testing define many key electrical parameters. The referred Agilent active probe architecture is presented in Figure 4.9. The probe heads are separated from the probe amplifier and the smaller probe head dimensions significantly reduce the load capacitance and inductance. The active probes do not cause significant load impedance to the circuit under testing. That makes the biggest difference versus the passive probes, where the load impedance and especially the capacitance can be very high compared to the device under testing. [23]

The active probes support differential and single-ended measurements. In the differential mode, the probe heads are directly connected to the differential positive and negative signals. The measurement method is valid, if a common mode voltage level is not needed, for example in protocol encoding. [23]

In the MIPI D-PHY measurement, the common mode voltage level is one of the key parameters. The signals need to be measured in the single-ended mode, where the positive probe head is connected to the signal and the negative probe head to the system ground.



Figure 4.10: Solderable active probe head (Agilent E2677A 12 GHz) [22]

The active probe type used is the Agilent 1134A (7 GHz). The probe is connected to the test fixture by using a solderable probe head E2677A (12 GHz). The solderable probe heads are suitable for constant setups and offer the best and most reliable connection to the test fixture. [22]

The key probe setup parameters for the D-PHY layer version 1.1 measurements: [22]

- Active probe bandwidth 7 GHz
- Probe head bandwidth 12 GHz
- Rise and fall time 60 ps
- Total load parameters in single ended mode
  - Resistance 25 k $\Omega$
  - Capacitance 0,44 pf
- Slew rate 18 V/ns
- Noise referred to input 3 mVrms

#### **4.2.4 MIPI D-PHY compliance test application software**

The used oscilloscope supports several automated compliance test applications. In this case the used application is the MIPI D-PHY compliance application. The test application is fully automated and tests all timing and voltage level parameters defined in the interface specification. [24]

The advantage of the automated test applications is the reliability of the result. Compared to manual testing, the automated test applications can use much more data for the result capturing. Manual testing is often based on only one signal waveform, which creates uncertainty to the results. Secondly, the automated applications are faster and tests can be looped to see variation in the results. [24]

As a final result, the application summarizes all of the measured parameters, shows the specification limits and the result margins of these limits. Additionally, the result summary includes screen captures from the signal waves, which helps the test engineers to detect possible root causes in fail cases. [24]

#### **4.2.5 Test automation**

Optionally, the test setup can be fully automated in order to measure all four multi-lane channels. The current limitation is that only one channel can be measured without disconnecting the cables. In long term use, connector wearing may cause impedance mismatch to the transmission line and cause signal distortion and unreliability to the measurements.

With the switch matrix, there is no need to disconnect the cables. The switch matrix connects data-lane signals to the scope inputs. A clock is needed with all measurements and can be connected directly to the oscilloscope. [25]

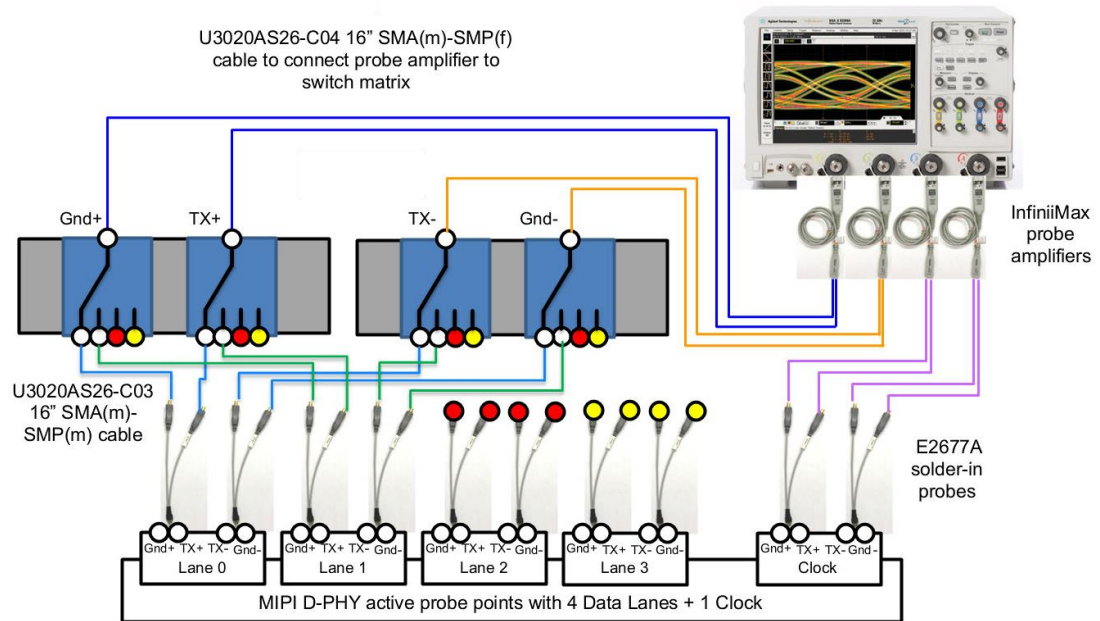


Figure 4.11 MIPI D-PHY fully automated 4-lane switch matrix option [25]

The switch matrix is to be used with the Infiniisim software to de-embed the test fixture effect. The de-embedding feature is presented in the next chapter.



## 5 CAMERA MODULE SIGNAL INTEGRITY VERIFICATION

Verification is an important part of the product creation chain and commercial products must fulfil several specifications in order to get approval to the market. The process is highly important especially for mass products, where customers expect high-quality devices without any functional issues. For the manufacturer, the quality corresponds more or less directly to warranty costs and causing harm to the company brand as well. Secondly, research and development costs for complex devices and components are very high and potential issues need to be found as an early phase as possible.

The system or system parts need to be verified in order to ensure functional and quality targets. The device needs to fulfil several generic standards such as the RF-connectivity and wired interfaces. At the same time, the device needs to be robust for the EMC interference, or similarly cannot cause interference to other system parts or other devices within definition limits. Additionally, the device components need to fulfill their own technical specifications such as the D-PHY and I2C in the camera interface case.

Typically, electrical engineers have two ways to ensure device functionality and signal integrity. These are simulations and measurements. Simulations are often used in early product design phase when the real hardware is not yet available, when changes to existing design are needed or any other cases when measurements are not possible. Measurements are used to verify a final product by measuring the actual signal behaviors.

### 5.1 Camera module signal integrity measurement

The purpose of the signal integrity verification is to ensure reliable system functionality. In the MIPI D-PHY interface case, it consists of electrical and timing parameters for the transmitter, transmission line and receiver system.

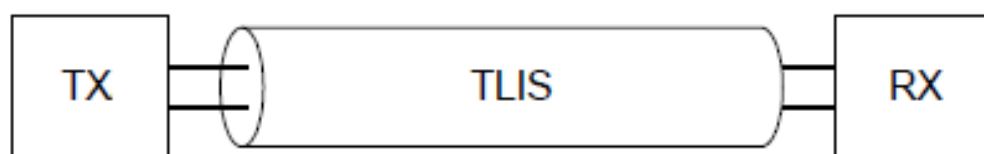


Figure 5.1 Transmission-Line-Interconnect-Structure [8]

In principle, the modules are already verified by component suppliers, but in the device manufacturer side some sensor register parameters are typically changed, which may affect the camera module signal output. A typical parameter is the frequency. Especially, many timing parameters are frequency dependent and do not behave linearly as a function of the frequency and all combinations cannot be tested by the component supplier. Electrically the transmitter drive strength is constant, which limits the maximum frequency by limiting the signal rise and fall times. Additionally, the interface specification includes parameters for the single ended and common mode voltage levels, the rise and fall time requirements and the receiver side requirements. As a summary, the target is to ensure system functionality in all target devices with the used settings.

The test system software application is built in a way that it uses exactly the same register settings which are used in the target devices. This ensures that the test setup works as closely as possible to the device setup and the results are comparable.

## 5.2 De-embedding

De-embedding is a combination of simulations and measurements. It is in practice a measurement, but the mathematical S-parameter models are used to create transfer functions to manipulate the measured signal. For example, the effect of the test fixture or cables can be removed from the measurement result. The de-embedding application is running in an oscilloscope and the corrected results are directly available without post processing. [24]

In Figure 5.2, the TLIS (Transmission-Line-Interconnect-Structure) represents a test fixture which can be modelled by using the S-parameters and can be removed from the final results. It is also possible to model the D-PHY transmitter and the receiver S-parameters.

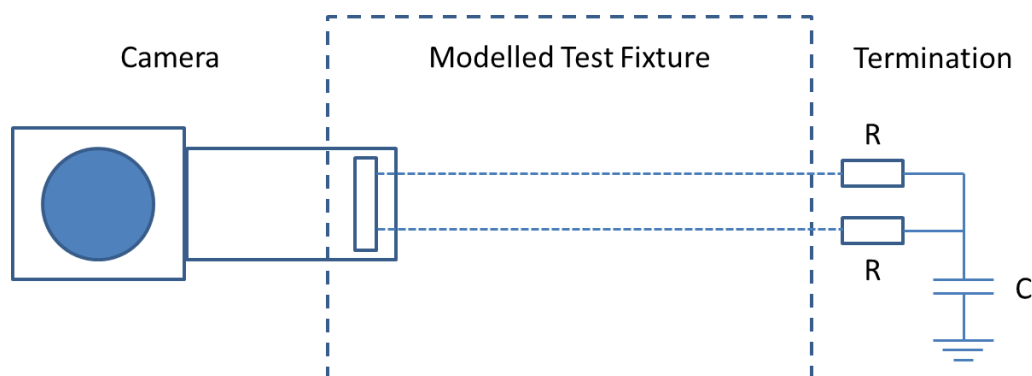


Figure 5.2 De-embedded camera model

Especially, the de-embedding is needed with the type of system presented in Figure 4.11, where the automated verification setup is built through a switch matrix. Long cables and the switch itself cause distortion, propagation delay and attenuation to the measured signal. The de-embedding feature is able to compensate these by using gain and phase shift corrections over the selected bandwidth range.

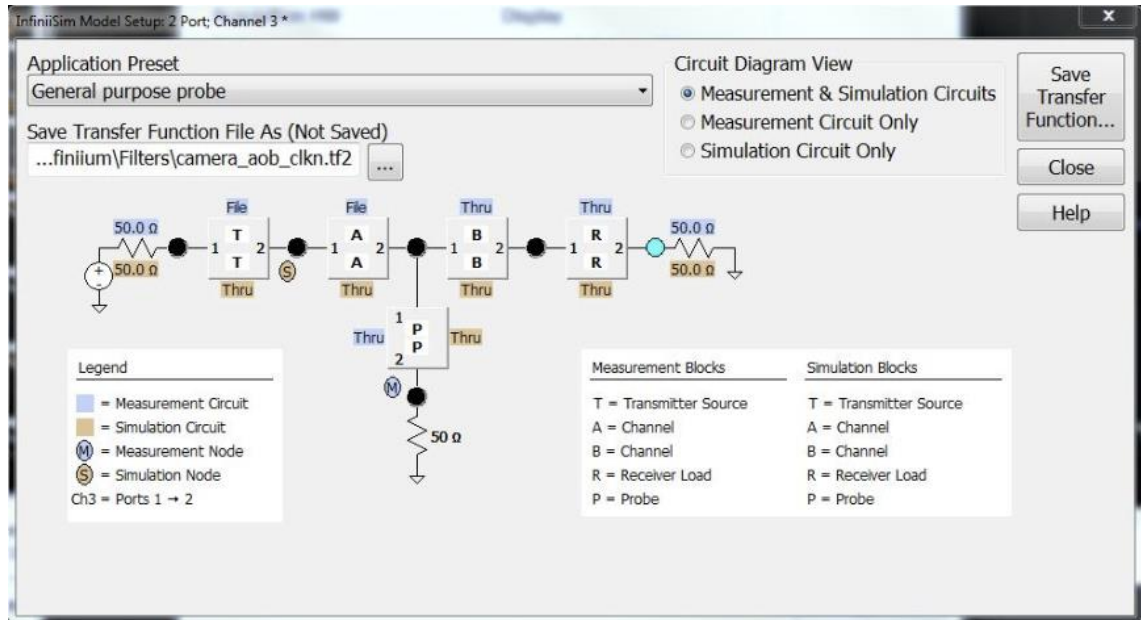


Figure 5.3 InfiniiSim transfer function setup interface window

A generic transfer function model creation setup structure is presented in Figure 5.3. The model can be created by using blocks. Every block can contain a different type of model, which are: an ideal through, an open, a transmission line (lossless), a S-parameter file, a RLC-circuit or a combination of sub-circuits. [24]

In the test fixture transfer function model case, there is only need to use the measured test fixture and the cable S-parameter models and additionally a one-port probe model to create a transfer function.

### 5.3 Test fixture model creation

As described in Chapter 3.2, the S-parameters are frequency specific. Different frequencies have a different gain and phase. For that reason, the S-parameters need to be sampled over the frequency band. In the test device application (Keysight InfiniiSim), the minimum requirements for frequency sample spacing are defined in the scope application guide as  $>1/(4 * t_{\text{delay}})$ , where  $t_{\text{delay}}$  is the cable signal propagation delay [24]. The same spacing is to be used in the measured or simulated models.

The S-parameter model is recommended to be measured instead of software simulations, whenever it is possible. Often the measured models are better than the simulated ones, because the whole test fixture transmission line frequency and delay response is

included in the created model, including the component variances. Secondly, accurate simulation models are not always available for all test fixture elements.



Figure 5.4 Roche&Swarz Vector Network Analyzer [26]

Differential S-parameters can be modelled by using the Vector Network Analyzer (VNA). The differential modelling needs a 4-port network analyzer with a frequency bandwidth which is wider than the oscilloscope bandwidth used. In that case, when using a 8 GHz oscilloscope and 7 GHz probes, the upper bandwidth is around 8 GHz. The lower bandwidth is limited by the VNA preferences. The VNA's cannot measure DC or low frequency components. The lowest supported frequency in the VNA used, is 10 MHz, and the S-parameter models are created by using a frequency band between 10 MHz – 8.01 GHz and with a 10 MHz frequency spacing. [24,27]

The MIPI D-PHY specification specifies the test conditions for the S-parameter measurements. The differential transmitter or receiver can be modelled by using a two-port model. The differential two-port model measurement is presented in Figure 5.5. [8]

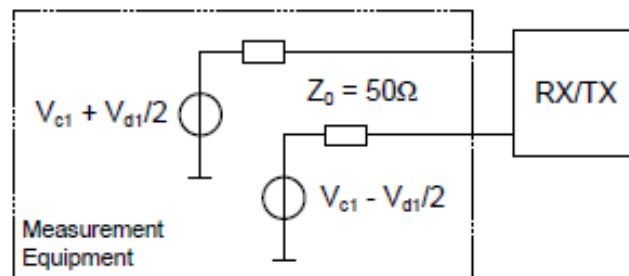


Figure 5.5 Differential transmitter or receiver characterization [8]

The balanced differential transmission line can be modelled by using the 4-port mixed-mode model. A four port VNA is needed to characterize the S-parameter model. [8,15]

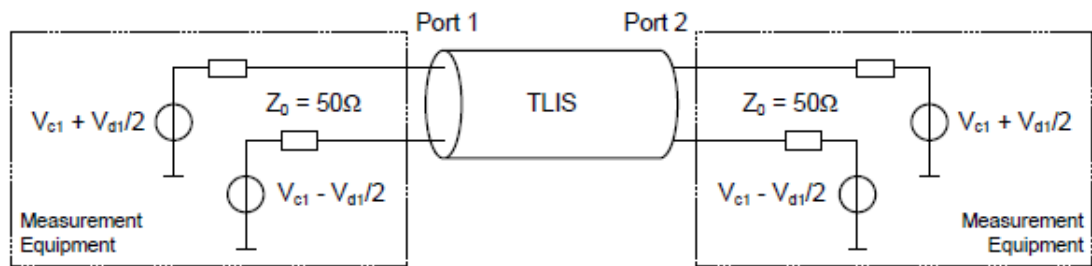


Figure 5.6 Differential balanced transmission line characterization [8]

In cases where the differential pairs are well isolated, it is also valid to use the simplified 2-port model instead of the 4-port mixed-mode model. In isolated fixtures, the line to line cross-talk is minimized and the effect for the S-parameter models is insignificant.

### 5.3.1 Simulations

The common method to model electrical circuits is simulations. The advantage of simulations is that any electrical device system or signal behavior can be modelled in the design phase or in a case where measurements are not possible in the final product. The simulations are done by using computer applications, which typically are a part of hardware design tool package which contains hardware design tools such as schematics and layout tools.

As an input parameter, the simulation application needs an accurate structure, dimensions and materials of the simulated board. Additionally, accurate models of the used components are needed as well. The parameters are very important especially in high-speed signal simulations, because these parameters define the transmission line features such as permeability and permittivity, which further define the nominal impedance and the phase velocity values for the transmission line.

Typical problems in simulations are the inaccuracy of the input parameters as mentioned above, component variation and practical manufacturing process accuracy. These will cause variation for the final product behavior. For that reason, it is more accurate and recommended to measure the real transmission line response when possible.

The simulation models of the used test system were not available and therefore the simulations are handled only theoretically.

### 5.3.2 S-parameter modelling by using time vector network analyzer

The standard way to create S-parameter models is a two port measurement. A calibrated network vector analyzer is able to create very accurate S-parameter models. As a pre-

condition, the transmission line, such as cable or test fixture, is connected to the vector analyzer ports and parameters are measured at both directions through the transmission line.

The problem in the camera test fixture case, is a board to board connector in the camera board end. The vector network analyzer can be connected reliably only to the reference termination board end. As a trial, the additional measurement fixture is soldered to the camera connector pads, but due to the connection structure characteristics, the impedance in this point is disturbed, which dominates the measurement and results. This can be observed when using the Time Domain Reflectometer (TDR) which shows the characteristic impedance as a function of time (Figure 5.7). The root cause is low capacitance, which results in high characteristic impedance. The analysis can be mathematically proofed by using an Equation 8.

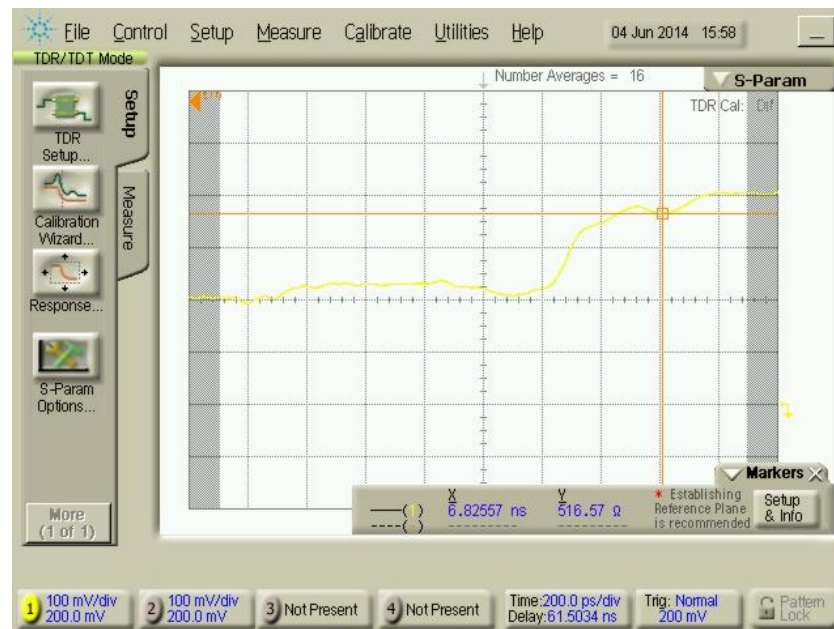


Figure 5.7 TDR measurement with extra measurement fixture

The S-parameters from the same case are presented in Figure 5.8. The high S11 return loss  $< -5$  dB dominates the measurement. The insertion loss S21 parameter is un-useful for the test fixture modelling.

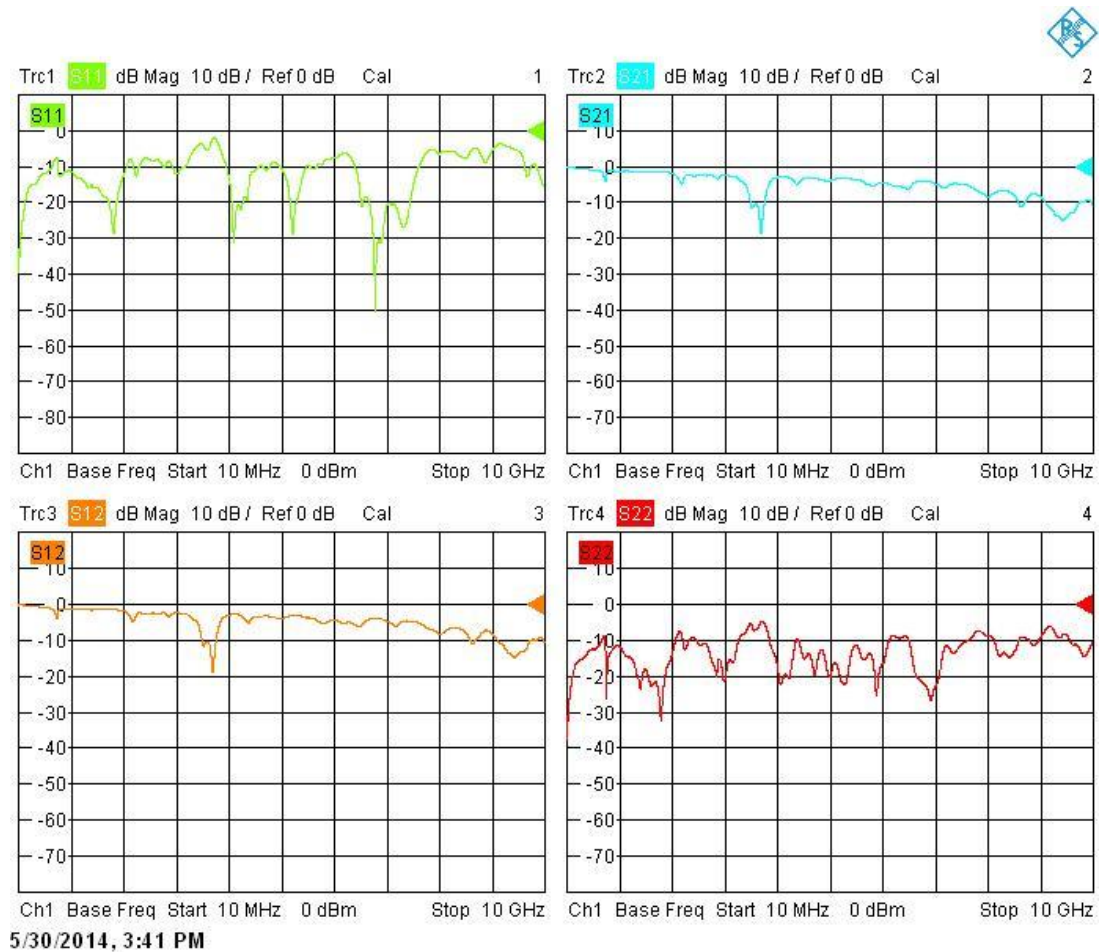


Figure 5.8 Two port s-parameters from the camera Add-On-Board + MIPI-board combination

The second method is to use a time domain gating, which is a vector network analyzer feature. The theory of the time domain gating is based on the mathematical transforms. The idea is to at first convert the frequency domain measurement to the time domain by using the inverse Fourier Transform function. In the time domain mode it is possible to detect discontinuity points, such as the connectors, as a function of transmission line propagation delay or length. This information can be used to set the gates. In the gating mode it is possible to take only the wanted or remove the unwanted part from the transmission line and the gating function works as a band-pass or a low-pass filter. After the gate(s) is set, the result can be converted back from the time domain to the frequency domain by using the Fourier Transform function. Finally, the signal response can be converted to the S-parameters. [27,28]

With modelled test fixtures, the method does not give reliable results. The Vector Network Analyzer is able to create reflection models, but when creating even a simple two port model, such as cables, the gating function is not able to create reliable S21 or S12 parameter models. The achieved results are not used in this project. However, the method is successfully used in similar S-parameter modelling [28].

### 5.3.3 S-parameter modelling by using Auto Fixture Removal application

The latest technology for the S-parameter modelling is the Auto Fixture Removal (AFR) application. The biggest advantage compared to other measurement methods is that the S-parameters can be modelled against open or short end termination. The application is able to create a full two port S-parameter model by using a one port measurement. The method is patented and the functional theory is not publicly available. The AFR application is available for the Keysight VNA product family.

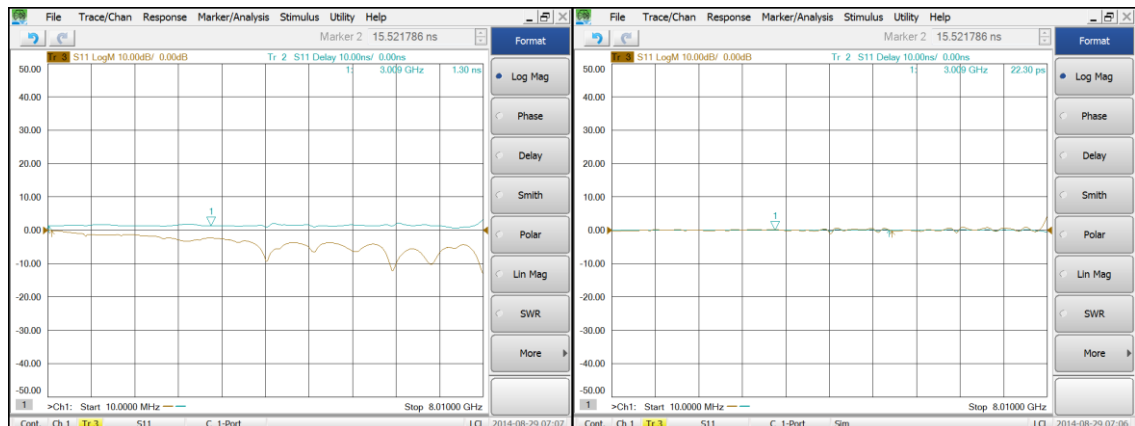


Figure 5.9 Good example, input return loss AFR disabled (5.9a) and AFR enabled (5.9b)

As a result, the compensation works excellently (Figure 5.9). Compared to the ideal compensation, the ripple is inside the 1dB margin, in the boards where the board design itself does not cause resonance drops.

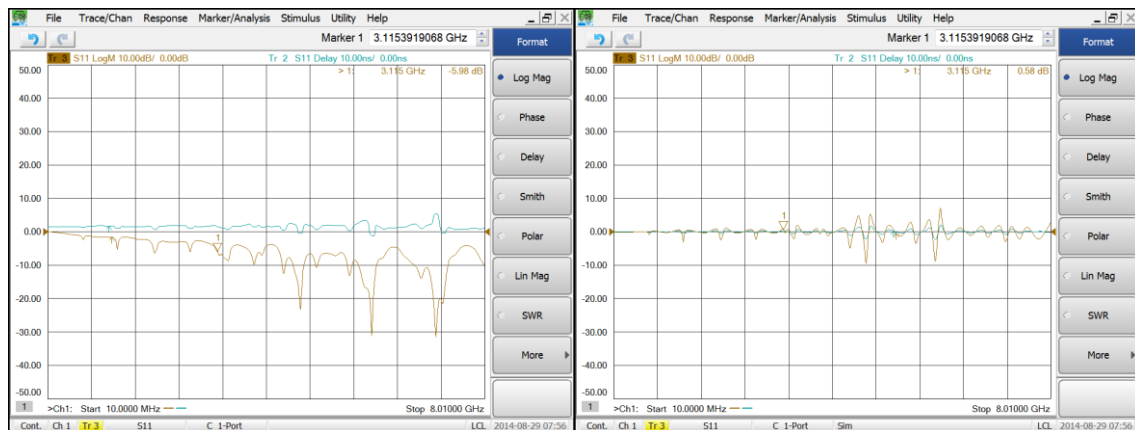


Figure 5.10 Bad example, input return loss AFR disabled (5.10a) and AFR enabled (5.10b)

Other example presented in Figure 5.10 is from a board where there are several resonance points due to the board layout design. The board is identically connected to the test system as in the previous example. The modelling works quite well for that board as well, but the application cannot fully remove all design issues. The margin is now about at 5dB level which causes uncertainty to the models.



## 6 RESULT ANALYSIS

As a final step of this project, the achieved results are analyzed. The primary target was to develop a reliable testing environment for the camera signal integrity verification. The reliable environment means that the test system itself does not cause significant distortion or variation for the results. All of the used test system components need to have a good enough quality in order to reach the system performance targets. Additionally, the usage and benefit of the de-embedding feature for the results is analyzed.

During this project, the importance of the hardware design quality was also noted. Significant differences were found from the camera add on boards. The reasons for the variation are discussed as well.

### 6.1 Gauge R&R analysis

The Gauge RR is a commonly used statistical method for defining variation sources from the results and measurement process. The term R&R comes from repeatability and reproducibility. Repeatability is a minimum variance condition for the measurement accuracy, when all of the external factors are constant and reproducibility is the maximum condition for the variance when all of the environment factors are varying.

Typically in the Gauge R&R analysis, it is recommended to use at least ten parts, measure three times and by three operators. However, the excel sheet [29] used in this analysis uses only five parts, two measurements and two operators. This affects the analysis accuracy but when absolute accuracy is not needed, such as in this case where the target is only to detect main variance sources and to compare measurement, the accuracy of the lighter method analysis is good enough. [29,30]

As an exception, in this analysis the “operator” is replaced with two identical test board setups to understand the variance and deviation caused from the boards. The both board setups are separately modelled and use their own transfer functions when the de-embedding is enabled.

Many external factors affect the measurement accuracy: [29]

- Operator (user)
- Equipment (measurement tools)
- Calibration (accuracy)

- Environment (temperature)
- Time elapsed between measurements (all above)

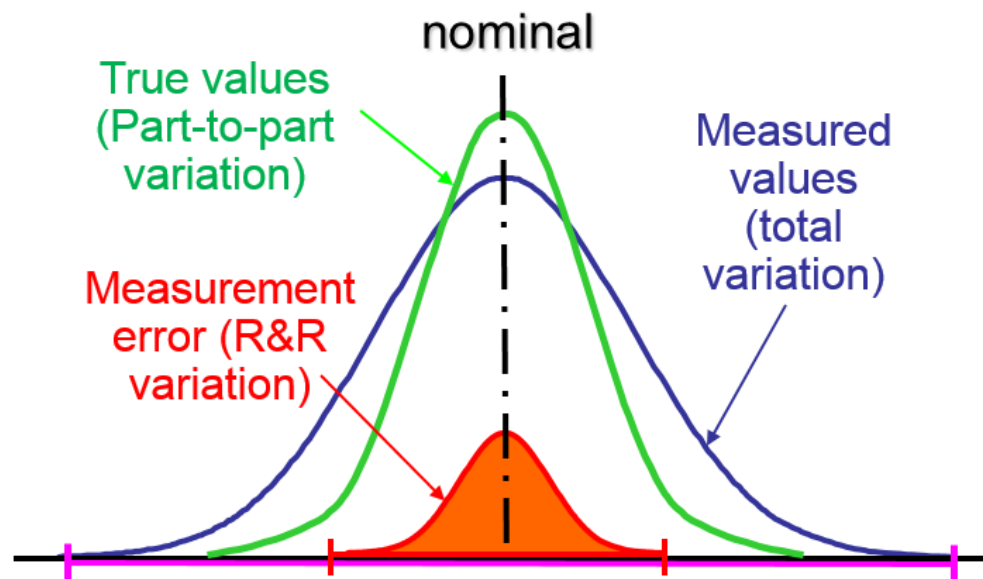


Figure 6.1 Gauge R&R variation definition [28]

Definition for the variation in Figure 6.1 and Tables are [30]:

- Repeatability (Equipment variation)
- Reproducibility (Operator variation)
- Reproducibility (Operator-by-part interaction)
- Part-to-Part variation (true actual variation of the parts)

The first Gauge RR analysis measures voltage behavior. The signal rise time parameter is selected, because it takes into account the gain of all the frequency components over the system bandwidth. The mean value for the results was 209 ps without and 183 ps with the de-embedding.

Table 6.1 Gauge RR analysis for data rise time ( $t_r$ ), Mean value 209ps.

	Part-to-part	Operator	Repeatability	TOTAL	Part*Operator	Reproducibility	TOTAL Gauge
	var	var	var	var	var	var	var
Variance (VarComp)	4,624	5,854	49,575	60,053	0,000	5,854	55,429
%Contribution	7,70 %	9,75 %	82,55 %	100,00 %	0,00 %	9,75 %	92,30 %
Standard Deviation	2,150	2,419	7,041	7,749	0,000	2,419	7,445
%Study Variation	27,75 %	31,22 %	90,86 %	100,00 %	0,00 %	31,22 %	96,07 %

Table 6.2 Gauge RR analysis for data rise time ( $t_r$ ) (de-embedding enabled). Mean Value 183ps.

	Part-to-part	Operator	Repeatability	TOTAL	Part*Operator	Reproducibility	TOTAL Gauge
	var	var	var	var	var	var	var
Variance (VarComp)	6,091	0,000	8,683	20,663	5,889	5,889	14,571
%Contribution	29,48 %	0,00 %	42,02 %	100,00 %	28,50 %	28,50 %	70,52 %
Standard Deviation	2,468	0,000	2,947	4,546	2,427	2,427	3,817
%Study Variation	54,29 %	0,00 %	64,82 %	100,00 %	53,39 %	53,39 %	83,98 %

The values in the used excel table go to zero when the parameter interaction is not significant. [29]

The biggest error source for the variation without the de-embedding enabled is the measurement equipment, the repeatability column in the table. The value dominates the total Gauge R&R variation results. When the de-embedding is enabled the variation is much smaller. The measurement process has been the same in both cases.

One clear difference when investigating the actual result data sheets, is the delta between the first and second measurement trial for the same component which are done in a row. Without the de-embedding the first trial values are higher (average +3.7 ps) than in the second one, but similarly when the de-embedding was enabled, the results were negative (average -2.5 ps) compared to the results without the de-embedding. Even though the number of the samples is small, the direction in results in both cases seems to be clear. The difference between the two samples is very probably explainable by the device temperature behavior. It is more difficult to understand why the direct measurement gives a positive average value and the measurement with the gain correction enabled (de-embedding) gives a negative value. One potential root cause is the frequency and temperature relationship. A component warm-up time is needed before the measurement.

The part-to-part variation is about the same level in both cases, but the board model (operator) value goes to zero in the de-embedding case, which means that the board model compensation has been successful.

The second analysis measures timing behavior. The Data-to-Clock skew parameter was selected to investigate how the de-embedding is able to compensate the lane propagation delay (phase).

**Table 6.3 Gauge RR analysis for Data-to-Clock skew (Tskew(Tx)). Mean value 50,5 UI.**

	Part-to-part	Operator	Repeatability	TOTAL Variation	Part*Operator	Reproducibility	TOTAL Gauge R&R
<b>Variance (VarComp)</b>	26,767	3,708	11,940	42,414	0,000	3,708	15,647
<b>%Contribution</b>	63,11 %	8,74 %	28,15 %	100,00 %	0,00 %	8,74 %	36,89 %
<b>Standard Deviation</b>	5,174	1,926	3,455	6,513	0,000	1,926	3,956
<b>%Study Variation</b>	79,44 %	29,57 %	53,06 %	100,00 %	0,00 %	29,57 %	60,74 %

**Table 6.4 Gauge RR analysis for Data-to-Clock skew (Tskew(Tx)) (de-embedding enabled). Mean value 50,3 UI.**

	Part-to-part	Operator	Repeatability	TOTAL Variation	Part*Operator	Reproducibility	TOTAL Gauge R&R
<b>Variance (VarComp)</b>	24,788	0,000	22,881	47,669	0,000	0,000	22,881
<b>%Contribution</b>	52,00 %	0,00 %	48,00 %	100,00 %	0,00 %	0,00 %	48,00 %
<b>Standard Deviation</b>	4,979	0,000	4,783	6,904	0,000	0,000	4,783
<b>%Study Variation</b>	72,11 %	0,00 %	69,28 %	100,00 %	0,00 %	0,00 %	69,28 %

The biggest advantage of the de-embedding in this environment is the ability to compensate gain and match line lengths by using the signal phase information from the modelled transfer function files. Based on the Gauge RR analysis, the Operator and Reproducibility values are zero, which means that the compensation of the boards has been successful and the test fixture boards do not have any significant effect for the results. The variation comes only from the components and the measurement devices.

However, the total Gauge R&R variance and deviation are slightly higher when the de-embedding is enabled. This is probably caused by resonance frequencies which cannot be fully compensated (Figure 5.9) or the model frequency accuracy is not accurate enough for these resonance points. This can be observed from the small noise increase in the signal when the de-embedding is enabled.

Generally this analysis gives a lot of information on how to optimize the measurement setup and which of the sources have the biggest effect for the result accuracy.

## 6.2 Normal measurements compared to de-embedding results

When the test fixtures and the cable S-parameters are reliably modelled, the transfer functions created can be used to remove the fixture effect from the results. In theory, the test fixture can be fully removed from the result and the test operator can only see a perfect signal output from the DUT terminated by the reference termination board. The final benefit of the de-embedding usage depends on the test fixture quality.

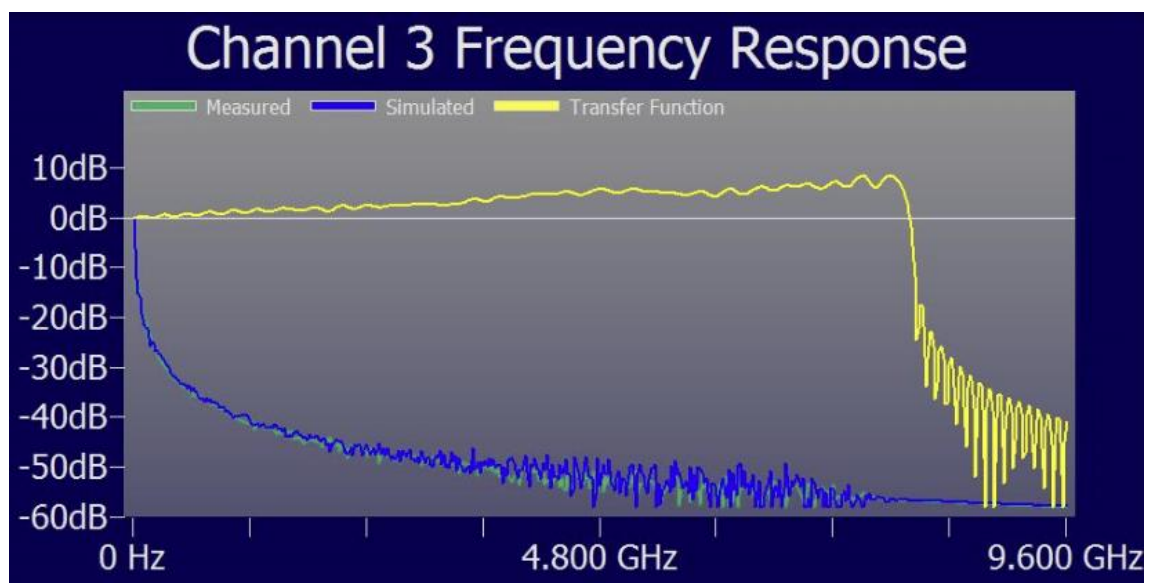


Figure 6.2 Created transfer function frequency response

A compensated test fixture frequency response by using the InfiniiSim application is demonstrated in Figure 6.2. The gain is corrected up to 8 GHz, which is over the used test system bandwidth 7 GHz. Additionally, the application shows the measured and

simulated signal frequency spectrum. The simulated signal in Figure 6.2, is a signal spectrum after the transfer function is applied to the measured signal.

Because the ideal edges are the sum of odd harmonics, the corrected gain affects especially the signal rise and fall time behavior. The achieved voltage compensation effect is significant for the result (Table 6.5).

**Table 6.5 Effect of the voltage gain compensation**

<b>De-embedding</b>	<b>Enabled (ps)</b>	<b>Disabled (ps)</b>
<b>tr</b>	209	183

Often more important factor is the propagation delay (phase) compensation. This is especially true with high frequencies where timing marginal could be only a nanosecond level. The application is able to compensate the delay by using the S-parameter signal phase information in the transfer function. This makes it possible to remove the line to line propagation delay differences, which are typically caused by the layout design or cables, when the interface transmission line lengths are not fully matched.

**Table 6.6 Effect of the phase compensation**

<b>De-embedding</b>	<b>Enabled (UI)</b>	<b>Disabled (UI)</b>
<b>skew</b>	-50.5	-50.3

In this case, the difference is not significant, but on the other hand, the test system lane and cable lengths are already very well matched. For that reason, the analysis does not fully prove how the actual propagation delay compensation works.

### **6.3 Test fixture design**

As a finding of the analysis, it is also noticed resonance behaviors in many camera add-on-boards. Theoretical root causes are the electrical LC-circuit resonance (energy from signal to ground) or the antenna structures (energy from signal to air). For further designs, it is important to take these factors into consideration in the design phase.

Two types of design have been used, the stripline and the microstrip. In the stripline design, the signal trace is surrounded by substrate material and two ground planes. The structure isolates the signal very well from other electromagnetic fields. The same structure is generally used in product design against radio frequency interference. Other option is the microstrip. The difference compared to the stripline is that the signal trace is located on the board surface and the other side is open (air). For that reason, the signal is more sensitive to interference and on the other hand works easily as an interference source.

To clarify the resonance type, the radiated emission measurement is done by using the vector network analyzer. In the measurement, port one is set to measure the return loss S-parameter and sweeps the signal over the selected frequency band. The same frequency band was used in the board modelling. Parallel with the reflection measurement, the wideband antenna is connected to the second vector analyzer port and measures radiated emissions as an insertion loss S-parameter (Figure 6.3).

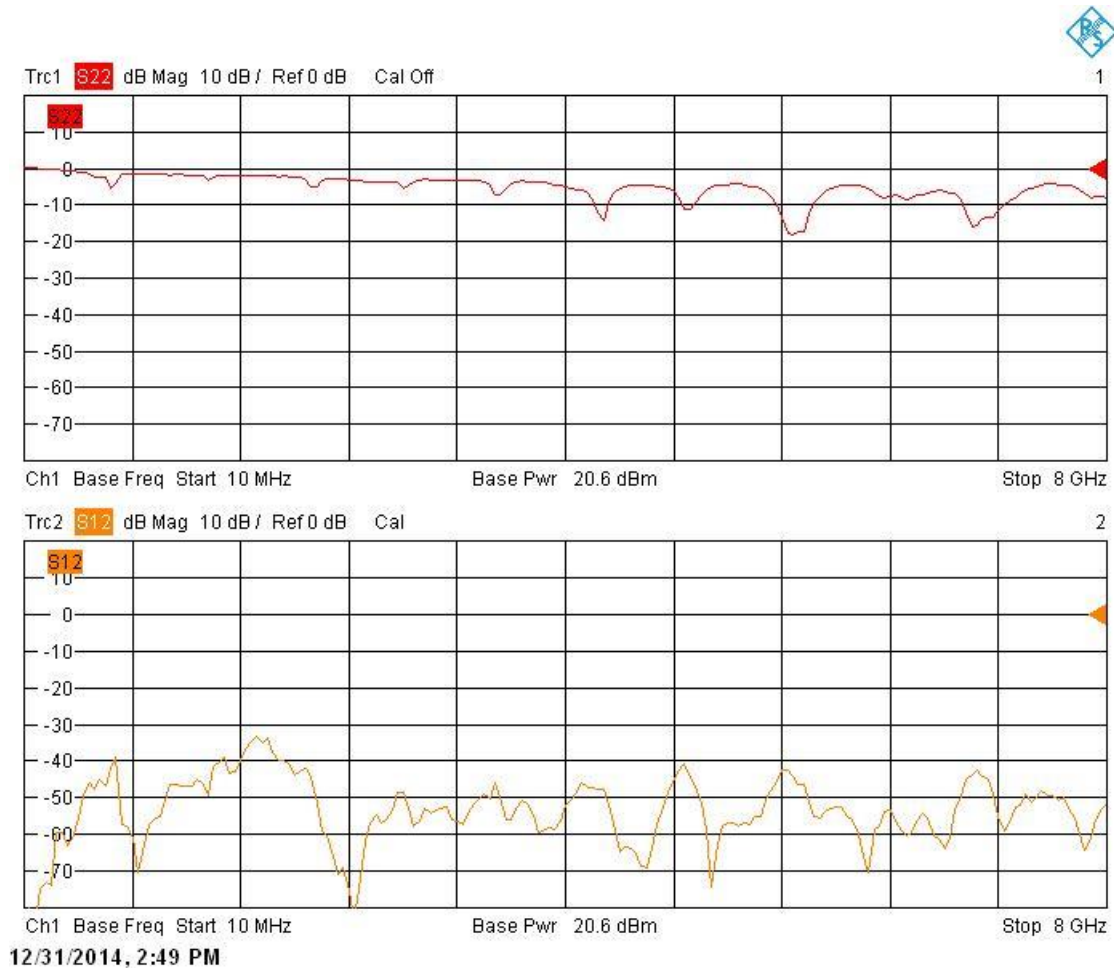


Figure 6.3 Frequency sweep and radiated emissions.

where  $S_{22}$  is the return loss of the AOB board and  $S_{12}$  is the insertion loss over the air from the camera add-on-board to the wideband antenna.

The results of this measurement show that resonances cause radiated emission which matches with the reflection loss results. However, this does not mean that radiated emission is the only loss source. Typically in electrical LC-circuit resonances energy is moving rapidly between two points. This will cause a loss due to resistance and most probably some energy will be radiated out. As a summary, it is hard to prove which of the resonance types is the main loss source, or both. Secondly, accurate radiated emission measurement must be done in standardized laboratory conditions, such as in an EMC-chamber.

## 6.4 Test system results compared to product verification results

Component suppliers have verified their components against very similar environment as presented in this document. The model is closer to an ideal transmission line than the real products, which consist of more unideal factors than simple test fixtures. In the product designs, the transmission line typically contains many interfaces, mismatches in connectors, different electrical structures or materials such as printed wired boards or flexes and different impedances through the transmission line. For that reason, the test fixture results are almost without exception better compared to the product level verification results.

The most typical parameters which are often out of specification are the rise and fall times. Figures 6.4 and 6.5 demonstrate the setup differences in eye diagrams. Both eye measurements are done using the same camera module version and settings. In camera verification setup, the rising and falling edges are much sharper. The product (mobile device) verification is done by using a breakout board. It is a measurement fixture assembled between a printed wire board and a processor chipset. The de-embedding is used to compensate the test fixture effect in that case as well. As a reference, the rise and fall time levels are around 250 ps in a camera verification setup and 390 ps in a product verification setup. The difference is significant and clearly visible in the eye diagrams. Additionally, the reflections affect the signal behavior in the product setup.

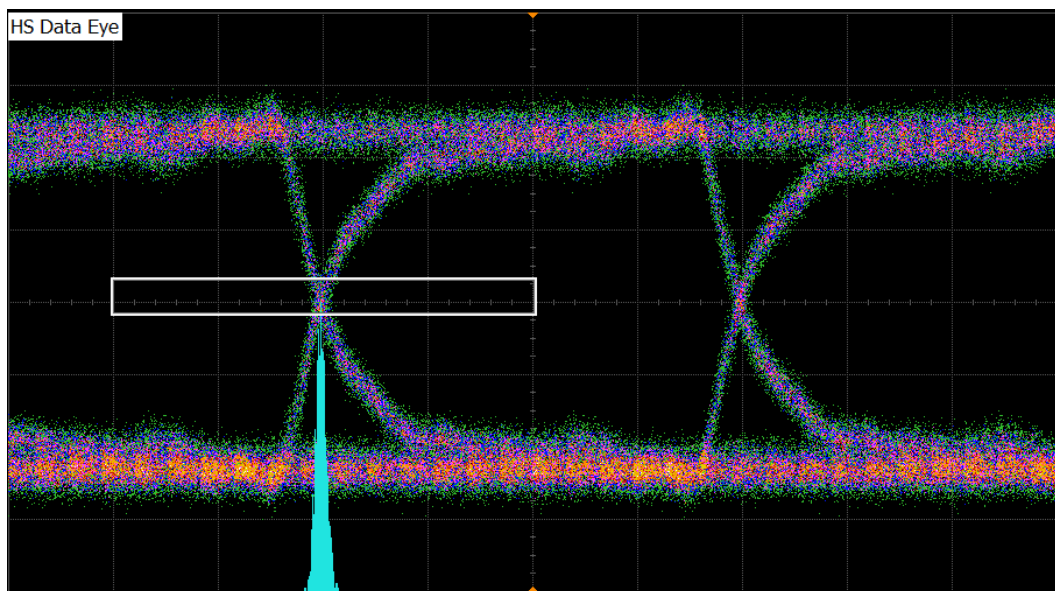


Figure 6.4 EYE diagram in camera verification setup

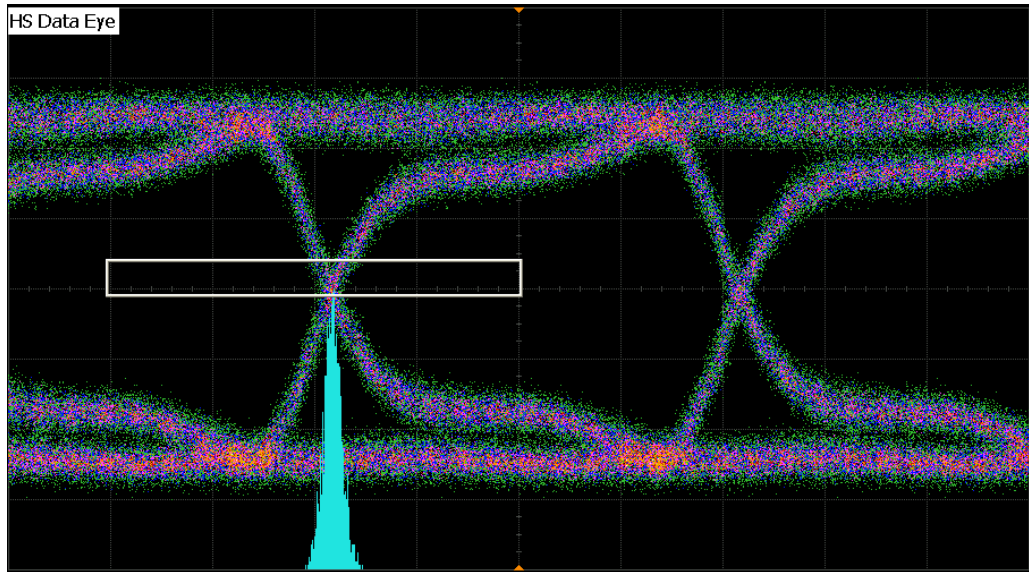


Figure 6.5 EYE diagram in product verification

Generally, most of the timing parameters have a direct relationship to the camera module, however there are some exceptions. The termination delay is always controlled by the receiver. Additionally the skew is dependent from the system design in a case where the trace lengths are not fully matched or compensated, for example by using the de-embedding. These parameters are to be considered as special cases and are not directly comparable.

As a summary, when the modules are tested by using the presented test system, the verification engineer must understand that a camera verification test system often generates better results especially with parameters which are related to the voltage behavior or voltage related timings. Secondly, all timing parameters are not directly comparable due to the receiver preferences.

## 6.5 Alternative test system usage

When the test fixture can be modelled reliably, the fixture can be fully removed from the results and the system can be used for other purposes than the camera signal integrity verification. The test setup can be used to verify camera module simulation model or simulate camera behavior in any black box system.

### IBIS model verification

For simulation purposes, the camera modules are electrically modelled in the Input / Output Buffer Information Specification (IBIS) simulation files. The IBIS model contains full S-parameters from a component's electrical properties. The IBIS models are typically used to simulate the product's signal integrity quality in the design phase. However, the camera component high-speed D-PHY interface is often very complex to



model properly and the product simulations and the measurements do not correspond to each other. This creates uncertainty for the measurement and the simulation's reliability.

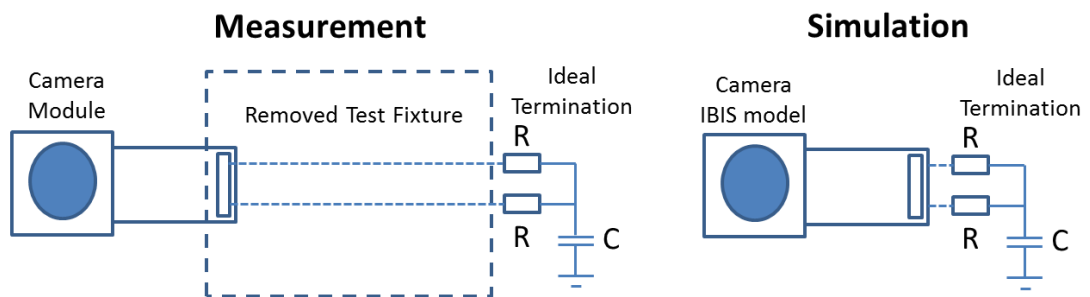


Figure 6.6 IBIS model verification

As a solution, when the test fixture can be reliably compensated and removed from the result, the camera modules can be theoretically measured against ideal termination. The same setup can be easily modelled by using the created IBIS files and the software simulations. Now the measured and simulated results are comparable. This creates an advantage for the future IBIS model accuracy.

### Black box simulations

The system and the InfiniiSim application can be used to simulate camera module signal behavior over any black box system. The S-parameter files are needed from the black box system to create the corresponding transfer function files. When in typical case the test fixture is removed from the results, the InfiniiSim application supports inverse simulation mode to add any black box transfer function model to the results. The black box effect can be now measured in real time and the setup can be understood as a combination of measurement and simulation.

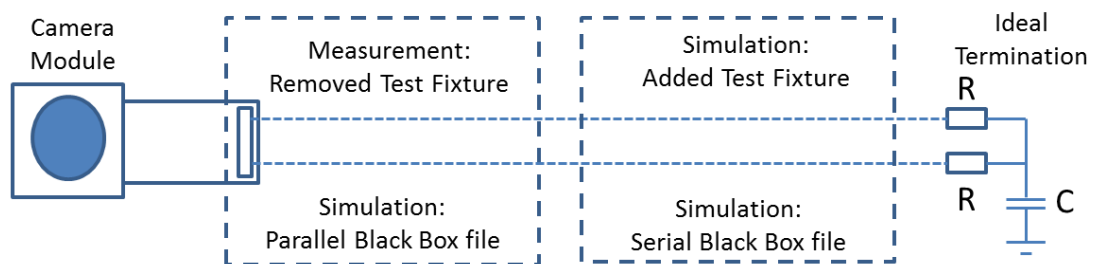


Figure 6.7 InfiniiSim simulation

The setup can be used for special purposes. For example, in order to simulate any sensor behavior in any product or any other transmission line parallel or series with the original test fixture setup.

## 7 CONCLUSION

A reliable verification setup is highly important for camera module research and development purposes. The system bandwidth is currently specified up to 2.5 Gbps per lane and the requirements for the needed measurement accuracy are increasing significantly compared to the current situation. The system can be verified, and in problem cases debugged, only if the verification setup quality is high enough. One of the original targets was to create a reference quality for the interface verification and the environment built during this project fulfills this requirement.

This project proves that the quality of the used test fixtures is high enough for the verification. Especially when comparing the results with real product devices, the difference is significant. The signal form behavior is very clean without any visible reflections and the edges are sharp, which proves that the system bandwidth is wide enough.

The setup modelling was the hardest part in this project. Several methods were used and the Auto-Fixture-Removal gave the most promising results. For the model verification, it is recommended to compare the model and results to other model creation methods. The easiest way to create models is the use of simulations, which were not available during this project due to the design tools used.

The de-embedding examined during the project, seems to be a very useful feature. It gives a big advantage if the reliable system models are available for the transfer function creation. However, it may disturb the results when the models are not reliable. For example in a case where the models show significant resonance points, the de-embedding is not recommended. For these reasons, it is necessary to understand the quality of the created transfer function, when the models are used to compensate the test fixtures.

Other important need of the simulations is the general board layout design. Many of the studied and modelled boards show significant resonance points. These need to be considered in the future designs. Parallel with simulations, it is possible to get S-parameter models from the designed boards. These models can be used for transfer function creation and de-embedding purposes.

The system is currently in use and successfully used for the camera serial interface verification. With the high quality system, the results are reliable and also practical issues

have been found during the verification, which have led to changes in the camera interface hardware design or the setting parameters.

The next step in the test system development will be the fully automated 4-lane CSI-testing. In that case, compensation is mandatory due to long cables and switch (gain loss) and possible differences in cable lengths (phase). The examined de-embedding compensation method is mandatory with that setup.

The same test system principles can be directly utilized in the C-PHY technology verification as well. The system setup will be very similar and the same practices used in this setup can be reused.

Finally, one of the most important things during this project has been personal development in the high-speed signaling, the electrical modelling and generally in the whole camera interface technology area. This personal knowledge is very important for the whole organization, now and in the incoming projects.

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