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FRICTION TRANSFER OF TEFLON TO TEMPLATE THE GROWTH OF ORGANIC SEMICONDUCTORS

Master of Science thesis

Examiner: Professor Jyrki Vuorinen
Examiner and topic approved by the
Faculty Council of the Faculty of
Engineering Sciences
on April 2015

ABSTRACT

TAMPERE UNIVERSITY OF TECHNOLOGY
Master's Degree Programme in Materials Science
MOSALLAEI, MAHMOUD: Friction Transfer of Teflon to Template the Growth of Organic Semiconductors
Master of Science Thesis, 62 pages, 2 Appendix pages
April 2015
Major: Polymeric Materials
Examiner: Professor Jyrki Vuorinen

Keywords: Organic Electronics, Organic Field Effect Transistor, PTFE, Thin Film Transistors, Surface Treatment, Vacuum Thermal Evaporation, DNTT, C_{10}-DNTT

Organic field effect transistors (OFET) based on the latest generation of p-type organic semiconductors (DNTTT, C_{10}-DNTT) display excellent characteristics, with charge transport mobility of up to 10 cm^2/Vs. These materials reach the quality levels of n-type oxide semiconductors (IGZO), potentially enabling the development of a complementary technology (CMOS) for low-cost electronic circuits on large area flexible foils. Examples of potential applications for such circuits are RFID tags, smart packaging, flexible displays and numerous biomedical applications. Among other things, the performance of OFET depends on the degree of crystallinity of the organic semiconductors. Higher ordering delivers better performance, and, the best OFETs are based on defect free single organic crystals. The production of thin films of defect free organic single crystals over large area is therefore highly desirable. This, however, remains a considerable challenge since the presence of only a few defects will negatively impact the spread of TFT characteristics. As the spread increases, the yield of circuits dramatically decreases.

Templating that relies on a good match between the crystal structures of the substrate and the grown material is very well known in the field of epitaxial growth of inorganic materials. In the field of organic electronics, however, much remains to be done. Therefore we aim to develop a method to transfer a thin, uniform and aligned film of Polytetrafluoroethylene (PTFE) on the substrate as a template to grow organic semiconductors and increasing their degree of order following by making OFET. The influence of the PTFE layer on the performance of OFET is studied.

Tampere, April 2015

Mahmoud Mosallaei

ACKNOWLEDGEMENTS

This thesis was carried out at the Department of Large Area Electronics at IMEC nano/micro Research Company during the years 2014-2015.

First of all I would like to thank Dr. Cedric Rolin for being a perfect advisor. During this period I have learned a lot about the principles of organic electronics, materials science, physics and transistors. I really admire him not only for his great level of knowledge and professional skills, but also for being a kind and caring person. I believe he has all criteria for a person who is supposed to be a perfect advisor.

I would like to thank Professor Paul Heremanns and Jan Genoe head of LAE and MNP group respectively, for making this thesis job possible and for well organizing the work atmosphere.

I was lucky to meet Dr. Afshin Hadipour during my work here. He was ready to give me an enormous amount of information about organic electronics and practical stuffs.

I want to thank Professor Jyrki Vuorinen, my university supervisor in Finland for his academic support.

I would like to appreciate my family for their continuous support and encouragement.

A special thanks to my girlfriend, Paula for her patience, sacrifice and love.

Finally I thank all MNP group members: Professor Andriy Kadashchuk, Masashi Nitani, Jeong-Hwan Lee, Pavlo Fesenko and Robby Janneck for their kind help and advice during my work in IMEC.

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LIST OF SYMBOLS AND ABBREVIATIONS

AFM	Atomic Force Microscope
C_{10}-DNTT	2,9-didecyldinaphtalo[2,3-b:2',3'-f]thieno[3,2-b]thiophene
CBE	chemical beam epitaxy
CMOS	Complementary Metal Oxide Semiconductor
DIW	Distilled Water
DNTT	dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]-thiophene
FET	Field Effect Transistor
HBC	Hexa-peri-hexabenzocoronene
HDPE	High Density Polyethylene
HVPE	hybrid vapor phase epitaxy
IPA	Isopropyl alcohol
JFET	junction field effect transistors
LDPE	Low Density Polyethylene
LPE	liquid phase epitaxy
MBE	Molecular Beam Epitaxy
MOCVD	Metal Organic Chemical Vapor Deposition
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
ODTS	Octadecyl-trichloro-silane
OFET	Organic Field Effect Transistor
OLED	Organic Light Emitting Diode
OTFT	Organic Thin Film Transistor
P3HT	Poly(3-hexylthiophene-2,5-diyl)
POM	Polarized Optical Microscope
PTFE	Polytetrafluoroethylene
QCM	Quartz crystal microbalance
Rpm	rounds per minute
SAM	Self-Assembled-Monolayer
UHVCVD	Ultra High Vacuum Chemical Vapor Deposition

b	half-contact width
C_{diel}	Gate capacitance (specific)
D_{fin}	Final thickness
E	Elastic modulus
F	Force
G	Gate
I_D	Drain current
I_G	Gate current
I_S	Source current
L	Channel length
P	Pressure
P_{max}	Maximum contact pressure
R	Radius
RR	Ramp Rate

S	Soaking time
T	Temperature
TF	Tooling Factor
V_{DS}	Drain Voltage
V_{GS}	Gate voltage
V_{th}	Threshold voltage
W	Channel width
μ	Mobility (effective)
ν	Poisson's ratio

1. INTRODUCTION

The last 20 years have seen strong research efforts to develop the potential of organic semiconductors. Despite their lower transport performances, organic semiconductors present a number of benefits in comparison with conventional inorganic semiconductors. They can be processed at low temperature on flexible substrates, making them good candidates for high-volume production of low cost electronic devices over large flexible substrates. Also they present strong interaction with light, opening up a number of opto-electronic applications ranging from light absorption in solar cells to light emission in Organic Light Emitting Diodes (OLEDs). As of today, this last application is the only one that has managed to find applications into commercially available products. This is due to the numerous advantages inherent to the OLED technology. Other technologies, such as organic solar cells and circuits based on Organic Field Effect Transistors (OFETs), still require further technological development in order to be able to compete with concurrent inorganic technologies.
In the field of OFETs, much research is currently conducted at material as well as device level in order to improve the performance of OFETs such as field effect mobility and environmental stability.
Thin film transistors based on latest generation of p-type organic semiconductors (DNTT, C_{10}-DNTT) display excellent characteristics and are used in this study. As higher ordering of semiconductor delivers better performance; therefore the aim of this thesis is to friction transfer of Teflon as a template to grow of highly ordered organic semiconductors.

1.1 Thesis outline

This thesis consists of 5 chapters. In chapter 2 the theoretical background of the study including organic semiconductor overview, OFET concept, device fabrication techniques and the idea of friction transfer of Polytetrafluoroethylene are discussed. Chapter 3 explains the experimental part of the work. In the first section, all required materials used in this thesis as well as producer companies are explained. In the next chapter all stages of sample preparation and surface treatment are explained. Methods of friction transferring of the PTFE, deposition method of organic semiconductors and gold contacts are discussed in detail. At the end of this chapter, characterization methods for analysis of the utilized materials and device performance are mentioned. Chapter 5 gives a brief summary of the whole work carried out in this thesis.

2. THEORETICAL BACKGROUND

Organic materials refer to a vast range of materials used in a wide array of applications. Although carbon and hydrogen are the two main constituents of all organic molecules, other atoms such as oxygen, nitrogen sulfur, fluorine, chlorine and bromine can take part in the structure of these molecules. The variability in molecular shape, size and constituents constitutes a great playground for creative chemists: Organic molecules can be tailored to suit a wanted application. Also, Organic solids display different degrees of microstructural order ranging from single crystalline, polycrystalline to amorphous formats. The weak electrostatic intermolecular binding forces render most organic solids soft and flexible. [1]

2.1 Organic semiconductors

Organic semiconductors are a subclass of organic materials that are characterized by a conjugated core enabling the delocalization of electrons populating the Pi orbitals of the sp2 hybridization.[2][3] The core is often made of repeating functional groups that are linked in the structure of organic semiconductors and have a rich delocalized □-electron cloud. [3] Some of the most common basic functional groups of organic materials are illustrated in Figure.1. [3]

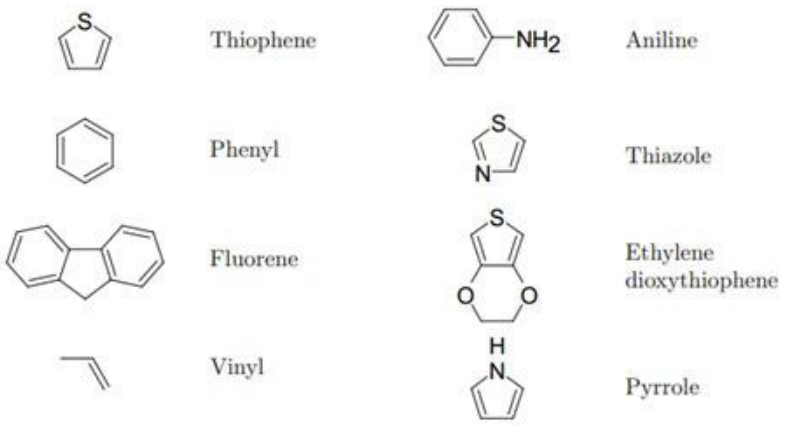

Figure 1.Some of the common repeating functional units in the structure of conjugated organic semiconductors [3]

This delocalization over the molecular core is accompanied by the opening of a band gap of forbidden electron energy, yielding semiconducting properties to the molecule. Organic materials present unique electronic and optical properties. And the ability to tailor the molecule to a specific need renders this class of materials attractive in the development of a number of opto-electronic applications. In addition, low temperature thin film manufacturing techniques such as melt, solution, or vapor processing methods and process-ability on flexible substrate make them good candidates in large area electronics on low cost flexible substrates such as plastic foils.[4][5]

Organic semiconductors are divided into two main groups: Conjugated polymers and conjugated small molecules. [2][3] Each group has its own properties. For example small molecule semiconductors can be grown with thermal evaporation techniques and can present a microstructure ranging from complete amorphous to fully crystalline, that is a broader range than polymer semiconductors. On the other hand, owing to their higher solubility, polymer semiconductors are easily processed in solution, which can be a more convenient method for large-volume production.[6] The limited intermolecular forces in organic solids enable great processability of organic semiconductors: thin organic films can be processed at low temperatures, close to room temperature. Also, the final film properties show a relative independence from the nature of the substrate. In consequence, organic semiconductors appear to be ideal candidates for the development of low cost electronic application on large-area flexible substrates.[4][5]

Charge transport in organic semiconductors requires a percolation of the charges through the molecular solid. As most practical systems are disordered, this percolation is usually described as a hopping system, where charges move by successively jumps from molecule to molecule. The ease of these jumps is governed by the extension of orbital overlapping between the molecules. [3][5] In organic semiconductors, electric charges transfer easier along the □□□ stacking direction. A microstructure that maximizes this overlap is favorable to transport. Disorder (structural and chemical) affects negatively the charge transport as it creates a spread of energy states that may trap or scatter the moving charge carriers. More ordered and pure systems present superior transport properties and single crystalline organic semiconductors such as rubrene single crystals may even present fully delocalized band transport. A measure for the ease of charge transport is the charge carrier mobility. More oriented organic film present higher charge mobilities.[5]

2.1.1 DNTT

In 2007 a novel semiconducting organic molecular core was developed by Takymiya and et.al. : dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]-thiophene (DNTT) whose chemical and crystal structure are shown in Figure 2.[9]

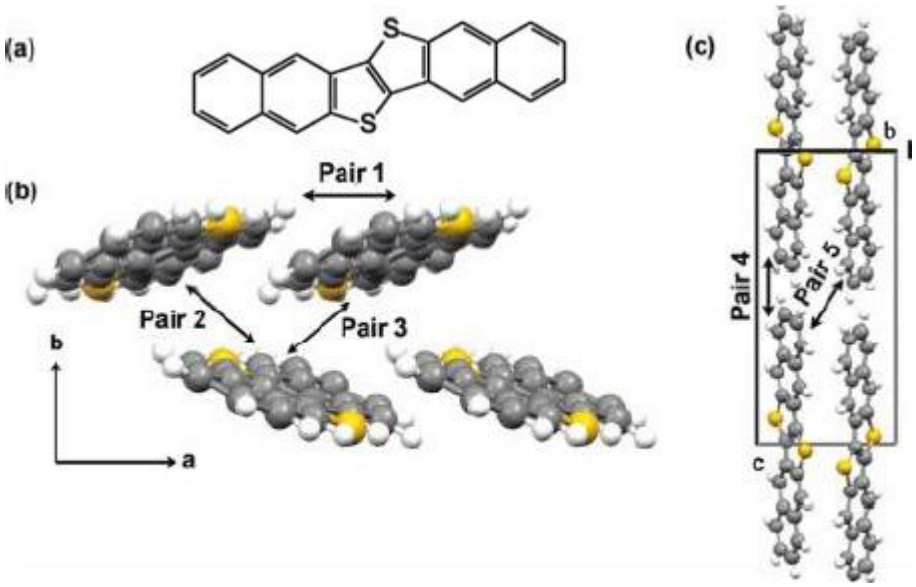

Figure 2.The molecular structure of DNTT, (b) (c) Crystal structure of DNTT in ab plane and bc plane respectively (a: 6.187Å, b: 7.662Å, c: 16.21 Å) [8]

DNTT has a π-extended heteroaromatic molecular structure with 6 fused rings which consist of 2 naphthalene and 2 tiophene groups. [9][1] Crystal structure of DNTT is triclinic and displays a herringbone arrangement in the ab-plane (a:6.184Å, b:7.22Å) and the layer spacing in the c-direction is equal to 16.21Å. [1] This microstructure is quite comparable to that of pentacene and is very common for rod-like conjugated molecules.

DNTT demonstrates a charge carrier mobility that is superior to pentacene. Indeed pentacene is one of the most common organic semiconductors from the acenes series used in organic electronics. Pentacene is a linear oligoacene molecule which consists of 5 fused benzene rings. [2] In addition DNTT has a better air stability than pentacene thanks to its higher ionization potential. [10] Indeed DNTT is characterized by a larger HOMO-LUMO forbidden bandgap of -2.4eV. It is therefore a promising candidate for organic field effect transistor applications. [11] In organic thin film transistors based on DNTT as the semiconductor layer, the mobilities of 3.1 cm^2/Vs and 8.3 cm^2/Vs for polycrystalline and single crystal thin film have been measured, respectively. [12]

2.1.2 C_{10}-DNTT

One issue of DNTT is its lack of solubility, rendering solution processing impossible. A way to circumvent this is the addition of functional groups to the molecular core. These retain the opto-electronic properties of the DNTT core while enhancing the solubility. The recent modified derivative of DNTT which has a long alkyl chain is 2,9-di-decyl-dinaphtho-[2,3-b:20 ,30 ;-f]-thieno-[3,2-b]-thiophene (C_{10}-DNTT). [13][14] C_{10}-DNTT is a highly $\pi-$conjugated small molecule organic semiconductor. Besides solubility, the long alkyl side groups in C_{10}-DNTT have improved the morphology and crystal structure of this organic semiconductor, resulting in a higher proximity of the molecular cores and improved orbital overlap: In comparison to the non-alkylated DNTT, the decyl substituents in C_{10}-DNTT push the molecules within the semiconductor layer into a tighter solid state packing, which improves the overlapping of orbitals; thus increasing the carrier mobility in the plane parallel to the substrate surface is expected.[14][15] It shows higher charge carrier mobility [13]. OTFTs based on polycrystalline C_{10}-DNTT show mobilities up to 10 cm^2/Vs [16]. Figure 3. illustrates the molecular structure of C_{10}-DNTT. [14]

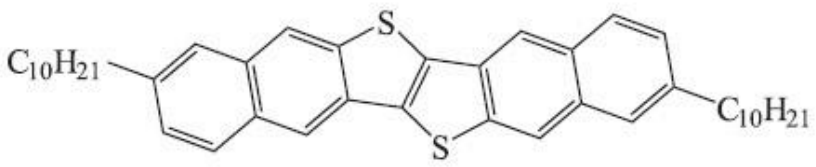

Figure 3.The molecular structure of the C10-DNTT [14]

The length of C_{10}-DNTT molecule is 39.3A° and the interlayer distances (d-spacing) is 38A° measured by X-ray diffraction. [13] [17] C_{10}-DNTT has a HOMO-LUMO gap about 3eV, enabling small off-state drain current and thereby a large on/off ratios. [15]

2.2 Organic Field Effect Transistors

The concept of field effect transistor (FET) was first proposed by Julius Edgar Lilienfeld in 1926 and Oskar Heil in 1934. The first practical semiconducting devices, junction field effect transistors (JFETs), were developed after the transistor effect was introduced by William Shockley in 1947, right after the 20 years patent period expired. In 1960 the metal oxide semiconductor field effect transistor (MOSFET), which is a paramount device in the development of the electronic industry, was introduced by Dawon Kahng and Martin Atalla.[18]

The conventional Si MOSFET benefits from the high quality interface formed between single crystalline Si and its native oxide SiO_2. Single crystalline silicon MOSFETs can

only be fabricated directly on the silicon wafer as a substrate. The whole fabrication requires doping treatment, contact metallization and photolithographic patterning. Several steps require high temperatures. Generally the processing for silicon based transistors requires temperature above 800°C and 200°C respectively for single crystalline and hydrogenated amorphous silicon transistors. Also, MOSFETs use the Si Wafer as a substrate, thereby putting severe constraints on the maximum size, the mechanical properties and the cost of high performance electronics.

Motivated by the display industry that requires large area back panel circuits to drive large area LCD displays, thin film transistors (TFTs) were developed that can be processed on large area glass substrates. In TFTs, the semiconducting layer is based on amorphous Si, polycrystalline Si, or, more recently, amorphous metal oxides such as Indium-Gallium-Zinc-Oxide. The processing of these semiconductors, however, often also require an annealing step above 300°C, banning most types of flexible substrates.

In 1980 OFETs were proposed that are using a thin film of organic semiconductor for the modulated charge transport from source to drain. OFETs (also called Organic Thin Film Transistors - OTFT), have an architecture similar to the MOSFET, but the channel in OFETs is operated in accumulation rather than in depletion of charge carrier[2]. A strong point of OFETs is the ability to design low temperature process flow and the variety in the choice of suitable dielectric materials. In consequence, OFET can be fabricated on low-cost, flexible substrates such as plastics [2].

OFET performance is characterized by different parameters. The most important are: field effect mobility, on/off current ratio and threshold voltage. These parameters show a strong dependence on the quality and the order of the organic semiconductor layer [5].

2.2.1 Structure of OFETs

For manufacturing of OFETs, thin layers of organic semiconductor, gate electrode, gate dielectric, source and drain electrodes are deposited onto the insulating substrate [2]. Based on the order of the deposited materials, different OFET topologies can be defined. Figure 4. shows four possible OFET architectures. [2]

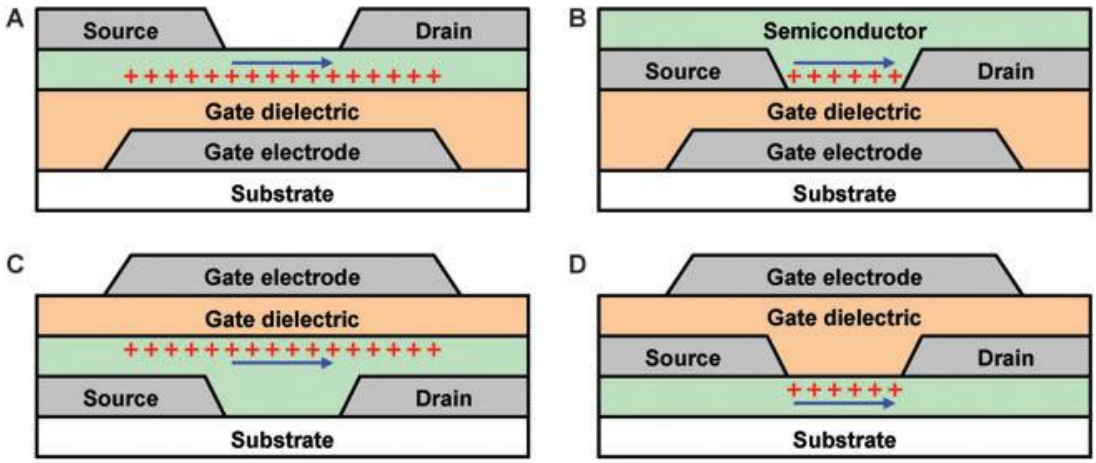

Figure 4.Schematic cross-sections of the four principle thin-film transistor (TFT) structures. The carrier channel is schematically shown in red. (a) Bottom-gate (inverted) staggered TFT. (b) Bottom-gate (inverted) coplanar TFT. (c) Top-gate staggered TFT. (d) Top-gate coplanar TFT [2]

Each structure has its own benefits and disadvantages [2]. For instance, bottom gate-top contact is the structure that is mostly utilized for material screening, research and development. For this architecture that we used in the present work, the gate dielectric (such as SiO_2) is thermally grown on top of a heavily doped silicon substrate. This supplies a gate and a dielectric that are common to all transistors on the sample. The organic semiconductor is then deposited on the top of the dielectric surface and finally source and drain contacts are deposited patterned on the organic semiconductor via metal evaporation through a shadow mask. [19]

2.2.2 OTFT operation

By convention, the source electrode (denoted S) is always grounded, and the voltages on the gate (G) and drain (D) electrodes are referenced to the grounded source. When a voltage is applied to the gate electrode (V_{GS}), a thin sheet of charge carriers is induced at the interface between the semiconductor and the dielectric layers [2][19]. This creates a thin channel with high density of mobile charge carriers. The charge density can be finely regulated by modulating V_{GS}. Another source is used to apply a voltage between source and drain contacts (V_{DS}). The accumulated charge then starts to drift, from the source that injects it into the channel to the drain that collects them from the channel. The current (I_{DS}) flows in the organic semiconductor layer as the charge carrier transfer through the organic semiconductor channel [19][2].

2.2.3 Thin film transistor equations

Contrary to c-SI FETs that operate in inversion mode, OFETs operate in accumulation mode [2][3]: charge carriers are accumulated in the channel when a gate voltage is applied. For p-type transistors, positive charges are accumulated upon application of a negative V_{GS}. [2].
Due the similarity between MOSFETs and OFETs, the gradual channel approximation model developed for FETs based on single crystal Si can be directly transferred to the case of OFETs. It delivers the equation (1) for the linear regime where $V_{DS} < V_{GS} - V_{th}$:[2]

$$I_D = \frac{\mu C_{diel} W}{L}\left((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right) \qquad (1)$$

Where W and L are width and length of the channel, C_{diel} is the gate capacitance and μ is the charge carrier mobility of the semiconductor. In the saturation regime, when $V_{DS} > V_{GS} - V_{th}$ one can assume $V_{DS} = V_{GS} - V_{TH}$. Therefore current is measured from the equation(2) [2]:

$$I_D = \frac{\mu C_{diel} W}{2L}(V_{GS} - V_{th})^2 \qquad (2)$$

Respectively charge carrier mobility for both linear and saturation modes are described with equations (3) and (4) [2]:

$$\text{Linear Mode} \qquad \mu_{lin} = \frac{L}{C_{diel} W V_{DS}} \frac{\partial I_D}{\partial V_{GS}} \qquad (3)$$

$$\text{Saturation Mode} \quad \mu_{sat} = \frac{2L}{C_{diel} W}\left(\frac{\partial \sqrt{I_D}}{\partial V_{GS}}\right)^2 \qquad (4)$$

Figure 5. is a typical example of a transfer curve in saturation regime for a device with the width and length of 2000 and 200μm respectively. The dependency of the gate source voltage and the drain current is illustrated.

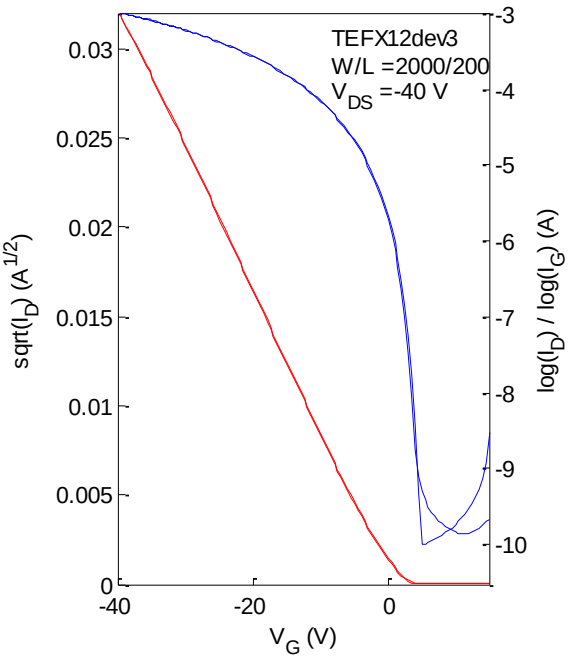

Figure 5.The transfer curve for a device with the width/ length of 2000/200µm

2.3 Device fabrication techniques

Organic materials can be processed from the melt, from solution or from vapor with a limited temperature budget, typically T < 300°C. The max temperature is limited both by the molecular degradation yielding impure films as well as by the structural degradation of the organic film due to the weak van der Waals intermolecular bonds [3]. These weak bonds also confer soft mechanical properties to the organic solids, making them flexible but easily damaged [3].

Substrates used for the growth of organic small molecule thin film devices are usually inert and/or display a number of defects. On this type of substrate, many nucleation sites are present, leading to the formation of polycrystalline films (in the case of a crystalline material) characterized by a high density of grain boundaries. Such structural defects make up for large concentration of trap and scattering centers in charge carrier transport. They, therefore have a negative effect on the charge transport. It is desirable to enhance the ordering of the molecules within the molecular crystal near the interface as well as the crystalline domain size. This results in a better charge transport characterized by higher charge carrier mobility [20]. In this work we explore a fabrication scheme aimed at the enhancement of molecular order. These techniques that involve substrate preparation and organic growth are presented along with other important techniques in this section.

As melt processing is only limited to very small organic molecules due to thermal degradation issues, we only consider the vapor and solution processing. The choice be-

tween these two routes depends on the vapor pressure and solubility of the organic semiconductors. [21]. Next we discuss the substrate preparation, before processing the organic layer. This has a very strong influence on the final film properties. The mechanical transfer of PTFE is a pretreatment studied in this work. Prior art is therefore described in more details in the last section.

2.3.1 Vacuum deposition

Vacuum thermal evaporation (VTE) is a deposition technique suited for most small molecule organic semiconductors displaying sufficient vapor pressure without thermal degradation [3]. This method can be used to deposit a very wide variety of small organic semiconductor molecules such as the acenes (tetracene and pentacene) [21].

The source organic powder is placed in a crucible or a boat inside a high vacuum chamber kept at a pressure of 10^{-8} to 10^{-6} Torr [3][21]. Using the high vacuum brings some benefits for the organic materials. First, evacuation of the vacuum chamber brings the organic compounds closer to Solid-Gas phase isotherm, thereby reducing the temperature of the sublimation point. This helps prevent thermal degradation of some of these compounds. Second, by essence, a vacuum chamber is a clean environment and delivers layers with a high degree of purity. [3]

The evaporation of organic semiconductors is triggered by resistive heating of the crucible or boat containing the organic powder. At sufficient temperature, the vapor pressure rises beyond the background pressure of the material in the vacuum chamber and evaporation starts. Placing a cold substrate in front of the source lets the organic molecules condense and form a thin film on the substrate. The deposition rate and the thickness of the layer can be precisely controlled with the help of a quartz crystal microbalance.

This technique reproducibly yields highly pure films with good structural (thickness, microstructure) control. In addition, it is possible to deposit more than one organic semiconductor without the risk of delamination of the previously deposited films [21]. Co-evaporation of several organic compounds is also possible. This gives access to the growth of complex multilayered and doped structures that are important for example in the fabrication of OLEDs. Drawbacks for this method are the high initial cost for the equipment and the complex scale-up to large-area substrates. [21].

The growth of high quality organic semiconductor layers by VTE requires a careful optimization of deposition parameters [21]. The molecular structure and morphology of the organic thin films are directly linked to the substrate temperature and the rate of

deposition. Based on the phase diagram, by keeping the temperature in the constant value, increasing of deposition rate will improve the nucleation growth. Figure 6. illustrates the relation between substrate temperature, deposition rate and growth region[41] .

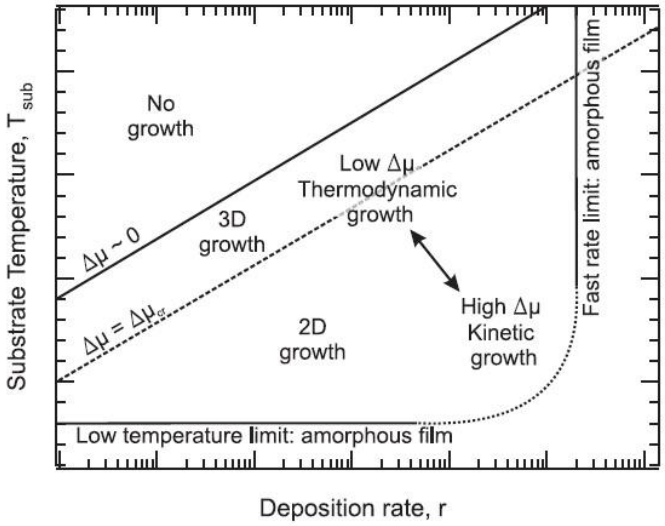

Figure 6.Qualitative illustration of organic thin film growth regions as a function of deposition rate r and substrate temperature Tsub [41]

As detailed later, the substrate surface and its pretreatment also affect the quality of the organic thin films. After deposition, based on the type and structure of organic semiconductors, annealing may improve the characteristics of final device[21].

2.3.2 Solution processing

In comparison to evaporation techniques, solution processing of organic semiconductors provides more direct routes towards the manufacturing of large area thin film with less production cost [21]. These methods however require the solubility of organic semiconductor in appropriate solvents [3]. Note that insoluble organic semiconductors can be engineered to become soluble through the addition of side functional groups [3][21].
There are different techniques for solution deposition such as spin coating, drop-casting, blade coating, slot die coating, gravure printing, and ink-jet printing. Figure 7. schematically show the common methods of solution based deposition techniques [22].

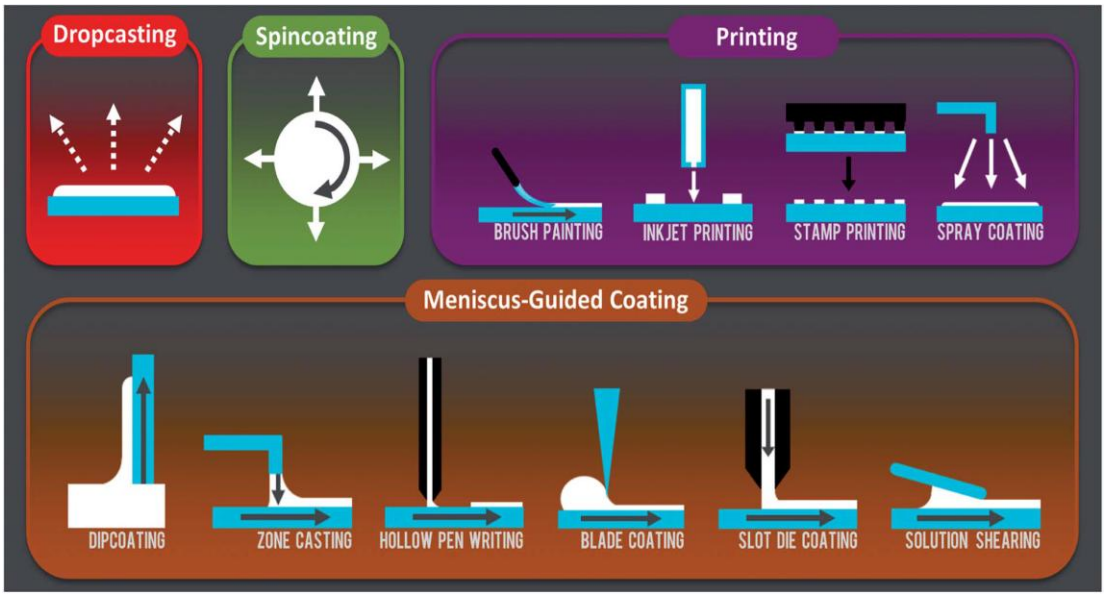

Figure 7.Schematic summary of commonly used solution based techniques [22]

Different parameters play a role in the formation of the organic semiconductor thin film and require optimization. These are for example solvent nature, semiconductor concentration, ink rheological properties (viscosity, etc.), the rate of solvent evaporation and the quality of the substrate surface [21].

2.3.3 Epitaxial growth

Epitaxy is a technique for growing of thin inorganic crystalline film that is commonly used in semiconductor industry [23] It is typically applied in vapor phase techniques such as Molecular Beam Epitaxy (MBE) and Metal Organic Chemical Vapor Deposition (MOCVD). But epitaxy can be achieved with various techniques such as liquid phase epitaxy (LPE), hybrid vapor phase epitaxy (HVPE), chemical beam epitaxy (CBE), molecular beam epitaxy (MBE) and ultra high vacuum chemical vapor deposition (UHVCVD). [24]This method is considered as a non-equilibrium operation in which the growing material is aligned with a pattern identical to the underlying substrate [25]. The nature and the degree of order of the substrate must be controlled so that it perfectly templates the growth of the subsequent layer, delivering single crystalline films with a crystal lattice that is commensurate to that of the substrate. [26][24]. If the thin film and the substrate are made of the same material, epitaxy is known as homoepitaxy. Otherwise it is called heteroepitaxy.

As it delivers single crystalline films, epitaxial growth is desirable to achieve the highest charge transport performance. In organic thin film growth, however, it has been shown that it is quite challenging to achieve epitaxy. It has been demonstrated for a variety of small molecules growth by VTE on a several single crystalline inorganic sub-

strates such as freshly cleaved mica, KCl or KBr. Also, there exist several reports of organic on organic epitaxial growth. Now, molecular crystals are characterized by low symmetry and large unit cell dimensions. Although the crystals show a higher degree of flexibility, finding crystal structures that match between two different materials is rather the exception than the rule.

2.4 Surface pretreatment

As mentioned above, the performance of OFET strongly depends on the structure of the organic semiconductor. In all processing cases, the nature of the substrate has a major impact on the quality of the organic layer above. The interactions between the organic compound and the substrate are primordial in defining how the organic molecules will assemble to form an organic solid. In general a low degree of interaction (inert substrate) is usually favorable to growth of ordered polycrystalline layers for OFET applications. However, as discussed later, the use of epitaxial relationship between an ordered substrate and an ordered semiconducting layer can yield layers with higher ordering degree.[5]

Below, we detail a few techniques used in this work to prepare our substrates. Starting from the simplest treatments up to the most complex.

2.4.1 UV-Ozone treatment

UV-ozone cleaning is a method of obtaining clean surface with little organic contamination. It is applicable to a variety of substrates such as glass slides and silicon substrates. The UV-ozone cleaning is considered as a photo sensitized oxidation operation that effectively removes all organic contaminations still present on the substrate after a regular solvent cleaning. Since this treatment is not a useful method for removing inorganic contaminations, pre-cleaning is necessary in order to have an effective UV-Ozone treatment [27][28].
In this technique, the exposure of ambient oxygen molecules to intense ultraviolet light delivers an oxidative atmosphere that decomposes organic contamination still present on the substrate into volatile molecules such as H_2O and CO_2. UV rays have the wavelength of 184.9nm and 253.7nm. First the 184.9nm UV-line decomposes oxygen molecules and synthesizes ozone and then 253.7 nm UV-line dissociates ozone. This process creates atomic oxygen which is a strong oxidizing agent. Besides, organic materials exposed to UV rays which can be subjected to photolysis, creating other substances such as ions, free radicals (like: –OH, -COO, -CO, and –COOH), exited molecules, or neutral molecules. Therefore these molecules tend to react with oxygen to form volatile molecules such as CO_2 and H_2O which desorbs from the surface. The result is a clean and hydrophilic surface without any organic contamination, ready for the next treatments[28].

2.4.2 Self assembled monolayers

Molecules able of self-assembly such as silanes, thiols and phosphonic acids usually present an amphiphilic character: A reactive head that reacts with the substrate and a functional tail with low interaction with the substrate and therefore the ability to modify surface properties. When a suitable substrate (metal or oxide) is exposed to a vapor or a solution of such molecules, these organize to form self-assembled monolayers (SAMs) that are covalently bound to the substrate and radically changes its surface properties. [29][30][31]. The tail group can be functionalized by attaching groups such as: -SH, -COOH, NH_2 to tailor the final surface properties. [4]
SAMs prepare a condition to proper crystal growth of organic materials on the surface of metal or metal oxide with the help of properly selected functional groups. For OFETs, dielectric surface treatment by SAMs modify the crystal growth and electronic performance of the semiconductor since the characteristics and performance of the organic semiconductors are in a direct relationship with the dielectric/semiconductor interface.[19][4] Based on the type and molecular structure of applied SAMs the surface energy of the dielectric, may be changed to provide a better fit to the semiconductor material. [4]. SAM surface treatment provides the following benefits: i) ease of preparation in solution or vapor phases ii) applicability on thin film structures iii) efficient improving of OFET performance [29].
After fabrication of SAMs on the substrate surface, they can be analyzed by utilizing of various methods such as: contact angle and wettability, ellipsometry, X-ray photon spectroscopy, atomic force microscopy and quartz crystal membrane [31].

2.4.3 Friction transfer of Polytetrafluoroethylene (PTFE)

In this section, we describe a substrate treatment used in this work that aims ordered growth of molecular crystals using grapho-epitaxy. Grapho-epitaxy doesn't require a match between the crystal lattices of the substrate and grown material. Instead, it acts on a longer scale to orient crystals as they growth along a certain preferential direction determined not only by the crystallinity of the substrate but also by its topography.

The fabrication of highly oriented film of PTFE by the friction transfer method was introduced by Wittmann et.al. in 1991[5]. The basic idea of the method is schematically shown on Figure 8.[5]

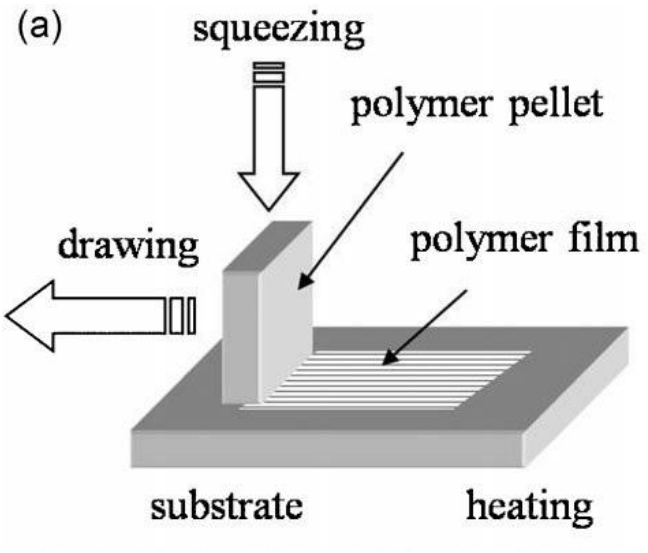

Figure 8.Schematic demonstration of the friction transfer method [5]

In this method a contact pressure of 1MPa is provided by PTFE bar on the glass substrate which is heated up to 300°C. By drawing of the PTFE bar with constant speed of 1mm/s, a uniform and aligned film is deposited on the substrate along the drawing direction. [32] Figure 9. shows the atomic force microscopy (AFM) image of a friction transfer PTFE film on a glass substrate.

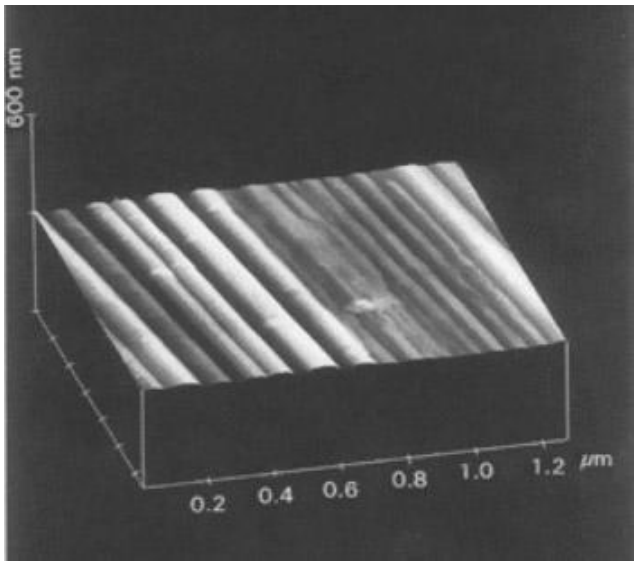

Figure 9.AFM image of PTFE transferred film [32]

The rough surface of PTFE film contains mounds and valleys. The distance between mounds is variable from 25 to 500nm whereas the height of each individual mound is between 1 and 50nm. The average thickness of PTFE film transferred by this method is 20 to 30nm. It can be concluded that the high ability of crystalline PTFE film to orient the over-layer is related to topography of the PTFE film. Indeed presence of small grooves on the surface can induce the anisotropy nucleation of overlayer materials, the concept which is known as grapho-epitaxy.[32]

Different types of polymers can be utilized for the friction transfer of oriented thin film on substrate although PTFE shows highly versatile results for a wide range of materials[33].The materials that are grown on the PTFE film can have various chemical compositions and physical properties, ranging from liquid crystals, small molecules, to polymeric materials and other inorganic compounds[33].Table 1. mentions materials which are successfully grown over PTFE.[33]

Table 1.Examples of materials grown in highly oriented form on mechanically deposited thin films of PTFE [33]

Species	Conditions*
Small organic	
adipic acid	vapour
anthraquinone	melt, 200 °C
chloranil (tetrachloro-*p*-benzoquinone)	vapour
alkanes	melt, 100 °C
perfluoroalkanes	melt, 180 °C
2-methyl 4-nitroaniline	vapour
Inorganic	
thallium chloride	vapour
Liquid crystalline	
mixtures of 4-cyano-4′-*n*-alkylbiphenyls	melt, 80 °C
4-*n*-propyl-cyclohexyl-4′-ethoxybenzene	melt, 100 °C
poly-[4-cyanophenyl 4-(6 acryloyloxy-hexyloxy) benzoate]	melt, 150 °C
Monomer	
para-xylylene, polymerized into poly(p-xylylene)	†
Polymer	
poly(tetrafluoroethylene) oligomers	melt, 200 °C
poly(ethylene terephthalate)	melt, 270 °C
poly(butylene terephthalate)	melt, 260 °C
polyethylene	melt, 160 °C
nylon 6	melt, 280 °C
nylon 11	melt, 200 °C
poly(1-butene)	melt, 150 °C
poly-ε(caprolactone)	melt, 100 °C
polyaniline	5 wt% solution in H_2SO_4, 25 °C
poly-para-(phenylene terephthalamide)	2 wt% solution in H_2SO_4, 25 °C

Thanks to its chemical inertness, its self-lubricating properties and its good thermal resistance, PTFE is a versatile engineering polymer used in a very wide field of applications. The molecular structure of PTFE is shown in Figure 10. [34]

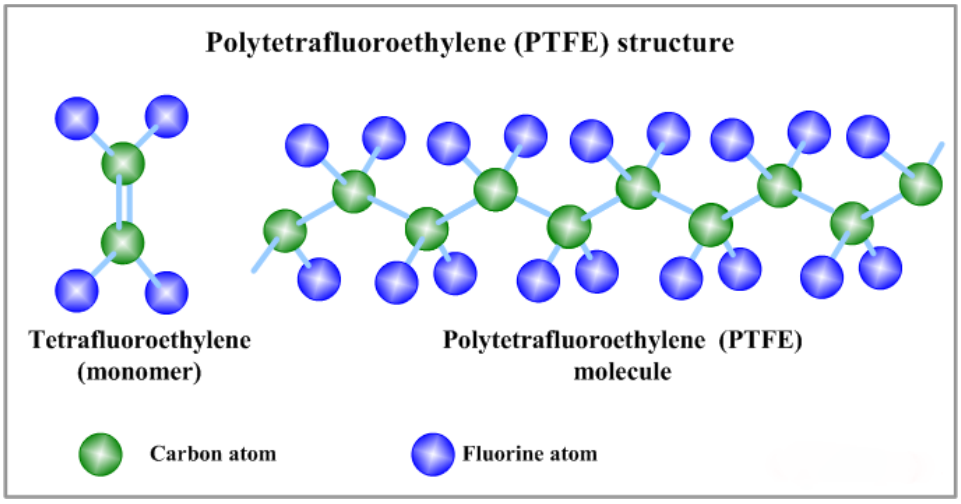

Figure 10.Molecular structure of PTFE [34]

PTFE demonstrates a low coefficient of friction when it is drawn on a hard surface. The coefficient of friction for PTFE is low compared to other polymers such as low density polyethylene (LDPE), high density polyethylene (HDPE) and nylon [35]. Despite the low friction, PTFE has a low resistivity against wear [35]. Combination of low coefficient of friction and low wear resistance makes PTFE easy to mechanically transfer as a thin film on a substrate. By drawing of PTFE on a hard surface, molecular chain of PTFE brakes into chain fragments by breaking –c-c- and/or –c-f- bonds. Subsequently, these active groups create chemical bond with the substrate. Creating active bonds result in forming a strong adhesion and a coherent transfer film on the substrate.[35]

Different types of organic semiconductors such as poly(3-hexylthiophene-2,5-diyl)(P3HT), hexa-peri-hexabenzocoronene (HBC) and pentacene have been successfully grown on PTFE layer, which could improve the anisotropic performance of the OFET applications [5]. Figure. 11a schematically shows the growth of columnar HBC stacks on the aligned PTFE layer. Figure 11. b and c illustrate the optical images of highly ordered film of HBC which are grown on the PTFE surface. The growth of HBC stacks on the top of the surface, free of aligned PTFE is shown in Figure 11. b top left corner, while the rest of image illustrates the oriented topography of HBC which is obtained in the presence of PTFE film. [5]

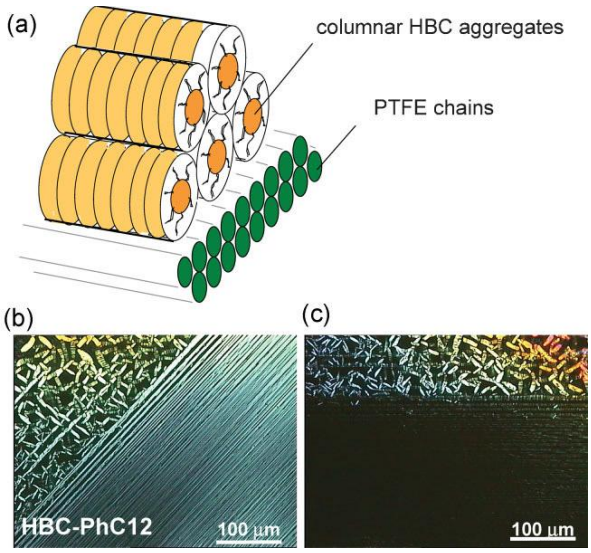

Figure 11.Schematic image of alignment of columnar HBC stacks on the highly ordered PTFE film (a) Polarized optical microscope images of HBC film on oriented PTFE ±45° (b) and along the alignment direction (c) [5]

For this typical example field effect mobilities of 0.5-1.0×10^{-3} cm^2/Vs is measured for devices with the channels along the HBC orientation while for devices with channels perpendicular to the HBC alignment mobilities of 1.0×10^{-5} cm^2/Vs are obtained [5].

3. EXPERIMENTAL

This chapter explains the experimental part of this study. It includes a description of the studied materials and it details the steps necessary to the fabrication of simple common bottom gate – top contact OFETs. The succession of steps is given in Figure 12. It includes substrate cleaning, PTFE friction transfer, UV-Ozone surface treatment, deposition of self assembled monolayer (SAM), deposition of 2 different organic semiconductors and finally deposition of gold contacts.

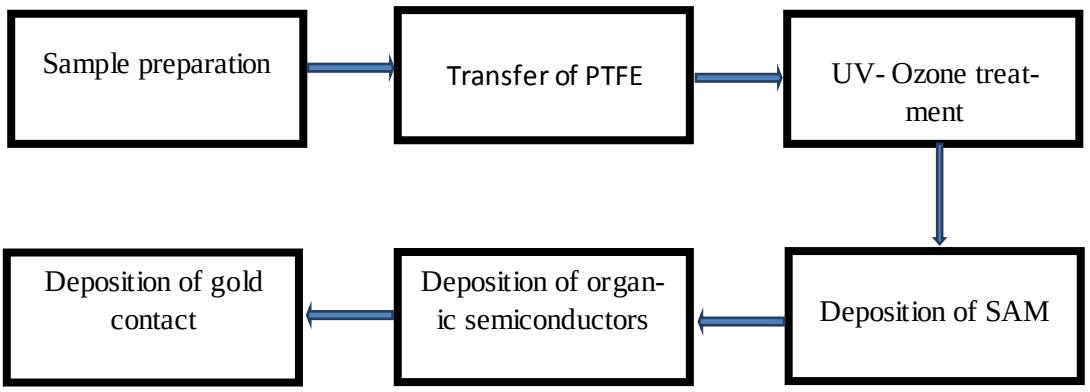

Figure 12.Successive steps from sample preparation to make new TFTs

3.1 Material

The materials used in this study have been described in the introduction chapter, when describing the state of the art. Here, for reproducibility purposes, we detail their origin and level of purity as well as relevant specifications which are utilized in the experimental part-Highly doped silicon substrate

3.1.1 Silicon substrates for PTFE transfer optimization

Silicon wafers are produced in large numbers by cutting single crystalline ingots that are extracted from molten silicon bath using the Czochralski Process. After cutting, the 200 mm diameter Si wafers are polished to deliver an atomically flat single crystalline surface. When exposed to air, this surface oxidizes, leaving a ~2 nm thick native oxide on the surface. For screening the best conditions for PTFE transfer by friction, we used 2x2 cm substrates cut from such a Si wafer.

3.1.2 Highly doped sSi/SiO_2 substrates for OFETs

In this case, after cutting and polishing, the Si wafer are heavily doped to become conductive and covered with 120-126 nm thermally grown silicon dioxide. The high quality SiO_2 is free of pinholes and provides a proper condition for growing of the thin film above the substrate. These constitute the common gate and the gate dielectric, respectively. 2×2 cm silicon substrates are then cut and detached from each individual silicon wafer.

3.1.3 PTFE

The PTFE used in this study is industrial virgin grade PTFE obtained from GoodFellow. The PTFE was shaped as a roll by a mechanical workshop using milling machines.

3.1.4 Liquid crystal

The liquid crystal solution for characterization by polarized optical microscopy (POM) was purchased from Accelerated Analysis. ''LC29R liquid crystal'' is a low viscosity solution of pure liquid crystal dissolved in solvent. This solution has the following composition:

i) Hexylcyanobiphenyl CAS No. 41122-70-7 < 10%
ii) Methylene Chloride CAS No. 75-09-2 > 90%

Liquid crystal is stored in cool and dry place with sufficient ventilation.

3.1.5 Octadecyl-trichloro-silane (ODTS)

The alkylsilane compound ODTS was used to form SAMs by reaction with the SiO_2 surface of the substrate. It was purchased from Sigma-Aldrich® and used without further internal purification. ODTS bottle is stored in the refrigerator prior to the use.

3.1.6 DNTT and C_{10}-DNTT

DNTT and C_{10}-DNTT in the form of powders and sublimed grade of 99% were provided by Nippon Kayaku Co., Tokyo, Japan.

3.2 Sample preparation

As it mentioned, two types of samples have been used throughout this study. To investigate the optimum condition for friction transfer of PTFE, we used 2x2 cm undoped silicon substrates with native oxide. After finding the reproducible condition for deposition of PTFE, we used 2×2 cm highly doped silicon substrates with thermally grown SiO_2.

Both types of substrates where subjected to the same cleaning procedure and UV-Ozone treatment.

3.2.1 Substrate cleaning

The substrate cleaning procedure is a very important process in order to remove all contaminants by breaking the bonds between substrate and contaminations without destroying the substrate. Contaminants can be in different types such as water, dust, oil particles and organic contamination. Cleaning process must be conducted carefully to guarantee reproducibility.
The cleaning, conducted under an appropriate chemical hood includes the following steps carried out in a dedicated beaker in order to avoid contamination.

- 5 minutes soap (Extran® MA 02 Neutral) combined with de-ionized water in the ultrasonic bath
- 2 minutes rinsing of the soap using shower of de-ionized water
- 5 minutes with de-ionized water in the ultrasonic bath
- 5 minutes with recycled acetone in the ultrasonic bath
- 5 minutes with clean acetone in the ultrasonic bath
- 5 minute with recycled isopropyl alcohol (IPA) in the ultrasonic bath
- 5 minutes with clean IPA in the ultrasonic bath

After following those steps every substrate is dried with the help of nitrogen pistol and kept in individual boxes that have been cleaned previously with acetone and IPA.

3.2.2 UV-Ozone cleaning

UV-Ozone treatment is used in order to remove all organic contamination. In this study all substrates were exposed to UV-Ozone right after solvent cleaning. In a few cases, substrates were exposed to UV-Ozone also after friction transfer of PTFE.

The process is carried out in a UVOCS® ultra-violet cleaning machine shown in Figure 13. in two successive steps:

-15 minutes pre-heating of the UV-Ozone machine
-15 minutes exposure of the sample by UV-Ozone

Figure 13.UVOCS® ultra-violet cleaning machine

After this treatment, all organic contamination is removed from the substrate surface and surface would be in a meta-stable oxidizing state. The next surface treatment step must therefore be done quickly after UV-Ozone treatment in order to avoid a return to equilibrium. In this study, the time between UV-Ozone and the next surface treatment is limited to 10 minutes.

3.2.3 PTFE friction transfer

A thin film of PTFE is mechanically transferred on the substrate. In this study, we designed and fabricated a friction transfer machine that improves the state of the art. The picture of this machine is shown in Figure 14.

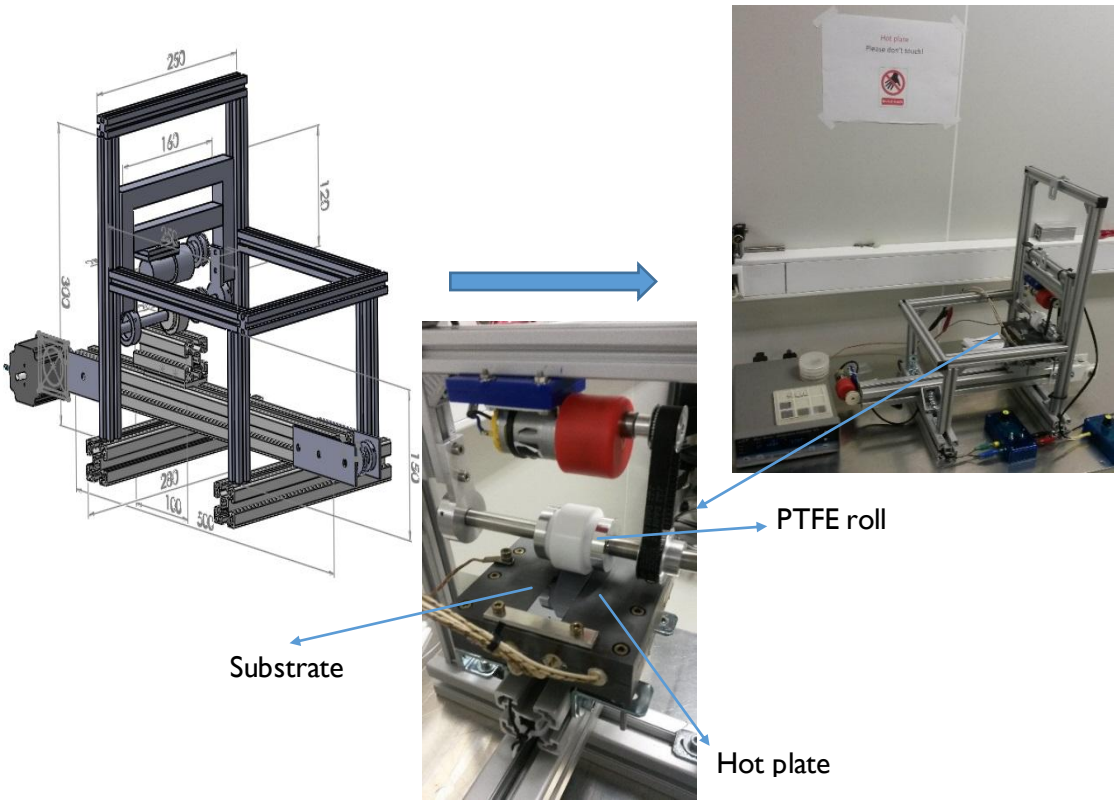

Figure 14.PTFE friction transfer machine used in this study

In this machine, 2×2 cm silicon substrate is mounted on the sample stage, which consists of a hot-plate equipped with thermostat. The substrate temperature can be set between ambient and 320°C. Thanks to a DC motor, the sampler stage linearly moves with a speed regulated between from 0.22 to 2.0 cm/s.

For transfer of PTFE, a 40 mm diameter PTFE roll is placed in contact with the substrate. The roll is rotated by a second DC motor with a speed regulated between 8 to 128 rounds per minute (rpm). The contact pressure provided by the PTFE roll on the substrate is set by the weight of the scaffold holding the roll and the motor. It can be adjusted by adding or removing of copper weights to the scaffold.
Thin film of PTFE is mechanically transferred by passing the substrate from rolling PTFE roller.

3.2.4 Deposition of SAMs

The formation of SAM takes place in Thermo Scientific Heraeus® Oven. This oven is equipped with a homebuilt small vacuum chamber that can be evacuated to a pressure of

approximately 100mbar. Figure 15. shows the SAM deposition equipment used in this study.

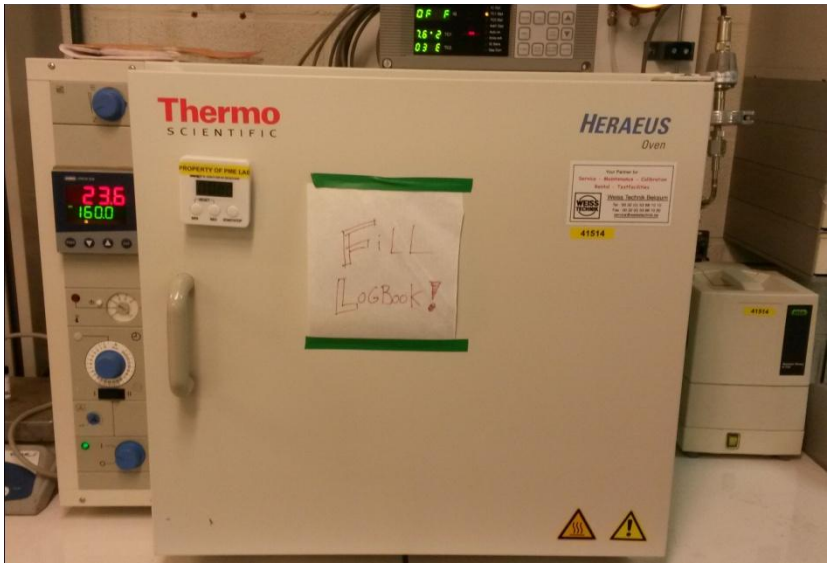

Figure 15.Thermo Scientific Heraeus® Oven used to deposit SAM

Cleaning of the deposition chamber prior to the process is important to improve the quality and reproducibility of deposited SAMs. The SAM for this study is octadecyltrichlorosilane (ODTS).The ODTS deposition process happens in two stages. First, the oven is preheated to a stable 160°C for 1hour. Then 60 µl of ODTS is poured onto a 15×15 mm glass slide inside the hot vacuum chamber. Samples are also placed in the evaporation chamber of the system. It is then hermetically closed and pumped down to a pressure in the range of 100 mbar. We then wait for 1hour, during which ODTS evaporates, diffuses in the deposition chamber and reacts with hydroxyl groups on the sample surface, delivering a self-assembled monolayer.

3.2.5 Deposition of organic semiconductors

Organic semiconductors are deposited by Vacuum Thermal Evaporation (VTE). In this study we used a Ultra High Vacuum cluster system with base pressure below 5 x 10^{-8} Torr. In this system, samples are transferred from a preparation glovebox into a loadlock. After pumping the loadlock to high vacuum, samples are transferred from the loadlock into one of the three deposition chambers, dedicated to different types of organic molecules.

All chambers are equipped with Knudsen evaporation cells and substrate heaters. The evaporation system permits to control the temperature of the sources and substrate by utilizing a feedback loop informed by thermocouples. Moreover, deposition rate is

measured by a calibrated Quartz Crystal Microbalance (QCM). The deposition process is controlled and monitored with the help of a Labview program. This program allows monitoring all process values, such as substrate and source temperatures, deposition rate and chamber pressure. It can also ease the deposition process by automatically warming up source cells and timing deposition.

In this study 3 different types of organic semiconductors including DNTT and C_{10}-DNTT and were deposited in the cluster system. The overall procedure for all organic materials are the same, although the source and substrate temperatures as well as deposition rate are different based on the type of organic molecules. Figure 16. shows a UHV VTE deposition chamber and its loadlock, similar to the cluster system used in this study.

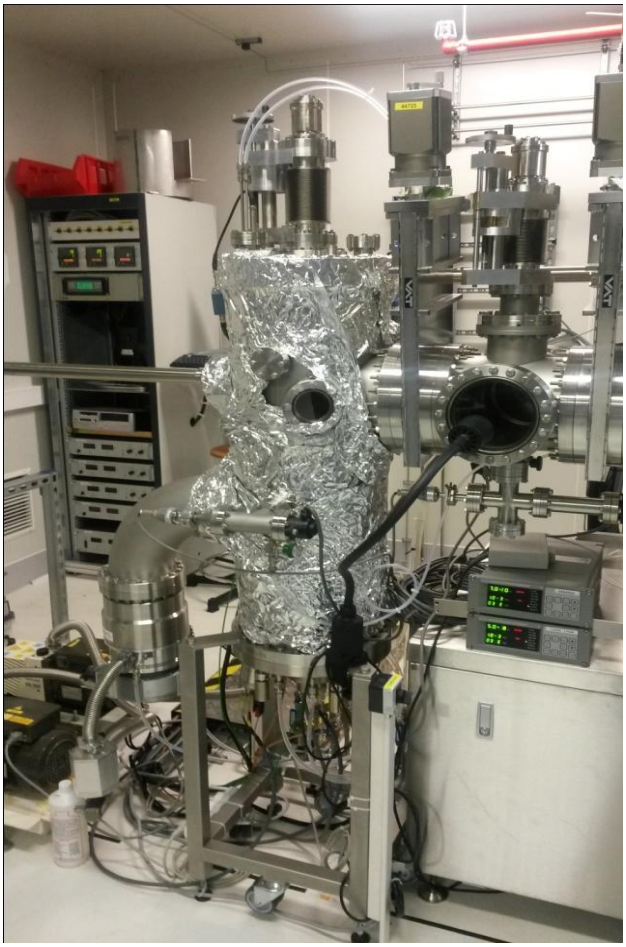

Figure 16.Cluster system used for deposition of organic molecules

3.3 Deposition of gold contacts

Gold contacts are deposited by VTE in a Angstrom Deposition System. Figure 17. illustrates angstrom system used in this study.

Figure 17.Angstrom system used for deposition of gold contacts

The Angstrom system is a metallization chamber that can fully automatically deposit different types of metals by setting a few parameters such as deposition rate, substrate temperature and final thickness. In order to deposit metal, a high voltage is applied on a tungsten boat containing small metal pellet (gold pallet in this study). For each deposition 1 short gold pellet is used which effectively deposits 60-80 nm uniform gold contacts.

Substrates are attached onto an aluminum slab, where it is possible to put different sizes of samples and to mount a shadow mask on top of the substrates, in order to pattern the metal layer. The shadow mask that was mostly used in this study is schematically shown in Figure 18.

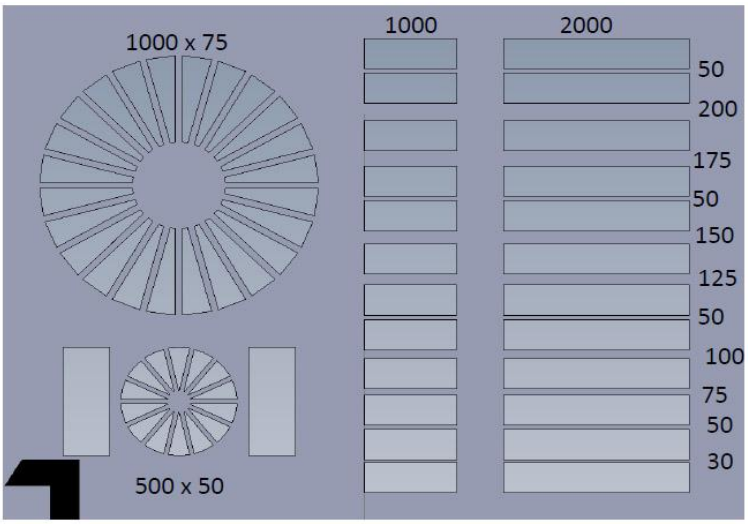

Figure 18.Shadow mask pattern used in this study

This shadow mask is a Kovar metal piece with well-defined tiny apertures. It patterns source and drain contacts defining transistors with different width and channel lengths,

as well as various channel orientations. After mounting the substrates and shadow masks, the sample holder (aluminum slab) is transferred from the glovebox directly into the vented metallization chamber. The aluminum slab is placed in good contact with cooling chuck whose temperature is regulated down to -10°C. After evacuation of the vacuum chamber (P < 5e-7 Torr), the tungsten boat loaded with gold pellets is resistively heated up to evaporation temperature. After deposition rate reaches to 1 Å/s and gets stable, the substrate shutter is opened and deposition starts. 60 nm of gold, as monitored by a calibrated QCM, is deposited on the sample through the shadow mask in duration of about 10 min.

3.4 Characterization

In this section characterization methods and equipments needed in this study are discussed. Indeed 3 techniques for characterization of transferred PTFE film were used which are explained in detail following by the method for measuring the wettability of the solid surface. In addition topography of grown organic semiconductors and electrical performance of devices are described.

3.4.1 Liquid crystal (LC) imaging technique

One easy and swift way to analyze the birefringent property of PTFE film is using liquid crystal under polarized optical microscopy. Actually a material is known as birefringent if it demonstrates different refractive index based on the polarization and propagation direction of the light. Birefringent materials mostly have asymmetric crystal structure[36].To analysis the birefringent property of the PTFE film, a drop of liquid crystal (LC29R) is removed by tip of the nylon liner brush. Then the brush is touched the surface to extend the liquid. In 30-60 seconds the solvent is dissipated and examination can be followed at room temperature with Olympus Provis optical microscope under cross polarized condition. To assess the birefringent therefore the sample is slightly rotated ±45° to the direction of the PTFE deposition. Thus the change in the intensity of transmitted polarized light is observed.

3.4.2 3D profilometer: Dektak instrument

The thickness of PTFE film is measured by using of Dektak 3D profilometer instrument. Dektak 150 accurately measures the height difference over the surface of the sample. This system operates by the stylus physically making contact with the sample surface and moving the stage front to back to measure changes in surface height. It is also used to determine photolithography resist thickness. Dektak measurement is con-

sidered as a destructive technique since a scratch must be introduced on the sample surface prior to the measurement.

3.4.3 Atomic Force Microscopy (AFM) analysis

Topography of the PTFE film is analyzed by using Agilent 5100 Atomic Force Microscopy. AFM analysis is a non-destructive technique which consists of scanning of the surface of the sample by an oscillating cantilever and interacting with the surface through the extremity of a very fine tip.

3.4.4 Contact angle measurement

The wettability of a solid surface is an important point in the theoretical research and industrial application [37]. Contact angle measurement is a fast and cheap method of analyzing the hydrophobicity degree of a solid surface. Indeed by measuring the contact angle, wetting behavior of a various liquids on the surface is obtained. This value therefore is used to determine the interfacial energies of the system[37]. The contact angle is dependent on the chemical composition and topography of the surface and it can be changed by altering these two parameters [38]. Water contact angle measurements were carried out using contact angle meter Data Physics OCS. A droplet of distilled water (DIW) is poured on the surface and the image of droplet is illustrated on the screen with protractor. By proper regulation the contact angle of the water droplet and solid surface at the point of contact is measured. Figure 19. shows the equipment and a contact angle measurement using DIW on the surface.

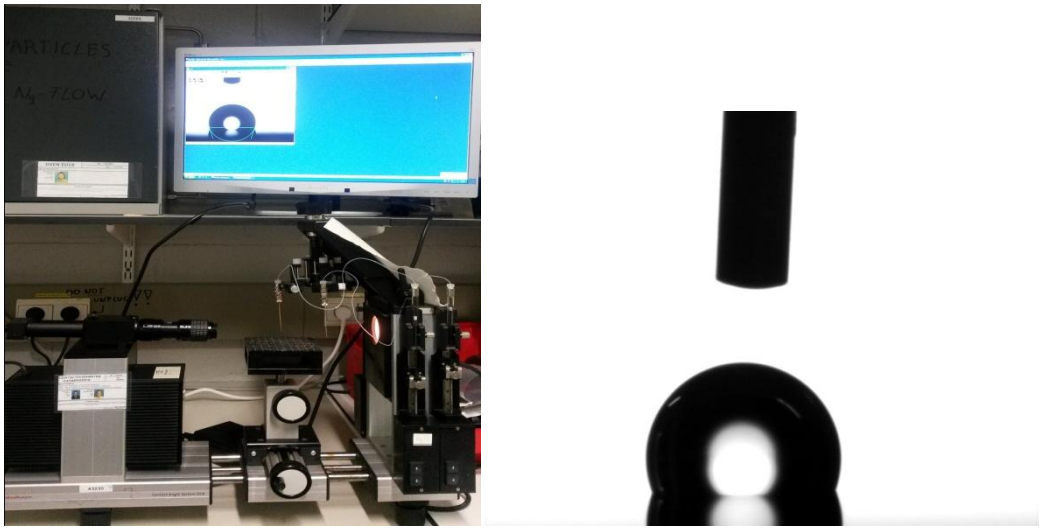

Figure 19.Left: Contact angle equipment used in this study, right: one typical contact angle measurement

3.4.5 Transistor electrical measurement

For characterization of the transistors, devices are measured by a mechanical probe station linked to the HP4156C parameter analyzer. Indeed mechanical probe station obtains signals from the internal nodes of a semiconductor device. In this study, a two needle measurement was used. When the device is electrically stimulated, the probe station obtains a signal and this signal is analyzed by the HP4156C parameter analyzer. After the measurement the LabVIEW virtual software collects data from the parameter analyzer. MATLAB program uses the data provided by LabVIEW; thus further information is extracted. Figure 20. indicates the probe station and parameter analyzer used in this experiment.

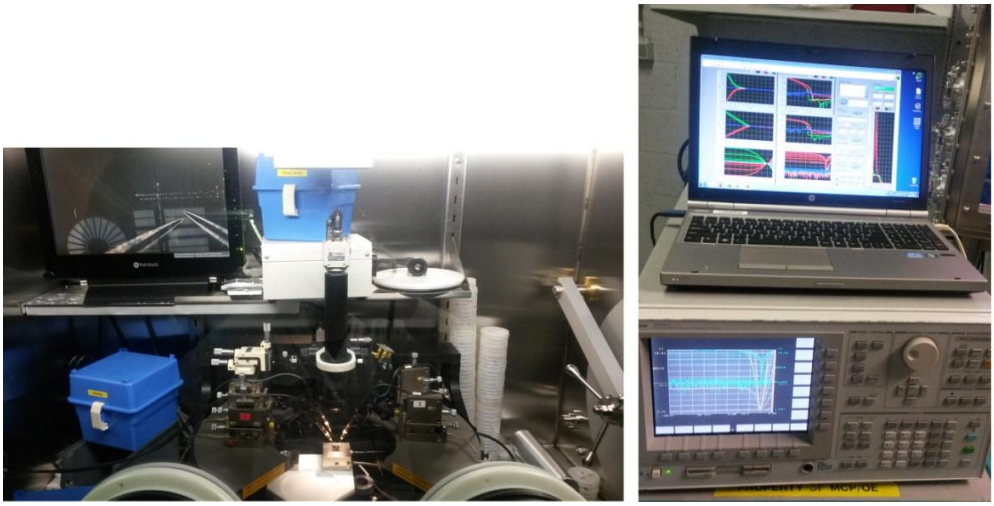

Figure 20.probe station system, right: HP4156C parameter analyzer

The performance of the transistor is characterized by measuring the devices in 2 distinct regimes: linear (Ohmic) and saturation (active) which are briefly explained.

By applying the gate bias (since we use p-type transistor, a negative gate bias is applied), a charge carrier (holes for p-type) are constantly accumulated along the channel and therefore transistor is turned on. The bias applied between source and drain allows for current to flow through the channel, by injection of charge from source to drain. The small charges between the source and drain contacts does not interfere much with the strong field generated by gate bias. In this condition, charge accumulation and thus current flow are linearly changed with the gate bias. Table 2. shows the parameter for both regimes [2][3].

Table 2.Parameters for measuring the transistor in linear and saturation regimes

Regime	Drain Voltage (V)	Initial Gate Voltage (V)	Final Gate Voltage (V)	Step (V/s)
Linear	-1	15	-40	0.5
Saturation	-40	15	-40	0.5

In the linear regime the initial and final gate voltage (V_{GS}) of 15 and -40V are respectively applied in the steps of 0.5V/s. The drain voltage (V_{DS}) is set to -1V.

Applying of a negative gate bias leads to accumulation of charge carrier in the transistor channel and turning the transistor on, although in the saturation regime the strong source and drain bias interferes with the fields induced by the gate. In the region of the drain, fields tend to cancel each other and eliminating of the charge accumulation that causes the channel pinch-off. In fact the onset of the saturation regime is called pinch-off. The current flows in the saturation regime are limited by pinch-off region. Accordingly the current saturation is independent of the applied gate bias in this regime [2][3]. As it is shown in table 2. the drain voltage is adjusted to -40V in this region.

By extracting the graphs from MATLAB program, it is possible to analysis the transistor in both linear and saturation regimes. For a precise measurement of the transistor it is recommended to characterize the devices in the both regimes. In fact, the linear mode is a conceptually simpler mode and the physics underlying the transistor operation can be identified in this mode. The contact resistance is particularly extracted in the linear regime[2][3].
On the other hand, since the saturation regime operates at high drain voltage, it shows how the transistor operates in digital mode as is done in the most circuits [2][3].

4. RESULTS AND DISCUSSION

This chapter looks at the results of the experiments carried out in this study. The friction transfer of aligned PTFE required the assembly of a specific tool and an optimization work to find the best processing conditions. This activity is discussed in the first section of this chapter. Two different organic semiconductors were then grown on substrate with aligned PTFE. The impact of this pretreatment on layer morphology and electrical characteristics is discussed in the second section of this chapter.

4.1 Aligned PTFE by friction transfer

As explained in the theory chapter, the aim for PTFE deposition by friction transfer is to form a coherent and oriented thin film of PTFE on the dielectric layer. This film can then serve as a template to orient the subsequent growth of organic semiconductor. In the literature, PTFE is usually transferred by translating a rod on the substrate. As it is difficult to precisely control the contact area between the rod and the substrate, this method yields non-uniform films that are difficult to reproduce. In this work, we explore a different approach to apply this treatment. The tool described in the experimental chapter relies on a PTFE roller that comes in contact with the linearly moving substrate, as schematically shown in Figure 21. In this case, the contact between the roller and the substrate is a line, not an area. It is therefore easier to ensure uniform contact. Also, the linear motion of the substrate under the roll ensures uniformity along the direction of motion. A number of parameters must be optimized to obtain the desired aligned PTFE films. The variables include:

1. Rotation speed of the PTFE roller
2. Linear speed of the substrate
3. Number of passes of the PTFE roller on the substrate
4. Contact pressure
5. Substrate temperature

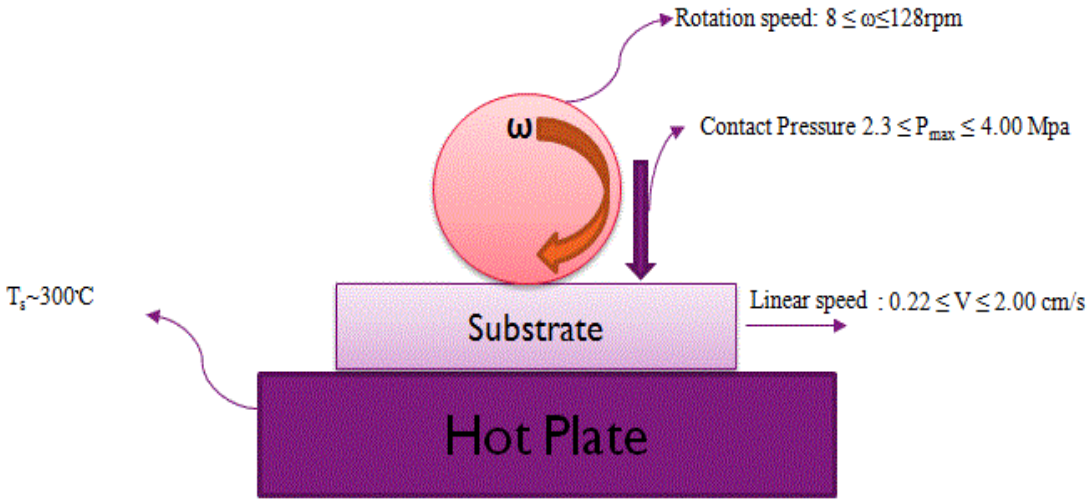

Figure 21. Schematic of variables of friction transfer machine of this study

All parameters are readily available but for the contact pressure. Indeed, as the contact between the PTFE roll and the substrate is a line, pressure applied by the roll on the substrate is a non-uniform field that depends on the local deformation of both the roll and the substrate. The value of contact pressure can be calculated using Hertzian contact pressure equation[39]. For effective using of this equation we assume a system consists of PTFE roller as a cylinder on the flat plate of silicon substrate. Figure 22. indicated the schematic image of the system[40].

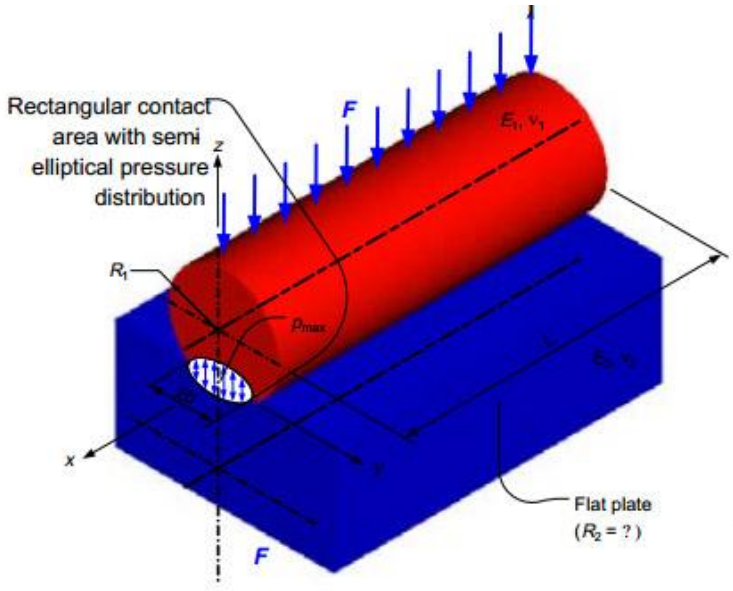

Figure 22.Schematic image of the system (Cylinder on the flat plate) [40]

The maximum Hertzian contact pressure P_{max} is calculated from equation (5) :

$$P_{max}=\frac{2F}{\pi bL} \qquad (5)$$

Where F is the force applied by the roll onto the substrate and L is the length of the contact line. The half-contact width b is obtained from the equation (6) :

$$b=\frac{4F[\frac{1-\nu_1^2}{E_1}+\frac{1-\nu_2^2}{E_2}]}{\pi L(\frac{1}{R_1}+\frac{1}{R_2})} \qquad (6)$$

Whereν_1 and ν_2 are the Poisson's ratio of PTFE roll and substrate E_1 and E_2 are the Elastic modulus of the roll and the substrate respectively, and R_1 is the radius of roll and . Since the radius of the substrate tends to infinity and E_2 is much higher than that of the roll we can simplify the equation (6) into equation (7) :

$$b=\frac{4FR}{\pi L}\left(\frac{1-\nu^2}{E}\right) \qquad (7)$$

In our experiments, equation (5) and (7) can be parameterized with:
$\nu = 0.4$, E= 0.5GPa, L=18mm, R= 20mm and the weight of PTFE roll and scaffold is variable between 976 to 3000 gr. Therefore the maximum contact pressure is between 2.3 and 4 Mpa.

During the study, two system enhancements helped improving the aligned PTFE layer quality: The addition of a heating stage on the equipment to warm the substrates up to 300°C, and the lowering of the contact pressure. In the following, the optimization work is divided between the work without and with the heating stage, as well as the work at lower contact pressure.

4.1.1 Room temperature experiments

At the beginning after repeating the experiments at different linear and rotation speeds, we recognized that the film with the better quality could be obtained in the slower speeds. Hence, we set the linear and rotation speeds to the value of 0.22 cm/s and 8.00 rpm respectively which were the slowest linear and rotation speed of our machine. Indeed the slower speeds deliver a better quality film on the substrate.

As the slowest speeds yield the most uniform films, it is interesting to multiply the number of passes in the hope to enhance the alignment.

For higher number of passes, i.e. more than 10 passes, a thick film of PTFE film was transferred on the sample. As it is shown in the Figure 23. , this film was under the risk of peeling.

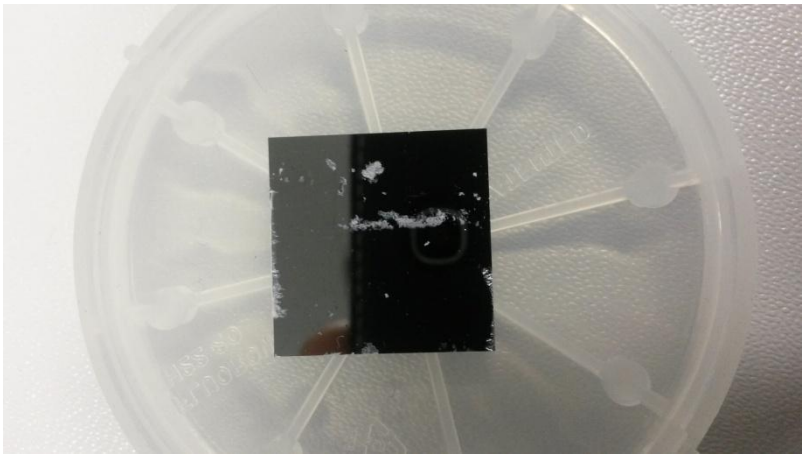

Figure 23.High thickness of PTFE on the substrate

To remove the peels we rubbed the PTFE surface on a piece of clean velvet cloth with the speed of 1cm/s in the distance of 100cm. It was also possible to remove the peels by blowing of the nitrogen on the PTFE surface. After characterization of a number of PTFE films we found out that in some cases although we could get an oriented film on the sample, they were not reproducible. In addition further passing of the PTFE on the substrate would shift the interaction from substrate-PTFE roller to PTFE film-PTFE roller with a very low coefficient of friction. So we understood that even with 1 pass we can get a thin film of PTFE on the substrate, thus we continued the experiments with 1 passing.

The experiment was followed by increasing the substrate temperature from ambient to slightly above the glass transition temperature of PTFE (T_g = 115 °C) and finally to 300 °C. In the both conditions, we used the slowest speeds and one pass of the PTFE roller. . Better results were more promising for samples prepared at the highest temperatures (300 ºC). However, sample to sample reproducibility remained was still a problem. So temperature was set to 300 ºC as the modified temperature and we started finding the optimal value for the contact pressure.

4.1.2 Lowering the contact pressure

In the room temperature experiments, we already experimented on contact pressure by adding copper blocks to increase the contact pressure. Each block was about 1kg. In this step experiments were continued by removing the copper weights due to reduce the con-

tact pressure. Based on the results, we were on the right track to get to a reproducible method of transferring PTFE film on the substrate.
Therefore maximum contact pressure was calculated P_{max}= 2.3MPa.

We understood that by increasing the contact pressure, friction is reduced thus wear of PTFE bulk goes down. Therefore transferring of the PTFE from the bulk would be less. By reducing of the contact pressure and calculated the value from Hertzian equation we optimized contact pressure as the last variable. By repeating the experiments with the optimal parameters, we got the reproducible results for transferring PTFE film on the substrate. Figure 24. shows the liquid crystal imaging of one of the samples prepared with optimal parameters.

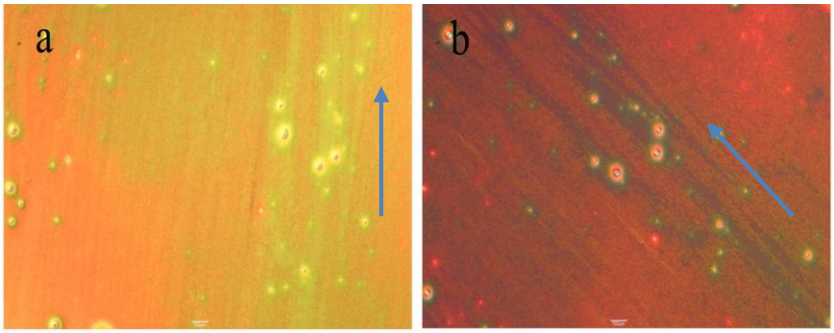

Figure 24.Difference in the intensity of transmitted polarized light for PTFE in ±45° to the deposition alignment

The difference in the intensity of the polarized light represents the aligned orientation of the PTFE film on the substrate.

We also took AFM image of different samples. As it is shown in the Figure 25. the surface of PTFE was not smooth but consisted of a bunch of steps of different heights.

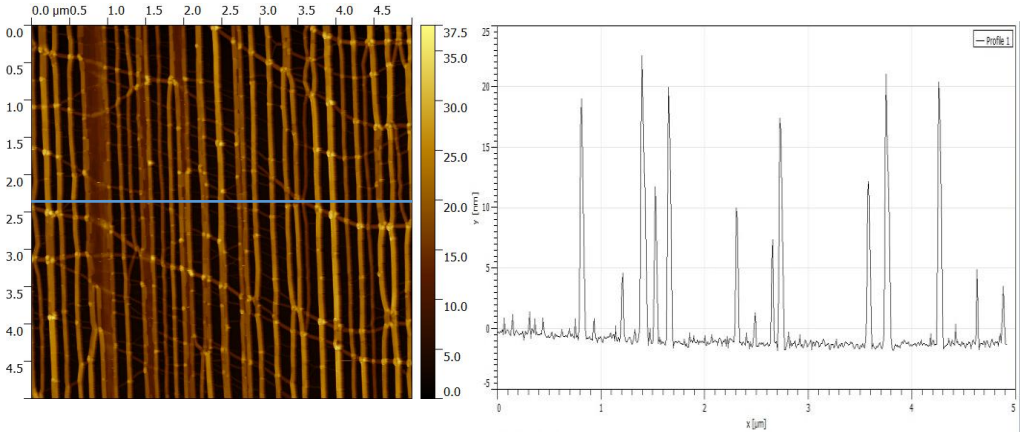

Figure 26.AFM image of a developed PTFE film in this study

Indeed these grooves and valleys were extended along the deposition direction. It is expected that these small scale grooves on the PTFE surface can dictated the anisotropic nucleation of the over-layer organic semiconductors. The concept which was discussed as grapho-epitaxy.

4.2 Growth of organic semiconductors on aligned PTFE

As it is explained in the experimental section, all organic semiconductors are deposited by vacuum thermal evaporation method via cluster system. Based on the type of organic molecules, deposition parameters such as deposition rate, ramp rate, substrate temperature and final thickness are different. In the following sections the deposition condition of the organic molecules used in this study are explained. The aim is to have the optimal condition for oriented growth of organic semiconductor molecules on the substrate. Therefore results are compared for 2 series of the reference and sample using PTFE layer.

4.2.1 Deposition of C_{10}-DNTT

Deposition of C_{10}-DNTT is carried out by increasing the temperature of substrate and source powder. First the substrate temperature is increased to 80°C. It takes about 1 hour to have a stable substrate temperature. The next stage is to warm up the source powder temperature. This stage is made of 3 consecutive temperature ramping and soaking steps. Table 3. shows the recipe for warming up the C_{10}-DNTT cell.

Table 3. Deposition recipe for C_{10}-DNTT layer. TF: Tooling Factor (Constant permitting to obtain thickness of material in the substrate by measuring the thickness of materials on the quartz monitor), Dfin: Final Thickness in Angstrom, T: Temperature. RR: Ramp rate, S: Soak Time.

Organic molecule	TF	Dfin (Å)	T1 (°C)	RR1 (°C/min)	S1 (s)	T2 (°C)	RR2 (°C/min)	S2 (s)	T3 (°C)	RR3 (°C/min)	S3 (s)
C_{10}-DNTT	200	150	175	20	240	203	5	120	207	1	30

The aim is to have a constant deposition rate of 0.1 Å/s. Therefore the final temperature is adjusted manually in order to keep the constant deposition speed. The final thickness for C_{10}-DNTT in this study is 15 nm and based on our recipe the overall deposition process takes about 25-26 minutes. Deposition is started and terminated by opening and closing the substrate shutter which blocks the beam of evaporated molecules. After deposition is over, the power to substrate and source heater is turned off which lead to drop

down the deposition rate. When deposition rate falls to 0 Å/s, samples are allowed to be extracted from the deposition chamber to the glovebox through the transfer chamber and the loadlock.

4.2.2 Device annealing

Transistors using C_{10}-DNTT were prepared in 2 series. The difference between these 2 series stem in the use of PTFE above the dielectric. Indeed for reference sample PTFE film was not used. First we decided to monitor the effective healing time for the both series of transistors. Therefore we prepared 2 series of transistors and measured their characteristics as a function of time. Figure 26. illustrates the electrical characteristics of them.

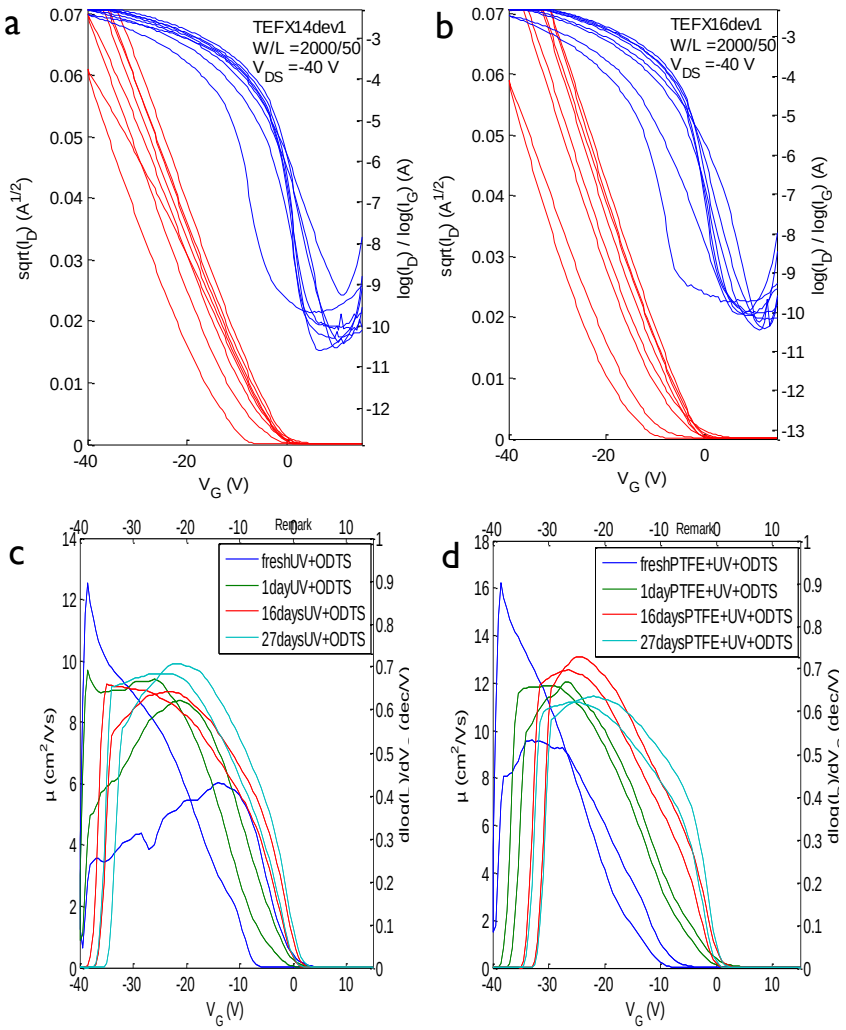

Figure 27.Electrical characteristics for 2 series of transistors prepared using C10-DNTT with the deposition rate of 0.1 Å/s and substrate temperature of 80 °C with the channel width and channel length of 2000 and 200 µm as a function of time. (a , c): Transfer curve and field effect mobility of reference samples, (b , d) Samples using PTFE thin film

Measurements took place in 4 steps. The first measurement happened after gold deposition. For the second measurements samples were kept on the hot plate with the temperature of 50 °C for one day. The third and fourth measurements happened 16 and 27 days respectively at room temperature in the nitrogen glovebox. As it is shown, for both series of transistors the effective evolution in the performance happened after about 2 weeks. Indeed the threshold voltage increased toward 0 V. Field effect mobility got stable. In addition hysteresis reduced over the time which leads to have a less charge trap density in the device. Analogous to the reference sample, healing happens more slowly for transistors with the PTFE film. In fact the reference sample gets to the stable condition faster.

The origin of this healing effect could stem in decreasing of contact resistance. In addition the morphological feature of the C_{10}-DNTT may be improved by recrystallizaion of the chains over the time.

For analysis the performance we compared the electrical characteristics after the healing process. We measured different devices with the channel width of 2000 µm and channel length range from 50 to 200 µm. Based on the results; the devices with the PTFE have the better performance for shorter channel length. We got the field effect mobility for device with the PTFE is 11.32 cm^2/Vs while for the reference is 9.75 cm^2/Vs. The threshold voltage for PTFE transistor and the reference are -3.66 and -3.84 V.

We found out that transistors with PTFE are systematically better for short channels although for longer channels they do not perform properly. The reason could stem from the impossibility for charge carriers to go around the scattering center that interrupt the grooves.

4.2.3 C_{10}-DNTT film morphology

AFM images were taken from both samples to observe the PTFE effect on the morphology compared to the reference sample. As it is shown in Figure 27. there are some degree of orientations for sample with PTFE, although it is not considered as a big evolution.

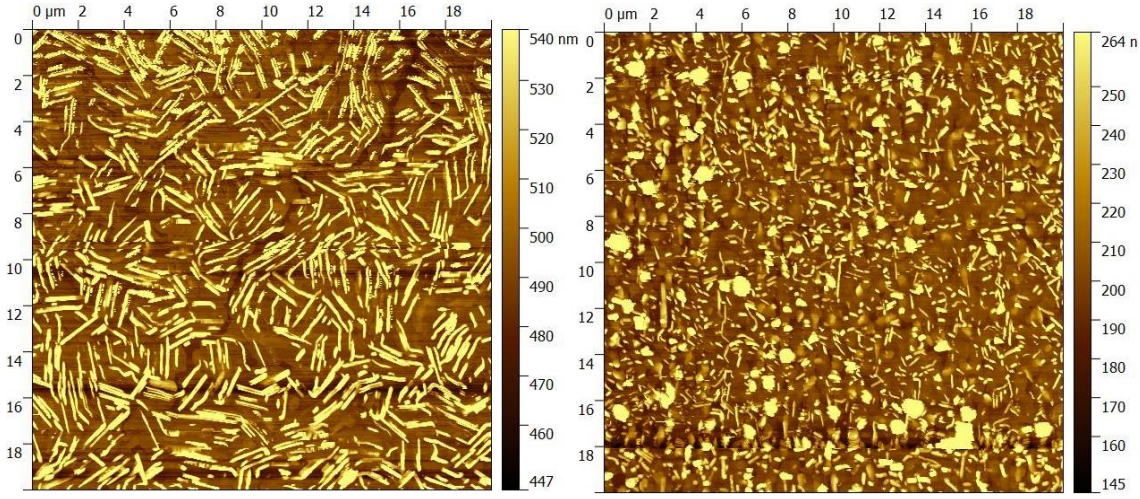

Figure 28.20×20 µm AFM taken by Bruker Dimension EdgeTM equipment. Left: Reference, Right: Sample with PTFE

4.2.4 Channel orientation dependence

As the next experiment, the angle dependence performance was measured for a number of devices with the channel width and length of 1000 and 75 µm. Figure 28. illustrates the transfer curve and field effect mobility for the transistor using PTFE.

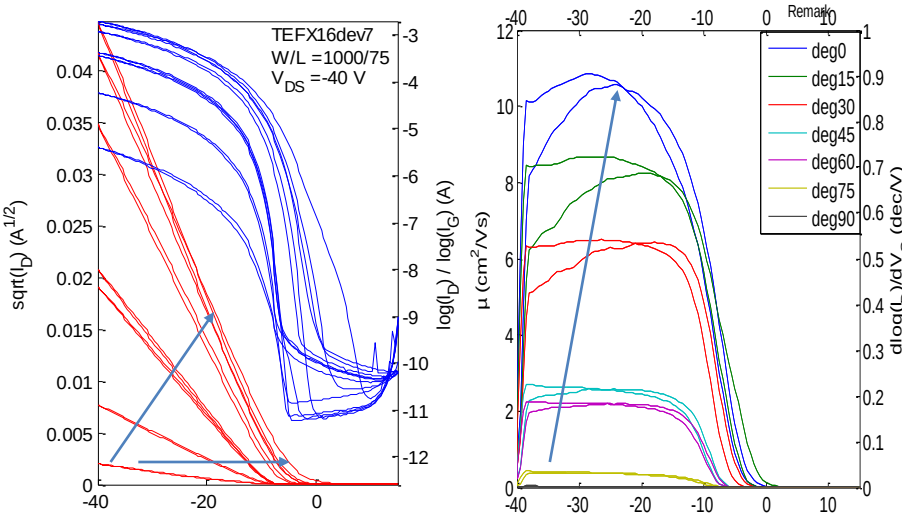

Figure 29.Electrical characteristics of the PTFE transistor as a function of channel orientation to PTFE deposition direction with the deposition rate of 0.1 Å/s and substrate temperature of 80°C with the channel width and channel length of 1000 and 75 µm. Left: Transfer curve, Right: Field effect mobility

For the transistor with PTFE, there is a strong effect of channel orientation to the performance. Indeed the best result is obtained for transistors with channels elongated in the direction of PTFE deposition.

For the transistor with PTFE, there is a strong effect of channel orientation to the performance. Indeed the best result is obtained for transistors with channels elongated in the direction of PTFE orientation.

4.2.5 Deposition of DNTT

DNTT is also deposited in the same cluster system. For this organic molecule, four different substrate temperatures of 42, 60, 80 and 100 °C are used. The final thickness for DNTT in this study is adjusted to 30 nm. We tried different deposition rates of 0.25, 0.5 and 1.0 Å/s. Table 4. indicate the recipe to warm up the DNTT cell.

Table 4. Deposition recipe for DNTT layer

Organic molecule	TF	Dfin (Å)	T1 (°C)	RR1 (°C/min)	S1 (s)	T2 (°C)	RR2 (°C/min)	S2 (s)	T3 (°C)	RR3 (°C/min)	S3 (s)
DNTT	200	300	175	20	240	203	5	120	211	1	30

4.2.6 Substrate temperature variation

Transistors using DNTT as organic semiconductor were prepared in 2 different series. In the first series of experiments, DNTT was deposited with constant deposition rate of 0.25Å/s with different substrate temperatures of 42, 60, 80 and 100 ºC. Devices in transistors prepared with the substrate temperature of 100 ºC did not work. Indeed this temperature was too high for DNTT molecules to condense on substrate. Thus we started to investigate devices prepared in lower substrate temperatures. We prepared 3 series of transistors. For all series DNTT molecule was vacuum evaporated with the speed of 0.25 Å/s to form the overall thickness of 30 nm above the PTFE treated silicon dioxide. Then devices with the channel width and channel length of 2000 and 200 µm respectively were measured. Figure 29. shows the measured transfer characteristic and the effective mobility as a function of substrate temperature for these 3 series of transistors. The highest mobility between these series of devices was obtained for the transistor prepared with the substrate temperature of 80 ºC.

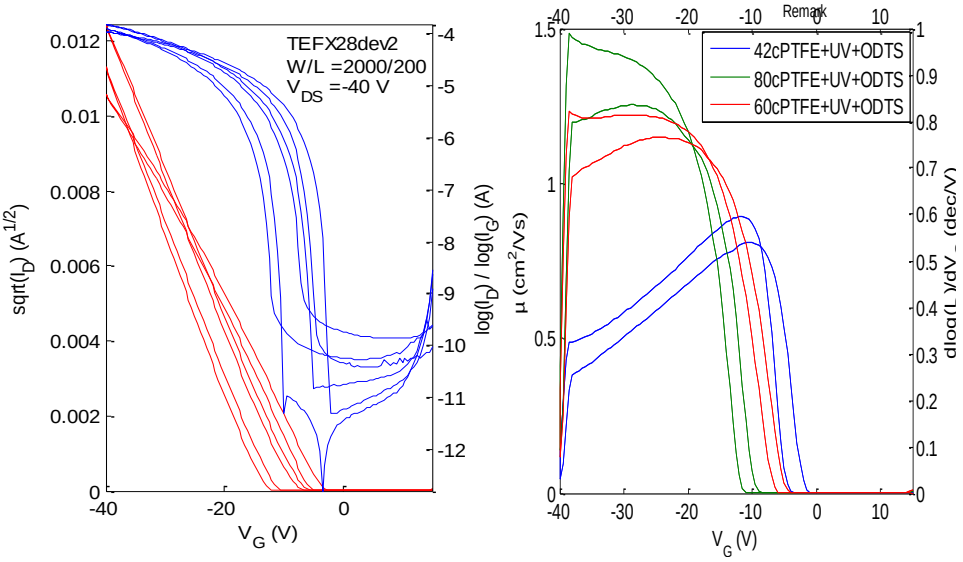

Figure 30.Electrical characteristics of a TFT using DNTT as the semiconductor in the saturation regime. The TFT has the channel length of 200 µm and a channel width of 2000 µm (Left): Transfer characteristics (ID versus VGS), (Right): Carrier field effect mobility

4.2.7 Deposition rate variation

In the second series of the experiments, DNTT layers were vacuum deposited with the substrate temperature of 80 ºC but with two different deposition rates of 0.5 and 1.0 Å/s. The aim is to improve the orientation growth of DNTT which results in enhancing of the performance of the devices. Based on the phase diagram which is explained in section 2.3.1, it was assumed that the better growth would be obtained for the deposition speed of 1.0 Å/s. After analysis the performance of devices, as it was expected, devices prepared with higher deposition rate showed the better performance. Figure 30. indicates the difference between 2 series of sample prepared with 0.5 and 1 Å/s at the same substrate temperature of 80 ºC.

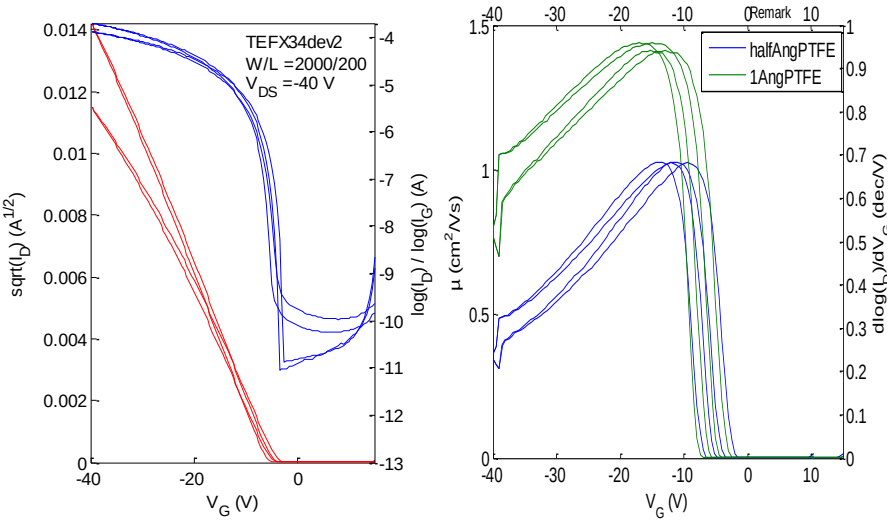

Figure 31. Left: Transfer curves Right: Field effect mobilities of 2 series of devices prepared by 0.5 and 1.0 A/s

4.2.8 DNTT film morphology

To observe the growth pattern, we took AFM images from 2 series of transistors: first transistors which were prepared with substrate temperature of 42 ºC and deposition rate of 0.25 Å/s and the second series, samples with substrate temperature if 80 ºC and deposition rate of 1.0 Å/s. Based on the phase diagram we expected to have transistor with better morphological features for higher substrate temperature and deposition rate. Figure 31. illustrates the AFM images of both series of samples.

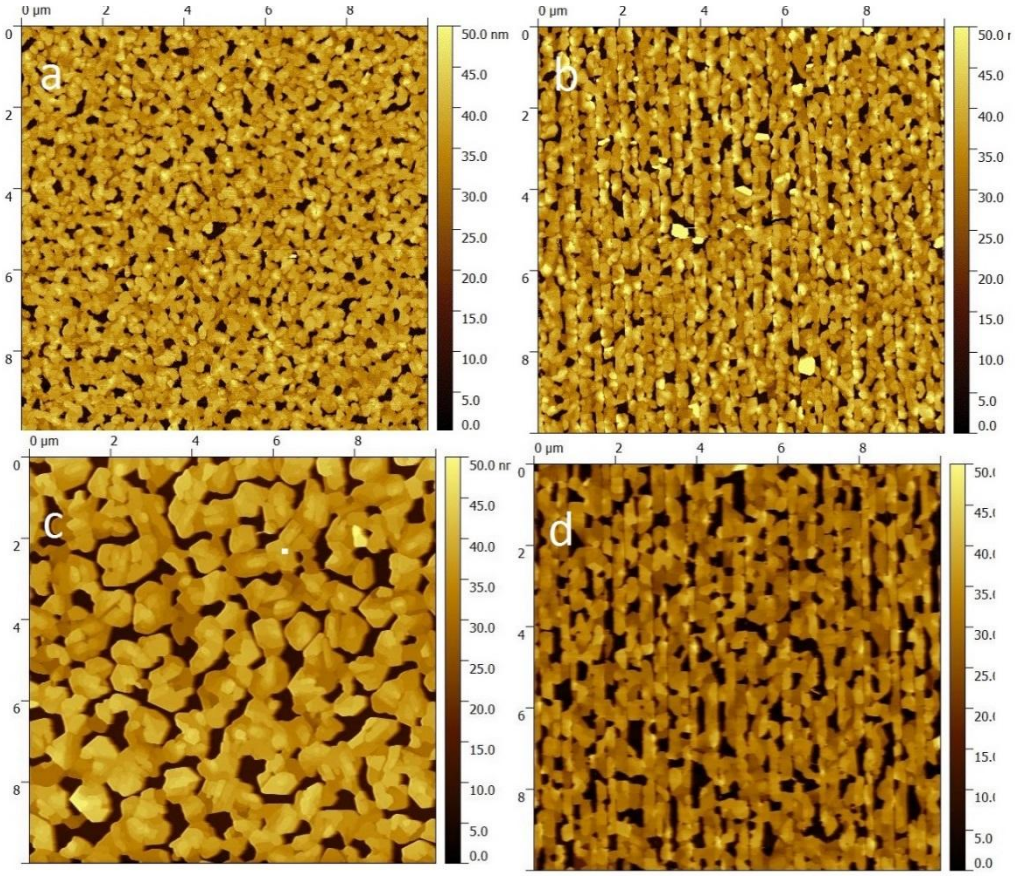

Figure 32.Morphological evolution for 30 nm DNTT film prepared by vacuum thermal evaporation with the deposition condition of: (a , b) r: 0.25 Å/s, Ts: 42°C and (c , d) r: 1.0 Å/s, Ts: 80 °C. a and c are reference and b and d are samples using PTFE film above the dielectric

Images a and c are AFM for reference samples without using PTFE layer. Both samples b and d which were prepared by using of a thin PTFE thin film demonstrate strong anisotropic growth compared to the reference samples. For sample c and d the grain size got bigger and they have a better connection in comparison to the sample a and b.

4.2.9 Best device performance

For analysis of the performance of transistors, we compared transistors c and d. As it is indicated in Figure 32. the subthreshold slope for the sample d which was prepared by PTFE is steeper compared to the reference sample which leads transistor to start up faster.

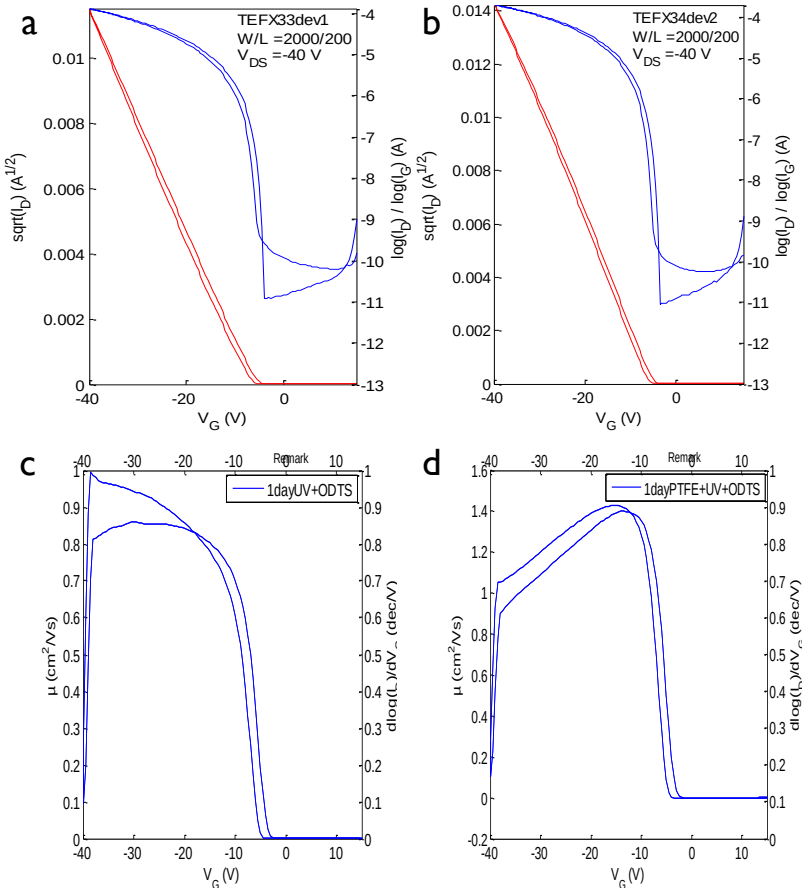

Figure 33.Electrical characteristics for 2 series of transistors prepared using DNTT with the deposition rate of 1.0 Å/s and substrate temperature of 80°C with the channel width and channel length of 2000 and 200 µm. (a , c): Transfer curve and field effect mobility of reference sample, (b , d) Sample using PTFE

The field effect mobility for the sample d is 1.41 cm^2/Vs while for the reference is equal to 0.92 cm^2/Vs. The threshold voltage for sample d is -5.6 V and for sample c the value is -7.4 V.

4.2.10 Channel orientation dependence

We also analyzed the performance of transistors as a function of channel orientation. As it was expected the highest mobility achieved for devices with channels along the PTFE deposition. Figure 33. illustrates the transfer curve and field effect mobility of devices in different orientation from 0º to 90º compared to PTFE deposition direction. The channel width and length are 1000 and 75 µm respectively.

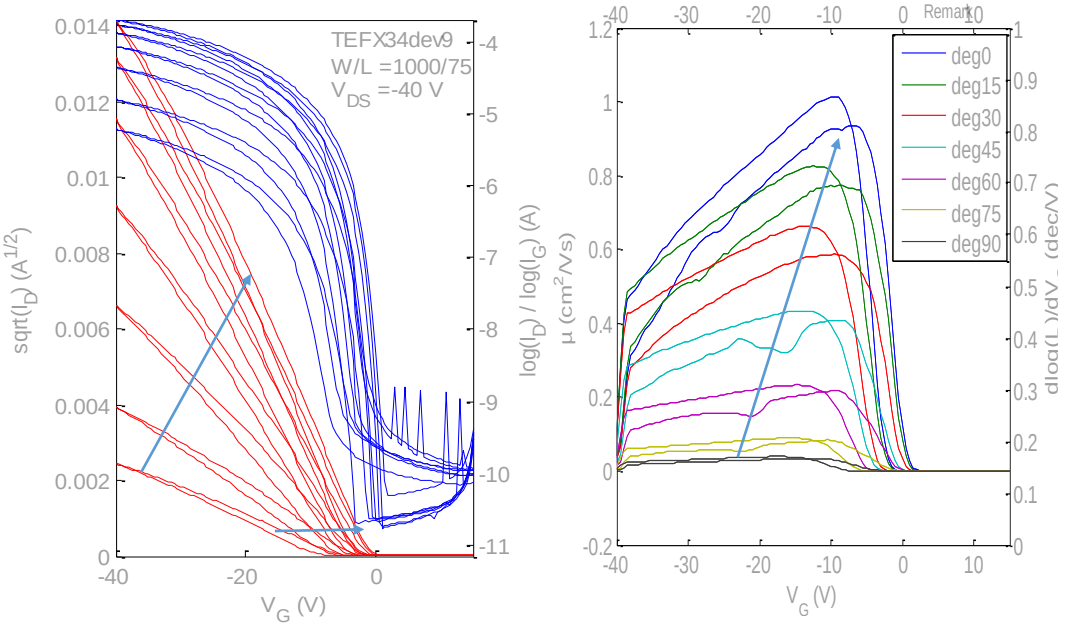

Figure 34.Electrical characteristics of the transistors as a function of channel orientation to PTFE deposition direction with the deposition rate of 1.0 Å/s and substrate temperature of 80°C with the channel width and channel length of 1000 and 75 µm. Left: Transfer curve, Right: Field effect mobility

As it is shown, strong anisotropy property of the sample can be seen. Indeed arrows are shown the progress in the performance of devices which have less deviation than PTFE deposition direction. The best results have been obtained for the devices with the channel along the PTFE deposition direction.

To have a better understanding of this phenomena, Figure 34. shows schematically the path that charge carriers should pass between the contacts

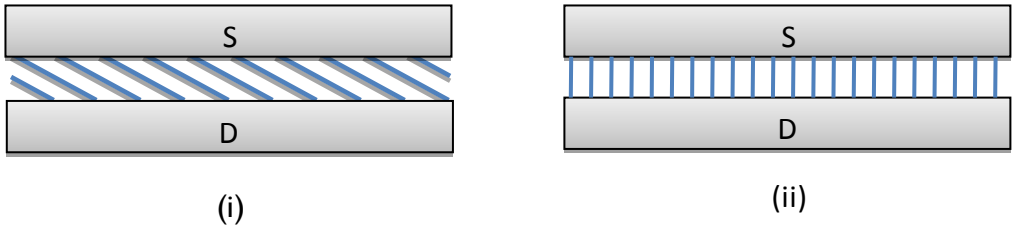

Figure 35.Device channel as a function of PTFE orientation direction. i)perpendicular ii) along the PTFE orientation direction

Indeed image i shows a channel oriented perpendicular to the PTFE orientation direction while in the image ii both channel and PTFE film are elongated in the same orientation.

For transistors with PTFE film, we assume that the charge carriers transport through small scale grooves which connect source and drain contacts through the channel. Since grooves are shorter for channels elongated in the direction of PTFE orientation; therefore charge carriers can travel easier with less dissipation in comparison with channels with some deviation from the PTFE direction which results to have higher field effect mobilities for these devices.

5. SUMMARY AND CONCLUSION

The objective of this thesis was to improve the orientation growth of organic semiconductor molecules (C_{10}-DNTT and DNTT). The thesis is divided to 2 parts. In the first part we developed a friction transfer machine in order to transfer an aligned and uniform layer of PTFE on the substrate. On the second part, organic semiconductor molecules were grown on the oriented PTFE film.

Oriented PTFE film can serve as a template to help oriented growth of organic semiconductor molecules. Since higher ordering delivers better performance, higher mobilities for devices using PTFE were expected. For transistors using DNTT, a systematic progress in the performance of transistor was observed. Indeed PTFE can successfully align the DNTT molecules. The growth of C_{10}-DNTT on the PTFE layer was not that promising though. In this case, samples with PTFE are systematically better for short channels. The possible reason could stem in charge carrier transport since there is a guess that charge carrier does not easily go around low density defects.

As the next stage for improving the morphology of grown organic molecules, we manipulated the deposition rate and substrate temperature. Indeed we studied the correlation between deposition condition and thin film morphology and we found out that deposition condition can directly affect the growth of organic molecules.

We also studied the electrical characteristics as a function of PTFE orientation direction. Devices with different orientation were measured and the best performance obtained for OFETs with the channels elongated to the PTFE orientation direction.

The surface treatment and deposition condition of this study can be also developed for other organic semiconductors such as pentacene.

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APPENDIX A

The name IMEC is an acronym meaning Interuniversity Micro-Electronic Center. The company's headquarter is situated in Leuven, in Belgium, near to Brussels. IMEC has offices in different parts of the world such as USA, China, Taiwan, Netherlands and others.

This company has been founded in 1984 after the idea of the Flemish Government to enhance the microelectronic industry in Flanders. At first, IMEC was a small center with only 70 persons, housed by the Katholiek Universiteit of Leuven, led by Roger Van Overstraeten, an university professor.

After 30 years, IMEC has become an independent research center that employs more than 2000 persons with a large number of industrial residents and guest researchers. IMEC has a large number of technology partners such as Intel, Samsung, NVIDIA, NXP Semiconductors and others.
IMEC campus is about 80.000 m^2 of office spaces, laboratories, training facilities, technical support rooms and cleanrooms. IMEC's campus contains two state of the art cleanrooms that are semi-industrial:

- 200 mm cleanroom for development in demand and prototyping.
- 300 mm cleanroom that is 450 mm ready: this cleanroom is more for R&D programs and for sub 10 nm treatments.

Figure 36.IMEC Campus

IMEC is still evolving by expanding their premises and constructing new labs or offices. For example, this year, IMEC's new office tower has been inaugurated: this tower counts 16 floors with office space for 450 people and also new light laboratories. In 2011, IMEC's revenue was about 300 million Euros.

IMEC explores a wide scope of research domains such as sub 22nm CMOS, Solar cells, Wireless Communication, organic electronics, Neuroelectronic, sensor for industrial application and others.

For my part, I have worked in the Large Area Electronics (LAE) department. The LAE department develops thin-film electronic circuits on flexible foils for applications such as RFIDs, flexible sensors arrays, and flexible OLED displays. The work in LAE is mostly performed in association with the Holst Centre (which is an associated R&D center founded in part by IMEC).

More precisely, I have worked in the MNP (Modeling aNd Physics) group of the LAE (Large Area Electronic) department. This group works principally on Organic based Thin Film Transistors (OTFT) and actually on P-type transistors. This team is composed of five persons: 1 post-doctoral worker, two PhD workers, one senior searcher, one R&D developer and one external worker. My position in this team is the intern research assistant. At the beginning of my stay, my supervisor showed me the state of the art in the group and proposed me some possible research tracks.

My work was divided into 2 parts. In the first part I worked on finding the optimal condition for transferring PTFE thin film on the substrate and for the second stage I was supposed to grow organic semiconductor molecules on PTFE layer and making thin film transistors.