TAMPERE UNIVERSITY OF TECHNOLOGY

MARKUS ALLÉN

NONLINEAR DISTORTION STUDIES IN WIDEBAND ANALOG-TO-DIGITAL CONVERTERS

Master of Science Thesis

Examiners: Professor Mikko Valkama, Professor Markku Renfors, M.Sc. Vesa Lehtinen
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ABSTRACT

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This thesis discusses nonlinearities of analog-to-digital converters (ADCs) and their mitigation using digital signal processing (DSP). Particularly wideband radio receivers are considered here including, e.g., the emerging cognitive radio applications. In this kind of receivers, a single ADC converts a mixture of signals at different frequency bands to digital domain simultaneously. Different signals may have considerably different power levels and hence the overall dynamic range can be very large (even 50–60 dB). Therefore, even the smallest ADC nonlinearities can produce considerable amount of nonlinear distortion, which may cause a strong signal to block significantly weaker signal bands.

One concrete source of nonlinear distortion is waveform clipping due to improper signal conditioning in the input of an ADC. In the thesis, a mathematical model for this phenomenon is derived through Fourier analysis and is then used as a basis for an adaptive interference cancellation (AIC) method. This is a general method for reducing nonlinear distortion and besides clipping it can be used, e.g., to compensate integral nonlinearity (INL) originating from unintentional deviations of the quantization levels. Additionally, an interpolation method is proposed in this thesis to restore clipped waveforms and hence reduce nonlinear distortion.

Through several computer simulations and corresponding laboratory radio signal measurements, the performance of the proposed post-processing methods is illustrated. It can be seen from the results that the methods are able to reduce nonlinear distortion from a weak signal band in a considerable manner when there are strong blocking signals in the neighboring channels. According to the results, the AIC method would be a highly recommendable post-processing technique for modern radio receivers due to its general ability to reduce nonlinear distortion regardless of its source.

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Tässä työssä käsitellään analogia-digitaalimuuntimien (AD-muuntimien) epälineaarisuuksia ja niiden lieventämistä digitaalisen signaalinkäsittelyn (DSP) avulla. Tätä on tarkasteltu erityisesti laajakaistaisten radiovastaanottimien näkökulmasta, joka käsittää mm. tulevat kognitiiviseen radioon liittyvät sovellukset. Tällaisissa vastaanottimissa yksittäinen AD-muunnin muuntaa samanaikaisesti useita eri taajuuskaistoilla olevia signaaleita digitaaliseen muotoon, jolloin yhteenlaskettu dynaaminen alue voi olla hyvin suuri (jopa 50–60 dB). Tämän takia AD-muuntimen pienimmätkin epälineaarisuudet voivat aiheuttaa huomattavasti epälineaarista vääristymää, minkä vuoksi voimakas signaali saattaa häiriöllään peittää muilla taajuuskaistoilla olevia selkeästi heikompia signaaleja.

Eräs konkreettinen epälineaarisen vääristymän aiheuttaja on aaltomuodon leikkaantuminen AD-muuntimen sisäänmenossa jännitealueen ylittymisen vuoksi. Tässä työssä johdetaan matemaattinen malli kyseiselle ilmiölle Fourier-analyysin avulla ja käytetään sitä lähtökohtana adaptiiviselle häiriönpoistomenetelmälle (AIC-menetelmä). Se on yleisluonteinen menetelmä epälineaarisen vääristymän vähentämiseksi, ja leikkaantumisen lisäksi sitä voidaan käyttää esimerkiksi kompensoimaan integraalista epälineaarisuutta (INL), joka on peräisin kvantisointitasojen tahattomista poikkeamista. Lisäksi tässä työssä esitellään interpolointimenetelmä leikkaantuneen aaltomuodon ehostamiseen siten, että epälineaarinen häiriö vähenee.

Esiteltyjen jälkikäsittelymenetelmien suorituskykyä analysoidaan ja havainnollistetaan useilla tietokonesimulaatiolla sekä niitä vastaavilla radiosignaalien laboratoriomittauksilla. Tuloksista voidaan nähdä, että nämä menetelmät kykenevät poistamaan huomattavasti epälineaarista vääristymää heikolta signaalikaistalta silloin, kun naapurikaistoilla on voimakkaita häiriösignaaleja. Tulosten perusteella AIC-menetelmä olisi erittäin suositeltava jälkikäsittelytekniikka moderneihin radiovastaanottimiin, koska se pystyy yleisesti vähentämään epälineaarista vääristymää riippumatta häiriön alkuperästä.

PREFACE

The research behind this thesis was conducted during the years 2008 and 2009 at the Department of Communications Engineering at Tampere University of Technology (TUT) under the project entitled “Dirty-RF: Advanced Techniques for RF Impairment Mitigation in Future Wireless Radio Systems”. The research was supported by the Academy of Finland, the Finnish Funding Agency for Technology and Innovation (Tekes) and the Technology Industries of Finland Centennial Foundation.

First I would like to thank my supervisor Professor Mikko Valkama not only for offering me a topic for the thesis but also for providing guidance and a very educative job as a research assistant, which has given me a good starting point for my career. I would also like to express my gratitude to other examiners of my thesis Professor Markku Renfors and M.Sc. Vesa lehtinen for all of their efforts. Special thanks go to my co-worker Jaakko Marttila, who started examining the wonderful world of analog-to-digital converters with me from the beginning and has ever since shared his knowledge to advance my research. In addition, I would like to thank all the co-workers and the staff of our department for creating a pleasurable working environment, especially my “nearest neighbors” M.Sc. Jukka Talvitie, M.Sc. Ville Syrjälä and M.Sc. Toni Levanen for giving valuable tips and sharing their thoughts with me.

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CONTENTS

ABBREVIATIONS

ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
AIC	Adaptive Interference Cancellation
BER	Bit Error Rate
DAC	Digital-to-Analog Converter
DNL	Differential Nonlinearity
DSP	Digital Signal Processing
FIR	Finite Impulse Response
FS	Full Scale
HCF	High Code Frequency
IF	Intermediate Frequency
INL	Integral Nonlinearity
IQ	In-phase/Quadrature
LCF	Low Code Frequency
LMS	Least Mean Squares
LNA	Low-Noise Amplifier
LO	Local Oscillator
LSB	Least Significant Bit
LUT	Look-Up Table
MSB	Most Significant Bit
Msps	MegaSamples Per Second
OFDM	Orthogonal Frequency Division Multiplexing
OSF	Oversampling Factor
PAPR	Peak-to-Average Power Ratio
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
rms	Root Mean Square
SAR	Successive Approximation Register
SDR	Software Defined Radio
SNDR	Signal-to-Noise-and-Distortion Ratio
SQNR	Signal-to-Quantization-Noise Ratio
WCDMA	Wideband Code Division Multiple Access

SYMBOLS

$\varepsilon(n)$	Compensation value retrieved from a LUT
$\varepsilon[k]$	Error between the ideal and the actual value of $T[k]$
$\theta_c(t)$	Argument for the carrier defined as $\omega_c t + \phi(t)$
$\phi(t)$	Phase of the carrier
ω_c	Angular frequency of the carrier
a	Polyphase branch index
$A(t)$	Signal envelope
$a_m(t)$	Time-variant Fourier coefficients
b	Number of bits in a quantizer
c	Polynomial weight
C	Crest factor in linear scale
CF	Crest factor in logarithmic scale (dB)
f_B	Useful signal bandwidth
f_s	Sampling frequency
G	Static gain of an ADC
$h(n)$	Impulse response of an interpolation filter
$INL_{HCF}(T[k])$	HCF part of INL for transition $T[k]$
$INL_{LCF}(T[k])$	LCF part of INL for transition $T[k]$
$INL_{noise}(T[k])$	Noise part of INL for transition $T[k]$
L	Oversampling factor
m	Index for Fourier series
M	Order of sigma-delta noise shaping
n	Sample index
N	Signal length
p	Number of conversion stages in a subranging ADC
P_{avg}	Average power of the signal
Q	Ideal code width
$r_I(t)$	Auxiliary variable defined as $\arccos\frac{V_0}{A(t)}$
$r_Q(t)$	Auxiliary variable defined as $\arcsin\frac{V_0}{A(t)}$
$\tilde{s}$	Input signal s after nonlinearity $g(\cdot)$
$\hat{s}(n)$	Compensated output signal

$\hat{s}'(n)$	Digital estimate of the derivative of the input signal $s(t)$
$s(t)$	Continuous-time input signal
$\overline{s}_f$	Mean value of $s_f(n)$
$s_f(n)$	Ideal test signal filtered to contain only the frequency band around 3 MHz
t	Time variable
$T[k]$	Actual input voltage corresponding to kth transition
T_1	Ideal value of $T[1]$
$T_{ideal}[k]$	Ideal value for kth transition
V_0	Clipping level
$v_{cl}(t)$	zero-symmetric hard-clipped signal
$v_{in}(t)$	continuous-time input signal
$V_{in(rms)}$	Rms value of the input signal
$v_{\mathrm{lim}}(t)$	Clipped output signal (limiter)
V_{os}	Output offset of an ADC
$v_{out}(t)$	Clipped output signal (hard clipping)
V_{pp}	Peak-to-peak input voltage
$V_{Q(rms)}$	Rms value of the quantization error
$W[k]$	Actual kth code width
$y(n)$	Output signal of an ADC
$\hat{y}(n)$	Estimate of the ADC output given by a black-box model
$\overline{y}_f$	Mean value of $y_f(n)$
$y_f(n)$	Distorted test signal filtered to contain only the frequency band around 3 MHz

1. INTRODUCTION

All modern mobile communication devices deploy digital transmission as well as digital signal processing and thus analog-to-digital conversion is an inevitable part in their radio receivers. There has been remarkable increase in the performance of the radio receivers in recent years. Unfortunately the development of analog-to-digital converters (ADCs) has not been as rapid [24], [41]. Therefore, the ADC has become a bottle neck for the whole receiver. This can be explained with one of the modern trends where the ADC is located as close to the antenna as possible in the receiver chain. In this way, the smallest possible number of analog components in the receiver can be achieved. Cutting down the amount of the analog parts is desired in order to reduce, for example, power consumption and required chip area of the receiver. Moreover, selectivity of the receiver is easier, more flexible and cheaper to implement in digital domain. In that case, receiver doesn't necessarily have to have several parallel receiver front-ends for different wireless standards. [19], [26]

The ultimate goal in receiver design would be a so-called software defined radio (SDR). It is a re-configurable receiver where all or most of the selectivity is implemented with digital signal processing (DSP). In extreme case, the received signal is digitized straight from the radio frequency (RF). Another possibility is a direct conversion principle, where the received signal is downconverted from RF to baseband and then, after an analog-to-digital conversion, the channel selection is performed. [31] In both cases, a wideband signal, which may consist of several separate frequency bands, is digitized as a whole. A wideband receiver front-end enables the cognitive radio concept, which uses spectrum sensing in order to exploit any feasible part of the spectrum [10]. This is the main case which is considered throughout the thesis. A wideband receiver sets very strict requirements for analog-to-digital converters. In practice it means that high resolution and especially high sampling rate are needed. The requirement for high resolution is stemming from the large dynamics of modern communications signals and also from the need to detect low-power frequency bands when there are considerably

stronger frequency bands in the same signal. This is illustrated in Figure 1.1. The dynamic range can be several tens of dB's. As a matter of fact, the sampling rate is a more limiting aspect than the resolution. When selectivity is implemented in digital domain, the ADC usually has to digitize wider frequency band and hence higher sampling rate is required. The trend towards wider bandwidths in the receivers can be seen clearly by studying the development of ADC technologies. After the year 1995 the maximum resolution of commercial ADCs hasn't increased but the sampling rate has been developing very fast [24]. In addition, the power consumption is a very critical aspect in mobile devices. As a general rule, high-resolution and high-speed ADCs tend to have very significant power dissipation.

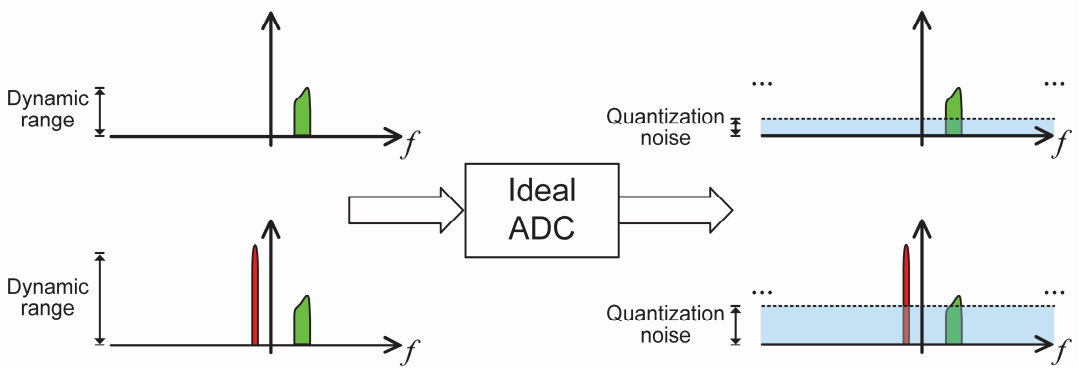

Figure 1.1. *Spectrum illustrations of the upper part show how an ideal ADC induces quantization noise to the signal due to finite resolution. In the lower part, the dynamic range is increased due to a strong blocking signal and hence the weaker signal is more affected by the quantization noise when the same ideal ADC is used.*

Especially when considering wideband receivers, it is important to be aware of the fact that real-world ADCs are not ideal. There are many different non-idealities that can distort the received signal. For example, due to nonlinear behavior of the ADC a strong signal can severely interfere with weaker signals on different frequency bands [27]. To be exact, the interference is mainly intermodulation distortion of the strong signal. This is illustrated in Figure 1.2. Fortunately, the technical development has noticeably increased the available computational resources. This has created a possibility to add more DSP to the receivers and thus digitally enhance the signal that is distorted by the ADC. Therefore, it is possible to create better receivers by exploiting DSP than it would be otherwise with the current hardware technology. On the other hand, if the additional performance is not needed, the DSP enhancement is still useful. That is because more nonlinear and therefore cheaper or less power-consuming ADCs can be used to provide the same performance as a whole.

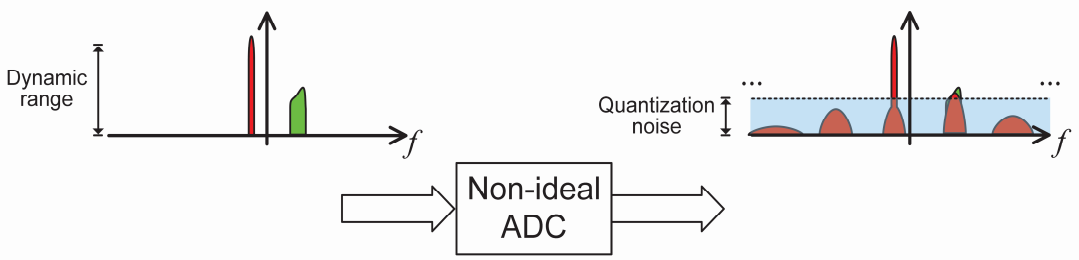

Figure 1.2. *Spectral illustrations from the input and output of a non-ideal ADC. The weak signal band is heavily affected by the nonlinear distortion stemming from the strong blocker signal.*

The nonlinearities in analog-to-digital converters are originating from several different sources and thus behave differently [25], [27]. The first goal of the thesis is to discuss what kind of nonlinearities there are in the ADCs and how they affect the received signal. Especially the case of wideband signal with several separate frequency bands is considered here. Such a survey gives a good starting point for developing new DSP methods for ADC nonlinearity compensation. The thesis concentrates specifically on nonlinearities in analog-to-digital conversion. Other non-idealities, such as sampling jitter, are omitted from the thesis, because it is a rather independent topic which is already widely covered in the existing literature.

One interesting source of nonlinear distortion, which is covered in this thesis among others, is waveform clipping in the input of the ADC. The phenomenon is stemming from the improper input signal conditioning due to the rapidly changing signal dynamics. This is a potential situation in the wideband receivers where different signals may have considerably different power levels. The amount of literature about the ADC clipping, especially in the radio receivers, is rather limited. This is one strong motive to study the clipping topic in more detail in this thesis.

There is a great need for ADC nonlinearity compensation methods not only due to emerging wideband radio receivers in mobile devices but also because most of the existing methods proposed in the literature have been designed for laboratory equipment. These methods may require, e.g., a considerable amount of memory or offline calibration and thus are not suitable for real-time mobile devices with limited resources. The second goal of the thesis is to cover the most used methods for nonlinearity compensation in ADCs which are proposed in the literature. After that, the goal is to develop and propose new nonlinearity compensation methods which are not, until this thesis, covered in the literature in the context of ADCs.

In the research for this thesis, the primary tool for developing new ADC nonlinearity compensation methods and confirming their performance is the well-known software called MATLAB by The MathWorks Inc. Furthermore, the developed algorithms are tested, to the extent possible, in a laboratory environment with a real commercial analog-to-digital converter [5]. In this way, it can be verified that the ADC model in the computer simulations has been accurate enough to model the nonlinear behavior. The technical contribution of this thesis has been also published in [1]–[3].

The structure of the thesis is organized as follows. Chapter 2 gives an overview of quantization and analog-to-digital converters based on the latest scientific literature. It goes through typical high-speed ADC architectures that can be used in radio receivers. After that, DSP-based compensation methods for ADC nonlinearities are discussed. It is worth mentioning that even though sigma-delta ADCs [35] are a potential option for modern radio receivers, their working principle and thus their nonlinearities are significantly different from all the other ADC architectures. Nonlinearity compensation of the sigma-delta ADCs deserves its own research and is therefore omitted from this thesis. Chapter 3 continues with the overview of the radio receiver architectures. It discusses especially how the receiver architecture choice affects ADC requirements. Some examples of the modern wireless standard specifications are considered here. Chapter 4 starts with proposing a mathematical model for a clipped signal. The model was derived to achieve better understanding of the clipping phenomenon and apparently it has not been presented in the literature until now. Next, Chapter 4 proposes two approaches for compensating ADC nonlinearities. Concrete examples of their performance are given in Chapter 5. Both computer simulations and laboratory measurements are considered here. Finally, Chapter 6 gathers everything together by drawing conclusions. Appendix gives details on deriving the mathematical clipping model introduced in Chapter 4.

2. ANALOG-TO-DIGITAL CONVERTERS AND NONLINEARITIES

Analog-to-digital converter interprets analog electrical quantities to digital code words. In real-life ADCs, there are several kinds of non-idealities that interfere with the conversion process. Modern communication systems have tight requirements for the ADCs in receivers, e.g. high sampling rate and resolution, and thus the non-idealities may have a significant role. In general, digital signal processing can be used to compensate these non-idealities after the conversion.

First, in Section 2.1 very basics of ideal quantization are discussed followed by the most essential non-idealities described in Section 2.2. Because different ADC architectures have different kinds of impact to digitalization process, the most common high-speed architectures are described in Section 2.3. After that, an introduction to digital compensation methods is given in Section 2.4. Finally, in Section 2.5, one special topic called clipping is covered. Although the so-called sigma-delta ADC architecture is presented in Subsection 2.3.4 due to its attractive features for modern radio receivers, its nonlinearities and their compensation are omitted from this thesis because the sigma-delta architecture differs considerably from all the other ADCs and would require a thesis of its own.

2.1. Quantization Process

Quantization implies presenting large number of values or even a continuous range with limited number of discrete code words. Therefore, input values are rounded to nearest corresponding output values. This means that quantization induces information loss and even in the ideal case it is a nonlinear operation. A coding method in a quantizer is related to the input range of an ADC. If the input range only consists of positive voltages, the quantizer is said to be unipolar. Similarly, an input range with both positive and negative voltages corresponds to a bipolar quantizer. [7]

Figure 2.1 illustrates typical transfer function for an ideal unipolar 3-bit ADC. The appropriate input range is marked between 0 and full scale (FS). First quantization level (ideally) starts from 0 V and its width is 0.5 LSB (least significant bit). The width of the last (highest) quantization level is 1.5 LSB. This is because there is -0.5 LSB offset in the positions of all the codeword transitions as is highlighted with a light blue region in Figure 2.1. The offset is intentional and desirable since the potential quantization error is then between -0.5 LSB and +0.5 LSB. Blue dots in Figure 2.1 illustrate locations where the quantization error is zero. Quantization error would be from 0 LSB to 1 LSB without the offset. [7] The lowest and highest quantization level in Figure 2.1 are drawn to continue outside the full scale range to emphasize the ADC behavior outside the intended scale. This phenomenon is called clipping and is discussed in more detail in Section 2.5.

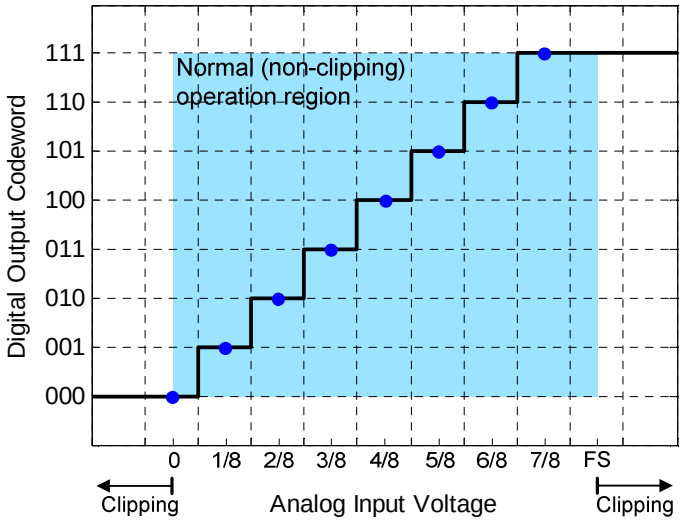

Figure 2.1. *Transfer function of an ideal unipolar 3-bit analog-to-digital converter.*

Quantization thresholds do not have to be uniformly spaced. For example, in some applications values near zero can be more important than large values. While keeping the number of bits constant, resolution for small values can be increased at the expense of accuracy in large values by using non-uniform quantizer. For instance, in logarithmic converters the code width increases logarithmically as a function of input voltage. This kind of approach has been used, e.g., in some communications, instrumentation and hearing aid applications. [16] Somewhat different approach is used in a floating-point ADC. It operates dynamically with respect to the amplitude of the input signal, i.e., code widths change when the dynamics of the input signal change [30].

Information loss as a result of finite word length is called quantization noise. It can be expressed conveniently with signal-to-quantization-noise ratio (SQNR). After ideal quantization, the SQNR in decibels is defined as

$$SQNR = 20\log_{10}\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right), \tag{2.1}$$

where $V_{in(rms)}$ is the root mean square (rms) value of the input signal and $V_{Q(rms)}$ is the rms value of the quantization error. Furthermore, a common assumption is that the quantization noise is white and uniformly distributed between ±0.5 LSB and hence

$$V_{Q(rms)} = \frac{Q}{\sqrt{12}}, \tag{2.2}$$

where Q denotes the width of one LSB, i.e., $Q = \mathrm{FS}/2^b$. The rms value of the input signal can be given with respect to the peak-to-peak input voltage V_{pp} and the crest factor C so that

$$V_{in(rms)} = \frac{V_{pp}}{2C}. \tag{2.3}$$

This follows from the fact that the crest factor is defined as a ratio of the peak amplitude and the rms voltage of the signal. In addition, a possible oversampling gain should be taken into consideration when defining the SQNR. The oversampling gain stems straight from the oversampling factor which, for one, is defined as a ratio of the sampling frequency and the double-sided useful signal bandwidth. When all the above-mentioned details are substituted in Equation (2.1), the SQNR finally becomes

$$SQNR = 6.02b + 4.77 - CF + 10\log_{10}\left(\frac{f_s}{2f_B}\right), \tag{2.4}$$

where b is the number of bits in the quantizer, CF is the crest factor of the input signal in dB's, f_s denotes the sampling frequency and f_B is the useful signal bandwidth. [22] Oversampling can be utilized to spread the quantization noise on a wider band and hence reduce the in-band noise. The out-of-band part of the noise can then be filtered away.

The SQNR equations in the previous paragraph considered white quantization noise. However, there is one special ADC structure that can shape the quantization noise so that most of it is outside the band of interest. It is called a sigma-delta ADC and its op-

erational principle is more carefully discussed in Subsection 2.3.4. By making an assumption that the oversampling factor is significantly larger than one, the SQNR for a sigma-delta ADC with first-order noise shaping can be written as

$$SQNR_{SD,1} = 6.02b + 4.77 - CF - 10\log_{10}\left(\frac{\pi^2}{3}\right) + 30\log_{10}\left(\frac{f_s}{2f_B}\right). \quad (2.5)$$

It can be seen that doubling the oversampling factor increases SQNR by 9 dB when first-order noise shaping is used. As a comparison, Equation (2.4) shows that without noise shaping only 3 dB gain can be achieved by doubling the oversampling factor. If the sigma-delta ADC uses second-order noise shaping, the SQNR becomes

$$SQNR_{SD,2} = 6.02b + 4.77 - CF - 10\log_{10}\left(\frac{\pi^4}{5}\right) + 50\log_{10}\left(\frac{f_s}{2f_B}\right). \quad (2.6)$$

In this case, the SQNR is improved by 15 dB every time the oversampling factor is doubled. In general, for Mth-order noise shaping, the SQNR equation is

$$\begin{aligned} SQNR_{SD,M} = {} & 6.02b + 4.77 - CF - 10\log_{10}\left(\frac{\pi^{2M}}{2M+1}\right) \\ & + (20M + 10)\log_{10}\left(\frac{f_s}{2f_B}\right). \end{aligned} \quad (2.7)$$

Therefore, doubling of the oversampling factor increases the SQNR by $(6M + 3)$ dB. [8], [22]

2.2. Non-Idealities in Quantization

Real-life ADCs have several different kinds of unwanted nonlinearities. Gain and offset errors are significant but their effects are rather trivial to mitigate. Other important nonlinearities are differential nonlinearity (DNL) and integral nonlinearity (INL). Various definitions for these nonlinearities can be found from the literature. The most used ones are presented in following paragraphs.

According to an application note of Maxim Integrated Products Inc. [29], offset error is defined as a constant shift of transfer function from its ideal location. Gain error can be evaluated after the offset error has been corrected. It is defined as a difference between the actual codeword after the last transition and the corresponding ideal one. An example of both offset and gain error in case of a unipolar ADC is illustrated in Fig-

ure 2.2. Ideal and non-ideal transfer functions are presented with solid black and blue lines, respectively. Straight lines are fitted through the starting point and the last transition of transfer functions to make the offset error of -2 LSB and the gain error of 1 LSB more visible. The dashed blue line in Figure 2.2 represents the non-ideal transfer function after correcting the offset error. Occasionally, also a term full-scale error is used in ADC datasheets. It is defined as a sum of offset error and gain error. In Figure 2.2, the full-scale error can be thought as a difference of the actual codeword after the last transition compared to the ideal transfer function. Therefore, in this case the numerical value is -1 LSB. It is also worth noticing that some of the quantization levels may be left unused in unipolar converters because of the offset error.

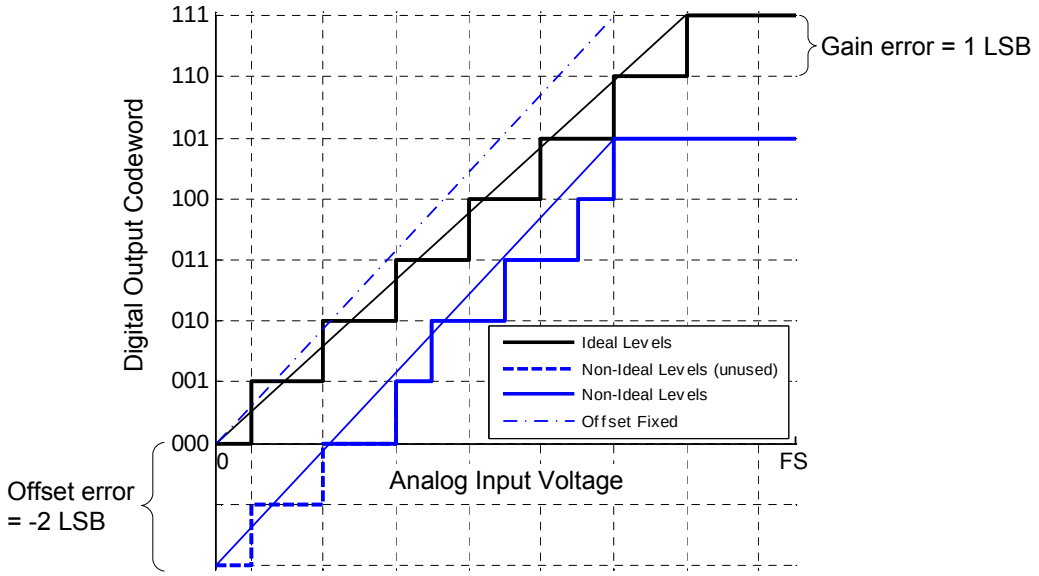

Figure 2.2. *Example of offset and gain errors in an unipolar 3-bit ADC.*

IEEE standard 1241-2000 for analog-to-digital converters [17] introduces another approach for defining offset and gain errors. The transfer function of an ADC can be described with the equation

$$G \times T[k] + V_{os} + \varepsilon[k] = Q \times (k-1) + T_1, \tag{2.8}$$

where G is the gain, $T[k]$ is the actual input value corresponding to kth transition, V_{os} is the output offset, $\varepsilon[k]$ is the residual error of kth transition, Q is the ideal code width and T_1 is the ideal value of $T[1]$. The IEEE standard [17] describes two ways of identifying offset and gain errors based on Equation (2.8). In independently-based method G and V_{os} get values that minimize the mean squared value of $\varepsilon[k]$ over all k. Another

method is called terminal-based, which defines that the offset and the gain are the values which cause the deviations of the first and last codes to be zero. In other words, the offset and the gain are evaluated when $\varepsilon[1] = 0$ and $\varepsilon[2^b - 1] = 0$, where b is the number of bits in quantizer.

INL and DNL errors can be calculated only after correction of offset and gain errors. DNL is the relative difference between the actual and ideal code widths compared to the ideal code width. It is defined as

$$DNL[k] = \frac{W[k] - Q}{Q} \tag{2.9}$$

in which $W[k]$ is the kth actual code width [17]. In a similar manner, INL is the difference between the actual and the ideal code transition threshold. Another way of interpreting the INL is thinking it as a cumulative sum of the DNL. According to [17], INL can be defined as

$$INL[k] = 100\% \times \frac{T[k] - T_{ideal}[k]}{2^b \times Q}, \tag{2.10}$$

where $T_{ideal}[k]$ is the ideal value for the kth transition. It should be taken into account that Equation (2.9) gives DNL as a multiple of LSB, but INL in (2.10) is given in relation to the full scale. In some cases, a more convenient equation is

$$INL[k] = \frac{T[k] - T_{ideal}[k]}{Q}, \tag{2.11}$$

which gives INL as a multiple of LSB. For instance, ADC datasheets typically use LSB unit. In addition to that, usually when DNL or INL is expressed as a single value it is the maximum of (2.9) or (2.11) over all k.

An example of DNL and INL errors is presented in Figure 2.3 so that more concrete conception can be attained. The dashed gray line indicates the ideal transfer function and the black line represents an example of non-ideal transfer function for a 3-bit unipolar ADC. The corresponding DNL and INL errors have been marked in Figure 2.3. There is an example of missing code, which means a situation where the DNL error is less than or equal to -1 LSB and therefore two quantization levels are fully overlapped. In case of Figure 2.3, the codeword *101* doesn't correspond to any input voltage. In some situations the errors can make the transfer function to be non-monotonic (not illu-

strated in Figure 2.3). It means that there are two separate ranges of input voltages that correspond to the same digital output codeword. The non-monotonicity is not possible in every ADC architecture, but it can happen, for instance, in pipelined ADCs. [7]

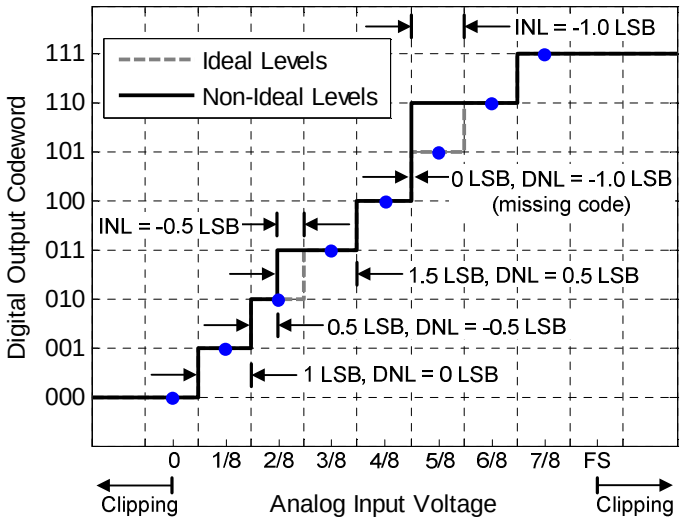

Figure 2.3. *Example of DNL and INL errors in a 3-bit ADC.*

2.3. High-Speed ADC Architectures

This section provides a small overview to different kinds of high-speed ADC architectures which can be classified to flash, subranging, successive approximation and sigma-delta ADCs. The operational principle of every architecture is described and also some examples of their practical applications and present performance are discussed. It is worth noticing that the sigma-delta ADC principle differs significantly from all the other aforementioned architectures not only by its noise shaping properties but also by its non-idealities.

Comparator is an essential building block in any ADC architecture. One or more of them can be found from every ADC structure described in the following. Basically, the comparator can be considered to be a 1-bit ADC. It outputs binary values by comparing the input signal voltage level to a constant threshold level. [7]

2.3.1. Flash ADC

A flash ADC is also called a parallel ADC which clearly describes its data conversion principle. It consists of 2^b-1 comparators as shown in Figure 2.4. The comparators are biased to correspond to the wanted quantization levels. The input signal after a sample-and-hold circuit is applied to all comparators at the same time. Therefore, the conver-

sion takes only one cycle and high-speed conversion can be achieved. Parallel comparators as a whole produce a thermometric representation and for this reason the level encoder is used to construct a more practical *b*-bit digital output. [13]

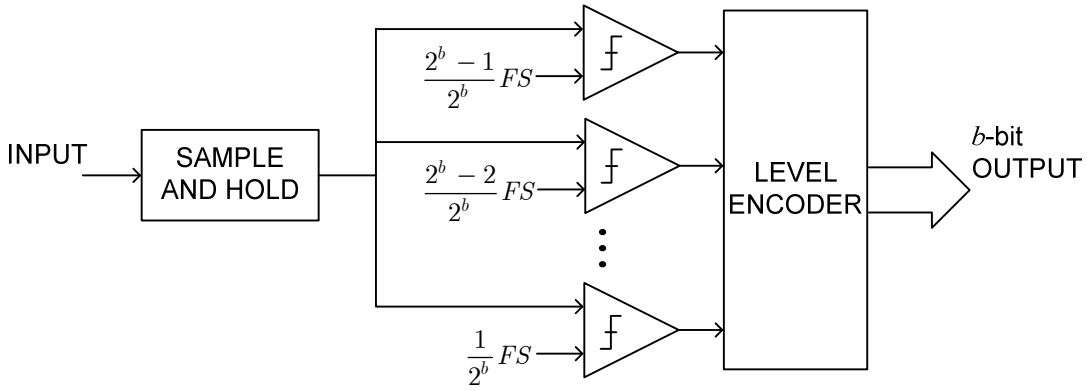

Figure 2.4. *Operational principle of flash ADC with b-bit output.*

As mentioned already, flash ADCs are suitable for high-speed applications. However, due to practical limitations the resolution can't be very high. It is worth noticing that the number of comparators increases exponentially as a function of bits used in quantization. This is directly proportional to the required silicon area and, especially, the power consumption. The high resolution also refers to very small differences between the reference voltages of the comparators. In practice, very small differences are challenging to achieve with a high enough accuracy. [27] The above-mentioned matters are the reason for which flash ADCs are mainly used in high-speed oscilloscopes and RF test instruments. Modern flash ADCs can reach sampling rates of even several gigasamples per second but the resolution isn't usually more than 8 bits. [33]

2.3.2. Subranging ADC

A subranging ADC was originally developed to overcome the limitations of the flash converters. It is composed of several consecutive low-resolution flash or other type ADCs. A simple two-stage subranging ADC is illustrated in Figure 2.5. After the sample-and-hold process, a coarse conversion is done by the b_1-bit ADC. This results in the most significant bits (MSB) of the final output. Then, the bits are converted back to an analog signal by the b_1-bit DAC and subtracted from the original input signal. The residue is amplified by the amplifier with gain G to precisely cover the input range of the b_2-bit ADC. The latter ADC provides the LSBs of the input signal which are joined together with MSBs in the output register. Hence, the final output has a word length of

b_1+b_2 bits. [7] A little bit modified version of subranging ADC is called pipelined ADC. It consists of identical consecutive stages where every stage is independent, containing a sample-and-hold circuit, an ADC, a DAC, an adder and an amplifier.

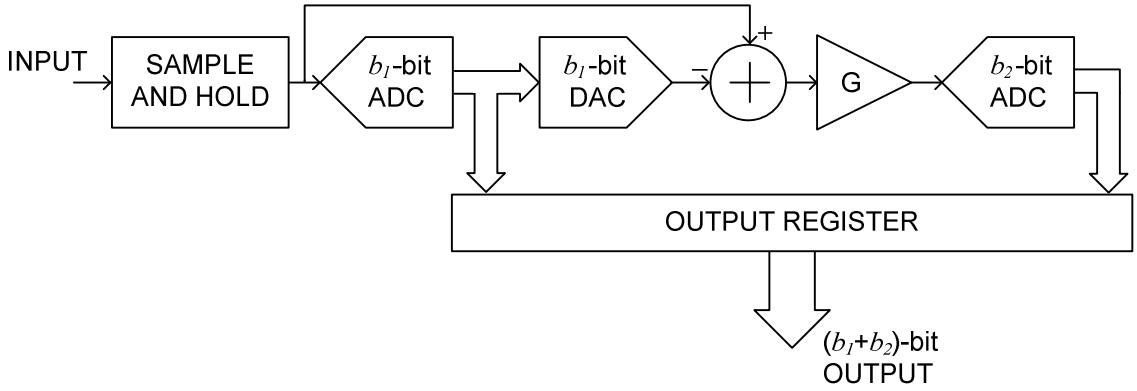

Figure 2.5. *Operational principle of two-stage (b_1+b_2)-bit subranging ADC.*

Compared to the flash ADC, the subranging architecture has an ability to provide high-resolution output with low-resolution converters. Therefore, the number of comparators is decreased to $p \times (2^b - 1)$, where p is the number of the conversion stages. The drawback is that the total conversion time is directly proportional to p. [13] One challenging problem in real-life subranging ADCs is the proper scaling of the residue signal. If the signal is not accurately scaled to the full scale of the subsequent ADC, a missing code situation may appear as described in Section 2.2. This is usually avoided by increasing the number of bits in the converter for internal use so that the final output resolution does not increase. [7]

Subranging ADCs can provide low power consumption and high resolution compared to flash ADCs and still being able to achieve rather high conversion speed. Hence, these converters are typically used in RF test equipment, lower speed digitizing oscilloscopes and high-end PC data acquisition systems. [33] In addition to that, subranging ADCs have their place in consumer electronics and communications. Intermediate frequency (IF) sampling, software radio, base stations and set-top boxes are good examples of the communications applications in question. Nowadays sampling rates of subranging ADCs can be up to slightly over 100 Msps (megasamples per second) and the resolution can be up to 14 bits. [23]

2.3.3. Successive Approximation ADC

A successive approximation ADC can perform high resolution analog-to-digital conversion using only one comparator. This can be achieved by exploiting the information about previously determined bits when making the decision of the next significant bit. The operation principle of the successive approximation ADC is partially similar to the subranging technique but it processes iteratively one output bit per conversion cycle. If the dynamic range of the ADC is from *0* to *FS*, the conversion process begins with determining whether the input signal is above or below *FS/2*. This corresponds to MSB of the final output codeword. After that, the input signal is compared with the threshold level of *FS/4*, if the input signal was below *FS/2*. In case where the input signal is above *FS/2*, it is compared with *3FS/4*. This procedure is continued in a similar manner until the desired bit resolution is accomplished. [27] In other words, during the conversion process the (already) quantized bits define the remaining possible value range. Then on the next conversion cycle it is determined, whether the input signal level belongs to the upper or lower half of the possible value range.

In practice, the successive approximation algorithm can be implemented as shown in Figure 2.6. The sample-and-hold circuit takes a sample from the input signal and holds it steady for comparator until all the conversion cycles for the current sample have passed. Threshold level of the comparator is varied by the DAC which is controlled with successive approximation register (SAR). In the initial state, SAR is set to zero but MSB to one. Then it is compared with the input signal and the output of the comparator is stored as the MSB of the SAR. On the next cycle, second most significant bit of the SAR is set to *1*, compared with the input signal and replaced with the output of the comparator. This continues until the target bit precision *b* is achieved. For the next input sample, the SAR is reset to the initial state. [27]

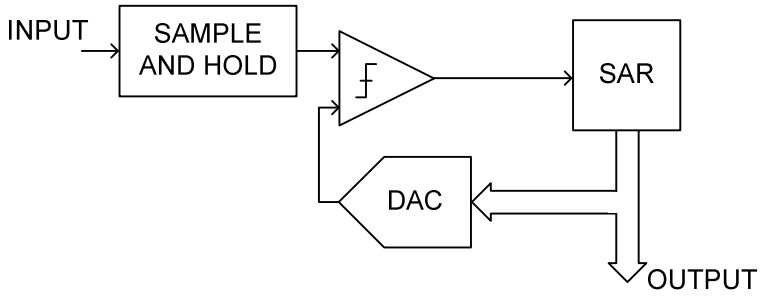

Figure 2.6. *Operational principle of successive approximation ADC.*

The conversion process in the successive approximation ADC is rather slow due to minimum of *b* conversion cycles per sample. In real-life implementations, one problem is the inaccuracy of the DAC. That can lead to a wrong decision in the comparator and, what is more, the error will propagate along all the conversion cycles. In the literature some error correction algorithms are proposed, however these are prone to increase the number of required conversion cycles. [27] Nonetheless, high resolution (up to 16 bits) can be achieved and modern successive approximation ADCs can have sampling rate of a few Msps. Successive approximation ADCs are cheaper and require less power than flash and subranging ADCs. Converters based on SAR are usually used in measurement products such as PC data acquisition systems. [33]

2.3.4. Sigma-Delta ADC

Sigma-delta converters work with high oversampling ratios and therefore even only a 1-bit analog-to-digital conversion combined with digital filtering can eventually provide a very high resolution. However, the fundamental trade-off in the sigma-delta method is that the high resolution achieved with the high oversampling ratio means low final sampling rate. The operational principle of the simplest sigma-delta ADC structure is illustrated in Figure 2.7.

The (oversampled) analog input signal is fed through an integrator to a comparator. After that, the output of the comparator is converted back to the analog domain in a feedback loop and then subtracted from the next input value before the integrator. This structure, which includes the integrator, the comparator and the DAC, is in general called a sigma-delta modulator. The final digital output signal of the sigma-delta ADC is formed by applying proper digital filtering to the output of the comparator and then downsampling it with the same factor as the input signal was oversampled. The integrator is also called a loop filter because it serves as the filter of the feedback loop shaping the quantization noise so that there is less noise at low frequencies than in high frequencies. Therefore the digitized signal is then less affected by the quantization noise because it can be mostly filtered out with a digital filter. [7] The noise shaping property is the fundamental reason for the whole sigma-delta structure and thus makes it distinct from all the other ADC architectures.

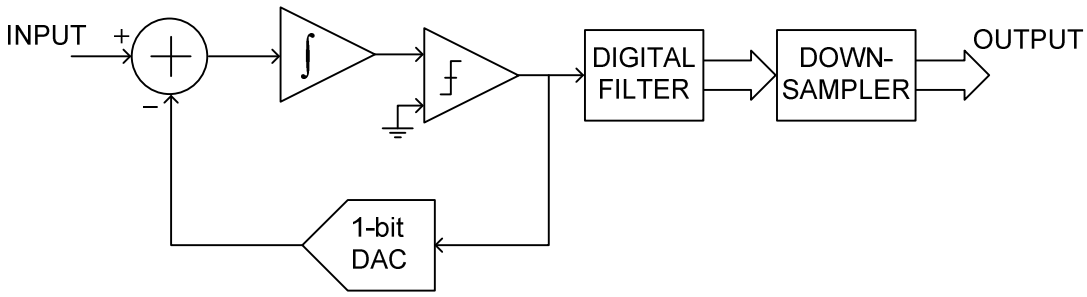

Figure 2.7. *Operational principle of 1-bit low-pass sigma-delta ADC.*

There are many improved versions from the basic sigma-delta ADC structure which provide better performance or other desired properties. For example, using a higher-order loop filter helps reducing the quantization noise even more from the wanted signal band and hence increasing the (effective) resolution of the ADC. The higher-order loop filter is implemented by increasing the number of integrators and feedback loops. In practice, the achievable resolution of the higher-order implementation will be limited due to stability issues. These issues can be relieved with a so-called multistage structure which means using several sigma-delta modulators in a cascade. Another way to increase the resolution is using a multi-bit quantizer instead of a comparator and correspondingly a multi-bit DAC is required in the feedback loop. The multi-bit implementation has a drawback that the multi-bit DACs tend to be rather nonlinear. This creates distortion which is not shaped in the loop and hence it is directly visible at the final output. [35]

Until now this subsection has only considered real low-pass sigma-delta ADCs which can be used for baseband signals. The sigma-delta principle is also applicable for band-pass signals. Practically this means modifying the transfer function of the loop filter so that it will push the quantization noise away from the band of interest towards higher frequencies as well as towards DC. When considering the digitalization of an in-phase/quadrature (IQ) signal with a sigma-delta ADC, there are essentially two options. First one is using two converters separately in parallel whereas another option is to use a so-called quadrature sigma-delta ADC, which exploits a loop filter with complex coefficients. Practically, it means that the noise shaping doesn’t have to be symmetric and hence it can be more efficient. [35]

There is still one important structural aspect mainly related to the loop filter. Most of the sigma-delta ADCs are nowadays using discrete-time loop filters implemented with switched capacitors. These loop filters have good accuracy and linearity. The

switched-capacitor circuit structure is also independent of the clock rate and hence it is easy to design a discrete-time sigma-delta ADC to use various sampling rates. Unfortunately, the maximum signal bandwidth is limited by the finite settling time of the circuit. An increasingly popular solution is to use continuous-time loop filters. This way the sampling of the signal can be postponed to after the loop filter, which means that the non-idealities of the sampling process have milder effect. Theoretically the maximum clock rate of the continuous-time sigma-delta ADC is limited by the quantizer and the feedback DAC. Therefore, higher clock rates can be achieved than it is possible with the discrete-time implementation. On the other hand, the continuous-time loop filters are not as linear and accurate as the switched-capacitor filters. In addition, the continuous-time loop filters are not easy to design, because they have to be tuned and calibrated separately for every clock rate. [35]

Traditionally sigma-delta ADCs are used in applications where high resolution is needed but sampling rate requirements are rather modest. This kind of applications are, e.g., PC data acquisition systems, temperature measurements and various data loggers. [33] Additionally, sigma-delta ADCs are widely used in mobile phones. In practice, the achievable resolution in a discrete-time sigma-delta ADC is up to 24 bits while a signal bandwidth is in the order of a few MHz. In continuous-time sigma-delta ADCs, the signal bandwidth can be a few tens of MHz. The sigma-delta ADCs are tunable in the sense that it is possible to reduce the resolution in order to increase the sampling rate. In addition, the sigma-delta ADCs are rather power efficient. These are some aspects, besides noise shaping, that have led to consider the sigma-delta ADCs to be used in software defined radios. [19]

2.4. Compensation Methods

Digital post-processing is a powerful tool for compensating ADC errors caused by non-idealities. Hence, plenty of literature has been published about this topic especially in recent years. A journal article of state-of-the-art ADC compensation methods by E. Balestrieri *et al.* [9] classifies the methods in four categories. Look-up table (LUT) based methods, dithering methods and model inversion methods are discussed in the following subsections. These are more or less applicable for any ADC architecture. The fourth category mentioned by E. Balestrieri *et al.* [9] is architecture based methods. These models concentrate on specific details and typical problems of the particular converter

architecture. An architecture based method can be more effective but the number of suitable applications is limited compared to more general approaches.

2.4.1. Look-Up Table

Look-up table methods are based on precalculated estimation values which are stored in a table. The output samples of an ADC are used for indexing to point out corresponding values from a LUT. The look-up table can carry values which are meant either for correction or replacement. In the correction scheme, the LUT value is added to the output sample of the ADC. Replacement scheme refers to replacing the output sample of the ADC with the corresponding value from the LUT. [25]

The indexing is one of the most important parts of the LUT method. Based on the literature, it can be done in several different manners. The simplest one is static correction where the same output value of the ADC is every time mapped into the same index. Here, two more advanced methods are discussed which are called state-space indexing and phase-plane indexing. Both take the memory of the nonlinearity into account. The state-space indexing exploits both the current output sample $y(n)$ and the previous sample $y(n-1)$ for creating the index. Therefore, the LUT can be considered as two-dimensional. This principle is illustrated in Figure 2.8. The continuous-time input signal $s(t)$ is converted with the non-ideal ADC and then output samples $y(n)$ and $y(n-1)$ are used to retrieve corresponding value $\varepsilon(n)$ from the LUT. This value $\varepsilon(n)$ is then used to create the compensated output sample $\hat{s}(n)$. The state-space indexing approach can be extended to use more than just one previous sample. Naturally, this increases the effectiveness of the compensation but, on the other hand, also the number of dimensions in the LUT increases. Consequently, the LUT then requires significantly more memory. One solution for this problem is to apply more quantization for delayed samples, i.e. to use less bits, so that the size of the index space can be reduced. [25]

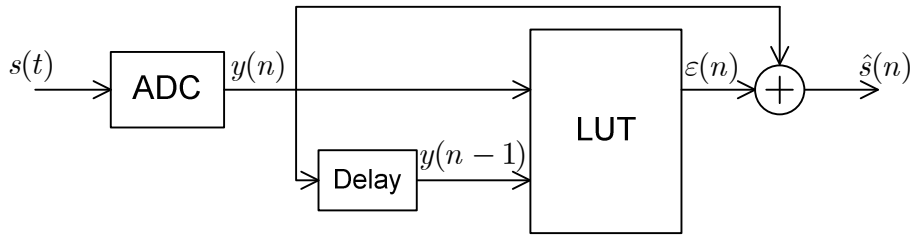

Figure 2.8. *Look-up table with state-space indexing, modified from [25].*

Another dynamic index method is phase-plane indexing. It is based on the present output sample $y(n)$ and estimate of the slope (or derivative) of the input signal $\hat{s}'(n)$. The principle is visualized in Figure 2.9. As in the previous method, the continuous-time input signal $s(t)$ is first converted with the ADC. Then a digital filter, for example a finite impulse response (FIR) differentiator, is used to produce the estimate $\hat{s}'(n)$. The corresponding LUT value $\varepsilon(n)$ is, once again, added to the output sample $y(n)$ to create compensated output sample $\hat{s}(n)$. Instead of using the digital filter, the slope can be acquired also by measuring the analog signal. [25]

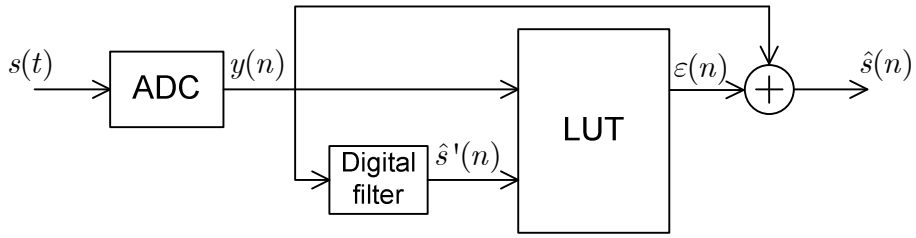

Figure 2.9. *Look-up table with phase-plane indexing, modified from [25].*

Apart from the indexing, a further challenge is to properly calibrate the correction (or replacement) values in the LUT. Basically, a calibration signal is fed to the ADC under test and the output is compared with the digital version of the calibration signal. Unfortunately the process is never ideal because only an estimate of the calibration signal can be used. The LUT calibration can be performed, for example, by using an additional very accurate ADC to acquire the digital version of the calibration signal fed to the ADC under test. Another option is to generate a digital calibration signal and use a DAC to feed the signal for the ADC under test. More advanced calibration methods proposed in the literature includes signal processing, e.g. based on a probability density function or optimal filtering, in order to estimate the calibration signal. [25]

2.4.2. Dithering

The essential idea of dithering is to intentionally add noise to ADC input signal before quantization and thus to reduce distortion induced by the quantization. The dithering reduces correlation between the input signal and the quantization error. For this reason, the pseudo quantization noise model can be made applicable. This model is exceedingly used because of its simplicity. It models the quantization error as an additive, uniformly distributed, white and zero-mean noise which is independent of the input signal. The dithering can also reduce distortion caused by quantizer non-idealities by randomizing

the DNL error pattern of a non-ideal uniform quantizer. Furthermore, dithering is able to increase the ADC resolution for slowly varying signals. It is typical that a quantized slowly varying signal has several consecutive output samples with the same value and thus quantization error cannot be reduced by averaging, i.e., low-pass filtering. By adding a proper dither signal prior to quantization, the output values are not all the same. Therefore in this case the averaging may yield better result and increase resolution. [25]

There are two types of dithering methods which are called subtractive and non-subtractive dithering. Both principles are illustrated in Figure 2.10. In the subtractive dithering, the dither noise is added to the input signal before the quantizer and the same noise is subtracted from the output after the quantization in the digital domain. However, it is worth noticing that the digital version of the dither noise is not always known explicitly and thus the subtraction is not ideal. On the contrary, the non-subtractive dithering method adds the dither noise prior to quantizer but is not even trying to remove all the noise after quantization. The method is based on the fact that the out-of-band noise can be filtered out in digital domain. Hence, only a part of the noise still exists in the final output signal. On the other hand, the non-subtractive method can never be expected to perform as well as ideal subtractive dithering. [25]

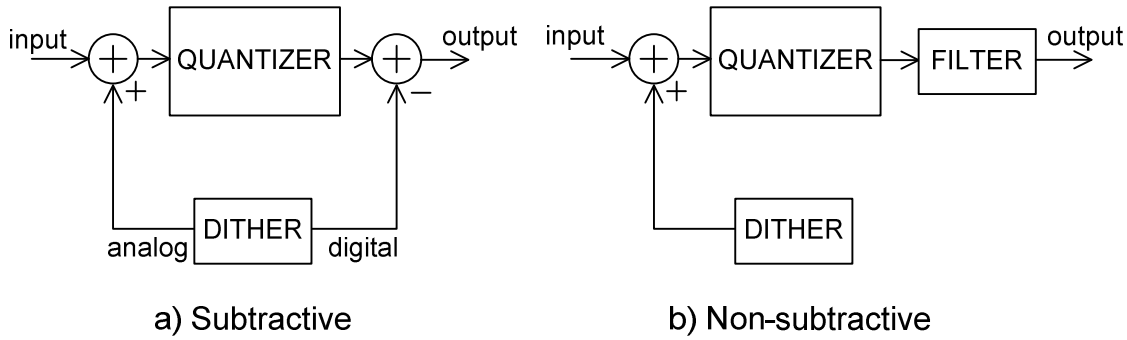

Figure 2.10. *Basic structures of a) subtractive and b) non-subtractive dithering principles, modified from [25].*

2.4.3. Model Inversion

The fundamental principle of the model inversion is to identify a mathematical system model which approximates the input-output relationship of the ADC. Then the inverse system, or approximation of it, is calculated to mitigate non-idealities from the output signal. These two stages are depicted in Figure 2.11. The model identification is performed by feeding a continuous-time input signal $s(t)$ to the ADC under test and to the ideal ADC. Then the test ADC output $y(n)$ and the model output $\hat{y}(n)$ are compared to

each other in order to tune the model H to match better with the test ADC. As presented in Figure 2.11 b), the post-distortion stage compensates ADC non-idealities by using the inverse of the model H, denoted with H^{-1}. There are several alternatives for the system modeling such as Chebyshev polynomials, but the most of the proposed methods in the literature are based on the Volterra model. Instead of the two-stage process illustrated in Figure 2.11, it is also possible to indentify the inverse model H^{-1} directly. In practice, this means tuning H^{-1} using error signal $\hat{s} - s$. [25]

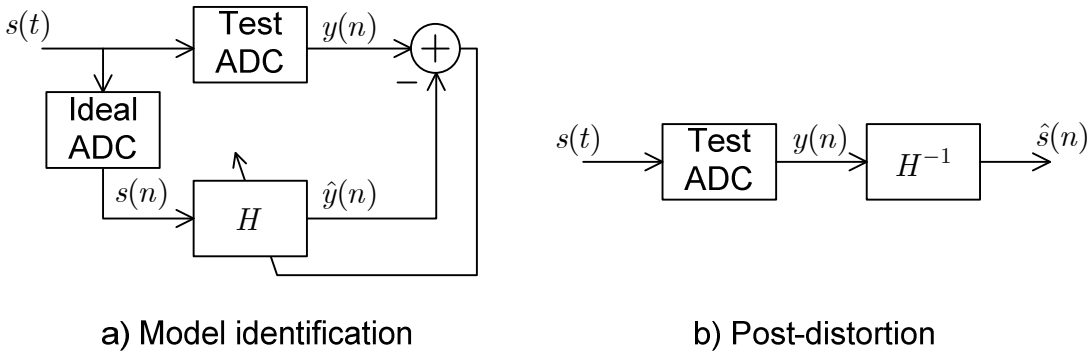

Figure 2.11. *Stages of a) model identification and b) post-distortion for ADC correction in the model inversion method, modified from [25].*

Volterra theory is a mathematical approach for describing causal nonlinear time-invariant systems with memory. The theory is usable for systems where the linear term is dominant compared to nonlinearities. The downside of the Volterra model is the computational complexity due to large amount of parameters. Therefore, simplified models such as Hammerstein, Wiener and Kautz-Volterra models have been introduced. Their number of parameters is lower but they don't have the generality of Volterra series. [12]

2.5. Clipping Effect in ADCs

In general, clipping stands for limiting signal amplitude to a certain maximum value. This can be either intentional or unintentional depending on the application. There are basically three different types of clipping: a limiter, hard clipping and soft clipping. An ideal limiter essentially outputs only the sign of the input signal. For the input signal $v_{in}(t)$ the ideal limiter is defined as

$$v_{\lim}(t) = V_0 \operatorname{sgn}\{v_{in}(t)\} = \begin{cases} +V_0, & \forall t : v_{in}(t) > 0 \\ -V_0, & \forall t : v_{in}(t) < 0, \end{cases} \tag{2.12}$$

where $v_{\mathrm{lim}}(t)$ is the clipped output signal and V_0 is the clipping level. [14] It is also intuitive to present transfer characteristics of the limiter in a graphical form as it has been done in Figure 2.12 a). Hard clipping differs from the limiter so that it also has a linear region. Therefore symmetric hard clipping is formulated to be

$$v_{cl}(t) = \begin{cases} v_{in}(t), & \forall t : |v_{in}(t)| < V_0 \\ +V_0, & \forall t : v_{in}(t) \geq V_0 \\ -V_0, & \forall t : v_{in}(t) \leq -V_0, \end{cases} \tag{2.13}$$

where $v_{cl}(t)$ represents the clipped signal. Figure 2.12 b) presents these input-output characteristics for the symmetric hard clipping. Furthermore, soft clipping is like hard clipping but it has smoother behavior near the saturation region. [39] This is visible in Figure 2.12 c). This can be modeled, for instance, with the arcus tangent function but naturally this is highly application dependent. It is worth noticing that various names are used in literature for different clipping types. There is possibility of confusion, for example, when the limiter is called hard clipping or hard clipping is called soft clipping.

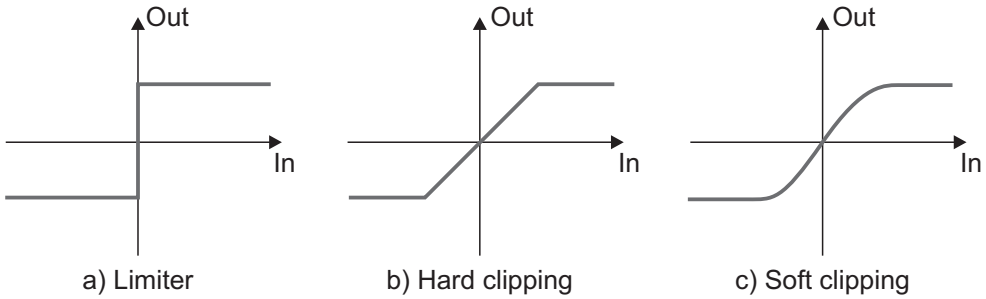

Figure 2.12. *Transfer functions for a) a limiter, b) hard clipping and c) soft clipping.*

When an analog signal with amplitude higher than the full-scale range is fed to the input of an ADC, the converter saturates and the signal is clipped. It is a rather realistic assumption that the behavior of the ADC can be modeled with symmetric hard clipping. The clipping is an instantaneous phenomenon which causes nonlinear distortion. In case of zero-symmetric hard clipping only odd-order distortion exists. Symmetry is a fair assumption at least when the DC offset has been corrected. It is important to avoid or mitigate the clipping because even light clipping in time domain can have severe effects to the frequency content. Detailed mathematical analysis of the symmetric hard clipping is presented in Section 4.1 and examples of clipping effects are depicted in Section 5.1.

2.5.1. Clipping in Radio Transmitters

Although this thesis focuses on radio receivers and ADCs, the transmitter side clipping is mentioned here for completeness. Deliberate clipping can be used in a radio transmitter to control the amplitude characteristics of the signal before transmitting. This has become more and more important due to more complex waveforms of modern communication systems. For example, orthogonal frequency division multiplexing (OFDM) and wideband code division multiple access (WCDMA) signals may have high peak-to-average power ratio (PAPR) which has to be controlled to ensure that power amplifiers and other critical components work on their optimal region.

If clipping has been used in a transmitter, it has to be compensated on receiver side. This is not a straightforward operation because of the filtering stages after clipping and especially due to the signal distortion stemming from the channel between the transmitter and the receiver. The literature proposes plenty of methods for the compensation. One possibility is to consider clipped samples as lost samples and reconstruct these by using other unclipped samples. This kind of method has been proposed by H. Saeedi *et al.* in [34] for OFDM systems. Their reconstruction algorithm is based on a least square method and requires an oversampled signal. Entirely different type of scheme, which doesn't need increased signal bandwidth, has been proposed by H. Chen *et al.* [15]. They used an iterative method to remove clipping noise from the received OFDM signal. First of all, symbols are normally decoded and detected from the received signal. After that the symbols are used to generate both clipped and unclipped estimate of the original transmitted signal. By subtracting these signals from each other, ideally only clipping noise remains. The clipping noise is then subtracted from the original received signal to achieve a cleaner signal for the next iteration cycle. However, the transmitter clipping compensation methods usually require exact knowledge of the clipping level and thus are not directly applicable for compensating receiver clipping, which is typically unintentional.

2.5.2. Clipping in Radio Receivers

Clipping on the receiver side is typically unintentional. One possible situation is clipping in an ADC due to improper input signal conditioning. Automatic gain control (AGC) attempts to keep the signal within the full-scale range of the ADC but this is not

always possible because of finite reaction speed of the AGC. This problem arises especially in wideband receivers where very strong blocker signals can change the signal dynamics rapidly. From the clipping compensation point of view, one challenge is that the exact clipping level is not known like it is in the transmitter clipping case. However, the good thing is that in the receiver side clipping there is no channel between the clipping and the compensator affecting the compensation performance.

The amount of literature about the clipping effects in receiver side seems to be somewhat limited but some compensation solutions do exist. T. Tomioka *et al.* [37] have proposed an interpolation technique for clipping noise suppression in cognitive radio transceivers. It requires an oversampling ADC so that sampling rate is high compared to the signal band of interest, although the band can be very wide already in case of cognitive radio. Suggested oversampling factors (OSFs) in the paper [37] were two and four. The algorithm starts with searching a cluster of clipped samples. Then polynomial interpolation, using two unclipped samples from before and after the cluster, is applied to the clipped samples. In this case, the polynomial interpolation refers to linear interpolation when the OSF is two or cubic polynomial if the OSF is four. This is a pre-interpolation stage which makes a main interpolator perform better.

T. Tomioka *et al.* [37] have used a fractional delay FIR filter as a main interpolator, which impulse response is a sampled and truncated sinc function. The oversampled signal can be thought through a polyphase decomposition where samples $Ln + a$ are in the same branch. Here the oversampling factor is denoted with L, the sample index is n and the polyphase branch index is a. The sinc interpolation is performed so that the center tap of the sinc impulse response is aligned with a clipped sample. Then a proper polyphase branch is chosen and a new value for clipped sample is calculated using the sinc-based polyphase filter of that branch. According to the paper [37] branch index a is selected by multiplying the nearest unclipped sample from both sides of the cluster with the corresponding sinc value. Then the sample that gives larger value is selected and the branch related to that sample is chosen.

Good compensation performance can be achieved with the interpolation of the oversampled signal. Especially in wideband systems, the efficiency of compensation schemes is very important. Therefore, partially similar type interpolation methods as presented in [37], but with more optimized implementation and better performance, are proposed in Section 4.3 of this thesis.

3. RADIO RECEIVER ARCHITECTURES AND ANALOG-TO-DIGITAL CONVERTERS

This chapter is devoted for the requirements of analog-to-digital converters in different types of radio receivers. In the past, an ADC was not the main concern because most of the receiver's selectivity was implemented with analog components and the digitalization was performed at a low center frequency. However, a modern trend is to reduce analog components and move the ADC as close to the antenna as possible in the receiver chain [26]. By cutting down the number of analog parts, more configurability and better integrability as well as savings in size and power dissipation can be achieved. The ultimate goal will be the so-called software defined radio. This sets significantly stricter requirements for ADCs because most of the signal processing is done in the digital domain.

Section 3.1 first discusses about the key parameters of analog-to-digital converters and what kind of trade-offs there are between them in practical ADCs. Then, some of the most common radio receiver architectures are presented in Section 3.2. Also architectures' impacts on the ADC requirements are mentioned. After that, Section 3.3 presents a few specifications of modern wireless standards and summarizes their effect on the analog-to-digital converters.

3.1. Trade-Offs Between Speed, Resolution and Power Dissipation

Wireless system standards have different kinds of requirements for the dynamic range. Resolution of an analog-to-digital converter, i.e. number of bits in ADC, essentially defines the maximum possible dynamic range. That is because the resolution describes the size of the LSB which actually is the smallest change in a signal that the ADC can accurately describe in the digital domain. The Equation (2.4) gives SQNR for an ideal quantizer and therefore gives another point of view to what kind of effect resolution has on dynamic range. It is worth noticing that the dynamic range of an actual ADC is de-

termined not only by the number of bits but also by the linearity of the ADC. Different kinds of nonlinearities cause spurious frequency components that reduce dynamic range of the ADC.

Dynamic range and linearity are particularly important in a wideband receiver where several signal bands are digitized as a whole. Some signal bands can be significantly stronger than others and the difference can be in the order of tens of dB's. There is usually automatic gain control in front of the ADC so that the received waveform is properly scaled for the full-scale range of the ADC. The scaling is based on strength of the overall waveform and therefore sufficient resolution is needed to detect also the weakest signals and not only the strongest. If the weak signal is not buried in quantization noise, i.e. resolution is high enough, problems may still occur due to spurious frequencies. The nonlinear behavior of the ADC may cause the spurious frequencies stemming from the strong signals to fall on top of the weak signal. [27]

Although dynamic range can be increased by using a higher resolution converter, there are inevitable trade-offs. First of all, high resolution converters typically have low sampling rates. Dependency of resolution and speed varies between different ADC architectures but it can always be seen. [24], [41] Another issue is the trade-off between resolution and power dissipation. High precision converters are likely to consume more power due to their structure. [31] This is important consideration particularly in mobile devices because of their limited amount of energy stored in a battery. Added to this, the power dissipation is directly proportional to the sampling rate of the ADC. This is because the most of the power is consumed in a sample-and-hold circuit and comparators. ADC architecture affects the number of comparators and thus different architectures can have significantly different power consumption. [24]

Figure 3.1 pulls together the relationships between the three discussed performance parameters of ADCs. When considering ideal analog-to-digital converters theoretically, these trade-offs are not directly visible. Nevertheless, in practice the trade-offs are strongly present even in modern ADCs. The relationships between the sampling rate, the resolution and the power dissipation are not necessarily linear – at least not for all ADC architectures [24]. Figure 3.1 visualizes in a simplified manner that power dissipation is increased if sampling rate and/or resolution is increased. It also shows the fact that high-resolution converters tend to have lower sampling rates for given cost and power dissipation.

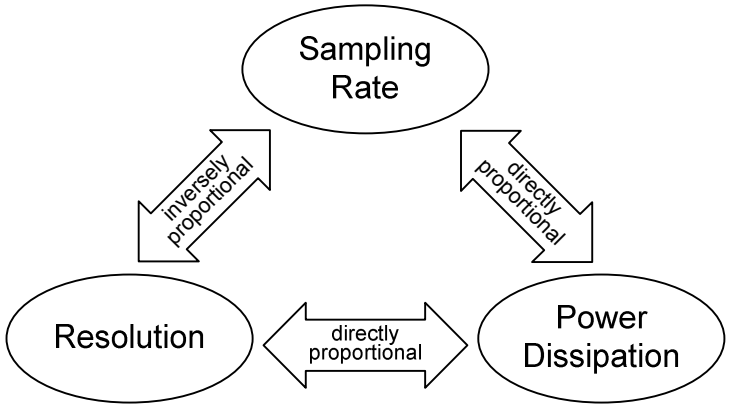

Figure 3.1. *Illustration of trade-offs between the three main performance parameters in analog-to-digital converters.*

3.2. Common Receiver Architectures

This section is devoted to present the most common radio receiver architectures. Advantages and disadvantages of every architecture are discussed. Especially the ADC related aspects are considered.

3.2.1. Superheterodyne Receiver

One of the most popular radio receiver architectures in the past has been superheterodyne. Despite its advantages, technology improvements and a need for configurability have nowadays led to receiver architectures which have less analog components. Basic principle of the superheterodyne receiver is depicted in Figure 3.2. After proper RF filtering and amplification the signal is mixed to the first (constant) IF. This is usually done by tuning the LO (local oscillator) frequency so that regardless of the original center frequency of the received signal it is always mixed to the same IF. The receiver uses two separate IF stages to relieve filter requirements related to selectivity as well as image suppression. IQ mixing is used to bring the signal to the second (lower) IF or baseband (BB). After the final channel selection filtering, the I and Q signals are digitized with separate analog-to-digital converters. [31]

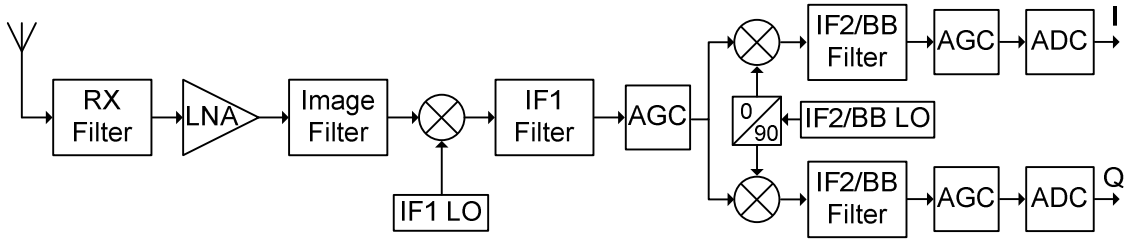

Figure 3.2. *Block diagram of a traditional superheterodyne receiver with two IF stages, modified from [19], [31].*

There is a substantial amount of analog processing in the superheterodyne receiver. Filtering, mixing and channel selection are all done before the analog-to-digital conversion. Therefore requirements are rather modest for an ADC considering linearity, dynamic range and bandwidth, especially because the final IF is usually rather low or even zero. Main disadvantages in the superheterodyne architecture are the poor configurability and analog parts that are challenging to integrate. [19]

3.2.2. Direct Conversion Receiver

Direct conversion architecture has a simpler analog side than the superheterodyne. It employs only a single mixing stage as illustrated in Figure 3.3. The direct conversion receiver has only the RF filtering and amplification stages before the signal is mixed to baseband. Therefore the LO frequency has to be tunable according the center frequency of the received signal as it was the case also with the superheterodyne architecture. Due to the IF being zero the image suppression filtering is not required. After IQ mixing, low-pass channel filtering is applied separately for both branches before the analog-to-digital conversion. If the zero IF is not desirable, another option is to use some low frequency near the baseband. This is usually called a low-IF receiver. The rather simple structure of the direct conversion receiver means better integration capability, lower power consumption and some savings in component costs. On the contrary, there are more problems with the DC offset and second-order distortion when operating around the baseband. Additionally, I/Q mismatch is a problem in direct conversion receivers. It is stemming from imbalance in the I/Q mixing stage and in the branch components (low-pass filters, etc.). [19], [31] Direct conversion receivers are frequently proposed for implementing multi-standard software defined radios, see e.g. [36] and the references therein.

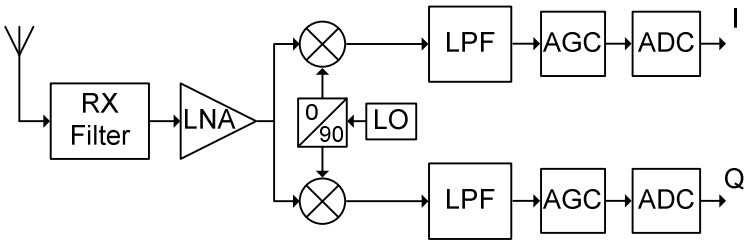

Figure 3.3. *Block diagram of a direct conversion receiver with a single I/Q mixing stage, which converts the received signal to the baseband before the analog-to-digital conversion, modified from [19], [31].*

Basic direct conversion architecture doesn't provide so much configurability because some amount of analog hardware is still needed. On the other hand, nowadays more wideband direct conversion receivers are designed. It means that several channels or even several separate signal bands can be digitized as a whole. There can be significant differences in the power levels of the separate signal bands and hence the large dynamic range has to be taken into account in the requirements for all receiver components. From the ADC point of view, requirements are rather relaxed if only a single channel is digitized at a time. This is because the analog filtering is rather selective and the signal with relatively low bandwidth is digitized at the baseband. [19] In the wideband direct conversion receiver, the dynamic range and the resolution as well as linearity of the ADC become key issues. High resolution is needed to make detection of weak signals possible when there are significantly stronger signals present in neighboring frequency bands. Nonlinearities in the ADC cause intermodulation distortion which means that signals at different frequency bands may interfere with each other.

3.2.3. RF-Sampling Receiver

An RF receiver employing RF sampling would be highly desirable architecture option for software defined radios due to its configurability for various wireless standards. Figure 3.4 shows the simple structure of the RF receiver. The coarse receive filtering doesn't implement strict selectivity but only prevents excessive aliasing and thus the signal to be digitized can be very wideband. In practice, the bandwidth can be tens of megahertz or even hundreds of megahertz while the dynamic range can be as much as 100 dB. This sets harsh requirements especially for the ADC and practical implementations are somewhat out of the question with today's technology. This is especially true, if the power consumption limitations and manufacturing costs of mobile terminals are considered. Additionally, the quickly changing signal dynamics require short reaction times from the automatic gain control and this requirement is challenging to meet with this kind of single-stage gain control. [31] Improper input signal conditioning for the ADC may cause severe nonlinear distortion. This topic is elaborated further in Section 4.1. Moreover, the jitter (timing uncertainty) caused by the sampling circuit and sampling clock is also one major problem in RF receivers. This is because the high-frequency signals are sensitive for timing errors. On the other hand, the RF-sampling

receiver provides high integration capability as well as flexibility to choose exact signal bands in the digital domain.

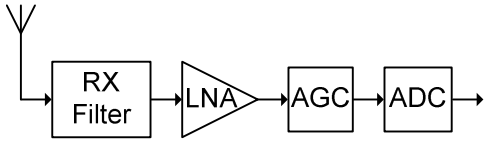

Figure 3.4. *Block diagram of RF receiver with only minimal filtering and amplification before analog-to-digital conversion, modified from [31].*

3.3. System Performance Requirements

Modern wireless system standards have considerably different kinds of signal bandwidths and operating frequencies. The trend seems to be towards wider bandwidths and higher operating frequencies in order to satisfy the growing demand of high data rates. It means that ADCs will be more and more the bottleneck for the whole receiver, especially when the ADC is a part of a wideband receiver and digitizes several signal bands together. This is straightforward to conclude from Table 3.1 which shows characteristics of a few important wireless systems. Many of them might coexist in same mobile device.

Table 3.1. *The operating frequencies and the channel bandwidths for different wireless standards [20], [21], [40].*

Wireless System	**Operating Frequency**	**Channel Bandwidth**
GSM	900, 1800 and 1900 MHz	200 kHz
WCDMA	1.9 and 2.1 GHz	5 MHz
LTE / LTE-Advanced	450–3600 MHz (several bands)	20 MHz / 100 MHz
Bluetooth	2.4 GHz	1 MHz
802.11g (WLAN)	2.4 GHz	20 MHz

The upcoming LTE-Advanced meet the IMT-Advanced requirements and will have channel bandwidth up to 100 MHz which directly gives sampling rate requirement of at least 200 Msps. In addition to that, individual terminals in LTE-Advanced can operate on a very wide range of frequencies reaching from 450 MHz to 3.6 GHz [20]. Current cellular systems such as GSM and WCDMA have narrower bandwidths but it is desirable that the ADC can digitize the whole cellular band and not just a single channel [40].

Considering the case where an ADC samples straight from the RF, full-power bandwidth of the ADC is likely to become a limiting factor. According to Table 3.1 LTE and LTE-Advanced has operating frequencies as high as 3.6 GHz and many other systems operate at frequencies over 2 GHz. Even if the ADC meets resolution and sampling rate requirements, the full-power bandwidth is usually not enough for this purpose. Until major improvements happen, analog mixing is needed to convert the signal from the RF to the IF prior to analog-to-digital conversion. [40] For a concrete example, a modern 12-bit converter MAX19542 has a sampling rate of 170 Msps and a full-power bandwidth of 900 MHz [28]. Power dissipation of the converter is 907 mW so it is not a feasible choice for mobile equipment. On the other hand, it would be useful in base stations where the power consumption is not so limited.

4. NONLINEAR DISTORTION COMPENSATION STUDIES

Symmetric hard clipping taking place, for example, in a radio receiver is possible to model mathematically by using the well-known Fourier series. It helps to give better understanding for the whole phenomenon since the Fourier series can represent different distortion orders (frequency components) separately. A special property of the Fourier series in the clipping case is the time-varying nature of the Fourier coefficients, if the signal has varying envelope. This topic is discussed in Section 4.1 and also published in [2].

Section 4.2 introduces a concept called adaptive interference cancellation (AIC) for compensating ADC nonlinearities. Two practical applications for AIC are considered here. The first one is clipping compensation and another is INL error mitigation. The AIC method is also discussed in [1]–[3]. Section 4.3 presents another kind of approach for the clipping compensation. It is based on interpolation which is rather traditional way to recover lost samples. The purpose of the section is to consider a case of an over-sampling ADC and discuss how the signal can be enhanced in a clever way by using polyphase decomposition approach. This is considered also in [3].

4.1. Mathematical Analysis of Symmetric Clipping

Knowing the exact behavior of symmetric hard clipping is important when dealing with clipping compensation algorithms for analog-to-digital converters. This section gives a frequency domain analysis view for the clipping effect by using a model based on Fourier series. The starting point of this analysis is partially based on the nonlinear distortion study in case of a limiter by A. Carlson [14]. However, the hard clipping case considered here is more complex because it is highly dependent of signal envelope.

4.1.1. Model for a Real Band-Pass Signal

A general model for a real band-pass signal can be stated regarding to time variable t as

$$v_{in,I}(t) = A(t)\cos\theta_c(t), \tag{4.1}$$

where $A(t)$ is the signal envelope and $\theta_c(t) = \omega_c t + \phi(t)$ which consists of angular frequency ω_c and phase $\phi(t)$. The subscript notation *I* is used because $v_{in,I}(t)$ is also the in-phase branch (I branch) of the corresponding complex band-pass signal. The complex version is discussed later in this subsection after the real model is first derived.

Clipping is an instantaneous phenomenon, i.e., it doesn't necessarily happen all the time. Naturally, when clipping doesn't happen the output signal is the same as the input signal $v_{in,I}(t)$. In case of clipping, the output is described with a function $v_{cl,I}(t)$. Therefore the output signal $v_{out,I}(t)$ has to be defined so that

$$v_{out,I}(t) = \begin{cases} v_{in,I}(t), & \forall t : |A(t)| < V_0 \\ v_{cl,I}(t), & \forall t : |A(t)| \geq V_0 \end{cases} \tag{4.2}$$

in which the clipping level is denoted with V_0. The definition is practical from the modeling point of view when using Fourier series. There is no need to analyze the clipping effect when the signal envelope is not clipped, because there is no distortion. Actually, the used Fourier series is valid only when the signal envelope $A(t)$ is clipped or is equal to the clipping level V_0. When this condition is satisfied, the Fourier series is created based on the symmetric clipping definition in Equation (2.13) which becomes now

$$v_{cl,I}(t) = \begin{cases} v_{in,I}(t), & \forall t : \left|v_{in,I}(t)\right| < V_0 \\ +V_0, & \forall t : v_{in,I}(t) \geq V_0 \\ -V_0, & \forall t : v_{in,I}(t) \leq -V_0. \end{cases} \tag{4.3}$$

This should be interpreted so that the Fourier series models the full signal behavior at the time instances when the signal envelope $A(t)$ is clipped – no matter if the signal $v_{in,I}(t)$ itself is clipped or not. The definition in Equation (4.2) is also practical in the sense that the Fourier series model is also valid for the quadrature branch (Q branch) at the same time instances if a complex signal is considered. Therefore the complex signal behavior can be modeled with complex Fourier series. This is discussed in Subsection 4.1.2.

Fourier series can describe how the energy is divided in the clipped signal between different frequency components and therefore gives better understanding for the whole phenomenon. The input signal $v_{in,I}(t)$ doesn't have to be periodic in time, but it can be always seen as a periodic function of θ_c where the period is 2π. When taking the time

varying nature of the signal into consideration it is clear from the definition of the Fourier series that

$$v_{cl,I}(t) = \sum_{m=1}^{\infty} \left|2a_{m,I}(t)\right| \cos\left(m\theta_c(t) + \arg a_{m,I}(t)\right), \tag{4.4}$$

where

$$a_{m,I}(t) = \frac{1}{2\pi} \int_{2\pi} v_{cl,I}(t) e^{-jm\theta_c(t)} \mathrm{d}\theta_c(t)\,. \tag{4.5}$$

Here the Fourier series index m can also be thought as a distortion order. If the signal envelope $A(t)$ is constant in time, Fourier coefficients $a_{m,I}(t)$ are also constants. It means that the whole clipped signal behavior would be possible to describe with a single set of constants reaching from $a_{1,I}$ to $a_{m,I}$. On the other hand, varying signal envelope requires that a different set of Fourier coefficients is needed for every time instant t.

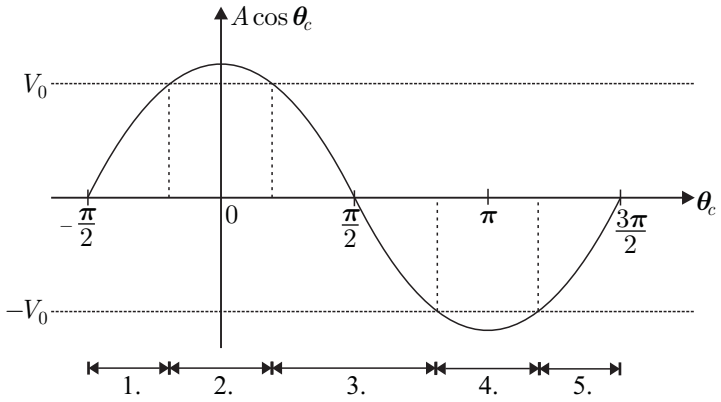

Figure 4.1. *In case of symmetric clipping of a real band-pass signal $v_{in,I}(t)$, the signal is here presented as a function of the instantaneous angle θ_c over one period for deriving the Fourier coefficients. The period of 2π is split into five integration intervals.*

Now let the time be fixed so that the equation for a set of Fourier coefficients from $a_{1,I}$ to $a_{m,I}$ can be derived. At every time instant t the function $\theta_c(t)$ has one specific value and all of these possible values can be covered in the period of 2π. In Figure 4.1, $v_{in,I}$ is illustrated over one period of θ_c. In other words, the signal envelope $A(t)$ has a single value at the specific time instant t and therefore the signal behavior can be described explicitly with a single set of Fourier constants. This set of Fourier constants is the same no matter what is the value of θ_c at the time instant t. If the value of $A(t)$ is

different at the next time instant t, then a new set of Fourier coefficients has to be calculated.

Figure 4.1 also shows five integration intervals which are used to derive the final equation for the Fourier coefficients from the Equation (4.5). The value of θ_c in the starting and ending points of clipped sections can be found with the help of equation

$$A\cos(\theta_c) = V_0\,. \tag{4.6}$$

When the integration intervals and the Equation (4.3) for $v_{cl,I}(t)$ are substituted in the Equation (4.5), Fourier coefficients get the following form

$$\begin{aligned} a_{m,I}(t) = \frac{1}{2\pi}\Bigg[& \int_{-\frac{\pi}{2}}^{-\arccos\frac{V_0}{A(t)}} v_{in,I}(t)e^{-jm\theta_c(t)}\mathrm{d}\theta_c(t) + \int_{-\arccos\frac{V_0}{A(t)}}^{\arccos\frac{V_0}{A(t)}} V_0 e^{-jm\theta_c(t)}\mathrm{d}\theta_c(t) \\ & + \int_{\arccos\frac{V_0}{A(t)}}^{\pi-\arccos\frac{V_0}{A(t)}} v_{in,I}(t)e^{-jm\theta_c(t)}\mathrm{d}\theta_c(t) + \int_{\pi-\arccos\frac{V_0}{A(t)}}^{\arccos\frac{V_0}{A(t)}+\pi} -V_0 e^{-jm\theta_c(t)}\mathrm{d}\theta_c(t) \\ & + \int_{\arccos\frac{V_0}{A(t)}+\pi}^{\frac{3\pi}{2}} v_{in,I}(t)e^{-jm\theta_c(t)}\mathrm{d}\theta_c(t)\Bigg]. \end{aligned} \tag{4.7}$$

The Equation (4.7) can be simplified in a rather straightforward manner and the final form of the formula is

$$a_{m,I}(t) = \begin{cases} \dfrac{A(t)}{2} - \dfrac{A(t)}{\pi} r_I(t) + \dfrac{V_0}{\pi}\sqrt{1-\left(\dfrac{V_0}{A(t)}\right)^2}, & m = \pm 1 \\ \dfrac{-2V_0\sin\left(mr_I(t)\right) + 2m\sqrt{A^2(t)-V_0^2}\cos\left(mr_I(t)\right)}{\pi m(m^2-1)}, & m = \pm 3, \pm 5, \pm 7, \ldots \\ 0, & m = 0, \pm 2, \pm 4, \ldots \end{cases} \tag{4.8}$$

where $r_I(t) = \arccos\frac{V_0}{A(t)}$. The detailed derivation for $a_{m,I}(t)$ can be found in Appendix. Due to distinct symmetry, only the indices m greater than zero are needed for analyzing real band-pass signals. Negative indices have significance in the complex case due to the asymmetric frequency content, which is discussed in Subsection 4.1.2.

From Equation (4.8) it is immediately clear that symmetric hard clipping does not create even-order nonlinear distortion. It can also be seen that in case of clipping the amplitudes of original frequencies ($m = 1$) are always attenuated. In special case,

when the amplitude $A(t)$ equals to the clipping level V_0, the Fourier coefficient for $m = 1$ is $\frac{A(t)}{2}$ and all the other Fourier coefficients reduce to zero. This is exactly as it should be when the clipping doesn't occur, i.e., only the fundamental frequencies are seen in the output with their original amplitudes. Another aspect worth noticing is the phase behavior. The original signal has its phase unchanged, but the nonlinear distortion components have phases that are multiples of corresponding m compared to the original signal phase. This is evident from the Equation (4.4).

4.1.2. Model for a Complex Band-Pass Signal

After deriving the mathematical model for the real band-pass signal, the complex version is a rather straightforward extension. Signal model for quadrature branch of the complex band-pass signal is

$$v_{in,Q}(t) = A(t)\sin\theta_c(t)\,. \tag{4.9}$$

It is used to derive a model for the clipped Q branch output $v_{cl,Q}(t)$ in exactly the same manner as for the I branch in the Equation (4.3). Hence

$$v_{cl,Q}(t) = \begin{cases} v_{in,Q}(t), & \forall t : \left|v_{in,Q}(t)\right| < V_0 \\ +V_0, & \forall t : v_{in,Q}(t) \geq V_0 \\ -V_0, & \forall t : v_{in,Q}(t) \leq -V_0 \end{cases} \tag{4.10}$$

and it's worth noticing that here the clipping level V_0 is the same as for the I branch. This assumption is justified because it's possible to achieve in real-life ADCs by using, for example, calibration.

Fourier coefficients for the Q branch can be derived from

$$a_{m,Q}(t) = \frac{1}{2\pi}\int_{2\pi} v_{cl,Q}(t)e^{-jm\theta_c(t)}\mathrm{d}\theta_c(t)\,. \tag{4.11}$$

Integration intervals are given in Figure 4.2 which illustrates the quadrature input signal $v_{in,Q}(t)$ over one period of θ_c when the time is held fixed. Now the Fourier coefficients in Equation (4.11) get form

$$a_{m,Q}(t)=\frac{1}{2\pi}\left[\int_{-\frac{\pi}{2}}^{-\arcsin\frac{V_0}{A(t)}}-V_0e^{-jm\theta_c(t)}\mathrm{d}\theta_c(t)+\int_{-\arcsin\frac{V_0}{A(t)}}^{\arcsin\frac{V_0}{A(t)}}v_{in,Q}(t)e^{-jm\theta_c(t)}\mathrm{d}\theta_c(t)\right.$$
$$+\int_{\arcsin\frac{V_0}{A(t)}}^{\pi-\arcsin\frac{V_0}{A(t)}}V_0e^{-jm\theta_c(t)}\mathrm{d}\theta_c(t)+\int_{\pi-\arcsin\frac{V_0}{A(t)}}^{\arcsin\frac{V_0}{A(t)}+\pi}v_{in,Q}(t)e^{-jm\theta_c(t)}\mathrm{d}\theta_c(t) \qquad (4.12)$$
$$\left.+\int_{\arcsin\frac{V_0}{A(t)}+\pi}^{\frac{3\pi}{2}}-V_0e^{-jm\theta_c(t)}\mathrm{d}\theta_c(t)\right].$$

The calculation for Equation (4.12) goes in a manner similar to that in I branch presented in Appendix. Hence, the final form is

$$a_{m,Q}(t)=\begin{cases}-j\left(\dfrac{A(t)}{2}-\dfrac{A(t)}{\pi}r_I(t)+\dfrac{V_0}{\pi}\sqrt{1-\left(\dfrac{V_0}{A(t)}\right)^2}\right), & m=1\\[2ex] -j\left(-\dfrac{A(t)}{2}+\dfrac{A(t)}{\pi}r_I(t)-\dfrac{V_0}{\pi}\sqrt{1-\left(\dfrac{V_0}{A(t)}\right)^2}\right), & m=-1\\[2ex] -j\dfrac{-2V_0\cos\left(mr_Q(t)\right)+2m\sqrt{A^2(t)-V_0^2}\sin\left(mr_Q(t)\right)}{\pi m(m^2-1)}, & m=\pm3,\pm5,\pm7,...\\[2ex] 0, & m=0,\pm2,\pm4,...\end{cases} \qquad (4.13)$$

where $r_Q(t)=\arcsin\frac{V_0}{A(t)}$. The coefficients $a_{m,Q}(t)$ are imaginary here due to the anti-symmetry of the sine function. The final forms of the Fourier coefficients will be real valued when the definition for Fourier series is considered.

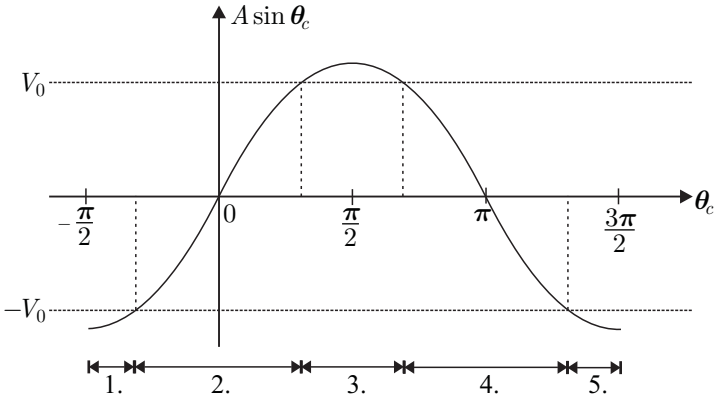

Figure 4.2. *In case of symmetric clipping of the quadrature branch $v_{in,Q}(t)$, the signal is presented here as a function of the instantaneous angle θ_c over one period for deriving the Fourier coefficients. The period of 2π is split into five integration intervals.*

The overall output signal in case of a complex signal waveform is

$$v_{out}(t) = \begin{cases} v_{in,I}(t) + jv_{in,Q}(t), & \forall t : |A(t)| < V_0 \\ v_{cl,I}(t) + jv_{cl,Q}(t), & \forall t : |A(t)| \geq V_0. \end{cases} \tag{4.14}$$

By using the definition for Fourier series and taking the time varying nature into account, model for the clipped complex band-pass signal is

$$v_{cl}(t) = \sum_{m=-\infty}^{\infty} \left(a_{m,I}(t) + ja_{m,Q}(t) \right) e^{jm\theta_c(t)} . \tag{4.15}$$

Because of the symmetry, the model can be written in a simpler form so that

$$v_{cl}(t) = \sum_{m=-\infty}^{\infty} 2a_{m,I}(t)e^{jm\theta_c(t)}, \quad m = (-1)^{k-1}(2k-1) \text{ and } k \in \mathbb{N} \setminus \{0\}. \tag{4.16}$$

This stems from the fact that the Fourier coefficients are the same for I and Q branches when index m has values 1, -3, 5, -7 and so on. In practice, this is possible to see from the spectrum of clipped signal where every second odd distortion order is located in the negative side. According to the mathematical model there is no signal energy with any other values of m. The Equation (4.13) for $a_{m,Q}(t)$ has opposite sign than $a_{m,I}(t)$ in the special case when $m =$ -1 and thus the combination of these two produces zero output.

4.1.3. Example of Clipping Distortion

The instantaneous nature of clipping can be clarified through an example. Figure 4.3 shows spectrum for both unclipped and clipped band-pass QPSK signal with 10 MHz center frequency and oversampling factor 256. Sampling frequency of 256 MHz is used. In this simulation example, the signal is ideally clipped without quantization or any other additional distortion to better emphasize the effect of clipping. The clipping level is identical for I and Q branches. From the power spectrum it's easy to see the odd-order nonlinear distortion due to the clipping around 10 MHz, -30 MHz, 50 MHz etc. However, the spectrum doesn't directly show the instantaneous nature of clipping.

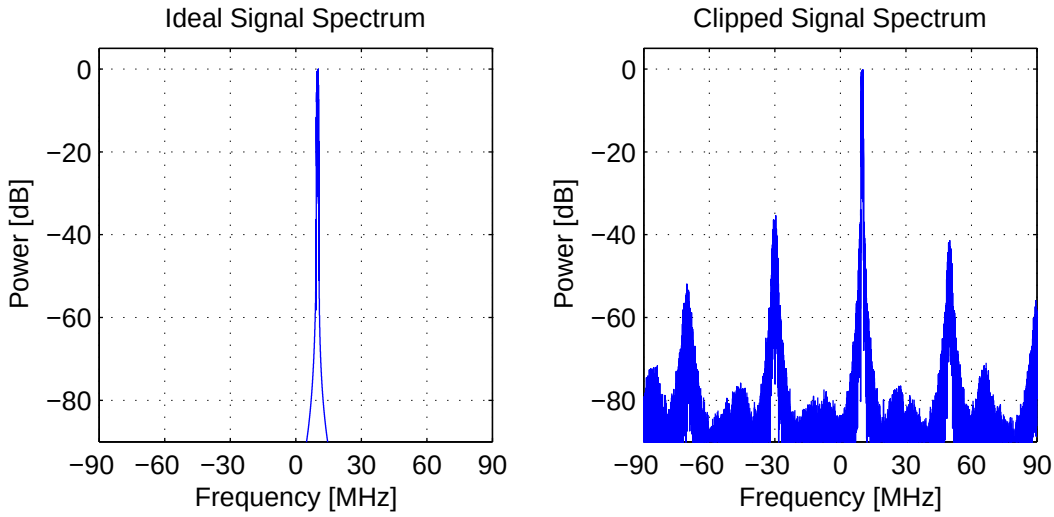

Figure 4.3. *Frequency domain illustrations for a complex band-pass QPSK signal with center frequency of 10 MHz and the symmetrically clipped version of the same signal.*

The instantaneous characteristics of clipping are clearly visible if the distortion is examined in time domain as it is done in Figure 4.4. The upper part of Figure 4.4 presents a piece of the original waveform with magenta and the corresponding clipped signal with black color. The original signal envelope $A(t)$ is plotted with green color. In the simulation the third-order nonlinear distortion is separated with a complex band-pass filter which has center frequency of -30 MHz. This is shown in the lower part of Figure 4.4 with black color. Cyan color represents the corresponding waveform calculated with the mathematical model given in Equations (4.14) and (4.16) when m equals to -3. The simulated third-order distortion waveform (black line) is only faintly visible because it matches very well with the mathematical model. Deviations are stemming from the non-ideal band-pass filter used in the distortion extraction. It is non-ideal in the sense that it can't be guaranteed that the filter picks up exactly the third-order distortion only and nothing else due to the limitations in filter implementation resources.

When considering individually, e.g., third-order distortion, it is not only present when the signal waveform is clipped but can be seen at other time instances also. To be more precise, the distortion is always there when the signal envelope $A(t)$ is clipped. Hence, in a sense the clipping distortion is spread in time if only one or a few distortion orders are considered. This is understandable because there is no frequency interpretation at a single time instant and therefore no interpretation for a single distortion order. The time spreading is hence only a feature when the distortion orders are separated but together, after summation, they describe the clipped signal waveform as a whole.

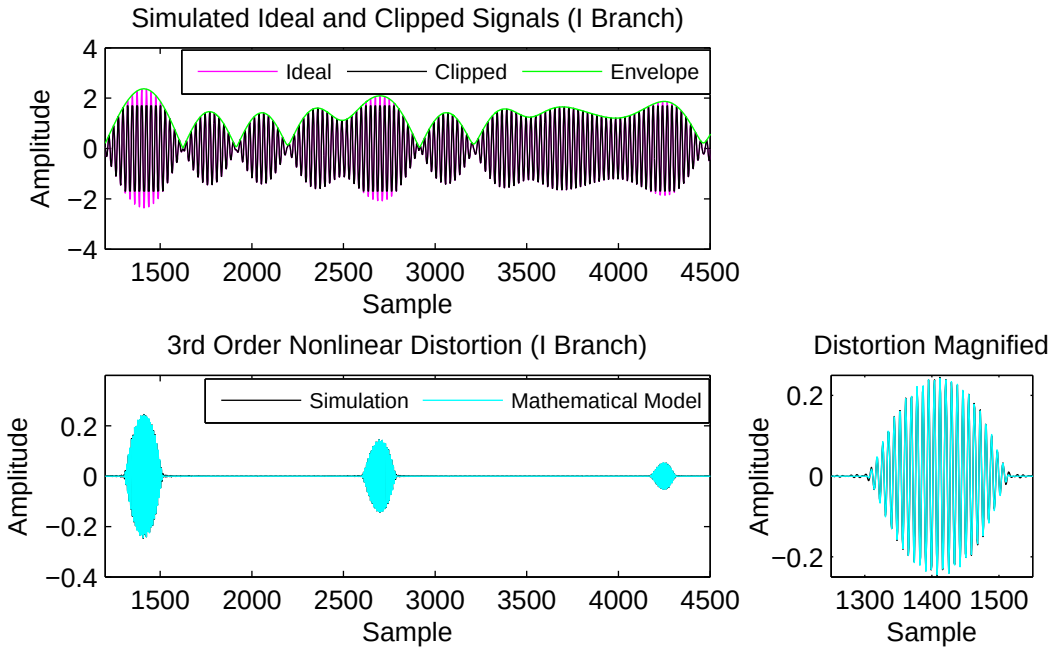

Figure 4.4. *Example of a clipped band-pass QPSK signal and its third-order nonlinear distortion in time domain, bottom right showing magnified version of the distortion waveform.*

4.2. Adaptive Interference Cancellation

An interference cancellation method discussed in this thesis relies on a presumption that ADC nonlinearities can be modeled with a memoryless nonlinearity and an ideal quantizer. The cascade of these two is presented in Figure 4.5 for input signal s and output signal y. One very general approach is to model the signal after the nonlinearity with a polynomial, which can be defined as

$$\tilde{s} = g(s) = c_0 + c_1 s + c_2 s^2 + c_3 s^3 + \ldots, \tag{4.17}$$

where c's are weights for the different powers of s. This kind of model is useful particularly from the interference cancellation point of view.

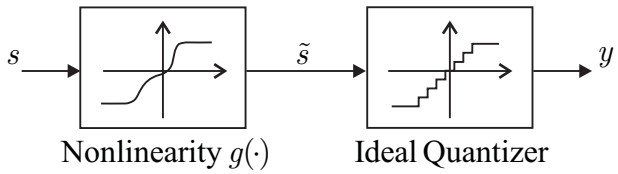

Figure 4.5. *Model for ADC nonlinearities consisting of a memoryless nonlinearity and an ideal quantizer.*

The digital post-processing principle presented in this thesis is based on adaptive interference cancellation. The basic idea is grounded on the study by M. Valkama

et al. [38]. They considered AIC for compensating mixer and low-noise amplifier (LNA) nonlinearities in wideband multicarrier radio receivers. This section describes how the AIC principle can be applied for the compensation of ADC nonlinearities. In addition to this, a modified approach is proposed to overcome some limitations of the original design by using an additional low-bit ADC. Especially, application details regarding to clipping compensation and INL mitigation are considered here.

4.2.1. Introduction to the Post-Processing Principle

The AIC principle is used with a wideband ADC that converts a wide frequency band consisting of several signals with different center frequencies. The overall signal may have dynamic range of tens of dB's and therefore nonlinearities in the ADC can have severe effects when the distortion from strong blocker signals fall at a weak signal band. The AIC system tries to reduce the interference on that weak signal.

The block diagram of the AIC principle is shown in Figure 4.6 accompanied by very simplified stage-by-stage spectrum examples labeled with capital letters from *A* to *F*. After the ADC, the input signal (spectrum *A*) is nonlinearly distorted which is illustrated in spectrum *B* in Figure 4.6. For the sake of simplicity only a single intermodulation frequency component originating from two strong blocker signals is drawn within the band of the weak signal of interest. The band-splitting stage uses digital filters to divide the distorted signal in two branches. The lower branch should contain only the interfering signals as it is shown in spectrum figure *C*. For now on, the lower branch signal is called reference signal. Correspondingly, the upper branch should contain only the distorted version of the desired weak signal band. This is illustrated in spectrum figure *D*.

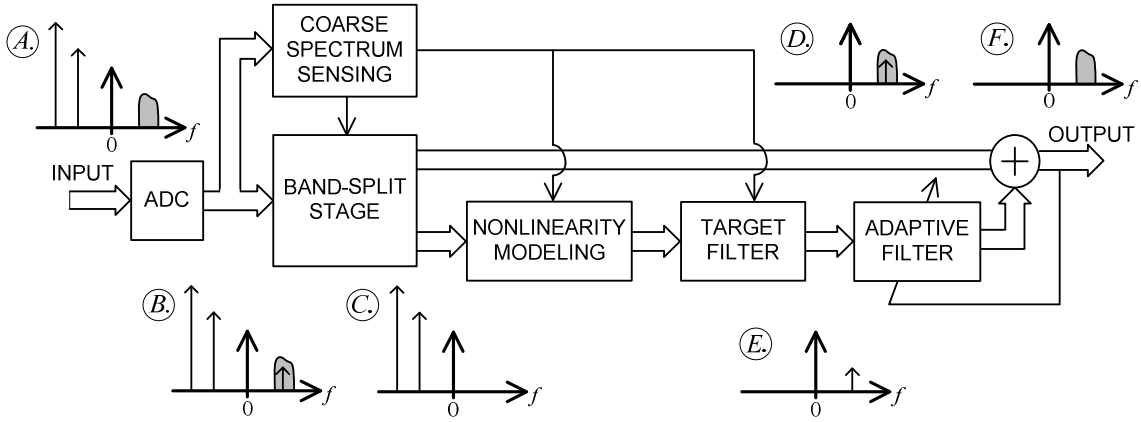

Figure 4.6. *Adaptive interference cancellation principle for reducing nonlinear distortion with digital post-processing.*

After the band-split stage, the target is to regenerate the interference at the weak signal band. This is done by modeling the nonlinearity by using, e.g., polynomial signal processing for the reference signal containing the interfering signal components. Equation for the polynomial or other nonlinear function highly depends on the application. The most important things to consider here are the form of the interference and from which frequencies the interference is originating. These affect the powers used in the polynomial model. For instance, if third-order distortion is wanted to be removed, then the reference signal is raised to the power of three. Correspondingly, whatever more complex signal alteration can be used to recreate the distortion. In practice, either parallel or serial processing can be used. Parallel processing requires more computational resources since it uses several processing branches at the same time. Each branch processes different order distortion and has its own adaptive filter coefficients. In the serial version only a single processing branch is used but there can be several processing cycles to cancel the different distortion orders. This may decrease the need for computational resources but increases the processing delay. Generally, the performance difference between the parallel and serial implementations is dependent on the used computer architecture. The target filter mentioned in Figure 4.6 is used after the nonlinearity modeling to extract only the distortion at the weak signal band. Spectrum figure *E* illustrates the reference signal after the target filter and only the regenerated intermodulation component is seen there.

Before the adaptive filter depicted in Figure 4.6, there is the weak signal with interference in the upper branch and only the interference in the reference signal of the lower branch. Now the coefficients of the adaptive filter are tuned in such a manner that the interference is subtracted from the weak signal band as perfectly as possible. The most apparent solution for coefficient optimization is to use least mean squares (LMS) algorithm for minimizing the interference power at the weak signal band. Due to the simple implementation of LMS, it is adequate choice for real-time systems. When the LMS algorithm has converged and the interference has been subtracted, there is ideally only the wanted weak signal without interference in the output. This is illustrated with spectrum figure *F* in Figure 4.6. The suitable number of adaptive filter coefficients depends on the application. If the distortion signal is generated accurately enough, it is usually adequate to use a single-tap adaptive filter in ADC applications. That is because the proper scaling of the reference signal is enough. Using more coefficients can help shap-

ing the reference signal to better match with the distortion on the weak signal band. Another example of using several coefficients is to compensate memory effects in power amplifiers [38]. Performance examples of the AIC method are presented in Chapter 5.

There is also possibility to use an outer-loop control mechanism which is called coarse spectrum sensing. It measures spectrum density of the digital signal from the ADC. This is performed for signal blocks with predefined length by using, for example, FFT. The information is then used to control band-split filter properties so that the weakest signal band or bands are selected for the interference cancellation. Furthermore, the spectrum sensing is needed to locate the strongest blocker signals. It can be then used to select distortion orders used in the polynomial signal processing stage. Naturally, the target filter properties have to be controlled also according to the location of weak signal band(s).

4.2.2. Utilization for Clipping Compensation

Signal clipping in the ADC essentially produces odd-order nonlinear distortion as shown in Section 4.1. From the nonlinearity modeling point of view that means non-zero weights only for the odd orders in the Equation (4.17). In practice third, fifth and seventh order distortion are the strongest and thus compensating these would remove most of the interference.

The adaptive interference cancellation principle relies on the assumption that the interference part of the signal, from where the reference signal is generated, is not distorted or contains only mild distortion. Unfortunately, this is not the case for a heavily clipped signal. Therefore the generated reference signal would contain additional interference that doesn’t match with the interference to be removed from the weak signal band.

One powerful solution for bypassing the reference signal distortion problem in AIC is presented in Figure 4.7. This modified AIC principle exploits two analog-to-digital converters. First one is the main ADC and the second one is used to create the reference signal. The latter converter can have lower resolution than the main ADC and is therefore rather cheap to include. The idea is to avoid clipping in the second ADC by using constant attenuation (with respect to the main ADC) when feeding the input signal. The appropriate attenuation can be, e.g., between 10 and 20 dB so that it is possible to digitize strong blocker signals intact. The weak signal bands don’t have to be concerned here

because the main ADC is taking care of those. Performance of this method is illustrated in Chapter 5.

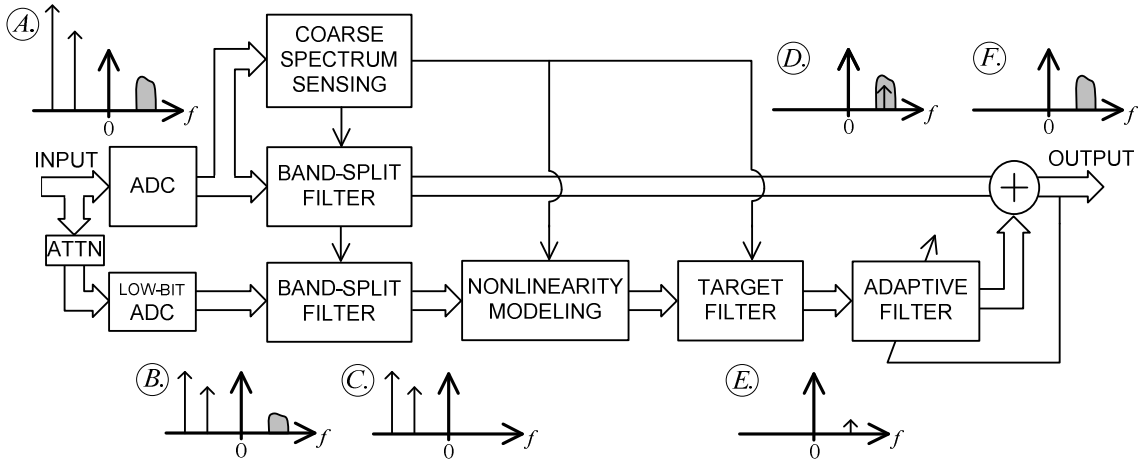

Figure 4.7. *Adaptive interference cancellation principle using two ADCs: attenuated version of the input signal is fed to the low-bit ADC to avoid clipping and thus non-distorted version of the blocker signal can be acquired for post-processing purposes.*

4.2.3. Utilization for INL Compensation

A practical way to visualize INL error is to present it as a function of digital output codes. From the curve like that it's easy to see what kind of correlation the INL error has between different quantization levels. It is a common practice to include a typical INL error curve to the data sheet of ADC. Figure 4.8 presents an example of INL error curve for a commercial 10-bit ADC. Although the structure of the INL error curve may vary considerably between different types of converters, it is never purely random. For example in Figure 4.8, the correlation between consecutive output codes is clearly visible.

For more detailed analysis, N. Björsell and P. Händel [11] have modeled the INL error to consist of three parts. The model is

$$INL\big(T[k]\big) = INL_{HCF}\big(T[k]\big) + INL_{LCF}\big(T[k]\big) + INL_{noise}\big(T[k]\big), \qquad (4.18)$$

where $T[k]$ is the kth code transition level. The low code frequency (LCF) component $INL_{LCF}\,(T[k])$ is the slowly varying fluctuation that can be seen in Figure 4.8. Correspondingly the high code frequency (HCF) component $INL_{HCF}\,(T[k])$ describes the rapid variations (architecture dependent) on top of the LCF component. These are usually modeled as piecewise linear. The rest of the INL error is random variations and this is modeled with noise component called $INL_{noise}\,(T[k])$. [11]

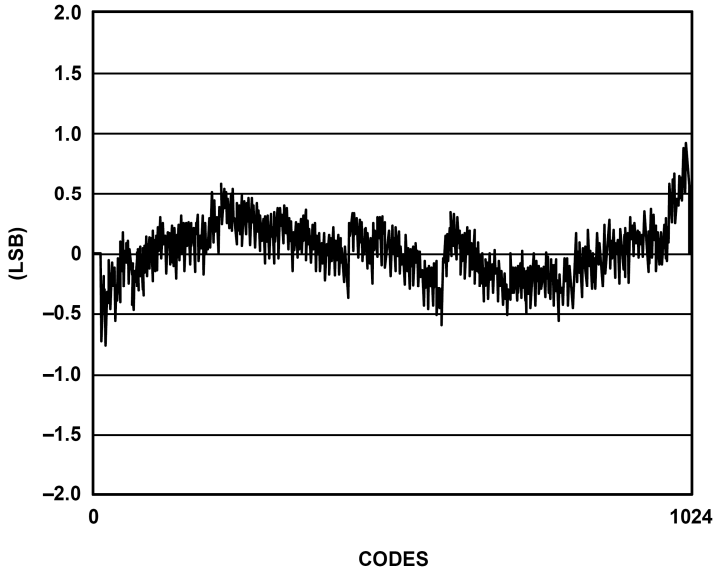

Figure 4.8. *Typical measured INL error curve as a function of digital output code for the 10-bit analog-to-digital converter AD9218 [4].*

The low code frequency component of INL error usually has more or less polynomial shape and therefore it generates mainly low-order nonlinear distortion. Even though the INL error is typically only in the order of a few LSBs, it may have significant effect in wideband applications. The INL error of a few LSBs is enough to generate noticeable distortion to weak signal bands, if strong blocking signals are present. The adaptive interference cancellation principle can be used to mitigate the effect of the LCF component. In order to minimize the number of powers to be used in the AIC some sort of calibration scheme is needed. That is because the polynomial shape of the LCF can vary considerably between different ADCs and especially between different types of ADCs. Performance example of INL mitigation with the AIC method is presented in Section 5.2.

4.3. Clipping Compensation with Interpolation

Interpolation is probably the first solution that comes to one's mind when talking about enhancing a clipped waveform. Especially, if the clipping happens in a radio receiver and thus the information about clipping distortion is very limited. In this case, for example, the clipping level would not be known. Due to the lack of information, there are various interpolation approaches whose accuracy is more or less the same. Real differences appear when the computational complexity is taken into account. In general, this section presents one specific application exploiting multirate signal processing and polyphase structures. An introduction to these topics are given, e.g., in [18].

This proposed interpolation method assumes that the signal is band limited when fed to the input of an analog-to-digital converter. The ADC itself must oversample the signal and the oversampling factor is here denoted by L. After the analog-to-digital conversion, the oversampled signal is uniformly divided to L different branches to form a so-called polyphase decomposition. This is illustrated in Figure 4.9 with a block diagram. Once the polyphase decomposition is formed, the signal is filtered using the branch filters. The fundamental idea of this filtering is to get an estimate for the clipped sample in one branch exploiting the samples in other branches. There are many suitable options for designing these branch filters and a simple but rather efficient solution is proposed here.

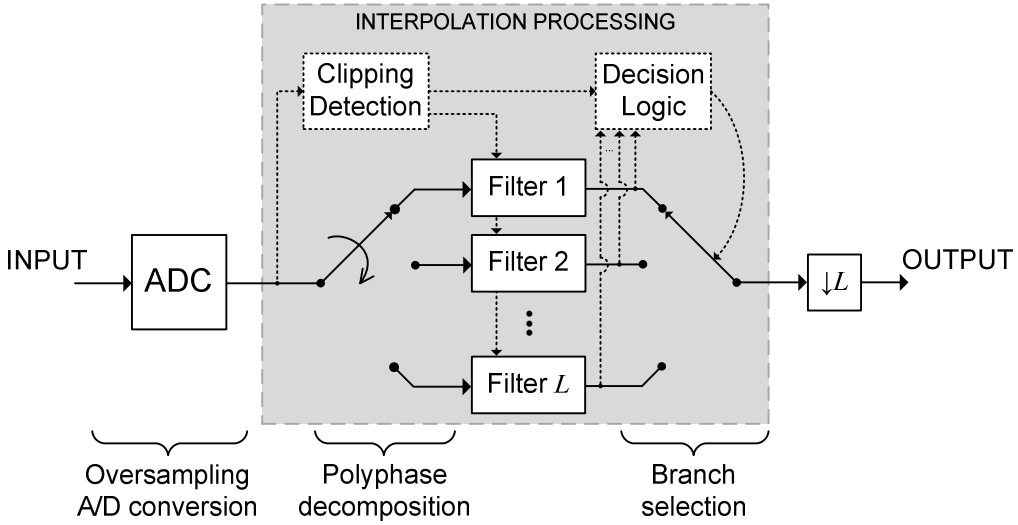

Figure 4.9. *Block diagram of the proposed interpolation scheme for a signal with the oversampling factor L. After the oversampling ADC, a polyphase decomposition of the signal is created and then, once filtered, the decision logic chooses, sample by sample, the best branch for the output. The clipping detection control changes the order of the branch filters according to the position of the clipped sample.*

One way to design the branch filters is creating a low-pass FIR filter with a pass-band corresponding to the bandwidth of the useful signal band. So this is essentially the same approach as is usually used in designing a basic decimation filter. The branch filters are created by simply making a polyphase decomposition of the impulse response of the FIR filter. If the overall impulse response is denoted with $h(n)$, then the branch filters are

$$\begin{aligned} h_0(n) &= \{h(0), h(L), h(2L), ...\} \\ h_1(n) &= \{h(1), h(L+1), h(2L+1), ...\} \\ &\vdots \\ h_{L-1}(n) &= \{h(L-1), h(2L-1), h(3L-1), ...\}. \end{aligned} \tag{4.19}$$

These branch filters are assigned to different branches according to the knowledge about the branch in which the clipped sample to be interpolated is located. For example, if the clipped sample is in the first (top) branch, which is illustrated in Figure 4.9, filters 1, 2, …, L are $h_0(n), h_1(n), ..., h_{L-1}(n)$, respectively. Whereas a clipped sample in the second branch would mean the filters 1, 2, …, L to be $h_{L-1}(n), h_0(n), h_1(n), ..., h_{L-2}(n)$, respectively. At the time instances when there are no clipped samples to be interpolated, the filtering is not necessarily required and this way the amount of computation can be reduced. It is also worth noticing that the outcome of the filter $h_0(n)$ doesn't have to be calculated when there is a clipped sample, because it is always replaced with the better estimate from the other branches.

One of the most important things in the interpolation scheme is the logic for selecting the best estimate for the clipped sample among all the branches. Here two different kinds of approaches are proposed. The first selection method is choosing always the branch which gives the biggest absolute value for the clipped sample and it is called here as *maximum method*. It requires calculating estimates with $L-1$ different filters and still only one of these estimates is eventually used. On the other hand, this method is likely to provide good estimates without the need for numerous iteration cycles. Another proposal for the selection logic is based on weights calculated for every branch and thus it is called as *weighting method*. The weight is determined by first multiplying every tap value in the branch filter impulse response with *0* or *1* according to if the tap corresponds to a non-clipped or clipped sample on the input signal, respectively. Then all of these products are summed together to provide the weight for the branch. The detection logic then chooses the branch which has the lowest weight. In other words, this means selecting the branch which is least affected by the clipped samples and hence provides the best estimate. In both of these aforementioned methods, it is good to check that the sample estimate is bigger than the clipping level. If it's not, the best output value would be the original clipped sample.

In the proposed interpolation scheme, the sampling rate is kept unchanged until the very end. That is because it's possible to iterate the filtering process several times in

order to achieve better interpolation results. After a sufficient number of iterations have been carried out, the sampling rate of the interpolated signal can be reduced with factor L. This is also illustrated on the right side of Figure 4.9.

The aim of this section is to propose a more efficient interpolation solution for the clipping compensation in the radio receivers than currently exists in the literature. Although, it is worth noticing that filter designing is not the focus of this thesis. Therefore, it is highly probable that more efficient filter structures exist for this purpose. One possibility would be to design individually proper all-pass filters for every branch. That is because the fractional delay is the key issue here and not the low-pass filtering of the overall signal. After all, the signal was assumed to be initially band limited.

T. Tomioka *et al.* [37] have proposed, to some extent, similar type of interpolation method as is described in this section. Tomioka's method was also shortly described in Subsection 2.5.2. One of the main differences is the interpolation filter. Tomioka *et al.* have used a sinc filter, which would be an optimal interpolation filter if the impulse response is infinitely long. In practice, the sinc impulse response has to be truncated to a very limited length. Therefore, the stop-band attenuation gets worse and the truncation also causes ripple in the pass-band and stop-band of the sinc frequency response. These filter design issues are considered, e.g., in [42]. The problems can be relieved by designing the interpolation filters using more optimal methods just as has been done in this thesis. Consequently, shorter filters can be used and still the filters can have better properties than the truncated sinc.

5. PERFORMANCE EXPERIMENTS

This chapter is devoted for giving concrete performance examples of the post-processing methods proposed in this thesis. This includes the AIC method and two different interpolation schemes. Here the AIC method is considered for compensating clipping distortion as well as effects of INL errors in case of a wideband analog-to-digital conversion where several separate signals with different center frequencies are digitized. The proposed interpolation schemes are only applicable for the clipping compensation.

Section 5.1 compares performance of the different implementations of AIC and interpolation methods, using both computer simulations and laboratory radio signal measurements, for reducing clipping distortion. After that, Section 5.2 demonstrates the performance of the AIC method for mitigating nonlinear distortion due to INL errors.

5.1. Clipping Compensation

A test signal for clipping compensation purposes is constructed so that it simulates a potential situation in a wideband radio receiver where several signals at different center frequencies are digitized as a whole. The test signal is also designed to demonstrate, as clearly as possible, consequences of the clipping phenomenon and also the performance of the compensation algorithms. It is here assumed that the overall signal is downconverted to the baseband prior to the analog-to-digital conversion. Therefore, individual signal bands have reasonably low center frequencies.

Figure 5.1 illustrates the power spectrum of the complex test signal which consists of five separate frequency bands and added white Gaussian noise. All five frequency bands contain single-carrier communication signals, which are QPSK-modulated and pulse-shaped with raised cosine filters. The signals have different bandwidths, and therefore symbol rates, to ensure that they are not correlating with each other. The overall test signal has a sampling rate of 64 MHz but only frequencies from -8 MHz to 8 MHz are used as shown in Figure 5.1. The sampling rate refers to both the original

sampling rate used in MATLAB when creating the test signal and the sampling rate used in the analog-to-digital conversion. This means that the test signal has oversampling factor of four, which is required in order to use the interpolation method proposed in Section 4.3. Although oversampling in the analog-to-digital conversion process is not really needed in the AIC method, the same oversampled test signal is used to ease the comparison between the different compensation methods.

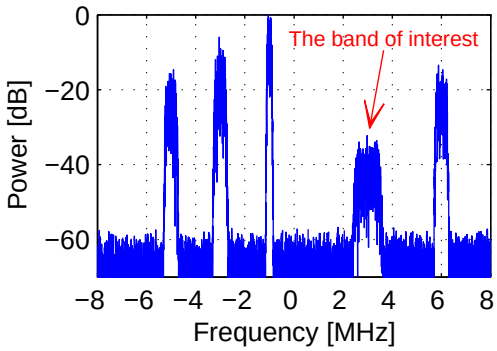

Figure 5.1. *Power spectrum of the complex test signal used in the clipping compensation studies. The signal contains five separate frequency bands with QPSK-modulated single-carrier signals within frequencies from -8 MHz to 8 MHz. Overall sampling frequency is 64 MHz to provide the oversampling factor of four.*

Not only the bandwidths but also the power levels of the five signal bands are different as can be seen in Figure 5.1. Naturally, this would be the case also in an actual radio receiver when all the signals are not controlled by the same communication system. In the case of this particular test signal, the weak signal at 3 MHz is chosen to be the band of interest. This frequency band is used to assess concrete performance of the different compensation methods. The performance is measured by calculating signal-to-noise-and-distortion ratio (SNDR) in the band of interest before and after applying compensation methods for the clipped test signal. For a distorted (e.g. clipped) signal the SNDR is calculated by using average powers so that

$$SNDR = 10\log_{10}\frac{\frac{1}{N}\sum_{n=1}^{N}\left|s_f(n)-\overline{s}_f\right|^2}{\frac{1}{N}\sum_{n=1}^{N}\left|\left(y_f(n)-\overline{y}_f\right)-\left(s_f(n)-\overline{s}_f\right)\right|^2}, \tag{5.1}$$

where N is the signal length, $s_f(n)$ is a filtered version of the ideal test signal (shown in Figure 5.1) containing only the frequency band around 3 MHz and $y_f(n)$ is a filtered version of the distorted signal containing the same frequency band. Furthermore, means

of $s_f(n)$ and $y_f(n)$ are denoted with $\overline{s}_f$ and $\overline{y}_f$, respectively. Special awareness is needed when comparing the signal powers to calculate SNDR in laboratory measurements because signal levels may be different before and after the measurement. This is discussed in more detail in Subsection 5.1.4. Another performance metric is bit error rate (BER) which is calculated by detecting the signal at 3 MHz and comparing the received bits with the correct bit sequence. Only so-called raw BERs are considered here, i.e., error correction coding is not taken into account.

For clarification, details of the test signal are collected in Table 5.1. The length of the test signal is somewhat an arbitrary choice to achieve convenient simulation times and a sufficient number of clipped peaks. In order to acquire more reliable results a large number of individual random realizations of the same signal are averaged (500 for simulations and 20 for laboratory measurements).

Table 5.1. *Summary of properties for the test signal employed in illustrating clipping compensation performance.*

Sampling frequency	64 MHz
Center frequencies	-5 MHz, -3 MHz, -1 MHz, 3 MHz, 6 MHz
Relative powers	-15 dB, -10 dB, 0 dB, -35 dB, -15 dB
Modulation	QPSK (for all five single-carrier signals)
Signal length	30,720 samples
PAPR (I branch)	9.7 dB

The peak-to-average power ratio shown in Table 5.1 is averaged over 500 random realizations of the test signal and although the test signal is complex, the PAPR is calculated only for the I branch. It is more illustrative number than PAPR of the whole complex signal when examining the performance examples discussed in the following subsections. That is because I and Q branches are digitized separately and hence it's convenient to compare the clipping level with the PAPR of the same branch in order to get an impression how severe the clipping essentially is. The clipping level (CL) is defined in these performance examples as a number of dB's over the average power level of the signal, i.e.,

$$CL = 10\log_{10}\left(\frac{V_0^2}{P_{\text{avg}}}\right), \tag{5.2}$$

where V_0 is the absolute clipping level and P_{avg} is the average power of the signal.

5.1.1. Adaptive Interference Cancellation

This first performance example is conducted by using MATLAB simulations. The test signal described earlier is quantized with an ideal 10-bit ADC and the power level of the test signal in the input of the ADC is set so that the signal is clipped in the conversion process. Ideal quantization is used in order to emphasize only the clipping behavior among quantization noise.

The power spectrum of the test signal after the ADC, when clipping level is 5 dB, is shown in Figure 5.2 a). Distortion due to clipping is clearly visible when compared to the ideal signal spectrum in Figure 5.1. In addition, the time domain behavior of the ideal and clipped waveforms is illustrated in Figure 5.2 b) so that it can be seen in practice how much the clipping level of 5 dB limits the signal in this case. When considering the weak signal band located around 3 MHz, most of the nonlinear distortion is originating from the strong signal band with center frequency of -1 MHz.

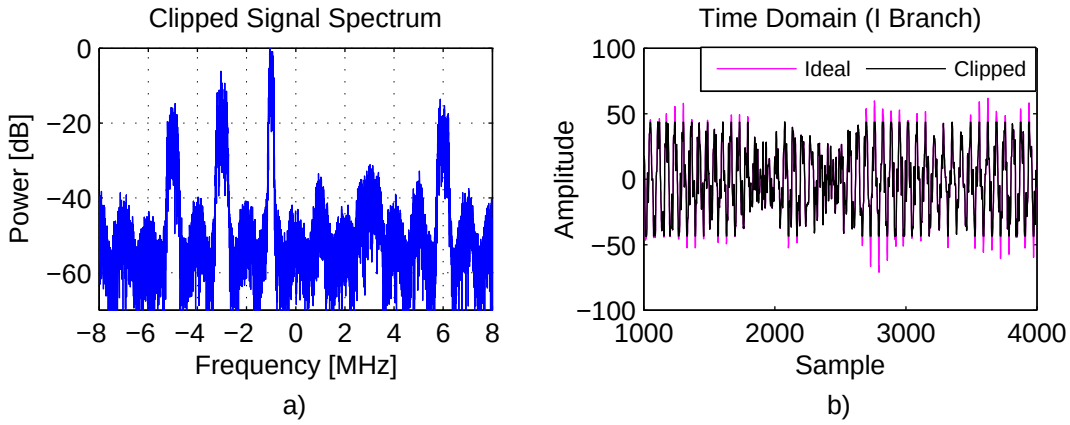

Figure 5.2. *The test signal after an ideal 10-bit ADC, when clipping level is 5 dB, illustrated a) in frequency domain and b) in time domain.*

The AIC method implemented in MATLAB according to Subsection 4.2.1 is applied to the clipped signal in order to remove the interference from the weak signal band. Although the third-order distortion is dominating, also the fifth and the seventh order distortions are cancelled consecutively. In the adaptive filter stage of the AIC method, only a single-tap is used for each stage, i.e., scaling only rather than filtering and the LMS algorithm is used for determining the coefficients. Figure 5.3 shows the constellation of the signal demodulated from the weak signal band at 3 MHz before and after applying AIC. It is clearly visible from the constellations that AIC can significantly reduce nonlinear distortion in the weak signal band. Inband SNDR is enhanced by

3.45 dB and BER for the QPSK signal is decreased from 0.07 to 0.02. The most limiting matter for the performance of the AIC method is the purity of the reference signal. There is a considerable amount of nonlinear distortion also outside the band of interest, i.e., the part of the spectrum for the reference signal generation. Therefore, the regenerated distortion used in AIC doesn't match exactly to the distortion at the band of interest.

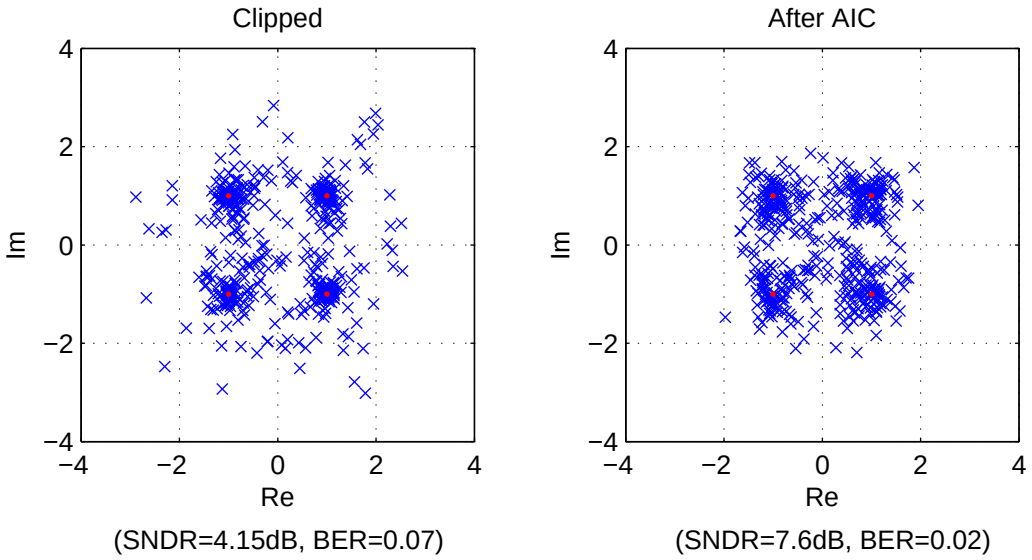

Figure 5.3. *Constellations of the QPSK signal demodulated from the weak signal band located around 3 MHz without and with AIC.*

The LMS adaptation of the adaptive filter coefficients for the aforementioned example case is illustrated in Figure 5.4. The interference cancellation is here performed consecutively for the different distortion orders, i.e., after removing third-order distortion the adaptive filter finds coefficients for the fifth order and then for the seventh order. It can be concluded from Figure 5.4 that after removing third-order distortion there is not much distortion left and thus the fifth and seventh-order coefficients are very similar.

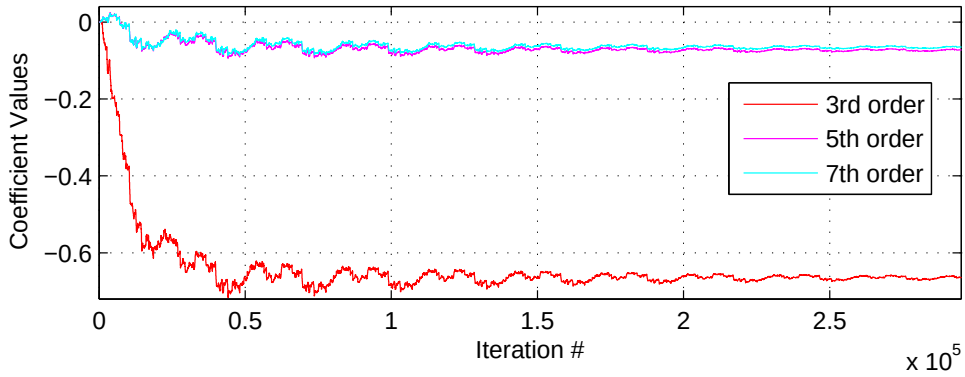

Figure 5.4. *LMS adaptation of the adaptive filter coefficients for the I branch.*

In case of clipping, the performance of the AIC method can be enhanced by using two ADCs as proposed in Subsection 4.2.2. This example employs an ideal 10-bit ADC as a main converter and an ideal 5-bit ADC as a secondary converter with 10-dB attenuation in its input. Here, the attenuation is sufficient to prevent the test signal from clipping. Figure 5.5 represents the constellation of the QPSK signal demodulated from the weak signal band at 3 MHz after the AIC exploiting two ADCs. It can be seen that the performance of the AIC is undoubtedly enhanced due to the more accurate distortion regeneration. SNDR is improved by 7.35 dB compared to the unprocessed signal and 3.9 dB compared to the original AIC method in Figure 5.3. Naturally, BER is also decreased more when AIC with two ADCs is used.

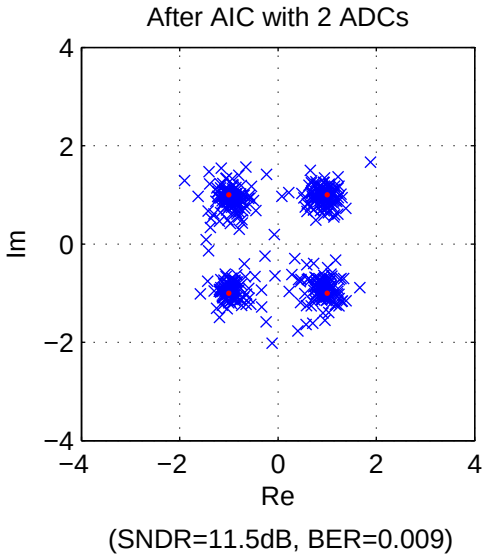

Figure 5.5. *The constellation of the QPSK signal demodulated from the weak signal band located around 3 MHz when using AIC with two ADCs. The low-bit ADC employed in the reference signal branch has a resolution of 5 bits and 10-dB input attenuation.*

When using AIC with two ADCs, one interesting question is how much the resolution of the secondary ADC affects the performance of the AIC method. It should be taken into consideration that, if the analog input voltage range is the same for both the main ADC and the secondary ADC, all the quantization levels of the secondary ADC are not usually used. That is because the automatic gain control is trying to match the received signal for the input voltage range of the main ADC but there is the reasonably large constant attenuation placed in the input of the secondary ADC. For the previously described test signal, the performance of AIC is illustrated as a function of the resolution of the secondary ADC in Figure 5.6. The results are averaged over 500 different

random realizations of the test signal as it is the case for all the MATLAB simulation based performance curves in this chapter. The performance metrics are illustrated for the clipping levels of 4 dB and 6 dB (in the main ADC) to give a wider view than a single example would provide. It can be concluded from Figure 5.6 that four or less bits in the secondary ADC is not adequate. This is stemming from the fact that there aren't enough quantization levels in use to express the signal precisely enough. When there are five or more bits in the secondary ADC, the performance is almost the same regardless of the number of bits. This is a concrete proof for the claim that the secondary ADC can have a low resolution and is still able to considerably enhance the post-processing performance.

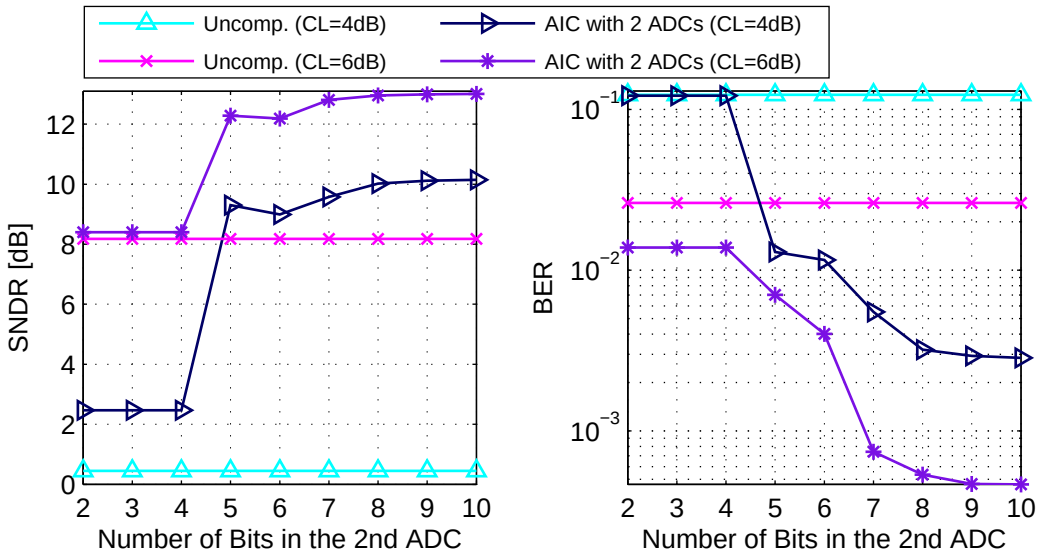

Figure 5.6. *Simulation example of how the resolution of the secondary ADC (with 10-dB input attenuation) affects to the overall performance of AIC. The SNDR and BER values are acquired from the QPSK signal demodulated from the weak signal band located around 3 MHz.*

One general parameter that affects the performance of the AIC method is the processing block length. It essentially has a trade-off, i.e., a shorter block length means more agile response to the time-variant properties of the signal behavior but a longer block length gives more data for the LMS algorithm and hence it is more likely to converge to a more optimal value. Moreover, the longer block length requires more memory and increases the processing delay in the receiver. Figure 5.7 illustrates the impact of the processing block length to the overall performance of AIC for the clipping levels of 4 dB and 6 dB considering both the original AIC method and the one with two ADCs. The processing block length is varied from 10 samples to the length of the test signal.

The performance improves as a function of the processing block length but due to the saturation it can be concluded that the practical value for the block length is between 1,000 and 5,000 samples.

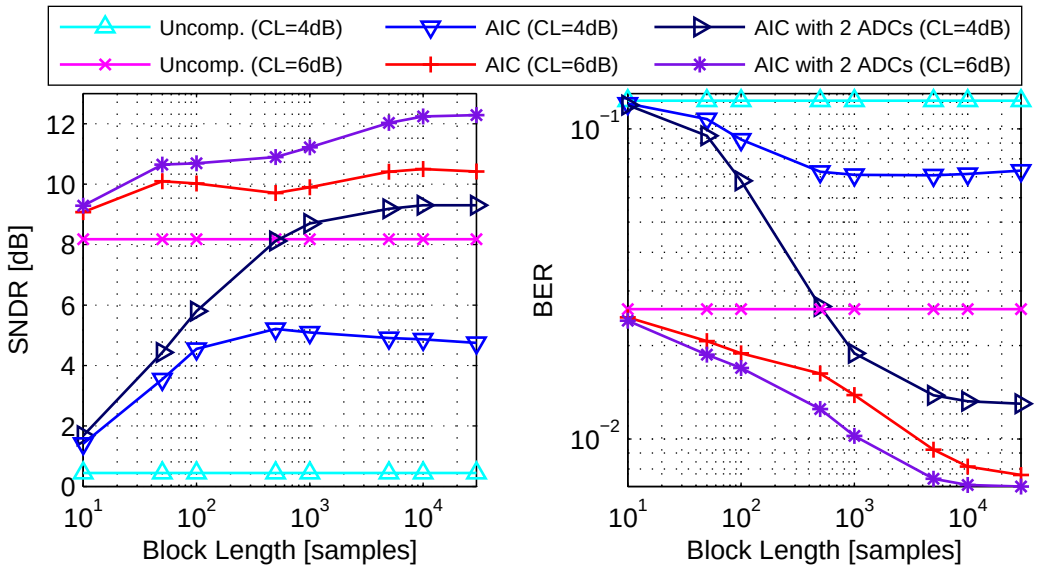

Figure 5.7. *Simulation example of the AIC performance for clipping levels 4 dB and 6 dB when the processing block length is varied. Both the original AIC method and the AIC method with two ADCs are considered. The latter method employs a secondary ADC with the resolution of 5 bits.*

It was mentioned in Subsection 4.2.1 that in some applications the performance of AIC can be improved by using multi-tap adaptive filters. Clipping is an instantaneous phenomenon and thus it doesn't have memory. Therefore, single-tap filters should be sufficient and, in fact, this is shown in Figure 5.8 by simulating the AIC performance as function of the number of taps in the adaptive filter stage. The number of taps here indicates the number of taps for the single distortion order being cancelled and the overall performance is illustrated in Figure 5.8 after canceling third, fifth and seventh order distortion. There can be small variations in SNDR and BER for a single block of data when using different number of taps, but if the results are averaged over several (here 500) random realizations of the test signal, it is clear that the number of taps in the adaptive filter stage does not have practically any effect in case of clipping.

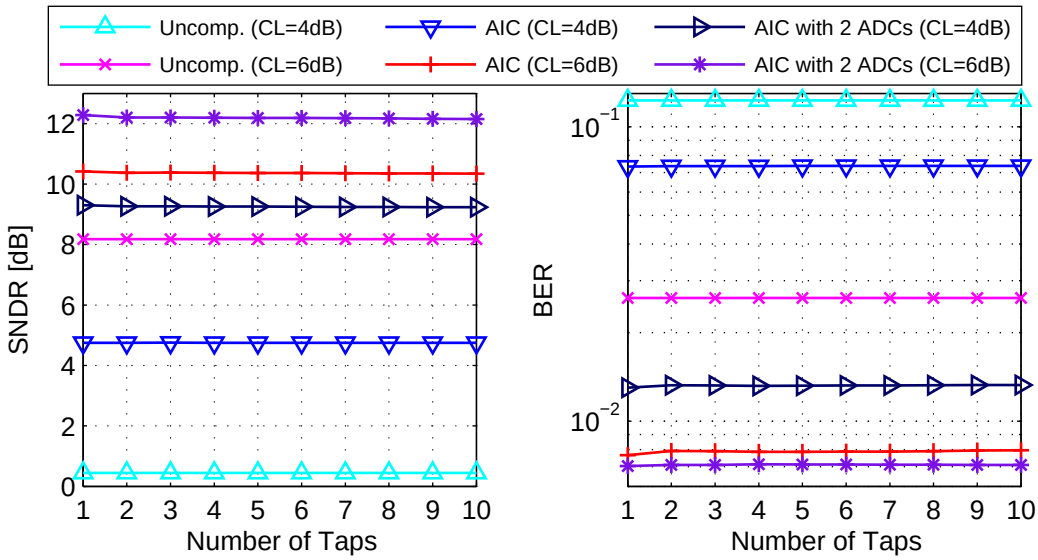

Figure 5.8. *Simulation example of the AIC performance for the clipping levels 4 dB and 6 dB with different number of taps in the adaptive filter stage. Both the original AIC method and the AIC method with two ADCs are considered. The latter method employs a secondary ADC with the resolution of 5 bits.*

5.1.2. Interpolation

This MATLAB simulation example demonstrates the performance of different interpolation techniques for reducing clipping distortion. Two interpolation schemes are proposed in Section 4.3 and their performance is here compared with the interpolation method proposed by T. Tomioka *et al.* [37]. Tomioka's method is also shortly described in Subsection 2.5.2. Here, the interpolation scheme that always chooses the largest branch filter output value (by absolute value) is called the *maximum method*. Correspondingly, the interpolation scheme that chooses the polyphase branch based on the number of clipped samples and their influence on reliability is called the *weighting method*.

In all the interpolation examples shown in this thesis, the maximum method and the weighting method are implemented with branch filters of length 32 taps. The branch filters are formed as polyphase components of a fourth-band FIR low-pass filter that has a length of 128 taps and its pass-band has a width of $\frac{1}{4}$ in proportion to the half of the sampling frequency. These are stemming from the fact that the test signal has oversampling factor of four. As proposed in [37], Tomioka's method was implemented with 128-tap sinc filters.

As in the AIC case, this simulation example employs an ideal 10-bit ADC to digitize the test signal and the signal power in the input of the ADC is adjusted so that the clipping level is 5 dB. After that, the maximum method is used for interpolating the clipped

signal. In order to achieve better results, two iterations of the interpolation are used here, i.e., every block of data is processed twice in the interpolation stage (see Figure 4.9). In Figure 5.9 a) the spectra of the ideal, the clipped and the interpolated signals are shown for this example. Correspondingly, Figure 5.9 b) illustrates the same signals in time domain. It can be concluded from the figures that the proposed interpolation method is able to reconstruct the time domain waveform relatively well and this can be seen as a decreased interference level in the spectrum.

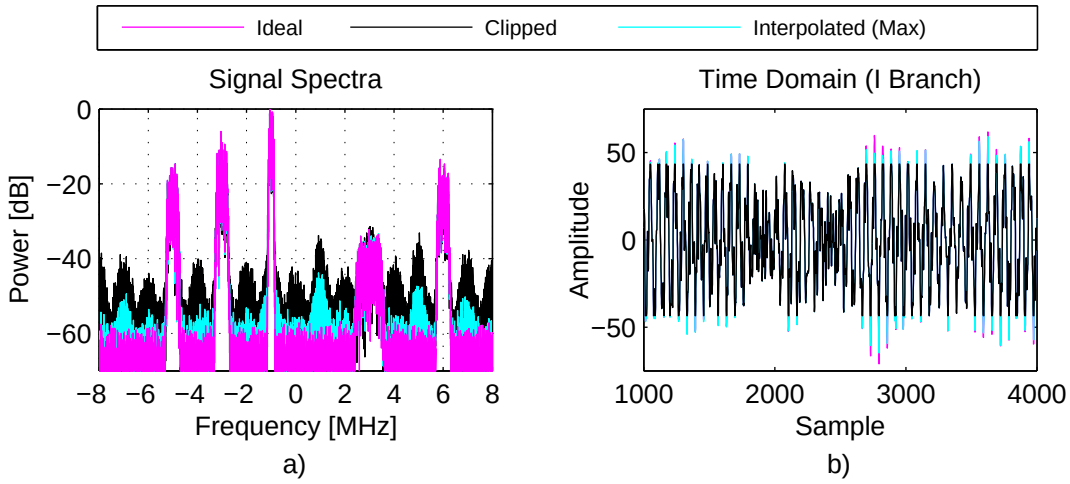

Figure 5.9. *The test signal before and after an ideal 10-bit ADC, when the clipping level is 5 dB, as well as after two iterations of interpolation with the maximum method illustrated a) in frequency domain and b) in time domain.*

Figure 5.10 concentrates on the weak signal band at 3 MHz by illustrating the constellation of the demodulated signal. This constellation can be compared with the cases in Figure 5.3 and Figure 5.5. SNDR is improved by 10.15 dB compared to the clipped signal without any post-processing. In this particular example, there is clearly less interference after the interpolation than there is after the AIC method. However, final conclusions can't be drawn based on this single experiment and hence more extensive studies are given here.

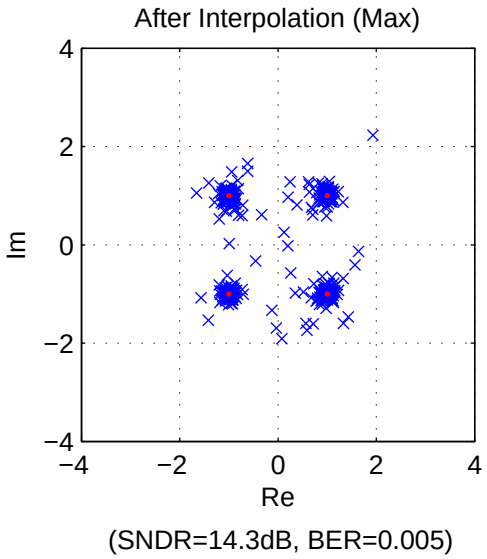

Figure 5.10. *The constellation of the QPSK signal demodulated from the weak signal band located around 3 MHz after two iterations of interpolation with the maximum method.*

All three interpolation methods which are considered in this section can be used in iterative manner. The number of iterations affects the required amount of computation and also to the processing delay. On the other hand, the amount of clipping distortion might reduce significantly, if the number of iterations is increased. This is demonstrated in Figure 5.11, where the interpolation performance is plotted as a function of the number of iterations. In this example, the clipping level is 6 dB for the test signal being digitized. As can be seen from the figures, there are substantial differences between the interpolation methods. The maximum method shows excellent performance with a low number of iterations, but on the other hand there is no guarantee that it will converge. The performance degradation, when using high number of iterations, is a consequence of the new values for the clipped samples that are getting higher than the ideal values (i.e. overshooting). The other two methods both converge, however the weighting method requires more iterations, but eventually it will outperform Tomioka's in this simulation example. Note that the maximum method and the weighting method don't employ a polynomial pre-interpolation stage as Tomioka's method does. The additional interpolation stage obviously requires more computations, but on the other hand it may increase the performance considerably [37].

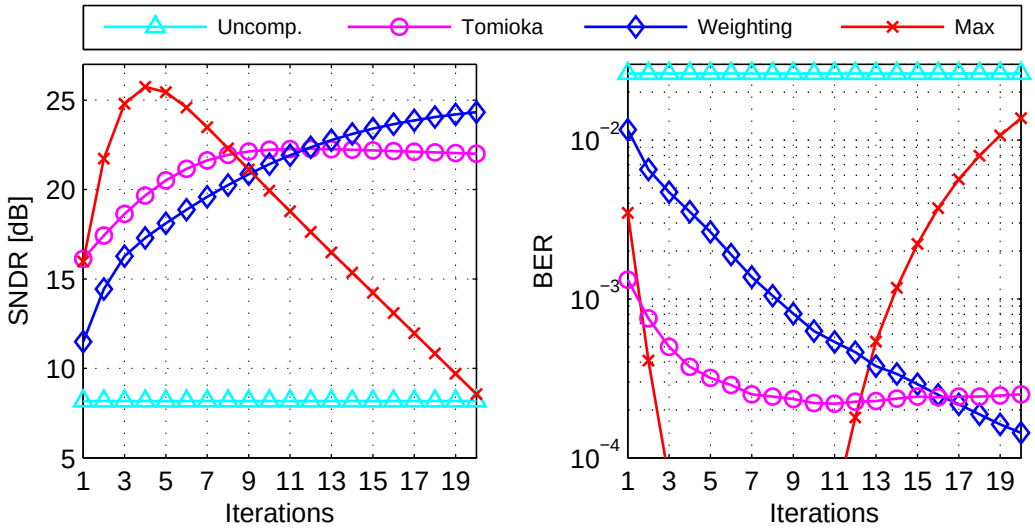

Figure 5.11. *Simulation example of how the number of iterations in the interpolation stage affects to the overall post-processing performance. The clipping level in the simulation is 6 dB and the results are acquired from the QPSK signal demodulated from the weak signal band located around 3 MHz.*

When the clipping level in the previous example is changed to 4 dB, the behavior of the different interpolation methods is similar to a certain extent. The results are presented in Figure 5.12. The stronger clipping affects the performance of the weighting method so that it requires more iterations to converge. Also the maximum method requires more iterations in this case, but with low number of iterations it still does better than the other methods. The fundamental reason for the poorer performance in the case of stronger clipping is the higher number of clipped samples involved in the interpolation process. In other words, the estimation accuracy of the interpolation scheme is decreased, if there are more than $L-1$ consecutive clipped samples. Additionally, it can be concluded from Figure 5.12 that for the maximum method and Tomioka's method a few iterations are sufficient, despite the fact that the peak performance is not achieved – at least not in the case of very heavy clipping.

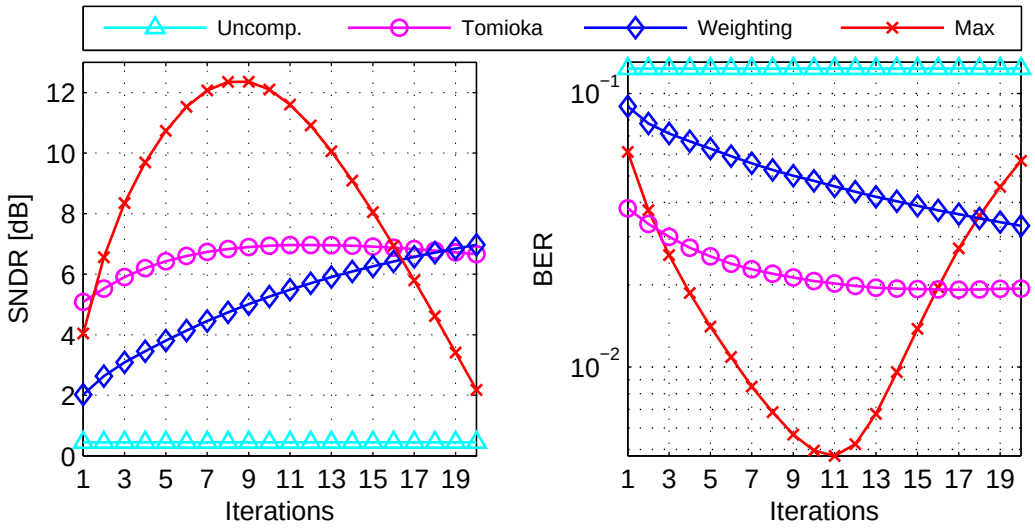

Figure 5.12. *Simulation example of how the number of iterations in the interpolation stage affects to the overall post-processing performance. The clipping level in the simulation is 4 dB and the results are acquired from the QPSK signal demodulated from the weak signal band located around 3 MHz.*

5.1.3. Comparison

In this subsection, all the discussed clipping compensation schemes, both AIC and interpolation based, are compared together. This is carried out with computer simulations where the clipping level for the test signal is varied in the 10-bit ideal analog-to-digital conversion and then both SNDR and BER values are calculated for the weak QPSK signal located at the center frequency of 3 MHz.

For the original AIC method and AIC with two ADCs, the results are illustrated in Figure 5.13. Based on the definition of the clipping level and the PAPR of the test signal (9.7 dB for the I branch), it is possible to say that the clipping level of 1 dB means very heavy clipping, whereas 10-dB clipping level indicates that clipping occurs rarely. It can be seen that the secondary ADC is most useful when the clipping level is below 6 dB. This is logical since under heavy clipping the overall distortion level is higher and thus prevents the proper regeneration of the distortion in the weak signal band. The problem can be bypassed with the help of the secondary ADC which, according to Figure 5.13, can give over 5-dB gain for SNDR. On the other hand, the original AIC approach outperforms the AIC method with two ADCs, if there is only mild clipping. This is stemming from the fact that the secondary ADC has only 5-bit resolution, which cannot provide as good reference signal as the main ADC with its 10-bit resolution. In addition, one important thing to notice is that AIC should not be used, if there is very mild

clipping or no clipping at all. In practice, it is important to set a proper threshold level for whether to use AIC or not in order to decrease the power consumption of the receiver.

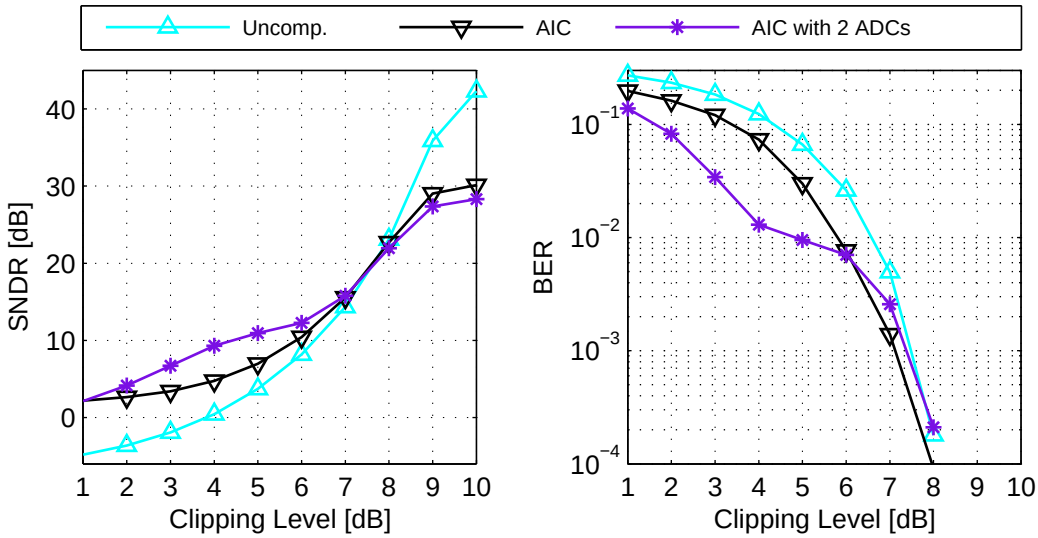

Figure 5.13. *Simulation example of the AIC performance as a function of clipping level. Both the original AIC method and the AIC with two ADCs are considered. The latter method employs a secondary ADC with the resolution of 5 bits.*

In a similar manner, Figure 5.14 gives the simulation results for the different interpolation schemes. In the interpolation stage, two iterations are used for every block of data. In this example, the maximum method gives somewhat better results than the other interpolation schemes from the SNDR point of view. When comparing the results in Figure 5.13 and Figure 5.14, it can be concluded that AIC is better in case of heavy clipping, but with milder clipping levels the interpolation is better approach. The performance results of the interpolation schemes can be further improved by using more iterations, but it increases computational complexity or make processing delays longer.

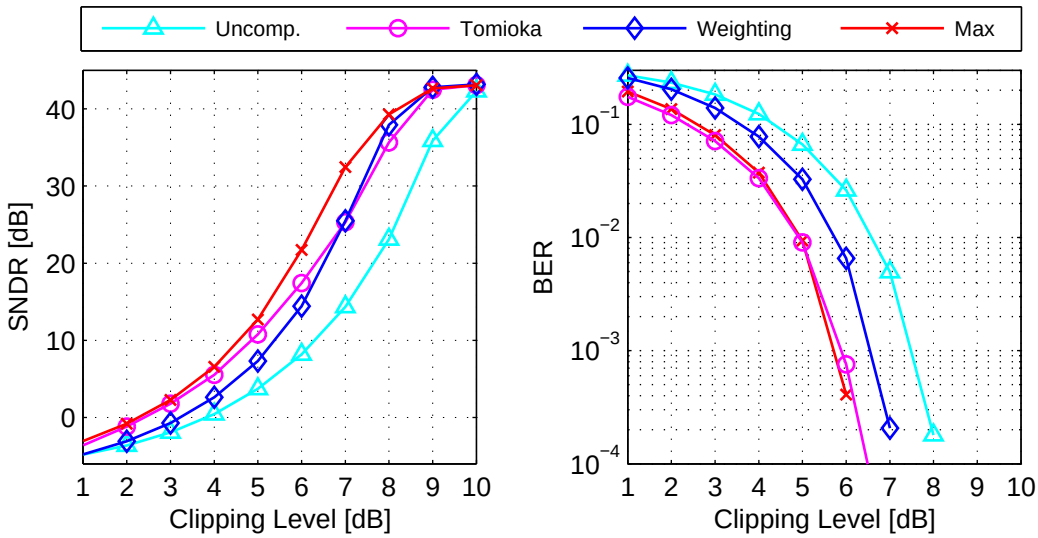

Figure 5.14. *Simulation example as a function of clipping level for the different interpolation schemes. Two iterations are used for every data block in the interpolation stage.*

5.1.4. Laboratory Measurements

The goal of the laboratory measurements is to verify the performance of the proposed clipping compensation schemes in more practical environment and also to illustrate differences between computer simulations and real-world measurements. Figure 5.15 illustrates the laboratory arrangements employed in the measurements.

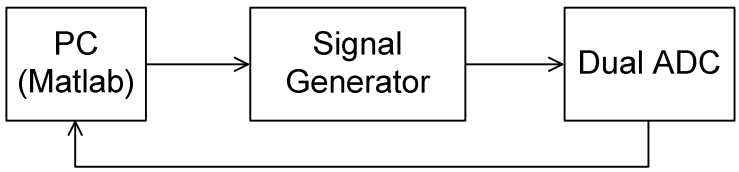

Figure 5.15. *Principal illustration of the laboratory arrangements for the ADC clipping experiments.*

Exactly the same test signal is used in the measurements as was presented in the beginning of Section 5.1. It is uploaded from the PC to the memory of Rohde & Schwarz AFQ100A baseband signal generator [32]. The analog waveform is then fed to the ADC evaluation board containing AD9248 dual 14-bit analog-to-digital converter [5]. The actual ADC device is illustrated in Figure 5.16. The output power of the signal generator is adjusted so that the wanted clipping level in the input of the ADC is attained. Finally, the digital output of the ADC is read from the onboard buffer memory to the PC and imported to MATLAB for post-processing purposes.

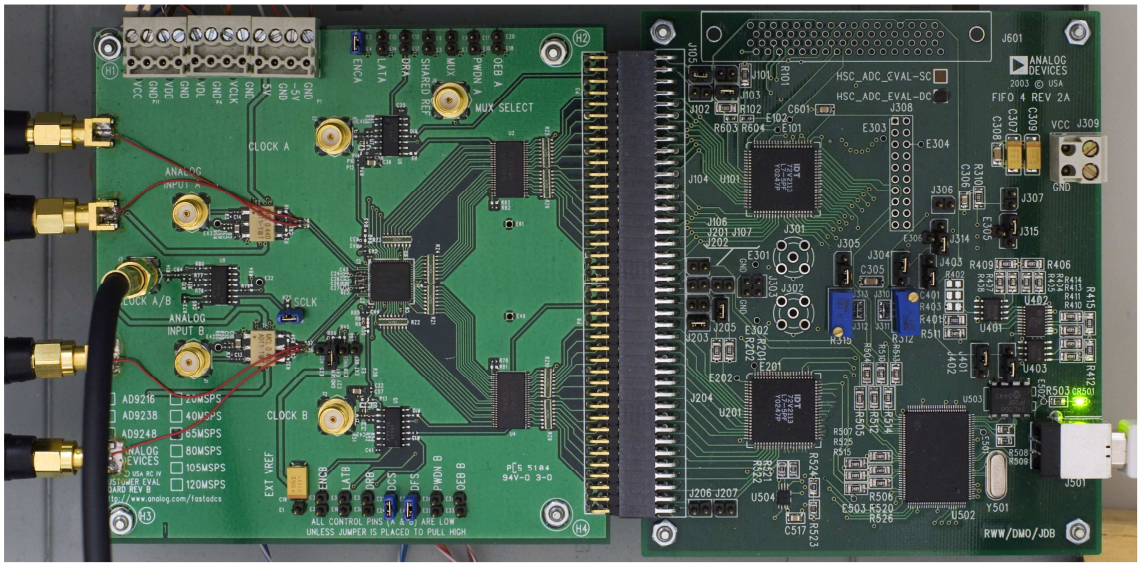

Figure 5.16. *The 14-bit analog-to-digital converter AD1948 [5] with its evaluation board (on the left side) and a buffer memory board for capturing digital data (on the right side).*

For the digitized measurement data, the symbol and phase synchronization can be found by comparing the measured data with the original test signal. Additionally, the original test signal is exploited to calculate the SNDR and BER values. In simulations, it is rather trivial to compare the signal powers for calculating the SNDR, but in the laboratory measurements more attention is needed, because the signal power level is likely to change during the measurement. For example, the signal generator automatically scales the original digital signal to match with its operation region. The right scale is found by comparing the measured data with the original test signal through the LMS algorithm.

Just as in the pure computer simulations, here several random realizations of the test signal are used and after the measurements the results are averaged. Unfortunately, the measurement process requires some manual operations and hence the number of random realizations has to be kept limited. In these experiments, the results are averaged over 20 realizations.

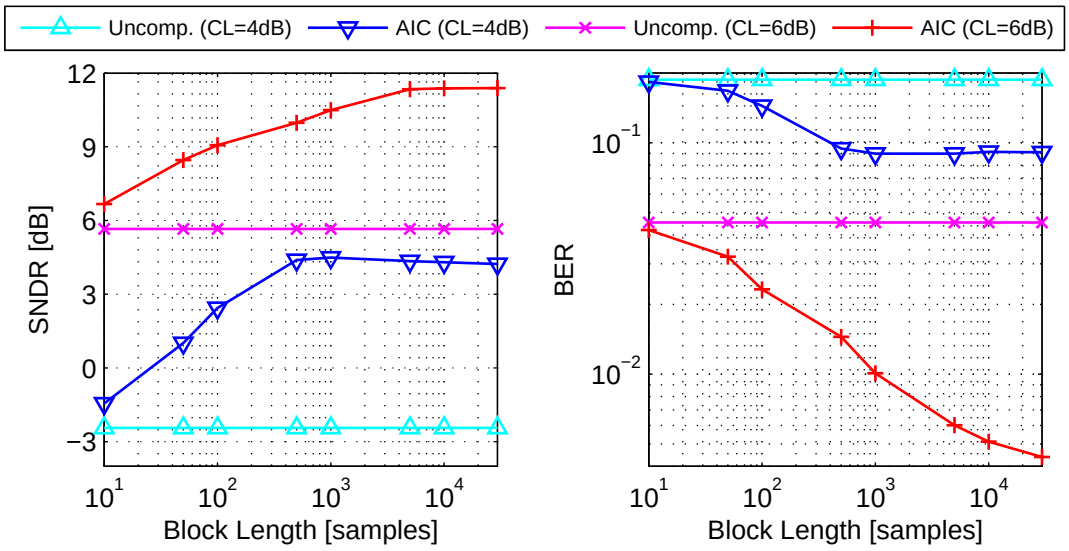

Figure 5.17. *Laboratory measurement example of the AIC performance for clipping levels 4 dB and 6 dB when the processing block length is varied. The results are acquired from the QPSK signal demodulated from the weak signal band at 3 MHz.*

First example deals with the block length of the AIC processing. Figure 5.17 presents the results for clipping levels of 4 dB and 6 dB. This laboratory measurement confirms the conclusion made based on the computer simulations that the sufficient block length is between 1,000 and 5,000 samples. Another conclusion that is undoubtedly affirmed is related to the number of taps used in the adaptive filtering stage. The measurement results related to this are shown in Figure 5.18. It can be seen from the figure that there is no gain of using more than one tap in the adaptive filters in the case of clipping compensation.

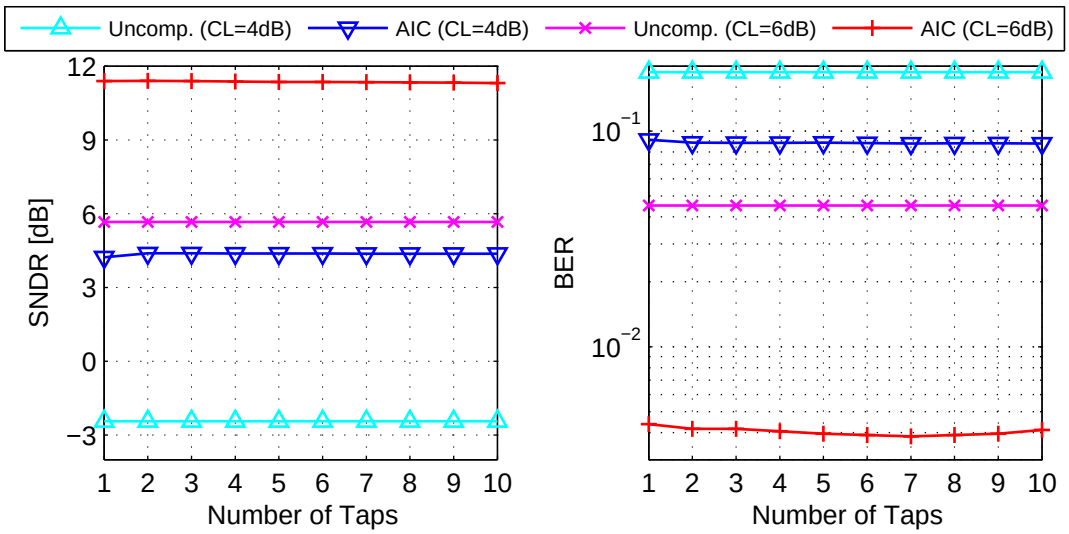

Figure 5.18. *Laboratory measurement example of the AIC performance for the clipping levels of 4 dB and 6 dB with different number of taps in the adaptive filter stage.*

Next, the different interpolation schemes are tested with the measurement data. All of the schemes are implemented exactly the same way as described in Subsection 5.1.2. Performance for different number of iterations in the interpolation stage the clipping level being 6 dB is presented in Figure 5.19. The behavior is almost the same as in the computer simulations (Figure 5.11). However, it can be noticed that especially the maximum method requires more iterations to achieve its peak performance. In addition, the weighting method cannot outperform Tomioka's during the 20 iterations. One possible reason for this might be that interpolation errors cumulate from iteration to iteration and hence less gain can be achieved with next iteration.

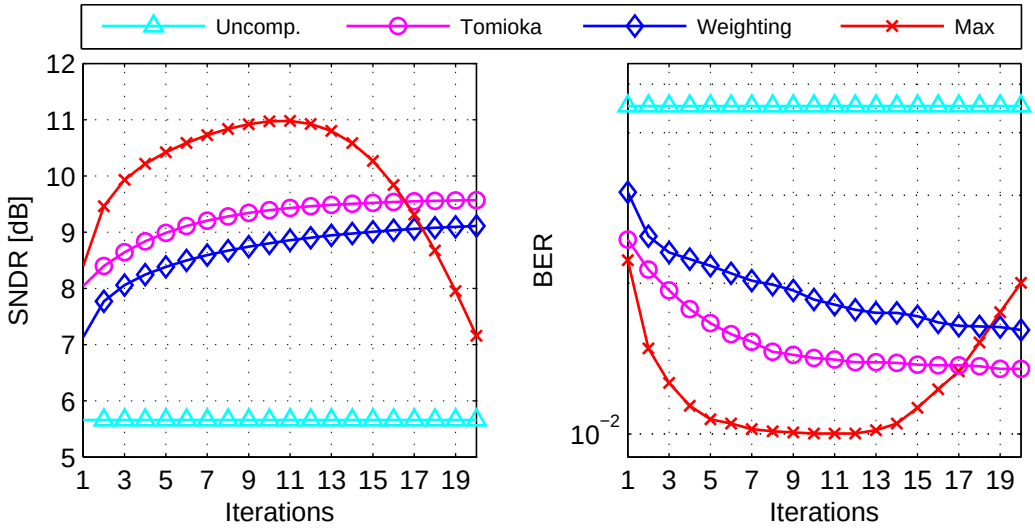

Figure 5.19. *Laboratory measurement example of how the number of iterations in the interpolation stage affects to the overall post-processing performance when the clipping level of the signal is 6 dB.*

Similar behavior is shown in Figure 5.20 where the clipping level of 4 dB is considered. Also these results are consistent with the earlier computer simulations. This latter example represents heavy clipping and hence the waveform reconstruction is very challenging. Especially the weighting method cannot provide good performance with a reasonable number of iterations.

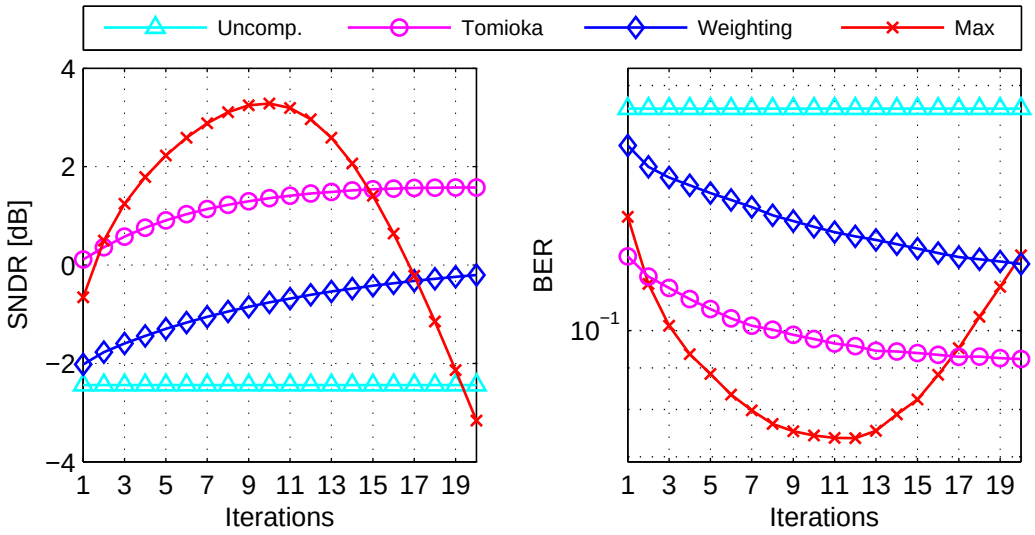

Figure 5.20. *Laboratory measurement example of how the number of iterations in the interpolation stage affects to the overall post-processing performance when the clipping level of the test signal is 4 dB.*

The last measurement example is devoted to compare the performance of the different clipping compensation techniques. This is carried out by varying the clipping level of the test signal from 3 dB to 10 dB as shown in Figure 5.21. The AIC method is clearly outperforming all the considered interpolation schemes regardless of the clipping level. This contradicts the conclusion made from the computer simulations (see Figure 5.13 and Figure 5.14). The final conclusion is that the AIC method is more robust than interpolation when employed in a real operation environment. The reason is that the AIC method is a general post-processing technique for reducing distortion regardless of the actual source whereas the interpolation focuses only on the clipping phenomenon. Therefore, all other sources of distortion and noise decrease the performance of the interpolation.

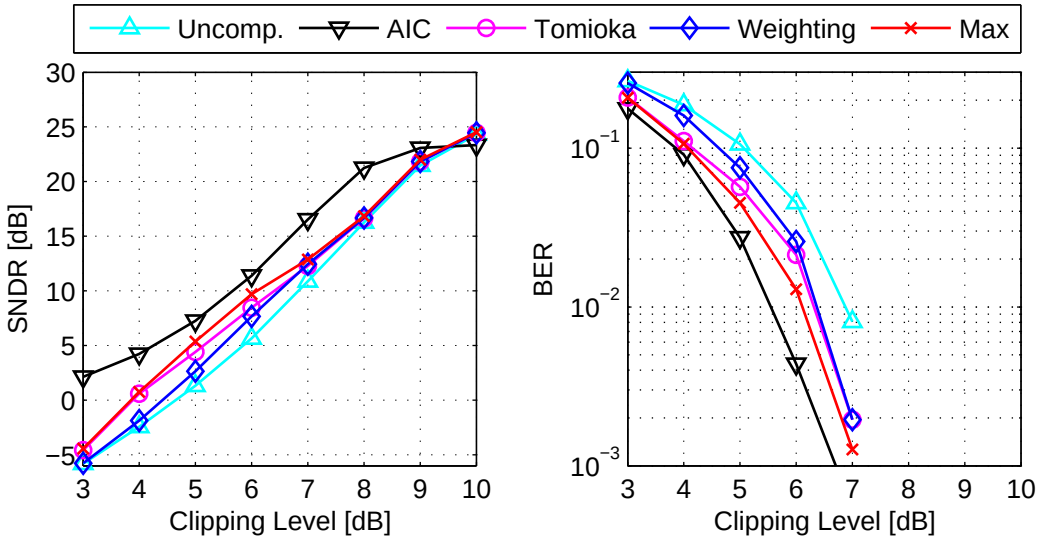

Figure 5.21. *Laboratory example as a function of clipping level. The different interpolation schemes with two iterations as well as the AIC method are considered.*

Another challenge in the interpolation process is detecting the clipped samples. In the output waveform of a real-life ADC, all the clipped samples don't have exactly the same value but more like variations from sample to sample. Figure 5.22 illustrates differences between the theoretical clipping and the clipping behavior of the true-world ADC used in laboratory measurements. Due to the variations, it is required to have a proper threshold for clipping detection. If the threshold value is too high, all the clipped samples are not interpolated and correspondingly, if the threshold is too low, even some of the unclipped values are interpolated and this might create additional distortion.

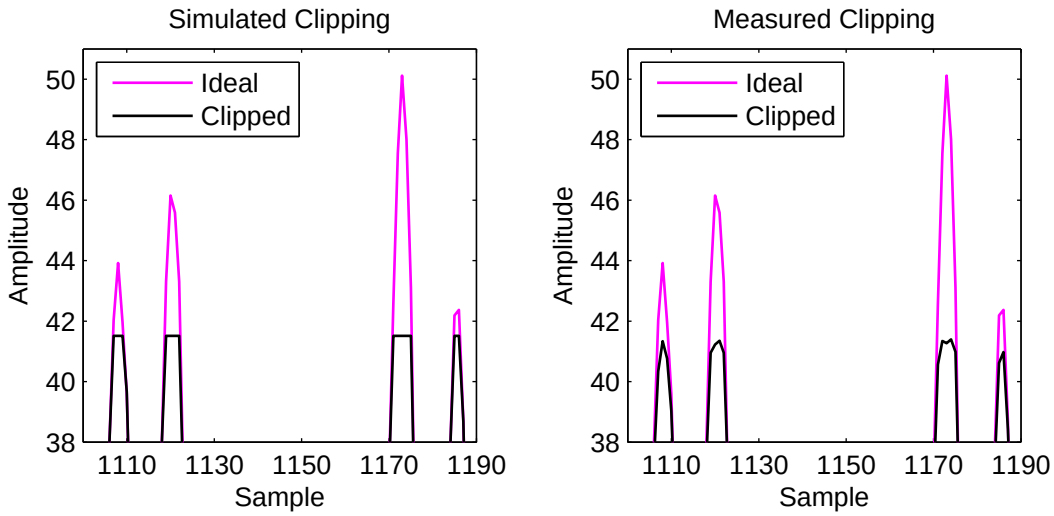

Figure 5.22. *A detail from the time domain waveform of the test signal after theoretical clipping in a computer simulation (on the left) and after clipping in the real-life analog-to-digital converter AD9248 (on the right). Approximately the same clipping level is used in both cases to illustrate the differences in clipping behavior.*

5.2. INL Mitigation

Integral nonlinearity is another source of nonlinear distortion in wideband analog-to-digital converters, besides clipping, that can be compensated with the proposed AIC method. The INL mitigation example presented here is carried out using computer simulations, but the used ADC model is based on a real commercial converter to emphasize practicality. The employed ADC is the 10-bit converter AD9218 [4] and its typical INL error curve is shown in Figure 4.8. In practice, the ADC is simulated in MATLAB using a behavioral model called ADIsimADC [6] provided by the manufacturer.

The test signal used in this INL mitigation example is similar to the one described in Section 5.1 for the clipping experiments, although some changes are made to emphasize INL effects. Details of the test signal are shown in Table 5.2. Power level of the weakest signal band is set low enough that the INL effects can be seen. Naturally, the power level must not be too low to guarantee that the signal is still distinguishable from the quantization noise. Other differences in the test signal, compared to the clipping experiment, concern the sampling frequency, center frequencies of the individual signal bands and overall PAPR. Nevertheless, these differences are not very essential here.

Table 5.2. *Summary of properties for the test signal employed in illustrating INL mitigation performance.*

Sampling frequency	32 MHz
Center frequencies	-10 MHz, -4 MHz, -1 MHz, 3 MHz, 8 MHz
Relative powers	-45 dB, -40 dB, 0 dB, -65 dB, -35 dB
Modulation	QPSK (for all five single-carrier signals)
Signal length	31,355 samples
PAPR (I branch)	7.6 dB

The spectrum of the (ideal) test signal is illustrated on the left side of Figure 5.23. Correspondingly, the same signal after analog-to-digital conversion by AD9218 is shown on the right side of Figure 5.23. The test signal is scaled so that it optimally uses the full input voltage range of the ADC, i.e., the signal is not clipped but utilizes maximum number of quantization levels. Due to the INL errors in the ADC, especially the nonlinear distortion from the strong signal band at center frequency of -1 MHz is falling on top of the (weak) signal band of interest around 3 MHz. This mainly stems from the LCF part of the INL. The HCF and noise components of the INL are basically seen as a

risen noise floor in the spectrum. Note that most of the noise is still due to the quantization and is therefore unavoidable from the quantization theory point of view.

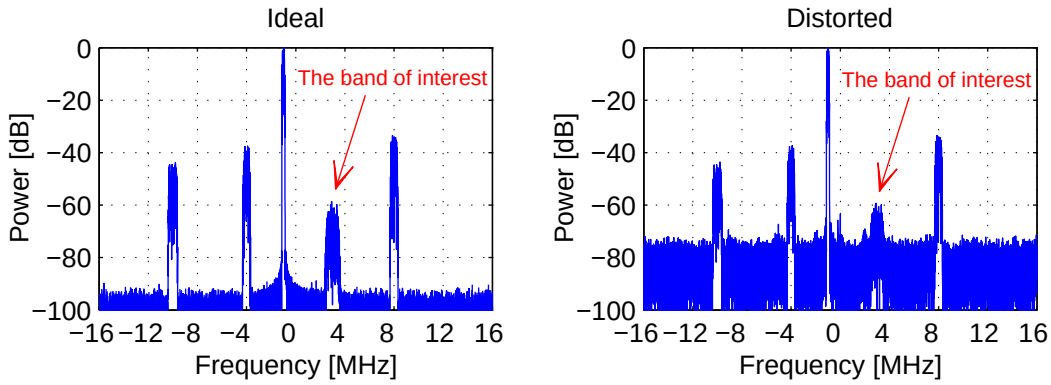

Figure 5.23. *Power spectrum of the test signal before and after analog-to-digital conversion with the 10-bit ADC (AD9218, [4]) illustrating the frequency domain effects of the INL errors.*

In the post-processing stage, the AIC method is employed so that it reduces nonlinear distortion of orders three, five and seven – here the third being the most dominant one. This stems from the shape of the INL curve. It is worth knowing that other types of converters can have other dominating distortion orders, e.g., second and fourth. In the adaptive filter stage, single-tap filters are employed. Their sufficiency was verified with a preliminary simulation, where it was noticed that multi-tap adaptive filters do not bring any additional gain in this experiment. Figure 5.24 illustrates the constellation of the weak signal demodulated from the signal band around 3 MHz before and after applying the AIC processing. It is clearly visible from the constellations that AIC can reduce nonlinear distortion which is stemming from the INL errors. In this example, the gain in SNDR is almost 3 dB. The most limiting matter for the performance of the AIC method is the fact that only the LCF part of the INL can be removed. Entirely different kind of approach would be needed in order to reduce the HCF part and still the performance is limited due to the inband noise, which cannot be removed with post-processing [11].

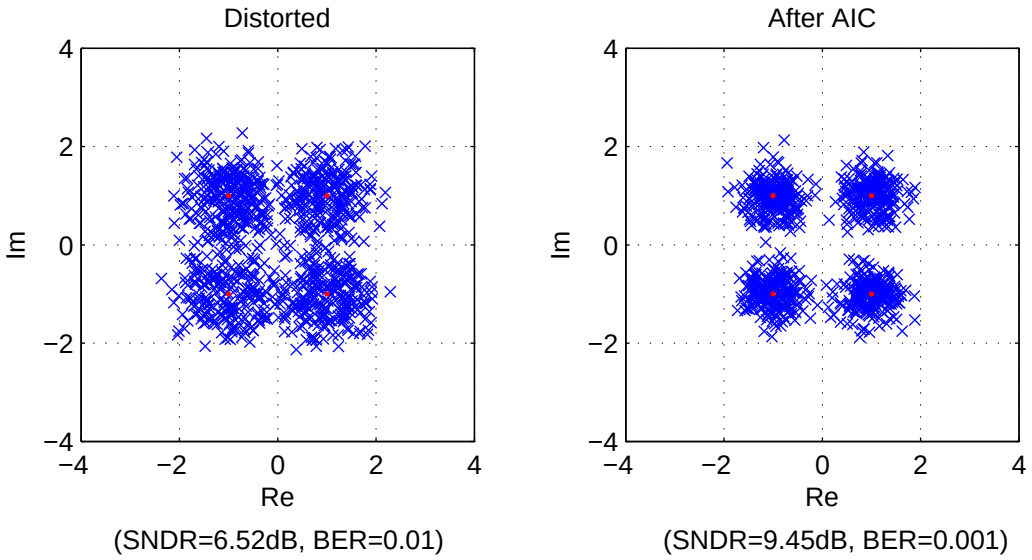

Figure 5.24. *Constellations of the weak QPSK signal demodulated from the signal band with center frequency of 3 MHz without and with the AIC post-processing.*

In the previous example the test signal (31,355 samples) was processed as a whole with the AIC method. As was concluded in Subsection 5.1.1, the processing block length affects to the performance of the AIC method. Therefore, this matter is also investigated in the INL mitigation case. Figure 5.25 illustrates the AIC performance with different processing block lengths. The results are averaged over 500 random realizations of the test signal.

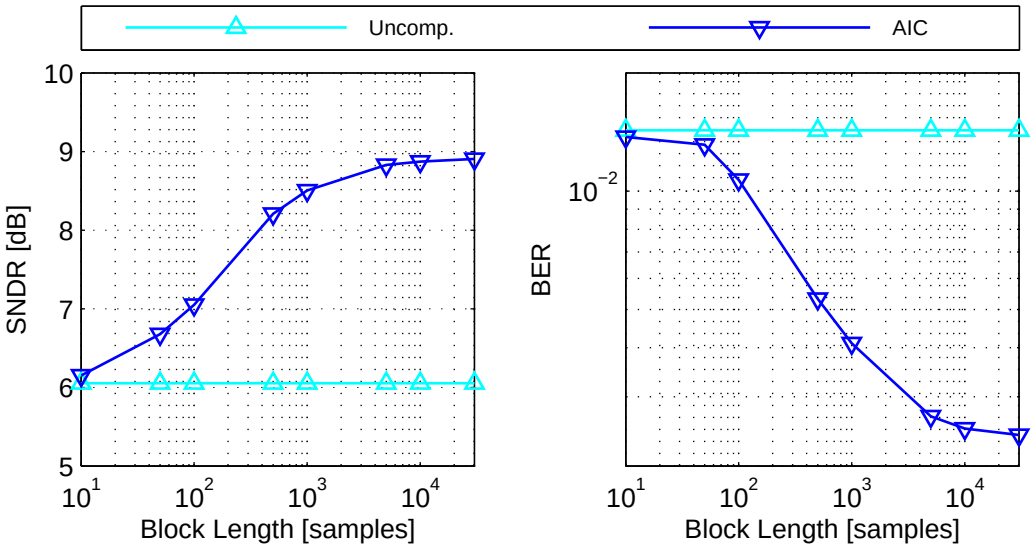

Figure 5.25. *Simulation example of the AIC performance as a function of processing block length. The SNDR and BER values are acquired from the weak QPSK signal demodulated from the signal band located around 3 MHz.*

The SNDR undoubtedly increases as a function of the processing block length but saturates around 9 dB in this specific case. It can be concluded that the processing block length in between 1,000 and 5,000 samples is sufficient to achieve reasonable performance. This is exactly the same conclusion that was made from the clipping experiment. This makes sense because the interference cancellation scenarios (distortion orders, etc.) are somewhat similar, although the actual phenomena behind the nonlinearities are very different.

6. CONCLUSION

In this thesis the topic of analog-to-digital converter nonlinearities and their compensation has been discussed with a special emphasis on wideband radio receivers. After defining the most essential ADC nonlinearities, such as DNL and INL, different high-speed ADC architectures were presented. The architectures have an inherent trade-off between sampling rate and required complexity to achieve a specific resolution. However, every architecture has its own benefits for certain applications and therefore none of them can be omitted. In addition, basic principles of the most common ADC nonlinearity compensation methods, considering look-up tables, dithering and model inversion, were given based on the latest scientific publications. Many of the proposed DSP-based post-processing techniques are designed for ADCs in measurement equipment or other such a usage where, e.g., offline calibration is possible. Therefore, the main part of the thesis focused on entirely online post-processing techniques.

Waveform clipping due to the improper input signal conditioning in the ADC was the main nonlinearity source, besides INL, that was considered in detail since it is becoming more and more important due to the new evolving wireless systems with rapidly changing signal dynamics. One of the contributions of the thesis is related to the mathematical analysis of the clipping behavior. A time-variant model based on Fourier series was derived and to the best knowledge of the author it couldn't be found from the existing literature at the time the research was conducted. The model describes separately the different orders of nonlinear distortion and this way of thinking was also used as the basis for the proposed clipping compensation method called adaptive interference cancellation.

The main contribution of the thesis is related to ADC nonlinearity compensation methods that are suitable for wideband radio receivers. The so-called AIC method stemming from interference cancellation was proposed and is applicable in both clipping as well as INL mitigation. Also the performance of the AIC method was tested separately in the cases of clipping and INL. It was shown that the proposed method was

able to significantly reduce nonlinear distortion from the band of interest when there are strong interfering signals present in the neighboring frequency bands. The performance was verified using both computer simulations and laboratory measurements. Both gave rather similar kinds of results and hence the AIC method can be seen as a very promising approach to be implemented in real radio receivers. This is especially true because the AIC method can reduce several kinds of distortion at the same time regardless of their sources.

Interpolation methods were also considered in the thesis for enhancing the clipped waveform and thus to reduce the amount of interference. The performance results from the computer simulations and laboratory measurements for the proposed interpolation techniques were compared with a method found from the literature. It was shown that a smart interpolation filter design and its proper application can help reducing computational complexity of the post-processing and improve the achievable performance. Furthermore, it can be concluded that a good performance in computer simulations does not necessarily guarantee good performance in practice. It was noticed from the laboratory measurements that noise and other distortion besides the clipping can noticeably reduce the effectiveness of the interpolation. On the other hand, it is probable that the interpolation performance can be yet increased with further filter optimization and might be worth considering in the future work.

In the literature survey part of this thesis it was mentioned that there are several clipping compensation methods for intentional clipping in transmitters. These methods require exact knowledge of the clipping level and hence are not directly suitable for compensating the unintentional clipping taking place in receivers. One topic for the future work is to study how to make the transmitter-related compensation methods applicable for receiver clipping. For example, some kind of blind estimation about the clipping level could be made, but it is not assured that the estimate is accurate enough for good performance. It was already seen in this thesis that a small change in the clipping level might have considerable effect to the amount of nonlinear distortion.

In the future work, it might be also useful to more carefully exploit the derived mathematical model for the clipping phenomenon. The case might be that its full potential was not exploited in this thesis. For example, the model gives amplitudes of the different distortion orders and it can be possible to use this knowledge in the compensation.

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APPENDIX: DERIVATION OF THE FOURIER SERIES FOR SYMMETRIC CLIPPING

Fourier coefficients for the Fourier series in case of symmetric hard clipping can be derived from the Equation (4.7) which was

$$a_{m,I}(t) = \frac{1}{2\pi}\Bigg[\int_{-\frac{\pi}{2}}^{-\arccos\frac{V_0}{A(t)}} v_{in,I}(t)e^{-jm\theta_c(t)}\mathrm{d}\theta_c(t) + \int_{-\arccos\frac{V_0}{A(t)}}^{\arccos\frac{V_0}{A(t)}} V_0 e^{-jm\theta_c(t)}\mathrm{d}\theta_c(t)$$
$$+ \int_{\arccos\frac{V_0}{A(t)}}^{\pi-\arccos\frac{V_0}{A(t)}} v_{in,I}(t)e^{-jm\theta_c(t)}\mathrm{d}\theta_c(t) + \int_{\pi-\arccos\frac{V_0}{A(t)}}^{\arccos\frac{V_0}{A(t)}+\pi} -V_0 e^{-jm\theta_c(t)}\mathrm{d}\theta_c(t)$$
$$+ \int_{\arccos\frac{V_0}{A(t)}+\pi}^{\frac{3\pi}{2}} v_{in,I}(t)e^{-jm\theta_c(t)}\mathrm{d}\theta_c(t)\Bigg].$$

For the sake of clarity, all five integrals are derived separately and the time variable t is omitted. The numbering of the integrals is according to Figure 4.1. Also notation $r = \arccos\frac{V_0}{A}$ is used.

Let's first consider the special case when $m = 1$. Then the integral number 1 becomes

$$\begin{aligned} a_{1,1,I} &= \int_{-\frac{\pi}{2}}^{-r} A\cos(\theta_c)e^{-j\theta_c}\mathrm{d}\theta_c = A\int_{-\frac{\pi}{2}}^{-r}\frac{1}{2}\left(e^{j\theta_c} - e^{-j\theta_c}\right)e^{-j\theta_c}\mathrm{d}\theta_c \\ &= \frac{A}{2}\left[\left(-r+\frac{\pi}{2}\right) + \frac{j}{2}\left(e^{j2r} - e^{j\pi}\right)\right] \\ &= A\left[-\frac{r}{2} + \frac{\pi}{4} + \frac{j}{4}(\cos 2r + j\sin 2r + 1)\right] \\ &= A\left(\frac{\pi}{4} - \frac{r}{2}\right) + j\frac{V_0^2}{2A} - \frac{V_0}{2}\sqrt{1-\left(\frac{V_0}{A}\right)^2}. \end{aligned}$$

The integral number 2 becomes

$$a_{1,2,I} = \int_{-r}^{r} V_0 e^{-j\theta_c}\mathrm{d}\theta_c = -\frac{V_0}{j}\left(e^{-jr} - e^{jr}\right) = 2V_0\sin r.$$

The integral number 3 becomes

$$a_{1,3,I} = \int_{r}^{\pi-r} A\cos(\theta_c)e^{-j\theta_c}\mathrm{d}\theta_c = \frac{A}{2}\left[\pi - 2r + e^{-j2(\pi-r)} - e^{-j2r}\right]$$
$$= A\left(\frac{\pi}{2} - r\right) - V_0\sqrt{1-\left(\frac{V_0}{A}\right)^2}.$$

The integral number 4 becomes

$$a_{1,4,I} = \int_{\pi-r}^{r+\pi} -V_0 e^{-j\theta_c}\mathrm{d}\theta_c = \frac{V_0}{j}\left(e^{-j(r+\pi)} - e^{-j(\pi-r)}\right)$$
$$= \frac{V_0}{j}\left(-2j\sin(r)e^{-j\pi}\right) = 2V_0\sin r.$$

The integral number 5 becomes

$$a_{1,5,I} = \int_{r+\pi}^{\frac{3\pi}{2}} A\cos(\theta_c)e^{-j\theta_c}\mathrm{d}\theta_c = \frac{A}{2}\left[\frac{3\pi}{2} - r - \pi + \frac{j}{2}\left(e^{-j3\pi} - e^{-j2(r+\pi)}\right)\right]$$
$$= \frac{A}{2}\left[\frac{\pi}{2} - r + \frac{j}{2}(-1 - \cos 2r + j\sin 2r)\right]$$
$$= A\left(\frac{\pi}{4} - \frac{r}{2}\right) - j\frac{V_0^2}{2A} - \frac{V_0}{2}\sqrt{1-\left(\frac{V_0}{A}\right)^2}.$$

Hence, substituting equations $a_{1,1,I}, a_{1,2,I}, a_{1,3,I}, a_{1,4,I}$ and $a_{1,5,I}$ in Equation (4.7) gives

$$a_{1,I} = \frac{1}{2\pi}\left[A(\pi - 2r) + 2V_0\sqrt{1-\left(\frac{V_0}{A}\right)^2}\right] = \frac{A}{2} - \frac{A}{\pi}r + \frac{V_0}{\pi}\sqrt{1-\left(\frac{V_0}{A}\right)^2}.$$

Very similar calculation for the case when $m = -1$ can be performed and the outcome is the same as for $a_{1,I}$. It means that $a_{-1,I} = a_{1,I}$.

The more general case, i.e. $m \neq 1,$ can be obtained in a similar manner, but leads into more complicated equations. Let's first derive that

$$\int A\cos(\theta_c)e^{-jm\theta_c}\mathrm{d}\theta_c = A\left(\frac{jm}{m^2-1}\cos(\theta_c)e^{-jm\theta} - \frac{1}{m^2-1}\sin(\theta_c)e^{-jm\theta}\right).$$

Now the integral number 1 becomes

$$a_{m,1,I} = \int_{-\frac{\pi}{2}}^{-r} A\cos(\theta_c)e^{-jm\theta_c}\mathrm{d}\theta_c = \frac{A}{m^2-1}\left[\left(jm\frac{V_0}{A} + \sqrt{1-\left(\frac{V_0}{A}\right)^2}\right)e^{jmr} - e^{jm\frac{\pi}{2}}\right].$$

The integral number 2 becomes

$$a_{m,2,I} = \int_{-r}^{r} V_0 e^{-jm\theta_c} \mathrm{d}\theta_c = \frac{2V_0}{m} \sin mr.$$

The integral number 3 becomes

$$\begin{aligned} a_{m,3,I} &= \int_{r}^{\pi-r} A\cos(\theta_c) e^{-jm\theta_c} \mathrm{d}\theta_c \\ &= \frac{A}{m^2-1}\left[\left(-jm\cos r - \sin r\right)e^{-jm(\pi-r)} + (-jm\cos r + \sin r)e^{-jmr}\right] \\ &= \frac{A}{m^2-1}\left[\left(-jm\frac{V_0}{A} - \sqrt{1-\left(\frac{V_0}{A}\right)^2}\right)(-1)^m e^{jmr} + \left(-jm\frac{V_0}{A} + \sqrt{1-\left(\frac{V_0}{A}\right)^2}\right)e^{-jmr}\right]. \end{aligned}$$

The integral number 4 becomes

$$a_{m,4,I} = \int_{\pi-r}^{r+\pi} -V_0 e^{-jm\theta_c} \mathrm{d}\theta_c = \frac{V_0}{jm}\left(-2j\sin(mr)e^{-jm\pi}\right) = -\frac{2V_0}{m}(-1)^m \sin mr.$$

The integral number 5 becomes

$$\begin{aligned} a_{m,5,I} &= \int_{r+\pi}^{\frac{3\pi}{2}} A\cos(\theta_c) e^{-jm\theta_c} \mathrm{d}\theta_c \\ &= \frac{A}{m^2-1}\left[\left(jm\cos\frac{3\pi}{2} - \sin\frac{3\pi}{2}\right)e^{-jm\frac{3\pi}{2}}\right. \\ &\quad \left.-(jm\cos(r+\pi) - \sin(r+\pi))e^{-jm(r+\pi)}\right] \\ &= \frac{A}{m^2-1}\left[(-1)^m e^{-jm\frac{\pi}{2}} + \left(jm\frac{V_0}{A} - \sqrt{1-\left(\frac{V_0}{A}\right)^2}\right)(-1)^m e^{-jmr}\right]. \end{aligned}$$

Now substituting the equations $a_{m,1,I}, a_{m,2,I}, a_{m,3,I}, a_{m,4,I}$ and $a_{m,5,I}$ in Equation (4.7) gives

$$\begin{aligned} a_{m,I} = \frac{1}{2\pi}\Bigg[\frac{A}{m^2-1}\Bigg[&\left(jm\frac{V_0}{A} + \sqrt{1-\left(\frac{V_0}{A}\right)^2}\right)e^{jmr} + \left(-jm\frac{V_0}{A} + \sqrt{1-\left(\frac{V_0}{A}\right)^2}\right)e^{-jmr} \\ &+\left(-jm\frac{V_0}{A} - \sqrt{1-\left(\frac{V_0}{A}\right)^2}\right)(-1)^m e^{jmr} + \left(jm\frac{V_0}{A} - \sqrt{1-\left(\frac{V_0}{A}\right)^2}\right)(-1)^m e^{-jmr} \\ &+\frac{2(1-(-1)^m)V_0}{m}\sin mr\Bigg] \end{aligned}$$

$$= \frac{1}{2\pi}\left[\frac{A}{m^2-1}\left[\frac{2m((-1)^m-1)V_0}{A}\sin mr + 2(1-(-1)^m)\sqrt{1-\left(\frac{V_0}{A}\right)^2}\cos mr\right]\right.$$
$$\left. + \frac{2(1-(-1)^m)V_0}{m}\sin mr\right]$$
$$= \frac{(-1)^m-1}{\pi}\left[\frac{V_0}{m\left(m^2-1\right)}\sin mr - \frac{A}{m^2-1}\sqrt{1-\left(\frac{V_0}{A}\right)^2}\cos mr\right]$$
$$= \frac{[(-1)^m-1]\left[V_0\sin mr - mA\sqrt{A^2-V_0^2}\cos mr\right]}{\pi m\left(m^2-1\right)}.$$

From the final form of $a_{m,I}$ it's easy to see that the equation reduces to zero if m is an even number. On the other hand, if m is odd, $a_{m,I}$ gets a form of

$$a_{m,I} = \frac{-2V_0\sin mr + 2m\sqrt{A^2-V_0^2}\cos mr}{\pi m\left(m^2-1\right)} \quad ,m = \pm 3, \pm 5, \pm 7, ...$$

which is the same as presented in the Equation (4.8).

If the model is used for a complex band-pass signal, there is still one special case to take into consideration. When the five integrals are calculated for $m = 0$ and substituted in the equation for Fourier coefficient, the outcome is

$$a_0 = \frac{1}{2\pi}\left[A\left(-\sqrt{1-\left(\frac{V_0}{A}\right)^2}+1\right) + 2V_0 r + 0 - 2V_0 r + A\left(\sqrt{1-\left(\frac{V_0}{A}\right)^2}-1\right)\right] = 0.$$