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HIGH SPEED DC-DC CONVERTER WITH SELF-OSCILLATING CONTROL

Master of Science thesis

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ABSTRACT

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In order to reduce the overall size of the power conversion device several advanced techniques can be applied. One of the direct ways is increasing switching frequency of DC-DC converter. This leads to decreased size of bulky energy storage components, such as inductors and capacitors. However, a rapid rise of operating frequency brings new challenges. Among those are significant switching and conduction losses, which make using conventional topologies of converters impractical. Therefore, various new topologies should be investigated.

This Thesis presents design and simulations of High speed DC-DC converter with self-oscillating control. The design procedure is described in details for discrete implementation on printed-circuit board. The simulation results are analyzed and a few additional recommendations for improving efficiency and performance of circuit are given. The proposed converter consists of cascaded power stage, duty-cycle detector, pulse shaper, and transformer. The primary winding of transformer serves as a filter load coil and secondary supplies feedback signal to the gates of switching transistors by employing duty-cycle detector and pulse shaping circuit. The designed High speed DC-DC converter with self-oscillating control provides an output voltage of 2.34 V while operating at 3.4 MHz switching frequency. The reported efficiency of circuit is 70.35%. The input voltage is 4 V and duty cycle is 58%. The operation of converter is intended for variable supply voltage from 3 V to 5 V.

A resonant gate driving technique with respect to the proposed DC-DC converter is also presented in that work. The converter provides 2.30 V of output voltage and efficiency of 72.4%. The operation frequency is 3.35 MHz.

PREFACE

This thesis work was done at the RFIC Laboratory, Department of Electronics and Communication at Tampere University of Technology. The research work is a continuation of a project, which was previously carried out by RF Integrated Circuit group.

Foremost, I would like to thank my direct supervisors Prof. Nikolay T. Tchamov and Prof. Teuvo Suntio for their continuous guidance and help. I want to thank the other team members from our research group for excellent work. Furthermore, the support and advices of our consultant Jani Järvenhaara had a great impact on research outcome.

Finally, yet importantly, I am grateful to my mother for her valuable and endless support. Thank you for giving me hope and encouragement.

Tampere, 20.4.2016

Stanislav Babaev

CONTENTS

LIST OF SYMBOLS AND ABBREVIATIONS

CMOS	Complementary Metal Oxide Semiconductor
DC-DC	Direct-Current to Direct-Current
IC	Integrated Circuit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
RF	Radio Frequency
VHF	Very High Frequency
ZVS	Zero-Voltage Switching
f	frequency
Ω	Ohm
τ	time constant

1. INTRODUCTION

The rapid development of portable electronics market dictates new trends in evolving design of complex parts such as processors, displays, memory chips and RF blocks. The requirements for these units are full integration along with power efficiency. Consequently, in order to meet modern strict requirements, efficient and light power supply solutions should be investigated. For low-power consumption units or for mobile applications, a Lithium-Ion battery is often used. Such a battery is described as variable voltage source with range between 2.8 V and 5.5 V. Therefore, DC-DC converters are essential in providing a stable supply voltage for various integrated parts of portable electronic device.

Increasing switching frequency of the DC-DC converter is a straight method to diminish size of its inductive and capacitive components, which in turn occupy a considerably large area of power supply unit. This is particularly important for integrated circuit (IC) devices, where small size of the power converter should coexist with high conversion efficiency and lead to a lower total power consumption, especially when these devices are used in power management unit (PMU) architecture. However, a rise in speed of the converter is usually followed by substantially increased losses. Consequently, at the very high frequency (VHF) range from 30 MHz to 300 MHz most of the standard topologies become unsuitable.

One of the new VHF converter topologies that was described recently is an Asymmetric VHF self-oscillating converter with integrated transformer [1]. This type of converter was designed for integrated fabrication, however, has not been implemented yet.

To some extent, measurement of characteristics of aforementioned converter and evaluating its performance can be carried out through its practical implementation on the printed-circuit board (PCB). Hence, this Thesis expands from the previously made research and addresses design issues of the high speed DC-DC converter with self-oscillating control implying its physical implementation on PCB. The latter is essential in order to gain an insight into main operational issues and possible suggestions for improvements.

In the scope of this work is a detailed procedure of modeling this converter while remaining proposed topology unchanged. Yet another objective is evaluation of converter's operation based on the simulation results and assessing main challenges associated with it.

Chapter 2 begins with overview of the high frequency converter topologies, which are investigated currently in certain scientific works. Then, different losses in power semiconductors as well as in inductive components under high frequency operation are studied. A PCB design considerations are also briefly discussed in that chapter. Finally, effect of parasitic components in high frequency drivers is introduced. Chapter 3 encompasses design procedure for the proposed converter. It starts with defining target design specifications and brief description of circuit operation. After that, the methods for sizing main circuit components are introduced. The optimization of power stage is presented within this section. The discussion about considering parasitic effects in simulation process concludes this chapter. Chapter 4 is dedicated to simulation results of a designed High speed DC-DC converter with self-oscillating control. It brings also under discussion the explanation of discrepancies between targeted and simulated results. Finally, several proposals are made for future improvements of power conversion efficiency and increasing switching frequency. In Chapter 5 one of the resonant gate driving techniques is applied to the proposed converter. Chapter 6 concludes this Thesis with summarizing main achievements.

2. BACKGROUND

The current demand for small and light power supply units, which are used, for instance, in mobile and automotive applications, dictates the development of new approaches in implementing switched-mode converters. Particular way is to increase switching frequency of converter, which in turn leads to reduced size of energy storage elements, such as capacitors and inductors. Unfortunately, the rapid increase of switching frequency brings new challenges to the operation of switched-mode power supply unit, such as high switching and conduction losses. The losses occur not only in switching components, but also in capacitors and inductors. Latter requires careful sizing and design when speed goes to the high switching range (more than 500 kHz).

This chapter introduces a brief overview of recently developed high frequency topologies in power electronics and lists the main challenges, which remained to resolve. To some extent, most of the scientific papers that are referred to the evolving high speed DC-DC applications comprise modelling and simulation of integrated circuit (IC) devices. However, as was mentioned in chapter 1, the purpose of this work is to confirm the feasibility of implementation VHF DC-DC converter on printed-circuit board (PCB). Although, it shows additional problems incurred, such as dominant impact of PCB parasitic while experiencing high frequency switching, an assembled DC-DC converter could be used in laboratory conditions as a cost-efficient prototype for carrying out measurements and tests and could confirm the feasibility of IC model and implementation.

2.1 Class-E-based power self-oscillating VHF converter

Class E usually referred to all power converters, which employ zero-voltage switching (ZVS) and zero-current switching (ZCS) techniques [2]. The class-E-based converters use a second degree of soft switching, which means that in spite of the turning switches on, when the voltage across them is zero, the derivatives of these signals are also taken into account. The power diagram in Fig. 1 introduces the application of the concept of a class E-oscillator to a class-E-based self-oscillating VHF DC-DC converter. The power stage was implemented with reported speed and efficiency of 97 MHz and 55%, respectively. This converter is based on the well-documented circuit topology from the communication electronics applications. There is one serious reported drawback of this converter, the voltage stress across power switch is 3.6 times larger than in hard switched converters.

The narrow adjustment range of the turn-on time of the MOSFET imposes the low degrees of freedom of proposed converter. Due to that, the levels of input and output voltages are limited significantly. In addition, the efficiency level is unacceptable due to high conduction losses in power switches, which are caused by the high on-resistance of the MOSFET. Later, the suboptimal operation of class-E converters was investigated and opened high degrees of freedom in the design of class-E DC-DC converters. This particularly means that derivative of ZVS-condition takes place during nominal load conditions and only ZVS holds in other cases.

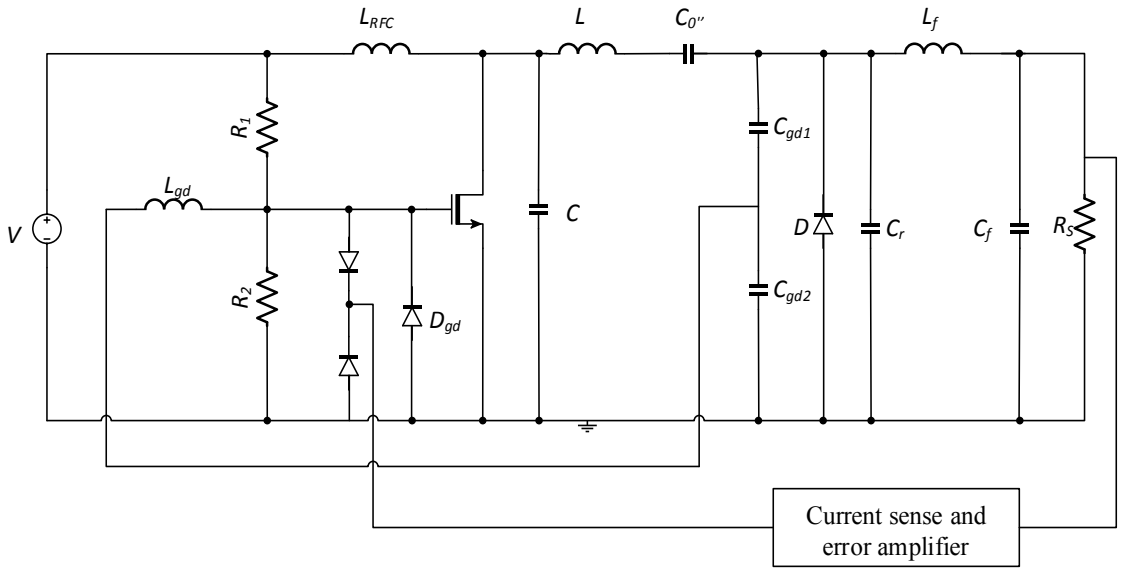

Figure 1. *Schematic of Class-E self-oscillating VHF converter.*

2.2 Self-oscillating DC-DC resonant converter

The converter does not employ any driver integrated circuit. A small self-oscillating low-power resonant tank is used as a driver function and a power tank with rectifier output stage is used to generate DC output voltage [3]. The communication control signal for self-oscillating converter is derived from the current feedback of its resonant load. The proposed topology in Fig. 2 allows to avoid the issue of variation of switching frequency with load changing, because the self-oscillating driver is independent from the load. The power stage is based on a well-known class-D converter topology. R_{so}, L_{so} and C_{so} represent a RLC circuit and is used as a low-power tank. Transformer T_{so} supplies the feedback current to the Zener diodes which shape the square-wave signals to drive class-D MOSFETs. The transformer could be implemented with air-core at high frequencies and has reduced size and cost.

The practically assembled converter was designed to operate converter at frequencies higher than resonance to achieve ZVS and in that certain case f_s is 510 kHz. The

measurements showed that having a 24V of supply voltage gave only 130V of output voltage, although simulations implied that V_{out} was expected to be 180V. The output power was also somewhat lower than simulated one. As stated in the results, this is a consequence of appearing dead-time effect in the rectified sinusoidal signal before DC filter. However, the power consumption of a driver was low and reported efficiency was 80%.

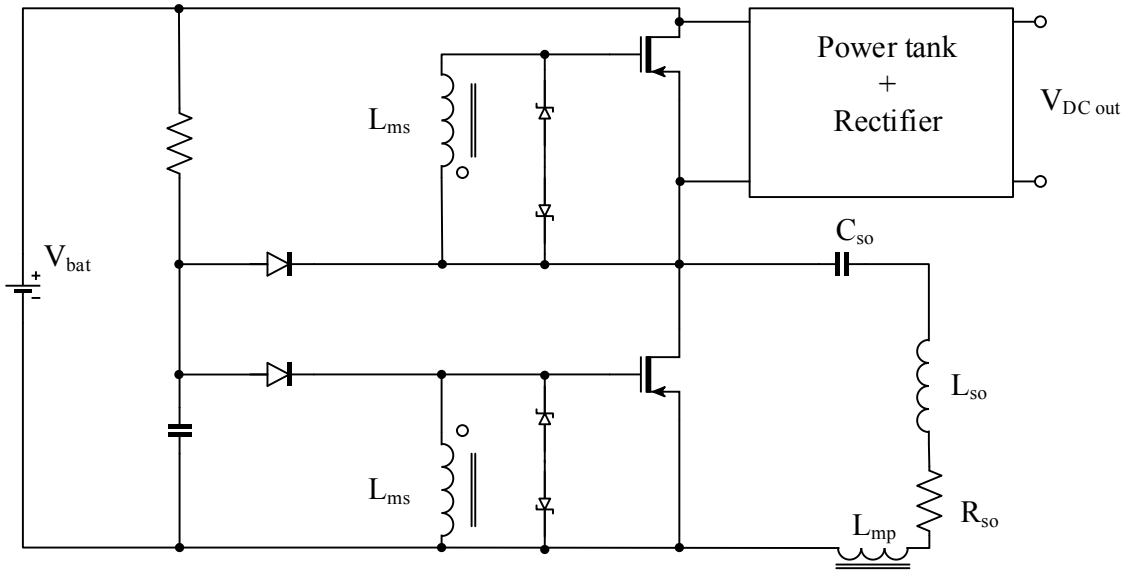

Figure 2. *Schematic of self-oscillating DC-DC resonant converter.*

2.3 Self-powered ultra-low power DC-DC converter

The presented converter is derived from the classical Armstrong oscillator structure [4]. Ultra-low input voltage and high voltage stepping-up abilities are among those benefits of that structure. A self-powering capability is one of the distinctive features of proposed topology. That particularly means that neither external energy source nor external control are needed for operation. The converter was designed to accept high source impedance up to several kOhm. Fig. 3 represents the power stage of power supply unit. The essential oscillator part comprises JFET, which amplifies the gate's input signal. The return loop is formed by the two coupled inductors and by the gate-source capacitor C_{gs}. The topology is based on a Forward mode and energy is transferred to the output during on-time, which avoids the interruption of the switch gate voltage oscillations during the off-time. Performed calculations on oscillations start-up conditions showed that the proper operation of converter with low input voltage and high source impedance is achieved when JFET cutoff voltage and zero-gate voltage drain current I_{DSS} are minimized.

The fabricated prototype was intended for RF energy harvesting. The performance of the converter was demonstrated using experimental tests. The efficiency of 25% was reported while harvesting low RF power (4μW-1mW). The calculated speed according to the frequency equation of Armstrong oscillator was approximately 600 kHz. The power device is very compact (<0.5cm^3) and provides a high voltage step-up ratio (up to 9). A large fraction of losses occurred due to the JFET on-resistance which is high because of the low gate-cutoff voltage. This low voltage as well as low zero-gate voltage drain current I_{DSS} are necessary in order to satisfy the oscillation start-up conditions for low source voltage and high source impedance. As it may be seen, this leads to increased losses in the steady-state. Therefore, there is a trade-off between start-up capability and steady-state efficient operation. The authors claimed that proposed converter could be adapted and used with other energy-harvesting transducers, when battery-less systems are considered.

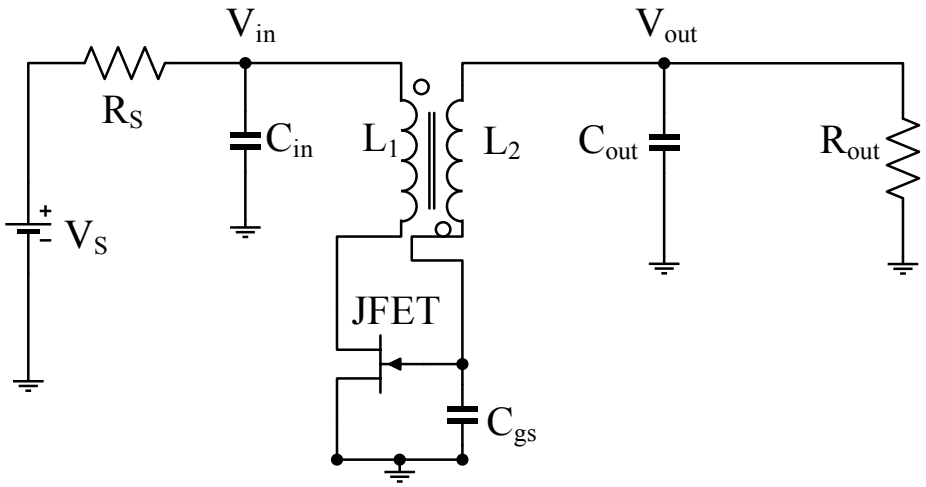

Figure 3. *Schematic of Self-powered ultra-low power DC-DC converter.*

2.4 An asymmetric VHF self-oscillating DC-DC converter with integrated transformer

This type of VHF DC-DC converter employs self-oscillating gate driver [1]. The driver is implemented with self-oscillating circuit, which is separated from the load by means of integrated transformer. The power stage of the proposed converter is depicted in Fig. 4.

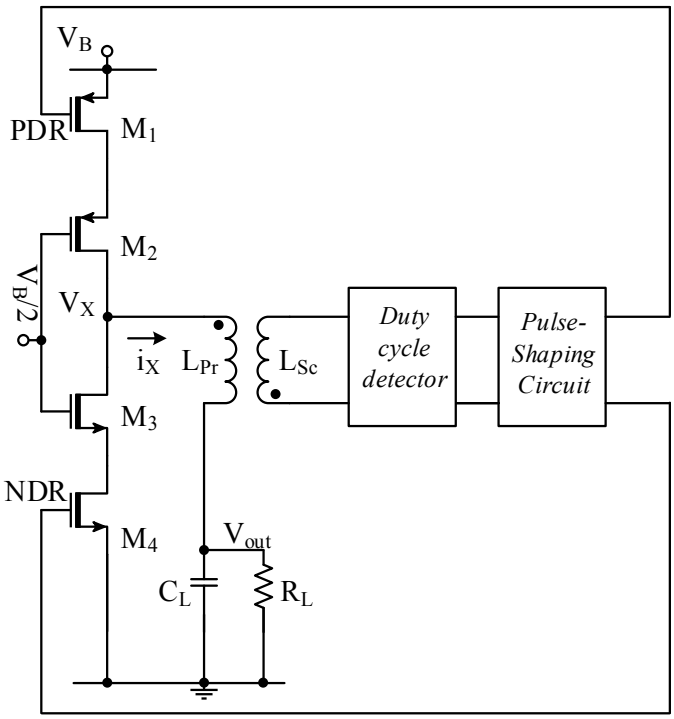

Figure 4. *Asymmetric VHF self-oscillating DC-DC converter with integrated transformer.*

The circuit includes cascaded transistors (M_1, M_2, M_3, M_4). As it may be seen, the traditional load filter coil is replaced with an integrated transformer. The primary side L_{pr}, makes the transfer of the power to the load. The feedback signal is provided by the transformer secondary L_{sc}. A pulse-shaping circuit and a duty cycle detector are also included in the feedback loop. Two rectangular pulses from the output of pulse-shaping block drive the gate of power switches. One of the important features of that converter is an automatic control of duty cycle. External or internal disturbances are perceived by the system as variation of frequency. The changing of output signal of duty cycle takes place with a delay as a response to the variation of frequency. This action is performed by duty cycle detector. Thus, if the input frequency decreases, the output signal of detector has a shorter duty cycle and the system will work at faster frequency.

The presented converter was designed for IC fabrication and simulated oscillation frequency was 220 MHz, which confirms a clear advantage of that converter. The reported efficiency was 61.5% and the large fraction of losses occurred in the switching transistors and in the integrated transformer [5]. In the forthcoming chapters we will concentrate on the main problems associated with VHF power supply and particularly with that converter. We will show the feasibility of implementing high-speed DC-DC converter with self-oscillating control on PCB. The results will be confirmed by the simulations. Furthermore, the approach for improving efficiency will be explained in details.

2.5 Losses and parasitics in power semiconductors in high frequency applications

As it is stated in [6], a significant loss mechanism, which is frequency-dependent, includes gating loss and switching loss. In order to avoid capacitive discharge losses and current and voltage overlap zero-voltage switching could be used. On the other hand, resonant (soft) gating is usually used to reduce the loss caused by charging and discharging MOS gates. Thus, the operation of VHF power supply units depends dramatically on the characteristics of the power switches. One may claim, that frequency limitations of the practical devices depend directly on the loss mechanism. Another type of dominant losses is conduction loss and for a MOSFET, the device conduction loss can be normalized to converter power P and can be estimated as

$$P_{Cond,Norm} \approx 2.363 \cdot \frac{P}{V_{DC}^2} R_{DS,on} \tag{1}$$

where $R_{DS,on}$ is the MOSFET on-state resistance in Ω. The sufficient gating loss for a MOSFET could be considered in case where the shape of the driving pulse is sinusoidal. Approximated power dissipation due to the gating loss and normalized to converter power P can be represented as follows

$$P_{Gate,Norm} \approx \frac{2\pi^2 \cdot f^2 \cdot C_{iss}^2 \cdot R_G \cdot V_{G,ac}^2}{P} \tag{2}$$

where C_{iss} is the input capacitance, R_G is the gate resistance, and $V_{G,ac}$ is the magnitude of the sinusoidal voltage swing at the gate. It is worth noting, that MOSFETs of the proposed high speed DC-DC converter with self-oscillating control incur lower gate driver losses because of the different waveforms (trapezoidal gate voltage due to "constant current" charge and discharge of the gate).

Another issue associated with high frequency power applications is an effect of parasitic elements of power semiconductor switch. They have a large impact on the design of the whole converter and they are a part of the design parameters. Therefore, the parasitic components form an integral part of the circuit and are not longer considered as undesired [2]. For instance, the output capacitance of the MOSFET in a class-E power supply is dependent on input voltage V_{in}, output power P_{out}, and switching frequency f, as

$$P_{Out} = 2\pi^2 \cdot f \quad \cdot C_{oss} \cdot R_G \cdot V_{in}^2 \tag{3}$$

Consequently, the output capacitance C_{oss} limits the maximum switching frequency for a given application. Thus, a careful and precise evaluation of power switches should be made in order to minimize losses during high frequency operation.

2.6 Loss characteristics of inductive components in VHF applications

The VHF operation can sufficiently decrease the energy storage requirements for magnetic elements as compared to usual switching frequencies, so large size reductions of magnetic components could be performed already at flux density levels of tens to hundreds of Gauss [7]. However, most magnetic materials incur significantly high losses at frequencies above a few MHz. Moreover, the available and well-known materials for frequencies above 10 MHz, are usually intended only for small-signal drive conditions, but not under high flux density conditions expected for power electronics applications. One may claim, that the biggest challenges encompass core losses, proximity and skin effect.

The quality factor Q_L of a magnetic core inductor is a function of flux (or ac current) and operating frequency and is usually used as base performance indicator of inductive component. The inductor quality factor is determined as the ratio of amplitudes of two ground-referenced voltages

$$Q_L \approx \frac{V_{out-pk}}{V_{in-pk}}. \tag{4}$$

Design of inductor should be optimized for a maximum Q_L over a range of frequencies. An appropriate setup for measurement and simulation of Q_L is depicted in Fig. 5. *L, R_{cu}, R_{core}* stand for inductor to be evaluated. A resonant capacitor with values of R_C and C should be also selected in order to resonate with the inductor at certain frequency. V_{in} is a pure sinusoidal voltage source. It is of importance that the quality factor provides an estimation of the total loss. This means that, for instance, core losses can be extracted from its value. It could be done by subtracting out an estimate of the copper loss.

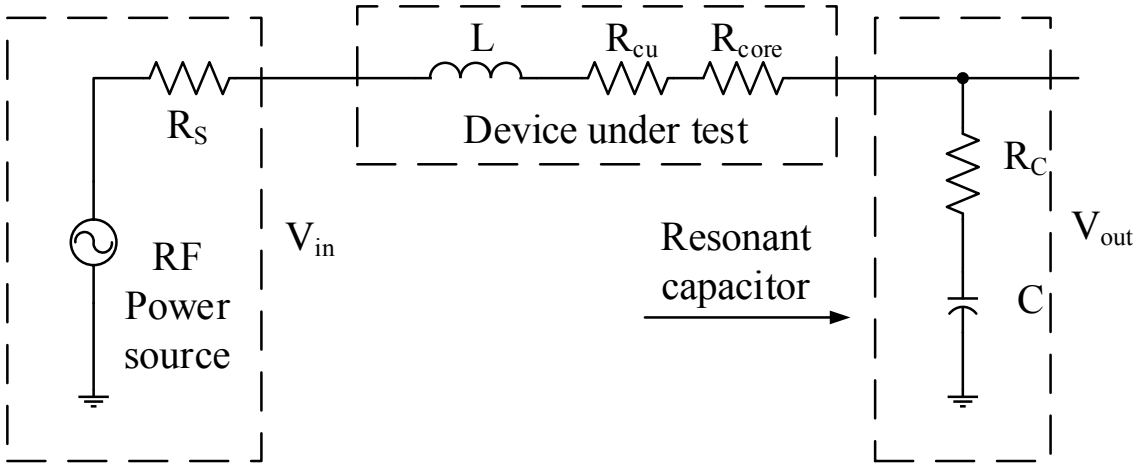

Figure 5. *Setup for measurement of inductor quality factor.*

According to Fig. 5

$$Q_L \approx \frac{2\pi f L}{R_{core} + R_{cu} + R_C} \tag{5}$$

and

$$R_{core} = \frac{2\pi f L V_{in-pk}}{V_{out-pk}} - R_{cu} - R_C. \tag{6}$$

With calculated value of R_{core} we can calculate the average core loss and represent it as a function of flux density

$$P_V = \frac{I_{L-pk}^2 R_{core}}{2V_L} \tag{7}$$

where V_L is a volume of the core.

According to [8], in the very high frequency range it is difficult to find low-loss magnetic materials, but because inductances which are usually being employed by VHF power devices are small, one of the possible alternative is using air-core inductors. In that case the weight and cost of core are eliminated, and issues with nonlinearity, magnetic saturation and permeability variation with temperature are avoided as well. Although, proximity and skin effect bring difficulties in designing low-loss inductors at these range of frequencies, it is possible to overcome those with toroidal configuration of an inductor. In addition, this configuration tends to keep inside large external field of air-core inductors, which causes electromagnetic compatibility (EMC) and electromagnetic interference (EMI) problems. The authors of [8] reported quality factor Q_L of 144 at the frequency of 50 MHz for such a toroidal inductor.

2.7 Effects of parasitic components in high frequency drivers

The practical performance of the driver circuitry involving additional power switches is greatly affected by the parasitic components, whose effect is amplified in applications operating at very high frequencies [9]. It is because of the internal parasitic inductance and parasitic output capacitance of the driver switches, some driver stages, which show acceptable performance provided that they are used in conventional frequency range, are not the applicable solution for very high frequency applications. So far, the parasitic elements in the layout and devices were not considered in driver analysis, however, they demonstrate harmful effect on the behavior of the driver. This holds not only for the efficiency, but also for the final expected gate voltage, during both conduction and blocking phases of MOSFET.

It is worthy of note that, during turn on, power switches in the driver stage discharge their output parasitic capacitance. In addition, switch lead inductances as well as any parasitic inductance due to traces and layout usually add to the external inductances and are employed by the circuit. These inductances have a large impact on the circuit behavior and can cause high frequency parasitic oscillations.

It has been also shown that switch-on time interval affects dramatically parasitic behavior. A simple resonant driver circuit is represented as an example in Fig. 6(a). The equivalent circuit of that resonant driver in case after switch S_1 turn off is depicted in Fig. 6(b).

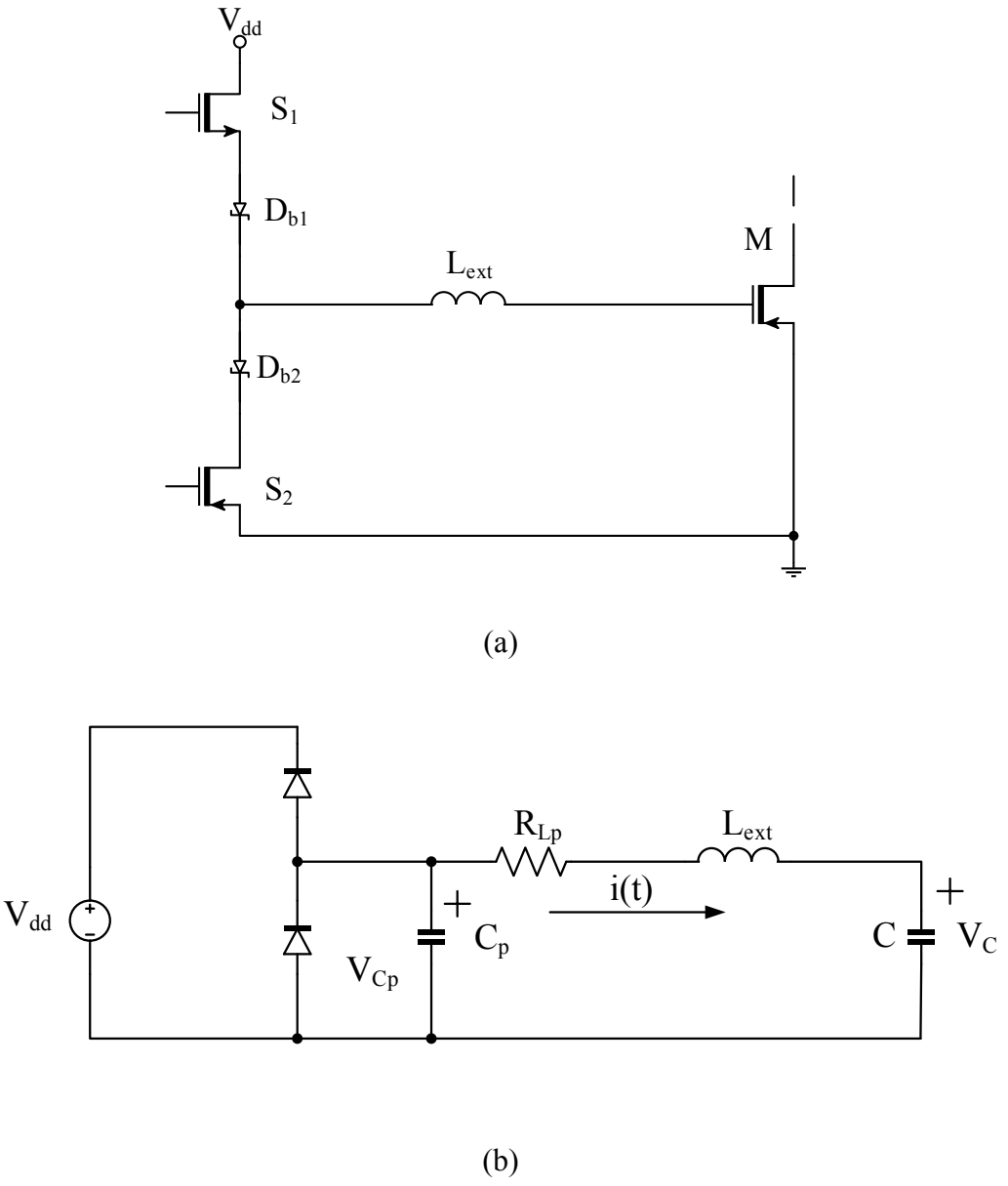

Figure 6. *(a) Power stage of resonant driver circuit. (b) The equivalent circuit of resonant driver.*

Authors of [9] claim that, during short switch-on interval, the S_1 instant occurs when inductor current level large enough to discharge the MOSFET's output capacitance and turn on the S_2 body diode D_2. In this case the parasitic capacitance C_p and load capacitor C are charged to completely different voltages. This in turn leads to damped oscillating waveforms, with a resulting load capacitor voltage affected by relative values of parasitic and load capacitances. Furthermore, the body diodes of MOSFETs are the reason of bounded voltage across the parasitic capacitance. Therefore, the final voltage across load capacitor is much lower than expected in case of unbounded oscillations. However, when the switch-on interval is long enough to commutate at a current level, which is not sufficient to totally discharge the MOSFET output capacitance, the capacitor voltage levels are close to each other and the capacitor voltage drop is lower than in case with bounded oscillations.

To sum up, the switch internal parasitic inductances and switch output capacitances, can greatly affect the circuit performance, causing additional losses and changes in the gate voltages during turn on and turn off times.

2.8 PCB design considerations

The PCB layout design is critical for switched-mode power supply, especially for units that embrace high switching frequencies. EMC (electromagnetic compatibility) and EMI (electromagnetic interference) are among important issues of PCB layout design. Moreover, typical errors in the design may lead to poor output voltage regulation and device malfunction. The following EMC principles are recommended to follow while designing a PCB [10]:

- The noise sources should be identified and eliminated as close to the source as possible. The first possibility for the designer to cope with noise is on the inputs of the system.
- The path to the ground is recommended to control. The circuit designer provides for the noise a path to the ground before noise leaves the system or reaches sensitive signals.
- The large current loops should be avoided. The current loops can be considered as antennas which emit and receive noise. Therefore, loops have to be as small as possible.
- The analog tracks are kept as short as possible as analog signals are sensitive to the disturbances.
- In order to decrease a radiation, 90° corners should be eliminated from traces. 45° angles are used instead.
- The layout is split in zones. The noisy parts are separated from the sensitive components.

The following five steps are proposed in order to make converter's PCB layout design robust [11]:

1. The input capacitor is one of the most important components, which is required for reliable operation of step-down converter. Consequently, it should be the first component to place in the layout after switching transistors. The capacitor is routed right after it has been placed. The excessive voltage spikes can occur due to the switching action and extra parasitic inductance between power and ground capacitor's input terminals. A wide and short connections minimize trace inductance.
2. The second important component to place is an inductor or transformer. Some snubber circuits are sometimes required to reduce EMI by slowing down the rise and fall times of SW (switching node). However, there is a trade-off between efficiency and slowing down the timings. The voltage swing of the switching node is typically from input voltage to ground with very fast rise and fall times. Therefore, it can be considered as a main origin if EMI in switched-mode power supply. To reduce emitted EMI the inductor should be placed as close to switching devices as possible, with the minimum area of switching node copper as copper at SW can be considered as one plate of parasitic capacitor, which is a noise coupling component.
3. The routing of the power components is finalized by placing an output capacitor. The group of power components consists of switching transistors, input capacitor, inductor with optional snubber and output capacitor. The output capacitor is the last component to be connected to the power ground terminal. It should be placed to keep a minimum distance from the inductor back to ground. Vias should not be used for routing these components, as vias add large inductance to the trace.
4. The analog small-signal components are sensitive to noise. They should be routed with short and direct traces in order to keep their noise sensitivity low.
5. The ground planes are usually kept separated: one ground for noisy power components and another for quite small-signal components. Furthermore, these two grounds are usually connected to a single point

To sum up, a main consideration for mitigating the effects from all sources of interference is to route connections as short as possible.

3. CONVERTER DESIGN

This chapter presents the design procedure for the high speed DC-DC converter with self-oscillating control, which is supposed to be assembled on a PCB with discrete components. First, the design specifications will be defined. We will move next to the sizing of the components and issues regarding optimization of the circuit. After that, the simulation results will be presented with discussion about parastics, which were included in simulation model. Finally, the comparison of achieved results with the design specification will be given.

3.1 Design specifications

Table 1 demonstrates specifications, which were chosen for the DC-DC converter. A fixed voltage of 3.6 V is a battery supply. The target frequency f_s is 5 MHz.

Table 1. *High speed DC-DC converter specifications.*

V_{in} (V)	Vout (V)	P_{in} (mW)	f_s (MHz)	η_{max} (%)	D (%)
3.6	1.8	500	5	75	50

3.2 Power stage

The power stage of the proposed High speed DC-DC converter is represented in Fig. 7. It is derived from the [1]. Though, the topology remains the same, some minor changes were applied to the circuit in order to make optimization of the operation reduce total losses and achieve reliable and stable conversion of the voltage.

The modification steps of the circuit include:

1. Additional MOSFETs $M_{2''}$ and $M_{3''}$ were connected in parallel to the cascaded stage of MOSFETs M_2 and M_3.
2. A small filtering inductor L_f was added to the output of the circuit.
3. A single output capacitor C_L was replaced with 3 capacitors connected in parallel.

The forthcoming chapters introduce an explanation and necessity of the performed steps of optimization. Modeling and simulations are carried out in the LTSpice environment.

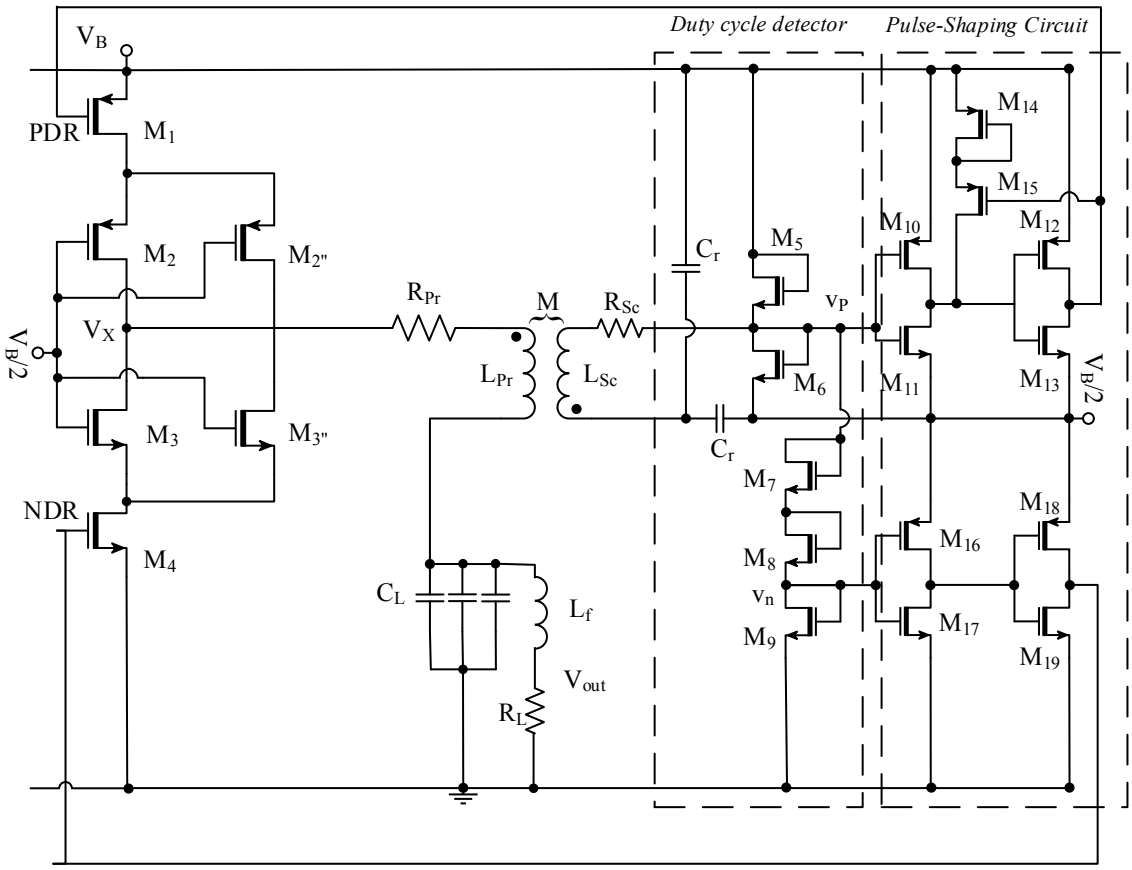

Figure 7. *High speed DC-DC converter with self-oscillating control.*

3.3 Operation of the circuit

A basic functioning of the circuit starts when the output of the p-channel pulse shaper has the level of the voltage high enough for operation of the driver gate. Considering the circuit is switched on, and the supply voltages are increasing in a gradient way. At this moment the switches M_{11} and M_{12} are off, consequently, M_{10} and M_{13} are on. The previous condition should be confirmed with a local positive feedback, which comprises transistors M_{14} and M_{15}. Thus, the transistor M_1 is on and the primary winding of the transformer obtains positive voltage, which is required to cause a negative pulse decreasing the voltage V_p and through the level-shifter (MOSFETs M_7, M_8, M_9) voltage V_n. At that moment, the switch M_{19} is on, and M_4 is off. When all the conditions are fulfilled, the correct operation leads to voltage V_x starts increasing.

The circuit now enters the oscillation mode. The discharging node V_x will cause current through the transformer secondary winding decreases, which in turn switches on M_4. Thus, the switching MOSFETs turned on with a delay and stay both in the on-state,

until switching node *X* is fully discharged. After that the cycle is repeated. The p-mos and n-mos gate pulses with dead time (dashed line) are represented on the Fig. 8.

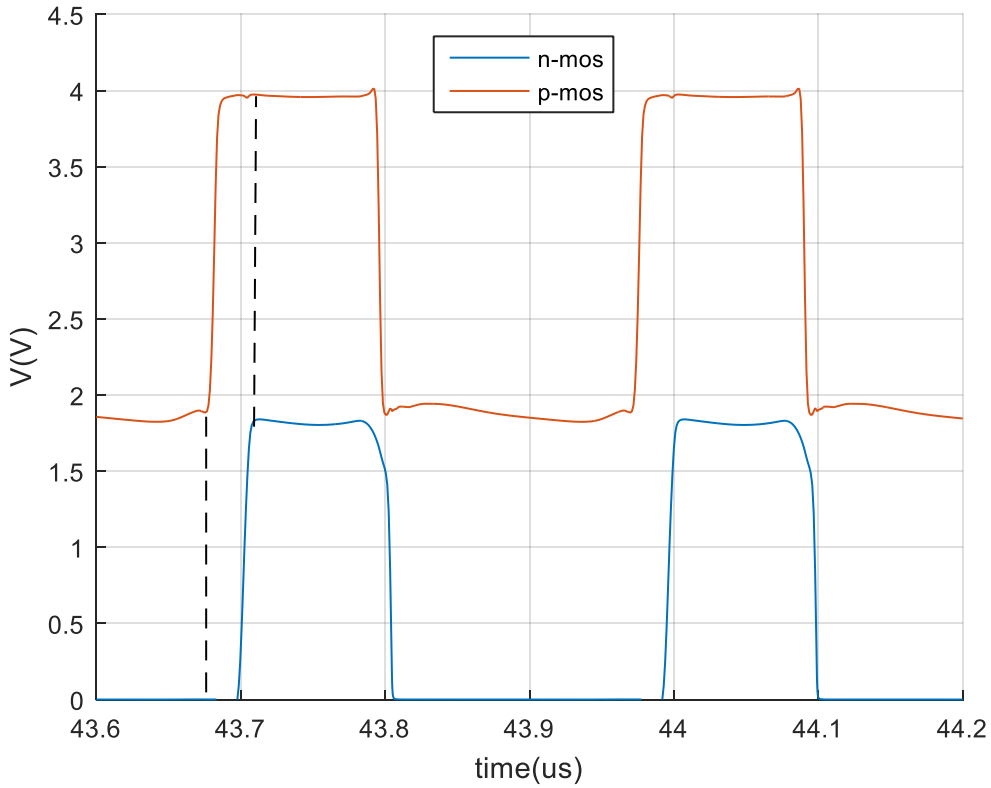

Figure 8. *The gate pulses for main switches.*

The dead time is tuned by means of employing inverter stages (M_{10}, M_{11}, M_{12}, M_{13} for p-mos side, M_{16}, M_{17}, M_{18}, M_{19} for n-mos side), which actually act as buffers. The adjusted delay is 0.02μs. This contributes to reduced switching losses by ensuring that both MOSFETs are not switched on simultaneously.

Furthermore, the probability of appearing shoot-through currents is low (rush of currents when both switches are in on state), therefore enabling enhancements for the improved efficiency of the circuit. The gate pulses of the switching MOSFETs with respect to the occurred drain currents are shown in the Fig. 9. It is clearly seen from the picture that peaks of the currents are allocated outside of the area, when both transistors are turned on.

The circuit operates with a fixed dead-time, which means that the duration of the delay should be chosen carefully. Too short delay can be a main reason of appearing shoot-through currents. However, too long delay is a most likely will lead to increased conduction losses.

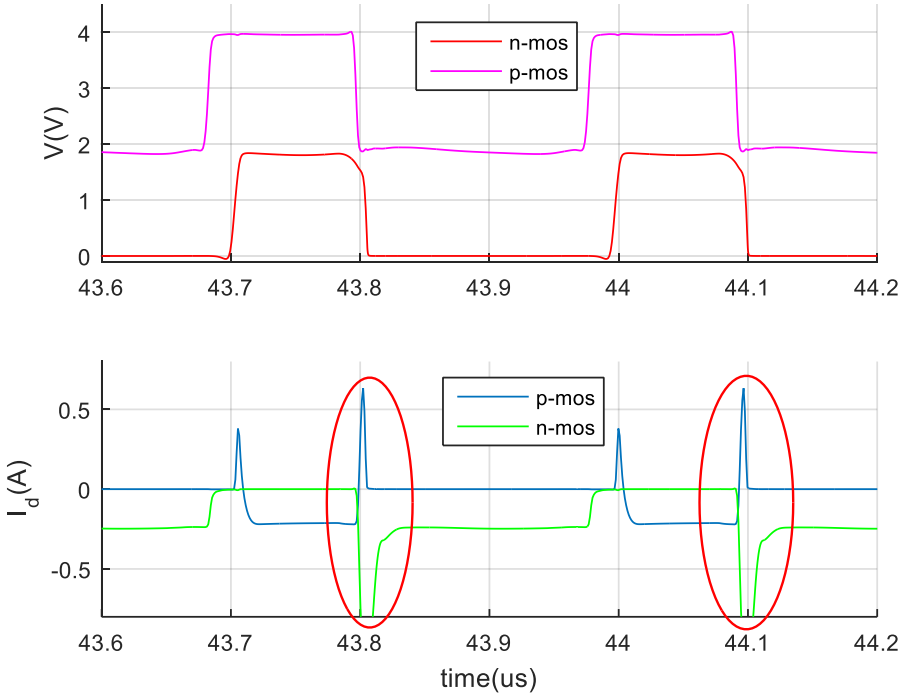

Figure 9. *The gate pulses with respect to drain currents.*

The behavior of the switching node V_x with respect to the current I_x circulating in the transformer's secondary winding depicted on Fig. 10.

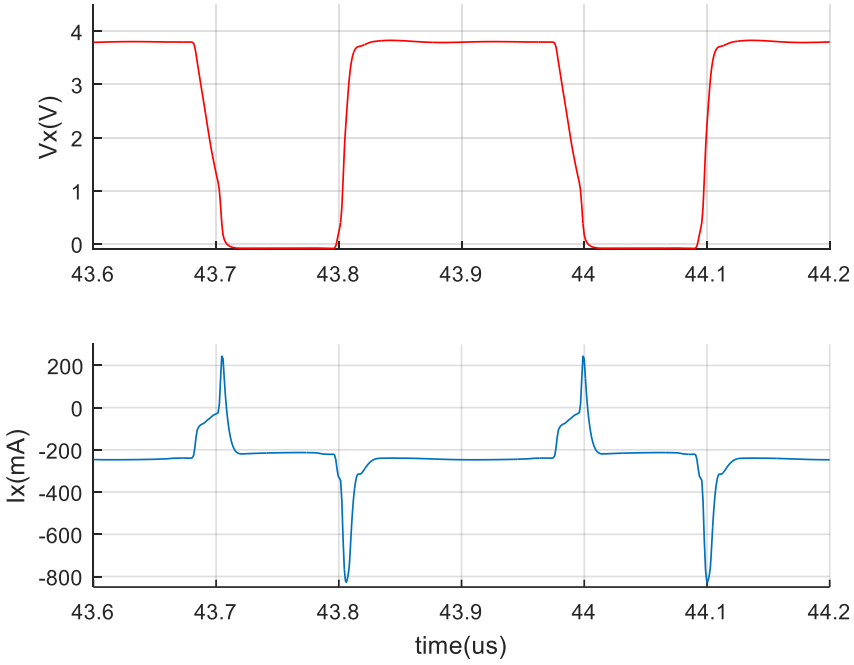

Figure 10. *The voltage and currents waveforms of the switching node.*

3.4 Operation of inverters

The pulse forming block of the designed DC-DC converter contains a tapered buffer stage, which is an essential part of the circuit. It performs several important functions. Firstly, buffer isolates the secondary winding of transformer from the large input capacitance of main switches. Secondly, it forms a square-wave shape signal from distorted input. Finally, it provides a dead-time delay, which depends on the size of buffer. The buffer that comprises two inverter stages is drawn in Fig. 11.

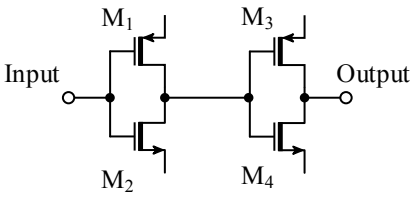

Figure 11. *Inverter stages.*

The distorted voltage that is provided by secondary winding of transformer can be considered as sinusoidal waveform. The output signal, which is used to drive a gate of the main switching MOSFET has a perfect square-wave shape. To some extent, the operation of proposed buffer resembles the one of Schmitt trigger, which tends to remove noise from input signal. The input and output waveforms of inverter stages are represented in Fig. 12.

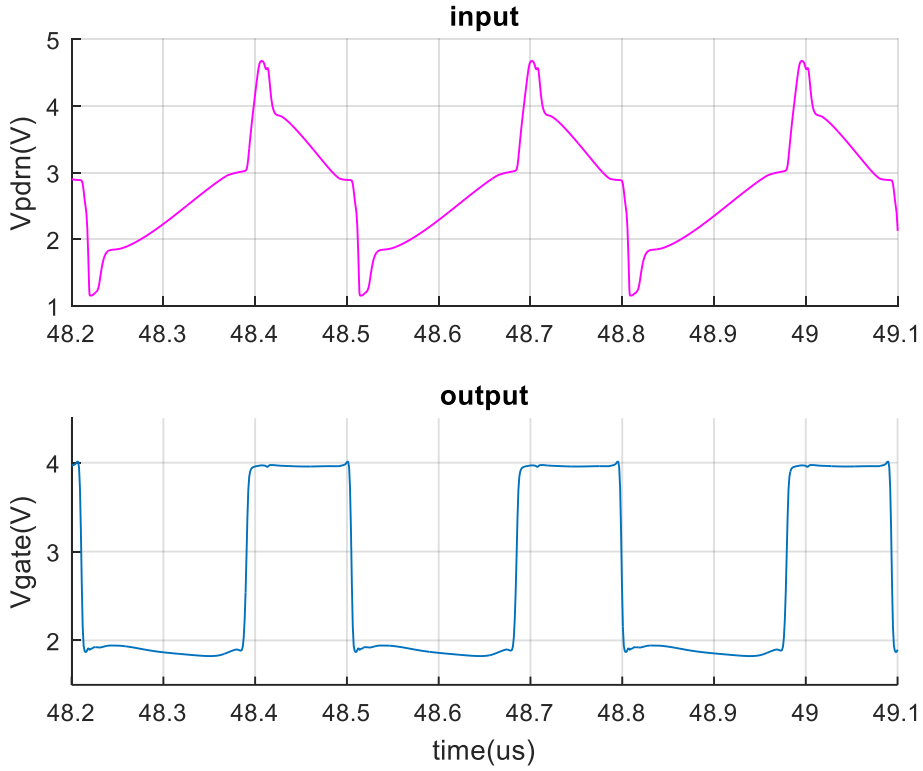

Figure 12. *Input and output waveforms of inverters.*

3.5 Sizing of the MOSFETs

The transistor characteristics depend mainly on the channel width *W* and length *L*. Thus, to obtain a transistor, which suits best to the specified application, *W* and *L* should be adjusted. According to [12], the device constant is defined as

$$K = \left(\frac{W}{L}\right)\frac{KP}{2} \tag{8}$$

where *KP* is as follows

$$KP = \mu_n C_{ox} \tag{9}$$

in which μ_n is the surface mobility of the carriers in channel and C_{ox} is a gate capacitance, which is defined per unit area. Usually, the aforementioned C_{ox} and μ_n are determined by the fabrication process. Therefore, the design process can be affected mainly by varying the aspect ratio *W/L* in order to obtain transistor, which is suitable for certain parts of the circuit.

The approach of matching was used in the modelling process of the High speed DC-DC converter with self-oscillating control. By using this approach, we were aimed to match *W/L* of the discrete MOSFETs to those, which were used in the integrated circuit design process [1]. The aspect ratio of discrete components was scaled accordingly to the *W/L* of the transistors that were designed and simulated at 45 nm CMOS technology.

First, the MOSFETs' parameters were extracted from the IC schematics. The channel width and V_{DS}, I_{DS} for the certain DC operating point are represented in Table 2. The channel length *L* is the same for all the transistors and equals to 150nm. The supply voltage is 3.6V.

Table 2. *The MOSFETs' parameters from IC design.*

Transistor	Width (µm)	V_{DS} (V)	I_{DS} (mA)
M_1	4800	-0.8	-36.02
M_2	4800	-0.83	-36.02
M_3	2100	1,63V	0.000037
M_4	2100	1,79V	0.000037
M_5	60	0.9	5.65
M_6	60	0.89	5.47
M_7	1.50	0.89	0.179
M_8	1.50	0.89	0.179
M_9	1.50	0.89	0.179
M_{10}	230	-0.44	-6.92
M_{11}	130	1.35	6.93
M_{12}	920	-1.79	-0.377

M_{13}	480	0.00154	0.377
M_{14}	50	-0.44	-0.018
M_{15}	50	-0.64	-0.018
M_{16}	210	-0.24	-5.15
M_{17}	100	1.55	10.32
M_{17}	690	-1.8	-0.000874
M_{18}	360	0.000004	0.000874

After the suitable discrete components having been identified with respect to the aspect ratio *W/L,* the next step is to evaluate transistors' performance. Usually it is done by measuring the f_t of a transistor. The f_t is a unity gain frequency of the transistor's current gain

$$|A_i| = \left|\frac{i_{ds}}{i_{gs}}\right| = \frac{g_m v_{gs}}{\omega C_{gs} v_{gs}} = \frac{g_m}{\omega C_{gs}} \tag{10}$$

where A_i is a current gain, i_{ds} is a drain current, i_{gs} is a gate current, g_m is a transconductance, ω is a frequency and C_{gs} is a gate-source capacitance. Thus, when A_i=1

$$f_t = \frac{g_m}{2\pi C_{gs}} \tag{11}$$

Therefore, from (10) it is clearly seen that the value of f_t is proportional to the transconductance g_m and inversely proportional to the gate-source capacitance C_{gs}.

In order to define f_t, which could be also considered as speed of the transistor, the measurement setup was established in the simulation environment. The parameters of the test bench are in the Table 3. The circuit is represented in Fig. 13.

Table 3. *Test bench parameters for MOSFETs' performance measurements.*

V_{ac} (V)	V_{DC} (V)	R_1 (kΩ)	R_2 (kΩ)	R_3 (Ω)	C (nF)
1	5	10	10	50	1

The voltage source at the output acts as a short circuit and provides bias. The voltage source at the input with AC magnitude of 1 makes available the direct measurement of the current gain.

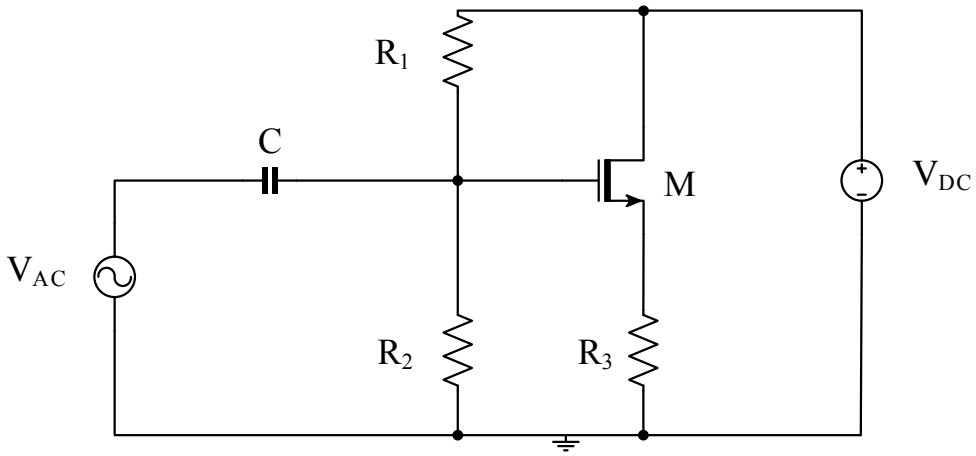

Figure 13. *Power stage of f_t measurement test bench.*

The Fig. 14 shows the f_t characteristic of the p-mos main power switch (M_1 in Fig. 7). The identified frequency before magnitude drops to zero is 150 MHz, which makes this particular transistor suitable for high-frequency applications.

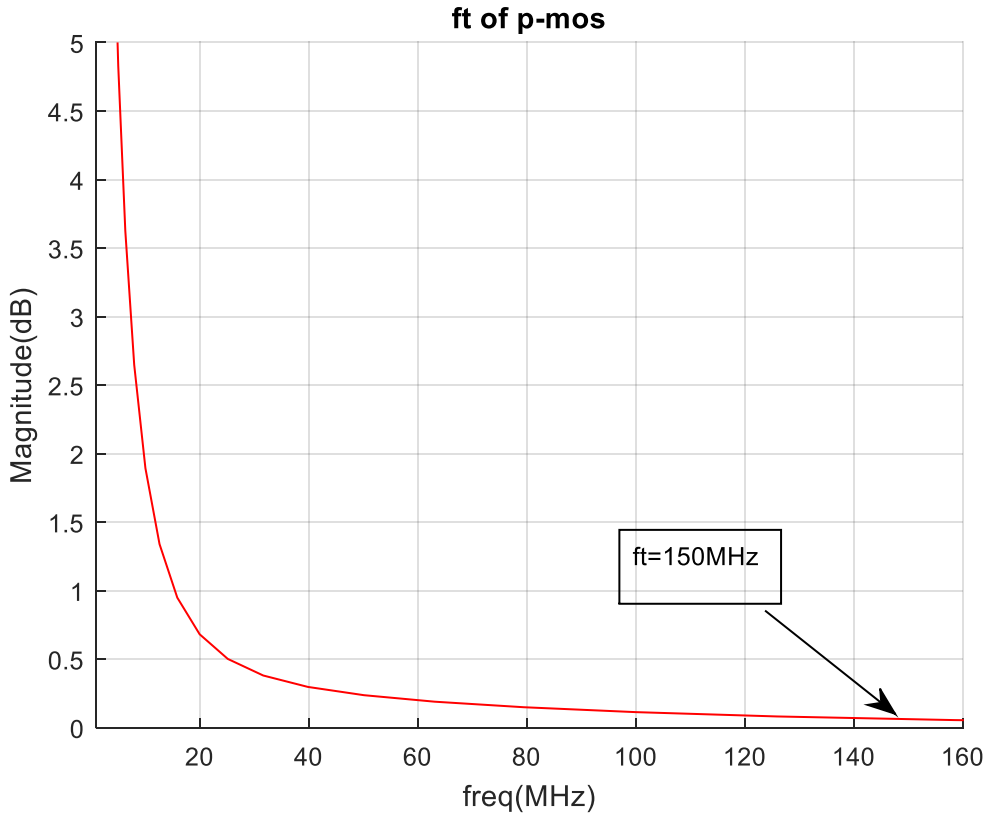

Figure 14. *f_t characteristic of the p-mos main switch.*

The performance of the n-mos side switch (M_4 in Fig. 7) is given in Fig 13. The unity gain frequency equals to 450 MHz. Therefore, the proposed MOSFET suits for high frequency applications. Exactly the same procedure was carried out for all the

transistors, which are included in the circuit drawn in the Fig. 7. Their f_t curves, however, are not presented in this work.

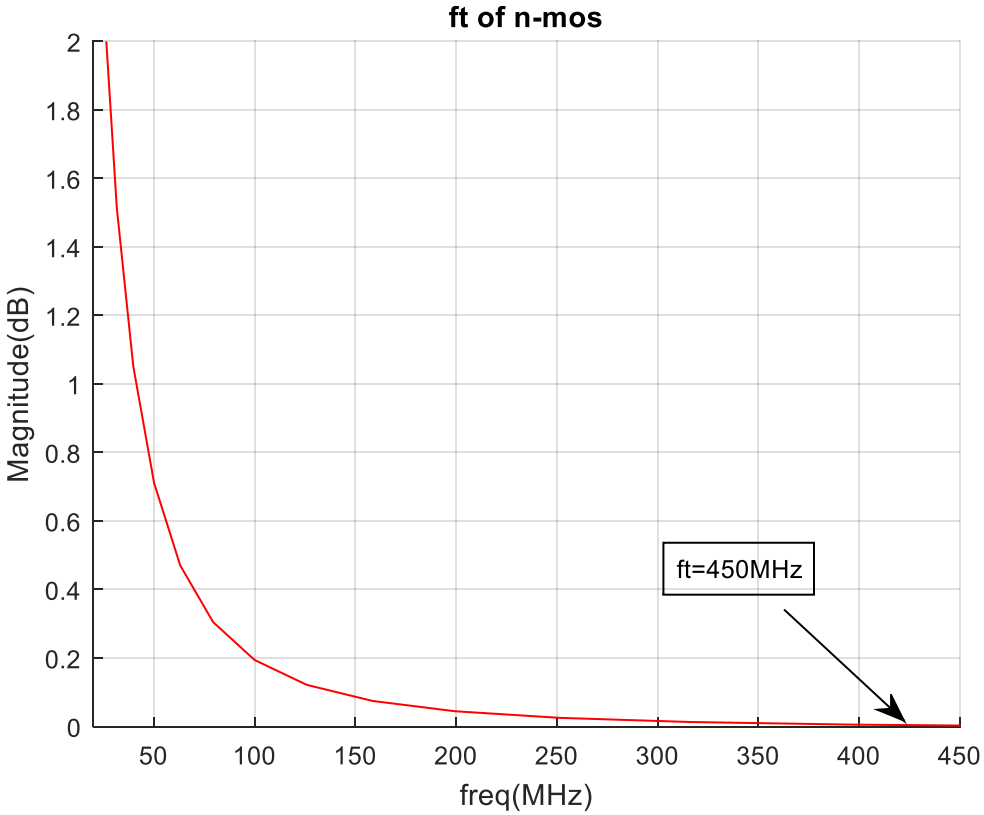

Figure 15. *f_t characteristic of the n-mos main switch.*

It is worthy of note that, cascaded structure of the transistors M_2 and M_3 intends to improve the efficiency of the circuit, ensures that V_{gs}, V_{gd} and V_{gb} do not exceed the maximum voltage difference and contributes to avoiding gate breakdown. However, it has been observed during simulation rounds, that sufficient additional losses occurred in that particular power stage (the loss contribution diagram will be presented in the forthcoming chapters).

As we stated in the previous chapters, the switching losses are comparably low in respect to the conduction losses. Consequently, the optimization of the circuit was performed leading to connecting additional MOSFETs in parallel with M_2 and M_3 ($M_{2''}$ and $M_{3''}$ in Fig. 7). This modification allowed us to achieve lower on-resistances and reduce conduction losses. Nevertheless, it should be noted that during assembling phase of the real prototype, other issues, which are related to paralleling of semiconductors, are also of concern. For instance, equalization of junction temperatures of each device.

3.6 Selection of the transformer

The authors of [1] stated that oscillation period of the proposed VHF self-oscillating DC-DC converter can be evaluated as

$$2T = \frac{2\tau_1\tau_2}{(\tau_1 - \tau_2)} \cdot \ln\left(\frac{\tau_1 + \tau_2}{\tau_2}\right) \tag{12}$$

where τ_1 and τ_2 are time constants

$$\tau_1 = \frac{L_{Pr}}{R_{Pr}} \tag{13}$$

and

$$\tau_2 = 2C_r R_{Sc} \tag{14}$$

where L_{Pr} is inductance of the primary winding of the transformer, R_{Pr} its series resistance, C_r is a capacitor of duty cycle detector, R_{Sc} is a series resistance of the transformer secondary. Therefore, the oscillation frequency is defined by the transformer parameters L_{Pr}, R_{Pr}, R_{Sc} and value of the capacitor C_r.

It is obvious from the (12) and (13) that decreasing inductance value of the transformer's primary winding leads to increasing switching frequency. This dependence is considered as an advantage of high frequency applications as it contributes to achieving small sizes of the bulky energy storage elements. Nevertheless, many of the inductive and magnetic components incur high losses at the operation frequencies, which are in megahertz range.

In our design process, after achieving a certain operating frequency with specific inductance value of the transformer, the characteristics of the selected transformer were determined by measuring its quality factor Q_L. The measurement setup, which was used for determining Q_L is shown in Fig. 16.

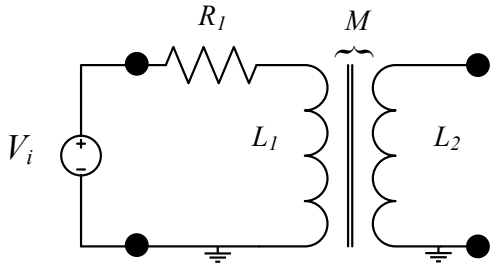

Figure 16. *The measurement setup for determining quality factor of the transformer.*

Based on the test bench simulation results, the quality factor of the transformer was estimated as

$$Q_L = \frac{Im(Z_{11})}{Re(Z_{11})} \tag{15}$$

The obtained quality factor for the certain operating frequency of 3.5MHz is presented in Fig. 17.

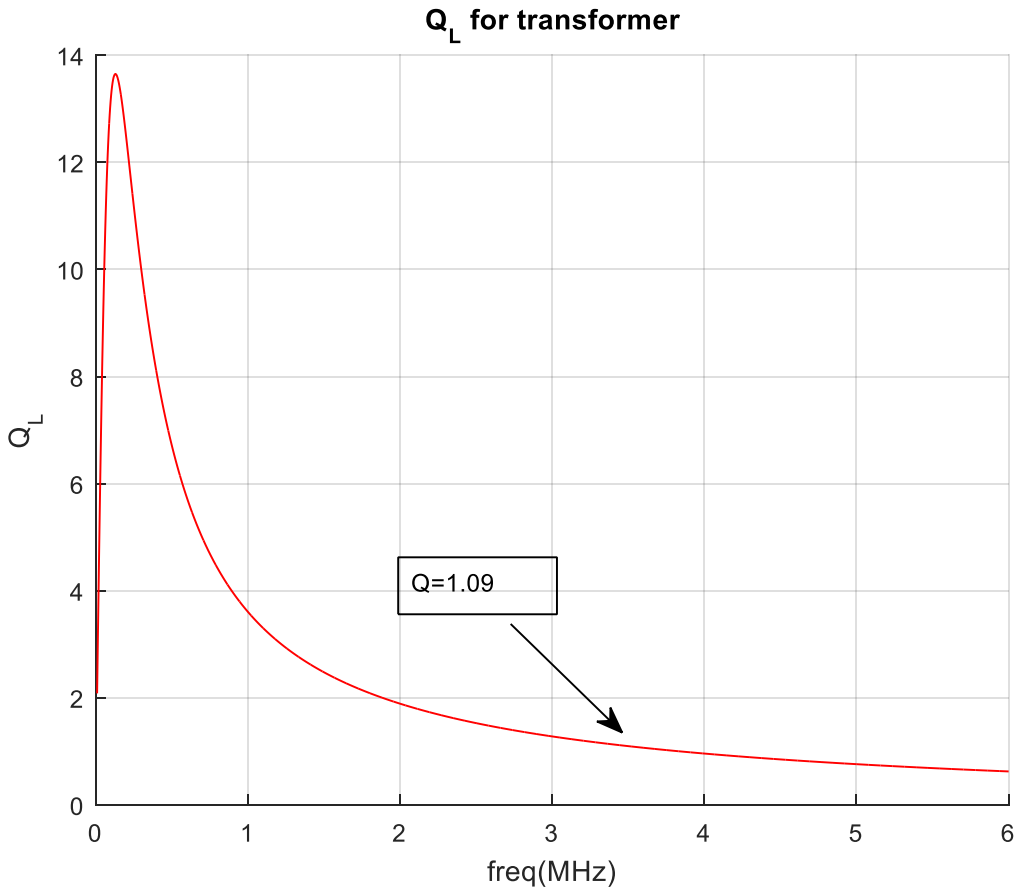

Figure 17. *Quality factor of selected transformer.*

Simulation results show that the highest Q_L of 13.5 is achieved at the frequency range of 400-500 kHz. However, the quality factor doesn't drop to zero value before 6 MHz and for 3.5 MHz it equals to 1.09, which is acceptable for operation of the designed high speed converter and confirms that selected transformer will not incur significant resistive losses.

It is worth noting that not only resistive losses in the transformer are of concern in high frequency applications, but also behavior of the winding, which can be possibly dominated by capacitance. To better understand the process, the equivalent circuit of the transformer winding is drawn in Fig. 18.

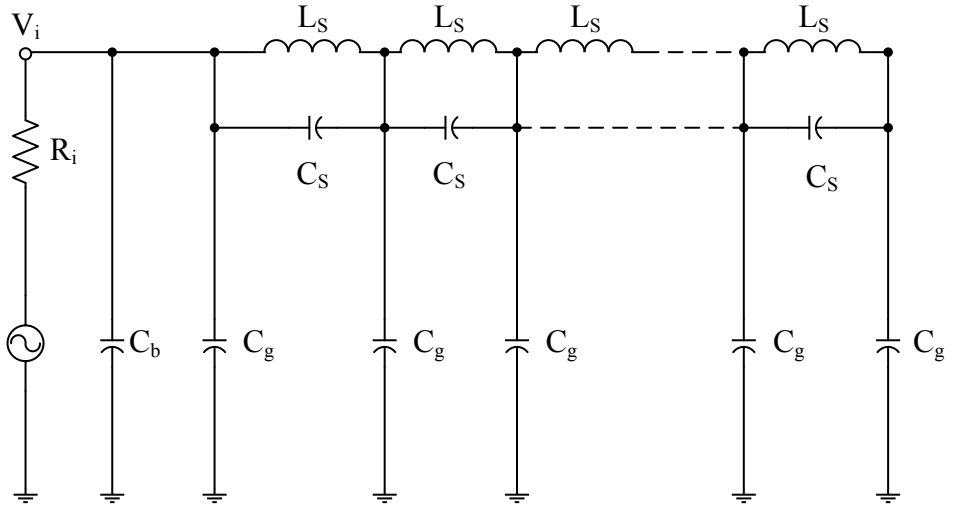

Figure 18. *The equivalent circuit of the transformer winding.*

The equivalent circuit consists of the cascaded π sections and comprises winding inductance L_S, ground capacitance C_g and series capacitance C_s. The number of π sections is usually equal to the number of winding turns. An impedance frequency response test was carried out for wide range of frequencies. Simulation result is depicted in Fig. 19.

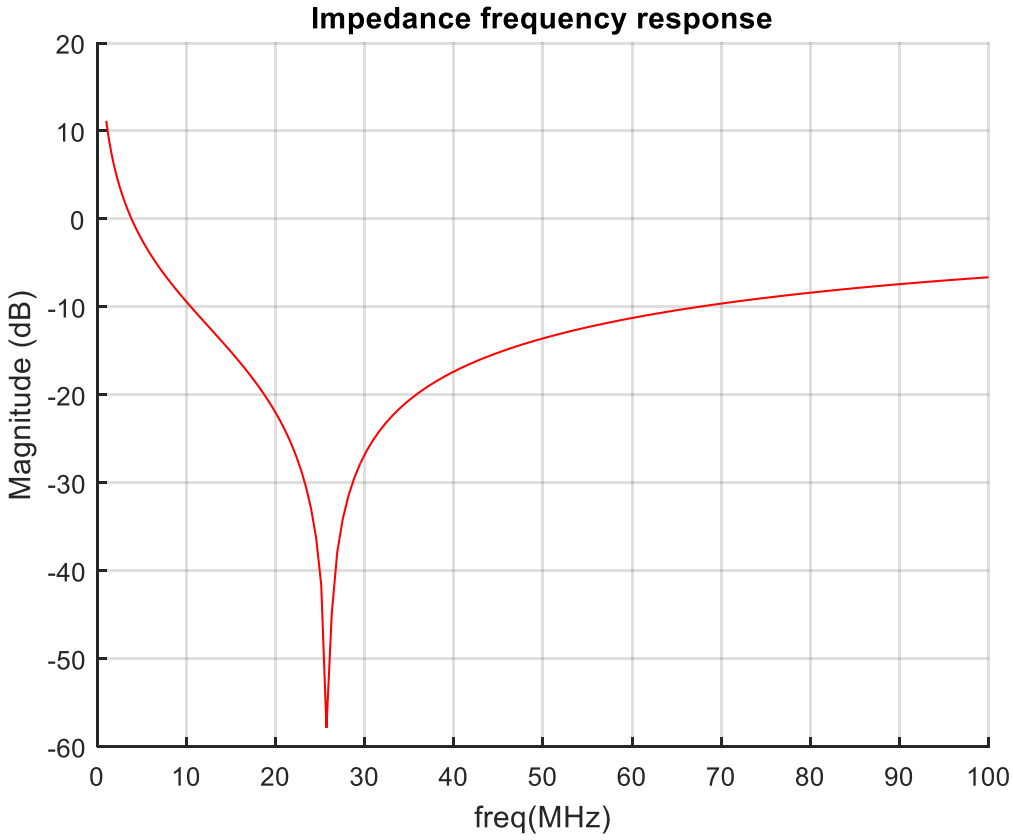

Figure 19. *Impedance frequency response of winding.*

A dominant capacitance effect can be clearly observed in the Figure 19 for frequencies above 25 MHz. The reason of such behavior is in distributed capacitance, which shunts the winding inductance. However, based on the simulations, we can state that selected transformer is suitable for our particular circuit with target frequency f=5 MHz.

3.7 Selection of the capacitors and design of output filter

As was stated in the previous chapters, the transformer's primary winding L_{pr} of the self-oscillating DC-DC converter (Fig. 4) is used to transfer power to the load. Moreover, it can be considered also as a substitute to the traditional load filter coil. Therefore, in order to diminish the output voltage fluctuations, a low-pass filter comprising capacitor and inductor should be used. The cut-off frequency was selected to be lower than the target frequency in order to effectively cancel the switching frequency ripple in the V_{out}. The corner frequency was defined as follows (the parameters of the selected components will be presented in the forthcoming chapters)

$$f_c = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{1 \cdot 10^{-6} \cdot 2.2 \cdot 10^{-9}}} \approx 3.39\ MHz \tag{16}$$

It is worthy of note, that in the analysis of the conventional DC-DC converters the output capacitor is usually assumed to be as large as to provide $v_o(t)=V_o$. However, based on observations, the particular high speed DC-DC converter suffers diminishing switching frequency and reducing efficiency while increasing value of the output capacitance. Thus, for that particular design, there is a tradeoff between quality of the output voltage and speed of the converter, both depending on value of the filter capacitance and tending to keep that value as low as possible.

One of the important issues concerning high frequency behavior of the capacitor is an equivalent series inductance ESL, which rapidly increasing effect on impedance becomes of concern in the frequency range above a few megahertz. However, before that point a decreasing impedance is delivered with increasing frequency, which is particularly desirable. The selected output capacitor has been tested by employing the similar test bench that is depicted on Fig. 16. An impedance frequency response is represented in Fig. 20.

The results show that selected capacitor is suitable for very high frequency applications. The dominant inductive behavior is explicit at the frequency range above 300 MHz. At the certain frequency of 3.5 MHz the associated impedance is 35 dB or 1.42 Ohm. Nevertheless, the simulation of the circuit operation showed that high losses incurred in that single capacitor. Therefore, a parallel connection of three capacitors with the same total equivalent capacitance was accepted.

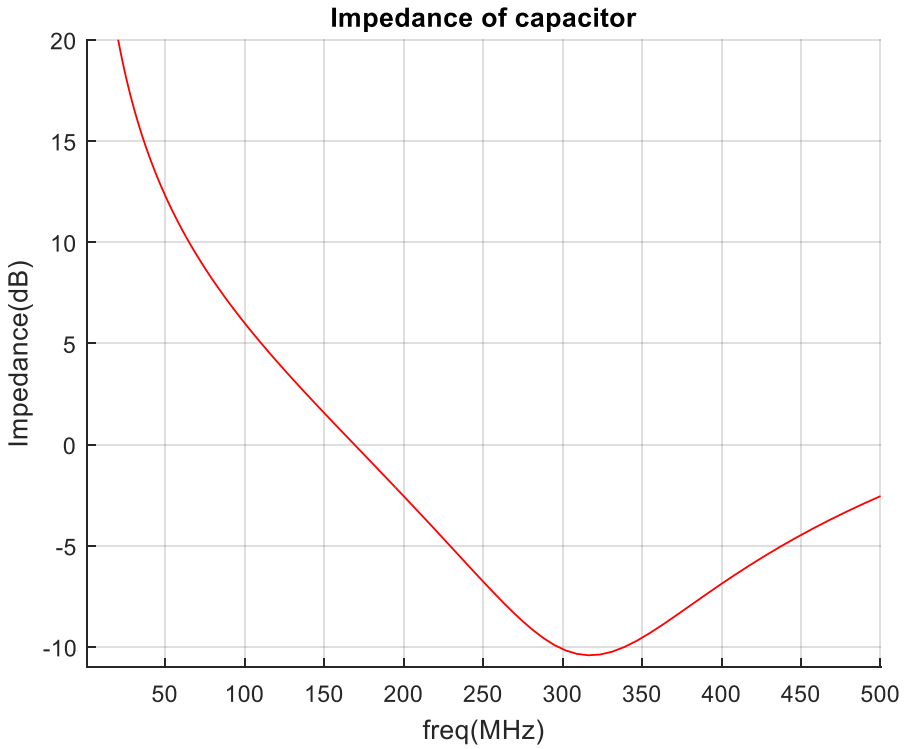

Figure 20. *Impedance frequency response of the capacitor.*

The impedance response of three parallel capacitors in comparison with single capacitor is presented in Fig. 21.

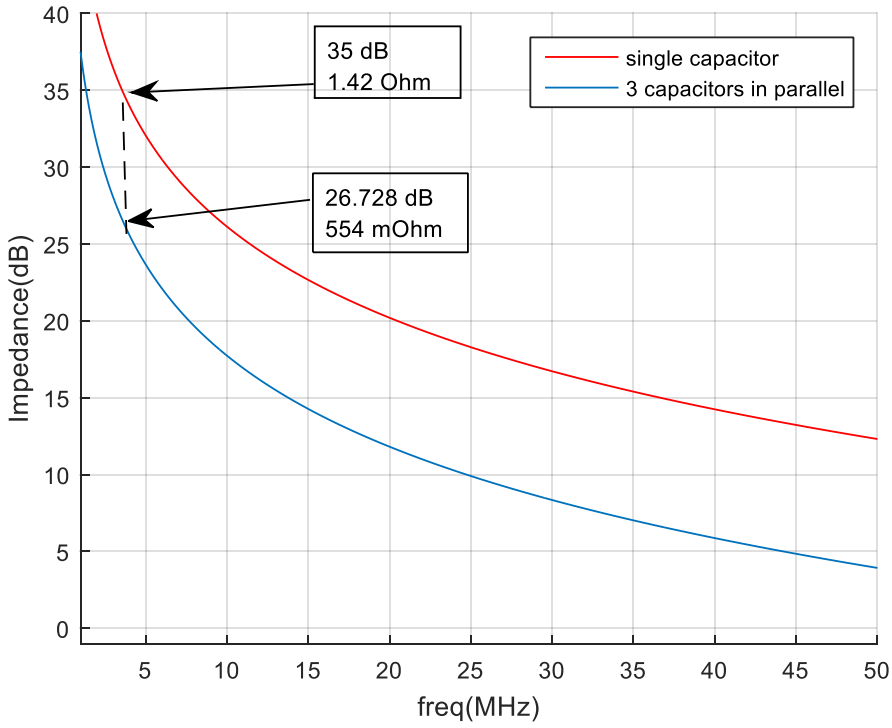

Figure 21. *Impedance frequency response of the capacitors connected in parallel.*

The previous graph shows that having three capacitors connected in parallel effectively reduces total impedance while delivering the same high frequency performance. The determined impedance at the certain frequency of 3.5 MHz is 26.728 dB or 554 mOhm.

Considered low-pass filter comprises also load resistor R_L, which provides damping to the output circuit. However, the output voltage waveform of designed converter showed a poor shape and high peak-to-peak ripple. This allows to conclude that previously made assumptions for the integrated circuit do not hold for circuit, which is designed for PCB assembling. Based on this the output filter was expanded further to third-order low-pass filter by adding a small inductor L_f in parallel with output capacitance. The obtained structure of the designed filter is referred to Cauer topology and depicted in Fig. 22.

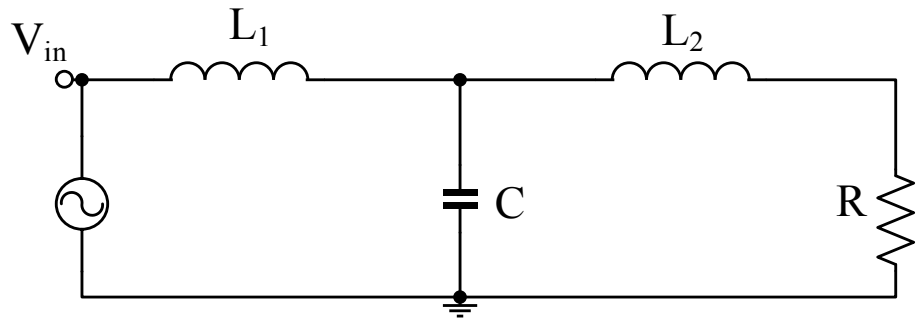

Figure 22. *Cauer filter topology.*

The selection procedure of the output capacitors, which is described in this chapter holds also for capacitors C_r (Fig. 7). As was mentioned before, according to (14) the value of this capacitor contributes to the switching frequency and in order to obtain high speed, the capacitors C_r should be small enough. After a few rounds of simulations the desired capacitance value was identified and impedance frequency response test was carried out. The obtained characteristic is depicted in Fig. 23.

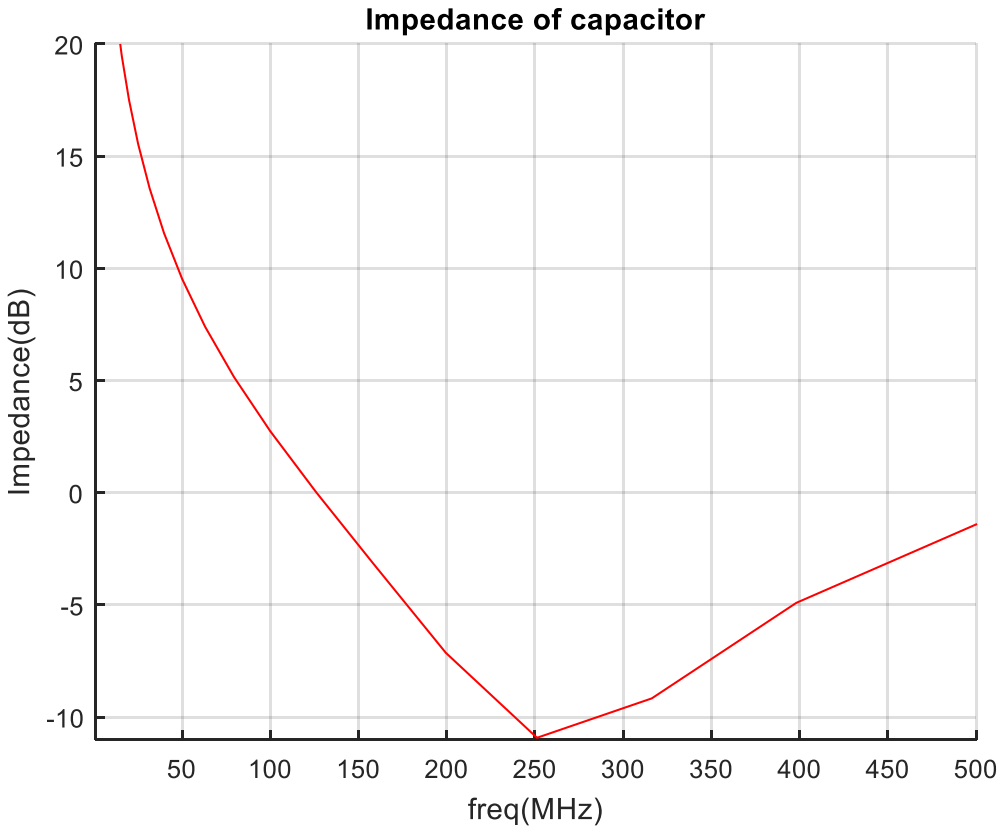

Figure 23. *Impedance frequency response of capacitor* C_r.

3.8 Parasitic effects

The parasitic effects were also included in the LTSpice simulation environment in order to test switching operation of designed converter as close to real conditions as possible [13]. Since parasitics are unavoidable in high frequency applications, their impact cannot be underestimated.

There are two main types of the parasitic effects, which are taken into consideration in this work. First, a PCB parasitic, which comprises component values and trace and depends mainly on length and width of trace as well as on switching frequency. Second, a parasitic inductance and equivalent series resistance, which are included in the static model of battery. The test bench presented in Fig. 24 implies a minimum influence of PCB layout parasitic effects produced by the traces.

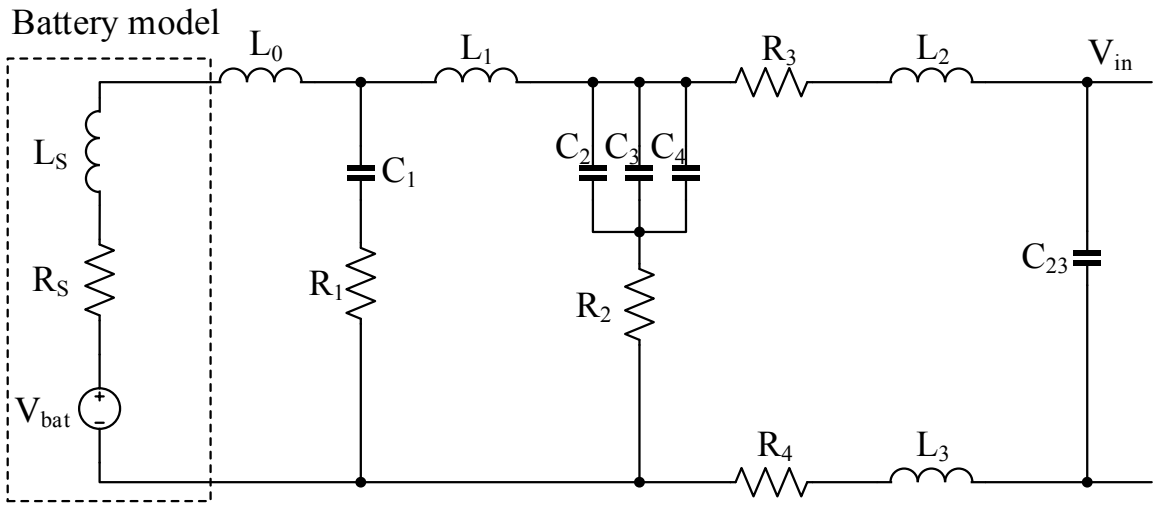

Figure 24. *Test bench with parasitic components.*

All the parasitic components are presented in Table 4.

Table 4. *Parasitic components.*

Parameter	Value	Origin
R_1, R_2	10 mΩ	Trace resistance+via
R_3, R_4	5 mΩ	Trace parasitics
L_2, L_3	100 pH	Trace parasitics
L_1	1 nH	VDD plane
C_{23}	2 pF	PCB parasitic

It is worth noting that test bench, which is presented in Fig. 24 includes not only parasitics, but also additional discrete components. The main purpose of these components is to reduce switching noise. The decoupling capacitor C_1 contributes to improved efficiency and reduced power consumption by providing part of the current when discharging C_1. Therefore, the current drawn by battery is less comparable with the case when decoupling capacitor is not used.

The switching noise effect is reduced by employing decoupling capacitors C_1, C_2 and C_3. It is usually desirable to use large capacitors, which usually show a better performance in terms of inhibiting the noise, however, they introduce a low resonance frequency at the same time, which is considered to be a restriction. Therefore, capacitors with small values were connected in parallel.

In addition to the designed output filter, a small inductor L_0 has been included in order to decrease contribution of the switching noise by suppressing its high frequency components. The discrete components values are introduced in Table 5.

Table 5. *Discrete components.*

Component	Value
L_0	68 nH
C_1	4.7 µF
C_2	100 nF
C_3	100 pF
C_4	2.2 nF
L_S	25 nH
R_S	180 mΩ

Furthermore, a parasitic trace resistances and inductances were added to the output stage of the converter as depicted in Fig. 25. The stage includes also effect of ground plane.

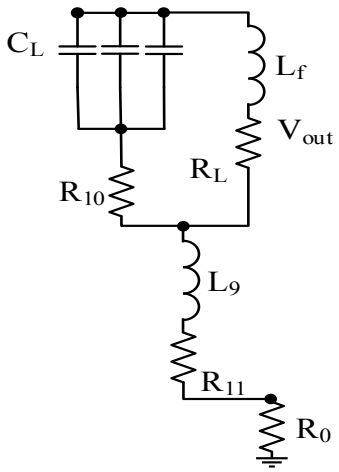

Figure 25. *Parasitic effects at the output stage of the circuit.*

The corresponded values of output stage parasitics are included in table 6.

Table 6. *Output stage parasitics.*

Parameter	Value	Origin
R_0	3 mΩ	Ground plane
R_{10}	10 mΩ	Trace resistance
R_{11}	5 mΩ	Trace parasitic
L_9	10 pH	Trace parasitic

4. SIMULATION RESULTS

This section brings under discussion simulation results, which were obtained while operating designed circuit with battery model and parasitic impacts of the PCB. The results will be compared with target design specifications and possible future modifications are suggested in order to achieve converter specifications.

4.1 Designed parameters

Based on the design process that is described in Chapter 3, the components with specified values are selected and represented in Table 7.

Table 7. *Parameters of the components.*

Component	Value	Manufacturer part number
L_{Pr}	1 µH	750312547
L_{Sc}	416 nH	750312547
R_{Pr}	30 mΩ	750312547
R_{Sec}	48 mΩ	750312547
C_r	1.2 nF	GRM155R71H122KA01
C_{L-1}	820 pF	GRM155R71H821KA01
C_{L-2}	390 pF	GRM155R71H391KA01
C_{L-3}	1 nF	GRM155B11E102KA01
R_L	10 Ω	ERC65-500
L_f	60 µH	B82134A5701M000

The chosen transistors are listed in the Table 8.

Table 8. *List of the MOSFETs.*

Designation	Manufacturer part number
M_1, M_2, $M_{2''}$, M_{10}, M_{16}	Si1315DL
M_3, $M_{3''}$, M_4, M_{11}, M_{17}	SIB912DK
M_{12}, M_{18}	Si1553CDLP
M_{13}, M_{19}	Si1553CDLN
M_5, M_6, M_7, M_8, M_9	US6M1
M_{14}, M_{15}	VT6M1

4.2 Output waveforms

A waveform of the converted voltage V_{out} is depicted in the Fig. 26. The operation of the designed high-speed DC-DC converter shows an acceptable quality of the output voltage and low ripple.

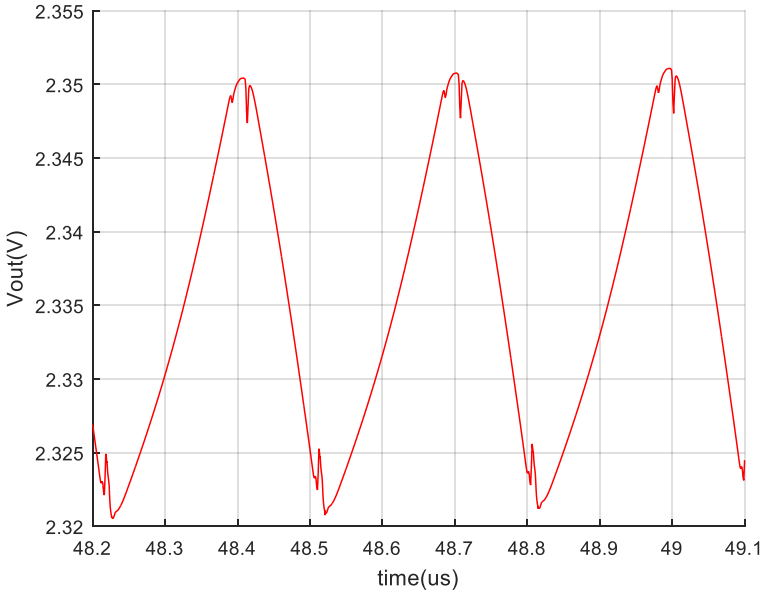

Figure 26. *Output voltage waveform.*

A waveform of the voltage V_p that is required to obtain driving signals as well as to provide correct start-up of the circuit demonstrates an appropriate behavior. A graph of the V_p is presented in Fig. 27.

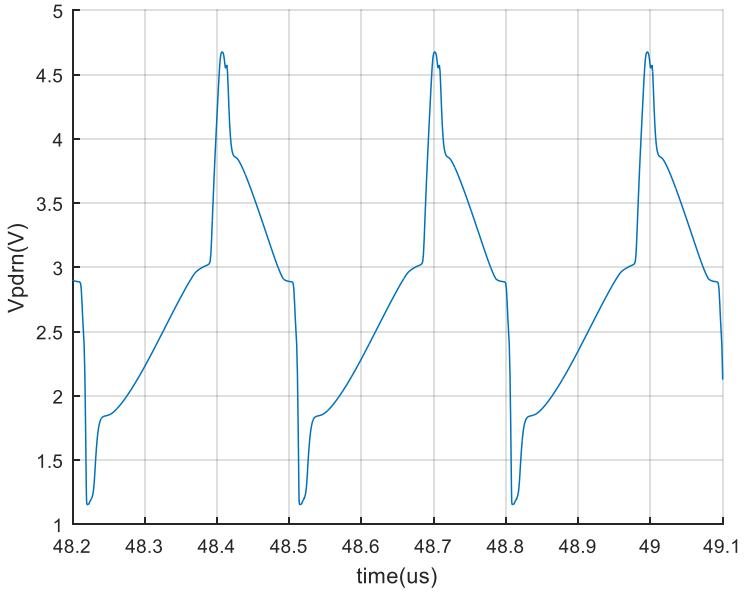

Figure 27. *A waveform of the voltage V_p.*

4.3 Switching noise effect

The parasitic effects, which were previously discussed in Chapter 3 affect the operation of the circuit resulting in switching noise. However, filter components that can be not only external components, but also part of parasitics (as discussed in Chapter 2) make a contribution to the switching noise. This happens because of the charging-discharging parasitic capacitance of inductor during transition from high state to low and vice versa. In addition, a common ground, which is used in PCB design, is also an important generator of the noise. The current flowing from output to the ground creates switching noise at the output.

The second trace of the Fig. 28 shows the impact of the switching noise on the V_{out}. Moreover, switching noise is also observable in the power supply part, particularly at the battery node (third trace in Fig. 28).

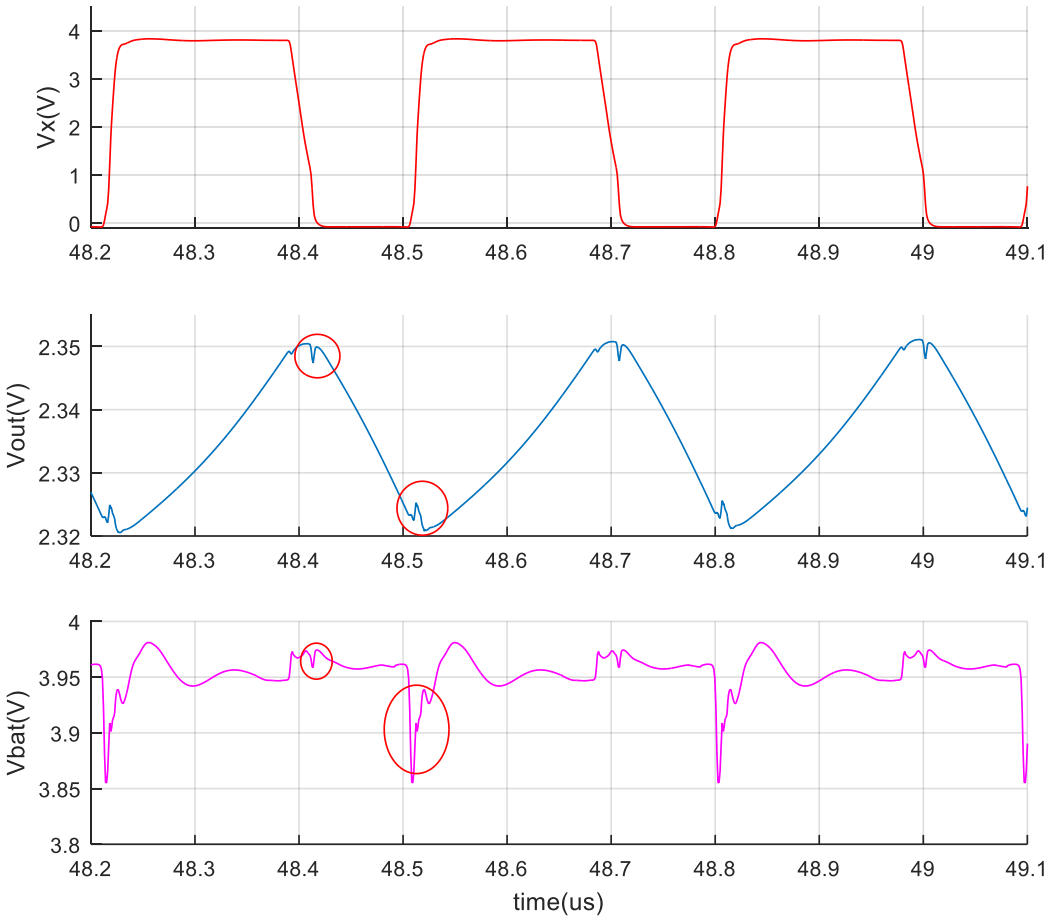

Figure 28. *Effect of the switching noise.*

4.4 Efficiency of the circuit

Efficiency of the designed DC-DC converter is calculated as a ratio between output power P_{out} at the load point and input power P_{in} that is supplied by static battery. The complete results of circuit operation are listed in Table 9.

Table 9. *Simulation results.*

V_{in} (V)	V_{out} (V)	D (%)	P_{in} (mW)	P_{out} (mW)	η (%)	f_s (MHz)
4	2.34	58	781.22	549.62	70.35	3.4

The power losses of each component in simulated circuit were calculated in order to define efficiency of the designed converter. The power loss diagram is represented in Fig. 29.

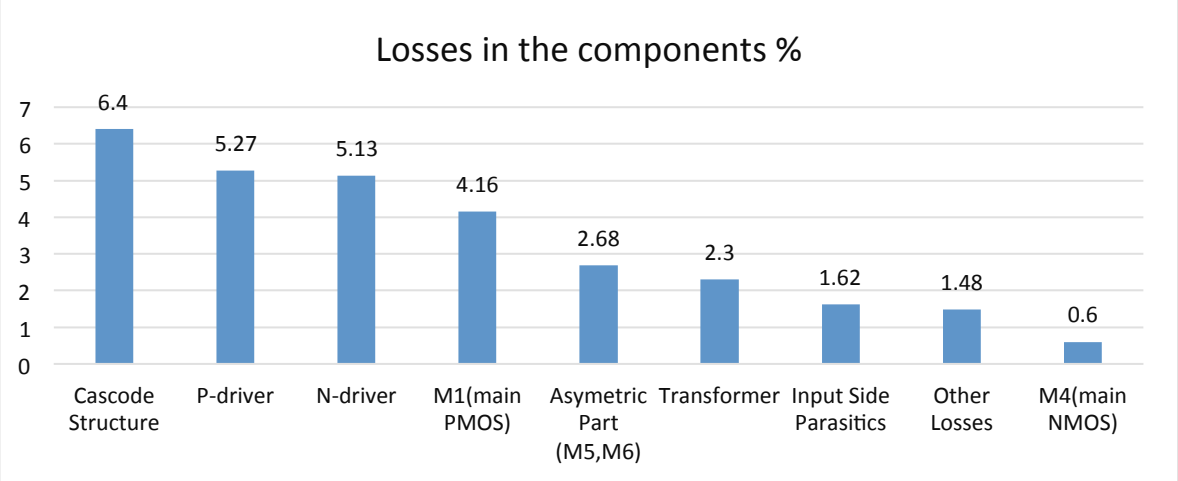

Figure 29. *Loss contribution diagram.*

As might be seen from power loss diagram the main loss contributors are cascaded structure, drivers of both P and N-MOS sides and transistor M_1. Their total impact on power losses is equal to 163.81 mW. Different optimization techniques could be used to improve further efficiency of the circuit. Among those are resonant gate driving and high speed DC-DC dead time architecture [14]. However, application of these methods to the investigated circuit requires additional research activities and changing of the present topology.

For the simulation stability purpose input voltage of 4V was accepted as it proved to demonstrate better performance of the designed DC-DC converter. Nonetheless, the operation of the Li-Ion battery is usually described with varying voltage range from 2.8 to 5.5 V and it depends on level of charge. So designed converter has to be capable of operating at this voltage range.

The modelled high speed DC-DC converter is a self-sustained system, which implies automatic control of the duty cycle. It compensates external disturbances and strives to preserve the operation with a constant duty cycle. In practice it means that duty cycle fluctuates near 50%, which is observable in the present work.

The achieved frequency of operation is dictated mainly by the transformer parameters. In order to reach target or even higher frequencies a transformer with lower inductance values has to be employed. Such a transformer should be designed for that particular circuit as currently presented products in the market do not comply with high frequency power supply needs. Design of the transformer, however, is beyond the scope of this work.

5. HIGH SPEED DC-DC CONVERTER WITH SELF-OSCILLATING CONTROL AND RESONANT GATE DRIVING

This chapter presents integration of the resonant MOSFET gate driver to the proposed DC-DC converter. Different resonant driver topologies are available nowadays. Among those are: a) unclamped turn-on and clamped turn-off; b) clamped turn-on and turn-off; c) unclamped turn-on and turn-off [9]. In this work the clamped turn-on and turn-off resonant driving technique is applied.

5.1 Schematic and operation of resonant gate driver

Gate drive loss is among overall losses occurred in high frequency converters. A resonant gate drive circuit provides efficient energy recovery at charging and discharging periods, thus, eliminates sufficient gate drive loss [15]. In general, resonant gate drive technique employs an L-C circuit in order to charge or discharge the MOSFET's V_{GS}. Moreover, L can be external inductor or leakage inductance of a transformer, whereas C is the equivalent gate capacitance. The utilized resonant gate driver is shown in Fig. 30.

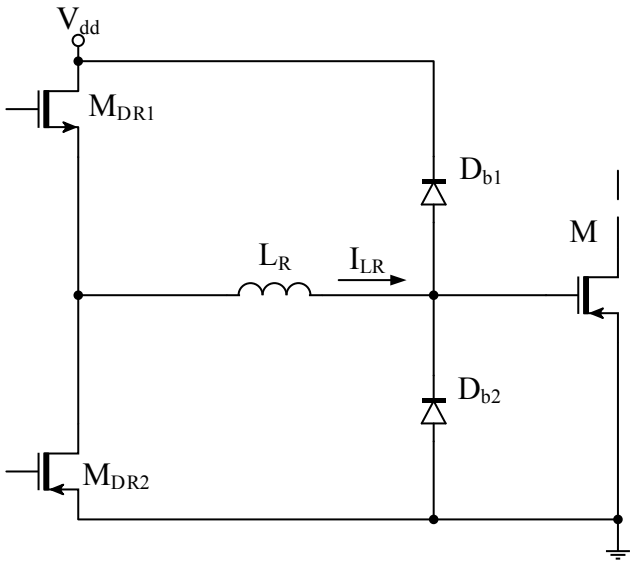

Figure 30. *Power stage of the resonant gate driver.*

In this circuit M_{DR1} and M_{DR2} is a driving pair, L_R is a resonant element (inductor) and D_{b1} and D_{b2} are diodes, which are used to clamp voltage V_{GS} and recover the driving energy. There are three basic steps in energy processing associated with that circuit. First, the energy is transferred from the power source to the resonant inductor and the gate capacitor. Second, the inductor energy is freewheeled. Finally, the energy is returned back to the source. Consequently, the driver itself consumes less power than a conventional driver. This mechanism leads to decreased gate losses as only the small portion of power becomes thermal loss as opposite to case where all the power is dissipated on R_G, where R_G is a total gate resistance. The proposed converter with integrated resonant gate drivers is depicted on Fig. 31.

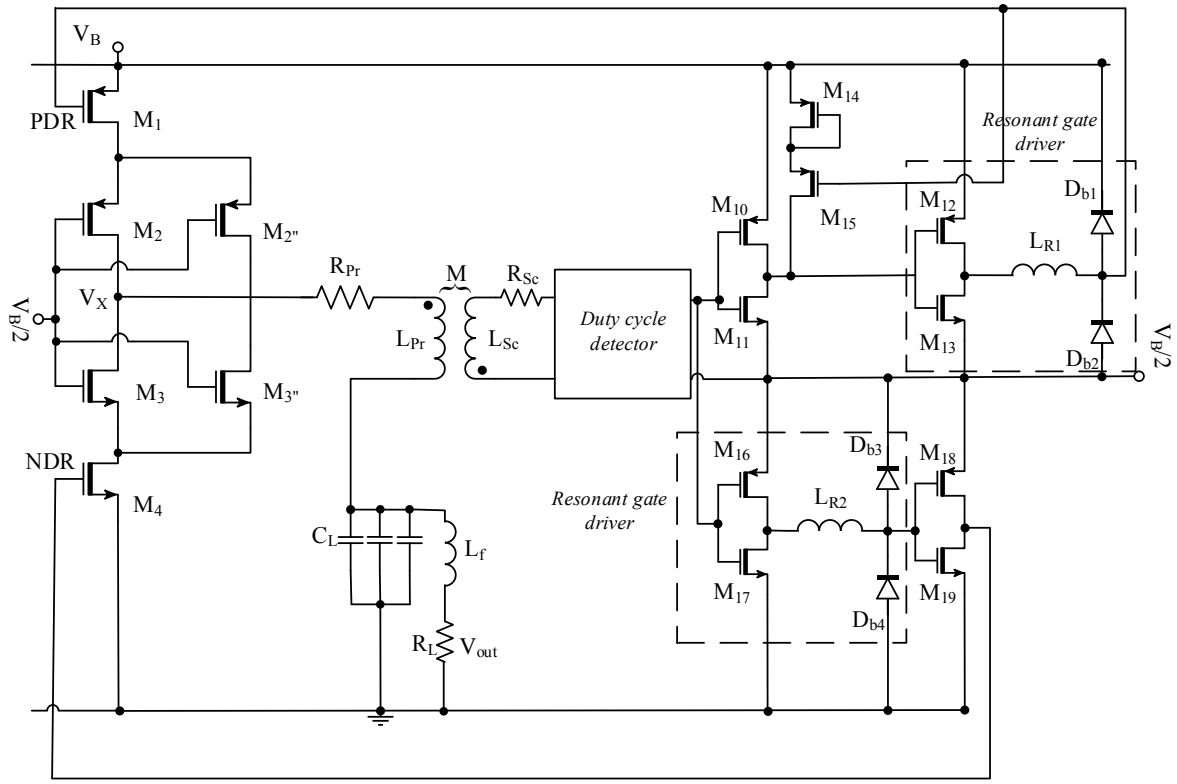

Figure 31. *DC-DC converter with integrated resonant gate drivers.*

Two resonant driver stages are utilized in that circuit. First is incorporated after the output of inverter stage M_{12} and M_{13}. Thus, it aims to drive main p-mos switch M_1. This resonant driver circuitry contains inductor L_{R1}, diodes D_{b1} and D_{b2}. The second is integrated between inverters M_{16}, M_{17} and M_{18}, M_{19} and consists of resonant inductor L_{R2}, diodes D_{b3} and D_{b4} Therefore, its main purpose is to reduce gate driver loss of MOSFETs M_{18} and M_{19}. The location of resonant drivers is mainly dictated by loss distribution according to Fig. 29. However, placing the proposed driver to the other parts of circuit didn't show any sufficient improvements.

It is worthy of note, that operation of additional diodes provides clamping of V_{GS}. Diodes D_{b1} and D_{b2} clamps V_{GS} at V_B and $V_{B/2}$, respectively. Clamping at V_B avoids over-drive voltage variation, whereas clamping at VB/2 ensures that excessive negative voltage doesn't occur. The same assumptions hold for D_{b3} and D_{b4}, except that voltage V_{GS} clamps to $V_{B/2}$ and V_{GG}, respectively. Another important function of diodes is to provide an electrical path for energy recovery.

5.2 Simulation results

The gate pulses for main switches are represented in Figure 32. Results show a better obtained delay between transition states. A shape of p-mos pulse is slightly distorted. This, however, doesn't diminish the efficiency of voltage conversion.

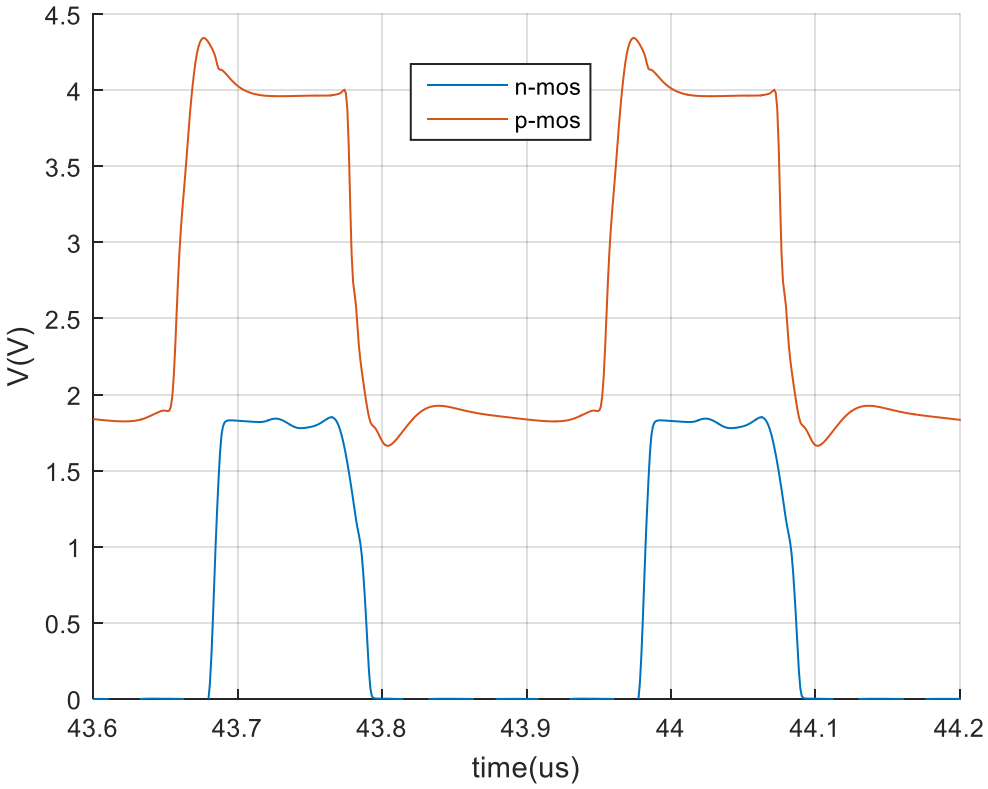

Figure 32. *Gate pulses for p-mos and n-mos switches.*

The gate pulse for p-mos switch M_1 with respect to inductor current I_{LR} is depicted in Fig.33. There is one important observation from the current behavior: the freewheeling time (when I_{LR} has already achieved its peak value and V_{GS} voltage is clamped) is negligibly short, thus, energy recover process starts immediately. This prevents operation of the driver from additional losses that occur due to forward voltage drop in diodes.

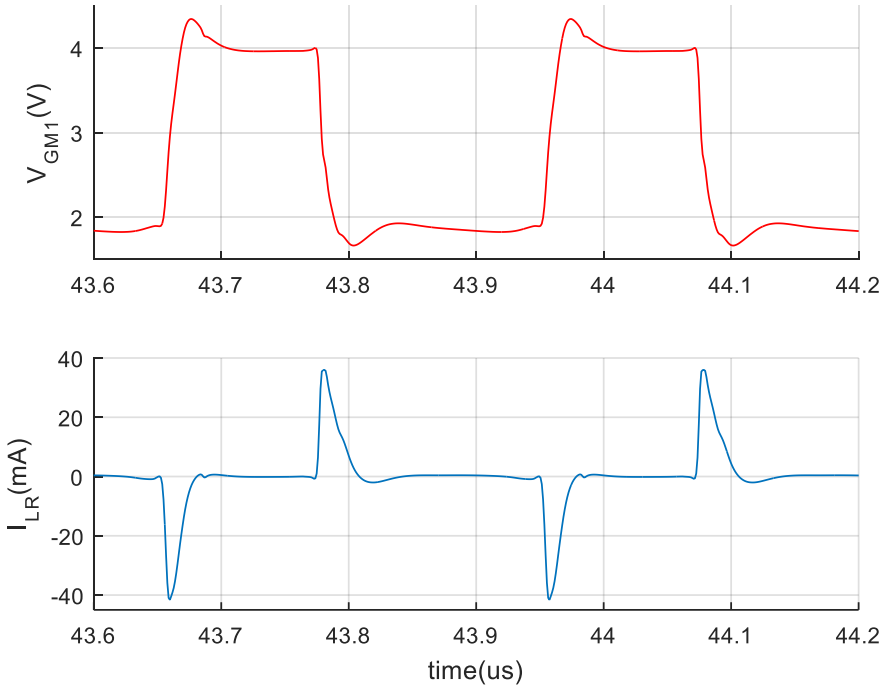

Figure 33. *The gate pulse for p-mos with respect to resonant inductor current.*

The output voltage waveform is shown in Fig. 34. The average Vout is 2.30V

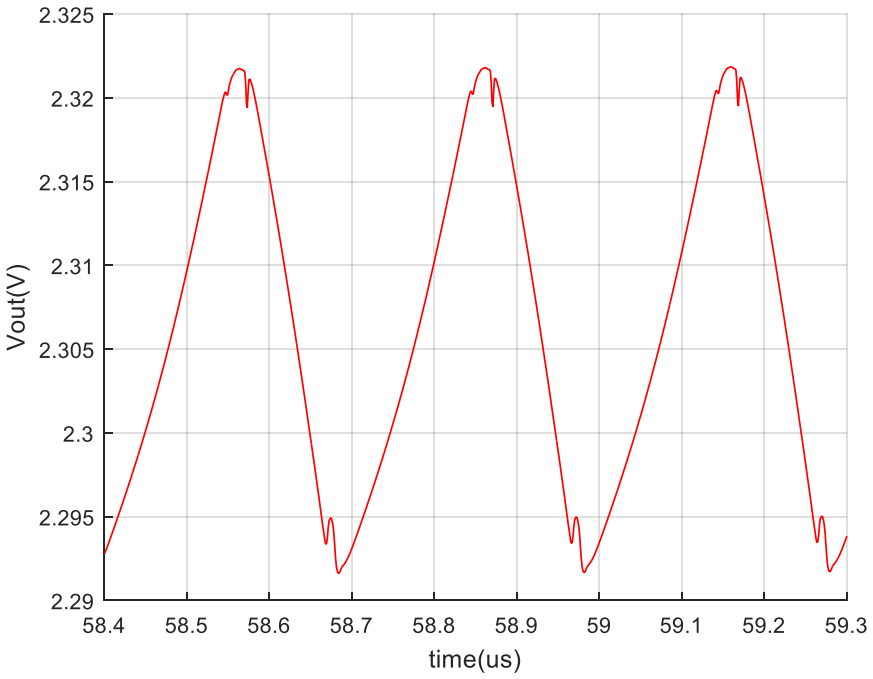

Figure 34. *Output voltage waveform.*

The list of the components for resonant gate drivers is presented in Table 10.

Table 10. *Resonant driver components.*

Components	Key parameters	Manufacturer part number
L_{R1}	R_{DC}=3mΩ, 330nH	DO1813H-331
L_{R2}	R_{DC}=1mΩ, 470nH	744373770047
D_{b1}, D_{b2}, D_{b3}, D_{b4}	V_{BR}=75V, I_F=0.2A	1N914

The simulation results are gathered in Table 11.

Table 11. *Simulation results.*

V_{in} (V)	V_{out} (V)	η (%)	f_s (MHz)
4	2.30	72.4	3.35

The results show that conversion efficiency is improved by approximately 2% and equal to 72.4%. At the same tame the operation frequency diminished insignificantly to 3.35MHz.

5.3 Evaluation of voltage stress across the transistors

During the time frame when power switch is open, in a correctly-designed power stage the diode starts conducting and the drain-source voltage rises due to parasitic ringing. The reason for that phenomena is a leakage inductance. After the period of parasitic ringing has ended, the drain source-voltage fixes at a certain value until switch is closed again. This drain-source voltage is of particular concern as if it violates the maximum voltage defined by manufacturer, the transistor breakdown can occur. Simulated waveforms of drain-source voltages (Fig.35-Fig.37) are represented further in order to ensure that they settled below the limit during operation of the converter.

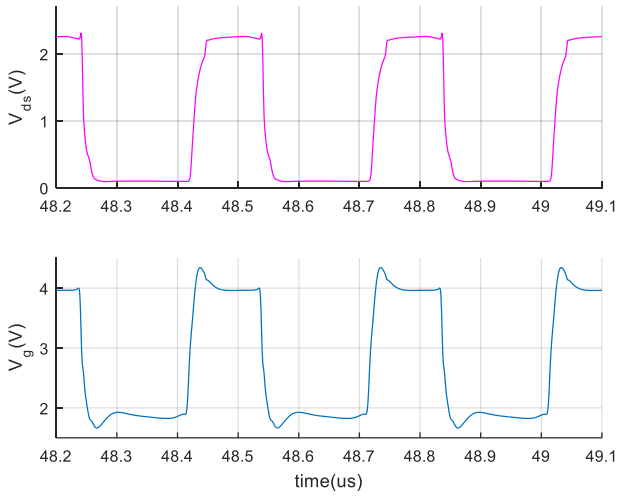

Figure 35. *Drain-source voltage over M1 (pink trace) and gate pulses (blue trace).*

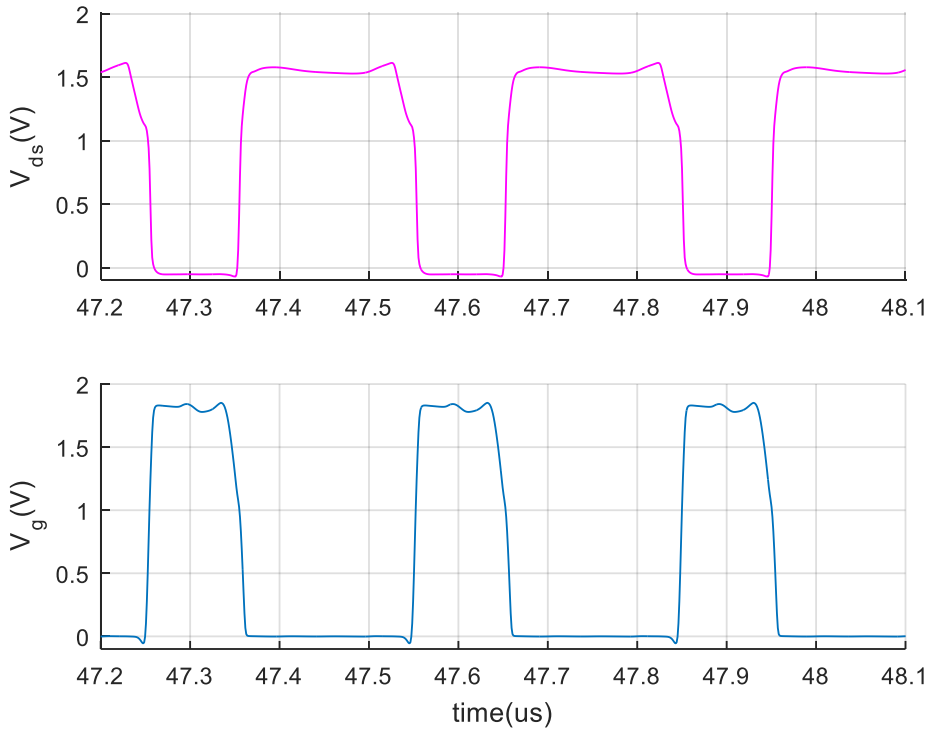

Figure 36. *Drain-source voltage over M4 (pink trace) and gate pulses (blue trace).*

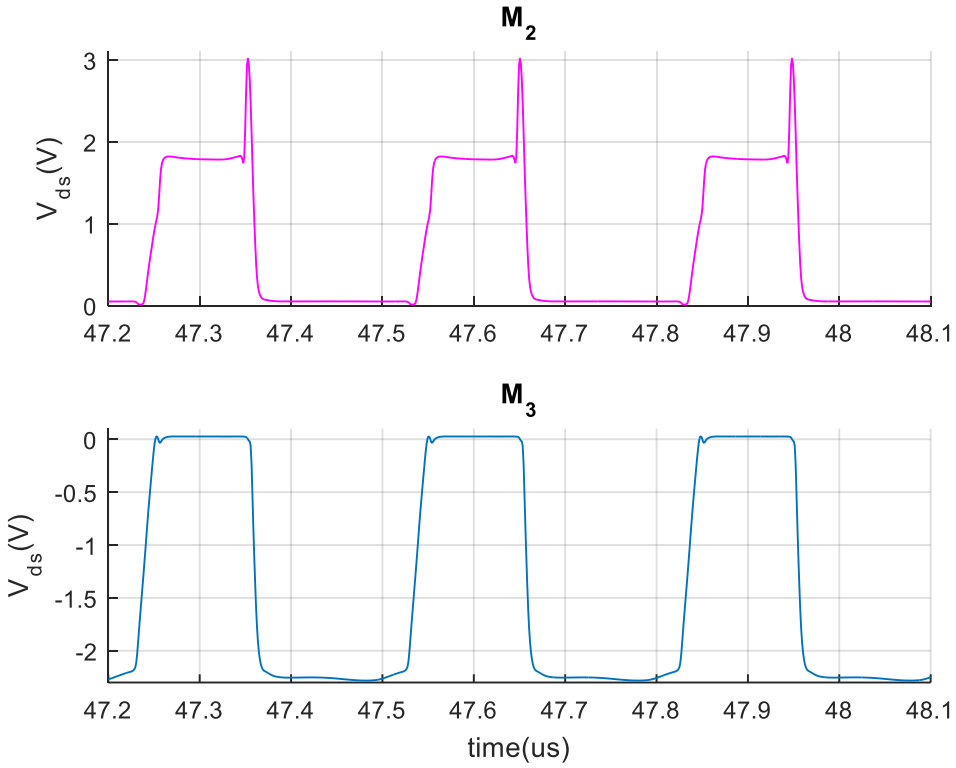

Figure 37. *Drain-source voltage over M2 (pink trace) and M3 (blue trace).*

The numerical results are collected in Table 12.

Table 12. *Results of voltage stress evaluation.*

MOSFET	Vds-peak (V)	Vds-data sheet (V)
M_1	-2.3	-8
M_2	-2.99	-8
M_3	2.27	20
M_4	1.61	20

According to table 12 the simulated behavior of power transistors' drain-source voltages allows to conclude that no breakdown can occur at certain input voltage 4 V. All in all, this converter topology demonstrates a significant advantage when compared to conventional buck converter, or, for instance, to flyback or forward converters, where voltage stress across main switches during demagnetizing time frame can be as high as double of input voltage.

6. CONCLUSION

The main purpose of this Thesis is designing High speed DC-DC converter with self-oscillating control for discrete implementation on PCB. The target input voltage of power supply unit is 3.6V. Presented topology is based on Asymmetric VHF self-oscillating DC-DC converter with integrated transformer, which was designed for IC fabrication with 45 nm CMOS technology [1].

The important parts of the power stage comprise duty cycle detector and pulse shaping circuit. The MOSFETs were sized carefully employing matching method. The high frequency performance of the selected transistors was ensured by utilizing specific simulation test bench. The same procedure was carried out for main switching transistors and cascaded structure.

Another vital part of the circuit is a transformer. The primary winding of the transformer is used as a load filter coil, and the secondary provides a feedback signal. The selection of the transformer was discussed in details in terms of measuring quality factor Q_L.

Furthermore, the filtering output stage was modeled to improve quality of the output voltage. This included evaluation of capacitors high frequency impedance characteristics.

The proposed circuit was simulated as a complete structure, which includes parasitic effects of PCB, namely parasitic inductance and resistance of traces. The equivalent series resistance and parasitic inductance of the static model of battery were also taken into account in the simulation environment.

Moreover, the converter topology was optimized in order to improve efficiency and avoid a large impact of switching noise effect. All in all, two MOSFETs were connected in parallel with cascaded structure to minimize conduction losses; additional inductor was employed at the output stage to improve waveform of the output voltage; single filtering load capacitor was replaced by parallel structure of three capacitors to reduce total impedance. In addition, a few decoupling capacitors were added to the simulation circuit in order to mitigate the impact of switching noise effect.

The circuit provided 2.34 V of output voltage at 4 V battery supply. The calculated efficiency is 70.35% with some 781.22 mW of input power. The registered switching frequency is 3.4 MHz. In general, this type of converter was designed to operate at

variable voltage supply in the range from 3 V to 5 V, which makes it applicable to comply with behavior of practical battery set.

The circuit with applied resonant gate driving provided 2.30V of output voltage at 4 V supply. The efficiency was improved by 2% and was equal to 72.4%. The switching frequency was 3.35 MHz.

Altogether this Thesis shows feasibility of practical implementation of the high speed DC-DC converter with self-oscillating control on PCB. The obtained results can be served as ready manual in preparing PCB layout of the converter and its further assembling.

A further research is needed to improve efficiency of the proposed converter and increase switching frequency. This mainly implies the design of transformer for high frequency application and employing several additional techniques for driving transistors, for instance, different topologies of resonant gate drivers and dead time latch.

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