Nano-Subsidence Assisted Precise Integration of Patterned Two-Dimensional Materials for High-Performance Photodetector Arrays

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ABSTRACT

The spatially precise integration of arrays of micro-patterned two-dimensional (2D) crystals onto three-dimensionally structured Si/SiO_2 substrates represents an attractive, low-cost system-on-chip strategy towards realization of extended functions in silicon microelectronics. However, the reliable integration of such atomically thin arrays on planar patterned surfaces has proved challenging due to their poor adhesion to underlying substrates, as ruled by weak van der Waals interactions. Here we report on an integration method utilizing the flexibility of the atomically thin crystals and their physical subsidence in liquids, which enables reliable fabrication of the micro-patterned 2D materials/Si arrays. Our photodiode devices display peak sensitivity as high as 0.35 A/W and external quantum efficiency (EQE) of ~90%. The nano-subsidence technique represents a viable path to on-chip integration of 2D crystals onto silicon for advanced microelectronics.

KEYWORDS

Two-dimensional materials, graphene, optoelectronics, on-chip integration, photodiodes, heterojunctions, four-quadrant arrays.

With Moore's law reaching its limit,[1] the semiconductor industry is urgently searching for innovative strategies to go beyond standard microelectronics. One of the most intriguing strategies in modern electronics, referred to as system-on-chip (SoC) for more-than-Moore electronics,[2-4] aims to integrate various active modules in individual chips wherein different functional materials are combined with standard silicon technology. This hybrid approach enables the introduction of extended functionalities such as data storage, sensing, communication and self-powering to conventional logic modules, therefore expanding the current capabilities of logic microelectronics. In this context, two-dimensional (2D) atomic crystals,[5-9] which include a vast library of materials with each one featuring distinctive physical and electronic properties, have emerged as outstanding candidates for integration into silicon to create hybrid devices with different capabilities.[10]

For the purpose of SoC application, different materials are required to be hetero-integrated onto silicon through direct contact or interconnection.[4] Previous reports revealed that 2D crystals could be directly transferred onto three-dimensionally structured silicon for energy harvesting,[11-13] photonics,[14-17] and electronics,[18] providing evidence for their potential as on-chip functional modules. In particular, graphene/Si heterojunctions have been employed as photodetectors, working either as photoconductors, with responsivity up to 10^5 A/W but unfavorably high dark current,[19] or as photodiodes, with above 65% peak external quantum efficiency (EQE).[20] However, in such experiments the cumbersome fabrication process following the 2D crystal transfer needs to be minimized, since the atomically thin 2D crystals are prone to shear from or even to come off the substrates during microfabrication processing, such as photoresist deposition and pattern development. These fabrication issues severely hamper the applicability of patterning large 2D sheets into micrometric functional arrays as active SoC components. For these reasons, to date such hybrid devices are mostly restricted to large 2D sheets forming individual active units; the precise and stable integration of arrays of micro-patterned 2D crystals for advanced electronics has been rare.

Here, we devised a nano-subsidence integration method which enables spatially precise and high-yield integration of arrays of micro-patterned 2D crystals onto three-dimensional substrates, *e.g.* patterned Si/SiO_2 surfaces. Such method enables the fabrication of high performance arrays of photodetectors. As a proof of concept, 2 × 2 type four-quadrant 2D crystal/Si diodes used as photodetectors are demonstrated. By engineering the work function of graphene and the optical antireflection, our

photodetectors exhibit high peak sensitivity up to 0.35 A/W (EQE of ~90%) at 480 nm, as well as high spatial uniformity. Depending on the optical wavelength range, the overall system performances are comparable to or higher than those of commercial silicon diode-based photodetectors.

RESULTS AND DISCUSSION

The conventional method for integrating 2D crystals into silicon-based technology consists in their direct transfer onto three-dimensionally predefined Si/SiO_2 substrates,[11-21] as portrayed in Fig. 1a. In this approach, the SiO_2 capping above silicon is used as both sacrificial and insulating layer. Selected SiO_2 sacrificial areas are pre-etched to form a cavity for conformal contact between the 2D crystals and underlying silicon, where the exposed silicon serves as active functional region and the remaining SiO_2 around the cavity works as insulating layer for external wiring, resulting in stepwise substrate surfaces.[22] When 2D crystals are transferred over patterned surfaces, they have to physically adapt to the pattern in relief. Since the large sheets of 2D crystals cannot uniformly land on the top part(s) of the relief(s) and on the surface during the mechanical transfer process, which usually results in the emergence of physical corrugations and bubbles[23,24] and, consequently, the poor adhesion between 2D crystals and substrates. Moreover, when transferring the 2D crystals entirely over the patterned silicon cavities, they tend to trap soluble impurities and to contaminate the junction interface after heat dry. The overall weak substrate adhesion could cause 2D crystals to slide or even to be removed in the subsequent lithography processing necessary for patterning the 2D crystals or defining the microelectrodes. As a result, it is extremely challenging to obtain clean 2D crystal/Si interfaces.

To address the above-mentioned challenges, we have conceived the nano-subsidence integration method that allows a high-yield hetero-integration (Fig. 1b). The method relies on the metallization before the 2D crystal patterning and SiO_2 etching, in order to use the solid electrodes as anchoring bars to prevent the 2D crystals from sliding during the following processing. The alignment among 2D crystals, electrodes, and step edges can then be accurately defined through photolithography, ensuring high spatial precision during the hetero-integration. Besides, the target substrates of transferred 2D crystals are preserved flat, which helps to expel the liquid transfer media smoothly. The third consideration is to etch the SiO_2 sacrificing areas in the last fabrication step and the arrays of micro-patterned 2D

crystals can gently subside, taking advantage of the flexibility of the ultrathin 2D crystals, and adapt to the stepwise substrates with negligible strain and improved adhesion (Supplementary Fig. S3). An additional bonus to form the heterojunctions in the last step also includes the minimized time of air exposure of bare silicon and the preserved fresh silicon surface. Hence, such protocol offers great flexibility in further interface engineering between silicon and 2D crystals.

Figure 1c sketches the individual processing steps of the integration technique while showing corresponding optical microscopy images. First, the large-area CVD graphene is transferred onto a flat SiO_2/Si substrate. Graphene adheres well to the substrate thanks to the large contact area and the superior flatness of the pristine SiO_2 surface. Metal electrodes with a given pattern are then deposited onto graphene through a standard photolithographic process followed by thermal evaporation of the metal and a lift-off step. Afterwards, graphene is patterned through photolithography and oxygen plasma etching. Finally, the SiO_2 layer in the device active region is wet etched *via* a photoresist mask, so that the graphene layers gently fall down and make contact to the exposed silicon. After thoroughly rinsing in deionized water, the samples are dried out in vacuum to expel the encapsulated water between graphene and silicon. By means of the capillary action formed during the vacuum evaporation of the encapsulated water, the graphene is in conformal contact with silicon. We found that the crystal/Si adhesion is readily wetting-enhanced and is much superior to that formed in the simple dry transfer.

As a proof of concept, we apply this method to demonstrate a four-quadrant graphene/Si photodiode detector, a typical beam position sensing module widely used as collimators and many other adjustment sensors in fiber communication and space guidance.[25-27] The yield of the subsidence integration of graphene to silicon was considerably high: 34 out of 36 quadrants were attained without obvious rupture or folding of graphene, thereby attesting a yield as high as 94 % (supplementary Fig. S2). We note that our approach is extremely versatile and the prototypical 2×2 array fabricated here (Fig. 1c) can be easily upgraded into more complicated arrays/devices.

Alongside the use of the subsidence integration method, we have paid particular attention towards the engineering energy levels of graphene which is known to be essential for attaining high photosensing performance.[11,13] Figure 2a depicts the energy level alignment and working principle of the graphene/Si photodiodes. The electron-hole pairs are first generated by light irradiation on silicon; then holes drift into graphene assisted by the built-in electric field at the graphene/Si interface. Hence,

the built-in electric field is the driving force for carrier separation and a high built-in electric field would be favorable for this process. In addition, a large interfacial barrier helps to block the drift of electrons to graphene, reducing the carrier recombination in graphene.

A high-quality CVD graphene[28] with an intrinsic carrier mobility of 2800 $cm^2V^{-1}s^{-1}$ (supplementary Fig. S5d) was used in this work. To increase the interfacial barrier, we implement p-type doping of graphene *via* spin-coating a thin layer of bis(trifluoromethanesulfonyl)amide (TFSA, $[CF_3SO_2]_2NH$, inset of Fig. 2b), a strong electron-withdrawing molecule.[13,29] In contrast to the weak doping effect by ambient oxygen and water molecules[30] with a shift of charge neutrality point of 17 V (supplementary Fig. S5a), the TFSA doping determines a larger shift of ~270 V (supplementary Fig. S6c). Such a large shift corresponds to a rather high surface doping concentration of 6.5×10^{13} cm^{-2} and a work function increase of 0.75 eV in graphene, as estimated through the equation $\varepsilon_F = \hbar \cdot v_F \cdot \sqrt{\pi n}$, where ε_F, v_F, n, and $\hbar$ denote Fermi energy, Fermi velocity, carrier concentration, and reduced Planck constant, respectively. The strong doping caused an effective interfacial barrier of 0.79 eV (supplementary Fig. S10d). Accordingly, improved photovoltaic behavior was achieved, as confirmed in Fig. 2b by the current-voltage (*I-V*) characteristics of the pristine and doped devices. TFSA-doped devices exhibited highly enhanced open-circuit voltage (V_{OC}), short-circuit current (I_{SC}), and fill factor (FF), indicating the critical role of the interfacial barrier on the photovoltaic performance. In Fig. 2c, we analyzed the *I-V* behavior of the doped device under dark condition, which reveals a good ideality factor of 2.02±0.01 and a high rectification ratio of 10^5 in the bias range of ±1 V, suggesting an excellent photodiode junction quality. The excellent junction quality is also corroborated by the photovoltaic tests. Before antireflection coating, the doped device shows high photovoltaic efficiencies of 10.1% and 9.1% under 520 nm/43.5 $mW\cdot cm^{-2}$ and AM1.5 conditions, respectively (supplementary Fig. S12 a and c), consistent with the literature results.[11-13] The series resistance (R_s) value was estimated to be 0.26 Ω/cm^2 for the 100×100 μm^2 device, which shows a reduction of at least 57% when compared with previously reported values (from 0.61 to 1.38 Ω/cm^2) obtained on devices fabricated by direct transfer.[11]

We have also measured the response speed of the photodiode under a monochromatic light source. Figure 2d shows a diagram of the piezoelectrically controlled monochromator used in our experiments. The angle of the incoming light from the Xenon lamp is fixed while the angle of reflection beam and the resulting

wavelength of the outcoming beam through the slit would change upon piezoelectrical rotation of the optical grating. Since the light power varies with wavelength (the characteristic spectrum of the system is given in supplementary Fig. S13), a modulated photoelectric response would be observed with changing the optical wavelength. Figure 2e displays the modulated photocurrent modes when the incident light wavelength changes from 500 nm to 300, 350, 400 and 450 nm, respectively. At shorter time scales (Fig. 2f) both the rise and decay time are within 500 μs, which represents the fastest signal that can be detected through our experimental setup limited by the millisecond-scale piezoelectric response rate of the grating driver. Hence, the response speed of our devices, of at least 500 μs, certainly represents an underestimate. Generally, the response time would be longer if the density of interfacial states and charge trapping centers were sizeable. The fast response featured by the devices made with our nano-subsidence method suggests that the graphene/Si interface of the photodiodes is of high quality.

In order to further optimize the performances of our photodiodes, we have employed a surface antireflection capping. This is commonly employed to increase the optical absorption of photodiodes by depositing single or multiple optically transparent antireflection dielectrics.[11,31-35] According to the principle of optical destructive coherence, the reflection rate for a certain light will be minimized when a single antireflective capping layer satisfies the double conditions that $n_{AR} = \sqrt{n_{air} n_{si}}$ and $d_{AR} = \lambda/4n_{AR}$,[32] where n_{AR}, n_{air}, and n_{si} are the refractive indices of the antireflective capping layer, air and silicon, respectively, and d_{AR} and λ are the thickness of the capping layer and the incident light wavelength. Given the atomic thickness of the 2D layers and the low formation energies of lattice defects that make them prone to damages generated by external high-energy atoms,[36-38] capping layers grown *via* aggressive deposition methods (*e.g.* sputtering) should be avoided. Towards this end, we have used thermally evaporated MoO_3 as the capping layer,[34,35] and the damage to 2D layers are expected to be minimized. The values of n_{MoO3} are close to those of $\sqrt{n_{air} n_{si}}$ in most range of visible light (supplementary Fig. S8), suggesting that it is a suitable antireflection material. By theoretical calculations, we also confirmed that the effect of graphene on optical absorption is negligible due to its atomic thickness (supplementary Fig. S9).

Figure 3a sketches the device cross section of pristine *versus* capped devices and their related optical images. Micro-area reflection measurement revealed that the

reflectivity is largely reduced from 36% to 8% at λ = 520 nm upon the use of a capping layer of 55-nm MoO_3. The reduction of the optical reflection is also corroborated by the difference in brightness of the optical images of the pristine and capped Si/graphene stacks, where a lower brightness is observed in the latter (around orange dot in the lower panels of Fig. 3a). As a result, the photoresponse of the devices is enhanced. Under 43.5 mW/cm^2 illumination at 520 nm, the photocurrent increases from 11.6 to 16.7 mA/cm^2 (Fig. 3b). The effect of the MoO_3 antireflective capping is further analyzed by correlating micro-area reflection spectra to the EQE of our devices. Here EQE is estimated by $\mathrm{EQE} = \frac{J_{ph}\hbar C}{eP\lambda}$ where J_{ph} is the photocurrent density, C is the speed of light within vacuum, e is the elementary charge, P is the light power. The EQE data was extracted from the photocurrent spectrum recorded between 320 to 690 nm. The open blue and red circles in Fig. 3c compare the EQE before and after deposition of a 55-nm-MoO_3 capping layer. As expected, the capping enhances (or reduces) the EQE around λ = 480 (or λ = 320 nm), in agreement with the interference conditions at the corresponding wavelengths (supplementary Fig. S9c). In Fig. 3c, we also compare the EQE with device absorption rate (1-R, with R the reflectivity) as measured by micro-area reflection. The EQE lines follow closely with the absorption rates, suggesting a near-unity internal quantum efficiency (IQE) since IQE=EQE/(1-R). In the experiments, the peak IQE reaches 90% at 480 nm, approaching the ideal unitary IQE of the photodiodes.[32] The ~10% reduction to the ideal values (supplementary Fig. S9, c and d) stems likely from local variations of refractive index in the MoO_3 capping layer caused by the presence of pinholes or oxygen loss. The extremely high IEQ achieved here corroborates again the high integration quality of the arrays *via* our nano-subsidence method.

The photocurrent properties of the capped devices were extensively characterized by varying the optical wavelength and power. Figure 3d plots the photoelectric sensitivity *versus* the two parameters of light wavelength and power. Despite of strong dependence on light wavelength, the sensitivity is basically power independent within the measurement range of optical power (from 10% to 100%) since the devices show negligible saturation in photoresponse below 100% power (Fig. 3e). To evaluate the potential of the nano-subsided photodiodes as a system-on-chip module, we also compare the EQE of our devices in Fig. 3f and Table 1 with currently commercial photodiodes based on silicon pn junctions (ThorLabs FDS010 and FDS10×10, Hamamatsu S1336BQ). Notably, our devices are superior to their commercial

counterparts in the visible region from 400 to 700 nm, therefore representing a prototypical high-performance system-on-chip module for the beyond-silicon circuitry.

Table 1 Comparison of EQE performance of nano-subsidence fabricated graphene/Si photodiode with typical commercial silicon photodiodes at different wavelength values. The values in parentheses show the EQE difference of the commercial devices as compared to our graphene/Si device.

Photodiode	EQE @ 350 nm	EQE @ 450 nm	EQE @ 500 nm	EQE @ 550 nm	EQE @ 650 nm
This work	27.2%	84.2%	90.3%	89.0%	86.2%
ThorLabs FDS10×10 (UV enhanced)	58.9% (+117%)	68.6% (-19%)	73.6% (-18%)	76.5% (-14%)	79.0% (-18%)
Hamamatsu S1336BQ (UV enhanced)	56.1% (+106%)	60.8% (-28%)	63.7% (-29%)	65.7% (-26%)	67.5% (-22%)
ThorLabs FDS010	19.0% (-30%)	40.8% (-52%)	54.2% (-40%)	64.5% (-28%)	76.8% (-11%)

The overall superior optoelectronic performance can be understood as follows. First, defects and surface states, though they determine the surface recombination velocity, are not the most important factors responsible for the carrier separation process during light harvest, since many defective photovoltaic materials can also afford excellent optoelectronic performance, such as polycrystalline silicon and porous perovskites. Instead, the matching of different energy levels between different electronic functional layers seems more crucial for attaining high performance, by forming appropriate built-in electric field for carrier separation and Ohmic electrode contacts for carrier extraction. As have been shown in Fig. 2b, the graphene/Si systems are extremely sensitive to the alignment of energy levels and the shape of the *I-V* curve is greatly improved after applying the dopant TFSA on graphene. Second, it has been reported that surface passivation can take place when immersing the Si substrates into HF-contained solution due to the saturation of dangling Si bonds at the surface.[39] Thus, the unintentional Si surface passivation in the BOE etching step may

also contribute to the high performance. Third, the high carrier mobility of the graphene electrodes helps to collect the separated carriers effectively, which is also likely one of the origins for the high performance.

To assess the photoresponse uniformity of individual array units, we mounted our samples onto a test printed circuit board (PCB) (Fig. 4a). In order to have a reliable (wire) bonding to device electrodes, no MoO_3 capping layer is deposited in this test. Figures 4b and 4c show enlarged images on local arrays at different magnification ratios where multiple quadrant photodiodes were prepared. During testing, each unit was exposed to a 532-nm focused laser beam with a power of about 10 W/cm^2. Figures 4d-4f show the corresponding photoelectric curves. Almost identical *I-V* curves were recorded for the four units, with I_{SC} =0.56±0.08 μA. A slight degradation of the fill factor was observed in all the four *I-V* curves, which is likely due to the effect of ambient moisture on the hygroscopic dopant TFSA during the measurements.

Finally, we have verified the generalization of the nano-subsidence assisted integration method by replacing graphene with another renowned 2D crystal, *i.e.* molybdenum disulfide (MoS_2). Figure 5a shows the optical images of a MoS_2/Si junction before and after SiO_2 etching. A mechanically exfoliated 5-layer-thick MoS_2 was used in this device. Since MoS_2 is normally slightly n-doped, the MoS_2/Si stack can be regarded as an n/n^{++} homo-junction with relatively small barrier heights. [32] Figure 5b shows a corresponding band diagram, where Φ_C and Φ_V are the barriers for blocking the reverse motions of electrons and holes at the conduction and valence bands, respectively. Owing to smaller Φ_C and Φ_V as compared to the case of doped graphene/Si (Fig. 2a), a large number of carriers can drift and recombine, resulting in lower V_{OC} and J_{SC} (Fig. 5c) and a reduced fill factor (Fig. 5d). However, in spite of the degraded photoelectric properties with respect to graphene/Si junctions, the MoS_2/Si junction still exhibited a photoelectric behavior similar to that of small-barrier diodes in which backward current is enhanced and reasonably high other photoelectric parameters. In particular, a large rectification ratio of 10^5 within ±1 V (Fig. 5c), notable photoelectric behavior (Figs. 5c and 5d), reasonably high peak EQE of ~25% (Fig. 5g), and fast photoresponse of 1 ms (Fig. 5h) are measured.

CONCLUSIONS

We have developed a method enabling the hetro-integration of arrays of atomically thin 2D crystals on planar patterned silicon substrates for system-on-chip electronics. Noteworthy, this integration method combines several advantages. First, the substrate

was kept flat in all photolithography steps, which facilitates the subsequent microfabrication processing. Second, high-yield integration of 2D crystals into the stepwise substrate was realized *via* controlled gentle subsidence assisted by capillary forces during vacuum dry, which helps to minimize strain accumulated in the flexible 2D crystals. Third, the exposure of bare silicon surface to air is minimized, resulting in a high quality of electronic interface which, as a result, improves the junction performances. Taking graphene and MoS_2 as model systems, we demonstrated the general applicability of such subsidence method to integrate flexible 2D crystals onto silicon as photodiodes. The photodetector performances surpass those of commercial photodiodes after appropriate device optimization. Not limited to the photoelectric function and materials demonstrated above, the concept of subsidence integration *via* an underlying sacrificial layer could also be extended to wider applications, such as 3D interconnection, optical waveguides, and microfluidic channels, and hence it holds great potential for realizing more versatile modules for the more-than-Moore microelectronics.

METHODS

Transfer of CVD graphene on flat SiO_2/Si substrates. Large-area high-quality monolayer graphene was grown on 25 μm thick copper foils by CVD.[28] A 20 mg/mL PMMA/chlorobenzene solution was spin-coated on the graphene/copper foils at 3000 rpm for 30 s, which was then heated dry on a hot plate at 180 °C for 1 minute. A PDMS scaffold with a hole of ~10 mm in diameter was gently pressed down onto the PMMA/graphene/copper stacks, with the PDMS scaffold attaching to the stacks. Afterward, the whole stack was placed floating on an ammonium persulfate (0.1 M) solution with the copper face downwards to etch the copper foil. After removing the copper foils, the PDMS/PMMA/graphene stack was rinsed in distilled water for several times and was finally scooped out by a flat SiO_2/Si substrate. The silicon wafers (from IPMS Fraunhofer Institute, Dresden) were capped with a 90-nm-thick thermally grown SiO_2 dielectric layer and were n-doped to a high level of $\sim 3 \times 10^{17}$ cm^{-3}.

Device fabrication.

Optical lithography was performed through a direct laser writing system (LW405B, Microtech Inc.). A thin positive photoresist AZ1505 was used as a mask for graphene patterning and metallization. The exposure resolution is about 1 μm. AZ 726 metal-

ion free developer and dimethyl sulfoxide were used for resist development and lift-off, respectively. To increase the adhesion ability of resist and development, the surface of silicon wafers was modified by thermally evaporated hexamethyldisilazane molecules before applying the resist. The SiO_2 dielectric layers were etched by standard buffered HF etchant (NH_4F : HF = 6 : 1). The electrodes were realized by thermal evaporation of 1 nm of chromium and 50 nm of gold. The use of chromium adhesion layer is necessary in order to prevent the unwanted lateral etching the SiO_2 underneath electrodes (See also supplementary Fig. S1). The nano-subsidence technique may fail under the following two circumstances. 1) Excessive shaking of the sample during etching or rinsing which may lead to the folding or rupture of 2D crystals; 2) Incomplete SiO_2 surface priming and low adhesion of mask resist to substrates which can result in unwanted SiO_2 etching under mask resist. In case of passivation or modification of silicon interface, liquid immersion techniques are applicable for this nano-subsidence integration,[39,40] while the conventional thermal or gaseous treatments would fail.

Characterization and measurements.

All optical images of graphene and devices were taken with an Olympus BX53M microscope. The monochromatic photoelectric characterization was performed with a monochromatic source (model Polychrome V, Till Photonic Inc.) and a Cascade EPS150TRIAX Probe Station inside a nitrogen-filled glovebox. The optical spectrum and its power were calibrated by a PM100A Power Meter (Thorlab) and the related data is shown in supplementary Fig. S13. For the characterization of the integration uniformity of the four-quadrant photodetectors, the device was mounted on a home-made PCB chip carrier which was placed under a focused 532-nm laser beam (~10 W/cm^2) from a Renishaw Raman spectroscopy in ambient. A dual-channel sourcemeter Keithley 2636A was used for the electrical characterization.

Author contributions

S.L.L., E.O. and P.S. conceived the experiment and designed the study. S.L.L. performed the experiments and developed the fabrication method. W.N, Y.H., W.G., B.W, and Y.L. synthesized and provided the CVD graphene sample. S.L.L., E.O. and P.S. co-wrote the paper. All authors discussed the results and contributed to the interpretation of data, as well as contributing to editing the manuscript.

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Supporting Information Available: Experimental details on etching rates of SiO_2 capped by different materials, nano-subsidence integration, intrinsic mobility and contact resistivity of pristine CVD graphene, effect of TFSA doping on CVD graphene, effect of HNO_3 doping on mechanically exfoliated graphene, refractive indices of candidate antireflection capping layers, design of MoO_3 antireflection layer, effect of barrier height (Φ_B) on V_{oc}, fit of series resistance in the circuit loop of photodiodes, performance as photovoltaic devices, output power and linearity of monochromatic light source. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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Figure Caption

Figure 1 Schematic diagrams of hybrid integration by conventional direct transfer and our nano-subsidence techniques. a, Cross-sectional diagram for the conventional direct transfer integration, which features several risks of tearing out and sliding off when the sizes of 2D crystals are small, due to the weak stickability of 2D crystals and the presence of stepwise substrate structure. **b**, The concept of the improved hybrid integration by nano-subsidence in which the 2D crystals are fixed by using the metallic electrodes as anchoring bars and selectively etching out the sacrificial SiO_2 layer in the last. The hybrid integration is completed after the gentle subsidence of 2D crystals. **c**, The processing flow and corresponding images for each critical integration step for the subsidence integration. Its processing sequence is renewed to transfer-metallization-patterning-etching to ensure the precise location of 2D crystals.

Figure 2 Photoelectric properties of hybrid graphene/silicon diodes prepared by the nano-subsidence integration. a, Diagram of the energy level alignment and operation principle of the graphene/silicon photodiodes. **b**, Comparative photoelectric behavior of the photodiodes before and after engineering band alignment *via* TFSA doping. Inset: The molecular structure of TFSA and the change of Fermi level of graphene before and after TFSA doping. **c**, Fitting of *I-V* curve under dark condition to extract the ideality factor of the diodes. Inset: Semi-logarithmic plot of the I-*V* curves under both dark and light conditions. High rectification and zero-bias signal-noise ratios of 10^5 and 10^7 are observed. **d**, Principle of wavelength scan for characterizing photoresponse time, where the piezoelectric response time is below the order of ms that defines the lower limit of our samples. **e**, Modulation of photocurrent by varying the excitation wavelength. **f**, Enlarged figure to analyze the rise and decay times of our photodiodes which are estimated to be better than 500 μs.

Figure 3 Photoelectric properties of graphene/silicon diodes after capping antireflective MoO_3. a, Cross-sectional diagrams and optical images of the pristine and MoO_3 capped devices. **b**, Comparative *I-V* behavior of the photodiodes before (blue) and after (red) capping 55 nm MoO_3 antireflective layers. The photocurrent increases from 12 to 17 mA/cm^2. **c**, Comparison of absorption rate (1-R, lines) and external quantum efficiency (EQE, open dots) before (blue) and after (red) MoO_3

capping. **d**, Contour plot of photoelectric sensitivity *versus* wavelength and light power. **e**, Sensitivity as a function of light power at different wavelength values from 350 to 650 nm. The devices show negligible saturation in photoresponse within experimental power range of ~50 mW/cm^2. **f**, Comparison of EQE with three typical commercial silicon photodiodes. Our devices (red dots) rivals the counterparts in the visible regime from 400 to 700 nm after the MoO_3 antireflective capping.

Figure 4 Test of the uniformity of array units. a, Optical image of a testing module with samples mounted onto a home-made printed circuit board. **b**, Enlarged image for a local area with three quadrant arrays. **c**, Further enlarged image for an individual 2×2 quadrant array. **d-g**, One-by-one test of the photoelectric behavior for the four array units (*i.e.*, from quadrant 1 to 4). Inset images show the illumination locations of the focused excitation laser.

Figure 5 Test of the feasibility of the subsidence integration technique to other 2D crystals. a, Optical images for a typical MoS_2/silicon diode before and after SiO_2 etching. **b**, Diagram of the energy level alignment of the MoS_2/silicon diode, which is actually an n/n^{++} heterojunction with small barrier heights (Φ_C and Φ_V). **c**, Semi-logarithmic plot of the *I-V* curves under both dark (black dots) and light (red circles) conditions. **d**, Corresponding linear plot of the *I-V* curve. **e**, Contour plot of photoelectric sensitivity *versus* wavelength and light power. **f**, Sensitivity as a function of light power at different wavelength values from 350 to 650 nm. The devices also show negligible saturation in photoresponse within experimental power range. **g**, Estimated EQE for different wavelengths from 320 to 700 nm. **h**, Modulation of photocurrent by varying the excitation wavelength.

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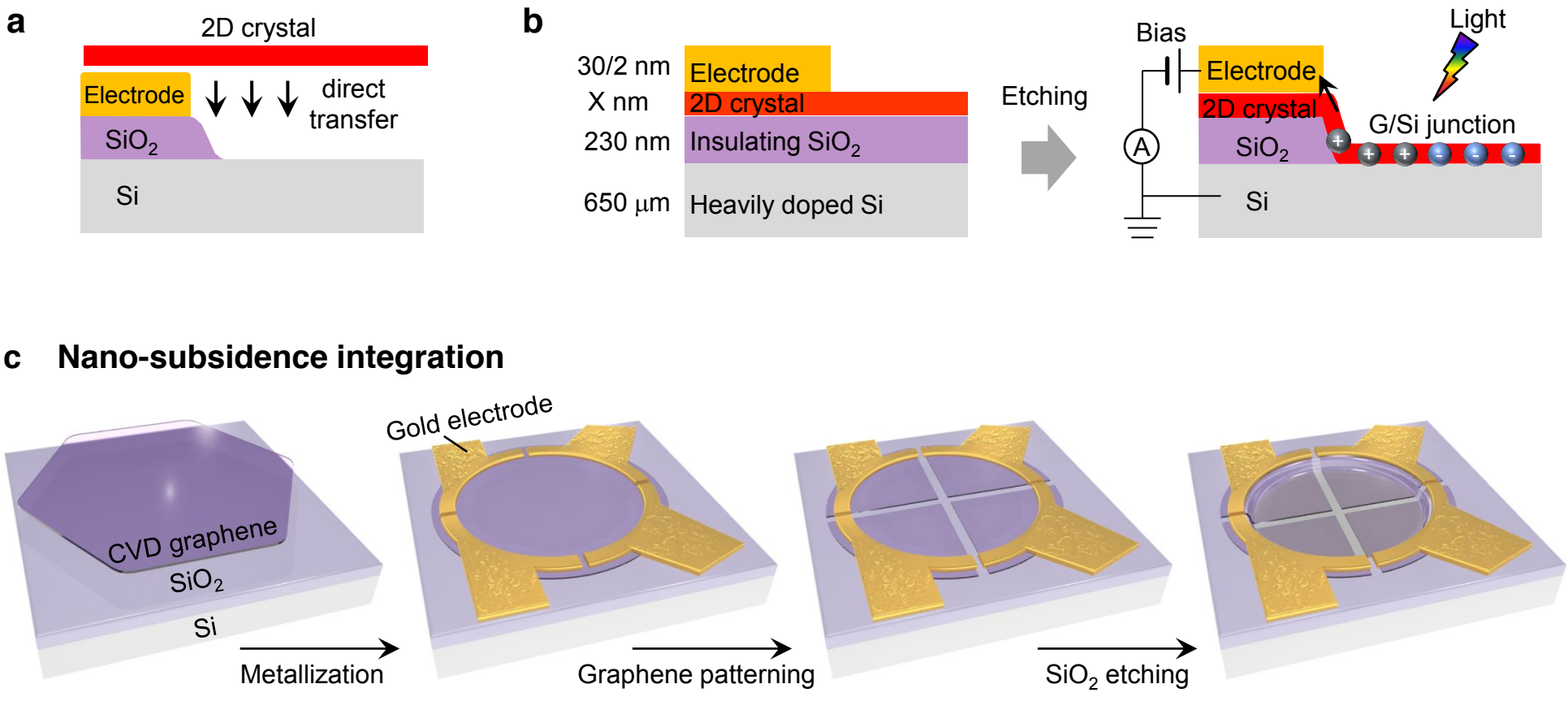

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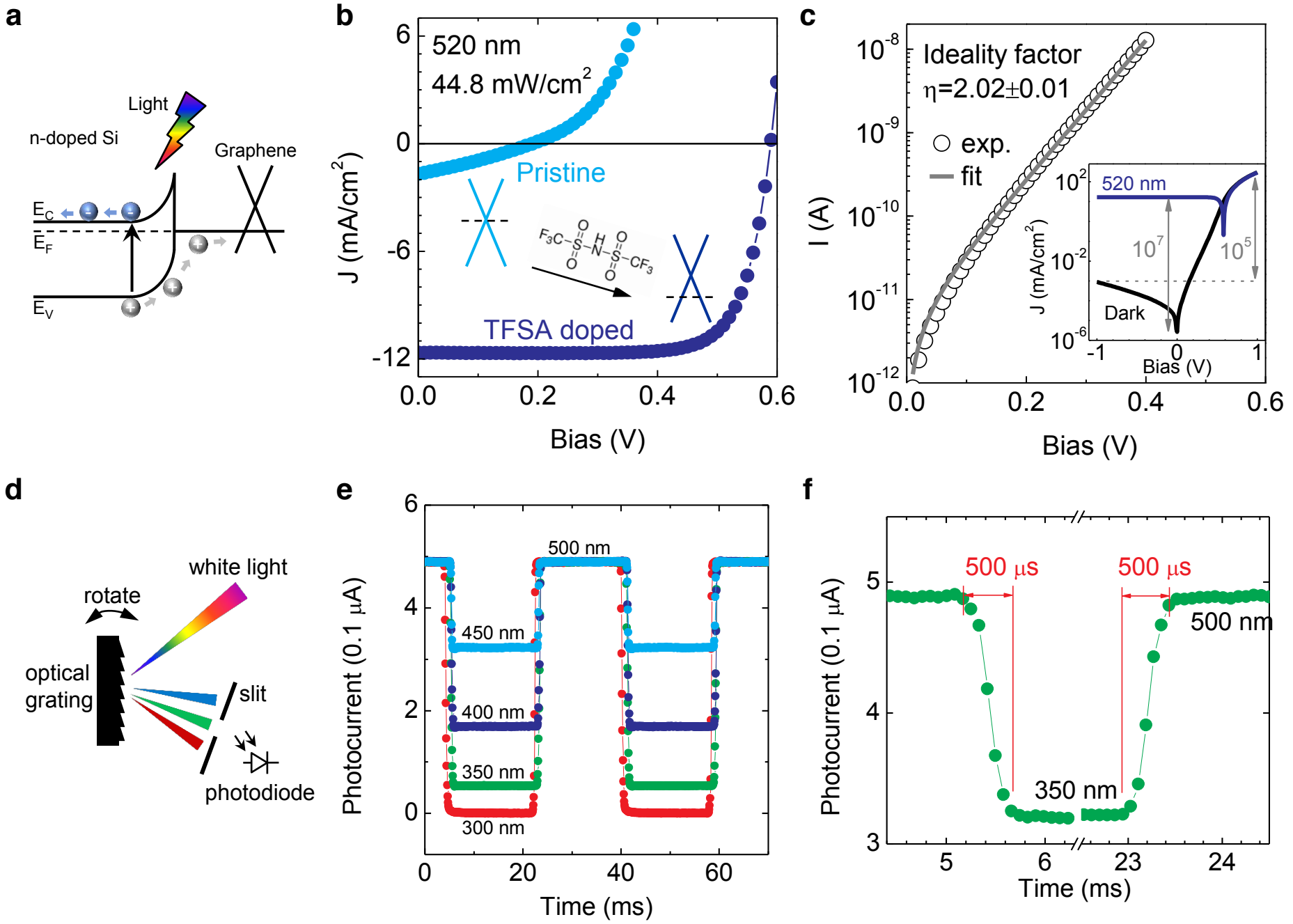

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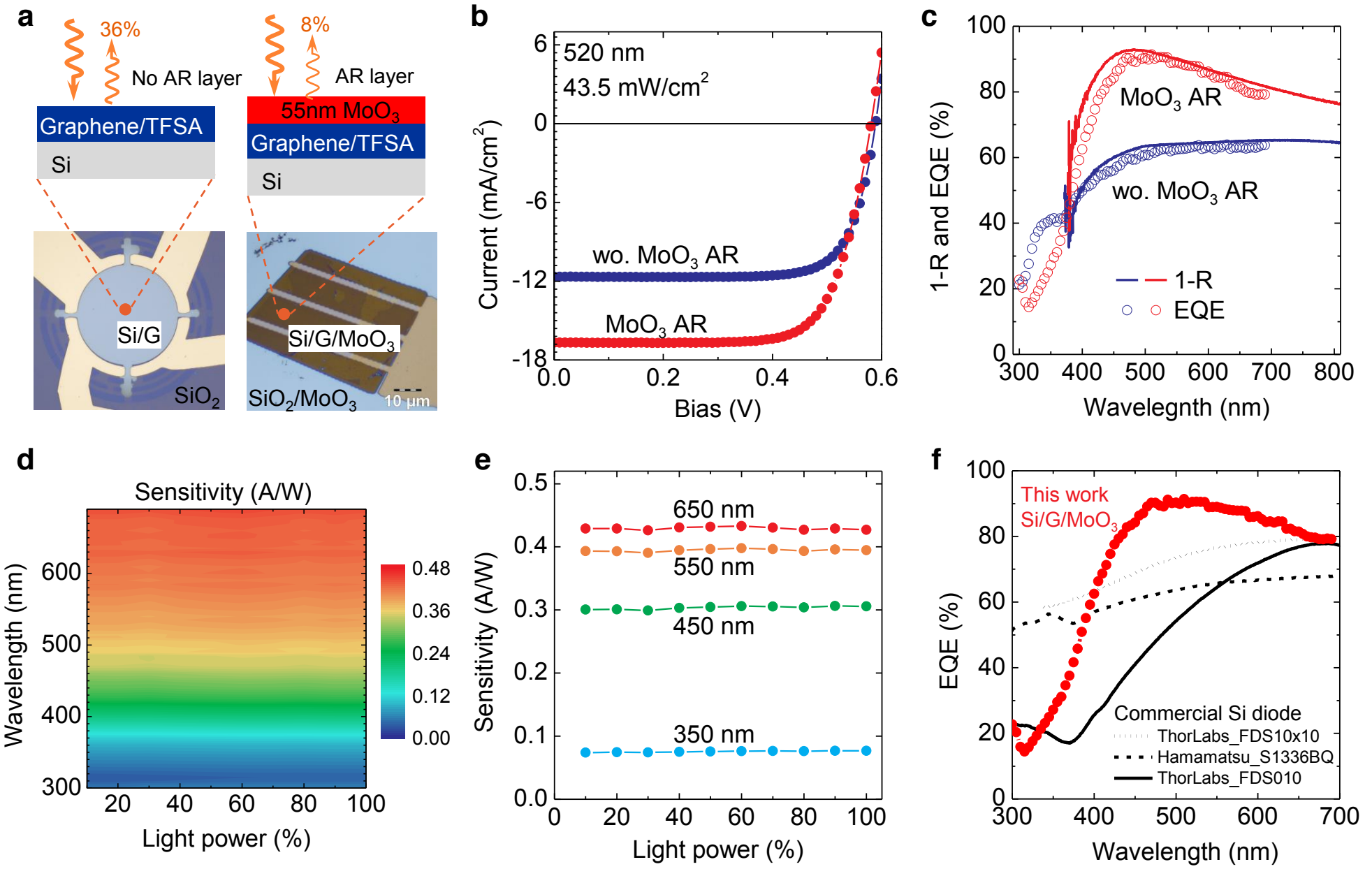

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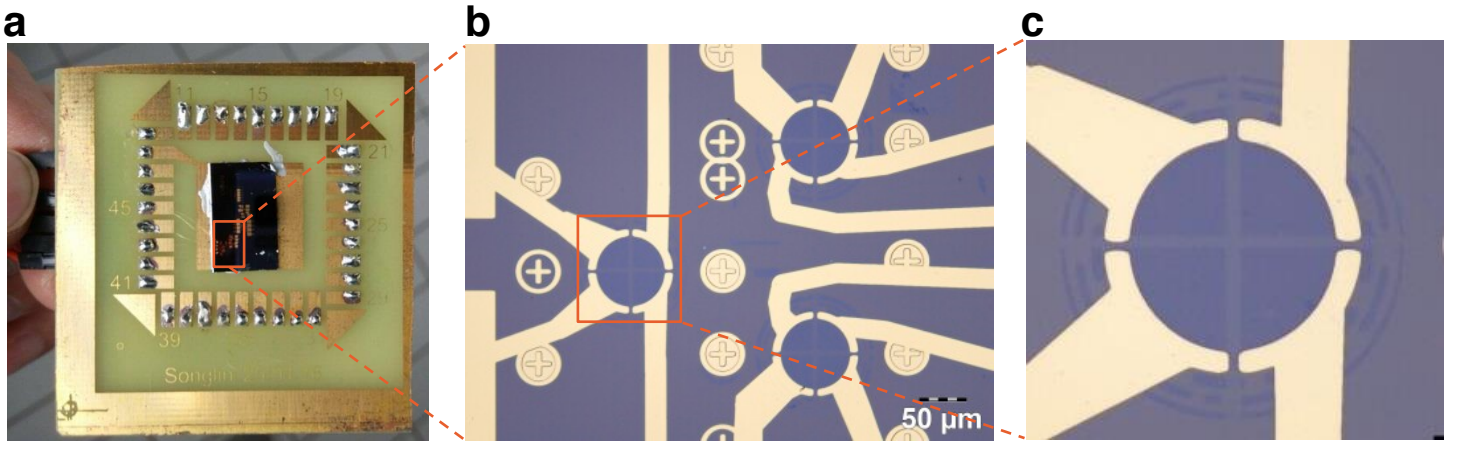

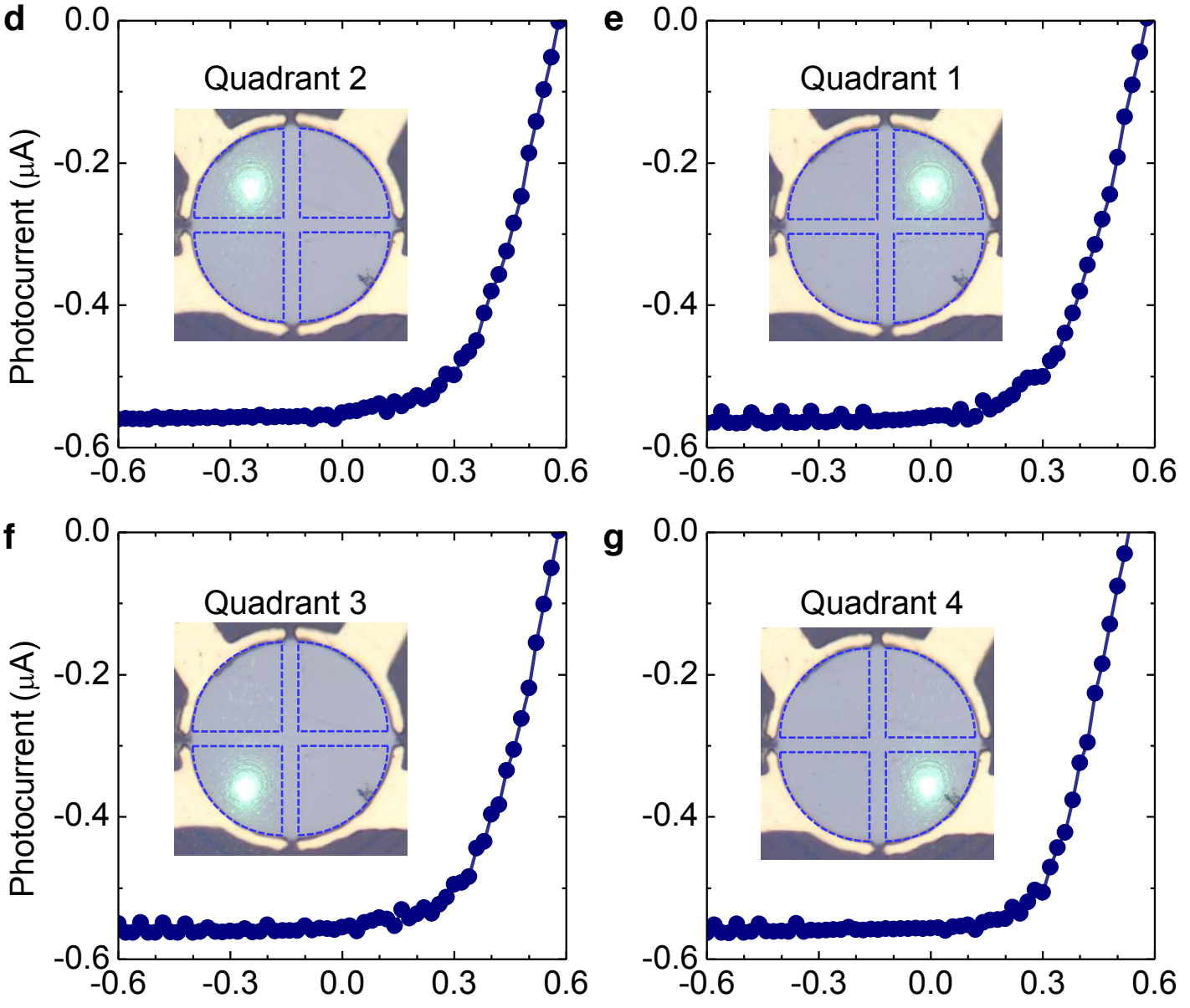

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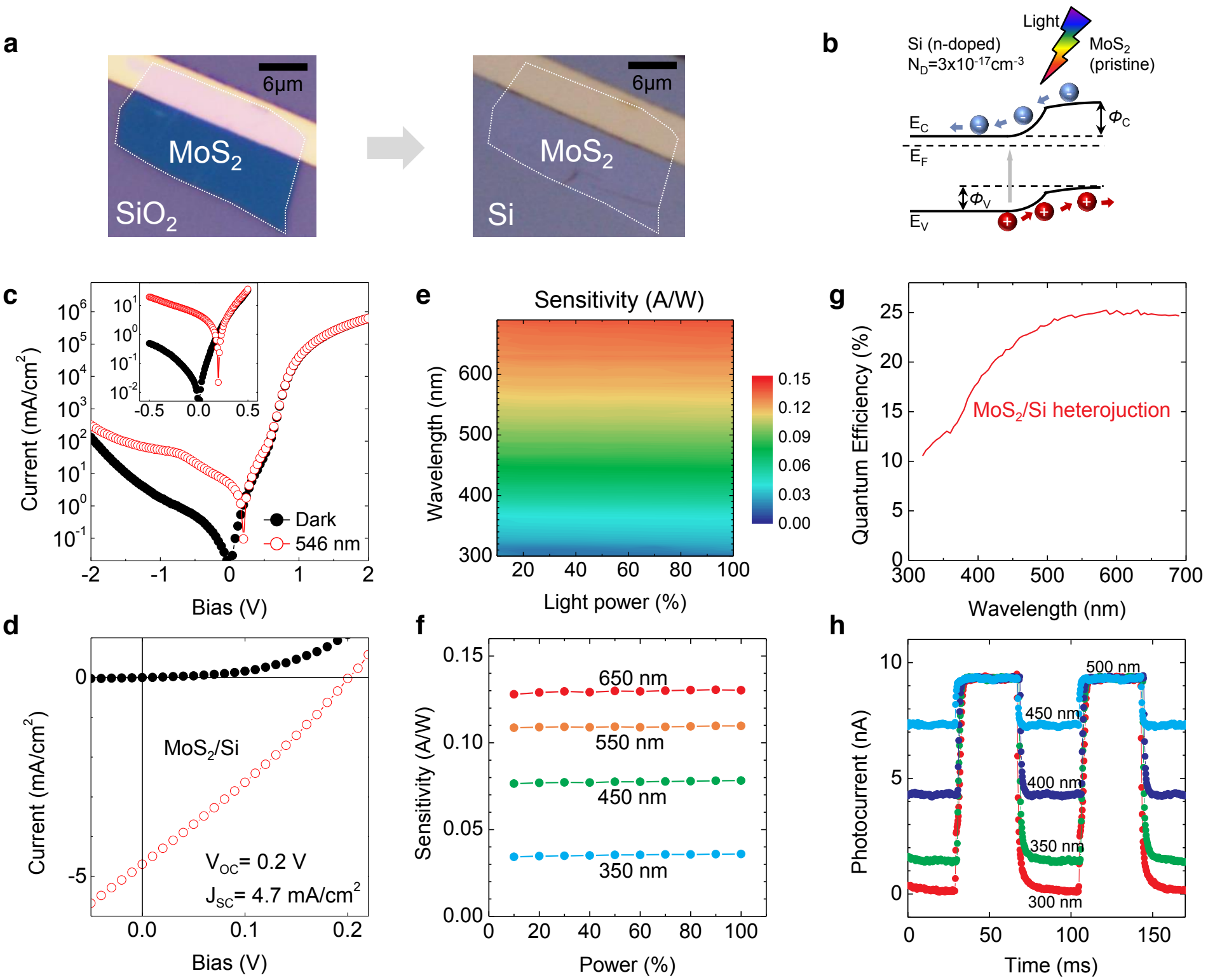

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