TSV development for miniaturized MEMS acceleration switch

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***Abstract*—Fragile micromachined MEMS structures are usually protected by bonding a capping wafer to the device wafer itself. As opposed to using lateral interconnects at the interface between the cap wafer and the device wafer, the use of vertical through silicon vias (TSVs) significantly simplifies the mounting of the components and it also results in the smallest footprint. This paper presents the concept chosen for fabricating a miniaturized MEMS acceleration switch with TSVs through the SOI (silicon on insulator) device wafer, as well as the experimental results of the TSV process development that was done for this particular application. Especially challenging was the development of an etching process that can etch the thick buried oxide of the SOI wafer through high aspect ratio trenches.**

I. Introduction

Acceleration switches are devices that open or close a circuit when a certain threshold acceleration is exceeded [1]. They may for instance be used to detect a certain acceleration event in applications where the power supply is limited or only periodically available such as in automotive, military or aerospace applications. MEMS technology enables low cost miniaturized acceleration switches with a threshold acceleration accurately defined by the design. Encapsulation of the fragile micromachined switch is preferably done at wafer-level by bonding a glass or silicon capping wafer to the device wafer. Lateral or vertical interconnects are then needed to contact the device inside the sealed MEMS cavity. Lateral electrical feedthroughs in between the cap and the device wafer result in a large footprint for the die, since wire bonding pads need to be placed outside the enclosed cavity. On the other hand, with through silicon vias (TSVs) the die size can be minimized and flip-chip bump bonding can be done. For encapsulated MEMS devices, TSVs can either be realized through the cap wafer or through the device wafer [2,3]. In order to electrically connect structures on the device wafer to TSVs in the cap wafer, a conductive bonding method is needed. However, if the process scheme and layout allows it, it might instead be less complicated to realize the TSVs through the device wafer. In that case non-conductive bonding methods can be used to bond the cap wafer. In general, fragile MEMS structures cannot be subjected to the typical process sequences that are needed to realise the TSVs. Therefore, a via-first approach will normally work best. A via-first approach also has the advantage of allowing high temperature deposition methods to fill the vias, which means that very high aspect ratio vias can be realized. For the miniaturized acceleration switch presented here, TSVs are fabricated through the SOI (silicon on insulator) device wafer, before the MEMS structures themselves are fabricated.

II. Proposed concept and process

A schematic cross-section of the proposed acceleration switch is given in Fig. 1. Using a 1.2 µm aluminium hard mask, TSVs with 7 x 70 µm through holes are etched through the SOI device wafer. Deep reactive ion etching (DRIE) is used to etch consecutively through the 40 µm silicon device layer, 2 µm buried oxide (BOX) and 300 µm silicon handle wafer. In order to avoid notching at the bottom of the TSVs, the oxide is removed from the backside of the SOI wafers and replaced by an aluminium layer. The vias are isolated from the bulk silicon using a 1 µm thermal oxide and filled with heavily phosphorus doped polysilicon. This is done by conformal deposition of undoped polysilicon and doping by phosphorus gas phase doping from a $POCl_3$ source. After the TSVs are filled, the excess polysilicon is removed from the wafer surfaces by reactive ion etching (RIE). Next the oxide is stripped from the front side of the wafer and a 100 nm thin polysilicon layer is deposited. This is done in order to protect the oxide covering the sidewalls of the TSVs from the release etch that will be done later during the processing. The MEMS structures themselves are then fabricated using DRIE through the device layer. Simultaneously, trenches are etched that divide the device layer in different regions that are electrically isolated from each other. An HF vapour release etch is done to remove the buried oxide (BOX) layer from underneath the movable structures, and a conformal NiCr/Au layer is sputtered on both sides of the wafer. The thickness of the NiCr/Au layer on the frontside (12 nm/ 250 nm) is chosen

such that it will not bridge the 2 µm gap between the released structures and the handle wafer. If subjected to a sufficient acceleration, the released silicon structure will move in the lateral direction and make contact with the sidewall of a neighbouring structure, thereby opening or closing a circuit. The fact that the sputtered Au covers the sidewalls of the silicon structures enables a low contact resistance for the switch. The fragile MEMS structures are encapsulated by bonding a glass wafer with cavities to the device wafer using adhesive wafer bonding with BCB. Finally, the Au and polysilicon on the backside of the wafers is patterned in order to define bond pads.

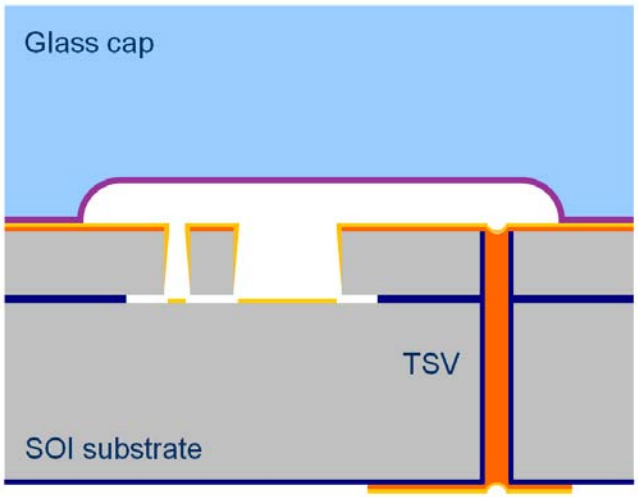

Fig. 1. Schematic cross-section of the miniaturized MEMS acceleration switch with TSV.

III. TSV ETCHING

Dry etching of the TSVs is a key step in the fabrication process for the proposed accelerometer. Process development for the deep reactive ion etching of the TSVs was done using the same SOI wafers as will be used for the actual acceleration switches.

The etch of the TSVs requires three consecutive dry etching steps which will be performed in the same dry etch tool. In the first step, the Bosch DRIE process [4] is used to etch through the 40 µm silicon device layer. In the next step, RIE is used to etch through the 2 µm BOX and in the final step, the Bosch process is used once again to etch through the 300 µm silicon handle wafer. By performing these three steps consecutively in the same dry etch tool a convenient process flow is possible.

The development of the dry etching processes involves two major challenges. Firstly we have to etch 7 µm wide trenches right through wafers that are 342 µm thick. This results in an aspect ratio close to 50:1, which poses several difficulties. The second challenge concerns the etching of the BOX layer, which for the selected SOI wafers has a significant thickness (2 µm) and it must be etched at the bottom of trenches that are 40 µm deep and only 7 µm wide. To make it possible to perform all etching steps using the same etch mask, an aluminium hard mask had to be used instead of e.g. resist.

The etch tool that is used is an Alcatel AMS200SE I-Productivity silicon etcher. It is equipped with a high density low pressure inductively coupled plasma source. The tool has been optimized to run the Bosch silicon etching process which is a so-called switched process, although it is also possible to run continuous etching processes for etching poly-silicon or dielectric thin films. The process gases used are C_4F_8, SF_6 and O_2. Their flows are regulated precisely by fast-acting digital mass flow controllers. The pumping system consists of a high capacity turbo-molecular pump which is backed by a dry rough pump. The process pressure is maintained by a system consisting of a variable conductance throttle valve and a capacitive pressure gauge. The tool is equipped with an electrostatic chuck which provides an evenly distributed clamping force for the substrate. The chuck temperature is controlled by a system consisting of an external chiller unit and resistive heaters. Thermal conductivity between the substrate and the chuck is achieved by a flow of Helium gas between the backside of the substrate and the surface of the chuck. To accelerate ionic species in the plasma sheath towards the substrate it is possible to apply a substrate bias. In this way, the energy of ionic species is controlled independently of their flux. The biasing can be achieved by either applying RF power (at a frequency of 13.56 MHz) or LF power (at frequencies below 460 KHz). If LF bias is used, it is also possible to pulse the bias on and off or between a high and low value.

As stated previously, the Bosch process is used for etching both the device layer and handle wafer. To etch through the 40 µm thick silicon device layer a straightforward single step etch recipe is used. The etch time for a target depth of 40 µm is predetermined by etching a test wafer and analysing its cross-section with the scanning electron microscope (SEM). An additional 5 % over-etch is performed in order to account for any non-uniformities in the etch-rate across the wafer.

To etch through the 300 µm handle wafer, a multi-step etch recipe must be used in order to maintain a straight and uniform etch profile. As the aspect ratio increases, it becomes increasingly difficult for the etch species (radicals and ions) to reach the bottom of the etched structures. Therefore, the durations of the etch and passivation pulses in the Bosch process as well as the applied substrate bias must be increased as the etch progresses. Depending on the balance between etching and passivation in the recipe, the etch profile can develop an unwanted positive taper (narrows towards the bottom) or negative taper (widens towards the bottom). Insufficient passivation can also lead to sidewall damage due to lateral etching [5]. By using a multi-step etch recipe, the process parameters for the etch can be altered as it progresses in order to compensate for any changes in the etch profile [6]. Several experiments were performed on patterned bulk silicon test wafers to develop an optimised multi-step etch recipe

which yields a straight and uniform etch profile for the 7 µm wide trenches.

Fig. 2 shows a SEM cross-section of one of the etched test wafers. On this wafer, the first part of the etch (40 µm) was done with the device layer etch recipe, followed by the optimised multi-step recipe that will be used for etching through the handle wafer on the actual SOI wafers. The etch depth achieved was 352 µm at the centre of the wafer which is close to our total target etch depth of 342 µm.

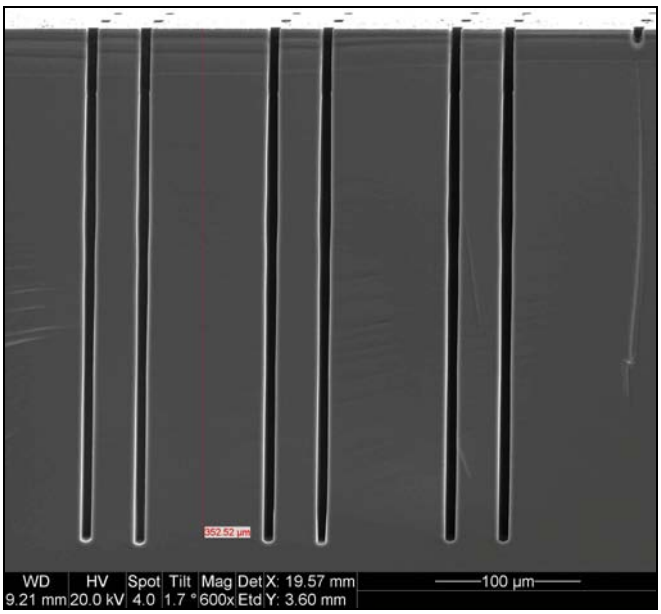

Fig. 2. SEM cross-section of a bulk silicon test wafer after performing the device layer DRIE followed by the handle wafer DRIE.

For dry etching SiO_2 it is essential to have ion bombardment at the SiO_2 surface in order to drive the etching reactions. For the present application, a 2 µm thick BOX layer has to be etched at the bottom of high aspect ratio trenches. The main difficulty is to have a sufficient amount of ion bombardment at the bottom of those trenches. In our initial experiments we used a standard dielectric etch process that is used to etch dielectric thin films on the surface of wafers. However, the etch rate of the BOX layer was extremely low which made the standard dielectric etch process unsuitable. In order to have a much greater amount of ion bombardment at the bottom of the trenches, a new etch process was developed where the process pressure was reduced and the applied substrate bias was increased significantly compared to the standard dielectric etch process. With this optimised process we were able to successfully etch through the 2 µm thick BOX layer at the bottom of 7 µm wide trenches in the device layer. Fig. 3 shows a SEM cross-section of an SOI wafer on which the device layer silicon was etched followed by the BOX layer.

Combining the developed etching processes for the device layer etch, BOX etch and handle wafer etch will allow to etch the 7 x 70 µm TSV structures proposed for the miniaturised MEMS accelerometer.

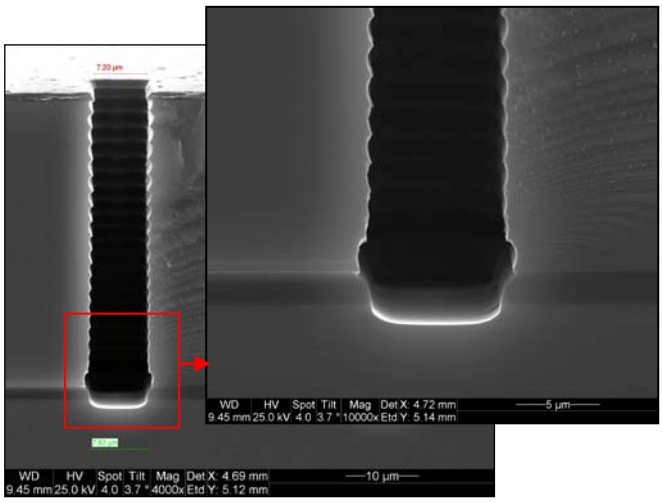

Fig. 3. SEM cross-section of an SOI wafer after etching through the 40 µm silicon device layer and 2 µm BOX layer.

IV. TSV FILLING, ETCHBACK AND METALLISATION

A short-loop experiment was conducted to investigate the filling of narrow TSV structures through silicon wafers with full thickness. TSVs with a width of 7 µm were etched through 300 µm thick silicon wafers, which corresponds to an aspect ratio of 42:1. After the aluminium etch mask and underlying oxide was stripped from the wafer surfaces, a 2 µm thermal oxide was grown to isolate the TSVs from the bulk silicon wafer. A 1 µm undoped polysilicon layer was deposited by LPCVD inside the holes and on the wafer surfaces. This layer was then doped by phosphorus gas phase doping from a $POCl_3$ source, resulting in a sheet resistance of 5.5 Ohm/sq. The sequence of depositing 1 µm undoped polysilicon and phosphorus doping was repeated several times until the TSVs were completely filled. The polysilicon that was deposited on the wafer surfaces was then removed by RIE. The recess caused by the polysilicon etchback (Fig. 4) was relatively small and did not hinder the photolithography step that was done later on. In order to characterise the polysilicon TSVs electrically, 1.2 µm Al was sputtered on both sides of the wafers and patterned using standard photolithography and wet etching. Fig. 4 shows a SEM cross-section of a U-shaped TSV structure after patterning of the aluminium.

The TSVs fabricated in this short-loop experiment showed excellent electrical results. As can be seen from Fig. 5, kelvin structures as well as daisy chains with 500 vias had 100 % yield when measuring 40 dies distributed over the wafer. A via resistance of 1.2 Ohm (stdev: 0.1 Ohm) was measured for U-shaped TSVs with a cross-section area of 1069 μm^2. For the 7 x 70 µm TSVs that will be used for the miniaturized acceleration switch, this should translate into a resistance of about 3.0 Ohm per via when taking into account the thickness of the SOI wafers.

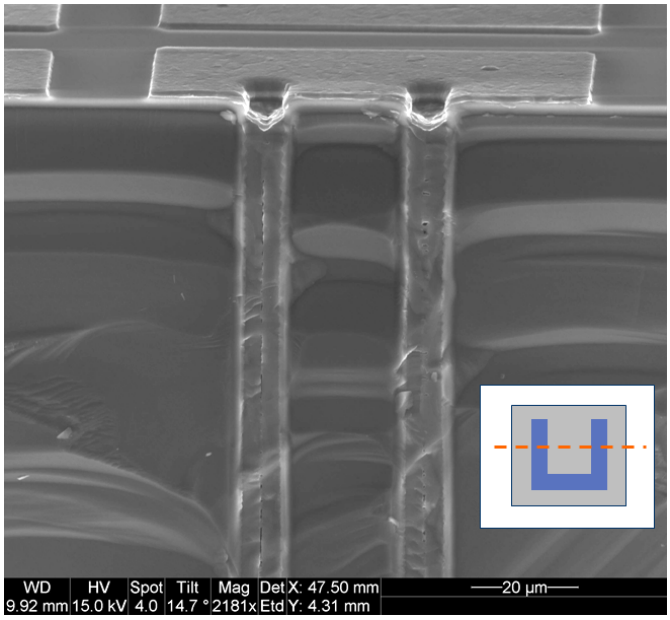

Fig. 4. SEM cross-section of a U-shaped TSV structure after patterning of the aluminium metallization. The via is isolated from the bulk silicon by a layer of thermal oxide and filled with phosphorus doped polysilicon.

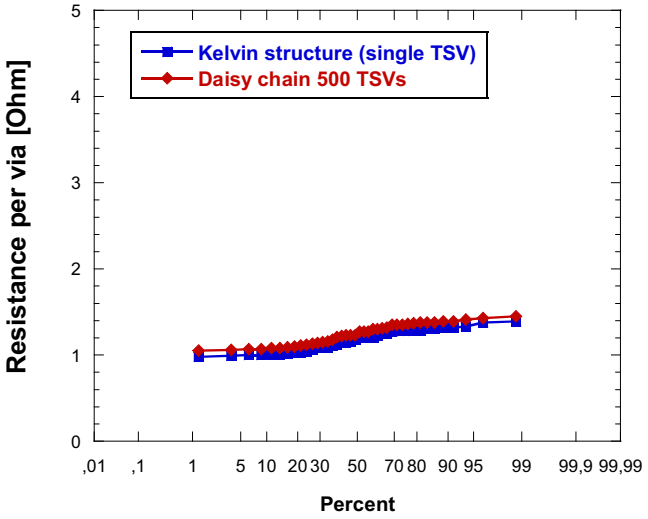

Fig. 5. Resistance per via for 7 µm narrow U-shaped TSV structures with a cross-section area of 1069 µm^2.

V. Conclusions

A novel concept is proposed for the fabrication of a miniaturized MEMS acceleration switch with through-silicon vias. Short-loop experiments were carried out in order to confirm the feasibility of the proposed concept. Advanced deep reactive ion etching recipes were successfully developed for etching 7 µm narrow TSV structures through 340 µm thick SOI wafers. Complete polysilicon TSV structures with 7 µm width were also fabricated through 300 µm silicon wafers, with excellent electrical results. Following the successful development of the processes required for realizing the TSVs in the proposed miniaturized acceleration switch, fabrication of a complete demonstrator has started.

Acknowledgment

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