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# Design of a 2X2 Reading and Writing Array for Programmable Metallization Cell

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**Abstract**

A transistor level 2X2 reading and writing array for non-volatile memory cell has been designed. This circuit is an innovative reading and writing circuit designed specifically for Programmable Metallization Cells (PMC). The write circuitry is designed to provide appropriate positive and negative voltage bias to an individual PMC memory cell in order to program it to high resistance state (write '0') or low resistance state (write '1'). A terminal switching mechanism is constructed using two pairs of complimentary MOS transistors in writing circuit. The read circuit is designed to read the data on an individual PMC memory cell based on current sensing. Row and Column decoder circuits have been used to access the desired cell depending on the provided address. Apart from the row and column decoder circuit, a Read-Write access circuit is also incorporated to select the read or write operation based on the input on the R/W line. A 2x2 memory cell array is illustrated in this paper to demonstrate the circuit's functionality; however, the circuit can be easily expanded to control memory cell arrays of any size.

***Keywords:*** Non-volatile Memory; Read circuitry; Write circuitry.

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* Corresponding author.

## 1. Introduction

Non-volatile memory is a memory device that can retain stored information even when electric power is not applied.

Examples of non-volatile memory include read-only memory, flash memory, and most types of magnetic computer storage devices. Usually, non-volatile memories are used as secondary storage in computers or as long term persistent storage. Programmable metallization cell (PMC) is a new type of non-volatile memory devices based on the Chalcogenide materials. It is proved to have fast reading/writing speeds and high scalability. On the other hand, chalcogenide memory devices are based on phase and/or electrochemical reactions, thus they have excellent data retention characteristics as compared to the flash memories that are based on the charge storage mechanism.

### *1.1. Programmable Metallization Cell*

There are in general two types of chalcogenide memories, i.e. Programmable Metallization Cell and Phase Change Memory. Programmable Metallization Cell (PMC) is a relatively newer one of the two. The active layer material of a PMC cell is a special type of chalcogenide glass named solid state electrolyte. A few examples of solid electrolytes used to form PMC include Ag-Se/S, Cu-Se/S, Ag-Ge-Se/S, Cu-Ge-Se/S [1-4].

A PMC cell is formed by sandwiching a thin layer of solid state electrolyte between an anode and a cathode terminals as shown in Figure 1. Anode must be a metal material that matches the metal ions contained in active layers. For example, if the solid state electrolyte is silver (Ag) based, i.e. Ag-Se or Ag-Ge-Se, the anode must be Ag. Cathode is an inert electrode, such as nickel (Ni) or aluminum (Al).

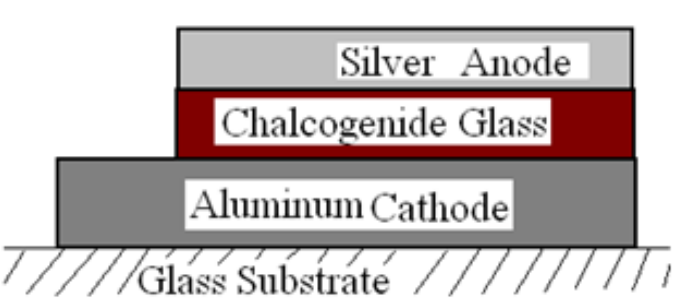


**Figure 1:** Cross-section view of a PMC cell fabricated on glass substrate. This device is a silver-based PMC [1].

The PMC cells can store data because it could switch between two non-volatile phases with different resistivity. Applying an above threshold forward voltage bias on the PMC cell causes the metal ions in the solid state electrolyte to be reduced to metal atoms and accumulate at cathode; and the metal atoms in the anode will be oxidized and enter the active layer to replenish the lost metal ions. This process eventually forms a conduction link between two electrodes, therefore, the PMC reaches a low resistance state, which corresponds to logic '1'. [5-7]. On the contrary, a reverse voltage bias causes the cathode to oxidize the previously accumulated metal

conduction link. This eventually dissolves the conduction links between the anode and cathode, therefore, the PMC reaches a high resistance state, which corresponds to logic '0'.

### *1.2. Reading and Writing Process of a Sample PMC*

A typical I-V characteristic of a PMC memory cell is shown in Figure 2. In our design, the voltage at which PMC switches from high to low is chosen as 0.5V, which is called the "SET" voltage; and the voltage at which PM switches from low to high is chosen at -0.8V, which is called the "RESET" voltage. The resistivity of high resistance (logic '0') state is three orders of magnitude greater than that of the low state resistance (logic '1') state.

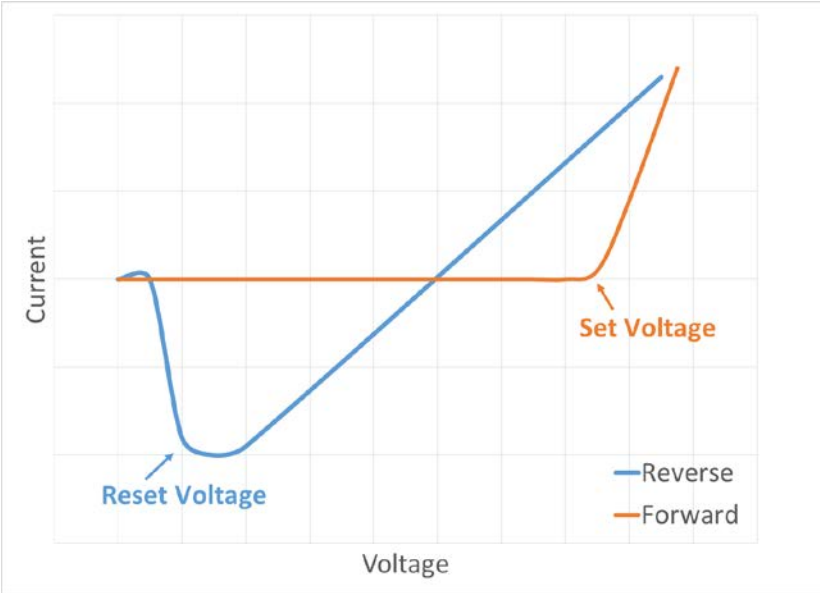


**Figure 2:** Illustration of I-V characteristic of a PMC cell

The reading and writing process for a sample PMC memory cell that serves as our design target can be summarized as following:

**1) Writing logic '1':**

To record logic '1' or to set a PMC cell, a forward voltage bias is applied. A 0.5V voltage pulse of 30-50 ns is used for this process.

**2) Writing logic '0'**

To record logic '0' on the cell, a reverse voltage bias of -0.8V is applied. A -0.8V voltage pulse of 30-50 ns is used for this process.

**3) Reading the data**

A low voltage pulse of approximately 0.1V is used for reading. The resulting current from the PMC cell is compared with a reference value to identify the logic state. If the current is higher than the reference, logic '1' is identified; if it is lower, logic '0' is identified.

The writing process requires access to both polarities of PMC cell, therefore a NMOS transistor plus a PMOS transistor is used in the design of the write circuit.

## 2. Design of Reading and Writing Array

The design process of our 2x2 reading and writing array is explained in this session

### *2.1. Reading and Writing Circuit of a Single PMC*

Figure 3 illustrates the block diagram of the reading and writing circuit for a single PMC memory cell [8]. The access to PMC cell is valid only when both row and column access are valid. Depends on the Read/Write control signal, either read or write circuitry is connected to PMC cell. In write circuit, data to be written (0 or 1) determines whether forward or reverse bias is necessary. In read circuit, the current generated from a 0.1V bias is compared with a pre-set reference to determine the stored data. Figure 4 shows the full schematic for write and read circuit.

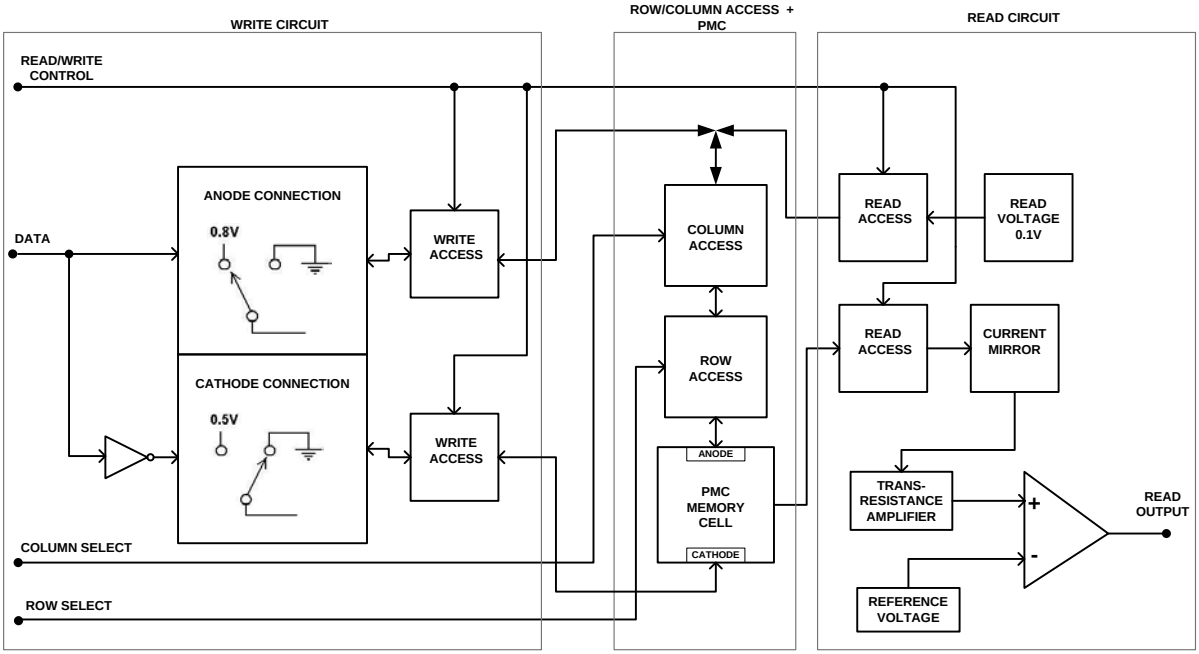


**Figure 3:** Block Diagram of Reading and Writing Circuit of a Single PMC cell [8]

The top half of Figure 4 illustrates the writing circuit. The writing circuit is used for recording data onto a PMC cell. Typically, logic '1' is recorded on the PMC cell by a current flowing from anode to the cathode at a voltage of 0.5V (positive bias), whereas the logic '0' is recorded by a current flowing in the reverse direction from cathode to anode at a voltage of 0.8V (negative bias).

To implement this behavior, a terminal switching mechanism is constructed using two pairs of complimentary

MOS transistors. Depending up on the input data, the transistor pairs toggle the anode and cathode terminals of the PMC between voltage sources and ground. The transistor pair consisting of P_Wr_1 (PMOS) and N_Wr_0 (NMOS) is active when the input data is '1', while the pair consisting of P_Wr_0 (PMOS) and N_Wr_1 (NMOS) is active when data is '0'.

When the input data is '1', transistor P_Wr_1 connects the anode to a voltage source of 0.5V and N_Wr_0 connects the cathode to ground, thus a current flow occurs from anode to cathode at a voltage of 0.5V setting a low resistance in the PMC cell. During this operation, the other pair of transistors is turned off.

The same operation is conducted in the reverse direction for an input data of '0' using the other pair of transistors. Transistor P_Wr_0 and N_Wr_1 connect the cathode to a voltage source of 0.8V and the anode to the ground respectively. This results in a current flow from cathode to anode, setting a high PMC resistance. Additionally, CMOS switches are employed for Row, Column and Read/Write control.

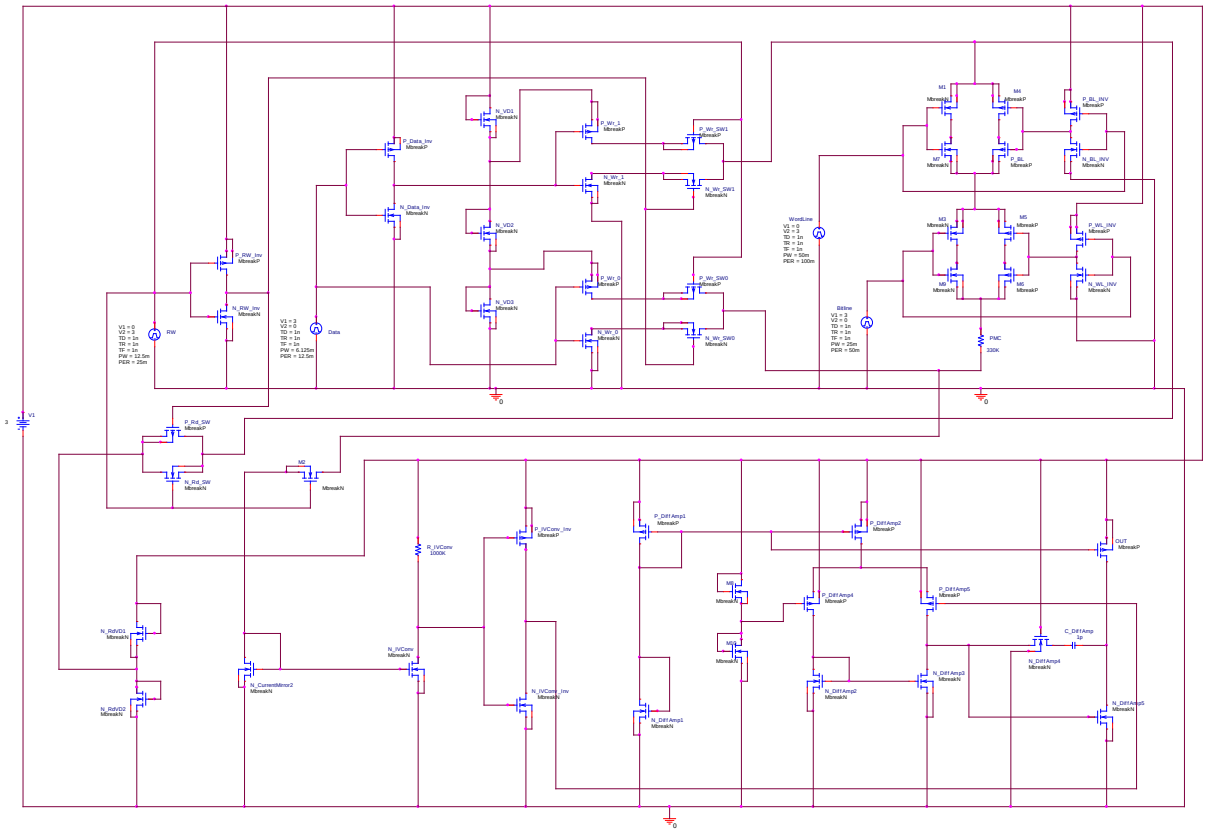

**Figure 4:** Reading and Writing Circuit Schematic for a single PMC cell.

The reading circuit for determining the resistive state of a PMC memory cell is shown in the bottom half of Figure 4. The circuit consists of a current mirror, trans-resistance amplifier and a voltage comparator. Additionally Read/Write access switches are also involved in the circuit.

A read voltage ($V_{read}$) of 0.1V is applied across the PMC cell to read the data stored in the cell, this voltage causes a current flow of the order of 1nA or 1uA respectively for High ($R_{high}$) and Low ($R_{low}$) states of the PMC

cell's resistance. This current passes through a current mirror and is subsequently converted to an amplified voltage using a trans-resistance amplifier. Finally the voltage output of the amplifier is compared with a reference voltage ($V_{ref}$) using a differential amplifier. The resistor R_IVConv in the trans-resistance stage plays an important role in creating appropriate voltage margin between high and low states. It is selected based up on the read voltage used (0.1V), the ratio of transistors in the current mirror (N_CurrentMirror2:N_IVConv) and the low state resistance of the PMC cell.

$$R\_IVConv = \left(\frac{Vdd}{Vread}\right) \times \left(\frac{(W/L)1}{(W/L)2}\right) \times R_{low} \qquad (1)$$

A logic '0' (high resistance) stored in the cell results in a voltage output less than the reference voltage from the trans-resistance amplifier, while a logic '1' (low resistance) results in a voltage greater than the reference voltage. Thus, the differential amplifier outputs a high voltage for logic'1' and low for logic '0' stored in the cell.

### *2.2 Reading and Writing Circuit of 2X2 PMC Array*

To implement a reading and writing circuit for a PMC cell array, the above mentioned single reading/writing circuit is used in conjunction with Row and Column selector circuitry to access a specific PMC cells in the array. To demonstrate the functionality of the circuit, a 2x2 memory cell array has been used as an example. Below in Figure 5 is the block diagram for Reading and Writing circuit for a 2X2 memory cell array.

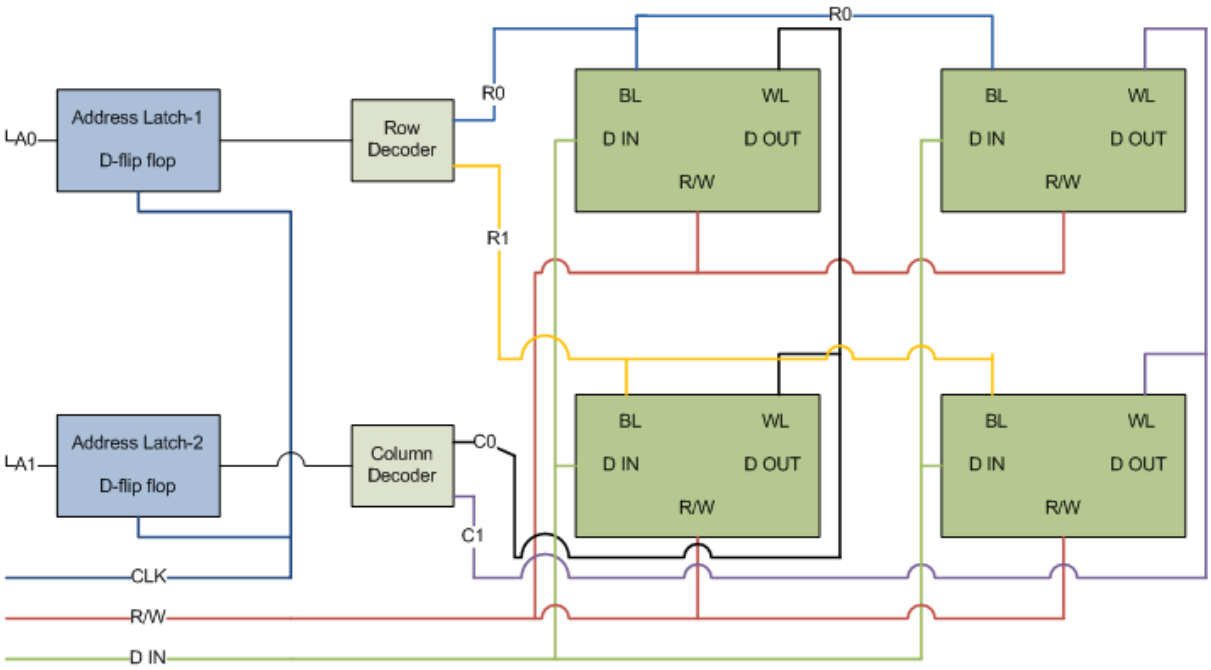


**Figure 5:** Block Diagram of 2X2 Reading and Writing Array.

To implement the row and column selector circuits, binary decoders have been used. The first output (R0) of

Row Selector is connected to the Bit-Lines of the first row of cells, i.e. cell 1X1, cell 1X2. The other output (R1) is connected to the Bit-lines (BL) of second row cells, i.e. cell 2X1 and 2X2. Similarly, the first output of column selector (C0) is connected to write lines of first column cells, and the other column decoder output (C1) is connected to the second column.

### *2.3 Binary Decoder of 2X2 Reading and Writing Array*

A decoder is a device which does the reverse of an encoder, undoing the encoding so that the original information can be retrieved. The same method used to encode is usually just reversed in order to decode.

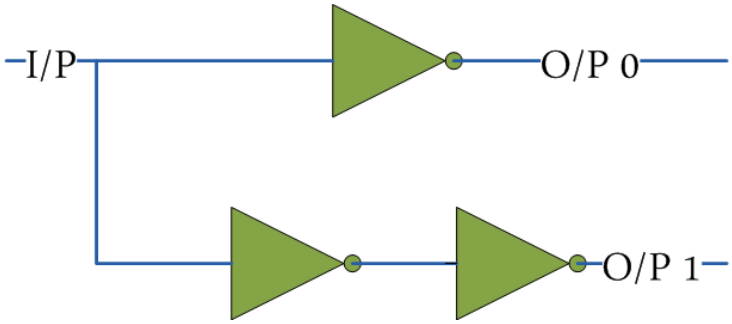


**Figure 6:** A Simple 1-2 Decoder

For this design we are using two simple 1-to-2 decoders as row-decoder and column-decoder. These decoders are used to select a cell from an array of cells. The data bits are given as inputs to these decoders and the outputs are connected to bit lines and write lines of the individual cells in the cell array. Depending on the input data different cells are selected. A simple 1-to-2 decoder can be represented as shown in Figure 6. To expand the design to larger memory array, only the decoder part needs to be change to an n-to-$2^n$ decoder, other portion of the design remains the same.

### *2.4 Final Design of 2X2 Reading and Writing Array*

Table 1 illustrates the row/column decoder operations. The first bit A0 of the address is given as input to the row decoder. The decoder output is connected to bit lines of a specific cell in the array. The first output R0 is connected to the bit line of first row cells, whereas second output R1 is connected to the bit lines of second row cells. This way if the input is 0, the outputs are 0 and 1 for R0 and R1 respectively, i.e. first row will not be active whereas the second row will be active.

The second bit A1 of the address is given as input to the column decoder. The decoder output is connected to write lines of a specific cell in the array. The first output C0 is connected to the write line of first column cells, whereas second output C1 is connected to the write lines of second column cells. This way if the input is 0 the outputs are 0 and 1 for C0, C1 respectively, i.e. first column will not be active, second column will be active.

When the address comes in to the circuit the first bit of the address A0 is given to address latch 1 and the second bit A1 to address latch 2. At the rising edge of the clock, the address is passed on to the row and column decoder

circuits. A PMC cell is accessible if and only if both the inputs BL and WL are high. The remaining operations completely depend on other inputs given to the circuit.

**Table 1:** Mapping cells to different address lines

| A1 | A0 | R1 | R0 | C1 | C0 | Active Cell |
|---|---|---|---|---|---|---|
| **0** | 0 | 1 | 0 | 1 | 0 | Cell 2x2 |
| **0** | 1 | 0 | 1 | 1 | 0 | Cell 1x2 |
| **1** | 0 | 1 | 0 | 0 | 1 | Cell 2x1 |
| **1** | 1 | 0 | 1 | 0 | 1 | Cell 1x1 |

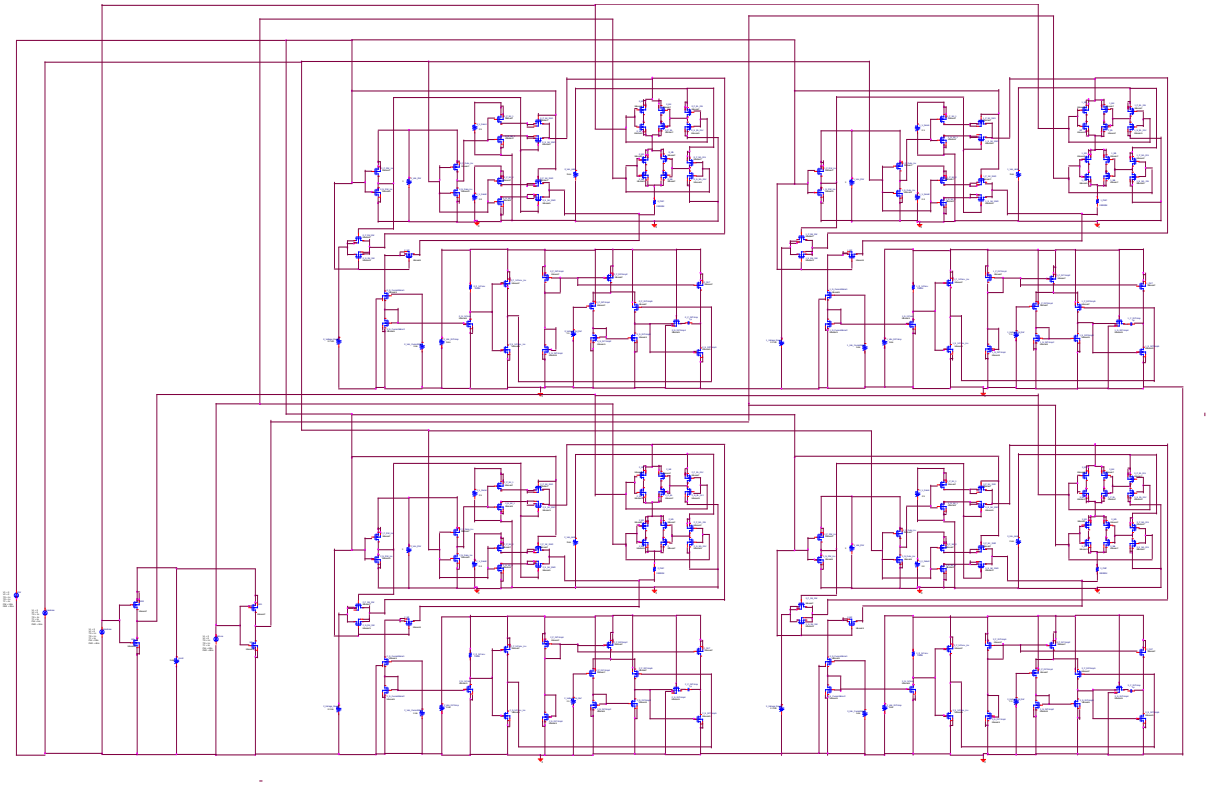

**Figure 7:** Final Design Schematic of 2X2 Reading and Writing Array for Programmable Metallization Cell

The other two inputs to the PMC reading/writing circuit are data input and R/W input. Every PMC cell in the array has its own Read-Write circuit. One of the two operations, whether Read or Write comes into play depending on the R/W input. If the R/W input is high, read operation is performed and the data stored on the PMC cell is sent to the output. If the R/W input is low, the write operation is performed. Depending on the data at the input, the write circuit applies a proper bias to the PMC cell. If the input data is '1', the write circuit applies a positive voltage bias of 0.5V, and while the data is '0', a negative bias of 0.8V is applied on the corresponding PMC cell. Final design schematic is shown in Figure 7.

## 3. Simulation Results

The final design circuit is constructed and simulation in PSPICE to verify the functionality of our design.

### *3.1 Reading Circuit Simulation*

As has been discussed above, the read operation is performed when the read/write line is high. The read circuit delivers an output of 3V for a data '1' stored on the PMC cell, while 0V for data '0' on the cell. To simulate the operation of the read circuit, we have preset the following data on the PMC cell, by using a resistance of 330K for data '1' and 330,000K for a data '0'. These resistor values closely match the high and low state resistance states of the PMC memory cell, see Table 2.

**Table 2:** Initial Data in PMC cell

| PMC Cell | Pre Stored Data | Resistance of the PMC Cell |
|---|---|---|
| 1X1 | 0 | 330000K |
| 1X2 | 0 | 330000K |
| 2X1 | 1 | 330K |
| 2X2 | 1 | 330K |

Based on above data, we simulated the voltage outputs on the read circuit corresponding to each PMC cell in the 2x2 cell array as presented in Figure 8.

**2X2 cell:** For the 2X2 cell, we observe a read circuit voltage of 3V, while the input on the address line is "00" (row line='0', column line='0') read/write line is high. This signifies that the pre-set data stored on this particular cell is '1', hence the 3V output.

**1X2 cell:** For the 1X2 cell, we observe a read circuit voltage of 0V, while the input on the address line is "01" (row line='1', column line='0') read/write line is high. This signifies that the pre-set data stored on this particular cell is '0', hence the 0V output.

**2X1 cell:** For the 2X1 cell, we observe a read circuit voltage of 3V, while the input on the address line is "10" (row line='0', column line='1') read/write line is high. This signifies that the pre-set data stored on this particular cell is '1', hence the 3V output.

**1X1 cell:** For the 1X1 cell, we observe a read circuit voltage of 0V, while the input on the address line is "11" (row line='1', column line='1') read/write line is high. This signifies that the pre-set data stored on this particular cell is '0', hence the 0V output.

### *3.2 Writing Circuit Simulation*

As we discussed earlier the cells are selected according to the row and column addresses. See Table 1. The write

operation is selected when Read/Write signal is low. The write circuit will deliver 0.5V to PMC if data to be written is ‘1’; or -0.8V to PMC is data to be written is ‘0’.

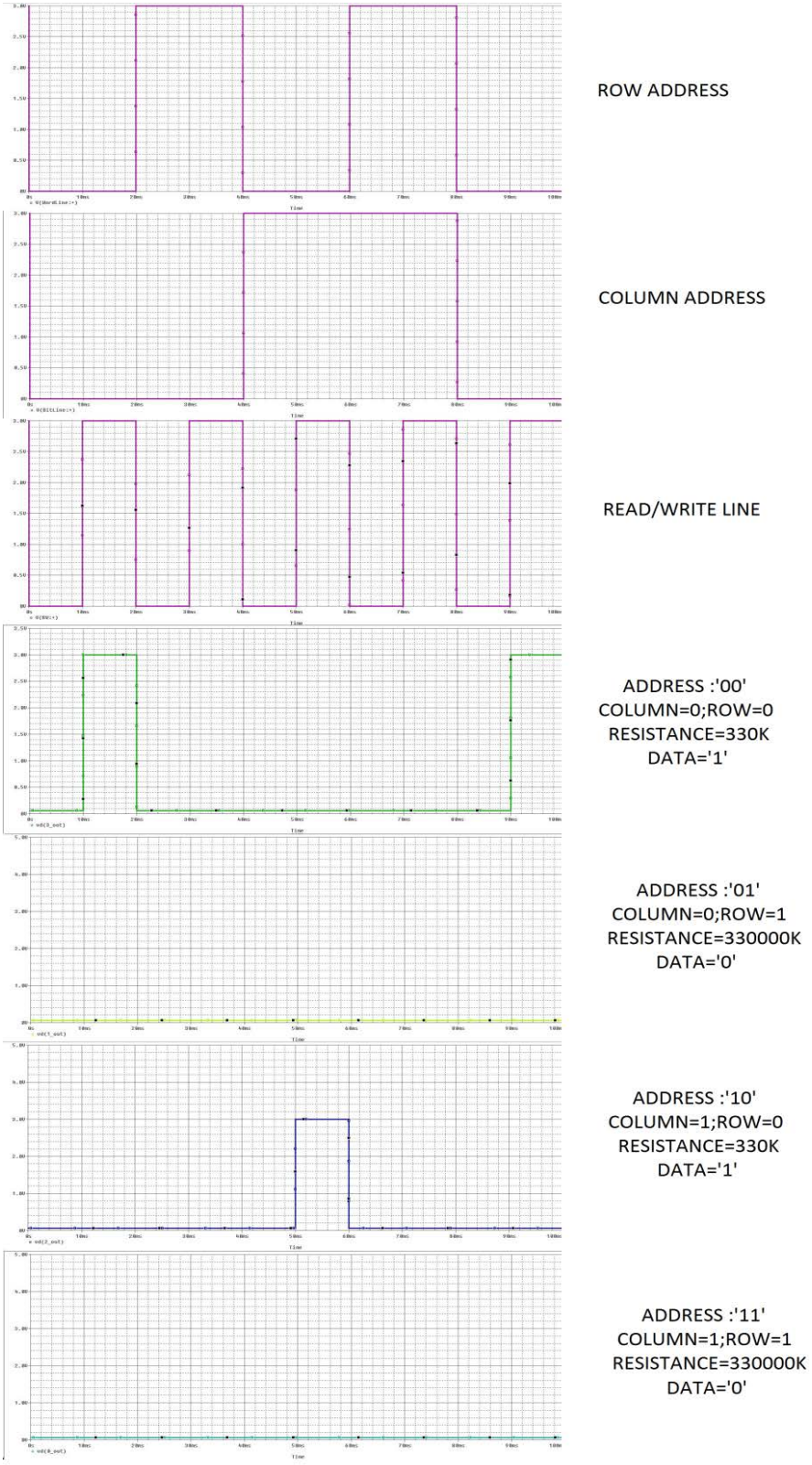


**Figure 8:** Reading Circuit Simulation Results

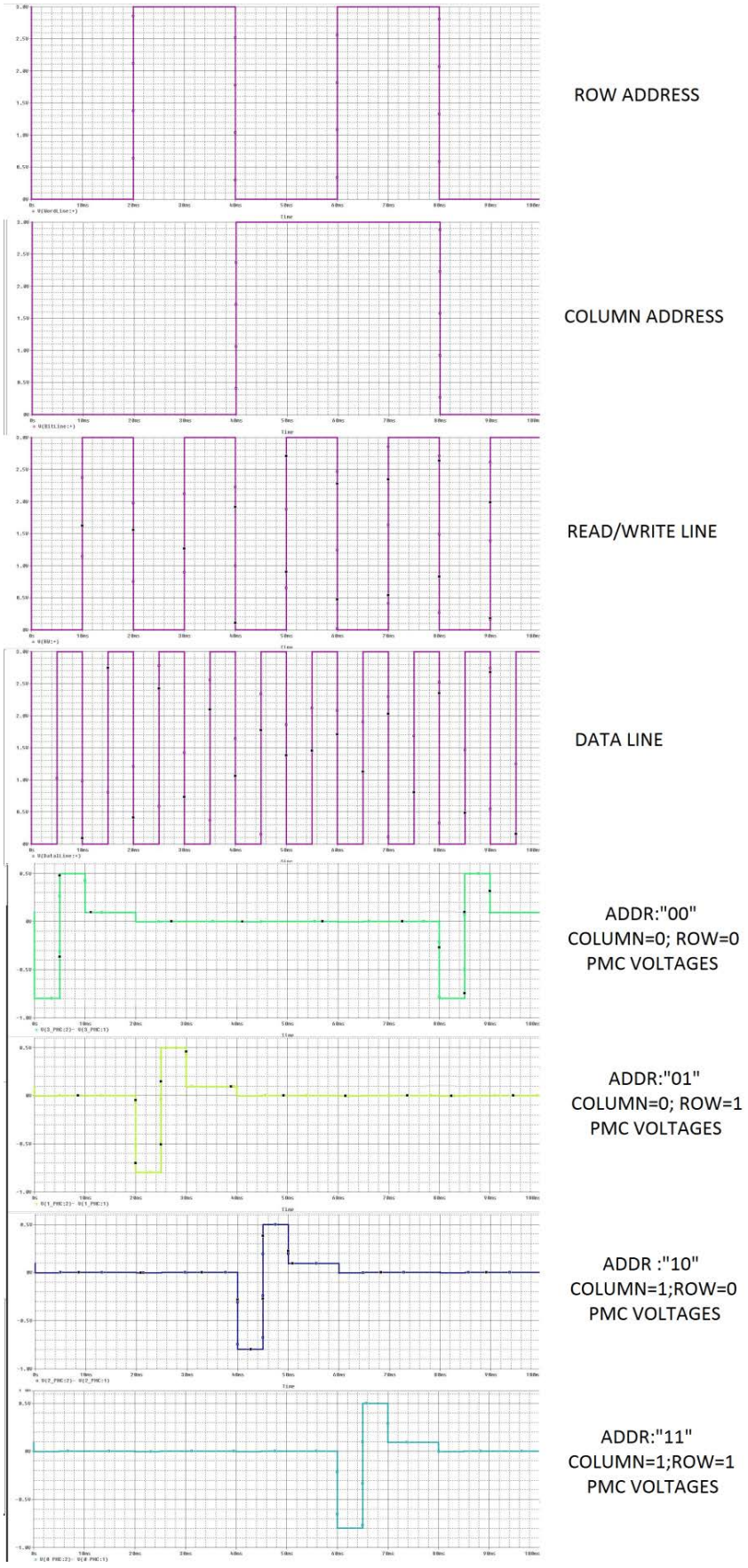


**Figure 9:** Writing Circuit Simulation Results

**When the address is '00':** Row address is '0' and column address is '0'. From table we can observe cell 2X2 will be active. When the read/write line is low, write operation is carried out on 2x2 PMC cell. The data input is written on to the PMC cell. From the figure you can see that if the input data is'1', the voltage on the PMC cell 0.5V, and when the data is '0', the voltage is -0.8V. When the read/write line is high, read operation is carried out and the content of the PMC cell will be read. For the read operation, the read circuit uses a voltage of 0.1V, therefore you can observe a pulse of 0.1V appearing on the PMC while the Read/Write line is high.

**When the address is '01':** Row address is '1' and column address is '0'. From table we can observe cell 1X2 will be active. When the read/write line is low, write operation is carried out on 1x2 PMC cell. The data input is written on to the PMC cell. From the figure you can see that if the input data is'1', the voltage on the PMC cell 0.5V, and when the data is '0', the voltage is -0.8V. When the read/write line is high, read operation is carried out and the content of the PMC cell will be read. For the read operation, the read circuit uses a voltage of 0.1V, therefore you can observe a pulse of 0.1V appearing on the PMC while the Read/Write line is high.

**When the address is '10':** Row address is '0' and column address is '1'. From table we can observe cell 2X1 will be active. When the read/write line is low, write operation is carried out on 2x1 PMC cell. The data input is written on to the PMC cell. From the figure you can see that if the input data is'1', the voltage on the PMC cell 0.5V, and when the data is '0', the voltage is -0.8V. When the read/write line is high, read operation is carried out and the content of the PMC cell will be read. For the read operation, the read circuit uses a voltage of 0.1V, therefore you can observe a pulse of 0.1V appearing on the PMC while the Read/Write line is high.

**When the address is '11':** Row address is '1' and column address is '1'. From table we can observe cell 1X1 will be active. When the read/write line is low, write operation is carried out on 1x1 PMC cell. The data input is written on to the PMC cell. From the figure you can see that if the input data is'1', the voltage on the PMC cell 0.5V, and when the data is '0', the voltage is -0.8V. When the read/write line is high, read operation is carried out and the content of the PMC cell will be read. For the read operation, the read circuit uses a voltage of 0.1V, therefore you can observe a pulse of 0.1V appearing on the PMC while the Read/Write line is high.

## 4. Conclusion

A 2X2 reading and writing array for Programmable Metallization Cell has been designed and simulated in PSPICE. The write circuitry is designed to provide appropriate positive and negative voltage bias to an individual PMC memory cell in order to program it to high resistance state (write '0') or low resistance state (write '1'). A terminal switching mechanism is constructed using two pairs of complimentary MOS transistors in writing circuit. The read circuit is designed to read the data on an individual PMC memory cell based on current sensing. Row and Column decoder circuits have been used to access the desired cell depending on the address. The row decoder narrows down a given address in to a specific row of all the available rows. Similarly, the column decoder selects a specific column depending on the address. Ultimately, the row and decoder circuit activates the corresponding cell to be accessible by reading/writing circuit. Apart from the row and column decoder circuit, a Read-Write access circuit is also incorporated to select the read or write operation based on the input on the R/W line. A 2x2 memory cell array has been used as an example to demonstrate the circuit's

functionality, however, the circuit can be used for controlling memory cell arrays of any size.

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