Charge Transport in Hexagonal-Phase Core Silicon Nanowires

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Abstract

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We built an atomically engineered laboratory inside a silicon nanowire (SiNW) to study fundamental transport mechanics and correlate results with crystal structure. We quantify the effects of ordered stacking faults (OSFs) present in SiNWs on their electrical transport capabilities. We use Raman spectroscopy to characterize the hexagonal-phase core structure of the Si crystal in our novel nanowires caused by the OSFs.

Our results indicate that electrical current is prevented from flowing within the hexagonal-phase core. Using OSFs to tune crystal structure in SiNWs can be used to control the effective cross-section of the nanowire without the need to change its physical dimensions.

We find that the channel conductivity of field-effect transistors formed using these nanowires is decreased substantially compared to the familiar cubic phase counterpart (from roughly 100 to 1 μS/cm). This result indicates that modulating crystal phase can be effective in tuning material conductivity, offering an additional degree of freedom in device engineering. We also show that hexagonal-core SiNWs have larger effective Schottky barriers with gold electrode contacts (from 0.48 to 0.67 eV), which increases device contact resistance.

Having a cubic-phase portion and a hexagonal-phase portion in series within a single kinked SiNW exploits this barrier asymmetry to create excellent gate-controlled and temperature-dependent rectifiers with rectifying ratios exceeding 100. Our transport model explains how the kink region also acts as a 10-nm scale diode.

These results indicate that controlling OSF density could be exploited in new device architectures and help optimize SiNWs for applications in high-impedance Schottky barrier rectifying transistors.

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Chapter 1

Introduction and Thesis Structure

A large portion of the physics research in this modern technological era falls into the vast domain of condensed-matter physics. Integrated circuits have transformed our lifestyle by allowing microprocessor engineering to continuously change the landscape of modern-day electronics.

Due to its enormous abundance in nature, silicon (Si) is the material of choice for substrates and channels in micro- and nano-electronics. One of the most well studied semiconductors, Si is often used for industrial applications as it is easy to manipulate, low in cost and familiar to scientists and engineers alike [1].

Nanowire geometries are promising for next-generation field-effect transistors (FETs), as these 1D channels have advantages to the usual 2D thin films (e.g. confinement effects leading to quantum dot behavior) [1, 2]. The physics of the interplay between crystal structure and electronic properties in scaled-down devices is interesting for possible industrial applications in miniaturization [3, 4].

There is also fundamental interest in studying silicon nanowires (SiNWs). Combining ordered stacking faults (OSFs) with complex heterostructures could offer new possibilities to tune quantum dots though strain engineering [5, 6, 7, 8]. Also, suspended SiNW devices could be used for Raman thermometric measurements to determine the thermal conductivity in SiNWs with OSFs and homojunctions [9, 10, 11, 12, 13].

The goal of this work is to study the contact injection and channel transport properties of a novel silicon nanowire crystal structure with the use of a Schottky barrier (SB) FET device design to acquire the necessary data. Grown with ordered stacking faults, our SiNWs are used as a tool to study the fundamental physics governing charge transport mechanisms in semiconductor materials. These OSFs generate a new local hexagonal crystal phase within the usual cubic lattice by changing the Si stacking ordering inside the nanowire volume (see Fig. 1.1(a)) [14]. The electronic properties of polytype crystals have been far less studied in group IV semiconductors compared to their group III-V counterparts [15, 16, 17, 18, 19, 20]. By studying our novel hexagonal-phase SiNWs, we provide new insight into semiconductor physics.

These polytype SiNWs have distinct properties from the already known cubic-phase only SiNWs. Since crystal structure affects charge carrier concentrations and band structure, the OSFs act as additional scattering sources and interface traps, hindering hole transport. This work will focus on eight SB-FET devices fabricated using SiNWs to form a channel between metal contacts (see Fig. 1.1(b)). The measurements of our SiNW SB-FET devices will be analyzed to show the impact of OSFs
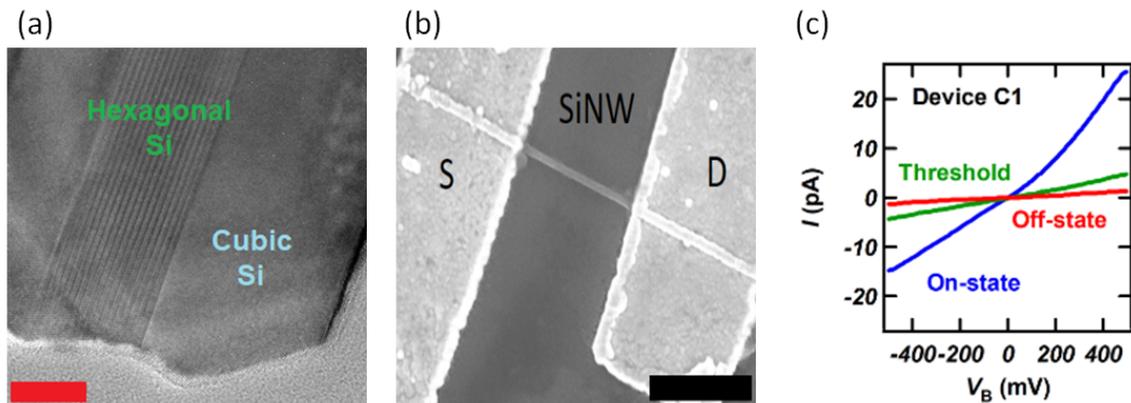
Figure 1.1: Images of our SiNW SB-FET devices. (a) TEM image of SiNW cross-section, showing hexagonal-phase Si formed by OSFs in nanowire "core", surrounded by a cubic-phase Si "shell". Scale bar 10 nm. TEM image from Moutanabbir Group archives. (b) SEM image of SiNW FET device showing a SiNW between two metal contacts (S and D). Scale bar 2 μm. (c) Representative $I - V$ data obtained from our SiNW SB-FET devices. Conductance can be tuned by the gate voltage by changing the state of the transistor (OFF-state in red, TH-state in green, ON-state in blue).

on various electronic characteristics (e.g. conductivity) (see Fig. 1.1(c)). Our data will show that OSFs increase device resistance, hindering hole currents by removing injection paths, effective nanowire cross-section and available charge density. By tuning OSF density along the length of a SiNW (from zero to a non-zero value), we will show how excellent rectifiers can be fabricated.

In Chapter 2, we will present the necessary theoretical background to help the reader understand our results. How we fabricated our SiNW SB-FET devices is the subject of Chapter 3. With the data acquisition process completed, Chapter 4 will present our key results on how OSFs affect hole transport through a SiNW. Then, we will show in Chapter 5 how we can engineer excellent rectifiers using kinked SiNWs by exploiting the properties of both Si crystal phases in a single device channel. The document ends with a brief chapter summarizing our work.

The following is a list of abbreviations used in this work.

AFM	Atomic Force Microscopy
APT	Atom Probe Tomography
BNC	Bayonet Neill-Concelman
CAD	Computer-Assisted Design
CVD	Chemical Vapor Deposition
DAQ	Data Acquisition
DC	Direct Current
DFT	Density Functional Theory
EBL	Electron-Beam Lithography
FET	Field-Effect Transistor
GUI	Graphical User Interface
HRTEM	High Resolution TEM
IPA	Isopropyl Alcohol
MIBK	Methyl Isobutyl Ketone
NW	Nanowire
OSF	Ordered Stacking Fault
PMMA	Polymethyl Methacrylate
RIE	Reactive Ion Etching
RF	Radio Frequency
SB	Schottky Barrier
SCE	Short Channel Effect
SEM	Scanning Electron Microscope
SiNW	Silicon NW
TAT	Thermally Assisted Tunneling
TEM	Transmission Electron Microscope
TFE	Thermionic Field Emission
UHV	Ultra-High Vacuum
UV	Ultraviolet
VLS	Vapor-Liquid-Solid
WKB	Wentzel-Kramers-Brillouin
WZ	Wurtzite
ZB	Zinc-Blende

Chapter 2

Transport Concepts in Hexagonal-Core Silicon Nanowire Transistors

In this chapter, we will present the concepts needed in this thesis to understand charge transport in hexagonal-core silicon nanowire (SiNW) transistors. The topics will be presented briefly, giving only what is required to move forward without full theoretical rigor. References dedicated to this subject are readily available and will be provided when relevant if additional information is desired (see Bibliography).

Section 2.1 presents the terminology that we will need to effectively discuss crystal structure, crystal defects, and electronic band structure. Using these definitions, we then present in section 2.2 the various properties of silicon crystals relevant to electronic transport in its equilibrium state. In section 2.3, we will show how the Fermi

gas model can be used to predict the conductivity of our SiNWs. In section 2.4, we will present the design and function of a field-effect transistor (FET) device fabricated using our SiNWs as the channel. This will lead to the discussion of our greatest experimental challenge in section 2.5: the metal-semiconductor contacts and the Schottky barriers (SBs). This chapter will conclude in section 2.6 with the physics of rectifying devices and how their behavior can help us understand the results presented in chapters 4 and 5.

2.1   Lattice and Band Structure

We will quickly go over the terminology from condensed-matter physics that will be used for the remaining of this text. This will allow us to properly define the material that is under study in this work.

2.1.1   Tuning SiNW Crystal Structure

Often, a semiconducting crystal is altered to tune its transport properties (e.g. charge conductivity, thermal conductivity) by incorporating a small but known amount of impurities (atoms that differ from the crystal's atomic composition) [21]. These will act as dopants, providing additional electrons or holes to the crystal, which in turn will give the material modified extrinsic properties (which we will discuss further in section 2.2).

Another method to tune a material's transport properties is to combine various

crystals of different atomic compositions to create heterostructures [1]. The new material formed by these crystals and their interfaces will often have new and interesting properties that are not simply the combination of those from its constituents.

However, a method that is less studied is by introducing controlled defects in the crystal structure itself without changing its chemical composition [1]. As a general rule, crystal defects give unwanted properties to a material. They typically create scattering centers which will hinder charge and phonon transport through the crystal. It is much simpler to try to limit defects from occurring, instead of attempting the complicated calculations required to understand their new characteristics.

There are three main classes of crystal defects [21]. The first are point defects, where individual atoms are either missing from a point in the lattice as vacancies or are placed at incorrect locations as interstitials. For example, dopants fall into this category, as they substitute an atom from the lattice to incorporate themselves. Next are line defects, which occur when a connected set of lattice points has misplaced atoms. For example, a crystal dislocation will create a line defect and will affect the mechanical strength of the material. The last are planar defects, where an entire plane in the lattice is at fault. In this work, it is this defect class that we are interested in studying.

In its natural state, the structure of a silicon crystal is two interpenetrating face-centered cubic lattices. As seen along the (111) crystal direction, the stacking sequence of the atom planes follow the 3C symmetry, meaning that three planes are required in order to generate the cubic-phase repetition. Calling these stacks "A",

"B" and "C", the 3C sequence corresponds to "...ABCABCABC..." (see Fig. 2.1(a)).
If there are no planar defects in the crystal, then the sequence is uninterrupted and
the lattice has the highest level of crystalline quality.

However, planar defects could appear, creating random deformations in the stacking sequence [22]. A single modification to the pure crystal stacking sequence is called a stacking fault. There are three main categories of stacking faults (SFs). The first are intrinsic SFs, where a single stack is missing from the sequence. For example, where "/" represents the SF, the sequence "...ABC/BCABC..." shows an intrinsic SF (the stack "A" is missing). The next are extrinsic SFs, where a single stack is added to the sequence. For example, in "...ABC/B/ABC...", the stack "B" is inserted incorrectly in the 3C pattern. The last are twin boundary faults, where the stacking sequence is rotated and the lattice becomes a mirror image of the regular order at the fault plane. This creates an inversion in the sequence at the twin boundary (for example, "...ABCA/ACBACB...").

Instead of allowing these defects to occur randomly, it is possible (in principle) to control the frequency and location of SFs within a crystal during formation. Under the correct growth parameters (see section 3.1.3), a crystal can be grown with a large number of SFs. If a set of multiple successive SFs is present in a given region, then they will become ordered stacking faults (OSFs). These in turn will create new ordered stacking sequences that differ from the 3C structure of the original crystal, which could correspond to a hexagonal close packed lattice. For example, they might generate a 9R pattern, meaning a repetition of nine stacks following the

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"...ABACACBCB..." order, giving a rhombohedral lattice. Another would be the 2H pattern, a simple hexagonal-phase lattice with the "...ABABAB..." order of two alternating stacks (see Fig. 2.1(a)).

If the stacking fault density isn't high enough, then these OSFs will simply act as defects. At least four consecutive stacking sequences are required to assign a new crystal phase [23]. In a silicon lattice, this means that a region of roughly 4 nm is required for OSFs to generate a hexagonal-phase crystal interface with the typical cubic-phase [24].

The silicon nanowires used in this work were grown by Dr. Uri Givan, a former post-doctoral researcher of Dr. Moutanabbir, at the Max Planck Institute in Germany. Using the VLS method (see section 3.1.3), our SiNWs were grown by incorporating OSFs within the lattice with the goal of generating a hexagonal-phase Si crystal (see Fig. 2.1(b)). Using TEM images, we confirm that the SiNWs have a "core-shell" structure of hexagonal-phase Si near the rectangular-shaped middle of the nanowire surrounded by cubic-phase Si near the surface (see Fig. 2.1(c)) [14, 15].

The properties of polytype nanowires having various distribution of crystal structure have already been extensively studied, especially in group III-V nanowires. In the case where two distinct elements are used to form the atomic crystal, the two equivalent symmetries for cubic and hexagonal are respectively zinc-blende (ZB) and wurtzite (WZ) [3]. Recent examples include InP nanowires and InAs nanowires [3, 4, 23].

However, theoretical studies of group IV nanowires sharing our structure are very
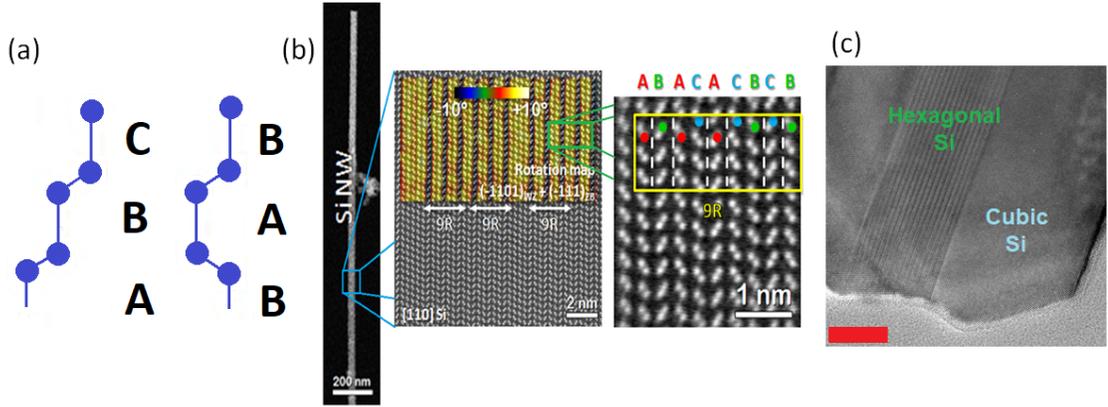
Figure 2.1: Transmission Electron Microscope (TEM) images showing the crystal structure of our SiNWs (a) Sketch of the 3C and 2H crystal stacking pattern. (b) High resolution TEM images showing the crystal structure of our SiNWs in various length scales. The 9R crystal stacking pattern can be identified. (c) TEM image of SiNW cross-section, showing hexagonal-phase Si formed by OSFs in nanowire "core", surrounded by a cubic-phase Si "shell". Notice that part of the hexagonal-phase Si portion is in contact with the NW surface. Scale bar 10 nm. TEM Images from Moutanabbir Group archives.

limited in literature, and experimental studies on their transport properties have not yet been published. Our novel hexagonal-core SiNWs are interesting to study, as they have a single chemical composition yet act as an inhomogeneous crystal structure [22]. This will allow us to focus on how solely the crystal structure affects the material's transport properties.

2.1.2 SiNW Band Structure

Crystal defects play an important role in transport mechanisms by modifying the semiconductor's band structure. For example, local lattice modifications creates new (or removes existing) energy levels available for electrons, holes and phonons. Charge traps generated by the defects often reduce the crystal's electrical conductivity, while

the addition of scattering centers alter its thermal conductivity. Moreover, the material's optical properties could also be modified. For example, new crystal vibrational modes introduced by the defects could be "Raman active", meaning detectable by Raman spectroscopy (see section 3.2.1).

As mentioned previously, with sufficient OSF density, a new crystal phase will be embedded within the surrounding lattice. In the case of our SiNWs, the hexagonal-phase Si (or "Hex-Si" for short) near the middle of the NW is sandwiched by cubic-phase Si (or "Cub-Si" for short) near the surface. This would introduce new properties beyond the familiar Cub-Si nanowire material (electrical, thermal and optical), both from the presence of Hex-Si and from the Hex-Si/Cub-Si interfaces.

The interface between two bulk crystal phases is called the grain boundary. The presence of grain boundaries in a material usually introduces several complications to the analysis of the physics governing the crystal's band structure. The interface is also rarely precisely defined, as it is often plagued by its own defects as the lattice of the two crystals attempt to bond with their neighboring atoms in the structure [1, 21].

A commonly found issue comes from lattice mismatch, when the lattice constants and the symmetry of both crystals are not identical. To successfully create an interface, the two crystals must bond with each other despite this mismatch, so accommodations must be made by introducing strain and deformations. The defects and dangling bonds generated at the grain boundary will lead to electron, hole and phonon scattering, which affects transport behavior [22, 25].

The Hex-Si/Cub-Si grain boundary is no exception to this phenomenon. With a lattice mismatch of 0.5% between Hex-Si and Cub-Si, it is expected that these new interfaces will affect the crystal's electrical and thermal conductivities (see section 2.6) [1, 26, 27].

To understand how the Hex-Si lattice alters the properties of our SiNWs, a description of the various energy levels available in both crystals and at the interfaces is required. One method to obtain a material's band structure is by theoretical calculations based on first-principles. Using appropriate approximations, the eigenstates of a crystal's Hamiltonian can be solved and plotted as band diagrams [26]. For example, with density functional theory (DFT) using the pseudopotential local density approximation (LDA), the electronic band structure of semiconductor heterocrystals can be predicted [24].

DFT calculations predict a type II band alignment (both valence and conduction bands are offset to higher values) at the Hex-Si/Cub-Si interface [24, 26, 28]. Using experimentally relevant NW diameter values (between 20 and 80 nm, depending on the study), it is predicted that both the maximum of the valence band and the minimum of the conduction band are offset to higher values in Hex-Si compared to an equivalent Cub-Si counterpart. If the crystal structure contains both phases, then the OSFs present in the SiNW will create shallow states within the gap of around 0.10 - 0.15 eV above the valence band in the NW core [24, 26].

2.2 Intrinsic and Extrinsic Transport Properties

When a crystal is pure and in thermal equilibrium, the ground-state of the semi-conductor describes its intrinsic electronic transport properties. When dopants are present to alter the material's lattice structure, new extrinsic properties of the crystal will emerge. This case is of course far more interesting, as the extrinsic electronic behavior of the crystal can be modified.

The key parameter that describes a crystal's electronic properties is its charge carrier density. It is defined as the number of electrons or holes found in a unit space of volume, and denoted by n or p, respectively. In this work, cm^{-3} units will be used when expressing charge density values, in accordance with the common unit system found in literature. How charge density is determined is the topic of this section.

2.2.1 Charge Carrier Densities

For an intrinsic semiconductor, the Fermi energy E_F is somewhere in the band gap, typically near the mid-gap point. The exact value for the intrinsic E_F depends on the electron and hole effective mass (which are determined by the curvature of the conduction and valence band edges) as well as the temperature T of the crystal [21]. If the Fermi level is exactly at the mid-gap point, then the electron n and hole p densities are equal. If not, then one of the charge carrier densities will be slightly greater than the other. However, the following simple relation will be respected between electron and hole densities, where n_i is the intrinsic carrier density and can be calculated

knowing the crystal's band structure.

$$np = n_i^2 \qquad\qquad (2.1)$$

In the case where E_F is at the mid-gap point, we will find that $n = p = n_i$, according to Eq. 2.1. Furthermore, in the equilibrium state, the Fermi energy has the same value at all points in the crystal, meaning that the charge density is constant and uniform within the material.

By applying a constant electric field through the crystal, the electrons and holes will diffuse in opposite direction, creating an electric current following Ohm's Law if the crystal is part of a closed circuit. Intuitively, the value of the current will increase when charge density increases, since more carriers will be available (this will be discussed in greater detail in section 2.3).

When a semiconductor is sufficiently doped at room temperature, it is possible to know exactly the values of both charge carrier densities. For example, in the case of an n-type semiconductor, if the density of donor impurities in the crystal is N, then it can be assumed for simplicity that $n = N$ and that p is the value given by Eq. 2.1.

However, there are a few disadvantages to controlling a semiconductor's charge densities with doping. The one most relevant to our work is that doping via ion implantation can create beam-induced damage and crystal amorphization [29]. Since our SiNWs are already grown without intentional impurities, these dopants would have to be introduced during the device fabrication process (see section 3.3), which

would both complicate the procedure and risk damaging the very crystal structure we are attempting to study.

The SiNWs used in this work are grown following the VLS process (see section 3.1.3), where gold nanodroplets are used to catalyze the growth. While it was desired to grow non-intentionally doped high purity Si crystals, some Au atoms will be incorporated in our SiNWs. Otherwise undoped, these Au impurities will give the NWs a weak p-type behavior, as Au are "deep-level" acceptor impurities in Si (creating acceptor levels far from the valence band and close to mid-gap).

Another method to tune the Fermi level must be used to control charge density in our work, as the doping approach will not be appropriate for our SiNWs with OSFs. This is done using a transverse electric field through the NW cross-section generated by an electric potential called the gate voltage. This will be the subject of a later section (see section 2.4.1).

2.2.2   Bulk Silicon Transport Properties

We briefly review the nomenclature of transport properties specific in Si. To start, we present the parameters of bulk Si in its familiar and usual cubic-phase lattice.

Si is by far the best-known semiconducting material. Textbooks on the subject of semiconductor or condensed-matter physics will either use Si as the primary example material or dedicate an entire chapter solely on its characteristics [21, 30, 31]. It is not difficult to find all relevant physical and chemical properties of bulk Si in literature.

The following table shows a list of the values for the relevant Si parameters that

will be needed in this work. Refer to the appropriate section of the text to find

information and definitions of the various properties shown.

Table 2.1: List of Typical Material Parameter Values for Intrinsic Bulk Si at Room
Temperature (300K) Used in this Work

Energy band gap	E_g	1.12 eV
Intrinsic Fermi level energy	E_{Fi}	0.571 eV
Effective mass (electron)	m_e^*	$0.33m_e$
Effective mass (hole)	m_h^*	$0.50m_e$
Relative permittivity	ϵ_r	12
Richardson constant (hole)	A^*	4.68 x 10^5 A/m^{2}K^2
Scattering-limited electron velocity	$v_{d,max}$	10^7 cm/s
Mobility (electron)	μ_e	1900 cm^2/Vs
Mobility (hole)	μ_h	425 cm^2/Vs
Resistivity at intrinsic charge density	ρ	6.4 x 10^4 Ωcm
Intrinsic charge density	n_i	1.18 x 10^{10} cm^{-3}

Values from [21, 30, 31]

We can study a semiconducting crystal in a NW geometry in order to explore how

these parameters differ from the bulk state. For example, we use the values in Table

2.1 to estimate the channel resistance of our SiNWs and then compare this to the

measured value [32].

2.3 Conductivity in the Fermi Gas Model

It is now necessary to provide a transport model to be able to predict our semi-

conducting material's conductivity. We will take our SiNWs as diffusive channels,

where the free electrons and holes within the NW drift in the orientation of the ap-

plied electric field. As long as the NW length L is larger than the mean free path

l of the carriers (average distance between collision), then the Fermi gas model will

adequately describe the electronic behavior of our SiNWs [21]. We will show later that this criteria is easily met in our work. In fact, all ballistic transport models are incorrect in our case and will therefore not be discussed [33].

In this section, we will provide the definitions for charge conductance, conductivity and mobility under the Fermi gas model. These will later be needed to properly understand the results obtained after completing the electronic measurements done on our SiNWs with OSFs.

2.3.1 Conductance and Conductivity

We begin with the familiar macroscopic version of Ohm's Law which defines the measured resistance R when applying a voltage V through a resistor. Assuming the resistor carries constant and uniform current I, one can also express the resistance using the dimensions of the resistor (length L and cross-section A) and its resistivity ρ (a property characteristic of the material used) via $R = V/I = \rho L/A$.

Equivalently, these equations can be inverted to give the definitions of conductance $G = 1/R$ and conductivity $\sigma = 1/\rho$. This simple Ohmic model will be used to describe the channel conductance of our SiNWs via $G = I/V = \sigma A/L$.

However, to understand the physics behind conductivity measurements, the microscopic version of Ohm's Law must be used. For metals (under the familiar Drude model), the relationship between effective charge density n, drift velocity v_d, electric field E and current density J also uses the concept of conductivity (where e is the elementary charge).

$$J = \sigma E = nev_d \qquad\qquad (2.2)$$

For semiconductors, both electrons and holes will contribute to current, so in general both must be accounted for when using Eq. 2.2. It can easily be shown that conductivity takes the simple form $\sigma = ne\mu_e + pe\mu_h$ in the linear regime [21].

The link between conductivity and charge density is called mobility. Note that the values for electron μ_e and hole μ_h mobility are not equal in general (see Table 2.1 as an example).

For large band gap ($E_g >> k_BT$) p-type semiconductors (our SiNWs meet this criteria), we may ignore the electron current [33]. This will allow us to write Eq. 2.3, and it is this equation that will be used in this work when calculating charge density from the measured mobility and conductivity of our SiNWs (the subscript "h" for hole mobility is dropped) [3].

$$\sigma = pe\mu \qquad\qquad (2.3)$$

Heavily doped NWs made from high quality crystals have very similar measured conductivity values, as the value of p is precisely known and controlled [34]. However, for undoped NWs (like the SiNWs used in this work), vastly different results can be obtained from even a set of seemingly similar samples. Several factors complicate the modeling of electronic transport in undoped NWs, most of which come from the NW's surface [4, 33, 34]. Impurities from the surface can act as charge traps in the form of

dangling bonds, modifying the value of p at the surface compared to the bulk value. If the NW diameter is very small, then these surface effects can completely supersede all bulk properties of the material, which complicates the analysis of electronic measurements.

2.3.2 Charge Mobility

In order to calculate the charge density in our SiNWs with Eq. 2.3, we acquire a measurement of conductivity and a measurement of mobility μ. Here, we will give the microscopic definition of charge mobility according to the Fermi gas model assumptions.

To satisfy Eq. 2.2, written under the Drude model, we define charge mobility μ as the ratio between the drift velocity gained by the charges diffusing in a material containing an electric field E and the value of that field. Since classical momentum resets after each collision, the average momentum gained by the charge between collisions is given by the impulse generated by the electric field in the time τ.

$$\mu = \frac{e\tau}{m^*} = \frac{v_d}{E} \tag{2.4}$$

In the Fermi gas model, only the free charge carriers of effective mass m^* found near the Fermi surface p_F are relevant when discussing the electrical current formed in the material under the electric field [21]. The value of τ represents the average time between scattering events (e.g. charge-phonon, charge-charge, charge-impurities).

These charge carriers, however, have a large Fermi velocity v_F, so that $p_F v_F = p v_d$. This change of perspective from the Drude model for metals to the Fermi gas model for semiconductors allows us to make a link between equations such as Eqs. 2.3 and 2.4 and the measurements done on our SiNWs [30].

Charge mobility can be viewed as a material property, expressing how effectively the charge carriers of effective mass m^* will diffuse through the crystal when a voltage is applied. Mobility is a measurement of the various scattering mechanisms the electrons and holes are subject to when in motion (this information is contained in τ). In the linear regime, mobility will not depend on E, but under a strong field the charge carrier sea will eventually saturate to its maximum drift velocity (with μ dropping as E increases). In bulk Si, the scattering-limited drift velocity saturates at 10^7 cm/s [35].

Another mechanism limiting mobility is collisions with impurities within the crystal. By doping a semiconducting NW, charge density p will increase, but this will generate additional scattering centers (the charge-phonon scattering rate increases locally near the impurity), which will lower mobility. These two competing factors must be accounted for when attempting to maximize conductivity Eq. 2.3. If these impurities are from surface states, then lowering the NW diameter will also decrease mobility [36].

Naturally, crystal defects will also play an important role in mobility. In III-V semiconductors, it is already known that polytype NWs have an undesired suppression of transport properties (e.g. conductivity), and lowering stacking fault density will

increase mobility [23]. According to Matthiessen's rule, mobility will be reduced to the value corresponding to the most dominant scattering mechanism. Our undoped intrinsic NWs are expected to have a very low mobility (several orders of magnitude lower than the bulk value, see section 4.1.2), as surface states and OSF defects will dominate transport [3, 36].

As a final note, instead of using the average time between collisions as a measurement of scattering, one could also use the average distance l (mean free path) a charge will move through the crystal before a collision using Eq. 2.5 [21].

$$l = v_d \tau = \frac{\mu}{e} \sqrt{k_B T m^*} \tag{2.5}$$

2.4 Nanowire Field-Effect Transistor Device

In previous sections, the formal definitions of relevant transport properties of a semiconducting crystal within the Fermi gas model were presented. We now require an applied model to link these properties to measurements done on our SiNWs in order to understand how OSFs affect charge transport.

The electrical measurement setup is to simply place two metal contacts on both ends on the NW channel. When applying a bias voltage V_B on the source electrode (S), an electric field inside the NW will create a current exiting the drain electrode (D) (see Fig. 2.2). Conductivity can be measured assuming the voltage drop occurs solely in the channel (however, this will not be the case for our SiNW devices, see

section 2.5 for details on how this will complicate our analysis). With Eq. 2.3, the charge density can be calculated knowing mobility which would complete the analysis of the crystal's transport properties.

The problem, of course, is that the hole mobility of our SiNWs is unknown (we can't simply take the bulk value as surface states and defects will greatly alter the value, see section 2.3.2). Furthermore, as they are undoped, the value of charge density in our SiNWs is also unknown. We require a measurement setup that permits the charge density value to be modulated by a separate tuning parameter. Studying how conductivity varies by this parameter will give us insight on which values p and μ must take to correspond to Eq. 2.3, and how they are altered by the presence of OSFs (through the *Hex* value, see section 3.2.3 for its definition).

A device setup that satisfies this criteria is the Field-Effect Transistor (FET) setup. Since a transverse electric field can modulate the Fermi level in a semiconductor, which in turn tunes charge carrier density, a third electrode is required to generate this field in our SiNW channels. In our case, this is done with a capacitively-coupled gate electrode (G) placed under the dielectric oxide layer which supports the NW (see Fig. 2.2). By applying a gate voltage V_G, it is possible to greatly change the device resistance, creating a transistor device. Details on how to fabricate these SiNW FET devices can be found in section 3.3.

To help illustrate the concepts presented in the remaining sections of this chapter, we will use data we obtained from selected SiNW FET devices. This will allow us to simultaneously show example calculations on the presented equations while providing
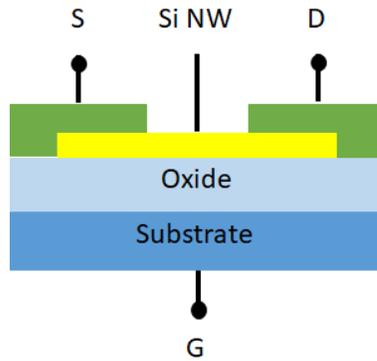
Figure 2.2: Sketch illustrating the SiNW FET design. The SiNW ends are seen between the source (S) and drain (D) electrode metal thin films and the oxide layer over the substrate acting as the back-gate electrode (G).

a useful data analysis tutorial for a reader who wishes to continue this work further. Only a few examples will be used, but a full list of all analyzed SiNW devices in this work can be found in section 4.1.

2.4.1 Gate Capacitance

A transistor device is a three-terminal electronic component where one electrode controls the current passing through the other two electrodes. For our FET devices, the voltage applied to the gate electrode produces an electric field affecting the current in the SiNW channel connecting the source and drain electrodes (see Fig. 2.2). It is important that the gate electrode produces an electric field inside the NW but does not supply current, meaning that there is no direct electrical connection between the gate and the channel. If a connection accidentally occurs, the functionality of the device is compromised (see section 3.4.2).

A dielectric material is placed between the gate and all other components of

the FET device to prevent this while creating the desired capacitively-coupled gate electrode. In our case, the oxide layer of the sample plays the role of the gate dielectric. Since the gate electrode is underneath the SiNW channel, our FET devices are in the "back-gate" configuration. Other gate configurations that can be found elsewhere are "top-gate" (the dielectric thin film is deposited over the nanowire) and "gate-all-around" (the NW is wrapped by the dielectric material), and they offer their own advantages and disadvantages.

The role of bias voltage is to generate the current itself and to vary the distribution of the carriers within the channel, while the role of gate voltage is to tune the current by modulating the value of p [37]. By applying the gate voltage, the gate field produced inside the semiconductor will move E_F by Coulomb interaction as long as the oxide layer has the dielectric strength necessary to carry the desired field.

For a heavily doped n-type gate electrode (the Si wafer backside) on a semiconductor (our SiNWs) FET device, positive values for V_G will move the channel's Fermi level from its original intrinsic position toward the conduction band, while negative values will move E_F toward the valence band (see Fig. 2.3). This means that tuning the gate voltage towards positive values will deplete the p-type NW, decreasing the current flowing through the channel. Tuning V_G toward more negative values will introduce additional holes in the SiNWs, increasing channel conductivity.

Fundamentally, the relationship between the charge introduced in the SiNW channel and the applied gate voltage is the gate capacitor. The oxide layer of thickness t_{ox} with permittivity ϵ acts as the dielectric within the capacitor. This oxide layer
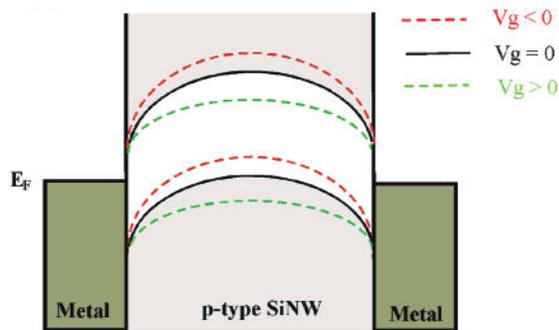
Figure 2.3: Sketch showing the effect of the gate electrode on the FET device band structure. The band structures of the metals are not affected by V_G. Image from [36]

separates the gate electrode (a conductive plane formed by the highly doped Si wafer backside) from the NW of diameter d and length L. The gate capacitance can then be calculated using a simple cylinder-on-plane model.

$$C_G = \frac{2\pi\epsilon L}{\ln(4t_{ox}/d)} \tag{2.6}$$

The issue here is that the SiNW is not metallic, meaning that Eq. 2.6 will overestimate the value of gate capacitance (the exact value of C_G is unknown). The gate field will enter the SiNW but will not be uniform in its cross-section. The top section of the NW is unaffected by the bottom gate voltage, meaning that only a small unknown volume of the SiNW near the oxide layer can be modulated by the gate [4]. For undoped NW FET devices on a SiO_2 back-gate, using 1.44 as the value for the oxide relative permittivity instead of the accepted value for the oxide layer (which is 3.9) when calculating Eq. 2.6 will account for this non-uniform gate field and give a better estimate value for C_G (we will take this calculated value as having a 10% error) [34].

Furthermore, any interfaces existing in the FET device channel either between the undoped SiNW and an oxide layer (e.g. the gate dielectric or the thin thermal oxide layer around the nanowire) or between different Si phases (for example, the Cub-Si/Hex-Si interface) will generate charge traps (see section 2.1.2). These will also reduce the effective gate capacitance, modifying the estimate for C_G as the traps will act as a series capacitance to the gate capacitor [38]. For interface trap density D_{it}, expressed in number of trap states per cm^2 per V, the interface trap capacitance C_{it} is given by $eD_{it}A_{it}$, where A_{it} is the interface area. This effect will greatly impact the gate coupling efficiency to our SiNWs, especially those with OSFs.

2.4.2 Device Switching: Transconductance and Threshold

With an understanding of the role the gate electrode takes on a FET device, we are now ready to present transport data obtained from measurements done on our SiNWs to demonstrate how to properly analyze the data and extract the desired parameters (e.g. mobility, conductivity). The model presented below is only applicable when the FET device is operating in its "linear" regime. In terms of the device parameters, this is where the current scales with the bias voltage (as opposed to the "barrier" and "saturation" regimes to be discussed later in the following section), where the bias voltage is much lower than the gate voltage, and only for FET devices where L is larger than both d and t_{ox} [39]. All presented SiNW FET devices in this work satisfy these conditions.

As our example, we use "Device C1" (see section 4.1 for full device list) to illustrate

our analysis of how the gate affects the current passing through a SiNW FET device. The relevant data from Device C1 is shown in Fig. 2.4. This particular device has a Cub-Si only (without any OSFs) SiNW of diameter $d = 50$ nm forming a $L = 2$ μm channel between two contact electrodes, all of which resting on a $t_{ox} = 300$ nm oxide layer forming the back-gate dielectric. Note that L is larger than both d and t_{ox}, as required. Using Eq. 2.6 along with the appropriate modification to the accepted value of oxide permittivity (to account for the non-ideal gate electrode), we estimate the gate capacitance to be 36.5 aF (atto- is the SI prefix for 10^{-18}).

Fig. 2.4(a) shows a graph of the measured current exiting the drain electrode at a fixed bias voltage applied to the source electrode as the gate voltage is modified. An *I-V* curve plotted under these conditions is called a transfer curve, which is often the standard method of presenting FET data to show its proper operation.
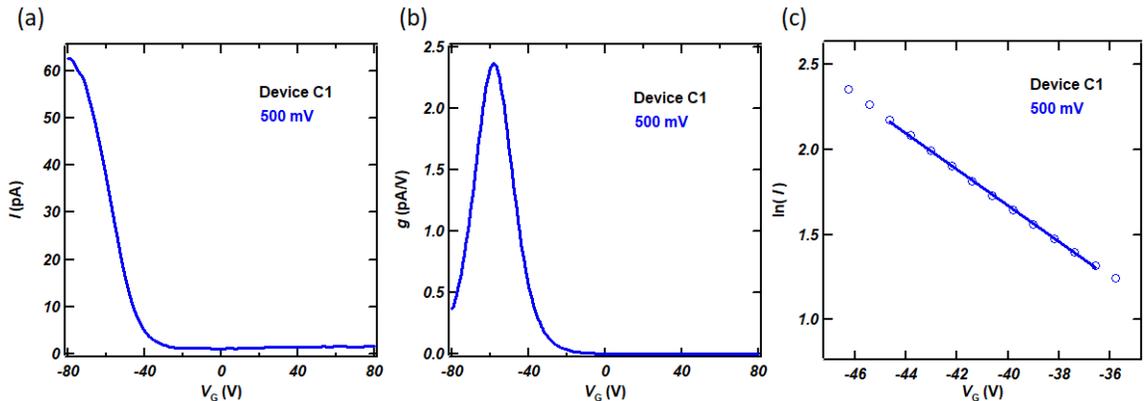
Figure 2.4: Transfer characteristics of Device C1 (see text) to demonstrate data analysis methods. All curves shown are taken at $V_B = 0.5$ V. (a) Transfer curve showing good FET behavior as the gate voltage can effectively control the device current. (b) Transconductance curve used to identify g_m parameter. (c) Logarithm of the transfer curve in the subthreshold gate voltage range. Data points are open circles, linear fit in solid line used to extract S.

Immediately, we notice that the gate electrode can effectively tune the current

passing through the channel. The $V_G = 0$ point describes the current that we would expect if this SiNW were not a part of a FET device but instead used as a basic resistor unit between two electrodes. With a very small current of 1.1 pA (showing the great difficulty we had in measuring our devices, see section 3.4.3) at $V_B = 0.5$ V, we obtain a device resistance of around 455 GΩ. This value does not change appreciatively in the gate voltage range from 80 V to -20 V, but when V_G passes through -20 V towards larger negative values we see the device conductance increasing significantly. This confirms the p-type behavior expected from our SiNWs and clearly demonstrates the "switching" profile of the gate on our FET devices.

The parameter used to describe gate switching is transconductance, labeled g. As opposed to conductance G, transconductance is defined as the differential $\mathrm{d}I/\mathrm{d}V_G$ and is visualized as the slope of the tangent on a transfer curve. As shown in Fig. 2.4(b), the transconductance of Device C1 is essentially zero in the gate voltage range from 80 V to -20 V, steadily increases to 2.365 pA/V around -58 V only to decrease again afterwards. This single peak behavior in g is the signature of a well-behaved FET device in the linear regime. The maximum value of transconductance at a given bias voltage g_m (the height of the peak) is of special importance to characterize a FET device.

The first use of identifying a FET device's g_m value is that it can be used to determine charge mobility [1]. Called the FET mobility μ_{FET}, it is used as a figure-of-merit for such transistor devices. In the linear regime, g_m scales with V_B, meaning that the measurement of μ_{FET} should be insensitive to the exact choice of applied

bias voltage as long as the FET is well-behaved.

$$\mu_{FET} = \frac{g_m L^2}{C_G V_B} \qquad (2.7)$$

For Device C1, using $g_m = 2.365$ pA/V in Eq. 2.7, we calculate a FET mobility of 5.2 x 10^{-3} cm^2/Vs. Note that this measurement was done at $V_B = 0.5$ V with g_m located at $V_G = $ -58 V, where the bias voltage is much lower than the gate voltage, as required. Typical values in literature for μ_{FET} found in similar FET devices made from undoped SiNWs are also in the 10^{-3} cm^2/Vs range, validating our results [36]. Only in the linear regime does the FET mobility μ_{FET} found using transconductance measurements equal the charge mobility μ found in the Fermi gas model equation for conductivity Eq. 2.3 [39].

The second use of identifying a FET device's g_m value is that it can be used to determine the threshold voltage V_{TH}. One of the most important values to characterize a FET device, the threshold voltage represents the gate voltage required to transition between weak and strong inversion in a semiconducting channel [40]. Visually, V_{TH} can be seen on a transfer curve at the onset of significant current flow (the device "switch" point on the V_G axis).

In order to extract a value for V_{TH}, the most widely used method is to take a linear extrapolation at the point on the transfer curve where g_m was found and calculate the point that intersects the gate voltage axis (where current equals 0) [40]. For Device C1, using $g_m = 2.365$ pA/V and $I = 33.4$ pA at $V_G = $ -58.3 V, the intersect

is calculated to give V_{TH} = -44.2 V.

As the gate voltage approaches the threshold value, the Fermi level moves from its original position inside the gap towards the valence band edge. Assuming the semiconductor has a quadratic energy dispersion for electrons and holes (which is the case for Si), a linear relationship will exist between the gate voltage difference and the displacement of E_F within the gap. This predicts an exponential dependence on charge density with respect to V_G in the "subthreshold" regime [21].

We can quantify how effectively the gate can control the Fermi level position with a parameter called the subthreshold slope, labeled S. By plotting the transfer curve on a logarithmic scale in the subthreshold gate voltage range, we expect the curve to become a straight line, indicating that conductivity indeed has an exponential dependence on V_G in this regime (see Fig. 2.4(c)). The slope S of this line measures the gate control quality of the FET device [1, 41]. A lower value for S means a better gate control quality.

$$S = \left(\frac{\mathrm{d} \log I}{\mathrm{d}V_G} \right)^{-1} \tag{2.8}$$

Theoretically, in the absence of any impurity states or interface trap states, S becomes the lowest thermodynamically possible value of $\ln 10 k_B T/e$, which numerically is equal to 60 mV/dec. However, any defects or oxide traps present in the FET device system will introduce additional states within the band gap that will require energy from the gate to occupy, reducing the effective gate control on channel conductivity.

Measuring subthreshold slope becomes a method to measure the effects of defects and traps on conductivity in our SiNWs when S is found to be above 60 mV/dec [42]. Furthermore, the value of S in Eq. 2.8 should be insensitive to the exact choice of applied bias voltage. If S is found to depend strongly on V_B, then short channel effects (SCEs) are in play, hindering normal FET behavior [1].

For Device C1, our measurement of S from the slope of the curve in Fig. 2.4(c) gives 21.66 V/dec, a significantly larger value than 60 mV/dec. This means that our SiNW FET devices have very high defect and trap densities, greatly reducing gate control and confirming that our FET devices are far from conventional.

As the gate voltage goes beyond V_{TH}, the Fermi level enters the valence band and rapidly introduces holes in the channel. In the linear regime, the gate voltage is now simply "charging" the gate capacitor, giving us a very simple relation between gate-induced charge density p_G and the "overpower" voltage $(V_{TH} - V_G)$ [34].

$$p_G = \frac{C_G(V_{TH} - V_G)}{LeA} \tag{2.9}$$

However, since the gate capacitor does not charge the entire cross-section A of the nanowire (only the bottom section, see section 2.4.1), this equation can only be used to estimate p_G [34]. For Device C1, at overpower voltage 14.1 V (corresponding to the point where g_m was measured), we estimate using Eq. 2.9 that $p_G = 8.2 \times 10^{17}$ cm^{-3}. Using Eq. 2.1, this allows us to quickly estimate that the density of electrons at this state is around a mere $n = 170$ cm^{-3}. As this value is extremely lower than

p, this justifies our assumption in writing Eq. 2.3 that the electron current can be safely ignored in the linear regime. Using Eq. 2.5 and assuming $\mu_{FET} = \mu$, we can also quickly estimate the mean free path of the holes as $l = 1.4$ nm. As this value is significantly lower than L, this also justifies our use of the Fermi gas model to describe the diffusive transport of the hole current.

The gate-induced p_G is only one of the three sources of holes in the SiNW channel. The total hole density p is the sum of the initial density p_o before any gate voltage is applied (corresponding to the original Fermi level position), the hole density introduced by thermalizing traps p_{it} in the subthreshold regime and p_G.

$$p = p_o + p_{it} + p_G \tag{2.10}$$

An estimate for p_o can be found using the intrinsic value n_i for Si and the additional holes from the impurity doping from the SiNW growth process. As p-type doping from gold atoms in Si creates a deep acceptor level near mid-gap, the maximum hole density that can be expected for p_o is around 10^{12} cm^{-3} (the minimum being the intrinsic value 1.18 x 10^{10} cm^{-3}). Further doping will come from surface traps in the subthreshold regime p_{it} (an estimate for this value would be difficult to produce) [43]. In any case, p_G can easily be much larger than the other two, which explains the jump in conductivity seen in the linear regime compared to the subthreshold regime. All three values needed in Eq. 2.10 are estimated, which makes the value of p completely unknown. It must be calculated using Eq. 2.3, which requires a precise measurement

of both σ and μ.

Obtaining accurate values for conductivity and mobility represents the greatest challenge that we had to surpass in this work. Not only were the measurements themselves very difficult (sub-pA currents were often found as we acquired data, creating low signal-to-noise ratios), but the analysis of the data from FET measurements on our SiNWs was greatly complicated due to the various consequences of having them undoped. Some of these obstacles have already been discussed, but the major problem came from the effects of the metal-semiconductor contacts formed when placing our source/drain electrodes on our undoped SiNWs. How we have modified the conventional FET model to account for these issues is the subject of the following section in this chapter.

2.4.3 ON-state and OFF-state

A FET device has three basic modes of operation depending on the value of the gate voltage with respect to the threshold voltage. The "ON-state" is found where V_G surpasses V_{TH} and the device enters the linear regime. This state is characterized by high currents and good gate tunability (useful for applications if the device is used as a sensor). In contrast, the "OFF-state" is found where V_G is not sufficiently high enough to prevent the channel from being mostly depleted of free charge [44]. In this state, the current passing through the FET device is very low (sometimes called the "leak" current) and is almost insensitive to applied gate voltages. The "TH-state" is simply when the FET is operating at $V_G = V_{TH}$. Here the device has an asymmetric

response to gate voltage changes and carries moderate current values.

In order to not simply guess the gate voltages required to operate our SiNW FETs and to give exact values for V_G at ON- and OFF-states, the following convention will be used in this work. The ON-state is defined at the exact overpower voltage required to reach the point where g_m is measured. By going to higher overpower values, transconductance will be lowered and will eventually drop back to near 0 values. The FET device would then leave the linear regime and enter the "saturation" region, which we must avoid in our study. For Device C1 (see Fig. 2.4), the ON-state would be found at V_G = -58.3 V. The OFF-state is defined at the exact reverse overpower voltage point, meaning at the V_G value of the same voltage difference between the ON- and TH-states but on the opposite side of V_{TH}. For Device C1, as V_{TH} was calculated to be -44.2 V, this means that the OFF-state is defined at V_G = -30.1 V.

As the purpose of a transistor in a circuit is to provide an ON/OFF switch by either letting the current pass through it or not, a figure-of-merit for a FET device is the ON/OFF ratio. Labeled simply as "ON/OFF", it is measured by comparing the current in the ON- and OFF-states, I_{ON}/I_{OFF} at a given bias voltage. Equivalently, the device resistance values at the ON- and OFF-states can also measure the ON/OFF ratio, R_{OFF}/R_{ON}. For Device C1, the ON/OFF ratio is found to be 14.9, a modest value.

Naturally, there are two methods to increase the ON/OFF ratio and improve the FET device's overall performance for a given semiconducting channel. The first is to increase the ON-state current by either increasing the bias voltage, increasing

charge density by doping the channel, decreasing the channel length or increasing its diameter. Care must be taken, however, as doing any of these actions may incorporate new issues (e.g. shortening the channel may introduce SCEs) or not change the ON/OFF ratio at all (e.g. increasing the bias voltage may also increase the OFF-state current, doping the channel further may decrease mobility) [45]. The second method to improving ON/OFF ratios is to decrease the OFF-state current. This can be easily be achieved by reducing the effective cross-section carrying current flow (known as "pinching" the channel). As the diameter of the SiNW decreases, this will lead to reducing OFF-state current by removing leak paths often found in Si defect states [46]. This effect will be especially pronounced in our SiNWs with OSFs.

Finally, a device is called a "depletion-mode" FET if the device is in the ON-state without any gate voltages applied ($V_G = 0$). It is called an "enhancement-mode" FET if the device is originally in the OFF-state. As a general rule, enhancement-mode FETs are more often desired for applications, as the device is nominally OFF which reduces the power requirements to operate the transistor [27]. All of the FET devices made from our SiNWs are enhancement-mode FETs.

2.5 Metal-Semiconductor Contact

In order to be able to acquire FET measurements on our devices, metal contacts must be placed on both ends of our SiNWs, both to apply the bias voltage on the source electrode and to measure the current from the drain electrode. We have already

discussed so far in this chapter the hole transport through the semiconducting channel, but we have yet to present the metal-semiconductor contact. Most of the fabrication and measurement challenges found in this work came from the contacts themselves, so an understanding of the transport physics at this interface is equally important.

In this section, we explain how metal-semiconductor contacts modify the energy levels of the holes inside the NW near the interface. As this will also modify charge density in the region near the contacts, these will affect device conduction by creating a new pair of parasitic resistances called the source and drain contact resistances. The section will end by presenting the parameter that best defines the contacts and characterizes their effects, the Schottky barrier.

2.5.1   Charge Injection Mechanism

The metal-semiconductor interface is one of the most challenging problems in device physics [47]. The reason comes from the several complications that arise from the structure around the contact region that makes predictions about the properties of the interface very difficult. These include new states in the semiconductor band gap due to its proximity to the metal interface, the amorphous oxide layer surrounding the NW sandwiched within the contacts, extra impurities adding trap states and surface roughness, just to name a few. It is very difficult and often impossible to fabricate two identical metal-semiconductor contacts, making each FET device unique. Even in seemingly perfectly similar SiNW FET devices (e.g. same channel parameter values for L, d, t_{ox}), different contact properties between the set of devices are the reason

behind the various experimental results obtained from their measurements [33]. It is of paramount importance that the contact effects on FET measurements be understood and removed from data analysis.

A first model for the structure of the contact region could be to study the simple interface between a very large metal (in the bulk state) in perfect electrical connection to a semiconducting NW. As a specific example, we take the gold thin film (assuming bulk Au properties) in contact with our SiNW as the interface of interest. Even if the Au only covers the top section of the SiNW, we define the section of the source/drain electrodes covering the SiNW and the entire nanowire volume under the metal thin film as the contact region of the FET device (see Fig. 2.5(a)).

In addition to the value of the band gap E_g and the Fermi level E_F, an important parameter in a semiconductor's band structure is its electronegativity. Labeled χ, its value is defined as the difference in energy between the vacuum level and the position of the conduction band edge. It represents the minimum energy required to create a free electron by extracting a single electron from the semiconducting material. For Si, $\chi = 4.05$ eV [30].

For the metal, the only parameter needed is its work function. Labeled ϕ, its value is defined as the difference in energy between the vacuum level and the position of the metal's Fermi level. Similarly to χ, the work function represents the minimum energy required to create a free electron by extracting a single electron from the conducting material. For Au, $\phi = 4.3$ eV [21].

Before making an electrical connection, when both materials are separated, the

metal's Fermi level and the semiconductor's Fermi level are not equal, in general. Using $E_g = 1.12$ eV, and using a Fermi level 0.568 eV above the valence band edge, this makes the original position of the Fermi level of our p-type semiconductor to be 4.637 eV from the vacuum level (since $\chi = 4.05$ eV). This value is greater than the metal's work function, $\phi = 4.3$ eV, meaning that the Fermi level of the SiNW is below the Fermi level of the gold electrodes on a band diagram.

Once they are in contact, however, the value of E_F must be the same across the interface in the equilibrium state. Anderson's rule states that both materials must share the same vacuum level, making it possible to compare their Fermi level positions. In order to move the Fermi level, charge will be displaced through the metal-semiconductor interface. Since it is much more difficult to move the Fermi level of a metal in its bulk state than that of a semiconductor, the system will be modified such that the Fermi level of the SiNW is pushed up to match the metal's value for E_F. The higher energy holes in the valence band of the SiNW will be pushed into the metal where a much larger density of lower energy states are available. This will leave uncompensated electrons in the semiconductor, creating pairs of charges across the interface.

This process continues until the Fermi level is uniform in the entire contact region. The charge pairs at the interface will generate a dipole-like electric field in the SiNW, which will "bend" the semiconductor conduction and valence bands over a distance λ. The contact region extends into the SiNW over this length λ, after which the

nanowire's characteristics become the same as those without contact effects (see sections 2.2 - 2.4) in the distance $L - 2\lambda$ between both contacts. As holes were extracted from the semiconductor, a pair of depletion layers are formed in the SiNW of length λ, which will act as rectifiers (which we will discuss further in section 2.6).

The main consequence of band bending is the creation of an energy barrier formed at the metal-semiconductor interface. For holes to be injected into the SiNW from the electrode metal, they must have an energy larger than simply the difference between the metal's Fermi level and the valence band edge. This barrier will prevent current from easily passing through the contact region, acting as a series resistance to the FET device that can also be tuned by both the bias and gate voltages (see Fig. 2.5(b)-(c)).
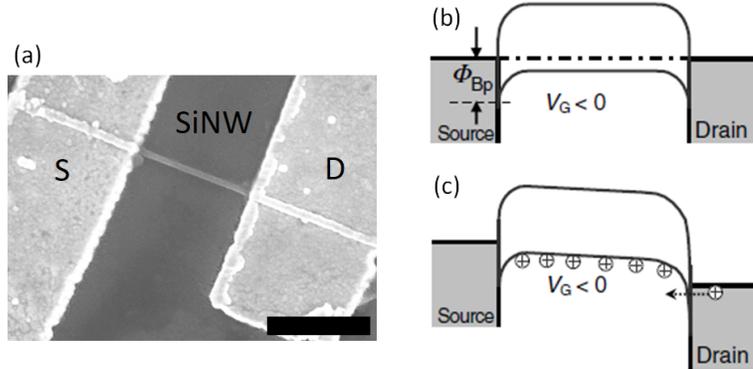
Figure 2.5: Image and band structure of Au-SiNW contact regions. (a) SEM image of SiNW FET device showing a SiNW between two metal contacts (S and D). Scale bar 2 μm. (b)-(c) Band diagrams showing effects of bias voltage on SiNW band bending and hole injection in ON-state. SiNW FET device operating at (b) $V_B = 0$ and (c) $V_B < 0$. Image adapted from [46].

There are two injection mechanisms for holes in the metal to cross the contact barrier and enter the semiconductor channel: thermionic field emission (TFE) and

thermally assisted tunneling (TAT) [48]. For the case of TFE, a hole gains enough

energy from the electric field created by the bias voltage to thermalize over the barrier.

As V_B increases or as the energy barrier decreases, the probability of this scenario

increases. For TAT, holes will tunnel directly through the energy barrier following

the laws of quantum mechanics. Using the WKB approximation and assuming the

energy barrier to be triangular in shape (where the maximum barrier height is found

at the contact interface, decreasing linearly over the length λ), a prediction for the

transmission probability can be obtained (see Fig. 2.6). Under room temperature,

barrier height much larger than $k_B T$ and undoped NW conditions (all of which are

satisfied for our SiNW FETs), the TFE case dominates the injection mechanism and

the TAT case can be ignored [48].
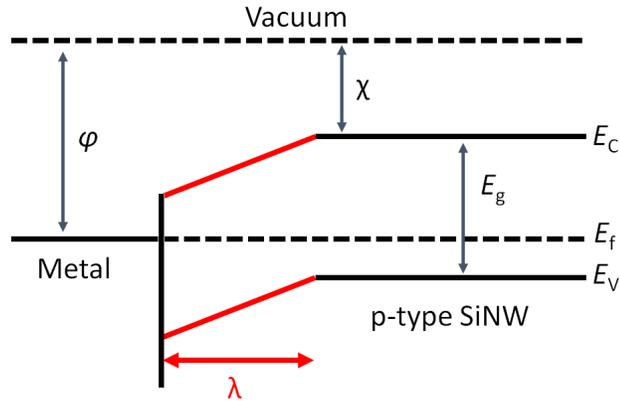
Figure 2.6: Sketch showing how band bending is formed near the contact region. Once the SiNW comes into contact with the metal electrode, the valence E_V and conduction E_C band edges will bend (in red lines) for a distance λ as the Fermi level E_f must be equal everywhere. The injection barrier is modeled as triangular in shape (the true curvature of the barrier is ignored in the sketch, see text). The band gap E_g, electronegativity χ and work function ϕ values are also visualized.

Before proceeding to quantifying the contact effects on FET data, a modification

to our contact structure model must be made. After growth, a thin oxide layer forms on the SiNW surface once exposed to air. This creates a thin insulating layer sandwiched inside the metal-semiconductor interface, which complicates the contact region in several ways.

First, thermally grown oxide is amorphous, creating roughness at the contact interface. Since surface morphology plays a role in determining the barrier, this will create additional traps for holes through the contact that are very challenging to model accurately.

Next, impurity and interface traps created by dangling bonds at the Si/SiO_2 interface will create a high density of hole states within the SiNW band gap. A phenomenon called "Fermi pinning", the oxide layer will effectively "lock" the position of E_F in the contact region at an unknown level in the gap (again, this effect is very challenging to predict). Fermi pinning greatly reduces the ability for the gate to control charge density in the contact region and is especially important in undoped SiNWs [34].

Finally, the insulating nature of the oxide layer will prevent a perfect electrical connection to be formed between the metal and the semiconductor, preventing the necessary band bending to reach the previously discussed equilibrium state. To amend this, a thin oxide layer sandwiched in the contact region can be modeled as an extra depletion layer, modifying the necessary motion of charges at the interface to satisfy the condition that E_F be equal in all three materials. Previously, an important value used to calculate the initial positions of the material's Fermi levels, $\phi - \chi$, was taken

41

as 0.25 eV for the Au/Si interface. A method to account for the oxide layer effects on the contact region is to simply modify this value and proceed through the barrier predictions normally afterwards. For our Au/SiO$_2$/Si structure, this required value for $\phi - \chi$ is taken as 0.82 eV [31].

2.5.2 Contact Resistance Parasitic Effects

With a model for the band structure of the metal-semiconductor interface, we can now make quantitative predictions on the various effects from the contacts on the hole transport in our SiNW FET devices. This will allow us to remove them from our data and focus on what we wish to study, the effects of OSFs on the electronic properties of SiNWs. There are three main contact effects that arise from the presence of the interface energy barrier: effective channel length reduction, parasitic contact resistance and mobility degradation.

As was already discussed, one of the effects of band bending near the contacts is the creation of a pair of depletion layers of length λ near the source and drain electrodes. This reduces the effective channel length to $L - 2\lambda$, creating undesired SCEs (deviations from normal FET behavior) if L is comparable to 2λ. The following equation is used to calculate the value of λ knowing the characteristics of the device structure.

$$\lambda = \sqrt{\frac{\epsilon_{si}}{\beta \epsilon_{ox}} t_{ox} d} = 1.5256 \sqrt{t_{ox} d} \qquad (2.11)$$

Using the values for the permittivity of the SiO$_2$ oxide, 3.9, and the Si channel, 11.8, we can find a value for λ for each individual fabricated FET device. The β parameter in Eq. 2.11 accounts for any non-uniformity in the gate field in the SiNW channel, and is taken as 1.3 in this work [49]. Using typical values $t_{ox} = 300$ nm and $d = 50$ nm, we find that λ will be around 186 nm according to Eq. 2.11. Any SiNW FET device with L less than 0.5 μm will be in serious risk to be hindered by SCEs. To remove the contact effect of effective channel length reduction in our FET data, the value $L - 2\lambda$ will be used instead of simply L in all FET equations.

Another effect of the metal-semiconductor interface is to create an energy barrier that prevents perfect hole injection from the contact to the channel. This can be modeled as a pair of series resistances to the channel resistance called the source and drain contact resistances. The total measured device resistance, $R = V_B/I$, is the sum of these three voltage drop sources.

$$R = R_{ch} + R_{con,s} + R_{con,d} = R_{ch} + R_{con} \qquad (2.12)$$

Since the channel resistance is the value needed to calculate the conductivity of our SiNWs, we must be able to determine $R_{con,s} + R_{con,d}$ and remove it from our measurement of R.

In standard practice, contact resistance values can be extracted using "4-pt measurements". The procedure is straightforward: four electrodes are placed on the

device in question, current is made to pass through two of them and a voltage difference is measured on the other two. This allows the calculation of the channel resistance between the two electrodes measuring the voltage using Ohm's Law. Using geometrical arguments, the channel resistance of the entire channel length is deduced, and contact resistance is calculated using Eq. 2.12.

However, this method is not applicable for our SiNW FET devices. Implicit in the 4-pt measurement method is the assumption that the voltage probe electrodes do not alter the channel's electronic properties. This assumption is incorrect in our case, as any interface between metal and our SiNW will create a depletion layer within the channel. The 4-pt measurement setup also assumes that the voltmeter input impedance is very large compared to R_{ch}, but this is also not true in our case as the measured values for the channel resistance of our SiNWs are often well over 10 GΩ [50].

Another approach is needed in our case to extract contact resistance on our SiNW FET devices. Even if the measured resistance from our data is the device resistance, it is still possible, under certain conditions, to be able to differentiate between the channel and the contact contributions to R. There are two types of contacts the metal-semiconductor interface creates.

The first type are called "Ohmic contacts". If the contact energy barrier is very low compared to $k_B T$ and thin (e.g. semiconductor is p-type doped in the contact region), then hole injection will be easy [51]. The current through the barrier will be proportional to the bias voltage, and this linear behavior will make the contact

resistance obey its own version of Ohm's Law [43]. The contact region will take a small voltage drop (most of V_B will be used in the channel), which means that R_{con} will be much smaller than R_{ch}. If device resistance R also has a linear behavior, the exact value of R_{con} will not be known, but it is possible to ignore it completely and simply claim that $R = R_{ch}$ [33].

The second type, and the one mostly found in our SiNW FET devices, are called "Schottky contacts". The conditions for Ohmic contacts are rarely satisfied in undoped nanowires [33]. Usually, the contact energy barrier is much higher than $k_B T$, and our undoped SiNWs cannot offer the necessary band bending to create thin barriers. In this case, hole injection will be difficult and contact resistance will not follow a simple linear behavior. Since the channel resistance will continue to obey a linear relationship between bias voltage and current, most of the non-linear behavior in device resistance R will be attributed to R_{con} [33, 43]. Under these conditions, the contact energy barrier is called a Schottky barrier (SB). How to model the SB will be discussed further in section 2.5.3.

This non-linearity in the FET device behavior can be exploited to extract the channel and contact resistances. In the case where the bias voltage is much smaller than the SB, the current passing through the FET device is contact-limited [32]. The current's response to a changing V_B value will be highly non-linear, making the data difficult to model and analyze. Worst, the FET device will certainly not be in its linear regime (regardless of V_G), making all FET parameter calculations discussed so far incorrect in this regime.

In the case of high bias voltage, however, the current passing through the FET device is channel-limited [32]. The device's response will become linear once more, meaning that the contacts will no longer affect FET behavior and it will again be possible to study the electrical properties of our SiNWs [33].

As V_B increases, the SB will thin, facilitating current flow. Most of the voltage drop will occur in the channel in this case (this is especially true when the FET device is in its ON-state) [46]. The differential conductance $\mathrm{d}I/\mathrm{d}V_B$ in the high bias voltage linear regime can now be claimed to be equal to G_{ch}, which becomes a measurement of channel resistance [32, 33]. Using Eq. 2.12, it is now possible to obtain R_{con} from R, making it possible to calculate the correct values for the conductivity of our SiNWs from our data.

Before moving on, we will define contact resistivity as it will be needed later. Labeled ρ_{con}, it is defined as the product of the contact resistance and the contact area A_{con}.

$$\rho_{con} = R_{con}A_{con} = R_{con}\pi dL_{con}/2 \tag{2.13}$$

In our model, we will assume that the Au thin film placed over our SiNW to create the contact is electrically connected to only the top half of the nanowire. The contact area used in Eq. 2.13 is then the product of half the nanowire circumference and the length of the SiNW covered by the Au, L_{con} [50].

The final contact effect to consider is mobility degradation. Due to Fermi pinning

near the contact region, the gate electrode does not have a perfect control over the channel conduction. This creates a reduction in observed device mobility, as transconductance has been affected by the contacts themselves [1]. The following equation is used to modify the measurement of g_m to the correct value g_{mi} (the intrinsic channel transconductance) knowing the channel and contact resistance values.

$$g_{mi} = \frac{g_m(1 + R_{con}/R_{ch})}{1 - g_m R_{con}} \qquad (2.14)$$

Accurate measurements of mobility are only possible once contact effects are removed, so it is this g_{mi} value in Eq. 2.14 that must be used in Eq. 2.7 [38]. In undoped SiNWs, mobility degradation is especially important, as R_{con} can be significant. Only in the linear regime and with FET data removed of contact effects is the FET mobility Eq. 2.7 equal to the Fermi gas mobility Eq. 2.3 [34].

2.5.3   Schottky Barrier

The most important single parameter to describe the metal-semiconductor interface's effect on FET device transport data is the height of the contact energy barrier. Called the Schottky barrier height and labeled ϕ_{SB}, it represents the energy barrier that must be crossed in order to inject current from the contact electrode to the channel. At room temperature, any SB with ϕ_{SB} greater than 25 meV will create Schottky contacts.

All metals form SBs with Si, so it will be no surprise to find Schottky contacts

on almost all of our fabricated SiNW FET devices. Great enhancement-mode FETs with Schottky contacts can easily be created with undoped SiNWs, as most SCEs are suppressed, the ON/OFF ratio can be good since the SBs will greatly reduce OFF-state currents, and the fab process is simple as no additional doping or annealing is required [46].

As was mentioned in section 2.5.1, the SB is created by band bending near the metal-semiconductor interface due to the necessity for E_F to be equal across the contact region. To simplify the model for our SBs, we will assume the energy barrier to be triangular in shape, where the maximum barrier height ϕ_{SB} is found at the contact interface, decreasing linearly over the length λ [49]. Mott's relationship predicts that the value of ϕ_{SB} for hole injection can be estimated by the difference between the semiconductor band gap and the $\phi - \chi$ shift value.

$$\phi_{SB} = E_g - (\phi - \chi) \tag{2.15}$$

Using $E_g = 1.12$ eV and $\phi - \chi = 0.82$ eV (the value for our Au/SiO$_2$/Si contact structure), we can estimate $\phi_{SB} = 0.335$ eV according to Eq. 2.15. Unfortunately, the exact value for ϕ_{SB} will not match the value predicted by Mott's relationship since the position of the Fermi level near the contact region is unknown due to Fermi pinning (caused by complex surface states "locking" E_F at the interface).

This means that the barrier height must be measured using our FET data and cannot be pre-determined [33]. Furthermore, the barrier width can also be tuned by

the gate, as higher currents in the ON-state compared to the OFF-state will be due to thinner SBs [48]. On a given SB, smaller values for λ will give better gate control over the values of ϕ_{SB} [49].

If the value of ϕ_{SB} is above the one predicted by Eq. 2.15, then a considerable amount of contact effects are present in the device in question due to strong Fermi pinning. Since this will be the case in this work, we will hereafter call our SiNW devices "SB-FETs". The electronic properties of a SB-FET differ from the ideal FET situation, meaning that we need to further modify the transport model to accurately predict the acquired data from our SiNWs.

First, for a SB-FET device, gate control comes mostly from modifications of the SB itself, with channel mobility playing a very small role. Even if there are several carriers in the channel, the current can still be effectively blocked by the SB [52]. The gate electrode is then mainly used to tune R_{con}, as the channel properties are not greatly affected by V_G. Second, the gate field around the contact region is responsible for tuning ϕ_{SB} and λ, meaning the precise structure of the metal-semiconductor interface plays a large role in determining R_{con}. The contact geometry and surface roughness are important parameters in controlling our SiNW SB-FET performance [52]. Despite their deviations from ideal FET behavior, the study of SiNW SB-FETs is promising as these devices will operate well even in small dimensions [52].

As the SB is a contact effect, the calculation of ϕ_{SB} first requires the measurement of R_{con} (see section 2.5.2) and depends on the contact area A_{con} [35]. Then, using Eq. 2.13 to calculate contact resistivity, the values of ϕ_{SB} for our SiNW SB-FET can

be determined using the following equation [51].

$$\rho_{con} = \frac{k_B}{eTA^*} \exp(\phi_{SB}/k_BT) \qquad (2.16)$$

The constant $A^* = 4.68$ x 10^5 A/m^{2}K^2 found in Eq. 2.16 is called the "Richardson constant" [33].

For large values of ϕ_{SB} (exceeding 0.6 eV), the SB-FET response to bias voltage can be highly non-linear with current being almost non-existent for V_B below a certain value called the cut-off voltage (we will discuss this effect further in the next section). In the case where one contact electrode has a SB much larger than the other (e.g. $R_{con,s} >> R_{con,d}$), the SB-FET device will have a rectifying behavior, allowing current to pass in one direction much more easily than the other. These rectifying SB-FETs have very high contact resistance values in undoped SiNWs, often surpassing the value for R_{ch} [51].

2.6   Rectifying Behavior

Caused by significant band bending at the metal-semiconductor interface in undoped SiNWs, Schottky contacts with large ϕ_{SB} values are characterized by high contact resistance [51]. As was mentioned in previous sections, our SiNW channel, located between two contact electrodes, will be greatly affected by the presence of the source and drain SBs via the formation of a pair of depletion layers (see Fig. 2.5(b)). The

energy barriers in the contact region will hinder hole injection and will create a non-linear response on the current passing through the SiNW SB-FET. Any asymmetry between the two contacts will also generate an asymmetry in the SB-FET data. In the case of large contact asymmetry, the SB-FET will obtain a rectifying behavior. As the device design does not require doping, more applications in technology are available for our SB-FETs to be used as diode elements in nano-circuitry [51].

In this last section, we will present the theoretical background necessary to understand the physics behind the rectifying behavior of Schottky contacts. First, we will characterize the depletion layer and the various structures that can generate one. Next, the method to extract contact asymmetry from our SiNW SB-FET output data will be shown. Then, the extreme case of large SB asymmetry and how this creates a rectifying device will be discussed. The chapter will end on our prediction that rectifying SB-FET devices fabricated using SiNWs with OSFs will be ideal to study the Hex-Si/Cub-Si band structure and electronic properties.

2.6.1   Depletion Layer

In order to satisfy the requirement that the Fermi level be equal on both sides of an interface between two materials, band bending will cause a re-distribution of charge density in the vicinity of the interface. In a semiconductor, this charge movement leaves behind a region called the depletion layer of thickness λ, the length scale where potential variations are screened [49]. At a distance from the interface beyond λ, the material is identical to its initial state before the electrical connection with the other

material was established (contact perturbations and band bending are not present).

To illustrate the conditions for the formation of a depletion layer, we will use the familiar p-n junction as an example. The depletion layer at the p-n junction acts as an asymmetric energy barrier, affecting current differently depending on its direction. For positive bias voltage values applied on the p-type side, additional holes are provided to the p-type material, which will shrink the depletion layer as less volume is necessary before the charge equilibrium condition is met, reducing band bending. Called the "forward-bias" mode, current can easily pass through the p-n junction and increases exponentially with V_B. For negative bias voltage values applied on the p-type side, however, holes in the p-type material are extracted from the interface, which will enlarge the depletion layer as more volume is necessary before the charge equilibrium condition is met, increasing band bending. Called the "reverse-bias" mode, the energy barrier becomes larger and prohibits normal current flow from crossing the p-n junction. An electronic device having this rectifying behavior is simply called a rectifier. The response of the current density passing through the p-n junction as bias voltage is modified is given by Eq. 2.17.

$$J_{id} = A^* T^2 \exp(eV_B / k_B T - 1) \tag{2.17}$$

For a metal-semiconductor interface, we have already discussed (see section 2.5.1) how the charge density gradient around the contact region causes a depletion layer to form on the semiconductor. The contact between the metal electrode and the

undoped SiNW also generates non-linear effects similar to a p-n junction. Called "Schottky diodes", an equation for current density through them can also be written by adding the presence of the SB height to Eq. 2.17 as an injection energy barrier according to TFE theory [4, 51].

$$J_{sd} = A^* T^2 \exp[(eV_B/\eta - \phi_{SB})/k_B T - 1]$$
(2.18)

The η parameter in Eq. 2.18 represents how the Schottky diode's characteristics might deviate from the ideal case ($\eta = 1$). The forward-bias mode, where current increases rapidly, might not begin exactly at $V_B = \phi_{SB}/e$, as parasitic series resistance sources (e.g. surface charge traps, oxide layers, structural roughness preventing perfect electrical connection) will also take some of the voltage drop across the Schottky diode.

The effect of bias voltage on depletion layer thickness can be summarized by the following equation [21].

$$\lambda_B = \lambda \sqrt{1 - \frac{eV_B}{\eta \phi_{SB}}}$$
(2.19)

In Eq. 2.19, λ is the size of the depletion layer with $V_B = 0$ given by Eq. 2.11. Positive bias shrinks the layer, allowing current to flow, while negative bias increases the band bending length, which illustrates the rectifying behavior of our SB-FET contacts.

For a "p$^+$-p junction", two p-type semiconductors in contact with each other will

also create diode-like behavior. The hole density gradient $p^+ > p$ will also create a

small depletion layer to balance charge as the Fermi levels are moved in alignment.

The forward-bias mode occurs when positive bias is applied to the p^+ side, and the

opposite voltage sign for reverse-bias mode. The difference in valence band edge levels

between the two sides of the interface caused by band bending can be predicted by

the following equation [30].

$$\Delta E_V = k_B T \ln \left(\frac{p^+}{p} \right) \tag{2.20}$$

This effect will play a role in our SB-FET devices made from SiNWs with OSFs.

Since the Hex-Si/Cub-Si interface does not share the same band structure (see section

2.1.2), the region near the OSFs will create small depletion layers via hole density

gradients according to Eq. 2.20. These are predicted to increase the SB-FET channel

resistance and effectively generate hole trap states at the Hex-Si/Cub-Si interface, as

E_F must be equal across the nanowire cross-section.

2.6.2 Contact Asymmetry

We will now present the methods used in this work to extract the various parameters

relating to the Schottky contacts such as contact resistance R_{con}, Schottky barrier

height ϕ_{SB}, and the "non-ideal factor" η. The asymmetry found in our SiNW SB-FET

data will give us the necessary tools to calculate contact asymmetry and quantitatively

define the rectifying behavior. This experimental evidence will allow us to make

various claims on how the Hex-Si/Cub-Si crystal structure affects electronic transport in SiNWs with OSFs.

As our first example, we use "Device C1" (see section 4.1 for full device list) to illustrate our analysis of how the bias voltage affects the current passing through a SiNW SB-FET device. This particular device has a Cub-Si only (no OSFs are present) SiNW of diameter $d = 50$ nm forming a $L = 2$ μm channel between two contact electrodes, all of which resting on a $t_{ox} = 300$ nm oxide layer forming the back-gate dielectric.

Fig. 2.7(a) shows a graph of the measured current exiting the drain electrode at fixed gate voltages as the bias voltage is modified. An I-V curve plotted under these conditions is called an output curve. In the examples shown in this section, the selected values of V_G are those corresponding to the SB-FET devices' ON-state (see section 2.4.3).
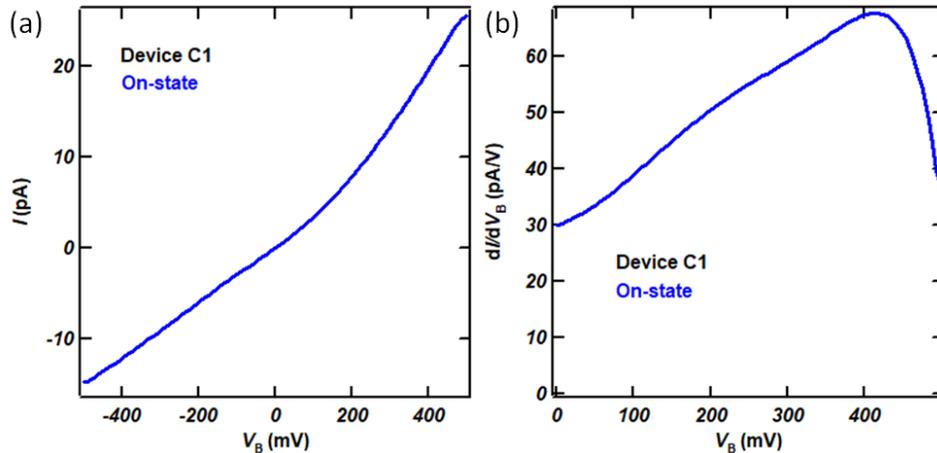
Figure 2.7: Output characteristics of Device C1 (see text) to demonstrate data analysis methods. All curves shown are taken at $V_G = $ -55 V (ON-state). (a) Output curve showing the bias voltage controlling the device current with a slight asymmetric behavior. (b) $\mathrm{d}I/\mathrm{d}V_B$ curve used to identify G_{ch}.

Immediately, we notice that Device C1 acts very similar to a simple resistor following Ohm's Law in its ON-state (V_G = -55 V). However, a slight asymmetric response to bias is found, as the current at V_B = 0.5 V (around 25 pA) is not equal to the current at V_B = -0.5 V (around -15 pA).

To determine the channel resistance, we first calculate and plot the differential dI/dV_B. As shown in Fig. 2.7(b), the slope of the output curve of Device C1 rises steadily from 29.89 pA/V at 0 V to 67.57 pA/V at 0.414 V only to decrease again afterwards (we use the positive bias side as an example, the analysis for the negative bias side is identical). In the case of a perfect resistor, the value of dI/dV_B would be constant and equal to the channel resistance. The deviation from a perfect linear behavior seen in the data is due to contact effects.

The maximum value of dI/dV_B at a given gate voltage is of special importance to characterize a SB-FET device. As mentioned before (see section 2.5.2), this value can be claimed to be equal to G_{ch}, which becomes a measurement of channel resistance $R_{ch} = 1/G_{ch}$. Using Eq. 2.12, we obtain R_{con} from R, making it possible to calculate the correct values for the conductivity of our SiNWs. For Device C1, we find that G_{ch} = 67.57 pA/V at 0.414 V, which gives R_{ch} = 14.8 GΩ. Since the current at 0.414 V is 20.56 pA, R = 20.13 GΩ and R_{con} = 5.33 GΩ. Notice that contact resistance represents about a quarter of the device resistance, confirming that contact effects cannot be neglected in SB-FET devices.

In a SB-FET device, the SiNW channel is sandwiched between two contact SBs

with opposite band bending orientations. At high bias voltage values, the modifications to the width of the source and drain depletion layers will be different (one will increase while the other will decrease) depending on the sign of V_B [51]. We can use this asymmetrical response to both contact SBs to discriminate between the contact resistance from the source electrode $R_{con,s}$ and from the drain $R_{con,d}$. At a given bias voltage sign, one of the Schottky contacts is in reverse-bias mode while the other is in forward-bias mode. Since the forward-bias barrier takes almost none of the voltage drop, most of the measured contact resistance is from the reverse-bias barrier, meaning that only one of the SBs are affecting our SB-FET data at a given bias voltage [32].

At large positive values for V_B, the source contact depletion layer is responsible for any non-linear behavior found on the output curve. We assume here that the measured R_{con} is equal to $R_{con,s}$, as the drain contact SB is in forward-bias mode. At large negative values for V_B, the measurement gives $R_{con,d}$.

Having obtained all three values for R_{ch}, $R_{con,s}$ and $R_{con,d}$ in our SiNW SB-FET device from the output data, we can now calculate the conductivity σ of the channel (our SiNW). Using Eqs. 2.13 and 2.16 with the appropriate source and drain parameters, the values of both $\phi_{SB,s}$ and $\phi_{SB,d}$ can be found. For Device C1, using the values already presented and ignoring other contact effects for the moment (i.e. effective channel length reduction and mobility degradation), we find $\sigma = 0.325$ mS/cm and $\phi_{SB,s} = 0.497$ eV.

As our second example, we use "Device H1" (see section 4.1 for full device list)

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to illustrate our analysis of how the bias voltage affects the current passing through a SiNW with OSFs. This particular SB-FET device has a Hex-Si/Cub-Si structure SiNW of diameter $d = 57$ nm forming a $L = 2$ μm channel between two contact electrodes, all of which resting on a $t_{ox} = 300$ nm oxide layer forming the back-gate dielectric. The ON-state of Device H1 is found at the gate voltage value of -80 V.
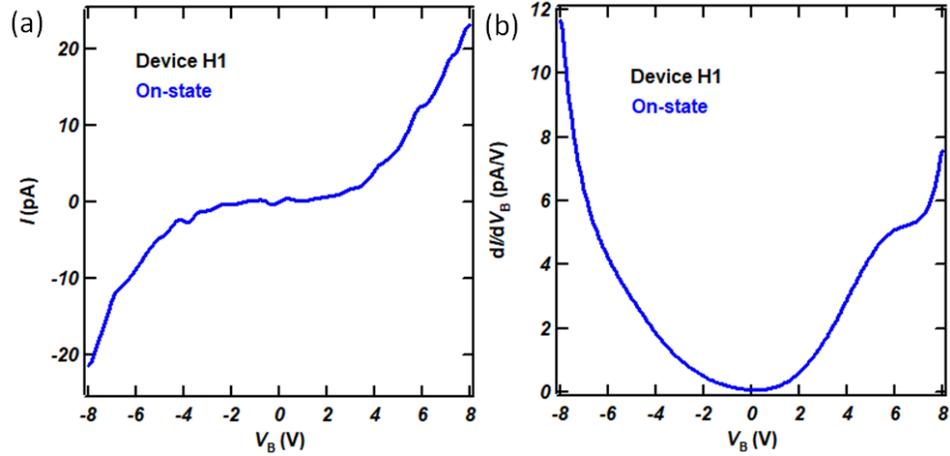
Figure 2.8: Output characteristics of Device H1 (see text) to demonstrate data analysis methods. All curves shown are taken at $V_G = $ -80 V (ON-state). (a) Output curve showing the bias voltage controlling the device current with high non-linear behavior. (b) dI/dV_B curve used to identify both G_{ch} values.

For this device, we immediately notice in Fig. 2.8(a) that the non-linear contact effects are much more apparent. As shown in Fig. 2.8(b), the maxima for dI/dV_B are found to be 11.67 pA/V at -8 V and 7.56 pA/V at 8 V (we are limited by the data available in the measured bias window), when the currents passing in the SB-FET are respectively -22.2 pA and 23.6 pA. For example, on the positive bias side, we calculate $R_{ch} = 85.7$ GΩ at $R = 360.7$ GΩ, meaning that $R_{con,s} = 275$ GΩ. Notice that contact resistance represents about three-quarters of the device resistance, confirming that contact effects cannot be neglected in SB-FET devices fabricated from SiNWs with

OSFs. Using all appropriate equations, we find $\phi_{SB,s} = 0.592$ eV and $\phi_{SB,d} = 0.627$ eV.

As can be seen in Fig. 2.8(a), the output curve for a highly non-linear SB-FET device has very little conductance near 0 V. Due to the very high values for $\phi_{SB,s}$ and $\phi_{SB,d}$, the SBs can effectively prohibit any current from flowing through the channel in the low bias voltage range called the "barrier regime". In the high bias voltage range, the energy barriers can be surpassed and the device enters the linear regime (where our transport model is applicable).

The voltage separating the contact-limited regime and the channel-limited regime is called the cut-off voltage V_{co}. An important signature of the presence of Schottky contacts, the cut-off voltage represents the bias voltage required to transition between the barrier and linear regime of the SB-FET device. Visually, V_{co} can be seen on an output curve at the onset of significant current flow on the V_B axis.

In order to extract a value for V_{co}, the most widely used method is to take a linear extrapolation at the point on the output curve where G_{ch} was found and calculate the point that intersects the bias voltage axis (where current equals 0). This method is similar to the one used to find the threshold voltage of the device. For Device H1, the intersects are calculated to give $V_{co,s} = 4.88$ V and $V_{co,d} = $-6.1 V.

In general, higher values for V_{co} represent a more significant SB, although the oxide layer in the contact region also contributes to the exact value [32]. Using Eq. 2.18, the cut-off voltage can be identified as the voltage necessary to switch the Schottky diode to its forward-bias mode, allowing us to write the following relationship between V_{co}

and ϕ_{SB}.

$$|V_{co}| = \eta \phi_{SB}/e \qquad (2.21)$$

Once V_{co} and ϕ_{SB} are determined, Eq. 2.21 is used to calculate the non-ideal factor η. This parameter gives us a quantitative interpretation of the quality of the metal-SiNW electrical contact and insight on how the structure of the contact region affects hole injection. In the ideal case, $\eta = 1$. For Device H1, $\eta_s = 8.24$ and $\eta_d = 9.74$, meaning that the source electrode makes a slightly better contact with the SiNW than the drain (this can also be seen in the output curve, as the current at positive bias is slightly larger than at negative bias).

This contact asymmetry is the primary factor that determines the shape of the output curve [33]. Symmetrical outputs are only found in SB-FET devices when both contacts are precisely identical, which is experimentally very difficult to accomplish [32]. As the contact region is very sensitive to small variations in charge density (R_{con} increases exponentially with decreasing p), devices fabricated with undoped nanowires are almost always characterized by asymmetric outputs [33, 43].

To quantify contact asymmetry, we define the asymmetry ratio, labeled δ, as the ratio of the SB heights. As a choice for a sign convention in this work, we take positive values for δ meaning that the device has higher conductance values for positive V_B values.

$$\delta = \frac{\phi_{SB,d}}{\phi_{SB,s}} \tag{2.22}$$

For very large δ values calculated with Eq. 2.22, the SB-FET device will act as a Schottky diode and exhibit a strong rectifying behavior. We define the rectifying ratio, labeled r, as the ratio of the forward-bias and reverse-bias mode currents at equal (but opposite sign) bias voltages when operating at a given gate voltage. As a choice for a sign convention in this work, we take positive values for r meaning that the device is in forward-bias mode for positive V_B values.

$$r = \frac{I_s}{|I_d|} \tag{2.23}$$

It is customary to call a SB-FET device a rectifying device (or simply a rectifier) when the absolute value of r calculated with Eq. 2.23 is at least 10.

The analysis of the SB-FET data (in both transfer and output curves) allows us to gather a large amount of information on the electronic properties of our SiNWs. By looking at how these calculated parameters vary with OSF density, it will be possible to study the effects of crystal structure on charge transport.

Chapter 3

Fabrication of Hexagonal-Core

SiNW SB-FETs

We describe the fabrication, Raman spectroscopy, and charge conductivity measurements used to verify the effects of ordered stacking fault defects in silicon nanowires (SiNWs). It is a challenging fabrication process, as there are numerous steps that are either low-yield or low-throughput.

The sections of this chapter are presented in chronological order during the fabrication procedure (sometimes called simply "fab"). This allows the reader to use this chapter as a manual to replicate our sample preparation and characterization in the future. From start to finish, completing all of these steps on a new batch of samples typically takes a highly experienced researcher one full week of work.

The first section deals with the steps needed to clean the substrates and grow the silicon nanowires. Next, in section 3.2, we will explain how Raman spectroscopy

can be used to quantify ordered stacking fault density in silicon nanowires. Section 3.3 describes the standard micro-fabrication methods used to place electrodes on the nanowires. Finally, section 3.4 shows how the SiNW SB-FETs are studied in our lab's custom electronic measurement setup. The presentation and discussion of our scientific results will be left for the following chapter.

3.1   Substrate Cleaning and Coordinate Grid Fab

In this section, we will present the simple methods needed to clean the substrates adequately and the procedure used by the Moutanabbir Group in order to grow our SiNWs.

3.1.1   Wafer Cleaning and Etching

To function properly, and to remove as many confounding factors as possible, our silicon nanowire devices must be fabricated on a clean substrate (e.g. a surface without any carbon residues).

We begin by selecting a heavily n-doped (typically by antimony incorporation) 4-inch <100> silicon wafer. These low-cost wafers are purchased having a 300 nm silicon oxide (SiO_2) layer grown on both sides. This choice of standard wafer will satisfy the requirements that our SB-FET devices must be fabricated over a dielectric thin-film coating a conducting substrate (see section 2.4.1).

The first step is to expose a surface of the highly conductive silicon by removing

the oxide layer on only one side of the wafer. The technique used to expose the n-type Si side of our wafers is by a dry etching procedure called Reactive Ion Etching (RIE). A wet etch technique (e.g. BOE) would incorrectly remove both oxide layers on both sides of the wafer.

The sample is placed inside a vacuumed chamber, then a specific set of gases are chosen to fill the chamber at a certain flow rate and pressure. The selection of gases corresponds to the task we wish to perform. A flow of fluoroform (CHF_3) with a small flow of oxygen (O_2) is used to easily etch SiO_2 [53, 54]. A large flow of oxygen is used to clean a surface from organic residues and impurities. A mixture of oxygen and argon (Ar) cleans the chamber itself to clear it from contaminants from previous use.

Once the desired chamber pressure is reached and the gas flow rates are stable, the gas is ionized using a RF power source. This creates a plasma inside the chamber that will etch away the desired targeted material. After SiO_2 removal, the exact value of the oxide thickness (the t_{ox} parameter needed for our transport model equations, see section 2.4.1) on the other side of the wafer is measured with a reflectometer.

Since the oxide thin film surface will be used to fabricate the SiNW SB-FET devices, an additional pure oxygen RIE treatment is done on this surface to remove any organic residues. This treatment can be repeated anytime the sample is found to be in need of cleaning from any residues left over from a step during fab.

Below is a table showing the two optimized RIE "recipes" used in this work for the various etching procedures. Preliminary tests were done to obtain the values shown

64

in Table 3.1 by etching various oxide thicknesses from silicon chips.

Table 3.1: RIE Treatment Recipes Used in this Work

Treatment	Materials Etched	Gas Flow	Chamber Pressure	RF Power	Etch Time
Oxide Removal	SiO_2	0.5 sccm O_2 4.5 sccm CHF_3	125 mTorr	300 W	20 min
Surface Cleaning	Organics, fab residues	20 sccm O_2	200 mTorr	300 W	5 min

3.1.2 Grid Pattern and Photolithography

As a clean surface is barren and relatively devoid of landmarks, it would be very difficult to know the location of any given point on the sample under a microscope. To solve this problem, we wish to prepare a grid pattern on the wafer using permanent markings. It would then be possible to make note of the exact location of a nanowire on our samples with micron scale precision.

The grid pattern will be made from patterned gold thin films over the oxide surface. The pattern is prepared using standard photolithography methods. This common tool in micro-fabrication uses a photosensitive thin film (called the "negative resist" layer) to transfer a pattern from a previously designed metallic mask onto a surface using radiation from a UV lamp.

The photolithography process is performed at the Polytechnique Montréal clean room using their "MA6" equipment. The mask, a reflective plate with the desired grid pattern design prepared by previous group members, is loaded into the equipment [54]. The grid pattern is drawn on a 5 x 5 mm surface, so alignment is made to

maximize the number of 5 x 5 mm chips patterns that can possibly be placed on each 4-inch wafer (see Fig. 3.1).

Once alignment is complete, the UV lamp exposes the mask from above for a fixed amount of time depending on the current lamp intensity (measured at each session with a powermeter). To finish the photolithography process, the sample is dipped in a developer.
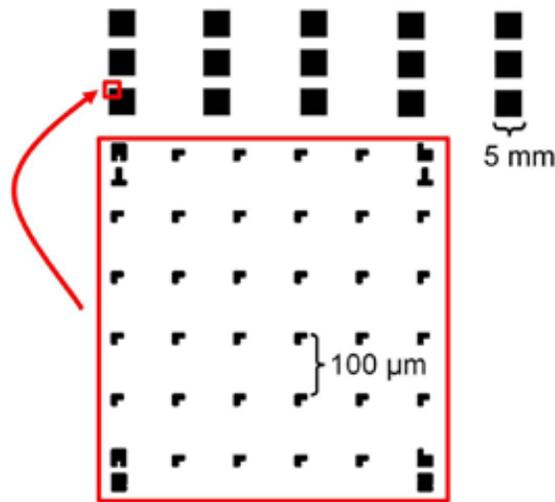
Figure 3.1: Photolithography grid layout mask containing 15 sets of 5 x 5 mm chip patterns. Inset shows the letters, numbers and grid marks dividing the surface in 100 x 100 μm framed spaces. Image from Champagne Group archives [53].

At this point, we wish to make the negative image of the grid pattern on the resist layer become a permanent positive image with a metallic thin film on the oxide layer. The procedure to place metal thin films by physical vapor deposition follows very basic principles and only simple equipment is required. The sample and metal sources are placed under UHV conditions inside the bell jar using a diffusion pump. A power source is used to evaporate the metal source (either by direct Joule heating

of the element, or with an electron beam), and the metal vapor deposits directly on the sample placed above the source on a stage pointing downward.

In the case of creating our grid patterns, we deposit 3 nm of Cr to form a stacking layer (this helps adhesion of the thin film to the oxide layer), then 80 nm of Au over the resist film. Metal thin film thickness was measured with a calibrated piezoelectric crystal monitor found inside the UHV system.

After deposition, the sample is dipped in 60°C acetone for an extended period of time (usually a few minutes) to dissolve the resist. The portion of the metal thin film resting on top of the resist will peel off during this process (called "lift-off"), leaving behind a metal thin film on the oxide layer matching the desired pattern made on the resist.
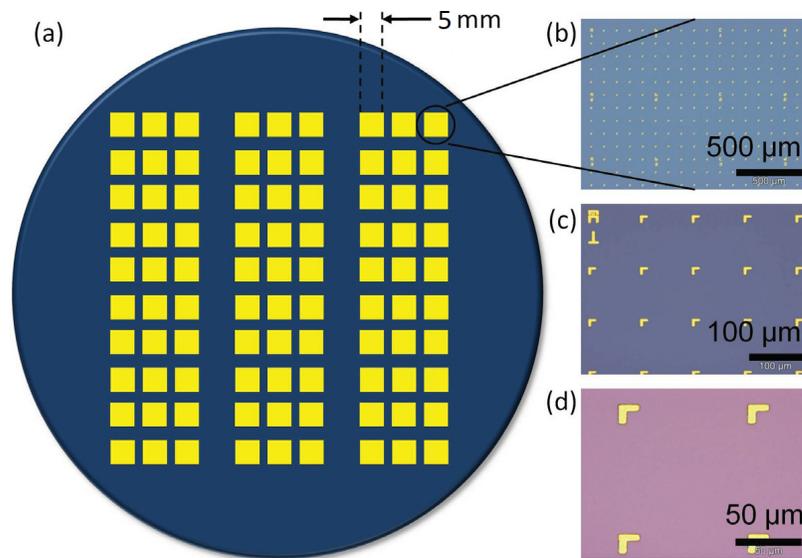
Figure 3.2: Surface location grid pattern. (a) Sketch showing the 90 sets of 5 x 5 mm chip patterns placed on a 4-inch wafer by photolithography and thin film metal deposition. (b)-(d) Optical images in various scales showing the letters, numbers and grid marks dividing the surface in 100 x 100 μm framed spaces. Image from Champagne Group archives [54].

The wafer is now diced using a diamond-tip pen into several 6 x 6 mm "chips". Around 90 chips are made on each 4-inch wafer (see Fig. 3.2(a)), each containing the 5 x 5 mm grid pattern (see Fig. 3.2(b)-(d)). If surface contamination is deemed too high after lift-off on certain chips, a RIE treatment to remove fab residues is performed, as a clean surface is needed for the following steps.

3.1.3   Silicon Nanowire (SiNW) VLS Growth

Here we will discuss the method in which our silicon nanowires (SiNWs) were grown. We repeat that the nanowires were not grown by myself, but was the result of the work done by Dr. Uri Givan, a former post-doctoral researcher in the Moutanabbir Group, at the Max Planck Institute in Germany. As we use these nanowires to obtain our results, however, we will present the procedure to grow them, and how the ordered stacking faults were introduced in the silicon crystal.

The silicon nanowires were prepared using the "vapor-liquid-solid" (VLS) growth method, a procedure developed at Bell Laboratories and a standard in the nano-fabrication industry [55, 56, 57]. The details vary depending on the exact desired semiconductor structure, but the basic principle remains the same. We present below the procedure followed to grow our SiNWs.

First, a 1 nm Au thin film is deposited on a 4-inch Si wafer. The crystal orientation of the grown nanowires will match the orientation of the substrate (in our case, <111>) [1]. The wafer is annealed for roughly 1 hour to form Au nanodroplets. The diameter of the droplet (called the "catalyst") determines the NW diameter (typically

around 50 nm for our nanowires).

Next, under UHV conditions, a flow of ultra-high purity silane (SiH_4) gas (called the "precursor") is introduced in the chamber. For reasons that were more relevant to other projects, the precursor for the growth was also isotopically pure to grow silicon nanowires having an exact isotopic composition, either made entirely of Si-29 or a mix of Si-28 and Si-30 [58]. Under the appropriate temperature and pressure conditions, the gas will react at the surface of the catalyst, causing the Si atoms to dissolve inside the Au nanodroplets (the $2H_2$ gas is pumped out of the chamber). This process continues until the Si concentration in the droplets is above the eutectic composition point of the Si-Au mixture.

Similar to how a super-saturated salt solution will spontaneously crystallize on the bottom of the container once the liquids conditions change, the Si atoms will also form a crystal under the Au droplet by expelling the excess equilibrium atoms [1]. The process continues until the conditions in the chamber prevent the Si-Au mixture to maintain itself in the super-saturated regime. This forms a multitude (millions if the process was successful) of vertical SiNWs on the wafer. The length of the nanowires is determined by the amounts of Au and Si available for the process and the time allotted during growth conditions (typically, 30 minutes correspond to roughly 10 μm NW length).

Since some of the Au is deposited in the SiNW during crystal formation, the nanowires will behave as lightly (unintentionally) doped p-type semiconductors [43]. The Fermi level of the material will be very close to the center of the gap at room

temperature, as Au forms a deep acceptor impurity level in the Si band structure. Exactly how dopants are incorporated during VLS growth is not typically well understood [59].

The Si crystal will be typically grown in the familiar cubic (3C) phase silicon lattice. However, by changing the growth conditions, the Si atoms can be arranged in a different pattern during crystallization. By modulating the pressure, gas flow rate and temperature of the chamber during the growth time, it is possible to make it thermodynamically more favorable to create new phases of Si crystals within the nanowire.

Under the conditions which generate an acceleration in the growth rate, the crystallization process will make "mistakes", causing some Si atoms to not be able to find their "correct" position of minimum energy inside the crystal. If this is repeated in each layer, stacking faults (planes of missing Si atoms in the cubic structure) will be embedded in the nanowire (see Fig. 3.3(a)) [60]. If these faults are ordered, this will introduce new Si crystal phases (see section 2.1.1), such as rhombohedral (9R) or hexagonal (2H), embedded in the cubic crystal (see Fig. 3.3(b)-(c)) [14].

At the point where ordered stacking faults (OSFs) are introduced in the nanowire during growth, the SiNW will sometimes kink (especially for high OSF density), changing growth direction from the original <111> to <112> [43, 61]. This is to relax the stress added to the system by the interface between the cubic and hexagonal phases. If a kinked SiNW is found in our samples, it is often shown that one side of the kink is a purely cubic Si crystal, while the other side shows the presence of OSFs.
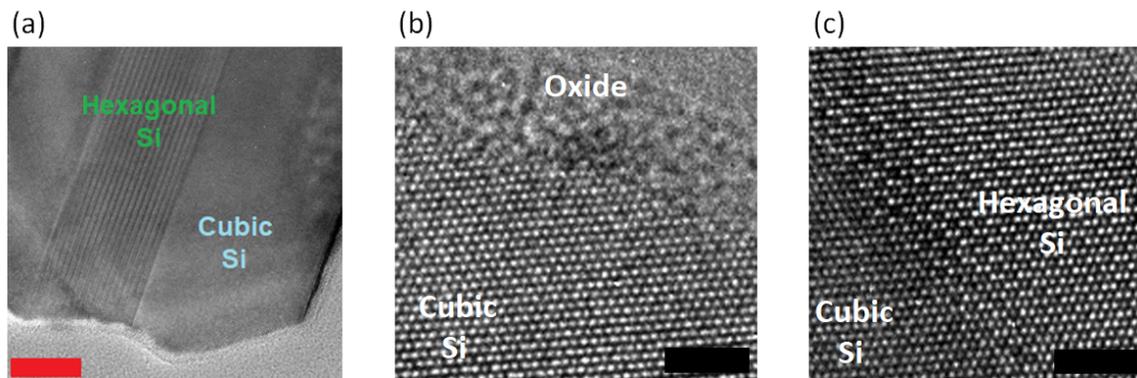
Figure 3.3: TEM images showing the crystal structure of a SiNW with OSFs. (a) TEM image of SiNW cross-section, showing hexagonal-phase Si formed by OSFs in nanowire core, surrounded by a cubic-phase Si shell. Scale bar 10 nm. (b) HRTEM image of SiNW cross-section near the nanowire's surface, showing cubic-phase Si and a native oxide layer. Scale bar 2 nm. (c) HRTEM image of SiNW cross-section near the nanowire's core, showing the cubic-phase Si and hexagonal-phase Si interface. Scale bar 2 nm. Images from Moutanabbir Group archives.

3.2   Hexagonal-Core SiNW Raman Spectroscopy

Before starting the SiNW SB-FET device fabrication procedure, the nanowires must be transferred from the growth wafer to our prepared chips, each of which containing the grid pattern over an oxide layer. Using a diamond-tip pen, a small chip is removed from the wafer provided by the grower (either the "cubic-only" or the "OSF" SiNW growth wafer). Since a roughly 5 x 5 mm chip (called a "source chip") can easily contain thousands of VLS grown silicon nanowires, they can be saved and used for almost the entire duration of a research project.

To transfer the SiNWs from a source chip to our samples (called the "scattering" process), the selected source chip (either the "cubic-only" or "OSF" chip) is placed in a small plastic vial and immersed in a few milliliters of acetone. The surface of the chip is then gently scratched with a sharp metal edge (e.g. from metal tweezers)

to release large amount of nanowires into the acetone liquid. The vial is sonicated in an ultrasound bath for 5 minutes to insure that the SiNWs are removed from the substrate and that the suspended nanowires separate from each other. A few drops of the SiNW-acetone solution are placed on each grid patterned chip, and a N_2 gun is used to help the acetone dry off without leaving too many organic residues.

After scattering the SiNWs on several chips, we use basic optical microscopy to find nanowires on the surface of the oxide layer. The grid pattern on the sample is used to note the exact location (with standard grid coordinate notation) of the SiNWs, making it possible to easily find the same nanowires again at any time. Typically, several dozen individual SiNWs may be found on each chip, but only a few (usually five or six) are recorded. We only select the best SiNWs as candidates to continue our study. The nanowire should be at least 5 μm long and not too close to grid markings or other SiNWs.

The crystal structure of each individual nanowire must be known, as we wish to correlate it with the results obtained from the SiNW device electronic measurements. The standard direct method to identify nanowire crystal structure is by electron microscopy using a Transmission Electron Microscope (TEM) [14]. However, this technique is costly and difficult. We chose instead to use an indirect approach to characterize the SiNWs via Raman Spectroscopy, which is the subject of this section.

3.2.1 Raman Spectroscopy

Knowledge of the exact atomic composition and structure of a crystal allows us to predict most of its physical properties (see section 2.1.2). Using quantum theory, the various energy levels for electrons and lattice vibrational modes (phonons) can be calculated, and these in turn are used to determine values for various measurable electrical, thermal and optical quantities [21]. The opposite case is also true, where an experimenter will use these measured quantities to infer electron and phonon energies and deduce a crystal samples composition and structure. This indirect approach can be used as an alternative method to more direct approaches in characterizing crystals, such as TEM or Atom Probe Tomography (APT) [62, 63].

A technique used to optically measure the phonon spectrum in a crystal lattice is by Raman scattering Spectroscopy, sometimes called simply "Raman" [21]. The information gathered from previous theoretical and experimental studies allow the data from Raman to be a way to probe crystal composition and structure in a sample.

When laser light is incident on a crystal, most of the reflected light contains photons of wavelength equal to the laser source. However, this scattering event may occur simultaneously with the emission or absorption of a phonon. When an optical phonon is emitted or absorbed, the process is known as Raman scattering (the process is called Brillouin scattering if an acoustic phonon is involved). The coupling between an electron energy level and a phonon mode in a particular crystal lattice determines the probability of a Raman event taking place.

In this case of photon-electron-phonon interaction, the emitted photon will not

be identical to the incident photon. The shift in energy between these two photons (called the "Raman shift", often expressed in cm^{-1} units) corresponds to a phonon mode that is specific to the materials crystal composition and structure. The intensity of the emitted ray at a certain energy shift is proportional to the probability of the Raman event occurring at that Raman shift.

In this work, the Raman Spectrometer found at Concordia University was used to take Stokes Raman scattering measurements (called "Raman scan") on our SiNW samples. Once the Raman scan is complete, the spectrometer software outputs a graph showing the spectrum of the intensity of the diffusive light from the sample. The curve on this intensity versus Raman shift plot is viewed as the "Raman signature" of the material under laser illumination. Raman spectroscopy is often used in material science and chemistry as an easy method to identify and distinguish various crystals and molecules. Each intensity peak on a Raman signature (or "Raman peak") corresponds to a specific feature of the material, serving as an optical "fingerprint" of its atomic structure.

Since Raman spectroscopy is very sensitive to a crystals lattice structure and symmetries, this material characterization method can also be used to measure subtleties in the crystal structure [64]. Careful measurements can detect local strain, crystal defects and even various atomic isotopes found in the lattice.

3.2.2   SiNW Raman Signature

Since our silicon nanowires are scattered on a silicon substrate, acquiring data of sufficient quality to differentiate the SiNW Raman peaks from the bulk Si substrate is very challenging. The substrates Raman signature will dominate the data by at least an order of magnitude (the SiNW contribution to the detected scattered light will appear as "noise"), so great care must be taken to analyze the data.

Using Raman has the advantage that this method is sensitive to the atomic isotope composition of the sample. As predicted by the harmonic oscillator model for phonons in a lattice, heavier atomic mass will red-shift the Raman signal by reducing the equivalent phonon modes energy. This effect is very useful to be able to distinguish the nanowire Raman signature from the background. Natural silicon consists almost entirely of Si-28 and gives a very familiar Raman peak at 520 cm^{-1} used to confirm the presence of cubic Si crystals in a given sample. This Raman peak, however, is red-shifted to 515 cm^{-1} in a cubic Si-29 crystal, and to 510 cm^{-1} for cubic Si-30 [58]. Our SiNWs are grown with these heavier isotopes during the VLS process (see section 3.1.3), which will allow us to distinguish the SiNW crystals fingerprint from the large background signature. This is only possible if the Raman equipment's spectral resolution and signal-to-noise ratio are outstanding.

In this work, the spectrometer is set to take a Raman scan in the 0 - 1100 cm^{-1} Raman shift window using a 532 nm laser to illuminate the samples at 2 mW for 3 s. The grating step motor (which the software will output as the Raman shift in our data) is calibrated using the 520 cm^{-1} peak found on a pristine Si chip (kept

separately for calibration purposes only). The laser is then placed on a sample chip at

a position next to the SiNW we wish to characterize, avoiding the gold grid patterns

and any visible surface impurities. The laser spot size is made as small as possible

(roughly 1.5 μm) by placing the chip at the 50x microscope objectives focal point.

A Raman scan is taken to record the local background Raman signature (see red

Raman scan in Fig. 3.4). Since the substrate is a natural silicon wafer, the signal is

dominated by the familiar 520 cm^{-1} peak (its position confirms proper calibration of

the 1800 lines/mm grating).
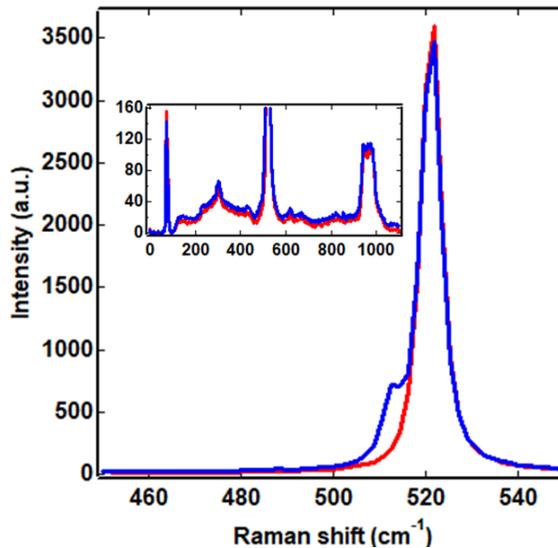
Figure 3.4: Raw Raman scan data in relevant 450 - 550 cm^{-1} Raman shift range from a SiNW containing no OSFs. Raman scan (red) from local background surrounding the SiNW and Raman scan (blue) showing SiNW Raman signature are shown. Large 520 cm^{-1} peak clearly shown as the scan's main feature. An extra peak found at 515 cm^{-1} in blue confirms the identity of the SiNW. Inset: Full Raman scan window of same data. Most of the features found in this Raman scan (direct output of the Raman equipment) are discarded.

To collect data, several Raman scans are taken on each SiNW by centering the

laser spot on various positions along the length of the nanowire, and the average is

taken as the accepted SiNW Raman signature. Only Raman peaks found in the 450 - 550 cm^{-1} Raman shift range are useful to characterize our SiNWs. Features found elsewhere (see inset in Fig. 3.4) are ignored. A peak found in the 510 - 515 cm^{-1} range confirms the identity of the SiNW. Since it is found very near the large 520 cm^{-1} peak, the SiNW signature usually appears as an asymmetrical shoulder on the substrate signature and can easily be overlooked (see blue Raman scan in Fig. 3.4).

However, by correctly subtracting the background Raman scan from the SiNW Raman scan data, the component of the nanowire-only signal can become more apparent and easier to analyze (see green Raman scan in Fig. 3.5). If the data were acquired very carefully, the large 520 cm^{-1} peak can even be omitted completely (only positive values for detected intensity are plotted in Raman scan graphs, as negative values are artifacts from subtraction).
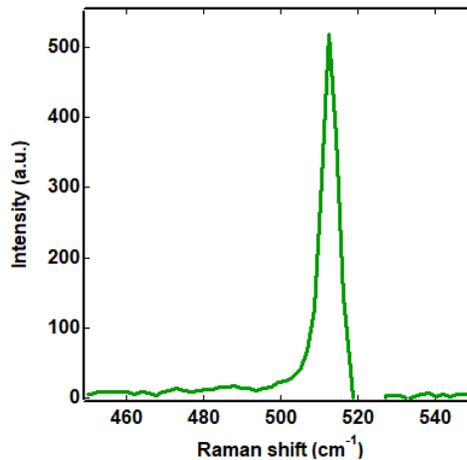
Figure 3.5: Raman signature in relevant 450 - 550 cm^{-1} Raman shift range of a SiNW containing no OSFs. Large 520 cm^{-1} peak from substrate in raw Raman scan data is removed by background subtraction. The extra peak found at 515 cm^{-1} which confirms the identity of the SiNW is now clearly visible.

The values for the peaks center position, width and height are extracted using a

dual Lorentzian-Gaussian curve fitting method known as a Voigt curve fit done by the Raman software [15].

3.2.3 Hexagonality

In addition to the cubic peaks (510 - 515 cm^{-1}), the Raman signature of SiNWs with OSFs will also contain a Raman peak roughly around 485 - 490 cm^{-1} (see Fig. 3.6(a)). The exact values for Raman peaks may vary by 1 - 5 cm^{-1} due to local temperature by laser heating, sample cleanliness and spectrometer calibration [65]. This extra feature probed by Raman spectroscopy identifies the presence of ordered crystal defects which offer new detectable phonon modes in the lattice [15, 66]. Note that we are interested in using Raman spectroscopy to simply confirm the presence of OSFs, not to characterize the exact local stacking sequence (e.g. 9R or 2H).

The data obtained with Raman allow us to not only confirm the presence of OSFs, but also to quantify their volume fraction, thus completing the SiNW characterization procedure. The ratio of OSFs found within the nanowire corresponds to the volume fraction arrangement of the hexagonal-phase Si crystal found in the nanowire core surrounded by the cubic-phase shell. This is directly measured by the ratio *Hex* of the integrated peak area (as calculated using the Voigt fit parameters) of the 485 cm^{-1} peak I_{SF} by the total integrated peak area from both the OSF Si peak and the cubic Si peak around 510 cm^{-1} I_C (see Fig. 3.6(b)) [28, 60].

$$Hex = \frac{I_{SF}}{I_{SF} + I_C} \tag{3.1}$$
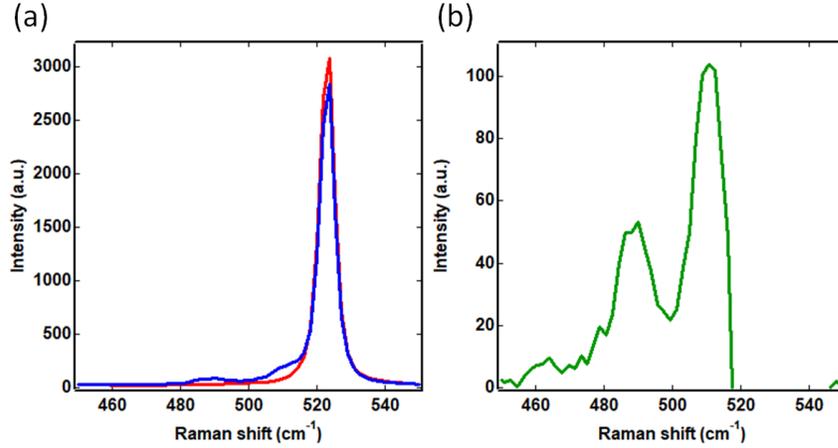
Figure 3.6: Raman scan data in relevant 450 - 550 cm^{-1} Raman shift range from a SiNW with OSFs. (a) Red: Raman scan from local background surrounding the SiNW. Blue: Raman scan showing SiNW Raman signature. Large 520 cm^{-1} peak clearly shown as the scan's main feature. The extra peaks found at 485 cm^{-1} and 510 cm^{-1} in blue confirm the identity of the SiNW and the presence of OSFs. (b) Large 520 cm^{-1} peak from substrate in raw Raman scan data is removed by background subtraction. The extra peaks are now clearly visible. Extracted *Hex* value for this SiNW is 0.313.

Defined as the "hexagonality" of the SiNW, the value of *Hex* varies from 0 to 1 and quantifies the hexagonal-core volume fraction. The SiNWs that only contain the cubic phase of Si will have a *Hex* value of 0, since $I_{SF} = 0$ in Eq. 3.1. The SiNWs with a non-zero value for *Hex* are identified as having OSFs. If *Hex* would be found to be equal to 1, the SiNW would only contain the hexagonal phase of Si, but we have not observed this case. In this work, the values of *Hex* vary between 0 and 0.4, meaning no SiNWs were found to have more OSFs than in 40% of its volume.

As was previously discussed (see section 3.1.3), some of the SiNWs with OSFs are found to be kinked. In this case, Raman measurements will show that the value of *Hex* changes substantially between both sides of the kink [15].

3.3 Fabrication of Electrical Contacts

A selection of SiNWs are now characterized by Raman spectroscopy, and a catalog is prepared containing an optical microscope image confirming their position on the chip along with a list of their lengths and *Hex* values. To complete their characterization, the diameter of the SiNWs are measured by Atomic Force Microscopy (AFM). The average of multiple scans along the length of the nanowire is considered to give the value of its diameter.

The desired set of SiNWs must now have contacts placed on them in order to take measurements of their electronic properties. Once two metal electrodes are in contact with both ends of the nanowire, the SiNW becomes the 1D semiconducting channel. Since the nanowire is already over a dielectric layer, with the heavily doped Si substrate acting as the back gate electrode, the SB-FET design is complete, and each contact-channel system is given a device name.

This stage in the fab process is the most challenging and has the lowest yield. In this work, either photolithography or electron-beam lithography (EBL) techniques were used to prepare contacts on our SiNW samples. The former was chosen if micron-scale precision was sufficient to obtain an acceptable yield, and the latter if nano-scale precision and complex contact patterns were necessary. In this section, both methods will be presented, as well as the procedure to connect the electrodes to our measurement circuit.

3.3.1 Photolithography: Stencil Method

Fundamentally, the procedure taken to define the contact patterns on the sample surface using photolithography is the same as the one followed when placing the grid patterns (see section 3.1.2). The difference is in the choice of mask used during the UV lamp exposure step. The contact pattern mask contains several "pad" (a large square used to facilitate wirebonding, see section 3.3.3) and "arm" (a thin rectangle connecting the pad to the nanowire) contact designs of various dimensions. A quick sketch of the chip and the locations of the nanowires can help to make decisions for which "pad-arm" designs will be used and how to best position them on the surface.

The goal, of course, is to place two arm designs so that their ends rest on both sides of the SiNW, each covering about a micron of the nanowire length, forming the contacts. This will leave a few microns of the SiNW between the two contacts that will act as the channel of the semiconductor device. Care must be taken in order to insure that the two designs do not overlap, causing a short circuit.

The biggest challenge to overcome in this step of the fab is the alignment issue. With a roughly 50 nm nanowire diameter, it is far from trivial to successfully place the arm pattern exactly on top of the SiNW target. The level of precision required is far beyond the typical capacity of the MA6 photolithography equipment. The camera system included in the MA6 has a low optical zoom and low resolution, which is sufficient for millimeter-scale mask alignment purposes. For our samples, the grid marks are visible under the camera's view screen, but the nanowires are too small to appear. This makes the alignment of the contact arms extremely difficult and mostly

guesswork, with a yield of about one successful attempt on ten.

The "stencil method", a photolithography method we developed to resolve this issue, is a technique requiring only basic materials and is simple to perform. In addition to the usual supplies, a transparency slide and a dry erase marker is brought to the clean room.

Once the sample is loaded into the MA6 with the equipment ready to expose the contact design, the optical image of the target SiNW taken on the microscope is loaded on the computer next to the MA6. The image size is then modified until an exact 1:1 scale between the optical image and the MA6 camera screen image is obtained. By placing the transparency slide over the computer screen, the outline of the nearby grid mark is drawn with the marker. A line is then traced over the SiNW, which provides its exact location on the surface with respect to the grid mark. The outline of the desired locations for the contact arms are added to the transparency (drawn by hand).

Placing the completed transparency over the MA6 screen, it is now very simple to align the contact design over our drawing. Despite being invisible on the MA6 screen, it is now possible to successfully place both contacts on the SiNW target. As long as the user has enough patience to get the stencil scaling done correctly and basic artistic ability, this method allows the photolithography alignment process to achieve a near perfect yield.

The stencil method is used when we wish to fabricate a large number of SiNW devices using simple photolithography techniques. To complete the process, metal

thin films are placed over the developed resist pattern using the CVD and lift-off procedures discussed previously (see section 3.1.2). Typically, the contact electrodes are made from 3 nm of Cr (sticking layer) and 100 nm of Au.

3.3.2 Electron-Beam Lithography

Another method to define the contact pattern on the resist layer is by Electron-Beam Lithography (EBL). Using EBL instead of photolithography has the main advantage of being much more precise and accurate [53, 54]. While the stencil method is very successful, it is not possible with this method to control the exact position of the contact arms on the nanowire surface. Placing more than two contacts on a single SiNW would also be nearly impossible with the stencil method, as photolithography is only accurate to within a few microns. However, using EBL methods introduces higher levels of complexity, difficulty and operating cost to the process.

We begin by loading the optical image of the SiNW on which we want to place EBL-defined contacts. The rotation and scaling of the image is adjusted until the 100 x 100 μm space framed by the four grid marks containing the SiNW in question lines up perfectly with a 5 x 5 μm Cartesian grid. With the CAD feature of the EBL software (in this work, we use "Raith E-line Plus"), the desired contact pattern (including the exposure doses for each section) is drawn over the Cartesian grid, giving them precise coordinates. The values of L_{con} needed in our transport model (see section 2.5.2) for all contacts are now known to within the order of 10 nm. The contact arms are connected to six rectangular bars placed at the border of the 100 x

100 μm space, which will be used later to facilitate placing the contact pads.

The chip is prepared by placing a bilayer resist of copolymer and PMMA by spin-coating, then inserted into the EBL chamber. Before allowing the SiNW and the 100 x 100 μm framed space to be exposed to the electron beam, great care is taken to calibrate the instrument for appropriate voltage and current values, proper beam focus and to prevent astigmatism effects. The CAD pattern is then loaded into the EBL computer, which will correlate the sample stage motor positions to our Cartesian grid using the four grid marks to define the frame. This will allow an automatic alignment between the desired contact pattern and the target SiNW.

Once the EBL equipment has successfully written the contact pattern, the chip is removed from the chamber. To develop the resist, the chip is placed in a MIBK solution, then transferred to methanol, and finally to IPA. Then, metal thin films are placed over the developed resist pattern using the CVD and lift-off procedures (see Fig. 3.7(a)) discussed previously (see section 3.1.2).

To place large contact pads connecting our EBL-defined contact arms (needed for wirebonding, see section 3.3.3), we use standard photolithography methods to align a simple six-point pad-arm pattern over the six rectangular bars placed at the border of the design. The entire process is completed once these additional metal thin films are placed using CVD and lift-off (see Fig. 3.7(b)).
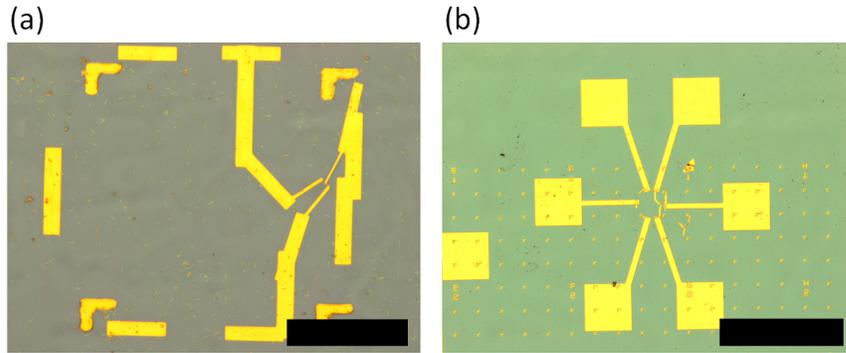
Figure 3.7: Images from optical microscope showing an EBL-patterned SiNW SB-FET device. (a) The success of the EBL equipment in writing the CAD designed contact pattern is made evident after the CVD and lift-off procedure. Scale bar 50 μm. (b) Large contact pads are placed by photolithography with a simple six-point pad-arm pattern to facilitate wirebonding. The arms of the pads are aligned with the rectangular bars previously placed by EBL. Scale bar 500 μm.

3.3.3 SiNW SB-FET Wirebonding

The final step to complete the fabrication of our SiNW devices is to make a connection between the metal electrodes and our transport measurement circuit. To facilitate this, a gold-plated 24-pin chip carrier is used to package the device. A small drop of silver paint is placed on the gold surface, then the chip is carefully pressed and left to dry. In addition to adhering the chip to the carrier, the silver also makes an electrical connection between the gold surface and the backside of the chip (see Fig. 3.8(a)). The back-gate electrode is now installed, which completes the desired SB-FET device configuration (see section 2.4.1).

A wirebonder is used to connect the source, drain and gate electrodes to the carrier pins. The wirebonder available in the Concordia University lab was used in this work. The equipment uses ultrasonic welding from the tip of the bonding tool to place very thin aluminum wires on a metallic surface (see Fig. 3.8(b)-(c)). Great care must be

taken while operating the equipment, as static electricity may damage the device. The user, tweezers, chip carrier, wirebonder and stage must all be properly grounded during the process.
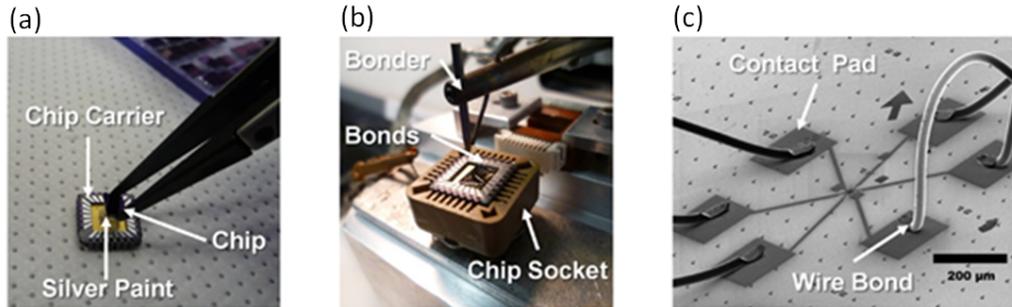
Figure 3.8: Images showing the wirebonding steps completing the fab process. (a) The chip is held in place on the chip carrier using silver paint. The gold surface of the carrier is now electrically connected to the gate electrode. (b) Aluminum wires are used to connect the carrier pins to the large contact pads. These wires are installed using a wirebonder. (c) Tilted SEM image showing the wirebonds and the device layout. Image from Champagne Group archives [54].

Once all the wirebonds are considered to be properly installed, we make note of which pin corresponds to which electrodes on each device on the chip using the carrier pin chart. Only a single pin is necessary for the common gate electrode to all devices, as they all share the backside of the chip.

We now have a library of fabricated SiNW SB-FET devices, with each nanowire channel on each chip carrier characterized and ready for electronic measurements.

3.4   Electron Transport Measurements

As the fabrication of our SiNW SB-FET devices is finished, we now proceed to prepare the measurement circuit setup to acquire data. Through lithography methods

and wirebonding, the micron-scale metal electrode contacts on each nanowire are connected to the chip carrier pins. Our data acquisition circuit uses simple BNC coaxial cables to connect the voltage and current sources to the measurement electronics. Prepared by previous group members in the Champagne Group, electronic instrumentation and software found at the Concordia University lab are used in this work to facilitate data acquisition.

In this section, we present the measurement circuit design, the preliminary tests necessary to insure that the setup will function properly, and the various methods to acquire data on our SiNW SB-FET devices.

3.4.1 Circuit Optimization for Low-Noise Measurements

Before constructing the measurement circuit, we must first be able to have easy electrical access to the pins on the chip carrier holding our collection of SiNW SB-FET devices. To achieve this, we use an instrument known in the Concordia University lab as a "stick". It consists of a long hollow metal pipe containing the necessary wiring to connect each pin of a chip carrier holder found at the base of the stick to its corresponding pin of a BNC breakout box found on top of the stick. The chip carrier is installed at the end of the pipe, which is electrically shielded from its environment. The stick can be placed inside a cryogenic dewar if we wish to control the temperature of the device.

Before loading the chip carrier in the holder, however, the stick must first be tested to confirm that the instrument and its wiring has not been damaged during

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previous use. Using a simple multimeter, we first make sure that none of the pins have a short to ground, which would compromise the electrical insulation of the chip carrier in the stick. Second, there must be no cross-talk between any of the pins, as this would falsify the data. Finally, we check that the resistance between each pin on the breakout box and its corresponding pin on the chip holder is very low (about 5 - 10 Ω is the expected value). Once it is confirmed that the stick is functioning properly, the chip carrier is carefully installed with all pins grounded. The user and tweezers must also all be properly grounded during this process.

We can now prepare the SiNW SB-FET device electrical measurement circuit using simple BNC coaxial cables to connect the stick to the various electronic components. The necessary equipment includes a National Instrument DAQ card (called simply "DAQ"), a Keithley voltage source (called simply "Keithley") and an Ithaco current preamplifier (called simply "Ithaco").

The DAQ is an electronic instrument capable of sending and receiving voltages according to instructions given by National Instrument software. Both input and output pins on the DAQ have a maximum voltage value of 10 V (a shunt to ground is activated to prevent overloading the card if excessive power is needed or received). The DAQ loses sensitivity and stability if voltages less than 0.1 V are involved. In this work, one of the DAQ output channels is used to supply the bias voltage V_B to our devices at the source electrode of the SiNW SB-FET device (see section 2.4), and one of the input channels is used to measure the bias voltage source itself.

The Keithley is used to supply the gate voltage V_G to our devices since the equipment can generate a much larger voltage than the DAQ (up to 250 V). It is also possible to control and monitor the voltages supplied by the Keithley at the gate electrode with our data acquisition computer. To prevent the gate voltage from fluctuating, a low-pass filter is placed at the output of the Keithley. A series limiting resistor of 1 MΩ is also added to prevent accidental high currents from damaging the equipment (which could occur during a dielectric breakdown of the oxide layer due to high electric fields generated by the gate voltage, or by or large gate leak currents, see section 3.4.2).

The Ithaco is a current preamplifier, which converts the current from its input channel to a corresponding voltage at its output. The input is placed on the drain electrode to measure the current passing through the nanowire. Since the current generated by our devices will be very low (often in the pA range), we use the highest sensitivity setting on the Ithaco in this work to amplify the signal as much as possible. The output of the Ithaco is then placed at one of the input channels of the DAQ.

An acquisition software written by previous Champagne Group members in National Instruments LabWindows CVI is used to both set the desired parameters for our experiments and to control and monitor the DAQ voltages [53, 54]. The software GUI allows the user to setup the desired voltage sweeps (bias, gate or both) by modifying parameters such as voltage ranges, number of steps and acquisition rates. All relevant information needed to properly interpret the output voltage of the Ithaco into its corresponding measured current (via the sensitivity conversion factor) can

also be included in the software. The GUI also includes a graph window that updates as data is taken to facilitate acquisition visualization while the sweep is in progress. The *I-V* data are recorded in a simple text file (.txt extension) that can then be loaded into a data analysis software (in this work, we use the "Igor" software from WaveMetrics).

Our DC SiNW SB-FET device measurement circuit is now ready to begin taking data. Before starting measurements, a few tests are necessary. We check that the entire circuit is properly grounded, then we use the DC measurement setup to verify the known value of resistance of a simple resistor. This will confirm that our circuit design is correct and functional.

3.4.2 Gate Leakage

A final but important step before taking data if to verify if the SiNW SB-FET suffers from "gate leakage". In an ideal back-gate SB-FET device, the gate electrode is only capacitively coupled to the channel (see section 2.4.1), meaning that there should be no current passing through the gate electrode. However, it is possible that the oxide layer acting as the gate dielectric is compromised, creating a parasitic connection between the gate electrode and a component of the chip surface. This could happen during the later stages of fab, while taking data on another device on the currently installed chip (if large gate voltages were used on a previous sweep, for example), or if static electricity damaged the device due to improper grounding during installation.

The main culprit, however, is the wirebonder. As was mentioned before (see

section 3.3.3), this instrument is used to place aluminum wires via ultrasonic welding onto the contact pads made from metal thin films. However, if the wirebonder tool pushes too hard on the surface, or if high ultrasonic power is used, it is possible that the equipment will damage the thin oxide layer underneath the contact pad. This will create an unwanted connection between the gate electrode and the source or drain electrode that cannot be undone. The measured current through the device, which is assumed to be solely passing through the SiNW channel, can now "leak" into or from the gate electrode, which may falsify the data and analysis.

Due to the nature of our micro-fabrication, which depends heavily on the experimenter's skill, some gate leakage is always expected to be present on our devices. Thankfully, it is often found that the gate leak acts as a simple linear resistor, and a gate leak "resistance", higher than the device resistance, can be extracted. Since the device resistance of most of our samples exceed the $G\Omega$ range, even a $T\Omega$ gate leak will appear in our data, but luckily will be removable by simple subtraction. This will allow us to ignore the effects of gate leakage and continue in the data acquisition and analysis of the device in question.

Occasionally, a device will have a strong gate leakage behavior that will effectively render it useless, forcing us to remove it from our device library and future analysis. If the gate leak resistance is at least a few orders of magnitude lower than the device resistance, then the gate leakage will dominate the measured current. The useful data will then act as being merely "noise" that will be difficult to properly extract.

Even worst, if the gate leak cannot be modeled as an ohmic resistor due to a non-linear behavior, then it will be impossible to subtract the gate leakage from our data reliably.

3.4.3   Data Acquisition Procedure

When satisfied that the measurement circuit is tested and functional, data acquisition can begin. The SiNW SB-FET devices are included in the circuit one at a time using the appropriate BNC pins from the stick's breakout box. Since our devices have very high impedance, the circuit must be able to measure sub-pA current levels with a good signal-to-noise ratio.

To optimize acquisition, data are taken at a low sweep speed of 1 data point (a measured current at a given bias and gate voltage) per second at maximum Ithaco sensitivity settings (300 ms rise time at 10^{-12} A/V sensitivity). To reduce noise in the measured current, we minimize the length of the various BNC coaxial cables used to make the circuit, we use long and grounded BNC cables to wrap around the circuit cables (to act as electrostatic shields), and we place the Ithaco in "battery mode" during acquisition to remove the noise from the ground itself.

A slow sweep of the gate voltage from $V_G = 0$ to the maximum desired value in the current experiment (typically 80 V) at zero bias voltage ($V_B = 0$) gives an idea about what kind of gate leakage the device is expected to suffer from. On an ideal SB-FET device, this sweep should measure no current whatsoever at all voltages, so any detected signal is identified as gate leakage. Monitoring the sweep while it's

running is important, as the test must be aborted if any strong or non-linear traits are present in the I-V curve (see section 3.4.2).

After checking for gate leakage, we begin by taking "bias sweeps", which are sweeps of the bias voltage at a fixed gate voltage. With the gate electrode "floating" (neither grounded nor set to any specific value), a slow sweep of the bias voltage from $V_B = 0$ to the maximum desired value in the current experiment (typically 8 V) is done in order to get an idea about the device's main characteristics. The shape of the I-V curve is an indication of whether the contacts play an important role or not in the device performance (see section 2.5.2), and a quick mental calculation of V_B/I gives the device resistance's order of magnitude. Again, monitoring the sweep while it's running is important, as the test must be aborted if any strong currents are overloading the electronic equipment (in such a case, the Ithaco and DAQ settings must be changed to accommodate before continuing acquisition).

Once confident that the device is measurable (a current was eventually detected, and this current is dominated by the device and not by gate leakage), a full bias sweep can be done where V_B varies from one end to the other of the desired bias "window" (typically from -8 V to 8 V) at V_G set to 0 (see Fig. 3.9). The symmetry in the I-V curve's features will give an idea about the different barrier effects on the channel between the source and drain contact electrodes (see section 2.5.2).

As mentioned before, an I-V curve obtained by sweeping the bias voltage at a fixed gate voltage is called an "output curve". To verify the validity of the features found on the output curve (to check that the data are reproducible to increase confidence),

we repeat the full bias sweep several times in both "forward" (negative to positive values of bias) and "reverse" mode (positive to negative bias). Any hysteresis found in these I-V curves is noted to understand device stability (verify if the values for the device resistances are changing over time) and circuit performance (verify if parasitic capacitance effects from the contact electrodes or from the electronic equipment are influencing acquisition).
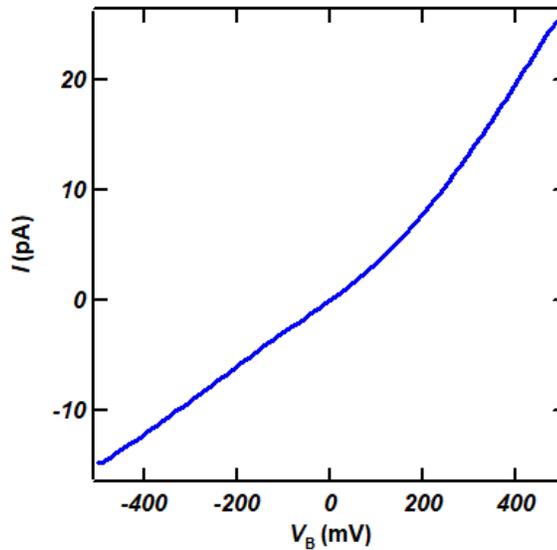
Figure 3.9: Graph of I vs. V_B showing a representative output curve obtained from our measurement circuit on a SiNW SB-FET.

At this point, we continue and begin taking "gate sweeps", which are sweeps of the gate voltage at a fixed bias voltage. By taking full gate sweeps, where V_G varies from one end to the other of the desired gate "window" (typically from -80 V to 80 V) at various V_B values (typically a few at low voltages, then a few at -8 V and 8 V), we can get an idea about the SB-FET behavior of the device (see Fig. 3.10). A featureless I-V curve (constant current) indicates that the device is not "gate-enabled" in the V_G window. The desired I-V curve feature is a switching behavior (see section 2.4.2),

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indicating the presence of an ON- and OFF-state.

As mentioned before, an *I-V* curve obtained by sweeping the gate voltage at a fixed bias voltage is called a "transfer curve". Again, to verify the validity of the features found on the transfer curve, we perform hysteresis checks on the gate sweeps.
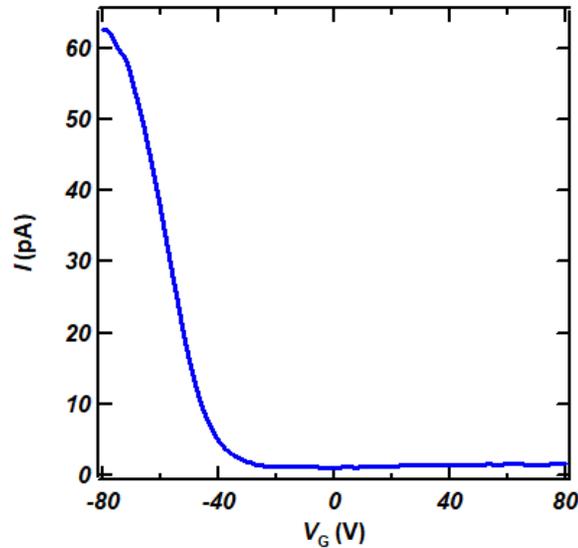
Figure 3.10: Graph of I vs. V_G showing a representative transfer curve obtained from our measurement circuit on a SiNW SB-FET.

Once all of these checks are complete, the main characteristics of the SiNW SB-FET are known, and a decision is made whether the device in question is important to study according to the results from each test. Devices that do not meet the required criteria are discarded, and the process is repeated on the next device.

Devices that are accepted as useful data entries are subject to a "mega sweep". In this case, the acquisition software takes multiple bias sweeps for all desired values of the gate voltage, creating a large "map" of all possible output and transfer curves found in the bias and gate windows.

Using our settings for optimal measurement quality, this full $I - V_B - V_G$ scan of

a single SiNW SB-FET device can take 8 hours to complete.

A library of over 50 SiNW SB-FET devices were fabricated for this work. Most were discarded due to significant gate leakage found during preliminary data acquisition, preventing proper device operation (see section 3.4.2). Of those that remained, others were discarded due to poor signal-to-noise ratios preventing the measurement of either the device resistance during bias sweeps or the transconductance during gate sweeps. Only eight devices are left, all of which are presented in the following chapters.

The collected data is now analyzed following the procedures presented in Chapter 2. The results of this analysis is discussed in the following chapters.

Chapter 4

Giant Conductivity Suppression in Hexagonal-Phase Core SiNWs

Using the SiNW SB-FET devices fabricated and the measurement methods presented in Chapter 3, we now explore the impact of introducing the hexagonal-phase core on SiNW transport. We will rely on the theoretical concepts from Chapter 2, extensive measurements and data analysis to give insight on the effects of OSFs on the transport properties of our NWs.

Specifically, we will show how adding OSFs in SiNWs greatly impacts their conductivity, charge mobility, and charge density. By tuning the volume of the hexagonal core (the *Hex* parameter), the channel conductivity of a SiNW SB-FET device can be suppressed from roughly 100 to 1 μS/cm. We demonstrate that the Cub-Si/Hex-Si crystal structure interface plays a dominant role in controlling charge injection from the contacts and current flow distribution within the nanowire cross-section. These

effects are explained by a transport model where current is prevented from flowing within the Hex-Si core section of the NW channel.

The first section describes the six SiNW SB-FET devices that are studied in this chapter. The parameters for their contact and channel transport properties are extracted, giving us key parameters to structure the discussion. In the second section, we quantify the impact of *Hex* on SiNW electrical properties such as conductivity, charge mobility, and charge density. A transport model will be presented for SB-FETs made from SiNWs with OSFs, allowing us to make predictions on how to control and predict device behavior.

4.1   SiNW SB-FET Parameter Extraction

Below is the list of the six devices that will be discussed in this chapter. They were selected due to their channel dimensions (length of roughly 2 μm or more) and their lack of gate leakage issues (see section 3.4.2). Three were fabricated using SiNWs with a purely cubic crystal structure (*Hex* = 0) and are named "C1", "C2" and "C3", respectively. Another three were fabricated using SiNWs with a Cub-Si/Hex-Si crystal structure of various *Hex* values and are named "H1", "H2" and "H3", respectively. Comparing and understanding the results from Devices C1, C2 and C3 to Devices H1, H2 and H3 is the primary purpose of this chapter. We will also study the effects of length (comparing the shorter Devices C1, C2 and H1 to the longer Devices C3, H2 and H3) and diameter (comparing the larger Devices C1, H1, H2 and

H3 to the smaller Devices C2 and C3) on the acquired results.

The relevant SB-FET physical dimensions (length between contacts L, diameter d and contact lengths L_{con} of the source and drain electrodes) of each device are also included in the table. The errors on the presented values are on the final significant digit (e.g. 2.0 means 2.0 ± 0.1). Length scales were measured using SEM images, diameters were measured using AFM scans, and *Hex* values were measured using Raman scans (see Chapter 3 for details).

Table 4.1: Dimensions and Crystal Parameters of Devices

Device Code	L μm	d nm	$L_{con,s}$ μm	$L_{con,d}$ μm	*Hex*
C1	2.0	50	1.0	1.0	0
C2	1.8	25	1.0	0.4	0
C3	3.4	27	1.0	0.3	0
H1	2.0	57	1.0	3.0	0.31
H2	3.6	53	1.5	1.5	0.15
H3	3.1	49	1.5	1.5	0.36

In this section, the transport data obtained from the six $I - V_B - V_G$ sweeps of the six SiNW SB-FET devices are presented. First, in section 4.1.1, the output data of the SB-FETs will be analyzed to extract all relevant contact properties (e.g. contact resistance, SB height) between the metal electrodes and our SiNWs. Second, in section 4.1.2, the transfer data of the devices will be analyzed to extract all relevant channel properties (e.g. conductivity, charge mobility, and charge density) of the SiNWs themselves. In both cases, we will first present the results obtained from C1, C2 and C3, as these devices are easier to compare since their properties should be similar to each other and to SiNW devices reported in literature. Their extracted

properties will then be shown next to those obtained from H1, H2 and H3 to get preliminary information about how OSFs affect the results. The discussion of these results will then follow in section 4.2.

4.1.1 Contact Properties: Contact Resistance and SB

To properly study solely the fundamental transport properties in our SiNWs, it is important to be able to understand and remove contact effects from the data.

Metal thin films are evaporated on our samples in order to place the source and drain electrodes to complete the SB-FET device layout using patterns prepared by either photolithography or EBL methods (see section 3.3). Specifically, our contact electrodes are made from 100 nm thick gold (Au) films evaporated atop of a 3 nm thick chromium (Cr) sticking layer. The SB-FET transport model (see sections 2.3 - 2.6 for all necessary equations and details) also includes a thin oxide layer sandwiched between the Au electrode and our SiNWs. This Au-SiO$_2$-SiNW interface creates a charge injection barrier known as the Schottky Barrier (see section 2.5.3). Understanding the formation and the effects of the SBs is the most difficult challenge to overcome in device physics.

SB-FETs are devices that depend largely on contact behavior [1]. We quantify these various contact properties by analyzing our SiNW SB-FET output data. By extracting contact resistance R_{con}, contact resistivity ρ_{con}, SB height ϕ_{SB} and width λ and the contact non-ideal factor η, we will have the necessary tools to remove all contact effects in future data analysis.

The value of λ is calculated using Eq. 2.11. This allows us to define the contact region and to adjust the channel effective length to $L-2\lambda$. Next, both of the maximum values for $\mathrm{d}I/\mathrm{d}V_B$ are identified as the channel conductance G_{ch}, since the slope of the output curve at large bias is limited by the channel resistance and is unaffected by the contacts [33].

Contact resistance is calculated simply using Eq. 2.12. To discriminate between the source and drain contact resistance values, the measured R_{con} at a given bias voltage is identified as the one from the reverse-bias contact only [32]. When the sign of V_B is negative, all calculated values are attributed to the drain electrode. For positive V_B values, they are identified as effects from the source contact. Using Eqs. 2.13 and 2.16, both values for source/drain contact resistivity and source/drain ϕ_{SB} are calculated, completing the description of the SBs on our devices.

The non-linear behavior found in our output curves shows how contacts affect our data. When contact effects are significant, a barrier regime will exist where conductance is very low until V_B is increased beyond the V_{co} value (see section 2.5.3). The cut-off voltage is extracted using a linear extrapolation of the output curve at the point where G_{ch} is found at the intersect of the bias voltage axis. The value of V_{co} quantifies the non-linear output behavior and is a figure-of-merit for contact effects.

The last parameters that can be extracted are η and δ. Using Eq. 2.21, the non-ideal factor η is calculated, quantifying the quality of the Schottky contacts. Using Eq. 2.22, the δ parameter is found, quantifying contact asymmetry. These two dimensionless values will give us insight on how the contact properties of a particular

SB-FET device are affecting the data and will make it easier to compare contacts between devices.

The output data for the three devices made from Cub-Si only SiNWs (C1, C2 and C3) are shown in Fig. 4.1. The left panels have the ON- (blue), TH- (green) and OFF-state (red) output curves while the right panels have the $\mathrm{d}I/\mathrm{d}V_B$ curve of the ON-state. See section 2.6 for details on how to analyze output data using our SB-FET transport model.

We notice that all devices are clearly controlled by the gate, as the conductance at large bias varies between all three states. In Fig. 4.1(a)-(b), we see how Device C1 has an excellent gate control behavior, as both contacts are tunable with V_G. For Device C2 (see Fig. 4.1(c)-(d)), large Fermi pinning causes the source contact to dominate the output behavior at positive bias, as the current is not modulated by the gate in that bias range. For Device C3 (see Fig. 4.1(e)-(f)), large Fermi pinning causes the drain contact to dominate the output behavior at negative bias. Since conductance increases from the value at $V_B = 0$ for the six contacts studied in this set of devices, all data analysis tools are available. We see that SB-FET devices made from Cub-Si only SiNWs have an output behavior that follows well the predictions of our transport model and are easily characterized (especially Device C1).

In contrast, the output data for the three devices made from Cub-Si/Hex-Si SiNWs (H1, H2 and H3) shown in Fig. 4.2 were both challenging to obtain (sub-pA currents were often found) and difficult to properly analyze.

We notice that all device have reduced gate control compared to their Cub-Si only

Figure 4.1: Contact properties extraction for Devices C1, C2 and C3 (see text for details). (a)-(b) Output and differential conductance for Device C1. (c)-(d) Output and differential conductance for Device C2. (e)-(f) Output and differential conductance for Device C3.
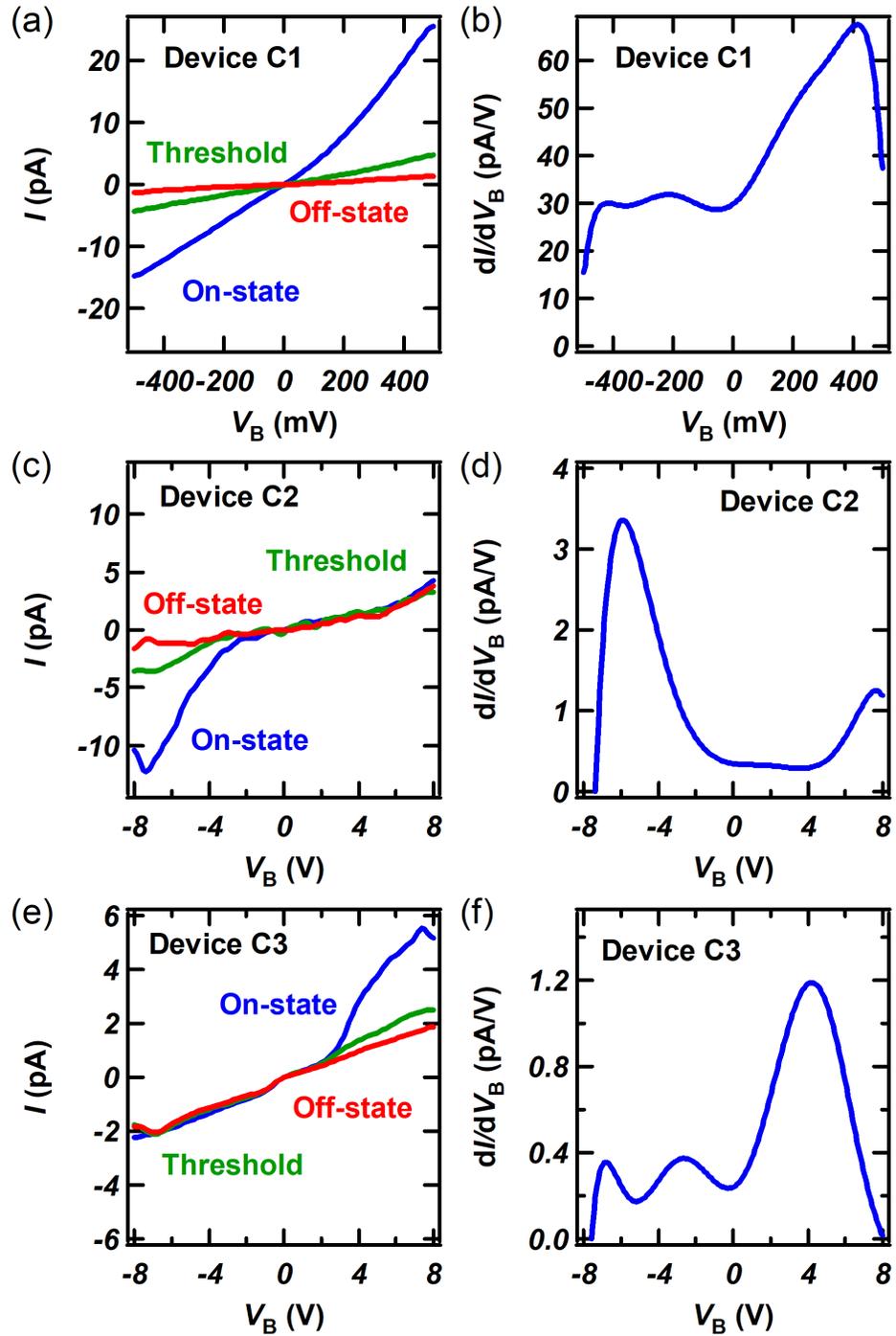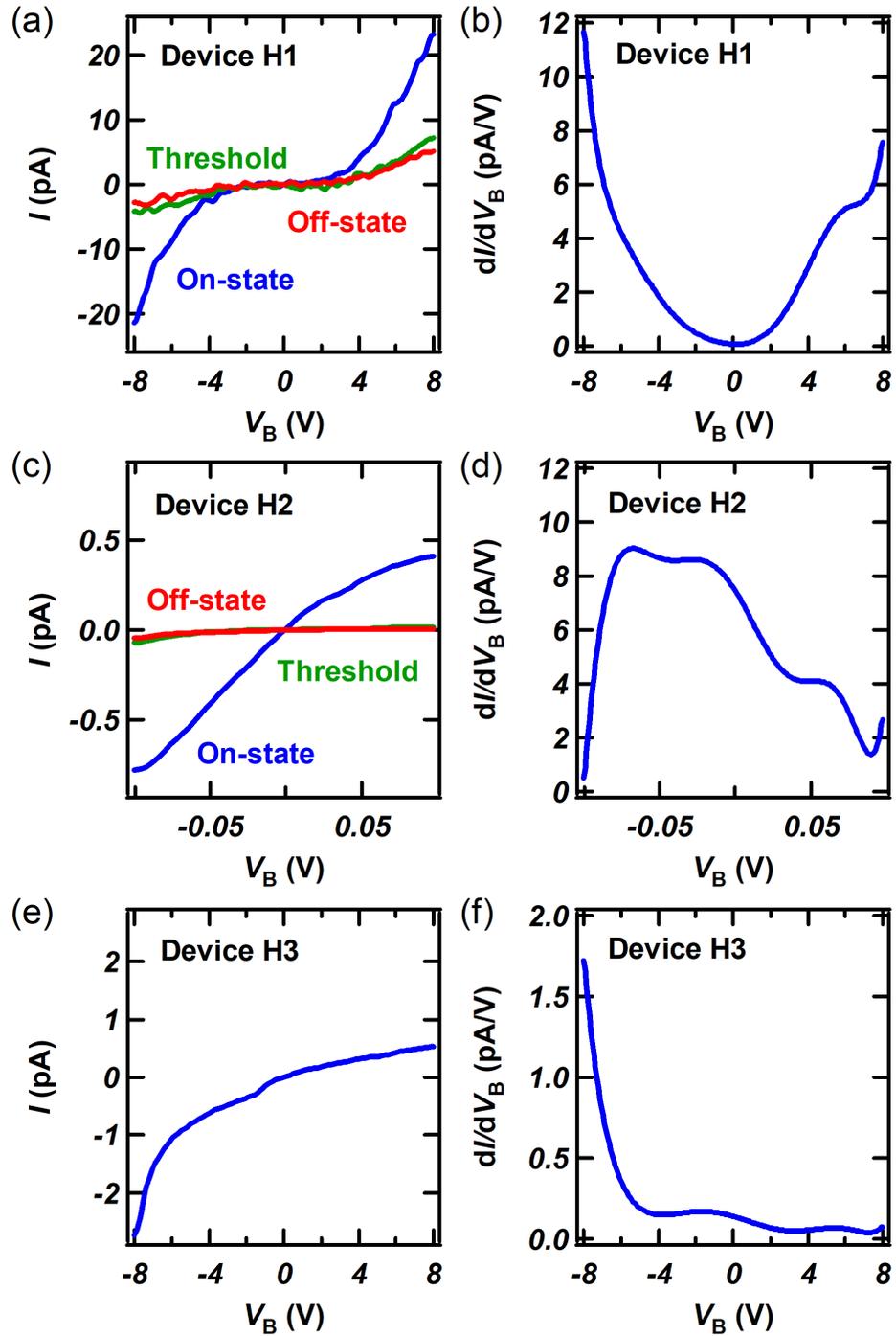
Figure 4.2: Contact properties extraction for Devices H1, H2 and H3 (see text for details). (a)-(b) Output and differential conductance for Device H1. (c)-(d) Output and differential conductance for Device H2. (e)-(f) Output and differential conductance for Device H3.

counterparts. In Fig. 4.2(a)-(b), we see the output data of Device H1. The data from this device is easily comparable to that of Device C1 due to their similar dimensions. We see that the TH- and OFF-state output curves overlap for Device H1, meaning that the gate cannot properly tune the Fermi level of the device. This enhancement in Fermi pinning effects is also seen in the strong non-linear output behavior and reduced conductance found in these three devices (compared to Device C1). In Fig. 4.2(c)-(d), we see that sub-linear behavior is also found in Device H2 at positive bias values. Since conductance decreases from the value at $V_B = 0$ in this case, most of the data analysis methods are not available. For Device H3 (see Fig. 4.2(e)-(f)), a very weak signature in gate tunability prevented us from properly extracting the TH- and OFF-state output curves, hindering future data analysis for this particular device. We see that SB-FET devices made from SiNWs with a hexagonal-phase core have an output behavior that is difficult to characterize (a new model is needed).

Below is a table summarizing the results from characterizing the contact properties of our SiNW SB-FETs. See section 2.6 for details on how to extract contact parameters from output data using our SB-FET transport model using Devices C1 and H1 for numerical examples. The errors on the presented values in Table 4.2 are on the final significant digit (e.g. 2.0 means 2.0 ± 0.1).

Notice that as a general rule, when SB height increases, the measured device current decreases. This confirms that contacts play a large role in SB-FET output behavior [48]. It is predicted that larger nanowire diameters will decrease SB height

Table 4.2: Contact Parameters of Devices

Device Code	λ μm	$R_{con,s}$ GΩ	$R_{con,d}$ GΩ	$\rho_{con,s}$ Ωcm^2	$\rho_{con,d}$ Ωcm^2	$\phi_{SB,s}$ eV	$\phi_{SB,d}$ eV	η_s	η_d
C1	0.19	5.3	1.6	4.2	1.3	0.51	0.48	0.22	0.022
C2	0.13	1200	380	450	60	0.63	0.58	7.2	5.8
C3	0.14	560	83	240	11	0.61	0.53	2.8	0.15
H1	0.20	210	280	190	740	0.60	0.64	8.1	9.6
H2	0.19		6.3		7.8		0.52		0.0069
H3	0.19		2300		2700		0.67		9.6

as the increase in metal-semiconductor interface surface will allow better charge injection. While this is certainly the case for our Cub-Si only devices, the data for our Hex-Si/Cub-Si nanowires does not allow us to claim that this remains true for SiNWs with a hexagonal-phase core, confirming that a new transport model is needed to explain their behavior.

For an ideal Au-SiNW interface, contact resistivity values should be around 5 x 10^{-4} Ωcm^2 [51]. The data from our SiNW devices show that we have observed contact resistivity values in the 1 - 1000 Ωcm^2 range, far exceeding the ideal case. Coupled with calculated η parameter values that differ from 1, this confirms the presence of the oxide layer sandwiched within the contact region causing enhanced Fermi pinning effects.

With the values in Table 4.2, it is possible to remove contact effects from our data and begin extracting channel properties in the following section. The vastly different results found between devices that are expected to be similar could be due to the preparation of the contacts themselves. This must be taken into account when discussing our results and comparing between devices, making rigorous data analysis

important.

4.1.2 Channel Properties: Conductivity, Mobility and Charge Density

Our transport model assumes that the channel is defined as the effective length $L-2\lambda$ of the SiNW placed between the source/drain electrodes. This region of semiconducting material is described by a Fermi level that can be modulated by the gate field (see section 2.4). Understanding the effects of the gate voltage on the current passing through our SB-FETs will allow us to extract the electronic properties of our SiNWs.

All fabricated SiNW SB-FET devices display a weak p-type gate behavior, confirming that the Au particles left inside our SiNWs during growth act as deep acceptors (see section 3.1.3). We quantify the various channel properties by analyzing our SiNW SB-FET transfer data. By extracting threshold voltage V_{th}, subthreshold slope S, transconductance g_m, mobility μ, conductivity σ and hole density p, we will have described the channel properties of our devices.

The maximum value for transconductance is identified as the important g_m parameter, defining the V_G value for the device's ON-state.

The threshold voltage is extracted using a linear extrapolation of the transfer curve at the point where g_m is found at the intersect of the gate voltage axis. Knowledge of the ON-state voltage and V_{th} allows us to calculate the OFF-state voltage as the V_G value of equal but opposite sign overdrive voltage (see section 2.4.3). The ON/OFF ratio can now be defined as the ratio of the ON- and OFF-state current at

the operating bias voltage.

By plotting the transfer curve on a logarithmic scale in the subthreshold gate voltage range (between V_{th} and around half-way to the OFF-state point), the subthreshold slope can be calculated using Eq. 2.8. The value of S will be useful to quantify the gate coupling factor and acts as a measurement of trap states [67].

The measured device resistance depends greatly on the overdrive voltage, as contact resistance depends on the state of the SB [68]. Beyond the threshold value, the hole density in the channel will increase rapidly as the gate voltage increases. This will reduce and thin the SB sufficiently to facilitate hole injection at the contact region and allow the device to enter the linear regime. The value of contact resistance can now be correctly extracted from the data to obtain G_{ch}. Using Eq. 2.14, the final parasitic contact effect can be removed from our data by calculating the correct value for transconductance in the ON-state.

Using Eq. 2.6, the value for gate capacitance C_G is calculated with the effective values for channel length and oxide permittivity. Along with the corrected value for g_m, channel mobility μ can now be calculated using Eq. 2.7. The value for hole mobility is a figure-of-merit for device performance and describes the amount of scattering sources within the SiNW.

The channel conductivity σ (a property of the material acting as the channel in a SB-FET) can be determined assuming uniform current density within the nanowire's cross-section. Finally, with Eq. 2.3, the hole density in the SiNW under study can be found.

Figure 4.3: Channel properties extraction for Devices C1, C2 and C3 (see text for details). (a)-(b) Transfer and transconductance for Device C1. (c)-(d) Transfer and transconductance for Device C2. (e)-(f) Transfer and transconductance for Device C3.
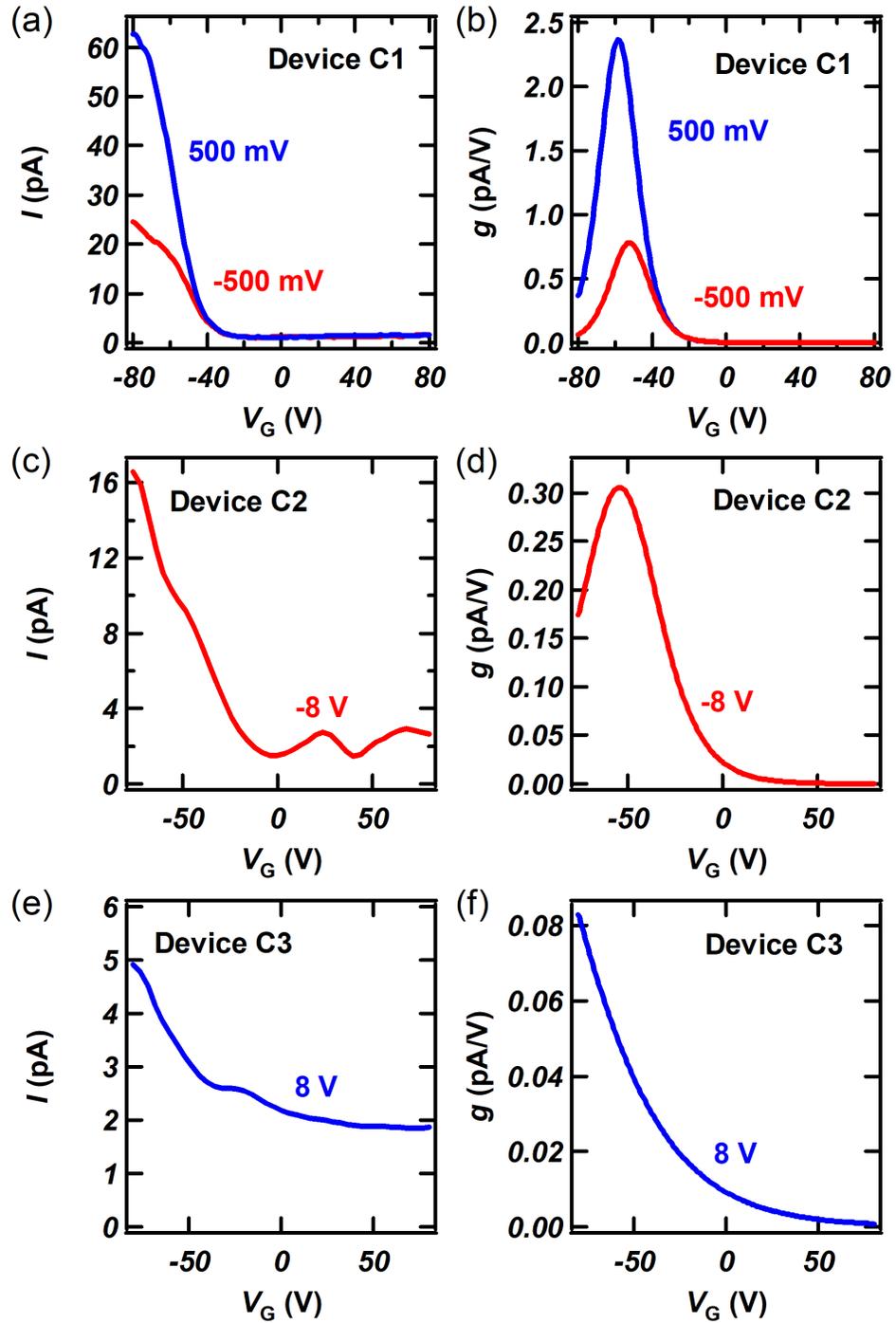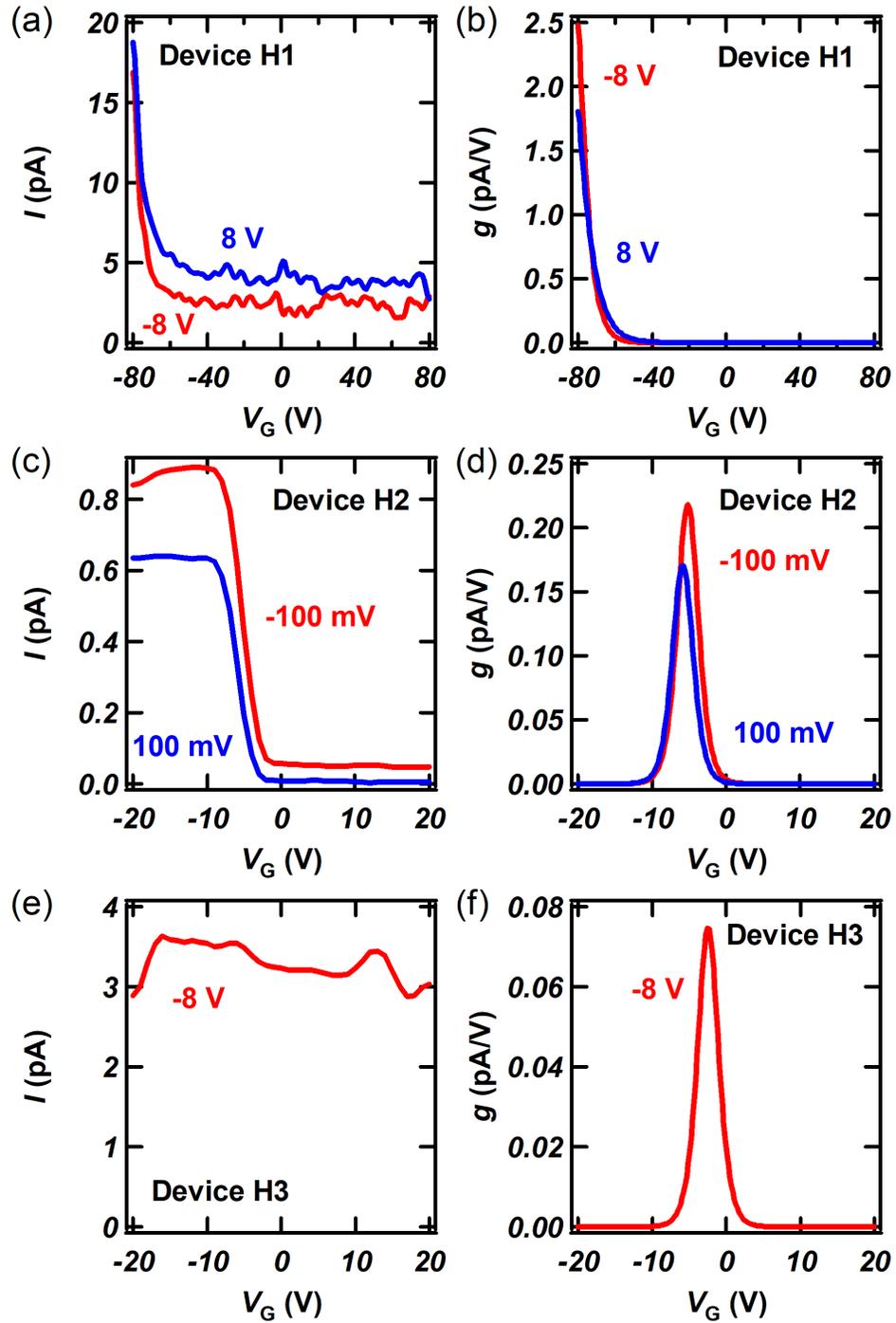
Figure 4.4: Channel properties extraction for Devices H1, H2 and H3 (see text for details). (a)-(b) Transfer and transconductance for Device H1. (c)-(d) Transfer and transconductance for Device H2. (e)-(f) Transfer and transconductance for Device H3.

The transfer data for the three devices made from Cub-Si only SiNWs (C1, C2 and C3) are shown in Fig. 4.3. The left panels have the transfer curves at both high bias values while the right panels have the corresponding transconductance curves. See section 2.4 for details on how to analyze transfer data using our SB-FET transport model.

We notice that all devices are clearly controlled by the gate, illustrating a well-defined p-type SB-FET behavior. In Fig. 4.3(a)-(b), we see how Device C1 has the best gate control behavior, with a transfer curve following the shape of a sigmoid function and a clearly defined single-peak transconductance. The differences between the positive/negative high bias curves are due to the asymmetry between the source/drain contact resistances, showing the importance in removing parasitic contact effects properly from our data. For Device C2 (Fig. 4.3(c)-(d)), large Fermi pinning causes the source contact to dominate the transfer behavior at positive bias, as the current is not modulated by the gate in that bias range, removing these transfer curves from our analysis. For Device C3 (Fig. 4.3(e)-(f)), large Fermi pinning causes the drain contact to dominate the transfer behavior at negative bias. We see that SB-FET devices made from Cub-Si only SiNWs have a transfer behavior that follows well the assumptions of our transport model and are easily characterized.

In contrast, the transfer data for the three devices made from Cub-Si/Hex-Si SiNWs (H1, H2 and H3) shown in Fig. 4.4 were both challenging to obtain and difficult to properly analyze.

We notice that these device have reduced gate control compared to their Cub-Si

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only counterparts, as contacts are dominating the SB-FET device characteristics [3]. A large threshold voltage value and noisy OFF-state currents were found for Device H1 (see Fig. 4.4(a)-(b)), showing the difficulty for the gate field to modulate E_f and illustrating device instability (V_{th} depends on the quality of the oxide layer) [49]. For Devices H2 (see Fig. 4.4(c)-(d)) and H3 (see Fig. 4.4(e)-(f)), the difference between the ON- and OFF- state currents is less than 1 pA, meaning that device switching is subtle. We see that SB-FET devices made from SiNWs with a hexagonal-phase core have a transfer behavior that is difficult to characterize (again, confirming that a new model is needed).

Below is a table summarizing the results from characterizing the channel properties of our SiNW SB-FETs. See section 2.4 for details on how to extract contact parameters from output data using our SB-FET transport model using Device C1 for numerical examples. The reported values are the average of those extracted from both high bias curves, since these parameters should be independent on V_B in the linear regime (SCEs are assumed to not be present). The errors on the presented values in Table 4.3 are 10% on the value rounded to a single significant digit (e.g. 560 means 560 ± 60).

Notice that as a general rule, all our extracted values for mobility and conductivity are significantly lower than the corresponding accepted bulk Si values (see section 2.2.2). This was expected, as undoped SB-FET devices suffer from large resistance, Fermi pinning and increased scattering [3]. For an ideal undoped Si nanowire, the expected value for channel conductivity is 2.5 mS/cm, which is still larger than our

Table 4.3: Channel Parameters of Devices

Device Code	L_{eff} μm	C_G aF	V_{th} V	S V/dec	g_m pA/V	μ 10^{-3} cm^2/Vs	σ μS/cm	p 10^{17} cm^{-3}
C1	1.6	41	-40	28	2.0	4.0	410	7.9
C2	1.6	33	-21	95	0.79	0.10	110	66
C3	3.2	67	-21	32	0.15	0.032	66	130
H1	1.6	42	-71	32	20	2.4	60	2.3
H2	3.2	83	-3.5	3.9	0.20	3.2	120	2.4
H3	2.7	68			0.45	0.080	25	20

extracted values [36]. The differences we find in our measurements to this value are attributed to parasitic contact effects that may still be present despite our efforts to remove them (e.g. fab imperfections, non-applicable assumptions in our contact model), unaccounted effects from the thin oxide layer surrounding our SiNWs, and the Cub-Si/Hex-Si crystal structure.

On average, SB-FET devices made from Cub-Si only SiNWs have a channel conductivity of about 200 μS/cm and a hole density of about 7 x 10^{18} cm^{-3}. Compared to the corresponding values for SB-FETs with SiNWs having OSFs, being 70 μS/cm and 10^{18} cm^{-3}, we see that crystal structure has an effect on the electronic properties of SiNWs, principally by suppressing conductivity. This is in accordance with previous studies on III-V nanowires where the presence of stacking faults was observed to dominate NW conductivity [3, 4].

However, our results indicate that the device behavior of our SiNW SB-FETs deviates from standard FET model predictions. For example, there is a relationship between our extracted values for mobility and subthreshold slope across all devices. A SiNW SB-FET device with better hole mobility also shows a reduced value for S,

but scattering should not affect the subthreshold region of an ideal FET device [48].

This makes it very difficult to compare and discuss our data between various nanowire channels as they are currently presented. This hints that a new model is required to take into account the unique crystal structure found in our SiNWs before making any claims about their channel properties.

How to modify our transport model to account for the Cub-Si/Hex-Si interface is the topic of the next section. With the values in Table 4.3, it will possible to begin defining the channel properties of our SiNWs in relation to their crystal structure.

4.2 Hex-Core Volume Effect on Channel Conductivity

In the previous section, the results obtained from our SiNW SB-FET data were analyzed to obtain values for various contact and channel parameters.

However, upon close inspection of Figs. 4.1 - 4.4 as well as Tables 4.2 - 4.3, it was clear that our data could not perfectly match the predictions of the standard SB-FET model. The very large values for S compared to the ideal 60 mV/dec hinted that the gate electrode was not adequately performing its designed task to control the channel's Fermi level. Extracted hole mobility values were found to be several orders of magnitude smaller than bulk Si values, meaning that our SiNWs suffer from remarkable scattering, even in the ON-state. In addition to values for ϕ_{SB} found much larger than the 0.335 eV value predicted by Mott's relationship, it was

confirmed that contact effects were significant on our devices due to enhanced Fermi pinning, demanding great care in data analysis.

This makes it very challenging to attribute the spread of extracted values to the effects solely arising from the presence of OSFs and the Cub-Si/Hex-Si interface in our SiNWs. However, by using a SB-FET model specifically designed to study the impact of crystal structure on charge transport, it will be possible to use our data as evidence towards our hypothesis.

In this section, we will quantify the impact of the volume of the hexagonal-phase core (created by the OSFs) on the electrical properties (e.g. channel conductivity) of our SiNWs. First, in section 4.2.1, the effects of interface charge traps on nanowire SB-FET data will be presented. These will be used to justify our new hexagonal-phase core (shortened to "Hex-Core") SiNW SB-FET transport model in section 4.2.2, where current is prevented from flowing within the Hex-Core section of the NW channel. Finally, in section 4.2.3, the new assumptions of our device model will be applied on our data to obtain corrected values for our channel parameters. These in turn will be used to draw conclusions on the validity of our model and to give a first description of the electronic properties of our novel material (Hex-Core SiNWs).

4.2.1   Interface Charge Traps

Any interface between two materials will have a certain number of defects, creating local impurities in the crystal lattice. These could occur at the interface between two crystal phases of the same material (creating homostructures), at the interface

between two different semiconductors (creating heterostructures) or at the interface between a semiconductor and an insulator. We will first focus on the last one, as all of our SiNW SB-FET devices include a thin oxide layer surrounding the silicon nanowire.

Created simply by exposure to air, a thin amorphous SiO_2 layer envelops the Si surface of our SiNW, generating dangling bonds and surface roughness. These will place additional states in the Si band gap, acting as charge traps. The free holes in the vicinity of the nanowire surface will become bound charges and will require a large gate field to re-contribute to electrical current [69].

The parameter describing this phenomenon is called the "interface trap density", labeled D_{it}. This value expresses the number of trap states per unit of voltage in a unit of interface surface area. Interface traps play a large role in device physics, as they are primarily responsible for all Fermi pinning effects shown in the electronic data [70]. Including the impact of D_{it} in a SB-FET transport model allows a better understanding of the origins of enhanced Schottky contact effects and reduced gate control.

During the device switching process (see section 2.4.2), the applied gate voltage generates a gate field inside the SiNW, moving the Fermi level towards the valence band edge. The threshold voltage measures the amount of gate voltage necessary to move E_F from its original intrinsic position (near mid-gap for undoped NWs) to exactly the E_V level. For intrinsic bulk Si under ideal SB-FET conditions, a gate voltage of 0.56 V would be necessary to cross half of the band gap. However, as Table

4.3 shows, our SiNW devices only begin switching at much higher voltages, requiring on average well over 30 V to reach the ON-state.

The interface traps on the SiNW surface are responsible for slowing down the gate-induced movement of the channel Fermi level. The energy provided by the gate must be also allocated to releasing holes from these traps, as the band gap is not vacant of any hole states (a change of 1 V on the gate electrode does not change E_F by exactly 1 eV). Since the subthreshold slope characterizes the device switching behavior, the value of S allows us to measure this effect.

Called the "gate coupling factor", labeled α, this device parameter quantifies gate control with the following simple relationship.

$$\Delta E_f = \alpha e \Delta V_G \tag{4.1}$$

The effectiveness of the gate field to control channel conductance is measured by the subthreshold slope [71]. To calculate α in Eq. 4.1, one simply compares the value of S to the ideal thermodynamic value.

$$S = \frac{2.3 k_B T}{e \alpha} \tag{4.2}$$

With a measured value of $S = 30$ V/dec often found in our SiNW SB-FET data, Eq. 4.2 gives a value for $\alpha = 0.002$ far from the ideal case ($\alpha = 1$). We have determined that it would take roughly 500 V applied to the gate electrode to change the Fermi level by only 1 eV. Along with large V_{th} values, this confirms how difficult it is to

tune the conductance of our SiNW SB-FET devices and why we have obtained data showing deviations from standard SB-FET behavior (e.g. significant Fermi pinning effects). The fact that our devices have such small α parameters also explains why we can't observe any n-type behavior at positive gate voltages, since roughly 560 V would be required to cross the entire band gap to reach the conduction band edge (called "inversion") [52].

Especially since our SiNWs are undoped, the large measured values of S is evidence that interface trap states play a significant role in controlling channel hole density using the gate field. This means we have over-estimated the ON-state charge density, as our gate electrode was not performing under normal SB-FET conditions. For Devices C1, C2 and C3, the main interface responsible for hindering gate control is the oxide-SiNW interface on the nanowire surface. This interface is well-studied, and the value of interface trap density is available in literature for various conditions. For our purposes, we will take $eD_{it} = 1.6$ x 10^{-9} F/cm^2 as our accepted value for a SiO$_2$-Si interface [70].

The depleted region at the oxide-nanowire interface acts as a series capacitance, reducing the effective gate capacitance, affecting the calculations of the channel parameters [38]. Called the "interface trap capacitance", labeled C_{it}, it is modeled as a series capacitor placed on the bottom half of the nanowire (the gate field only impacts the bottom of our SiNWs, see section 2.4.1). We can now calculate the effective gate capacitance C_{eff} knowing the dimensions of the SB-FET device using Eqs. 4.3 and 4.4.

$$C_{it} = eD_{it}A_{it} = eD_{it}L_{eff}\pi d/2 \tag{4.3}$$

$$\frac{1}{C_{eff}} = \frac{1}{C_G} + \frac{1}{C_{it}} \tag{4.4}$$

This allows us to adjust the calculated values for hole density in the ON-state and include the effects of the oxide interface trap density on our SiNW SB-FET data. Using Eq. 2.9, we see that the value of p is proportional to gate capacitance in the linear regime, giving us a simple relationship for effective hole density p_{eff}.

$$p_{eff} = p\frac{C_{eff}}{C_G} \tag{4.5}$$

This new value for charge density according to Eq. 4.5 requires us to calculate the oxide-adjusted mobility value μ_{Cub-Si} using Eq. 2.3. With the values in Tables 4.1 and 4.3, we can make a new list of adjusted charge density and mobility values that includes the effects of the oxide interface depletion layer for Devices C1, C2 and C3. The errors on the presented values in Table 4.4 are 10% on the value rounded to a single significant digit (e.g. 560 means 560 ± 60).

Table 4.4: Channel Parameters Including Oxide Trap Effects

Device Code	d nm	C_{it} aF	C_{eff}/C_G	p_{eff} 10^{17} cm^{-3}	μ_{Cub-Si} 10^{-3} cm^2/Vs
C1	50	2.0	0.048	0.37	69
C2	25	0.90	0.030	1.9	3.5
C3	27	2.1	0.031	4.0	1.0

We immediately notice that we have been under-estimating hole mobility in our SiNWs. The true μ_{Cub-Si} values have the appropriate diameter dependence (more Cub-Si volume allows for a better flow of charges) as predicted by the SB-FET model. This also confirms that smaller nanowires have reduced mobility as surface scattering effects are more pronounced as d decreases.

4.2.2 Hex-Core SiNW SB-FET Transport Model

Having a better understanding of our SB-FET devices fabricated with Cub-Si only SiNWs, we can now use our results as insight to comprehend the devices made from SiNWs with OSFs. Here, we present our new transport model for Hex-Core SiNW SB-FETs, and we will show how its assumptions fit well with our data.

Polytype materials are homostructures of several crystal phases of the same chemical composition. The physics of polytype semiconductors is very complex as the various interfaces between crystal structures are not well understood [4]. However, it is generally accepted in literature that polytype channels lead to transport suppression in fabricated FET devices [23].

Since our results in Table 4.3 also suggests that SB-FETs fabricated with Hex-Core SiNWs have signatures of hindered hole transport compared to their Cub-Si counterparts, we propose a new SiNW SB-FET transport model. The principle hypothesis of our model is that the Cub-Si/Hex-Si interface creates a depletion layer preventing current to flow within the OSFs. An inhomogeneous hole density will be responsible for limiting effective transport to solely the cubic-phase shell section

(shortened to "Cub-Shell") of the nanowire.

Fig. 4.5 is a sketch showing the essence of our Hex-Core SiNW SB-FET transport model. In Fig. 4.5(a), the SB-FET transport model presented in Chapter 2 is shown. The modifications needed for our Hex-Core SiNW SB-FET transport model is shown in Fig. 4.5(b). The core section filled with OSFs has a thickness of d_{hex} and covers a cross-sectional area A_{hex}. Using Raman spectroscopy (see section 3.2.3), values for A_{hex} can be determined on each individual SiNW.
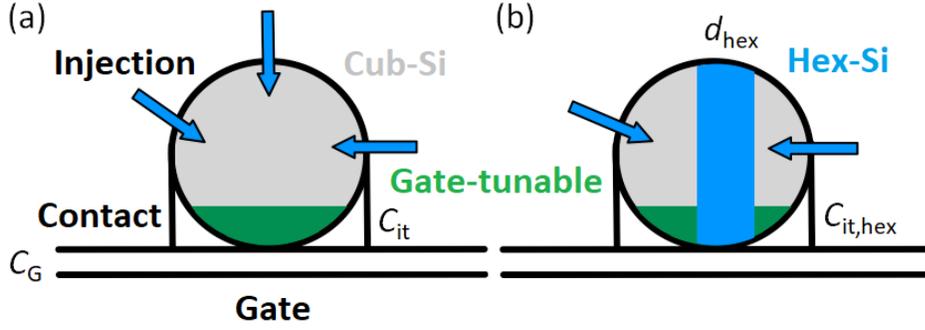
Figure 4.5: Hex-Core SiNW SB-FET Transport Model for current flow within NW channel. (a) Sketch for the transport model of a SB-FET device fabricated using a Cub-Si only SiNW. Cross-section shows circular SiNW on top of the gate dielectric surrounded by a metal electrode in contact with the top half of the NW. Region in green corresponds to the gate tunable channel volume. Blue arrows indicate possible paths for charge injection from the contacts. The current carried by the channel flows through the Cub-Si section in gray. Gate capacitance C_g and interface trap capacitance C_{it} are visualized. (b) Sketch showing model modifications for Hex-Core SiNW devices. Region filled with OSFs in blue of thickness d_{hex} does not permit current flow due to depletion layer formed by the Cub-Si/Hex-Si interface. Hex-Core interface trap capacitance $C_{it,hex}$ is also visualized. This reduces effective gate tunable volume and effective contact injection area.

$$A_{hex} = HexA = Hex\frac{\pi d^2}{4} \tag{4.6}$$

To determine d_{hex}, we assume that the OSFs are perfectly centered within the

nanowire (in reality, the Hex-Core region may be slightly displaced from the middle). Using polar coordinates, an integral can be written to geometrically determine A_{hex}. With Eq. 4.6 and calling $x = d_{hex}/d$, Eq. 4.7 is used to calculate d_{hex} knowing the measured value of Hex.

$$\arcsin \frac{x}{2} + 2x\sqrt{1 - \frac{x^2}{4}} = Hex\frac{\pi}{2} \tag{4.7}$$

The SiNW channel acts as two parallel resistors since current could flow through either the Cub-Shell or the Hex-Core. The channel conductance is then the sum of the Cub-Si section's conductance G_{cub} and the Hex-Si section's conductance G_{hex}. Using Eqs. 4.6 and 2.3, we can write a relationship between channel conductivity and the channel properties of both Si crystal phases.

$$\sigma_{ch} = (1 - Hex)p_{cub}e\mu_{cub} + (Hex)p_{hex}e\mu_{hex} \tag{4.8}$$

For Cub-Si only nanowires, $Hex = 0$ and Eq. 4.8 matches trivially our previous results. For SiNWs with OSFs, however, the Hex ratio will tune conductivity in a very convoluted manner, since the Cub/Hex channel properties (i.e. p_{cub}, μ_{cub}, p_{hex} and μ_{hex}) depend on the effective length scales of the core/shell structure.

Similarly to the oxide-NW interface previously discussed, the Cub-Si/Hex-Si interface will also generate interface traps. These will further affect the channel hole density and the effective gate coupling. Mobility and charge density already depend on position due to the oxide layer, as both are lower near the nanowire surface [72].

It is already known in III-V polytypes that charge density in the WZ section is lower than in the ZB section, greatly affecting the NW's electronic properties [4]. Our polytype silicon nanowires will also have $p_{hex} < p_{cub}$, and a depletion layer will be formed at the Cub-Si/Hex-Si interface (see section 2.6.1).

To correspond Eq. 4.8 with our working hypothesis, our transport model assumes that this additional depletion layer is wide enough to include the entire nanowire region of OSFs so that $p_{hex} = 0$. Our measured *Hex* values across all cataloged SiNWs are always lower than 0.4, meaning that we have not observed a SiNW having OSFs of considerable volume.

$$\sigma_{ch} = (1 - Hex)p_{eff}e\mu_{cub} \qquad (4.9)$$

This new equation for channel conductivity includes our three adjustments to the standard SB-FET transport model. The "1-*Hex*" term corresponds to the reduced SiNW cross-section allowing charge flow, as free holes are pushed away from the Hex-Core. The corrected value for p_{eff} includes the effects of all interface traps reducing gate control. Finally, only the mobility of the Cub-Shell region is relevant on Hex-Core SiNW SB-FET device measurements. To use Eq. 4.9 on Devices H1, H2 and H3, we need to determine the individual p_{eff} and μ_{cub} values for each of these devices fabricated using SiNWs with OSFs as the channel material.

Much like the oxide layer interface, the Cub-Si/Hex-Si interface generates additional hole trap states within the band gap. Just as we have previously modeled

the oxide depletion layer as a series capacitance, we will further reduce the effective gate capacitance of a Hex-Core SiNW SB-FET device by adding a new series capacitance in the presence of OSFs. Called the "Hex-Core interface trap capacitance", labeled $C_{it,hex}$, it is modeled as a second series capacitor placed on the bottom of the Hex-Core region (on top of the oxide layer interface). Assuming a simple rectangular interface area, we can now calculate the effective gate capacitance C_{eff} knowing the dimensions of the Hex-Core SiNW SB-FET device using Eqs. 4.10 and 4.11. We will continue to take $eD_{it} = 1.6$ x 10^{-9} F/cm^2 as our accepted value for all Si interfaces.

$$C_{it,hex} = eD_{it}A_{it,hex} = eD_{it}L_{eff}d_{hex} \tag{4.10}$$

$$\frac{1}{C_{eff}} = \frac{1}{C_G} + \frac{1}{C_{it}} + \frac{1}{C_{it,hex}} \tag{4.11}$$

Using Eq. 2.9, we correct the calculated values for hole density in the ON-state and include the effects of both the oxide and the crystal structure interface trap densities on our Hex-Core SiNW SB-FET data.

We now require a value for the oxide-adjusted mobility value μ_{Cub-Si} in order to calculate conductivity. As current only flows in the Cub-Shell section of the nanowire, the effective diameter of the channel is reduced from its true geometrical value d. Assuming a *Hex* value around 0.3, with Eq. 4.7 we can calculate a d_{hex} value of around 10 nm for a $d = 50$ nm nanowire. This means that the SiNW is cut into two Cub-Shell semi circular sections with length scales close to 20 nm. Since Devices C2

and C3 resemble our Hex-Core SiNW in terms of channel dimensions (Device C1 is the only true "50 nm diameter" SiNW channel), we will use a common μ_{Cub-Si} value for Devices H1, H2 and H3 as the average of the C2 and C3 values, giving 2.3 x 10^{-3} cm^2/Vs (see Table 4.4). This satisfies the model's prediction that mobility decreases as diameter decreases, since surface scattering effects dominate transport in undoped NWs [36, 73].

4.2.3   Channel Properties of Hex-Core SiNWs

By applying our new transport model on our data, we can now adjust the calculated results from Table 4.3 for Devices H1, H2 and H3. The errors on the presented values in Table 4.5 are 10% on the value rounded to a single significant digit (e.g. 560 means 560 ± 60).

Table 4.5: Hex-Core Channel Parameters Including Interface Effects

Device Code	Hex	d_{hex} nm	C_{eff}/C_G	p_{eff} 10^{17} cm^{-3}	σ μS/cm
H1	0.31	11	0.0060	0.014	0.34
H2	0.15	5.0	0.0029	0.0071	0.22
H3	0.36	11	0.0062	0.12	2.8

These corrected values for p_{eff} and σ allow us to compare our results across all six analyzed devices in this chapter. To facilitate our discussion, Fig. 4.6 shows the distribution of the extracted key transport parameters for Devices C1, C2, C3, H1, H2 and H3 according to their corresponding *Hex* value.

Immediately we notice the correct trends in channel and contact parameters in terms of what the raw data (see Fig. 4.1 - 4.4) was suggesting. In Fig. 4.6(a),
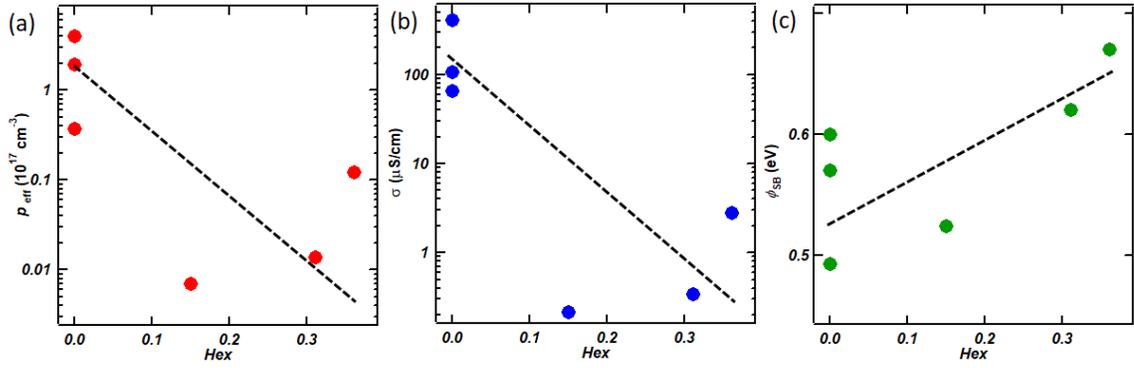
125

Figure 4.6: Graphs summarizing our results on extracted transport parameters for our SiNW SB-FETs. Horizontal axis is *Hex* parameter describing the crystal structure of the corresponding device's SiNW channel. Black dotted lines are guides-to-the-eye to visualize trends. (a) Effective channel hole density in Cub-Shell section. (b) Channel conductivity, showing how the presence of the Hex-Core can reduce SiNW conductivity by several orders of magnitude. (c) Average Schottky Barrier height over source/drain contacts, showing how large OSF volume can prevent hole injection from contacts.

we see how effective channel hole density decreases in Hex-Core SiNWs. In Fig. 4.6(b), we see how conductivity is suppressed in channels containing Hex-Si in the core region. In Fig. 4.6(c), SBs are seen to be pronounced when *Hex* becomes large. Note that the variations found within the results are not due to measurement error, but by the differences between individual SiNW channels in terms of their dimensions (diameter and length), their surface oxide layer (thickness and roughness) and the exact structure (position, crystal phase and orientation) in terms of their OSFs (see sections 2.4 through 2.6 for details). However, we will discuss in Chapter 5 how we are able to remove all of these confounding factors and compare the effects of OSFs on channel conductivity in a single device (see Table 5.3).

On average, Cub-Si only SiNW SB-FETs have a channel conductivity of around 200 μS/cm, while the Hex-Core SiNW SB-FET devices have an average of around 1

μS/cm. The observed scatter of values around the averages is due to the enhanced surface scattering effects in undoped NWs causing large device variations [34]. Our results show that the conductivity of a SiNW can be suppressed by several orders of magnitude by adding OSFs and modulating their relative density, confirming the working hypothesis of our new transport model that current flows predominantly in the cubic region. This means that tuning crystal structure by using homostructures can be used as an efficient degree of freedom to control a material's electronic properties (similar to using heterostructures or doping).

As the weak p-type behavior comes from deep level acceptor Au states left during the growth process, most of the gate-induced charge density in our otherwise undoped SiNWs comes from surface trap states [43]. The low values found for p_{eff} confirm that charge traps at the polytype interface affect the electronic properties of our SiNWs by reducing effective gate control [3]. Similar to the results found in group III-V nanowires, we have observed that polytype SiNWs create devices with higher resistance values than their Cub-Si only counterparts [4]. We must be careful, however, when comparing our devices to those found in literature, as most research groups control the value of charge density directly by doping the semiconductor, which leads them to report much larger values for mobility and conductivity.

The contact properties of our SiNW SB-FETs further prove our Hex-Core transport model. It is predicted that contact resistance increases exponentially as charge density decreases [43]. The additional depletion regions created by both the oxide

layer and the Cub-Si/Hex-Si interface near the contact region enhance all Fermi pinning effects, causing the SB-FET to deviate from standard FET behavior [34, 74]. It is found that Schottky Contacts formed on a SiNW with OSFs are typically more pronounced, as the depleted Hex-Core prevents normal hole injection from the contact.

To conclude this chapter, we will summarize our key findings. The output and transfer data from our devices have shown that Hex-Core SiNW SB-FETs have reduced gate tunability and contact injection compared to the Cub-Si only SiNW SB-FETs. When accounting for oxide and polytype interfaces, the Hex-Core reduces effective charge density and conductivity by several orders of magnitude. As current flow is modeled to be restricted to the Cub-Shell section of the nanowire (see Fig. 4.5), the *Hex* parameter allows us to modulate the effective channel cross-section without changing the actual size of the device. Controlling OSFs within a SiNW is shown to be a new degree of freedom to engineer devices with specific electronic properties.

Chapter 5

Intrinsic SiNW Homojunction Rectifiers

In this chapter, we demonstrate how homojunctions between Cub-Si NWs and Hex-Core SiNWs form high-quality rectifying devices. By analyzing the electronic data acquired from output and transfer sweeps on these devices, we will be able to have an even deeper insight of the physics governing the effects of OSFs on transport properties of SiNWs. The success of our kinked SiNW SB-FET model will also be used as further experimental evidence of the claims made in the previous chapter.

The first section deals with a description of crystal phase homojunctions and present theoretical predictions on the rectifying behavior of kinked SiNWs. The final section will present the analysis method applied on our output and transfer curves measured at various temperatures to extract all meaningful contact and channel properties. We will conclude on how the kink region itself makes kinked SiNW SB-FETs

excellent tunable rectifiers.

5.1 Kinked SiNW FET Devices

Rarely, a kinked SiNW, a nanowire that does not follow a straight line, is found scattered on our samples. When a high density of OSFs are created during the VLS growth process, the SiNW will often kink to a new growth direction (see section 3.1.3). With Raman spectroscopy, we have confirmed that kinked SiNWs are made of a Cub-Si only portion and a Hex-Core portion separated on both sides of the kink (see section 3.2.3). Fabricating a SB-FET device using these kinked SiNWs will allow us to further study the Cub-Si/Hex-Si interface, as the kink acts as a way to connect a Cub-Si only channel to a Hex-Core channel.

Called kinked SiNW SB-FETs, these devices formed with a novel material (a SiNW with variable OSF density along its length) exploit the various electronic properties of both phases of Si within a single channel. The transport data acquired from these devices suggest that kinked SiNW SB-FETs not only behave as the sum of the properties of both parts, but the kink itself acts as a homojunction (a crystal structure changing from Cub-Si only to Hex-Core when crossing the kink region) creating additional unique properties. It is found that kinked SiNW SB-FETs exhibit excellent rectifying behavior as the homojunction acts as a tunable diode.

In this section, we will define the kink region and quantify its impact on the electrical properties (e.g. conductivity and mobility) of our SiNWs. First, the structure

of the Cub-Only/Hex-Core homojunction will be presented. Then, the kinked SiNW SB-FET transport model is described, giving us the theoretical background needed before showing and analyzing our data.

5.1.1 Cub-Only/Hex-Core Homojunction

At the point during the VLS growth process where a high OSF density is being introduced, SiNWs will often kink (see section 3.1.3). By observing the nanowire growth direction changing, this gives us visual confirmation that the crystal structure has been modified at the kink region. Preparing SiNWs with such controlled and non-uniform OSFs is but one example of the various possibilities offered by VLS growth [1].

The kink region is defined by the length of the SiNW where the *Hex* parameter and the growth direction vary. It is the nanowire volume where crystal structure transitions from a Cub-Si only (shortened to "Cub-Only") portion to a Hex-Core portion. The diameter of the nanowire does not change through the kink.

Several factors complicate the study of the Cub-Only/Hex-Core homojunction [47]. Additional interface trap states are generated at the Cub-Only/Hex-Core interface as the sudden introduction of OSFs create stress-induced lattice defects and boundary roughness. As the results from our experiments on simple Cub-Only or Hex-Core SiNW SB-FETs have shown (see section 4.2.3), the charge density of a Cub-Only SiNW is larger than that of a Hex-Core SiNW due to the depletion layer caused by the Cub-Si/Hex-Si interface.

As discussed previously (see section 2.6.1), the trap states at the Cub-Only/Hex-Core interface will cause a change in charge density, creating a depletion layer at the homojunction. The kink region's electronic properties are dictated by the state of the "kink depletion layer". Similarly to the one under the contact region causing the SB, the kink depletion layer will also be tunable by modulating the bias and gate voltage. By taking output and transfer measurements on kinked SiNW SB-FETs, we will be able to characterize the kink region.

Finally, knowledge of the homojunction band structure will be useful to understand the acquired data. The homojunction will be characterized by a valence band offset according to Eq. 2.20 since the homojunction acts as a "p^+-p" interface [4].

5.1.2   Kinked SiNW SB-FET Transport Model

We present the transport model applied to analyze the data acquired from kinked SiNW SB-FETs. It is a modified version of the transport model already presented in Chapter 4. The measurement process of these devices is shown in the next section.

A kinked SiNW SB-FET device is described by a channel comprised of two portions acting as two series resistors and a homojunction between them (see Fig. 5.1). The total channel length L is the sum of the Cub-Only portion of length L_c and a Hex-Core portion L_h. The source electrode is placed on the Cub-Only SiNW portion, and the drain electrode is on the Hex-Core portion. The back-gate electrode under $t_{ox} = 300$ nm of oxide creates a gate field on the entire kinked SiNW length.

Many of the contact and channel properties determined from the previous chapter
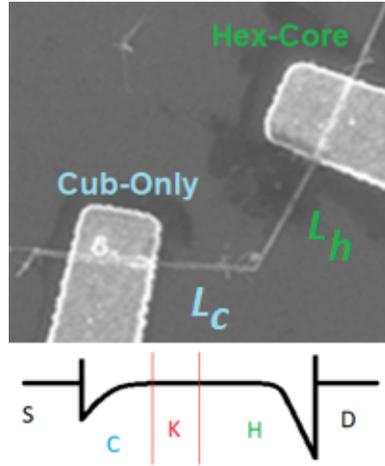
Figure 5.1: SEM image of a kinked SiNW SB-FET device. The Cub-Only and Hex-Core portions are identified at their respective contact electrodes. Inset shows valence band edge across the device in the flat-band voltage condition. The source "S" and drain "D" contact band bending regions are respectively at both ends of the Cub-Only "C" and Hex-Core "H" portions of the SiNW. The kink "K" region is defined between both red lines (size of kink region is exaggerated for illustrative purposes).

will also characterize kinked SiNW SB-FET devices. Since the two channels are in series, it is expected that kinked SiNW channels will offer high device resistance values as channel conductance will be limited by the Hex-Core portion. However, the control on device resistance from the gate will be due to charge density modulations in the Cub-Only portion (see section 4.2.3). The channel properties of the Hex-Core portion are completely independent of V_G.

We also expect large contact asymmetry in kinked SiNW SB-FETs. We have already determined (see section 4.1.1) that the contact region in Hex-Core SiNWs are characterized by higher ϕ_{SB} values, causing enhanced Fermi pinning effects compared to the Cub-Only contact region [1]. The asymmetry ratio δ, being the ratio of the SB heights between both contacts, is very large for kinked SiNW SB-FETs (see section 2.6.2). The device essentially acts as a Schottky diode, exhibiting strong rectifying

output behavior [33].

The kink region, however, will be the source of additional rectifying behavior. In series with both Cub-Only and Hex-Core SiNW resistors is a homojunction. This p$^+$-p interface will form a depletion layer acting as a "kink diode", generating a rectifier within the channel accompanying the Schottky diode from the contacts. Since we have found in Chapter 4 that the current cannot flow through the OSF volume, we will assume that the kink region has a length scale similar to the value of d_{hex} centered on the homojunction covering the entire nanowire cross-section. It is in this p$^+$-p depletion layer volume that band bending is present, creating an energy barrier of height ΔE_V called the "kink barrier".

This channel asymmetry means that the direction of current flow will affect the acquired data. It will be harder for holes to flow from the source to the drain electrode, as the effective cross-section of the SiNW decreases when crossing the homojunction from the Cub-Only side to the Hex-Core side. However, current flowing from the drain to the source will be unaffected by the Cub-Only/Hex-Core interface, as there will be no energy barrier preventing injection in this case.

By modulating the gate voltage, we can study the kink region band bending and extract all relevant parameters. Since we have determined that the Fermi level can be affected by the gate solely on the Cub-Only portion, only the hole density value on that side of the interface can be tuned. Using Eq. 2.20, we see that the kink barrier's height can be modified with V_G. With higher negative values of applied gate voltage, the value of p^+ will get larger, which will both increase the Cub-Only channel

conductivity and enhance the kink barrier. With positive gate voltages, the Cub-Only portion will pinch-off, eventually inverting the kink barrier (negative value for ΔE_V). The value for V_G where the valence band is equal throughout the homojunction (ΔE_V = 0) is called the "flat-band voltage".

By varying the signs of both the high bias and high gate voltages, different asymmetries in the band structures are created, allowing us to properly study both the Schottky diode and the kink diode separately [51]. Finally, another tool to study energy barriers is changing the temperature of the kinked SiNW SB-FET device. Measuring the injection currents for different values of T will give us further insight on the formation of the homojunction energy barrier and a method to quantify ΔE_V.

5.2   Rectifying Behavior in Kinked SiNWs

Now that our novel transport model for kinked SiNW SB-FETs is established, we are ready to test its predictions on acquired data. With the adjusted equations developed in the previous chapter, we will be ready to properly analyze our measurements and confirm our understanding of the Cub-Only/Hex-Core homojunction. We will also characterize the rectifying behavior of these new devices and show how crystal structure control could be a viable pathway to engineer excellent rectifiers.

In this section, the data obtained from the $I - V_B - V_G$ sweeps of the kinked SiNW SB-FET devices are presented. First, the fabrication and crystal structure characterization of the devices are shown, including a new device list. The output and

transfer data are also displayed to give context to our analysis. Next, the extraction of all relevant contact and channel properties is presented between the metal electrodes and our kinked SiNWs. The discussion of these results will follow, showing how our kinked SiNW SB-FET rectifiers can be tuned by both temperature and gate voltage. Then, the concept of channel asymmetry assumed in our transport model is applied on the rectifier data to extract the kink barrier height. Finally, the set of all acquired results from this section is used to draw conclusions on the validity of the kinked SiNW SB-FET model as well as confirming our assumptions on the impact of OSFs on SiNW electronic transport from the previous chapter.

5.2.1   Characterization of Kinked SiNWs

On the Hex-Core SiNW source chip, a large number of nanowires should be kinked, especially those with a high volume of OSFs. However, the scattering process (scratching and sonication) will break almost all kinked SiNWs at the kink itself. Finding a suitable kinked SiNW for device fabrication on our samples is extremely difficult, as they rather become two smaller straight NWs (one Cub-Only and the other Hex-Core).

On the very rare chance that on kinked SiNW is found on the chip surface, Raman spectroscopy (see section 3.2.3) confirms that the value of *Hex* differs drastically from one side of the kink to the other. The side "before" the kink with $Hex = 0$ is denoted the Cub-Only portion. The side "after" the kink (where OSF formation is complete) is the Hex-Core portion with a uniform non-zero *Hex* value along its length (see Fig.
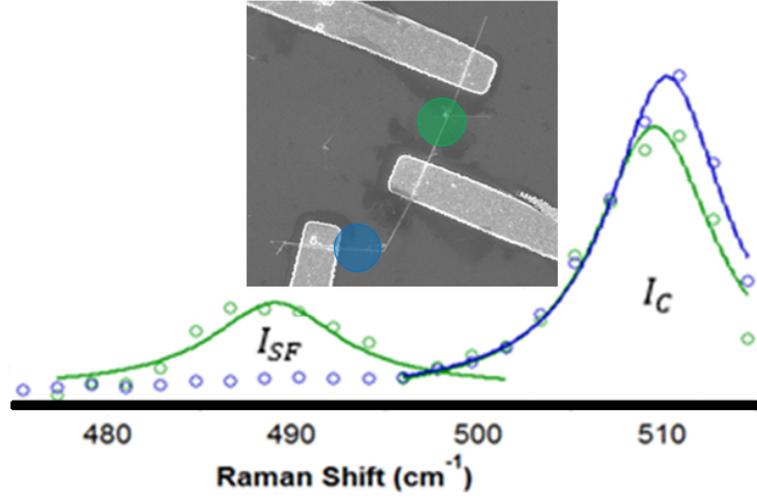
5.2).

Figure 5.2: Raman data of a kinked SiNW showing how *Hex* value changes from one side of the kink to the other. Points in blue describes the Cub-Only portion of the SiNW before the kink. Points in green, taken at a point after the kink, shows the presence of OSFs in the Hex-Core portion. Curves show fits on their respective peaks. Inset shows SEM image of a kinked SiNW SB-FET device. Locations of acquired Raman scans are shown in blue and green circles, corresponding to the blue and green Raman data.

During the course of our work, only two kinked SiNWs were found and characterized. The fab process (see section 3.3) was performed to obtain two kinked SiNW SB-FET devices. The following table is a list of the relevant device parameters describing the two kinked SiNW SB-FETs that will be presented in this chapter. Their respective device names are K1 and K2. The error on the presented values in Table 5.1 are on the final significant digit (e.g. 2.0 means 2.0 ± 0.1).

Table 5.1: Dimensions and Crystal Parameters of Kinked Devices

Device Code	L_c μm	L_h μm	d nm	$L_{con,s}$ μm	$L_{con,d}$ μm	Hex
K1	0.6	1.4	49	1.5	1.5	0/0.36
K2	3.0	3.0	50	5.0	3.0	0/0.27

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5.2.2 Temperature- and Gate-Tunable Rectifiers

We now present the transport data obtained from our kinked SiNW SB-FET devices. In this section, the data presented is the result of having the source electrode placed on the Cub-Only portion of the device. The analysis necessary to extract relevant contact and channel parameters largely follows the same steps as those discussed already in Chapter 4 (specifically, see section 4.1 for any additional details).

The output data for the two devices made from kinked SiNWs are shown in Fig. 5.3. Device K1 is shown in Fig. 5.3(a)-(b), and Device K2 is shown in Fig. 5.3(c)-(d). As predicted by our kinked SiNW SB-FET transport model, large non-linear behavior is found in our acquired output curves. Significant contact effects (see section 2.5.2) are present in our data, especially from the drain electrode covering the Hex-Core portion of both nanowires. When negative bias voltages are applied to the devices, the large resistance barrier regime provides qualitative evidence of hindered hole injection at the drain Schottky barriers.

For positive bias voltages, we see that the devices can be controlled by the gate in the linear regime, especially for Device K1. Large Fermi pinning seems to prevent Device K2 from exhibiting typical SB-FET behavior, as the current only changes by sub-pA values despite large ΔV_G values during device switching.

For Device K1, only the source electrode's SB height could be confidently extracted, giving $\phi^s_{SB} = 0.576$ eV with a contact quality of $\eta = 7.81$. The Hex-Core contact barrier is assumed too large to quantify properly using our setup. For Device
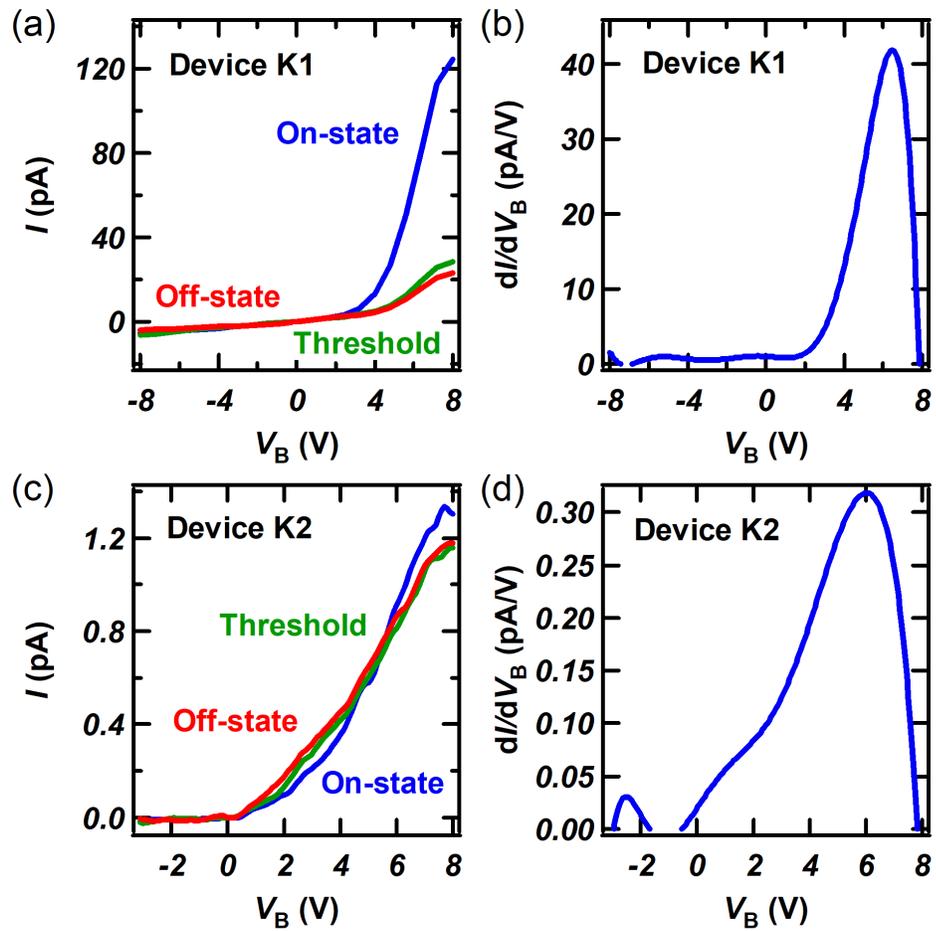
Figure 5.3: Rectifying properties extraction for Devices K1 and K2 (see text for details). Source electrode is on the Cub-Only portion of the device. (a)-(b) Output and differential conductance for Device K1. (c)-(d) Output and differential conductance for Device K2.

K2, the Cub-Only SB height is $\phi_{SB}^{s} = 0.47$ eV while the Hex-Core portion is characterized by $\phi_{SB}^{d} = 0.71$ eV with a quality of $\eta = 4.41$. We have confirmed here the large contact asymmetry $\delta = 1.51$ predicted by our transport model to be the cause of the observed rectifying behavior of our kinked SiNW SB-FETs.

The channel parameters can now be extracted to characterize the kinked SiNW itself. Since our transport model dictates that only the Cub-Only portion of the nanowire is tunable by the gate, the effective length of the device is taken as the value of $L_c - 2\lambda$ (the Hex-Core portion is modeled as a simple resistor).

The transfer data for the two devices made from kinked SiNWs are shown in Fig. 5.4. Device K1 is shown in Fig. 5.4(a)-(b), and Device K2 is shown in Fig. 5.4(c)-(d). Both devices exhibit p-type SB-FET behavior. The current through Device K1 increases rapidly in a small gate window, while Device K2 only switches out of its OFF-state at large gate voltages (roughly around -60 V).

Below is a table summarizing the results from characterizing the channel properties of our kinked SiNW SB-FETs. All known parasitic contact effects (see section 2.5.2) have been accounted for when calculating these reported values. The errors on the presented values in Table 5.2 are 10% on the value rounded to a single significant digit (e.g. 560 means 560 ± 60).

Table 5.2: Transport Parameters of Homojunction Rectifiers

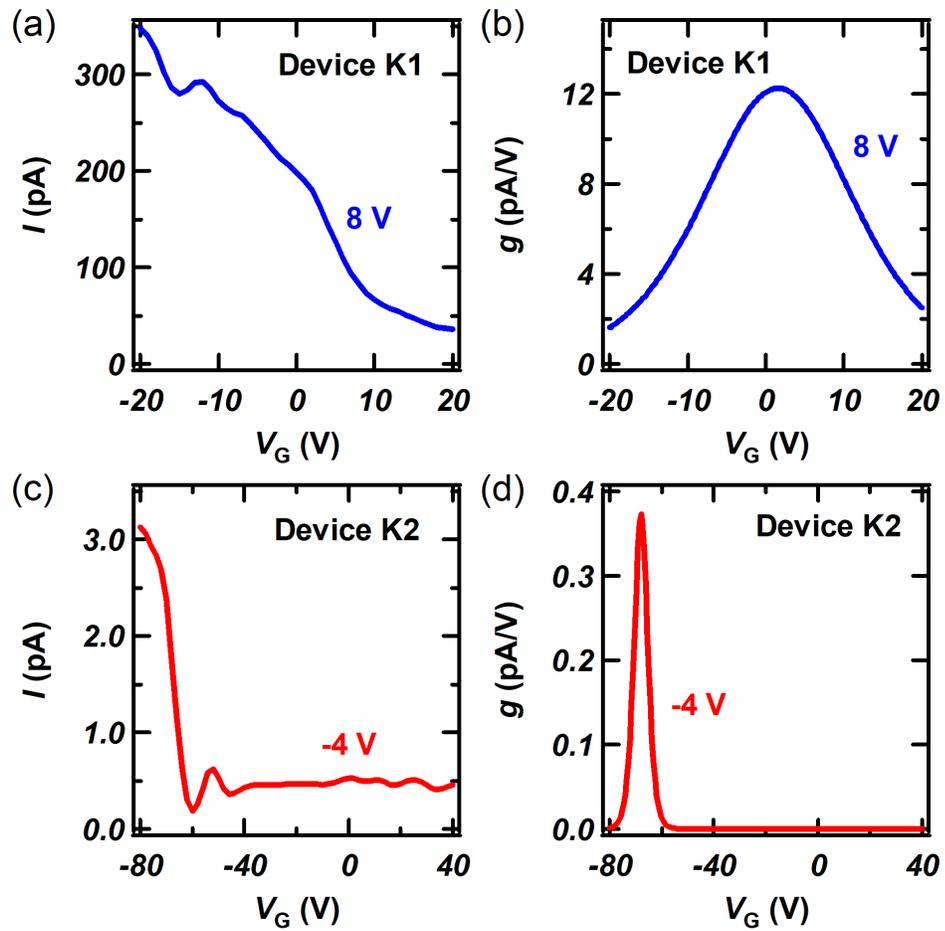| Device Code	L_{eff} μm	R_{ch}^{s} GΩ	R_{ch}^{d} GΩ	ON/OFF	S V/dec	g_m pA/V	σ μS/cm	p 10^{17} cm^{-3}
K1	0.23	24	650	5.1	35	120	51	0.33
K2	2.6	3100	33000	7.2	7.9	2.8	4.3	0.28

Figure 5.4: FET properties extraction for Devices K1 and K2 (see text for details). Source electrode is on the Cub-Only portion of the device. (a)-(b) Transfer and transconductance for Device K1. (c)-(d) Transfer and transconductance for Device K2.

Notice that kinked SiNWs have very large channel resistance values (even exceeding 30 TΩ in Device K2) due to small effective charge carrier concentrations and the presence of the Hex-Core portion of the nanowire. More importantly, however, we see that channel parameters depend greatly on the direction of current flow. By changing the sign of V_B, channel resistance can vary by over an order of magnitude, confirming the Schottky diode behavior of our kinked SiNW SB-FETs (see section 2.6.2).

The parameter characterizing a Schottky diode is the rectifying ratio, labeled r and defined in Eq. 2.23. The measured current when the device is operating in the forward-bias mode is called the "forward-current". The current in the reverse-bias mode, "reverse-current", is sometimes also called the "leak current". The ratio of the forward- to reverse-current is used as the figure-of-merit for a rectifier device. A large forward-current and a small reverse-current is desired when fabricating rectifiers to reach values of r that exceed 10.

For our Schottky diodes, the forward-current is observed at positive bias voltages when the current flow direction is from the Cub-Only contact electrode to the Hex-Core portion. The reverse-currents of our kinked SiNW SB-FETs are very small (in the fA range) and robust as they are relatively constant for any applied gate voltages. Since the forward-current can be modulated by applying a gate voltage, the rectifying ratio can be efficiently tuned with V_G. For Device K1, when operating at 8 V, the value of r can be modified from 10 to 100, depending on the sign of V_G.

The large tunability of the rectifying behavior of our devices confirms the transport model of our kinked SiNW SB-FETs. When negative gate voltages are applied, the

charge density of the Cub-Only portion increases, which effectively reduces the SB by thinning the depletion layer at the source contact region (see section 2.6.1). However, the leak current is not affected by V_G, showing that neither the charge density nor the SB of the Hex-Core portion can be effectively tuned by the gate. By applying large gate voltages, the contact asymmetry of the SB-FET device increases, which enhances the Schottky diode's rectifying behavior.

Another method to control a semiconductor's intrinsic charge density is by changing the temperature. The maximum attainable current that can be carried by a semiconductor channel is limited by the operating temperature of the device [35]. By heating the sample, additional charge carriers will thermalize and be available to carry current. By cooling the sample, the charges will "freeze" as the band gap will become much larger than the thermal energy, forcing the holes to be bound in various trap states. Undoped NWs will have very low conductivity vales below room temperature, giving SB-FET devices very low currents as the values for ϕ_{SB} will be much larger than $k_B T$ in this case [3].

For our kinked SiNW SB-FETs, we see in Fig. 5.5 that heating the samples during our measurements increases the rectifying ratio, reaching almost 300 for Device K1 when also applying negative gate voltage. By increasing the temperature, thermally-assisted holes can easily surpass the source SB, but the drain injection rate remains relatively unchanged as the OSFs keep the charge carriers trapped in the Hex-Core contact region. By cooling down K1, the undoped SiNW is depleted of available charges on both sides of the channel which reduces the asymmetry of the device. The

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rectifying behavior is even lost completely at positive gate voltages where $r = 1$.
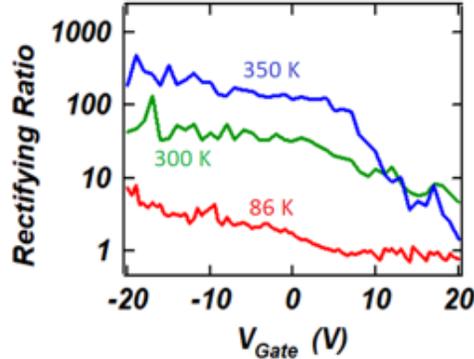

Figure 5.5: Temperature- and gate-tunable rectifying ratio of 1 to 300 for Device K1. Applying gate voltages changes the value of r by modulating the SB height of the source contact. The rectifying behavior is enhanced when the charge density of the Cub-Only portion increases. This can be done by either applying a large negative gate voltage or by heating the device. Curves are labeled with their corresponding values for T.

5.2.3 Channel Asymmetry and Rectification of Homojunctions

We have shown that contact asymmetry is largely responsible for the rectifying behavior found in our kinked SiNW SB-FET devices. However, even after removing all contact effects, there remains asymmetry found in the output data. This means that another source for rectifying behavior must be present within the channel. The structure responsible for this channel asymmetry is the crystal homojunction in the kink region, as predicted by our transport model (see section 5.1.2).

To probe the channel asymmetry, the transport data for Device K1 was acquired twice. On the first run, the source electrode was taken to be the Cub-Only portion

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while the drain electrode was on the Hex-Core contact. This meant that the forward-bias mode was for positive V_B values. On the second run, the source/drain electrodes were switched (i.e. source on Hex-Core), giving negative forward-currents at negative bias.

For a SB-FET device with a symmetrical channel, the value of both forward-currents (in absolute value) before and after switching the electrodes is the same. However, as can be seen in Fig. 5.6, reversing the direction of current flow on kinked SiNW SB-FETs does not give the same output result. The measured forward-bias mode channel resistance is not identical, which is the signature of a preferred direction for current flow. This is evidence of channel asymmetry which must be caused by the kink itself, confirming our model's assumptions on how OSFs affect hole transport.
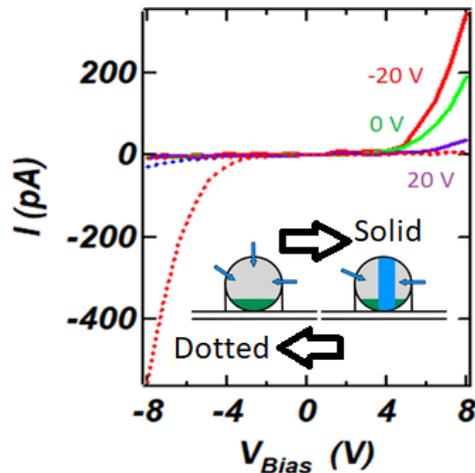
Figure 5.6: Channel asymmetry for Device K1 showing kink effect. Solid lines show output curves when the source electrode is on the Cub-Only portion of the device. Dotted lines show the same output curves when the Hex-Core portion acts as the source contact. Switching the electrodes affects forward-currents, as direction of current flow is important due to the kink barrier. Gate tunability is illustrated by color (red for gate voltage of -20 V, green for 0 V and purple for 20 V). Inset shows sketch depicting our transport model for illustrative purposes (see Fig. 4.5).

The crystal homojunction acts as a diode, described by a barrier of height ΔE_V. To quantify the effect of the kink barrier, the temperature dependence on channel asymmetry will be analyzed at various gate voltages. Using Eq. 2.17, we see that the current passing through a depletion layer can be modulated by changing T.

The difference in forward-currents before and after source/drain switching is labeled ΔI. Since for a symmetrical channel, $\Delta I = 0$, this value characterizes the channel asymmetry caused by the kink diode. To extract the kink barrier height, the following relationship is used (where C is a device-specific constant that is not needed).

$$\ln(\Delta I / T^2) = C - \Delta E_V / k_B T \tag{5.1}$$

By forming an Arrhenius plot (a graph of the $\ln(\Delta I / T^2)$ on the y-axis and $1/k_B T$ on the x-axis) at various gate voltages, the corresponding value of ΔE_V is calculated with Eq. 5.1 as the negative of the slope of a linear fit on our data points [4, 48]. An example is shown in Fig. 5.7(a).

The results of this analysis are shown in Fig. 5.7(b). We notice immediately that the kink barrier is tunable by the gate. This shows that the Fermi level of the Cub-Only portion can be modulated but not the Hex-Core portion. If both could be easily moved with gate voltage, then a rigid shift of the valence band would occur and the kink barrier would remain unchanged. Our data is evidence to the contrary, confirming our transport model's hypothesis.
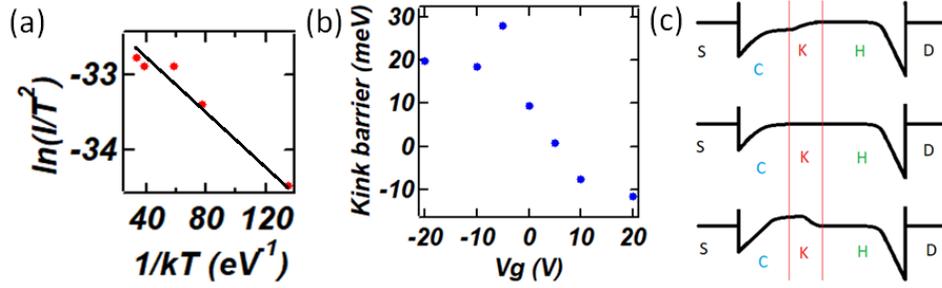
Figure 5.7: Kink barrier extraction for Device K1. (a) Arrhenius plot obtained at $V_G = $ -20 V. The slope of the linear fit quantifies the height of the kink barrier. (b) Gate-tunability of the kink barrier, showing how the homojunction can be modulated and confirming our transport model. Flat-band voltage is found near $V_G = $ 5 V. (c) Valence band edge across the device at gate voltage values above (top sketch) and below (bottom) the flat-band voltage (middle). Kink barrier in the kink region "K" can be modulated by changing the Fermi level of the Cub-Only portion.

The flat-band voltage is found to be near 5 V where $\Delta E_V = 0$. By slightly depleting the Cub-Only portion, the depletion layer at the homojunction is removed. This confirms that the Hex-Core portion has a lower charge density value than the Cub-Only portion due to the presence of OSFs (see section 4.2.2). By increasing V_G even further, we are able to cause inversion at the kink region, switching the direction of the kink band bending (see Fig. 5.7(c)).

In the ON-state, the value of ΔE_V is 10 meV. Using Eq. 2.20, this allows us to quantify the value of the Hex-Core portion knowing the measured value of p. This in turn allows us to adjust the calculated values for hole density in the ON-state and include the effects of the oxide interface trap density on our kinked SiNW SB-FET data (see section 4.2.1). The following table summarizes our results (we have assumed that Device K2 has a similar ON-state kink barrier). The errors on the presented values in Table 5.3 are 10% on the value rounded to a single significant digit (e.g. 560

means 560 ± 60).

Table 5.3: Channel Parameters Including Oxide Trap Effects of Kinked Devices

Device Code	Portion	C_{eff}/C_G	p_{eff} 10^{17} cm^{-3}	μ_{Cub-Si} 10^{-3} cm^2/Vs	σ μS/cm
K1	Cub-Only	0.047	0.016	200	51
	Hex-Core	0.0062	0.0014	2.3	0.032
K2	Cub-Only	0.048	0.013	20	4.3
	Hex-Core	0.0050	0.00094	2.3	0.025

Knowing the conductivity values for both SiNW portions, we can now calculate the effective channel conductivity. Since both portions are in series, the process is straight-forward.

$$\sigma_{eff} = \frac{L}{\left(\frac{L_c}{\sigma_c} + \frac{L_h}{\sigma_h} \right)} \tag{5.2}$$

Using Eq. 5.2, we can find the expected value for channel resistance. How this value differs from the measured channel resistance is identified as the "kink resistance", labeled R_{kink}. The following table shows how the value of R_{kink} depends greatly on the direction of current flow, confirming the presence of the kink diode at the Cub-Only/Hex-Core interface. The errors on the presented values in Table 5.4 are 10% on the value rounded to a single significant digit (e.g. 560 means 560 ± 60).

Table 5.4: Homojunction Diode Parameters

Device Code	σ_{eff} μS/cm	R_{kink}^s GΩ	R_{kink}^d GΩ	r_{kink}
K1	0.037	0.65	630	970
K2	0.046	3100	33000	11

The rectifying ratio of the kink diode, r_{kink}, is found to be nearly 1000 for Device

K1. As the Cub-Only section is very small, the gate-tunable region is merged with the kink region, which explains why the rectifying behavior found in Device K1 is dominated by the homojunction. For Device K2, the large contact asymmetry dominates the rectifying behavior.

Band bending at the homojunction creates an energy barrier that holes must be able to cross to flow from one NW portion to the next, creating a large kink resistance and an additional rectifying behavior in the output data [51]. As the kink region is merely 11 nm in size, we have shown how the homojunction acts as an excellent rectifier even at the nanometer scale.

5.2.4 Kinked SiNW SB-FET Rectifier Properties

Using our transport model for kinked SiNW SB-FETs, we have been able to characterize their rectifying behavior and quantify their various contact and channel properties. The rectifying ratio can be tuned by both gate and temperature, which affect the heights of both the contact SBs and the kink barrier. Extensive analysis of Device K1 has allowed us to understand how kinked SiNW SB-FETs can be modulated and to confirm the hypothesis of the effects of OSFs on SiNW electronic properties.

Device K1 was observed to have a greatly tunable r value due to small reverse-currents at all gate voltages and temperature. The rectifying ratio was found to exceed 300 when the device was warm and operating at negative gate voltages, while the device could have its rectifying behavior turned off completely ($r = 1$) when cold and operating at positive gate. Device K2, while having reduced tunability, still

operated as a great rectifier. With an extremely small leak current of 40 fA and a forward-bias mode conductance of 1.5 pA/V, this device had a r value of 100 at 6 V.

It is already known that good rectifiers are fabricated with the intent of having very small leak currents by reducing the diameter of the nanowire channel [46]. We have been able to achieve similar results by exploiting the smaller effective channel cross-section of Hex-Core SiNWs to obtain small reverse-currents. Using OSFs to change the internal crystal structure can produce the same effects as reducing the physical size of the device.

To conclude, we have shown in this chapter how kinked SiNW SB-FET devices simultaneously exhibit rectifying output behavior and p-type transfer behavior. With our new transport model, we have demonstrated how a SiNW where the OSF density changes along the length of the nanowire creates a novel material. This allows us to fabricate SB-FET devices with a Cub-Only portion in series with a Hex-Core portion, combining the electronic properties of both crystal phases. In addition to the crystal homojunction found at the kink, these SiNW SB-FETs with varying *Hex* values exploits both contact and channel asymmetries to create excellent rectifiers with r values tunable by several orders of magnitude with gate voltage and temperature. Introducing controlled OSFs into SiNWs may offer a new method to engineer rectifying components into integrated circuits technology.

Chapter 6

Conclusion and Outlook

The main objective of our project was accomplished, as we have quantified the electronic properties of silicon nanowires containing ordered stacking faults. The principle hypothesis of our transport model, that current flow is restricted to the cubic-shell section of the SiNW due to the presence of a depletion layer in the hexagonal-core section, was confirmed by our electronic measurements.

The internal crystal structure of SiNWs can be characterized using Raman spectroscopy. Using this *Hex* value quantifying OSF density, we have provided experimental evidence that OSFs increases parasitic interface trap density effects such as Fermi pinning, hindering the contact and channel properties of SB-FET devices fabricated using these SiNWs.

We have also shown how kinked SiNWs uses contact and channel asymmetry to create excellent tunable rectifiers. The kink barrier formed at the crystal homojunction has been characterized as proof of how gate control is hindered in Hex-Core

SiNWs.

For future work, a full theoretical treatment of the Schottky contact could be done to compliment our transport model and study in more detail the impact of OSFs on the metal-SiNW interface, as understanding metal-semiconductor contacts remain a challenge in device physics [52, 75, 76, 77, 78]. Doping the SiNW OSF core in the contact region could help understand the interplay between OSF density and contact quality [79, 80, 81]. Photoconductivity measurements could be used as experimental evidence of this contact model and to confirm the presence of both the OSF core as well as the kink barrier [71, 82, 83, 84, 85].

Combining OSFs with complex heterostructures could offer new possibilities to tune quantum dots (QDs) though strain engineering [5, 6, 7, 8]. It is already known that Ge/Si core/shell NW heterostructures can easily form QDs (see Fig. 6.1(a)). By using Hex-Si as the shell material instead of the conventional Cub-Si, it may be possible to further tune and control the coupling between the QDs and the gate, as SiNW SB-FETs have already been shown to exhibit Coulomb blockade oscillations at low temperatures (see Fig. 6.1(b)).

Also, suspended SiNW devices could be used for Raman thermometric measurements to determine the thermal conductivity in SiNWs with OSFs and the effect of the kink [10, 11, 12, 13]. Suspended SB-FETs could also be fabricated on plastic substrates to study the effects of strain on current flow through our Hex-Core SiNWs (see Fig. 6.1(c)).

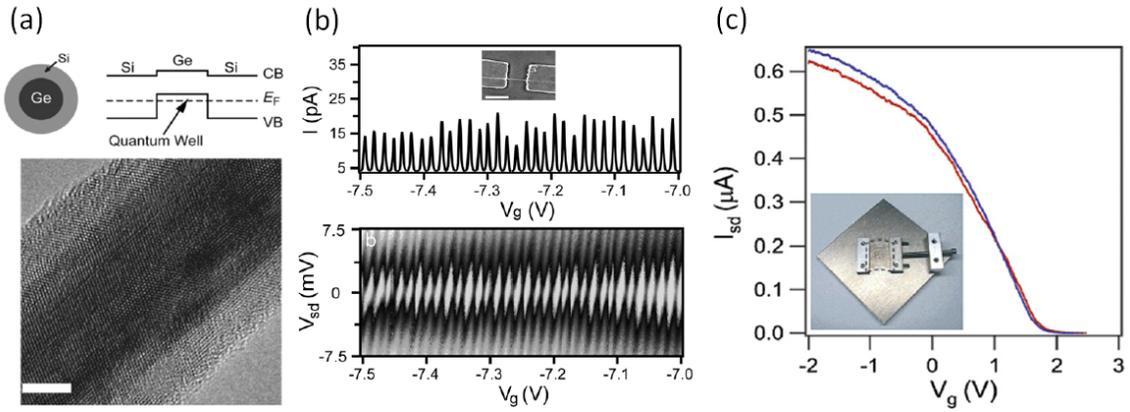Usually, Schottky contact formation in FET devices is not wanted. However,

Figure 6.1: Images of various other NW FETs found in literature. (a) Sketches and HRTEM image showing how a Ge/Si core/shell NW heterostructure can create quantum dots in the NW core. (b) Coulomb blockage oscillations observed at 4.2 K on SiNWs formed by SB tunnel barriers at the metal/Si contacts. (c) Transfer data for a SiNW FET device fabricated on plastic showing how bending the substrate (flat in blue, bent in red) tunes conductivity through strain. Images adapted from [1].

devices formed with large SBs have certain advantages over ordinary FETs, such as having simple and low temperature fabrication procedures and good SCE suppression [51, 74, 86]. Furthermore, SB-FETs are an alternative to ordinary FETs in sub-100 nm devices because they have better scaling properties and eliminate the need for precise doping steps during fab [87]. Furthermore, the control of large SBs are necessary for spin polarized current injection in semiconducting NWs [88]. For technology purposes, enhancement-mode SB-FETs are desired to reduce OFF-state power, which we have shown to be easily obtainable for SiNWs with OSFs [67].

For future applications, we have demonstrated in this work, through our results, that SiNWs with OSFs qualify as a candidate material for SB-FET devices, as their

properties satisfy most of the desired conditions proposed in literature. Using theoretical predictions of our Hex-Core SiNW SB-FET transport model and the experimental evidence of its validity, we could study various homostructures and engineer novel electronic devices.

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