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Design of High-Linearity PVT-Robust Dynamic Amplifier

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Design of High-Linearity PVT-Robust Dynamic Amplifier

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Dedicated to my family.

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Abstract

Design of High-Linearity PVT-Robust Dynamic Amplifier

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Modern electronic device market demands high power-efficiency, high-speed, and high-resolution analog-to-digital converters (ADC). Amplifiers become increasingly significant in the high-performance ADC design. Dynamic amplifier stands out for its low power consumption feature. However, the process-voltage-temperature (PVT) variation and limited linearity prevent it from wide usage. This thesis presents a high-linearity and PVT-robust dynamic amplifier. It implements the capacitively degenerated linearization (CDL) method to achieve high linearity. Furthermore, it combines a PVT-sensing amplifier and a voltage-to-time (V2T) converter as the control timer. Once the foreground calibration is done, the proposed dynamic amplifier will track the PVT variation and provide high-linearity and stable gain. Compared to the conventional CDL dynamic amplifier and the PVT-stabilized

dynamic amplifier, this design suffers from less gain variation over PVT fluctuation while exhibiting high linearity. Therefore, it suits the application of the pipeline ADC and other types of ADC.

A design prototype in schematic level is implemented in 40nm TSMC CMOS technology. The simulation results indicate that the circuit provides less than -80dB total-harmonics-distortion (THD), ranging from $-15°C$ to $100°C$ with 140mV peak-to-peak differential sinusoidal input. When the supply voltage varies from 1.15V to 1.25V, the gain variation of this design is within $\pm 2.5\%$ and the THD is less than -75dB.

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Chapter 1

Introduction

1.1 Overview

In recent years, the reduction of cost and power consumption is increasingly urged for modern electronic device market. Analog-to-digital converter (ADC), the bridge between the real and digital worlds, has to satisfy this booming demand.

As technology goes into the sub-micron region, successive-approximation-register (SAR) ADC structure is increasingly favored because of its scaling-friendly characteristic. Advanced process technology provides a smaller unit capacitor and metal-oxide-semiconductor-field-effect transistor (MOSFET), increasing the density of the integrated circuits. Futhermore, the high power-efficiency also makes SAR ADC suitable for low-power, medium-speed applications such as the Internet of things (IoT).

When it comes to high-speed and high-resolution design, the pipeline ADC structure becomes one of the most suitable choices. To follow the low-power demand trend, the SAR-assisted pipeline, as know as the pipeline-SAR ADC, becomes a promising structure. It benefits from the pipeline structure to process high-speed signal while maintains high power efficiency .

The critical part of the pipeline-SAR ADC is the residue amplifier. The need for high resolution brings the stringent requirement of high linearity, low noise, and stable gain. Traditionally, an operational amplifier (OPAMP) with negative feedback is used for this part. However, it occupies a large fraction of the power budget because of the huge static power consumption. Another common approach, using the open loop amplifiers, is affected by the PVT variation, even though they give great performance on power efficiency. The category of the residue amplifiers is shown in Figure 1.1.

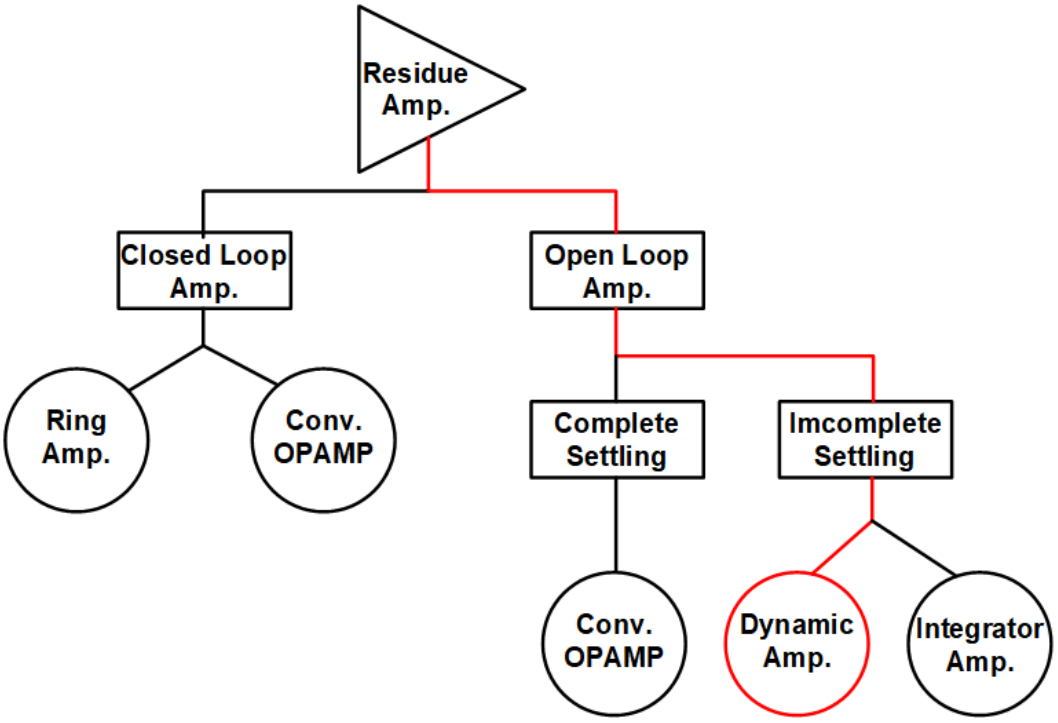


Figure 1.1: Category of the residue amplifiers

Works towards the power-efficient residue amplifier is always a hot topic both in academic and industry. Several techniques have been proposed, such as

ring amplifiers [3, 4], zero-crossing based circuits [5, 6] and integrator-type amplifiers [7]. Among these innovative amplifiers, the dynamic amplifiers become one of the most promising structures because of its many favorable features, which will be discussed in following several sections. The dynamic amplifier inherently allows for low bandwidth design since the amplification is realized by integrating the current. Its unsettled characteristic and dynamic behavior reduce the power consumption. Besides, during the amplification phase, the dynamic amplifiers provide noise-reducing feature [8, 9], which is beneficial for the design of the next stages. However, although the features of the dynamic amplifiers are so attractive, they exhibit more nonlinearity and PVT-sensitivity. Even though the digital background calibration can be utilized to reduce these undesired effects, extra digital correction at higher frequency also brings extra power consumption and reduce the speed of the ADC.

1.2 Performance Terminology

This section discusses the definition performance metrics for an amplifier and will use them throughout the thesis.

1.2.1 Total Harmonic Distortion

Total harmonic distortion (THD) is introduced to measure the linearity. It is defined as the ratio of the sum of the power of all harmonic components to the power of the fundamental signal. Usually, up to 7^{th} harmonics components

are taken into calculation. The formula is shown below,

$$THD = \frac{HD_2^2 + HD_3^2 + ... + HD_7^2}{P_{signal}} \tag{1.1}$$

where HD_n^2 represents the power of the nth harmonic distortion.

1.2.2 Transient Gain

Conventionally, the gain of two-port network is defined as the ratio of the output amplitude to the input amplitude. In terms of the dynamic amplifier, the gain changes with the amplification time. The transient gain needs to be defined. Assuming that the input voltage V_{in} maintains stable after sampling in each clock cycle, the transient gain is defined as the ratio of the transient output voltage to the stable sampled input voltage.

$$A(t) = \frac{V_{out}(t)}{V_{in}} \tag{1.2}$$

1.3 Dynamic Amplifiers

Figure 1.2 shows the structure of a conventional dynamic amplifier. ϕ_{RST} and ϕ_{AMP} are two non-overlapping clock phases, representing the reset phase and the amplification phase. Two N-channel MOSFETs (NMOS) work as the active part, and their sources are connected together with a current source, forming the fully-differential topology. When ϕ_{RST} is activated and ϕ_{AMP} is disabled, the voltage across output capacitors is pre-charged to V_{DD}. At this moment, there is no static current flowing through the circuit.When the amplification phase comes, the pre-charge switches are turned off and

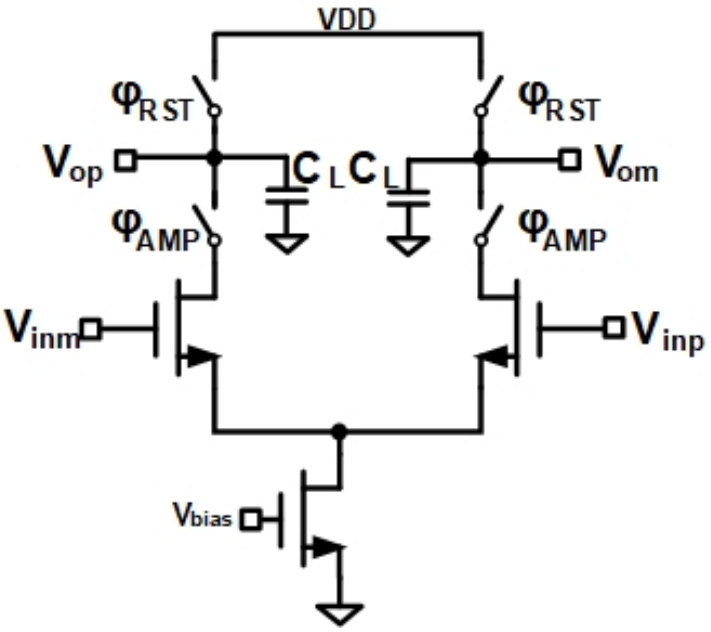


Figure 1.2: Schematic of the open-loop dynamic amplifier

ϕ_{AMP} is activated. NMOS starts to discharge the output capacitors. The output voltage of each half of the amplifier decreases at different rates, which is $g_m \Delta V_{in}/C_L$. Their waveform is shown in Figure 1.3. The voltage at V_{om} and V_{op} are shown as follow [1],

$$V_{om} = V_{DD} - \frac{I_{D0} + g_m \Delta V_{inp}}{C_L} t_{amp} \tag{1.3}$$

$$V_{op} = V_{DD} - \frac{I_{D0} + g_m \Delta V_{inm}}{C_L} t_{amp} \tag{1.4}$$

where I_{D0} is the common-mode current, C_L is the output loading capacitor, t_{amp} is the amplification period, and g_m is the transconductance of NMOS. From Equation (1.3) and (1.4), the transient differential gain can be derived

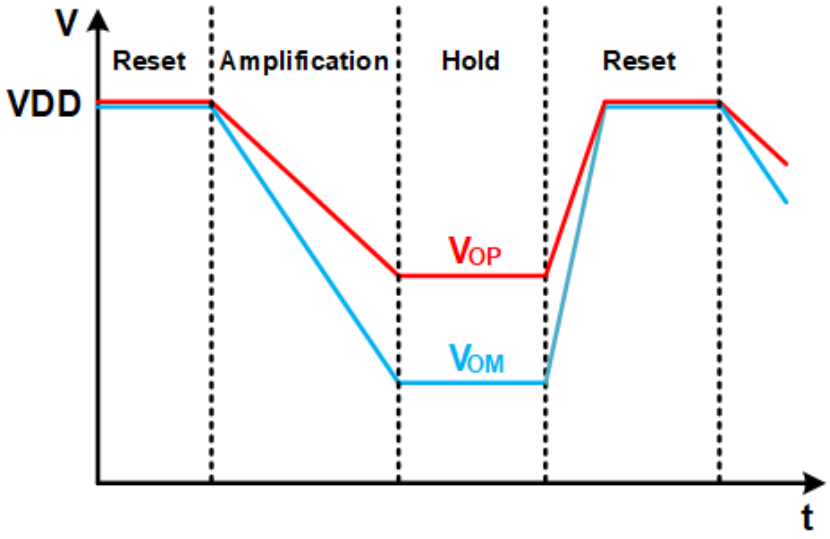


Figure 1.3: Output waveform of the dynamic amplifier

as

$$A_{diff} = \frac{V_{op} - V_{om}}{\Delta V_{inp} - \Delta V_{inm}} = \frac{g_m}{C_L} \cdot t_{amp} \tag{1.5}$$

1.3.1 PVT sensitivity

As Equation (1.5) shows, the gain is proportional to the transconductance g_m. However, the transconductance g_m is not a PVT-robust factor. If an NMOS is biased in the saturation region. That is, $V_{GS}>V_{TH}$, $V_{DS}>V_{GS}-V_{TH}$. Using "the square law", the drain-to-source current I_{DS} is given by

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{1.6}$$

Then we can derive the transconductance g_m as

$$g_m = \frac{dI_{DS}}{dV_{GS}} = \sqrt{2\mu_n C_{ox}\frac{W}{L} I_{DS}} \tag{1.7}$$

where μ_n, C_{ox}, W/L, and I_{DS} are the carrier mobility of NMOS, the oxide capacitance per unit area, the dimension ratio of device size and the static drain-to-source current respectively. From Equation (1.7), the temperature and supply variation would influence g_m, since μ_n is temperature-sensitive [10] and I_{DS} varies because of the PVT variation of the bias circuit. If we provide a fixed amplification period, the gain of the dynamic amplifier is also a PVT-sensitive performance factor.

1.3.2 Nonlinearity

As Equation (1.7) shows, the input signal changes the gate-to-source voltage V_{GS}, introducing the variation of transconductance g_m. Therefore, the gain becomes signal-dependent. As known, the signal-dependent gain would bring the harmonic distortion and impair the linearity of the amplifier. Take the pipeline ADC for example, the nonlinearity of the residue amplifier limits the tolerant input range. Consequently, the resolution of the previous stage has to be large enough to provide small residue voltage for the residue amplifier. It would prolong the conversion time of each stage, limit the number of the stages, and finally reduce the speed of the pipeline ADC. If utilized as the residue amplifier in pipeline, the dynamic amplifier can only amplify small-swing signal, such as a 10mV$\sim$50mV differential peak-to-peak sinusoidal voltage, and provide 50$\sim$60dB linearity [2, 11, 12].

1.4 Related Techniques

Even though the dynamic amplifier provides such excellent features, its drawbacks such as nonlinearity and PVT-sensitivity prevent it from wide usage. Besides, the dynamic amplifiers also suffers from insufficient gain and low-speed constraints. Therefore, many techniques were proposed to improve the dynamic amplifier performance on these aspects.

1.4.1 Self-controlled Dynamic Amplifiers

For a dynamic amplifier, its incomplete settling behavior would introduce nonlinear gain if the amplification period is not well controlled. If an external control signal is utilized, the control clock circuit has to be low-noise which will consume huge extra power. [1] provides a common-mode voltage detection technique to realize the ultra-low-power and high-speed application without external circuits to provide accurate amplification period. Furthermore, the self-controlled technique benefits from the low-noise feature designed for the dynamic amplifier.

As derived in Equation (1.5), the differential gain can be represented as

$$A_{diff} = \frac{g_m}{I_{D0}}(V_{DD} - V_{com}) \tag{1.8}$$

where V_{com} is the output common-mode voltage. The relation between t_{amp} and V_{com} is shown below

$$t_{amp} = \frac{(V_{DD} - V_{com}) \cdot C_L}{I_{D0}} \tag{1.9}$$

From Equation (1.8) and Equation (1.9), the amplification period can be controlled by detecting the voltage drop of the output common-mode voltage. [1] gives its technique to realize this idea.

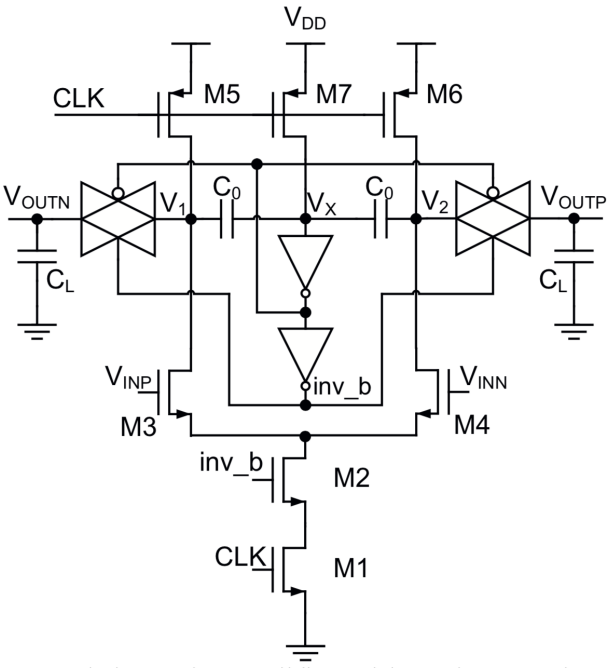


Figure 1.4: Schematic of the common-mode voltage detection dynamic amplifier [1]

Figure 1.4 shows an inverter-based technique to realize the common-mode voltage detection, where V_X represents the output common-mode voltage. Assuming that the parasitic capacitance at node V_X is ignored, when V_X starts to fall across $V_{DD}/2$, the inverters are triggered to terminate the amplification phase and the amplifier will hold the output voltage. Then the

transient gain at this moment becomes

$$A_{diff} = \frac{g_m}{2 \cdot I_{D0}} V_{DD} \tag{1.10}$$

Equation (1.10) shows that using this technique, the dynamic amplifier realizes self-controlled process.

1.4.2 Temperature Compensated Dynamic Amplifier

As discussed before, since the dynamic amplifier works in open loop and behaves as an unsettled amplifier, it is under the influence from the temperature variation. Basically, there are two main methods to relieve this temperature-sensitive phenomenon. One is to build a replica to track the temperature variation and reflect it into amplification period [12]. Another way is to build a temperature compensation circuit to compensate for the temperature variation as Figure 1.5 shows [2]

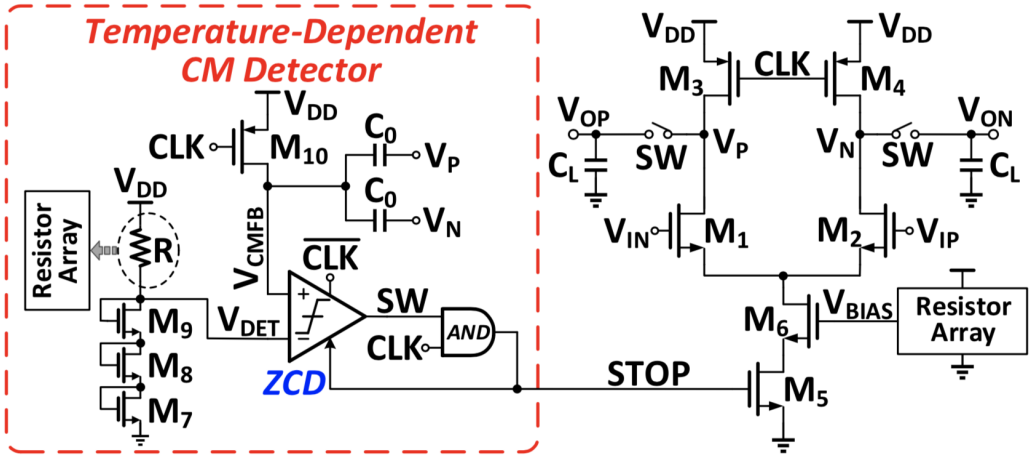


Figure 1.5: Schematic of temperature-compensated dynamic amplifier [2]

The output common-mode voltage V_{CMFB} is detected by two series capacitors. V_{DET} is the threshold voltage of the common-mode (CM) detector, provided by the voltage division of a resistor array and the sum of V_{GS} of M_9, M_8, and M_7. The operation of this method is similar to the common-mode detection technique: when the common-mode output voltage drops across V_{DET}, the zero-crossing detector (ZCD) is triggered and terminates the amplification phase. From the discussion above, the gain is derived as below:

$$A_{diff} = \frac{g_m}{I_{D0}}(V_{DD} - V_{DET}) \tag{1.11}$$

g_m/I_{D0} is controlled by the bias voltage of the tail current source V_{bias}, which can also be tuned by another resistor array.

To make the gain insensitive to the temperature variation, $V_{DD} - V_{DET}$ is designed to compensate the temperature variation of g_m/I_{D0}. The temperature coefficient (TC) of g_m/I_{D0} is given by

$$TC_{g_m/I_{D0}} = \frac{\partial(g_m/I_{D0})}{\partial T} < 0, \tag{1.12}$$

and the TC of $V_{DD} - V_{DET}$ is given by

$$TC_{V_{DD}-V_{DET}} = \frac{\partial(V_{DD} - V_{DET})}{\partial T} > 0 \tag{1.13}$$

As long as $TC_{g_m/I_{D0}}/TC_{V_{DD}-V_{DET}} = -1$, the temperature effects on gain is eliminated. We can achieve this goal by tuning the resistor arrays in the CM detector and the bias circuit.

1.4.3 Gain-boost Dynamic Amplifier

From Equation (1.8), the gain of the conventional dynamic amplifier is usually determined by g_m/I_{D0} and the common-mode output voltage range. However, the common-mode voltage is limited by the supply voltage, and the overdrive voltage limitation constrains the ratio of transconductance and drain current. The conventional dynamic amplifier cannot exhibit very high gain. The limited gain of the residue amplifier increases the fraction of the input-referred noise from the following stage. [11, 13, 14] provide a variety of ways to increase the gain of the dynamic amplifier.

1.4.4 High-Linear Dynamic Amplifier

When dynamic amplifier is used in pipelined ADC, the nonlinearity problem limits the resolution of each stage and also limits the speed of the ADC. [15] gives a method that using negative feedback to linearize the dynamic amplifier in the time domain.

1.5 Motivation

Recent publications [2, 12, 16] have revealed that the dynamic amplifier is a promising structure for the residue amplifier in pipeline ADC and other applications like integrators [17]. However, it suffers from the PVT-sensitivity and inherent nonlinearity. This thesis proposes a PVT-robust high-linearity dynamic amplifier design. Even though the temperature and supply voltage vary significantly, the dynamic amplifier still exhibits stable gain and high

linearity with large input amplitude.

1.6 Thesis Organization

The rest of this thesis is organized as follow: Chapter 2 presents the proposed dynamic amplifier. The characteristics of MOSFET in the sub-threshold region is discussed. Then the capacitively degenerated linearization (CDL) dynamic amplifier is presented and analyzed. Besides, a floating-battery-capacitor invertor-based differential amplifier is exhibited as a single-pole amplifier to sense the PVT variation. A voltage-to-time converter (V2T) is presented to convert the voltage containing the PVT information into a square-wave pulse, which controls the CDL dynamic amplifier.

Chapter 3 shows the specification of the dynamic amplifier and the circuit implementation details.

Chapter 4 presents the simulation results, including the linearity and gain variation versus the temperature and supply variation.

Chapter 5 concludes this work and discusses some future works.

Chapter 2

Proposed Dynamic Amplifier

In this chapter, the characteristics of the MOSFET in the sub-threshold region is discussed first. Then, the capacitively degenerated linearization (CDL) technique is presented, so is the analysis of its high-linear, PVT-sensitive features. To track the variation of the optimized amplification period, a PVT-sensing amplifier and a voltage-to-time converter are combined to generate the amplification control signal.

2.1 Sub-threshold Region Characteristics

Before we introduce the proposed dynamic amplifier, the characteristic of MOSFET in the sub-threshold region needs to be illustrated. For different gate-to-source voltage (V_{GS}), the MOSFET is biased in different regions. Conventionally, if $V_{GS} > V_{TH}$, the MOSFET is considered to be biased in "strong inversion region". The inversion layer, which is the channel, is generated in the bulk. Most of the drain-to-source current is formulated by the drift current. The charge carriers are pulled and pushed by the applied electric field. Assuming $V_{DS} > V_{GS} - V_{TH}$, the transfer characteristic function can be

approximated to Equation (2.1) following the "square law equation".

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{2.1}$$

where μ_n, C_{ox} and W/L are the carrier mobility of the NMOS, the oxide capacitance per unit area and the dimension ratio of the device respectively.

If $0 < V_{GS} < V_{TH}$, MOSFET will work in "weak inversion region". The channel has not been completely formulated yet and the current through the drain and the source is mainly formed by the diffusion current, which is due to the transport of charge carriers by the non-uniform carrier density among the drain, the source, and the bulk.

Note that there is no obvious boundary between the strong and the weak inversion. The transition region is called "moderate inversion region". In this region, both diffusion and drift mechanisms show their effects [10]. In our analysis, we assume that the MOSFET works either in weak inversion region or strong inversion region for simplicity.

Among the sub-threshold region property, the drain current and the slope factor are related to our proposed design. The following sections will discuss them in detail.

2.1.1 Channel Model

The NMOS model is shown in Figure 2.1. All voltages are referred to the p-type substrate. The positive voltage at the gate will attract electrons to the interface between the oxide layer and the p-type substrate, resulting in an

inversion charge layer. The mobile inversion charge density is defined as Q_{inv}. The channel voltage V_{ch} is defined as the difference between the quasi-Fermi potentialof the electrons forming the channel ϕ_n and the Fermi potential Φ_F.

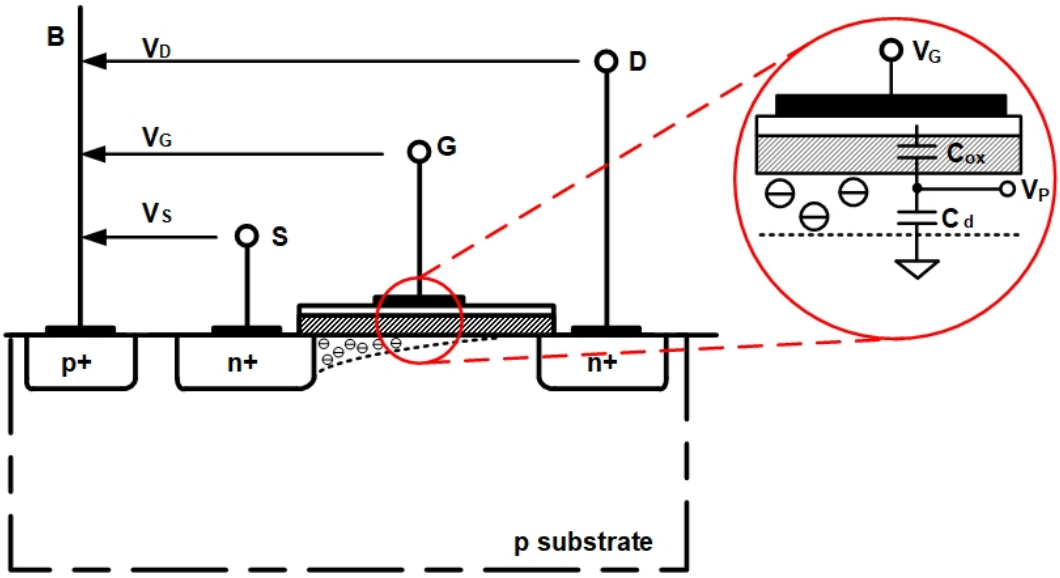


Figure 2.1: Ideal model of the N-channel MOSFET

When the Q_{inv} becomes zero, meaning the inversion layer is about to be formed, the channel voltage is defined as the pinch-off voltage V_P. It can be regarded as the effective voltage of the gate voltage impacting on the channel as shown in Figure 2.1 [10].

2.1.2 Drain Current

As mentioned before, in weak inversion, the drain current is formed by the diffusion current, which satisfies the diffusion equation. Assuming that the mobility μ_n is constant in the sub-threshold region at a specific temperature

and there is no velocity saturation happened, the drain current is derived as Equation (2.2) [10]

$$I_D \approx I_{D0} e^{\frac{V_G}{n \cdot U_T}} [e^{\frac{-V_S}{U_T}} - e^{\frac{-V_D}{U_T}}] \tag{2.2}$$

where I_{D0} is defined as Equation (2.3). It is a process-dependent parameter, indicating the leakage current through the channel when $V_G = 0$. U_T is the thermal voltage kT/q.

$$I_{D0} \equiv I_S \exp\left(\frac{-V_{T0}}{n \cdot U_T}\right) \tag{2.3}$$

n is the slope factor in weak-inversion, indicating the effect of the gate voltage on the channel, which will be discussed in the next section. I_S is the specific current defined as [10]

$$I_S \equiv 2 \cdot n \cdot \beta \cdot U_T^2 \tag{2.4}$$

where β is the product of the ratio of dimension W/L, the mobility μ, and the oxide capacitance per unit area C_{ox}. Usually, the specific current I_S is used as a crossover point between the weak and strong inversion. In another word, the drain current smaller than I_S implies the MOSFET enters the weak inversion while the greater one indicates the MOSFET works in strong inversion.

2.1.3 Slope Factor

As discussed above, the slope factor n is defined as the slope of V_G versus V_P. From Figure 2.1, we can derive the slope factor as

$$n \equiv \frac{dV_G}{dV_P} = 1 + \frac{C_D}{C_{ox}} \tag{2.5}$$

where C_D is the depletion layer capacitance per unit area. The slope factor n is around 1.4 ranging from $-15°$C to 100°C. However, it is the function of the pinch-off voltage V_P and approximately derived as [10]

$$n \equiv \frac{dV_G}{dV_P} = 1 + \frac{\gamma}{2 \cdot \sqrt{\Psi_0 + V_P}} \tag{2.6}$$

Ψ_0 is the approximation of the surface potential in strong inversion at equilibrium where the channel voltage V_{ch} equals to zero. The body effect factor γ is defined as:

$$\gamma = \frac{\sqrt{2 \cdot q \cdot \epsilon_s \cdot N_{sub}}}{C_{ox}} \tag{2.7}$$

From Equation (2.5), the slope factor n is also under the influence of the gate biasing voltage and the temperature variation. But if the MOSFET is biased in deep sub-threshold region, the slope factor n can be regarded as a PVT-insensitive parameter [10].

2.2 Capacitively Degenerated Linearization Structure

The basic structure of capacitively degenerated linearization (CDL) dynamic amplifier is shown in Figure 2.2 [16]. The degenerated capacitors C_{DEG} are connected with the source of the NMOS, while the load capacitors C_L are connected to the drain. Switches are in parallel with the capacitors to work as pre-charge switches.

In terms of nonlinearity, there are two basic types, the compressing and the expanding features. The compressing nonlinearity means that as the input amplitude increases, the gain of the amplifier decreases. The fully differential

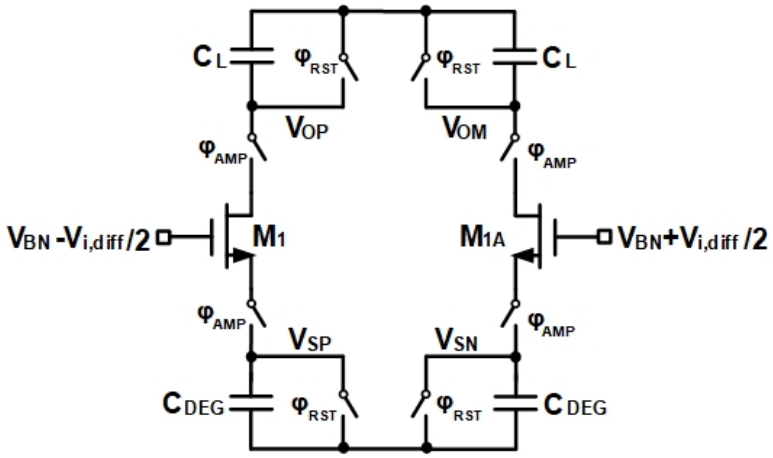


Figure 2.2: Structure of the CDL dynamic amplifier

amplifier presents this type of nonlinearity since the output impedance of the tail current source is large. Vice versa, the expanding nonlinearity provides the opposite phenomenon that the gain is increasing with the increasing input amplitude. The pseudo-differential amplifier exhibits the expanding nonlinearity because the impedance looking from the source is zero.

There are two phases for the CDL technique. In the reset phase, the C_{DEG} is discharged to ground while the C_L is pre-charged to V_{DD}. During the amplification phase, the initial voltage V_S across the degenerated capacitor is zero, which means the source is "tied" to ground. Thus the impedance looking from the source Z_S is approximately equal to zero. At this time, the whole amplifier exhibits the expanding nonlinearity. With the drain current charging the degenerated capacitors, the source voltage starts to increase, resulting in the decrement of the gate-to-source voltage V_{GS}. That is, the source impedance Z_S is increasing. Therefore, the nonlinearity of the amplifier starts

to change from the expanding to the compressing. We can intuitively speculate that there exists a moment that the amplifier is being across the boundary between the compressing and the expanding nonlinearity. It means that the gain is independent from the input amplitude and the amplifier provides high linearity.

The capacitively degenerated linearization (CDL) technique requires the I-V characteristic of the amplifier to be exponential. The analysis will be discussed in the next section. For MOSFET, the I-V relation is exponential only when the transistor is biased in the weak inversion region, also as known as sub-threshold region. Similarly, this CDL technique could be implemented by the bipolar junction transistor, of which the collector current I_C is exponential to the base-to-emitter voltage V_{be}.

2.2.1 Analysis

The drain-to-source current I_{DS} of the MOSFET in the weak inversion is exponential to the gate voltage as given by Equation (2.2). If the drain voltage V_D is much greater than the thermal voltage U_T, resulting in $\exp(-V_{DS}/U_T) \ll 1$, so the drain-to-source current approximately equals to

$$I_{DS} \approx I_{D0} \exp\left(\frac{V_G}{nU_T}\right) \cdot \exp\left(-\frac{V_S}{U_T}\right) \tag{2.8}$$

For the positive half circuit, the following Equation (2.9) is valid all the time:

$$C_S \frac{dV_{SP}}{dt} \equiv I_{D0} \exp\left(\frac{V_{BN} + V_{i,diff}/2}{nU_T}\right) \cdot \exp\left(-\frac{V_{SP}}{U_T}\right) \tag{2.9}$$

where V_{BN} is the biasing voltage of the NMOS differential pairs and V_{SP} is the source voltage of the positive half. Integrated over time, V_{SP} is derived as below:

$$V_{SP} = U_T \ln [\frac{I_{D0}t}{C_{DEG}U_T} \exp (\frac{V_{BN} + V_{i,diff}/2}{nU_T}) + c_1/U_T] \tag{2.10}$$

At the beginning of amplification, the source voltage is zero, thus we can get $c_1 = U_T$. The term "$I_{D0} \exp (V_{BN}/nU_T)$" is the quiescent current I_{Q0} of the amplifier when the input amplitude is zero. For simplicity, we define $\alpha = I_{Q0}t/C_{DEG}U_T$. Thus Equation (2.10) is rewritten as

$$V_{SP} = U_T \ln [\alpha \cdot \exp (\frac{V_{i,diff}}{2nU_T}) + 1] \tag{2.11}$$

and for the negative half circuit, the source voltage V_{SN} is similarly expressed as

$$V_{SN} = U_T \ln [\alpha \cdot \exp (-\frac{V_{i,diff}}{2nU_T}) + 1] \tag{2.12}$$

Assuming there is no parasitic capacitance, the charges flowing into the degenerated capacitor C_{DEG} are from the pre-charged load capacitor C_L. Since there is no other path to share the charges, Equations (2.13) and (2.14) are held during the amplification phase

$$C_L \cdot \Delta V_{OP} \equiv C_{DEG} \cdot \Delta V_{SP} \tag{2.13}$$

$$C_L \cdot \Delta V_{OM} \equiv C_{DEG} \cdot \Delta V_{SN} \tag{2.14}$$

where ΔV_{OP} and ΔV_{OM} are the changed value of the output voltages of the positive and negative branches. The transient gain is defined as

$$A(t) \equiv \frac{\Delta V_{OP} - \Delta V_{OM}}{V_{i,diff}} = \frac{C_{DEG}}{C_L} \cdot \frac{\Delta V_{SP} - \Delta V_{SN}}{V_{i,diff}} \tag{2.15}$$

Replace ΔV_{SP} and ΔV_{SN} with Equations (2.11) and (2.12), the gain is rearranged as

$$A(t) = \frac{C_{DEG}}{2nC_L} + \frac{C_{DEG}}{C_L}\frac{U_T}{V_{i,diff}} \ln\left[\frac{1 + \alpha \cdot \exp\left(\frac{V_{i,diff}}{2nU_T}\right)}{\alpha + \exp\left(\frac{V_{i,diff}}{2nU_T}\right)}\right] \tag{2.16}$$

As long as $\alpha = 1$, the second term related to the input signal is eliminated. The transient gain $A(t)$ becomes independent of the input signal amplitude $V_{i,diff}$. It means at this moment, the amplifier exhibits high-linear gain. The amplification period at this moment is called the optimized time t_{opt}. We can rearrange the expression of α as

$$t_{opt} = \frac{U_T C_{DEG}}{I_{Q0}} \tag{2.17}$$

and the corresponding gain is called the optimized gain A_{opt}

$$A_{opt} = \frac{C_{DEG}}{2nC_L} \tag{2.18}$$

The derivation above explains why the CDL technique provides high linearity at the optimized time t_{opt}. Besides, Equation (2.18) shows that the optimized gain A_{opt} is a PVT-insensitive factor, since the slope factor n is PVT-robust in deep sub-threshold region. However, t_{opt} is sensitive to temperature and supply voltage variation, because Equation (2.17) shows that the thermal voltage U_T and the quiescent current I_{Q0} are both temperature and supply voltage dependent parameters.

To calibrate the variation of temperature and supply voltage, [16] uses an extra DAC to tune the bias current I_{Q0} to make the optimized time satisfy

the condition that $t_{opt} = U_T C_{DEG}/I_{Q0}$. However, it needs periodic multiple foreground calibrations to track PVT variation, which reduces the speed and power-efficiency of the amplifier. To achieve PVT-robostnesss, one way is to design a constant-g_m biasing circuit, which automatically adjusts the bias current over PVT fluctuation and keep the transconductance g_m constant. Thus, the less linearity deterioration requires a smaller tuning range resulting in foreground calibration process easier. Another way is to automatically match t_{amp} to t_{opt} over PVT variation and keep the slope factor n constant. Therefore, the dynamic amplifier will provide great high linearity, stable gain and be PVT-robust.

2.2.2 Cross-Coupled Degenerated Capacitors

For a conventional dynamic amplifier in the amplification phase, both positive and negative branches discharge the load capacitors. The differential output voltage depends on the difference between two slewing currents. However, the common-mode output voltage drops during the phase, constraining the duration of the amplification phase and the gain of the dynamic amplifier.

To relieve this limited gain issue, the inverter-based structure is implemented by reusing the current [18]. The output range is also enlarged by making the positive and negative output voltages changing in two opposite directions. However, the mismatch of the quiescent current of PMOS and NMOS requires the common-mode feedback (CMFB) circuit to maintain the common-mode output voltage.

In this design, the degenerated capacitors are implemented in the cross-coupled structure shown in Figure 2.3 [16]. The degenerated capacitors are connected between the sources of the positive and negative branches.

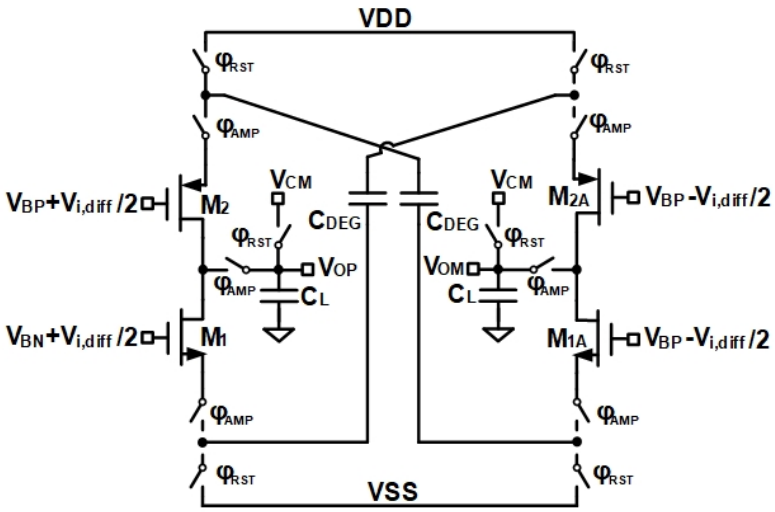


Figure 2.3: Structure of the cross-coupled CDL dynamic amplifier

For the differential signal, the equivalently effective circuit is shown in Figure 2.4. C_{DEG} works effectively as $2C_{DEG}$ at each source of NMOS and PMOS for the conventional CDL dynamic amplifier in Figure 2.2. Ignoring any parasitic capacitance, there is no common-mode current flowing into the load capacitor during the amplification phase, since the current is supplied by two pre-charged floating capacitors. But the differential currents are still flowing in and out of the load resulting in differential output voltage. By implementing the cross-coupled structure, the amplifier provides excellent common-mode voltage rejection characteristic. Thus, there is no need for CMFB circuit.

In addition, by using the inverter-based structure and the cross-coupled

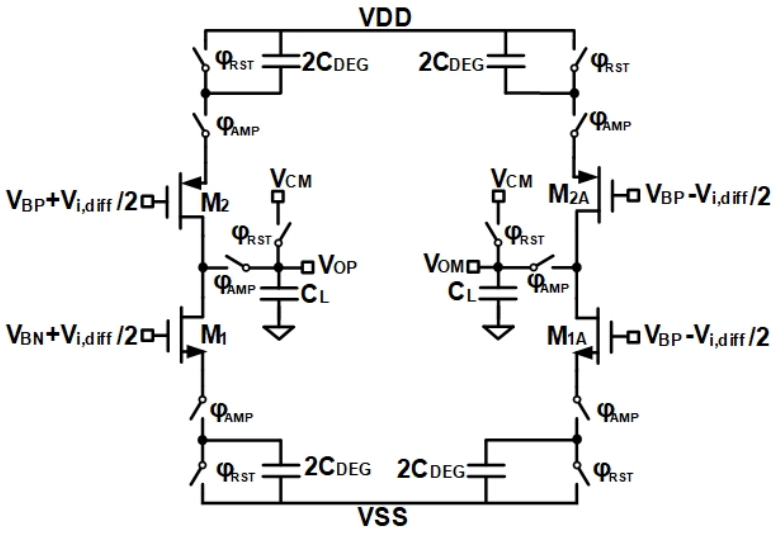


Figure 2.4: Effective circuit of the cross-coupled CDL dynamic amplifier

degenerated capacitors pair, the effective degenerated capacitor in Equation (2.18) is actually enlarged fourfold, reducing the required capacitors and increasing the optimized gain.

2.3 PVT-sensing Amplifier

As we discussed before, there are two ways to achieve automatic stabilizing linearity and gain. One is to adjust the bias currents to make the optimized time t_{opt} matched to the fixed amplification period t_{amp}. Another way is to adjust t_{amp} to follow the variation of t_{opt}. In this design, we decided to explore the second way to realize a high-linearity, stable-gain, and PVT-robust dynamic amplifier.

To make the amplification period t_{amp} keep tracking the PVT variation,

a PVT-sensing block and a PVT-information-to-time converter are needed to control the CDL dynamic amplifier. In this section, the single-pole amplifier is discussed and used as a PVT-sensing amplifier.

2.3.1 Single-Pole Amplifier

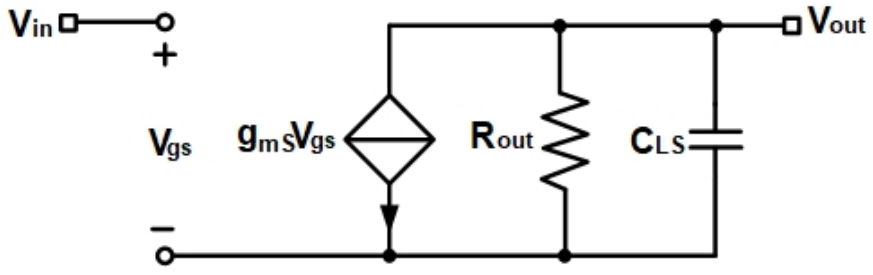


Figure 2.5: Structure of the single-pole amplifier

The single-pole amplifier is shown in Figure 2.5. The Laplace transfer function of a single-pole amplifier is given by

$$H(s) = \frac{A_{DC}}{1 + s/\tau} \tag{2.19}$$

where τ is the time constant of the single-pole amplifier. Usually, $\tau = R_{out}C_{LS}$, where R_{out} is the output resistance of the amplifier and the C_{LS} is the load capacitor. The A_{DC} is the DC gain of the amplifier. For the amplifier in Figure 2.5 specifically, $A_{DC} = g_{mS} \cdot R_{out}$, where the g_{mS} is the transconductance of the single-pole amplifier.

At $t = 0$, there is a step signal V_{step} at the input, and the Laplace transform of the signal is shown as

$$V_{in}(s) = \frac{V_{step}}{s} \tag{2.20}$$

Assume that the whole system is a linear-time-invariant system (LTI), so the Laplace transform of the output voltage can be derived as

$$V_{out}(s) = V_{step}A_{DC}(\frac{1}{s} - \frac{1}{s+\tau}) \tag{2.21}$$

In the time domain, the output voltage is shown as

$$V_{out}(t) = V_{step}A_{DC}(1 - e^{-t/\tau}) \tag{2.22}$$

Apply the Taylor-series expansion to Equation (2.22), assuming $t \ll \tau$. Then replace A_{DC} with $g_{mS}R_{out}$ and τ with $C_{LS}R_{out}$. The output voltage becomes

$$V_{out}(t) \approx V_{step}A_{DC} \cdot (t/\tau) \approx V_{step} \cdot \frac{g_{mS}}{C_{LS}} \cdot t \tag{2.23}$$

From the derivation above, we can conclude that for a very short period t_{ramp} at the beginning, the output voltage V_{out} could be approximately regarded as a ramp signal. The slope of the ramp approximately equals to $V_{step} \cdot g_{mS}/C_{LS}$. If applying the output voltage to a voltage-to-time converter (V2T), the objective time will contain the PVT variation information. Here, we rearrange the Equation (2.23) to

$$t_{ramp} = \frac{C_{LS}}{g_{mS}} \cdot \frac{V_{ramp}}{V_{step}} \tag{2.24}$$

where V_{ramp} is defined as the threshold voltage of V2T in next stage.

In the discussion of sub-threshold characteristics, from Equation (2.8), we can derive the transconductance g_{mS}. If the MOSFET is biased in the weak inversion, assuming the source is connected to ground, $V_S = 0$, the transconductance g_{mS} is given by

$$g_{mS} = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{I_{D0}}{nU_T} \exp{(\frac{V_G}{nU_T})} = \frac{I_{QS}}{nU_T} \tag{2.25}$$

I_{QS} is the quiescent drain current of the single pole amplifier, which equals to $I_{D0}\exp\left(V_G/nU_T\right)$. Thus, Equation (2.24) is rewritten as

$$t_{ramp} = \frac{U_T C_{LS}}{I_{QS}} \cdot n \cdot \frac{V_{ramp}}{V_{step}} \tag{2.26}$$

Equation (2.26) shows that if a single-pole amplifier is biased in the sub-threshold region and combined with a V2T converter, the output time t_{ramp} can contain the PVT information $U_T C_{LS}/I_{QS}$. After initial tuning, making t_{ramp} equals to t_{opt}, the PVT-sensing amplifier and the CDL dynamic amplifier can experience the same effect by the PVT variation.

$$t_{ramp} = \frac{U_T C_{LS}}{I_{QS}} \cdot n \cdot \frac{V_{ramp}}{V_{step}} = \frac{U_T C_{DEG}}{I_{Q0}} = t_{opt} \tag{2.27}$$

It means that the amplification period t_{ramp} should always match t_{opt} over the PVT variation once the tuning is done. If we utilize t_{ramp} as the amplification period, the CDL dynamic amplifier should theoretically resist the PVT variation influence and remain high-linearity during the amplification.

2.3.2 Floating Battery Capacitor

As discussed in the last section, a single-pole amplifier biased in the sub-threshold region can sense the PVT variation. The design in [12] uses a single-ended output amplifier to generate the ramp voltage as shown in Figure 2.6.

The output voltage of this structure reflects the fluctuation of NMOS's transconductance. However, for the cross-coupled CDL dynamic amplifier,

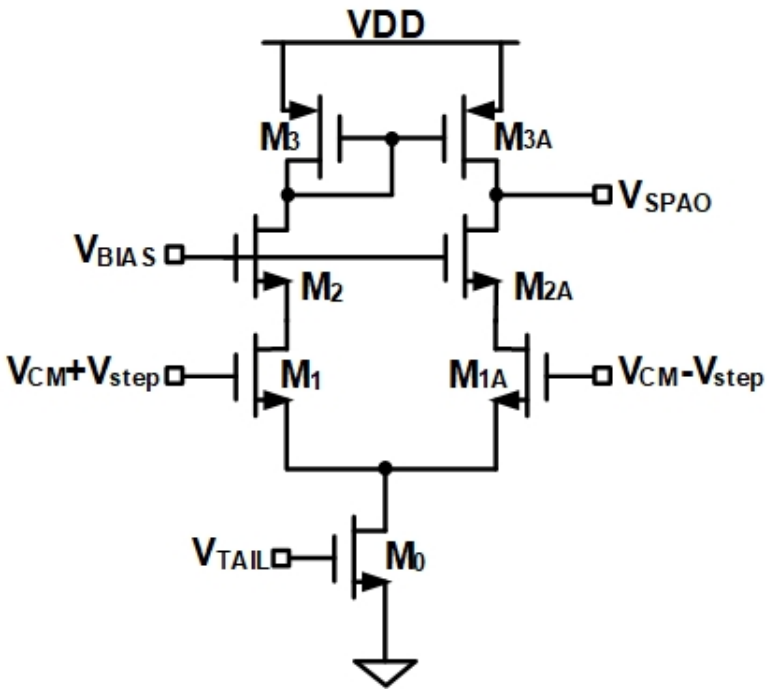


Figure 2.6: Schematic of the single-ended output amplifier

the change of transconductance of PMOS also needs to be reflected in the ramp voltage. Therefore, the inverter-based structure is implemented to make PVT-sensor and the CDL dynamic amplifier matched.

Similarly, the conventional inverter-based structure needs the CMFB circuit to stabilize the output common-mode voltage. In this design, we use a floating battery capacitor as the supply [18]. The circuit design is shown in Figure 2.7. To reduce the source voltage V_S variation during the amplification phase, the floating battery capacitor is required to be much greater than the load capacitors, which is $C_B > 10C_{LS}$.

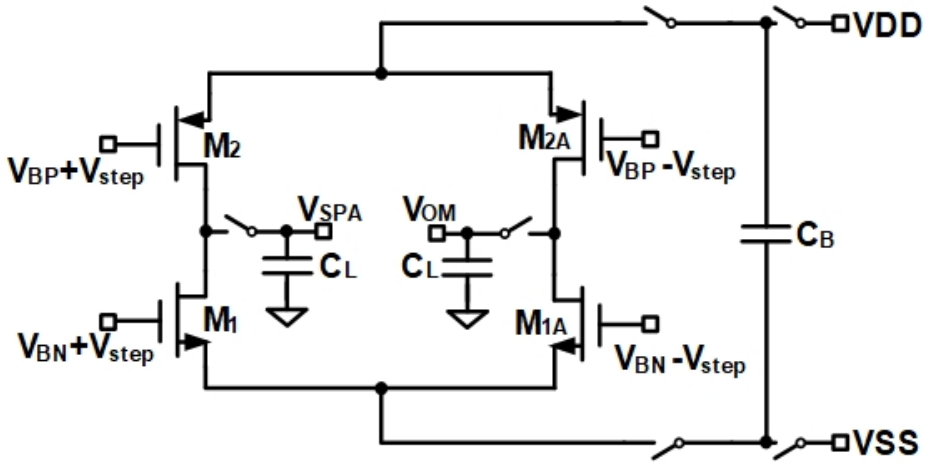


Figure 2.7: Schematic of the floating battery capacitor differential amplifier

2.4 Voltage-to-time Converter

To make the amplification period t_{ramp} proportional to the output voltage of the PVT-sensing amplifier, we want to design a V2T converter which has the PVT-robust threshold voltage V_{ramp}. There are many designs about the V2T converter [13, 19], but these V2T converters are PVT-sensitive and not suitable for PVT-robustness expectation. In this design, we implement the cascade inverters technique for the V2T converter, which has less variation under PVT influence [12].

2.4.1 Structure

The voltage-to-time converter is implemented with cascaded inverters as shown in Figure 2.8.

Here is how it works: At the reset phase, S1/S2 are off, and S7/S8,

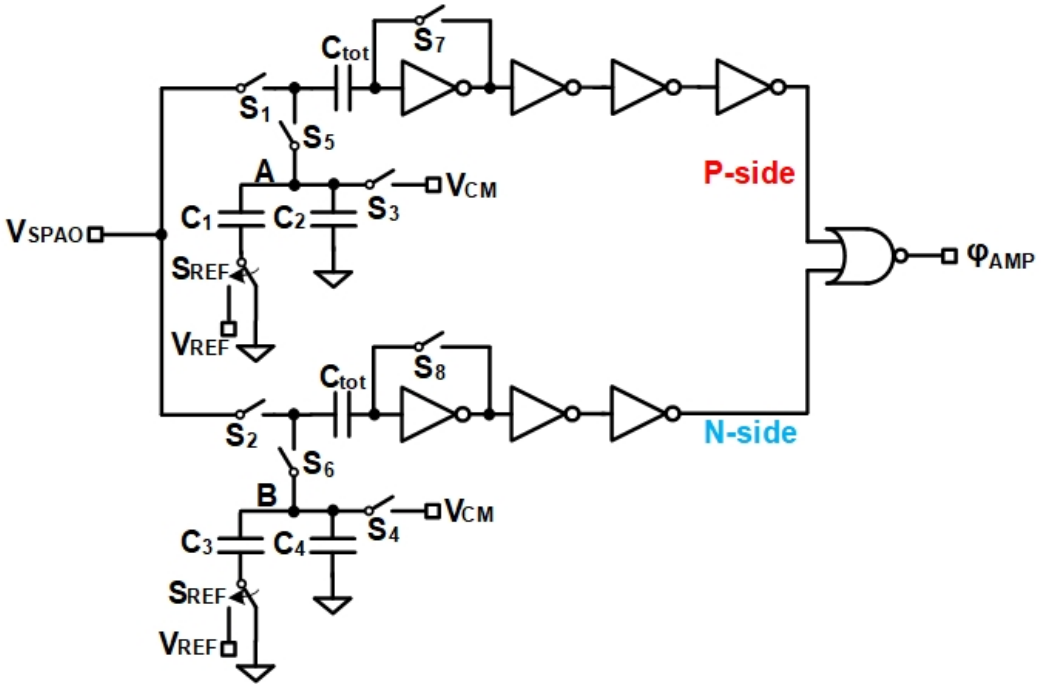


Figure 2.8: Structure of the cascaded-inverters V2T converter

S5/S6, and S3/S4 are turned on to make the first inverters of both paths into auto-zero mode [12]. The input and output of the inverters in the chain will be biased at the edge of the threshold voltage ($V_{th,inv}$). After every node is settled, the node voltages V_A and V_B is charged to V_{CM}. Then, turn off S3/S4 and then change the bottom plates of C_1 and C_3 from the ground to the reference voltage V_{ref}. Since the nodes A and B are floating, the voltages V_A and V_B are added by a fraction of V_{ref}, which is determined by the ratio of C_1/C_3, C_2/C_4, and C_{tot}. Once all nodes are settled, turn off the S5/S6 and S7/S8.

At this moment, if $C_1 + C_2 = C_3 + C_4 = C_{tot}$, the across voltages of the

P-side and N-side capacitors C_{tot} are shown as

$$\Delta V_{P-side,C} = V_{CM} + \frac{C_1}{2C_{tot}} \cdot V_{ref} - V_{th,inv} \tag{2.28}$$

$$\Delta V_{N-side,C} = V_{CM} + \frac{C_3}{2C_{tot}} \cdot V_{ref} - V_{th,inv} \tag{2.29}$$

The output voltage of the PVT-sensing amplifier is V_{SPAO}. Since we use the floating battery capacitor structure, V_{SPAO} is given by

$$V_{SPAO} = V_{CM} + \Delta V_{out}(t) \tag{2.30}$$

where $\Delta V_{out}(t)$ is the transient varying value of output voltage. After turn on S1/S2, the voltage at the input of the first inverters in both sides will be

$$V_{inv,P} = V_{SPAO} - \Delta V_{P-side,C} = \Delta V_{out}(t) - \frac{C_1}{2C_{tot}} \cdot V_{ref} + V_{th,inv} \tag{2.31}$$

$$V_{inv,N} = V_{SPAO} - \Delta V_{N-side,C} = \Delta V_{out}(t) - \frac{C_3}{2C_{tot}} \cdot V_{ref} + V_{th,inv} \tag{2.32}$$

When $V_{inv,P}$ or $V_{inv,N}$ exceeds $V_{th,inv}$, the inverter will be triggered. i.e.

$$\Delta V_{out}(t_1) = \frac{C_3}{2C_{tot}} \cdot V_{ref} \tag{2.33}$$

$$\Delta V_{out}(t_2) = \frac{C_1}{2C_{tot}} \cdot V_{ref} \tag{2.34}$$

Here is the following operation: S1/S2 is turned on and the slewing current of PVT-sensing amplifier starts to charge the capacitor C_{LS}. At $t = t_1$, when ΔV_{out} is across over $V_{ref} \cdot C_3/2C_{tot}$, the N-side V2T converter is activated and the output control signal Φ_A will be activated and go to high voltage level. Meanwhile, the dynamic amplifier starts to amplify the input signal. ΔV_{out}

keeps increasing when equals the threshold voltage of the P-side at $t = t_2$, the output control signal Φ_A will fall, resulting in dynamic amplifier to stop amplification and keep the output voltage held. The amplification period t_{ramp} is represented as $t_2 - t_1$. The voltage difference between these two moments is exactly the threshold voltage of the V2T converter V_{ramp} [12].

$$V_{ramp} = \frac{C_3 - C_4}{2C_{tot}} \cdot V_{ref} \tag{2.35}$$

By substituting Equation (2.35) into (2.24), t_{ramp} is rewritten as

$$t_{ramp} = \frac{C_{LS}}{g_{mS}} \cdot \frac{C_1 - C_3}{2C_{tot}} \cdot \frac{V_{ref}}{V_{step}} \tag{2.36}$$

If V_{ref} and V_{step} are connected with reference voltage source, which is insensitive to PVT variation. The expression of t_{ramp} shows that it represents the transconductance information. If we bias the PVT-sensing amplifier and the CDL dynamica amplifier at same situation. The reference voltage V_{ref} can work as a tuning knob to make t_{ramp} matched to t_{opt} during calibration.

2.4.2 Dummy Load

At the beginning of generating the ramp output of the single-pole amplifier, the load capacitor C_{LS} is merged with the capacitors C_{tot} in the V2T converter. For real capacitors, like the metal-oxide-metal capacitor (MOM-CAP), there are about 10% parasitic capacitance to AC ground at each terminal. Therefore, it brings the offset voltage to the initial ramp output voltage of the PVT-sensing amplifier. To attenuate the effects of this merging connec-

tion, only the positive output is connected to the input of the V2T convertor, and the amplification control signal is triggered by two voltages.

Moreover, the parasitic capacitance also influences the slope of the ramp output voltage if only one side is used for voltage-to-time conversion, because the mismatch between the load capacitors introduces the variation of the common-mode output voltage. To attenuate this asymmetric load effects, a dummy load, same as the front end of the V2T converter, is placed at the negative output of the PVT-sensing amplifier. Figure 2.9 illustrates the dummy load structure.

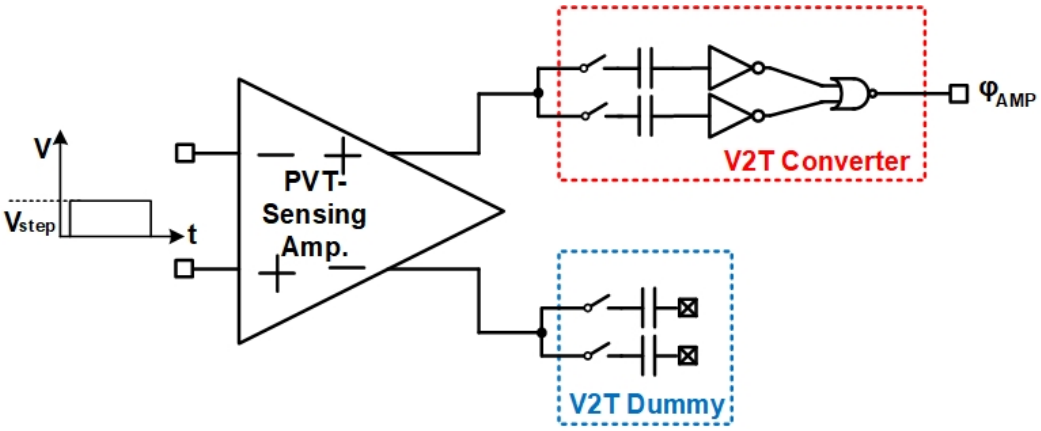


Figure 2.9: Structure of the dummy load

Chapter 3

Circuit Implementation

In this chapter, the circuit implementation details of the proposed design are presented. The top-level diagram is shown Figure 3.1.

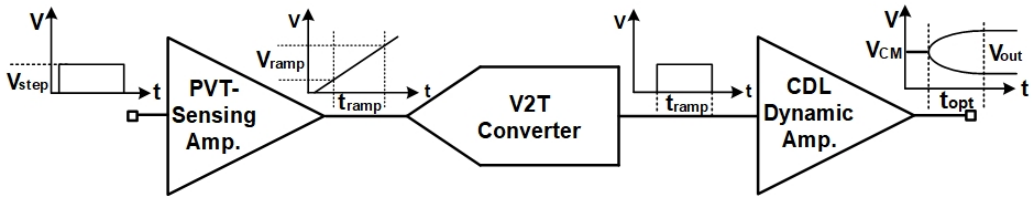


Figure 3.1: Block diagram of the proposed dynamic amplifier

3.1 Specification

The targeted specification of the dynamic amplifier is shown in Table 3.1

Sample Frequency	51.2MS/s
Gain	>3
THD($V_{i,diff}$ = 100mV)	<-80dB
Temperature Variation	$-15°C \sim 100°C$
Supply Variation	1.15V $\sim$ 1.25V

Table 3.1: Table of the design specification

3.2 CDL Dynamic Amplifier

The full schematic of the CDL dynamic amplifier is shown in Figure 3.2 . The device information is provided in Table 3.2 .

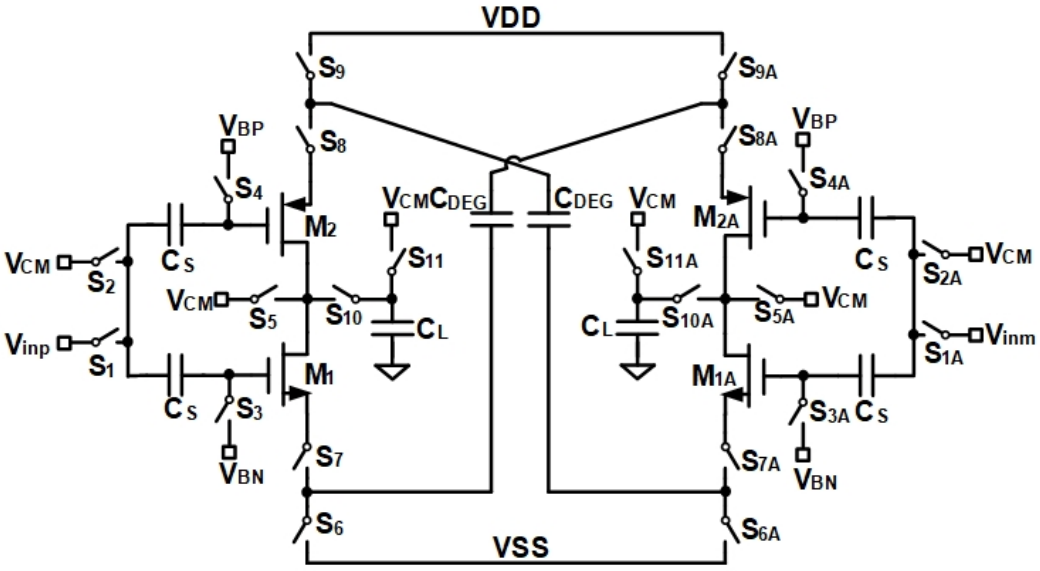


Figure 3.2: Schematic of the CDL dynamic amplifier

We use the high-threshold-voltage MOSFETs as the active part since they require a smaller size and less current to enter the sub-threshold region than the low-threshold voltage ones. The capacitors are implemented by MoM-Cap and the expected values are also shown in Table 3.2. Besides, the type, size and activated phase of switches are listed in Table 3.3. In the signal path, all switches are bootstrapped to maintain high linearity. For switches S_3/S_{3A} and S_4/S_{4A}, ϕ_{RST_E} falls 200ps earlier than ϕ_{RST} for realizing bottom-plate sampling. We assign the pulse width of ϕ_{RST} to 2ns and ϕ_{RST_E} to 1.8ns. In

Name	Device Type	Size
M_1/M_{1A}	NMOS hvt	$16\mu m/40nm$
M_2/M_{2A}	PMOS hvt	$32\mu m/40nm$
C_S	MoM Capacitor	$309fF$
C_L	MoM Capacitor	$600fF$
C_{DEG}	MoM Capacitor	$3.16pF$

Table 3.2: Table of the device of the CDL dynamic amplifier.

Name	Switch Type	Size Dimension	Activated Phase
S_1/S_{1A}	Bootstrapped NMOS	$19.2\mu m/40nm$	ϕ_{AMP}
S_2/S_{2A}	NMOS lvt	$3.6\mu m/40nm$	ϕ_{RST}
S_3/S_{3A}	NMOS lvt	$1.2\mu m/40nm$	ϕ_{RST_E}
S_4/S_{4A}	NMOS lvt	$1.2\mu m/40nm$	ϕ_{RST_E}
S_5/S_{5A}	NMOS lvt	$3.6\mu m/40nm$	ϕ_{RST}
S_6/S_{6A}	CMOS	N($3.6\mu m/40nm$) P($9\mu m/40nm$)	ϕ_{RST}
S_7/S_{7A}	CMOS	N($9.6\mu m/40nm$) P($24\mu m/40nm$)	ϕ_{AMP}
S_8/S_{8A}	CMOS	N($3.6\mu m/40nm$) P($9\mu m/40nm$)	ϕ_{AMP}
S_9/S_{9A}	CMOS	N($9.6\mu m/40nm$) P($24\mu m/40nm$)	ϕ_{RST}
S_{10}/S_{10A}	Bootstrapped NMOS	$19.2\mu m/40nm$	ϕ_{AMP}
S_{11}/S_{11A}	NMOS	$3.6\mu m/40nm$	ϕ_{RST}

Table 3.3: Table of the switches of the CDL dynamic amplifier

this way, we can calculate the required maximum on-resistance of the switches and then assign their size. For switches S_9/S_{9A} and S_6/S_{6A}, they are designed to be CMOS switches to control the current charging C_{DEG}. For switches S_7/S_{7A} and S_8/S_{8A}, their on-resistance will degrade the optimized gain and move the optimized time a bit earlier [16]. Thus, they are designed to be CMOS switches with large size. ϕ_{AMP} and ϕ_{RST}/ϕ_{RST_E} are two non-overlapping

phases generated by the V2T converter and external control circuit.

3.3 Voltage-to-time Converter

3.3.1 Threshold Voltage Detector

The full schematic of the voltage-to-time converter is shown in Figure 3.3. And the clock diagram is shown in Figure 3.4. Table 3.4 depicts the device category and size.

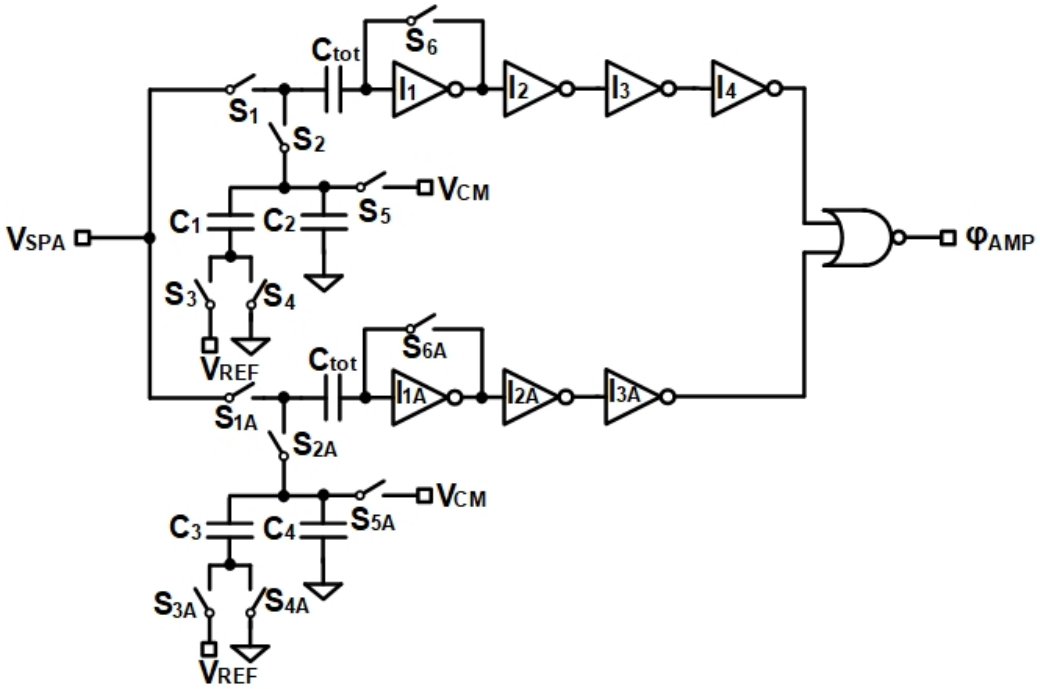


Figure 3.3: Schematic of the V2T converter

The inverters chain and the NOR gate are implemented by the logic gates in the standard library. From the previous discussion, the size of the gate only needs to satisfy the settling requirement.

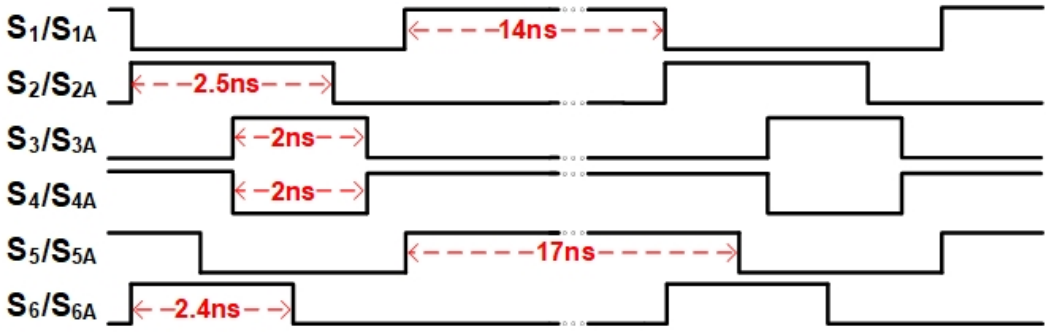


Figure 3.4: Clock diagram of the V2T converter

Name	Device Type	Size
C_1	MoM Capacitor	$64fF$
C_2	MoM Capacitor	$39fF$
C_3	MoM Capacitor	$11fF$
C_4	MoM Capacitor	$91fF$
C_{tot}	MoM Capacitor	$100fF$
I_1/I_{1A}	Standard cell library	-
I_2/I_{2A}	Standard cell library	-
I_3/I_{3A}	Standard cell library	-
I_4	Standard cell library	-
$NORgate$	Standard cell library	-

Table 3.4: Table of the device of the V2T converter.

Name	Switch Type	Size	Activated Phase
S_1/S_{1A}	CMOS	N($2.4\mu m/40nm$) P($4.8\mu m/40nm$)	ϕ_{S1}
S_2/S_{2A}	NMOS lvt	$600nm/40nm$	ϕ_{S2}
S_3/S_{3A}	NMOS lvt	$600nm/40nm$	ϕ_{S3}
S_4/S_{4A}	NMOS lvt	$600nm/40nm$	ϕ_{S3_B}
S_5/S_{5A}	NMOS lvt	$1.2\mu m/40nm$	ϕ_{S5}
S_6/S_{6A}	NMOS lvt	$1.2\mu m/40nm$	ϕ_{S6}

Table 3.5: Table of the switches of the V2T converter

The type, size, and activated phase of the switches are listed in Table 3.5. Except for the S_1/S_{1A}, all switches control charging or discharging the node to static voltages. There is no high-linearity requirement for these switches as long as the node is charged to an expected voltage on time. Therefore, the NMOS switches are utilized. However, the charge injection effect brings the voltage fluctuation to the node when the switch is turned off. A dummy switch is deployed near the critical node to reduce this undesired effect. The width of the dummy switch is the half of that of the active switch. In this design, S_2/S_{2A} and S_6/S_{6A} implement this dummy-charge-injection cancellation as Figure 3.5 shows.

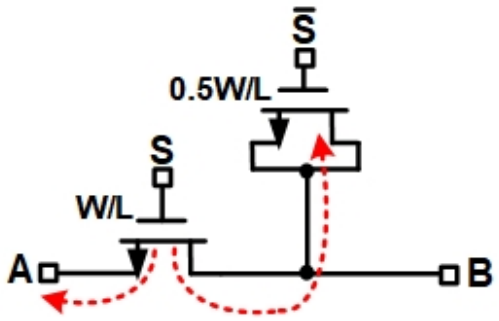


Figure 3.5: Dummy-charge-injection cancellation

A dummy NMOS is deployed at the sensitive node B near the NMOS switch. The gate voltage of the dummy NMOS is controlled by the inverse control signal $\overline{S}$. When the control signal S is disabled, the electrons stored in the channel are about to be injected into two nodes, A and B. Meanwhile, the dummy switch needs the electrons to form the channel. If we design the device area of the dummy as half of that of the transmission switch, the charges

injected into node B would be absorbed by the dummy NMOS, and there is less voltage variation at the node B when S is off.

3.4 PVT-Sensing Amplifier

3.4.1 Floating Battery Capacitor Dynamic Amplifier

The full schematic of the PVT-sensing amplifier is shown in Figure 3.6. Table 3.6 provides the size and category of the devices. The PVT-sensing amplifier input V_{step} is connected to a reference voltage. The positive output V_{SPA} is connected to the input of the V2T converter and the negative output V_{OM} is connected to a dummy of the V2T converter. From the discussion in Chpater

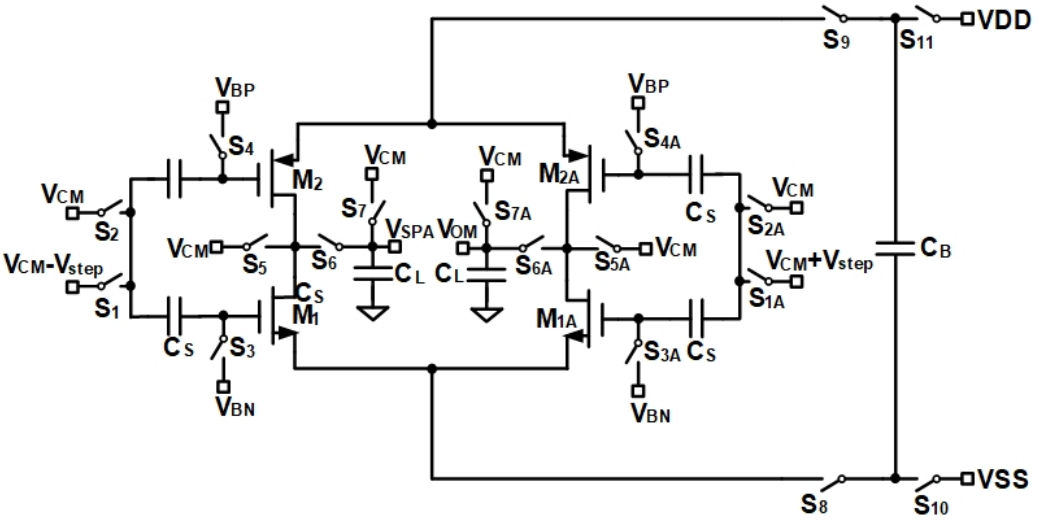


Figure 3.6: Schematic of the PVT-sensing amplifier

2 about the PVT-sensing amplifier, we want to use a signal-pole amplifier, of which the time constant τ should be much greater than the amplification period t_{ramp}. The active part of the PVT-sensing amplifier is implemented

Name	Device Type	Size
M_1/M_{1A}	NMOS hvt	$30\mu m/1\mu m$
M_2/M_{2A}	PMOS hvt	$60\mu m/1\mu m$
C_S	MoM Capacitor	$195fF$
C_L	MoM Capacitor	$313fF$
C_B	MoM Capacitor	$3.16pF$

Table 3.6: Table of the device of the PVT-sensing amplifier

by the long-channel high-threshold-voltage MOSFETs to increase the output resistance R_{out}. The battery capacitor C_B is chosen to be 10 times larger than the load capacitor C_L to attenuate the variation of the source voltage.

Table 3.7 lists the switch information. For the PVT-sensing amplifier, the requirement for linearity is not as strict as the CDL dynamic amplifier. So the linearity of the NMOS and CMOS switches are good enough to satisfy our demand.

Name	Switch Type	Size Dimension	Activated Phase
S_1/S_{1A}	NMOS lvt	$3.6\mu m/40nm$	ϕ_{RST}
S_2/S_{2A}	NMOS lvt	$1.2\mu m/40nm$	ϕ_{AMP}
S_3/S_{3A}	NMOS lvt	$1.2\mu m/40nm$	ϕ_{RST}
S_4/S_{4A}	NMOS lvt	$1.2\mu m/40nm$	ϕ_{RST}
S_5/S_{5A}	NMOS lvt	$3.6\mu m/40nm$	ϕ_{RST}
S_6/S_{6A}	CMOS	N($1.2\mu m/40nm$) P($3\mu m/40nm$)	ϕ_{AMP}
S_7/S_{7A}	NMOS lvt	$3.6\mu m/40nm$	ϕ_{RST}
S_8/S_9	CMOS	N($9.6\mu m/40nm$) P($19.2\mu m/40nm$)	ϕ_{AMP}
S_{10}/S_{11}	CMOS	N($9.6\mu m/40nm$) P($19.2\mu m/40nm$)	ϕ_{RST}

Table 3.7: Table of the switches of the PVT-sensing amplifier

3.5 Bias Circuit

The schematic of the bias circuit is presented in Figure 3.7. The reference current I_{BIAS} is designed to be from an off-chip current source. In simulation on spectre, an ideal current source is utilized. Since the PVT-sensing amplifier is designed to track the PVT variation of the CDL dynamic amplifier, they have to share the same bias voltage V_{BN} and V_{BP}. The device dimension of the bias circuit is the same as that of the CDL dynamic amplifier.

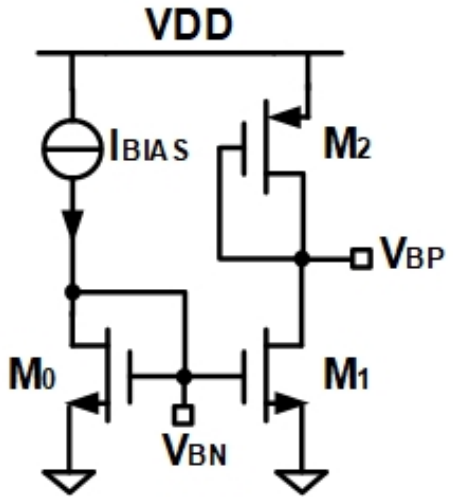


Figure 3.7: Schematic of the bias circuit

Name	Device Type	Size
M_0	NMOS hvt	$16\mu m/40nm$
M_1	NMOS hvt	$16\mu m/40nm$
M_2	PMOS hvt	$32\mu m/40nm$
I_{BIAS}	Reference Current Source	$20\mu A$

Table 3.8: Table of the device of the bias circuit.

Chapter 4

Simulation Results

The PVT-robust dynamic amplifier is implemented in the 40nm technology and simulated by spectre. The simulation also illustrates the relation between the linearity and the amplification period of the CDL dynamic amplifier.

4.1 CDL Dynamic Amplifier

4.1.1 Test Setup

The block diagram of the CDL dynamic amplifier testbench is shown in Figure 4.1. For testing the CDL dynamic amplifier, the main target is to find the optimized time t_{opt}, when the transient gain is signal-independent. To reduce the disturbance of the noise floor, the sample number should be 2048 or more. From the specification, the required sample frequency is 51.2MS/s. It means the total sampling time should be over $46\mu s$. Our targeted linearity, which is over 80dB, requires high accuracy of the simulator. For the transient simulation, the max step is set to $100ps$ and the simulated voltage tolerance "*vabstol*" is set to 10^{-9}. However, we need to run the simulation many times for tuning the amplification period. The simulation and tuning for the CDL

dynamic amplifier are time-consuming tasks.

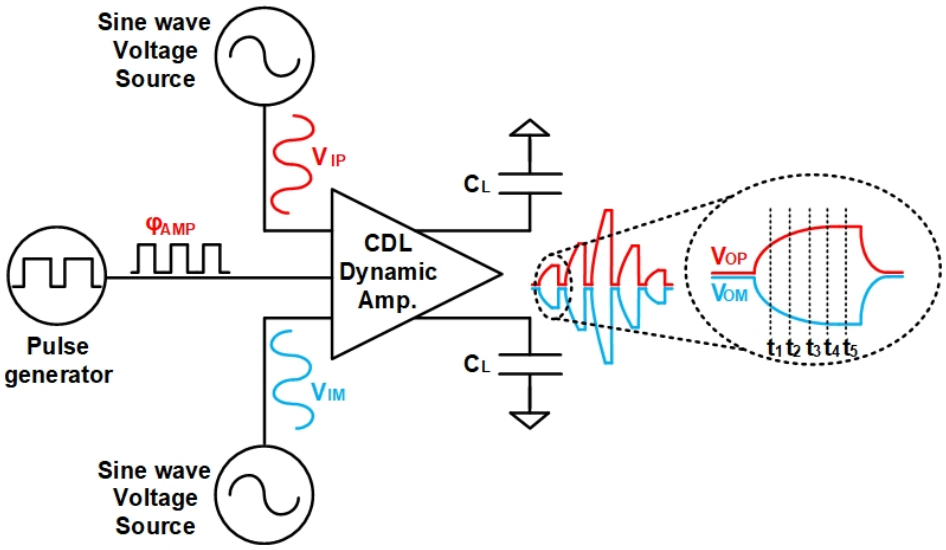


Figure 4.1: Block diagram for the CDL dynamic amplifier testbench

To reduce the workload of the simulation and tuning, we proposed a smart testbench to find the optimized time quickly. As shown in Figure 4.1, the pulse width of the amplification control signal ϕ_{AMP} is design to be redundant. It means we intentionally activate the dynamic amplifier, to amplification phase, for a sufficiently long time. After one long-time simulation, we sampled the output voltage with same period but at different start time. In Figure 4.1, these t_1, t_2, t_3, t_4, and t_5 indicate the different start time, which is the amplification period t_{AMP}. Then do fast Fourier transform (FFT) for these sampled data, we can get the graph that t_{AMP} versus THD, which will be shown in next section. The time exhibiting the lowest THD is the optimized time t_{opt}. In this thesis, we sampled the amplified voltage at an interval of

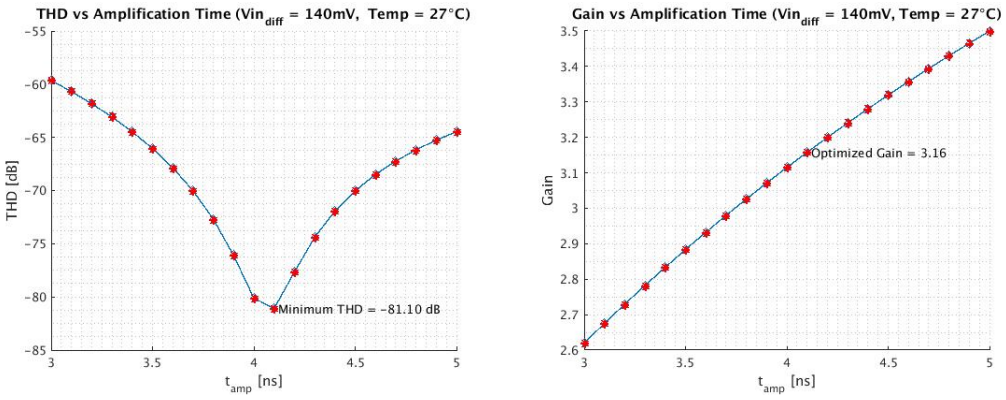
$0.1ns$ starting from $3ns$ to $12ns$.

In fact, in this quick smart testbench, we ignore the delay of the bootstrapped switches and other non-ideal effects when the output switches start to hold the amplified voltage. The actual optimized time is shifted a bit from that of the fast testbench. A couple of tuning trials in the conventional way are still needed. Besides, the accuracy of the simulation result also depends on the integration algorithm of the simulator. Using different integration algorithm, we may get different THD from the same testbench with the same amplification period.

4.1.2 Linearity

The result of THD versus the amplification period t_{amp} is shown in Figure 4.2a. It is clear that there exists an optimized time that the amplifier presents high linearity. Figure 4.2b also shows the curve of the the corresponding gain versus t_{amp}.

The simulation are performed at 51.2MS/s sample speed with a 140mV differential peak-to-peak input signal at room temperature. The expected gain is around 3. Figure 4.2a indicates that the THD is below 80dB when the amplification period t_{amp} is 4.1ns, which is actually the optimized time, and the optimized gain is around 3.16.



(a) THD vs t_{amp} (b) Transient gain vs t_{amp}

Figure 4.2: Simulation results of the quick testbench for the CDL dynamic amplifier

4.2 PVT-stabilized CDL Dynamic Amplifier

After we run the simulation for a few times and finish tuning the CDL dynamic amplifier, the optimized time t_{opt} is acquired and will be used in top-level simulation. We combine all blocks, the CDL dynamic amplifier, the V2T converter, and the PVT-sensing amplifier, and then test them robustness against the variation of temperature and supply.

4.2.1 Test Setup

The block diagram of the testbench is shown in Figure 4.3. There are three calibration "knobs", I_{BIAS}, $V_{REF,N}$, and $V_{REF,P}$. I_{BIAS} is the bias circuit reference current, provided by an off-chip current source. $V_{REF,N}$ and $V_{REF,P}$ are the reference voltage sources used for the N-side and P-side V2T converter.

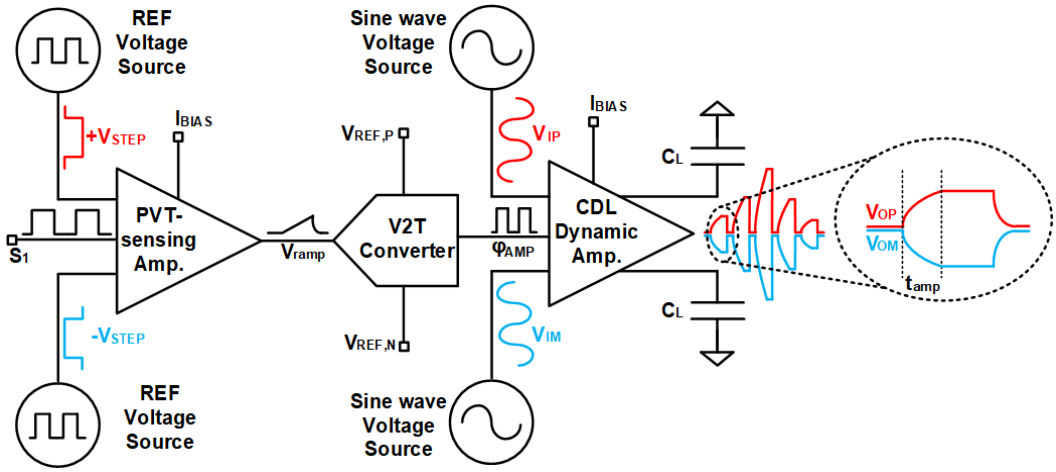


Figure 4.3: Block diagram of the proposed dynamic amplifier testbench

First, tune I_{BIAS} to make the optimized time t_{opt} within the tolerated range, which is around $4ns$ in this thesis. Second, tune $V_{REF,N}$ and $V_{REF,P}$ to make the V2T converter generating the amplification control signal. After a few trials, the amplification period for the CDL dynamic amplifier is matched to the optimized time. Finally, the dynamic amplifier is controlled by a PVT-stabilized timer and the calibration is done.

With the sample clock performed, which is 51.2MS/s, a sinusoidal input voltage is connect to the input of the CDL dynamic amplifier and the amplified output voltage is sampled at the hold phase. The sampled output data is processed by running the fast-Fourier transform (FFT) in MATLAB. The simulation is repeated for many times at different temperature and different supply voltage. In the end, we acquire the relation curve about the relation between the THD and gain variation versus the temperature and supply fluctuation. Meanwhile, a conventional CDL dynamic amplifier is also tested at

the same temperature and supply voltage as this work. But its amplification period is fixed after the calibration. Both structures are calibrated at $27°C$ under 1.2V supply voltage. The sinusoidal input exhibits 140mV peak-to-peak differential voltage and $13.5M$Hz input frequency.

4.2.2 Temperature Variation

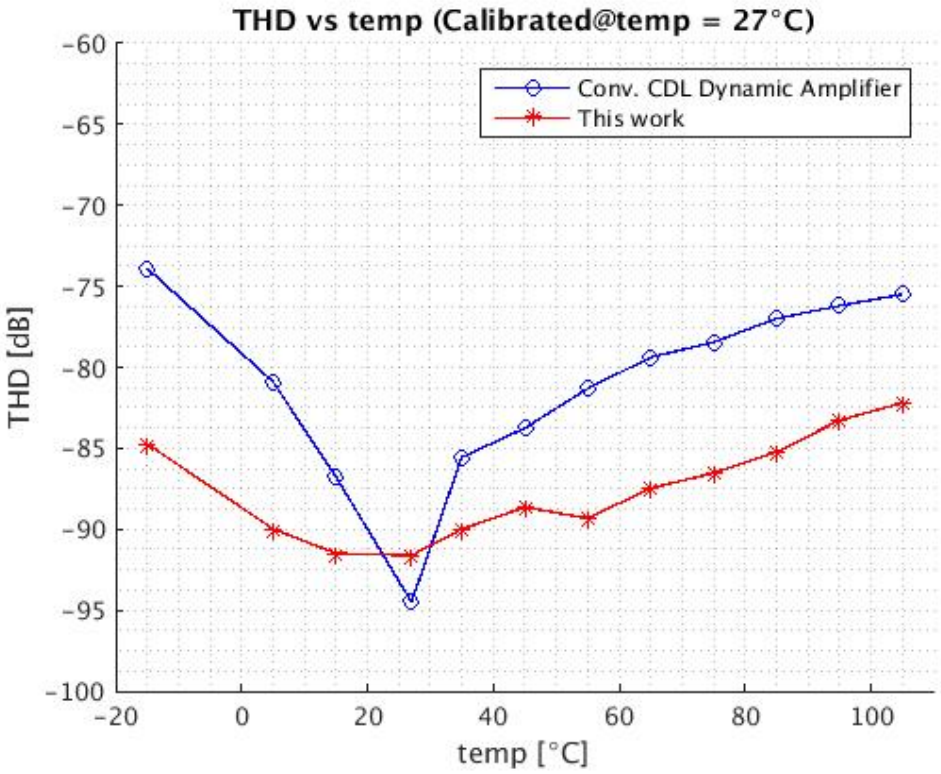


Figure 4.4: Simulation results of the THD versus temperature

Figure 4.4 presents the THD versus temperature variation. From $-15°C$ to $100°C$, the THD of our design remains less than -80dB. Compared to the conventional one, the linearity of proposed design is 10dB better. Note that

at the calibrated point ($27°C$), the 3dB discrepancy of the THD between this work and the conventional one is from the integration algorithm calculation mismatch of the simulator.

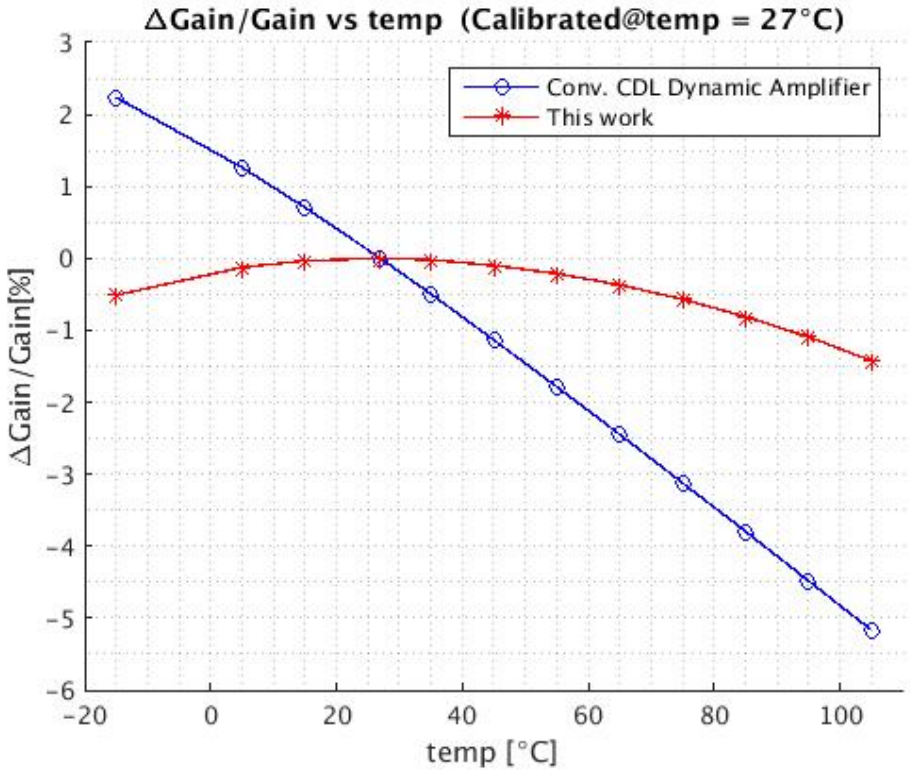


Figure 4.5: Simulation results of the gain variation versus temperature

Figure 4.5 shows the gain variation versus the temperature. The optimized gain at $27°C$ is 3.03. Ranging from $-15°C$ to $100°C$, the proposed dynamic amplifier only suffers from less than 1.5% gain variation. However, the gain variation of the conventional CDL dynamic amplifier is from 2% to -5%. We can conclude that our design provides a more stable gain than the conventional CDL amplifier with harsh temperature variation.

4.2.3 Supply Variation

Figure 4.6 exhibits the relation between the linearity of the amplifier and the supply voltage variation. With the supply voltage varying from 1.15V to 1.25V, the THD of this work is still less than −75dB, providing 6dB better linearity than the conventional work. It shows that the deterioration of linearity of the CDL dynamic amplifier is reduced by using our technique.

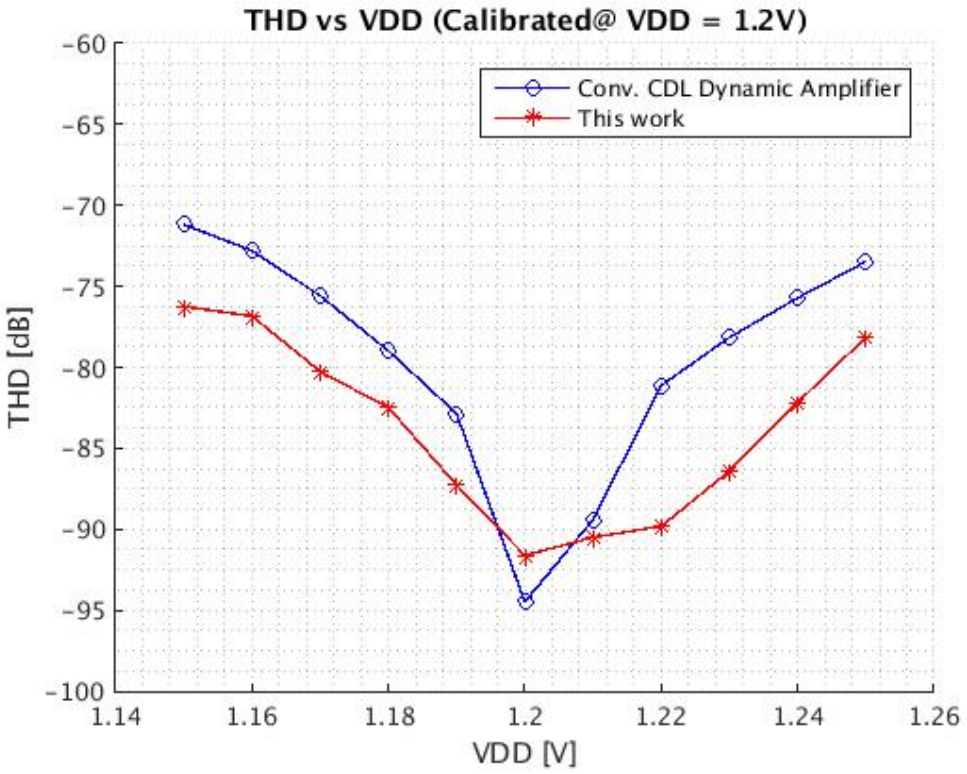


Figure 4.6: Simulation results of the THD versus supply voltage

When it comes to the influence of the supply voltage variation on the gain of the dynamic amplifier, our design also behaves outstandingly. Figure

4.7 illustrates that even though supply voltage varys from 1.15V to 1.25V, the gain variation of this work is still less than ±2.5%. Moreover, the conventional CDL amplifier suffers from the nearly double gain variation, which is from −4% to +4%. Similarly, our technique relieves the issue that the gain varies with the supply voltage.

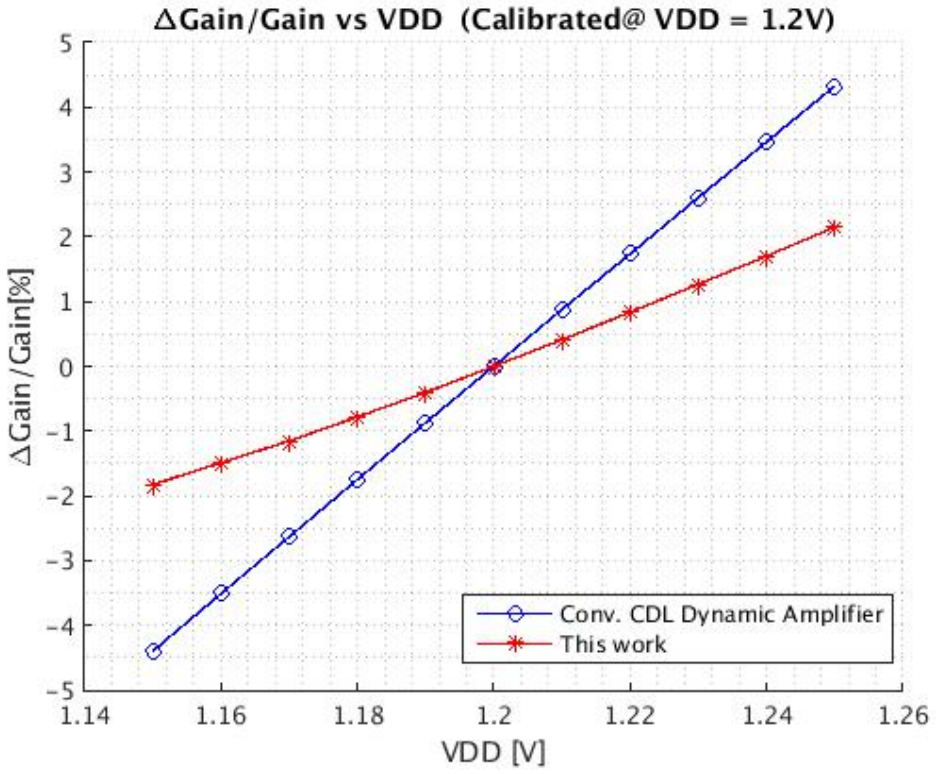


Figure 4.7: Simulation results of the gain variation versus supply voltage

Chapter 5

Conclusion and Future Work

5.1 Conclusion

This thesis presents a PVT-robust high-linearity dynamic amplifier. By combining the capacitively degenerated linearization method and the PVT-stabilized technique, the proposed dynamic amplifier exhibits high-linearity and stable gain with the PVT variation. The amplification period of the dynamic amplifier is controlled by the combination of a PVT-sensing amplifier and a V2T converter. They track the PVT variation of the CDL dynamic amplifier and keep the amplification period matched to the optimized time. Compared to the conventional CDL amplifier, this work only needs one-time calibration rather than multiple periodic background and foreground calibrations against the PVT variation. Once the calibration is done, the proposed dynamic amplifier will provide high-linearity and stable gain. Compared to the work in [12], the high-linearity feature of our work makes the dynamic amplifier more suitable as the residue amplifier for higher-speed pipeline ADC.

The simulation results indicate that the circuit provides less than -80dB total-harmonics-distortion (THD) ranging from $-15°C$ to $100°C$ with 140mV peak-to-peak differential sinusoidal input. When supply voltage varies from

1.15V to 1.25V, the gain variation of this design is within $\pm 2.5\%$ and the THD is less than -75dB.

5.2 Future work

This design illustrates the idea of designing a PVT-robust high-linearity dynamic amplifier, while there is still much to be done to tape out and for future research.

First of all, the process variation is still showing its influence. For a different process, the optimized time is different. Besides, the mismatch between the PVT-sensing amplifier and the CDL dynamic amplifier may worsen the their correlated response for the PVT variation. This thesis does not include the results of the process variation and we expect to reduce the mismatch effect.

Secondly, this dynamic amplifier structure needs three calibration knobs. It may increase the workload of calibrating the circuit. For future work, the reduction of the calibration nodes and trials is expected.

Thirdly, the noise from the PVT-sensing amplifier and the V2T converter occupies a large part of the total noise budget. Even though the PVT-sensing amplifier utilizes the dynamic technique, which consumes power only when it is activated, the V2T converter still consumes a lot of power during the auto-zero mode and conversion phase. Self-control and compensation methods as [1, 2] show their advantages for low-noise feature. We expect to build up a

low-noise, high-linearity, and PVT-robust dynamic amplifier in the future.

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