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Analysis of Single Amplifier Biquad Based Delta-Sigma Modulators

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Analysis of Single Amplifier Biquad Based Delta-Sigma Modulators

by

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Dedicated to my parents.

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Abstract

Analysis of Single Amplifier Biquad Based Delta-Sigma Modulators

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The University of Texas at Austin, 2019

Supervisor: Nan Sun

Continuous-time delta-sigma modulators (CT DSMs) are becoming a popular choice for high speed and high resolution applications. One of the challenges in their design is the loop filter power consumption, which increases with the modulator order. To alleviate this problem, single amplifier biquads (SABs) have been used. This report presents an analysis of finite gain, UGB effect and thermal noise of the biquads. Furthermore, an extension to the T network biquad is proposed for implementing a fourth order transfer function and is compared against the conventional architecture. The proposed topology requires only two OTAs to realize the transfer function. However, further analysis shows that the system becomes more sensitive to the finite UGB of the OTA.

Table of Contents

List of Tables

List of Figures

x

Chapter 1

Analog to Digital Converters

1.1 Introduction

Digital processors have seen a huge growth in their production as well as their market. They benefit from a low power implementation and scalable technologies. Digital signals are easier to process and store because they have defined levels. They are also less prone to noise as compared to analog signals [3]. Due to these advantages, the analog signals are converted to digital by means of an analog to digital converter (ADC) for processing. However, use of an ADC presents a bottleneck to the whole system performance, which might get limited by the ADC speed, power, etc. Therefore, choosing the right ADC for an application becomes very important.

1.2 ADC Architectures

Fig. 1.1 shows the different ADC types categorized by their bandwidth and resolution. Their description is as follows:

- Flash ADCs are used in very high speed applications which do not require high resolution. For n-bits, these require 2^n comparators which can result in significant power consumption and area with increasing resolution.
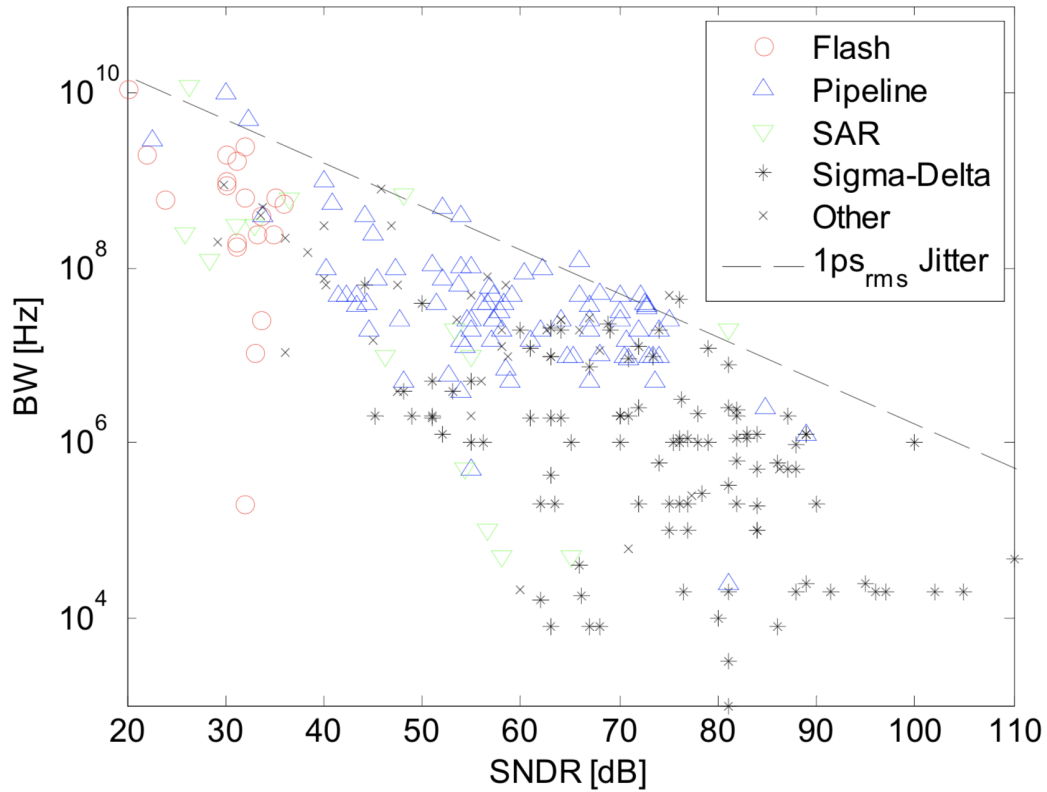
Figure 1.1: Bandwidth vs SNDR data for different ADC architectures [2]

Moreover, the requirement of high resolution places stringent constraints on the comparator sizes and causes their area to increase.

- Pipelined ADCs are used in applications that require high resolution and medium to high speeds. The ADC operation is divided between several stages with an inter-stage gain to relax the design of subsequent stages. Each stage output is then combined to get the required resolution. The drawback in their design is the latency, which increases with the number of stages.

- Successive Approximation ADCs, or SAR, use only a single comparator with binary search operation for analog to digital conversion. Since they require mostly digital components with just one comparator and a DAC, they can provide a power efficient implementation. They are well suited for medium resolution, low speed and very low power applications. One of the limiting factors in their design is the matching requirement in the DAC.

- Delta-sigma modulators provide the highest resolution using the over-sampling technique. However, this resolution is achieved at the expense of speed. They can be further categorized into discrete-time and continuous-time ADCs. More discussion on these ADCs has been provided in the later chapters of this thesis.

1.3   Static Performance Parameters

The static metrics used to measure an ADC performance are shown in Fig. 1.2 and are given below-

- **Offset:** It is a measure of shift in the start point of the ADC output vs input voltage characteristics, compared against its ideal value. Offset is not an issue in most designs as it can be easily calibrated digitally after fabrication.

- **Gain Error:** It is measured after the offset has been calibrated out and can be quantified as the shift in the end point of the ADC output vs

3
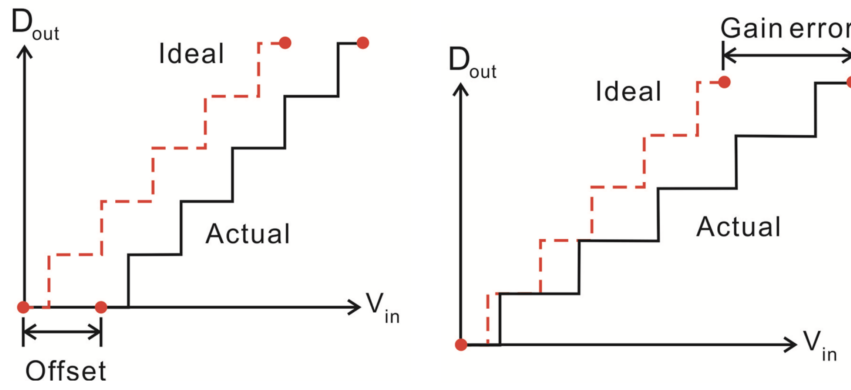
(a) Offset (b) Gain error
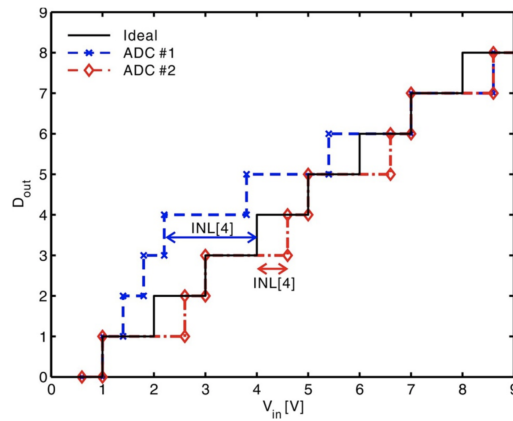
(c) Integral Non-Linearity (INL)

Figure 1.2: Static performance parameters [2]

input voltage characteristics. Similar to offset, gain error can also be easily calibrated digitally.

- **Differential Non-Linearity (DNL):** Ideally, all ADC codes should have uniform width. But mismatch in the ADC can cause the width to vary across different codes. DNL is the measure of this code width

4

deviation from its average value. It is given by the following formula-

$$\text{DNL}[k] = \frac{W[k] - W_{avg}}{W_{avg}}$$

where

$$W[k] = T[k+1] - T[k]$$
$$W_{avg} = \frac{\sum_{k=1}^{N} W[k]}{N}$$

$T[k]$ is the input for which the ADC output makes transition to the kth code. DNL of -1 for an ADC implies that it has a missing code.

- **Integral Non-Linearity (INL):** It is the measure of deviation of ADC characteristics from its ideal value. It can be calculated using the following formula-

$$\text{INL}[k] = \frac{T[k] - T_0[k]}{W_{avg}}$$
$$\text{INL}[k] = \sum_{i=1}^{k-1} \text{DNL}[i]$$

Both INL and DNL are measured after correcting for gain and offset errors.

1.4 Dynamic Performance Parameters

The dynamic metrics used to measure an ADC performance are given below-

- **Signal-to-Noise Ratio (SNR):** It is defined as the ratio of signal power to total noise power, which excludes DC, input bin and the all harmonics between 2nd and 7th.

- **Signal-to-Noise+Distortion Ratio (SNDR)**: SNDR is calculated as the ratio of signal power to total noise and distortion power, which excludes only the DC bin and the input bin. It is also used to compute the effective number of bits (ENOB), which is given as-

$$\text{ENOB} = \frac{\text{SNDR(dB)} - 1.76}{6.02}$$

- **Spurious Free Dynamic Range (SFDR):** It is the ratio of the signal power to power of the largest spur, which need not be an input harmonic.

- **Dynamic Range (DR):** It is defined as the ratio of the maximum signal power to the minimum detectable signal power, which is the input power that results in 0 dB SNR.

Chapter 2

Continuous-Time Delta-Sigma Modulators

2.1 Introduction

Applications such as wireless communication require high resolution and high bandwidth analog to digital converters (ADC) [4][5]. Delta-sigma modulators (DSM) are a great fit for these applications as they provide very good resolution compared to other ADC architectures. Discrete-time (DT) DSM have a high dynamic range but are limited in speed and have a high power consumption. Continuous-time (CT) DSM are a better fit as they can satisfy the high bandwidth requirement while consuming less power than their DT counterpart. Their bandwidth has already been pushed to the range of several megahertz [6].

CT DSM use oversampling technique that allows for a high resolution. They posses inherent anti-alias filtering, and can therefore, relax design requirement of the AAF (anti-alias filter). Unlike DT modulators, sampling operation is performed before the quantizer and not at the modulator input. Furthermore, CT DSM requires a compensation path for the excess loop delay (ELD) in the system. The main building blocks in CT-DSM along with the ELD block are shown in Fig. 2.1 and are discussed below.
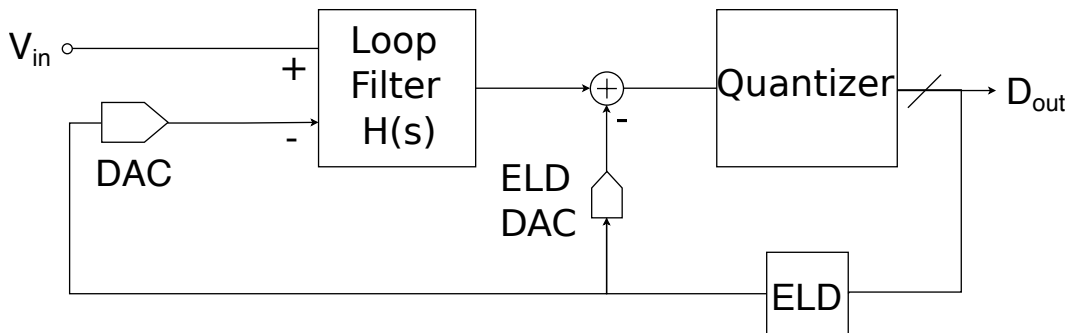
Figure 2.1: Delta-Sigma modulator block diagram

2.2 Loop Filter

In a CT system, loop filter generally consists of either active R-C or Gm-C integrators. R-C integrators have good linearity performance, attained at the expense of a power hungry OTA. Gm-C integrators, on the other hand, can be more power efficient but are limited by their input range [7].

Typically, loop filter takes up a significant amount of power budget and is therefore, important to optimize in order to achieve a low power implementation. Furthermore, the first OTA and the summing amplifier are bottlenecks when it comes to loop filter power. The first OTA power is governed by its noise and linearity requirements, while the last OTA power is usually determined by its output settling requirement due to the DAC pulses.

Use of single amplifier biquad allows to implement a second order transfer function with only one OTA. These have been discussed in detail in the later sections. Another technique to reduce power was presented in [5], which targeted the power hungry summing operation. The technique was shown to

8

be effective for high speed applications.

2.3 Quantizer

This block converts the sampled filter output to a digital code, which then goes to a decimation filter for filtering and down-conversion. Additionally, it can be used to provide an extra order of shaping. For example, this concept has been demonstrated by implementation of noise shaping quantizers like VCO based quantizers in [8] and noise-coupling technique in [9]. Adopting these methods can relax the loop filter design and allow for a more power efficient implementation. However, as mentioned in [4], they place some other constraints on the modulator in terms of speed and linearity.

2.4 Digital to Analog Converter (DAC)

CT operation requires the digital output code to be converted to analog by means of a DAC while closing the feedback loop. Mismatches in this block are a dominant source of modulator non-linearity and hence, DAC needs a careful design and layout. Additionally, for high linearity applications dynamic element matching (DEM) is performed which shapes the mismatch errors.

DAC is also a critical element when it comes to clock jitter sensitivity. As mentioned in [10], return-to-zero (RZ) DACs are more sensitive to jitter than non return-to-zero (NRZ) DACs. Switched capacitor DACs are the least sensitive to jitter but they compromise anti-alias filtering of the modulator [11].

This issue was addressed in [12] with their proposed dual switched capacitor RZ DAC.

2.5   Excess Loop Delay (ELD)

All quantizers require a finite amount of time for proper settling of their outputs. Also, the DEM block consumes extra time if it is used for enhancing DAC linearity. To account for these, the DAC clock is delayed by a fixed amount which introduces ELD in the loop and hence causes instability. To compensate for this delay, a direct path from DAC to quantizer input is required. Higher the delay, higher is the gain of this direct feed-forward path. It is very crucial for modulator stability and dominates the UGB requirement of the summing amplifier.

2.6   Zero Optimization

In scenarios where OSR is small, zero optimization becomes an important technique to improve SQNR of the modulator. For the same, NTF zeros need to be moved from DC such that they become imaginary, which creates a notch in the transfer function. Since NTF zeros are the same as loop filter poles, zero optimization can be achieved by placing two integrators in a negative feedback, resulting in a resonator. This shifts the loop filter poles from DC to the imaginary axis, thereby, realizing NTF zeros at the required location. Fig. 2.2 shows the NTF and its pole-zero map for a fourth order modulator having one pair of optimized zeros. Also, Table 2.1 shows the optimized zero

location and SQNR as a function of the filter order. It can be seen that higher order filters benefit more from zero optimization.
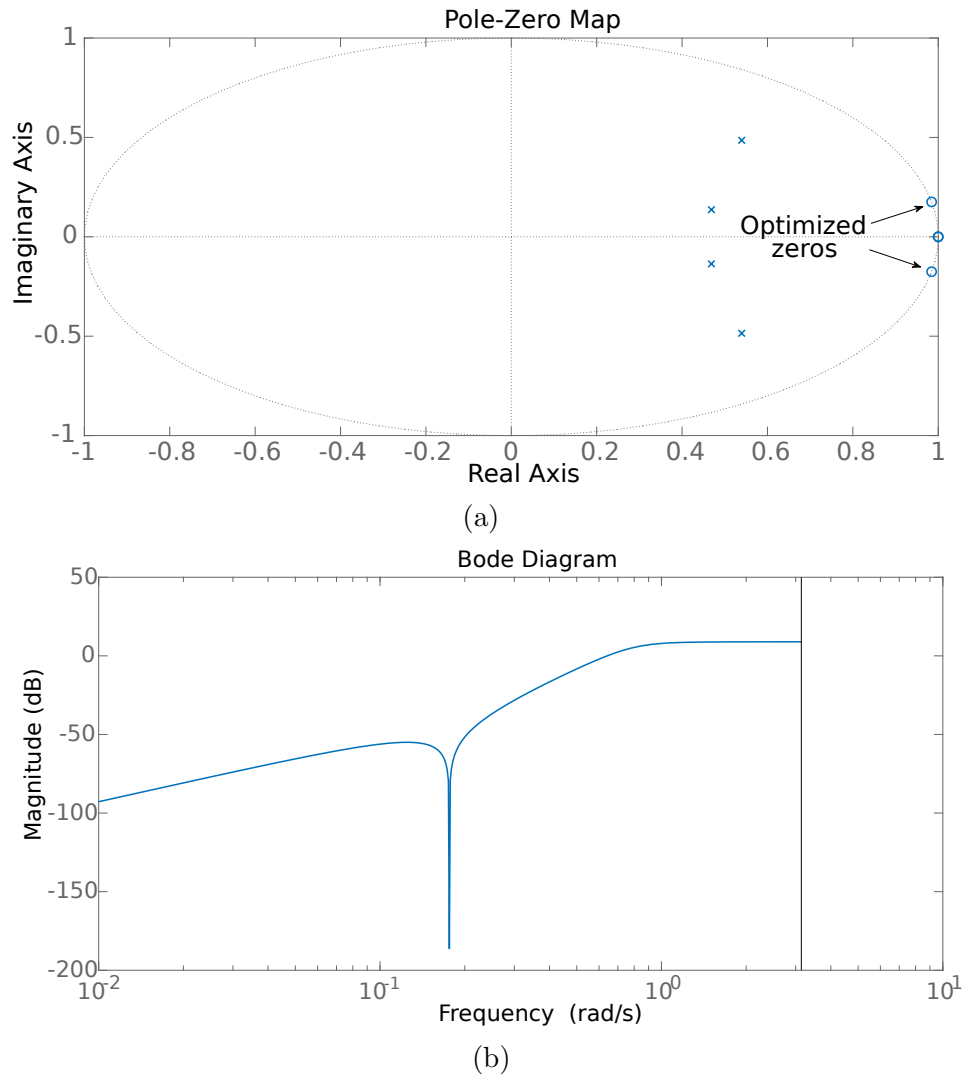

(a)

(b)

Figure 2.2: Zero optimized NTF for a fourth order modulator- pole-zero map and magnitude plot

Order	Optimized Zeros Relative to Bandwidth	SQNR Improvement (dB)
1	0	0
2	$\pm\frac{1}{\sqrt{3}}$	3.5
3	$0, \pm\sqrt{\frac{3}{5}}$	8
4	$\pm\sqrt{\frac{3}{7} \pm \sqrt{\left(\frac{3}{7}\right)^2 - \frac{3}{35}}}$	13

Table 2.1: Optimized zero locations [1]

2.7   DT to CT Conversion

The method used to design the loop filter has been explained in this section. Once the filter order, OSR and out-of-band gain was decided, NTF for a DT-DSM was obtained using Schreier's toolbox [13] on MATLAB. This was further used to obtain the DT loop filter transfer function as-

$$H(z) = \frac{1}{\text{NTF}(z)} - 1$$

To account for DAC in the path, CT filter had to be designed such that its response to a delayed pulse (assuming NRZ DAC and ELD), sampled every clock cycle, should be the same as the impulse response of the DT filter [10]. For example, if for a second order system coefficient of $1/s$ and $1/s^2$ path is k_1 and k_2 respectively, while k_0 is the ELD path gain, then-

$$\begin{bmatrix} l_0[1] & l_1[1] & l_2[1] \\ l_0[2] & l_1[2] & l_2[2] \\ & \vdots & \\ l_0[n] & l_1[n] & l_2[n] \end{bmatrix} \begin{bmatrix} k_0 \\ k_1 \\ k_2 \end{bmatrix} = \begin{bmatrix} h_1[1] \\ h_1[2] \\ \vdots \\ h_1[n] \end{bmatrix}$$

where $l_0[n]$ is the sampled pulse (delayed) response of ELD path, $l_1[n]$ is the response of $1/s$ path, $l_2[n]$ is the response of $1/s^2$ path and $h[t]$ is the impulse

response of DT loop filter. This equation can be used to compute k_0, k_1 and k_2.

Chapter 3

Single Amplifier Biquad (SAB) Filters

In a CT-DSM, power consumption in the loop filter is an important concern for designers. To improve upon this aspect, single amplifier biquad (SAB) filters have been employed [4][6][14]. Fig. 3.1 shows two of the commonly used SAB structures, the T network and the self-coupled (SC) biquad. The self-coupled biquad uses positive feedback to achieve the extra order and requires $C_{2,SC}$ to be equal to $C_{1,SC}$, whereas, T network SAB has no such matching requirement. The transfer function for T network and SC biquad is-

$$H_t(s) = \frac{1 + sR_{2,t}(C_{1,t} + C_{2,t})}{s^2 R_{1,t} R_{2,t} C_{1,t} C_{2,t}} \tag{3.1}$$

$$H_{sc}(s) = \frac{1 + sR_{2,sc}C_{2,sc}}{s^2 R_{1,sc} R_{2,sc} C_{1,sc} C_{2,sc}} \tag{3.2}$$

To implement the same transfer function, $R_{2,sc} = 4R_{2,t}$ and $C_{sc} = C_t/2$ must hold, where $C_{1,sc} = C_{2,sc} = C_{sc}$ and $C_{1,t} = C_{2,t} = C_t$. It can be seen that the capacitance needed in SC biquad is half compared to the capacitance needed in T network biquad. Therefore, SC biquad is more efficient in terms of area.

The impact of finite gain and UGB as well as noise analysis has been carried out in the following sections. For the same, comparison of the two
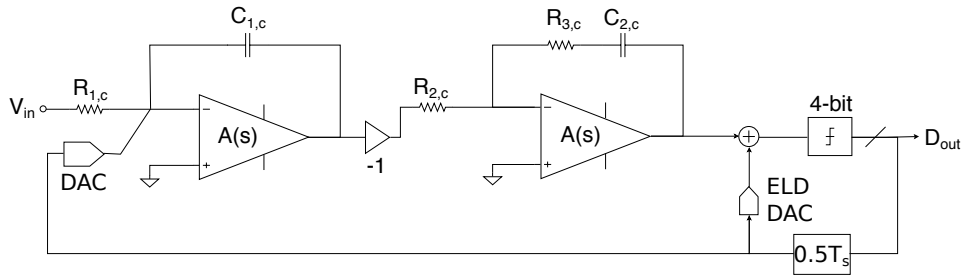
(a) Conventional Filter
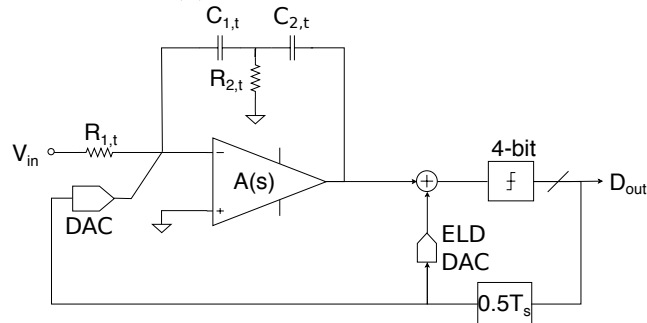
(b) T network SAB

(c) Self Coupled (SC) SAB

Figure 3.1: Second order filter implementations

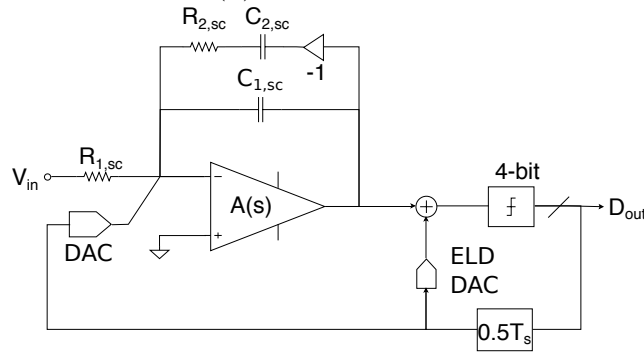topologies has been made with the conventional method of implementing a loop filter as shown in Fig. 3.1. The three modulators under test are second order with an OSR of 32 and a 4-bit quantizer. The ELD path has been implemented with a separate adder which is considered to be ideal. The analysis is similar

15

to the one carried out in [4] and [15]. The desired CT loop filter transfer function (normalized to sampling frequency) for half cycle ELD is-

$$H(s) = \frac{1.66}{s} + \frac{0.75}{s^2} = \frac{1.66s + .75}{s^2} \qquad (3.3)$$

3.1 Finite Gain Impact

Assuming finite gain and infinite bandwidth, the OTA transfer function $A(s)$ is equal to A_{DC}. Employing this OTA model, Fig. 3.2 shows the loop filter pole-zero map and NTF for the conventional architecture. Its loop filter transfer function is as follows-

$$H_c(s) = \frac{1 + sR_{3,c}C_{2,c}}{s^2 R_{1,c}R_{2,c}C_{1,c}C_{2,c}} E_{1,c}(s)E_{2,c}(s) \qquad (3.4)$$

where,

$$E_{1,c}(s) = \frac{sA_{DC}R_{1,c}C_{1,c}}{1 + s(1 + A_{DC})R_{1,c}C_{1,c}} \qquad (3.5)$$

$$E_{2,c}(s) = \frac{sA_{DC}R_{2,c}C_{2,c}}{1 + s[(1 + A_{DC})R_{2,c}C_{2,c} + R_{3,c}C_{2,c}]} \qquad (3.6)$$

In Equation 3.4, the two DC poles are cancelled by DC zeros (Equations 3.5 and 3.6). Effectively, finite gain of the OTA pushes filter poles from DC to the left half plane with the zero location unaffected. This shifting of poles saturates the NTF at low frequencies and results in an increased in-band quantization noise, thus, degrading the SQNR.

For a T network biquad, the transfer function is as follows-

$$H_t(s) = \frac{A_{DC}(1 + sR_{2,t}(C_{1,t} + C_{2,t}))}{1 + s(R_{1,t}C_{1,t} + R_{2,t}(C_{1,t} + C_{2,t})) + s^2(1 + A_{DC})R_{1,t}R_{2,t}C_{1,t}C_{2,t}}$$
$$(3.7)$$

16
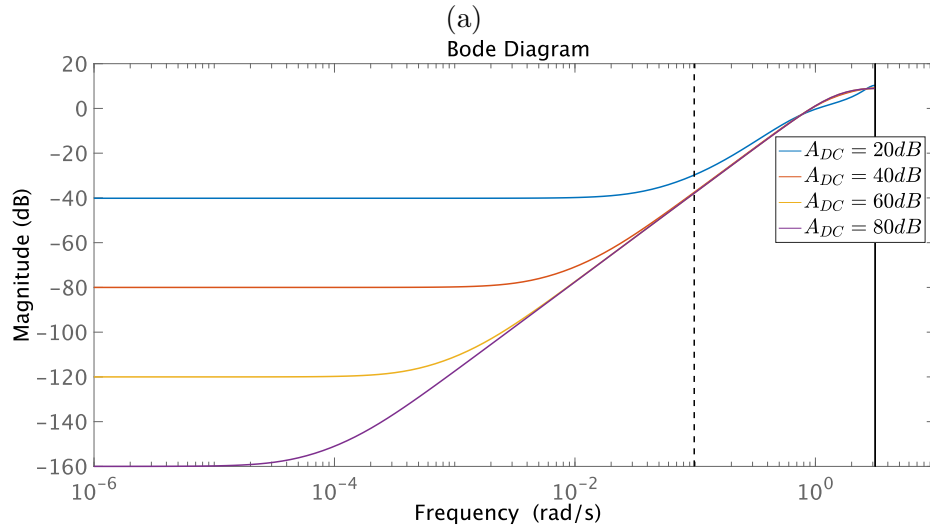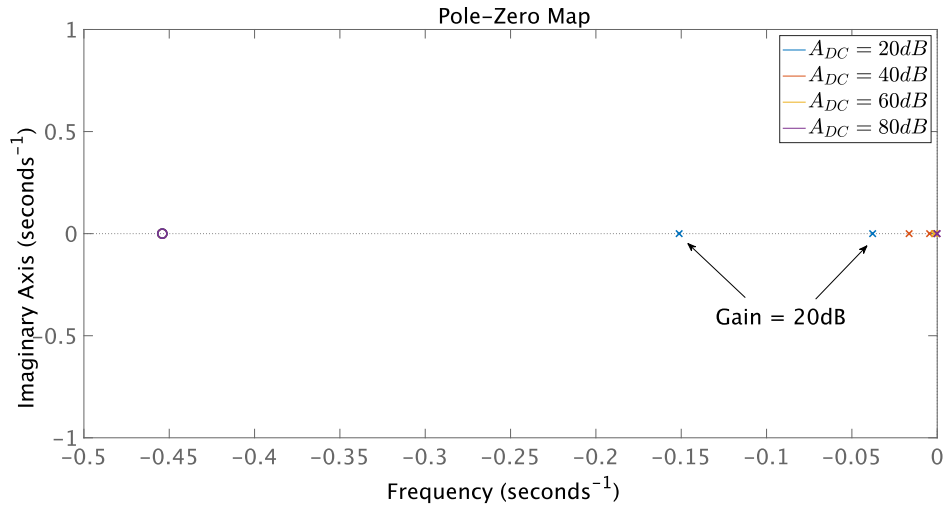
Figure 3.2: Conventional modulator- Loop filter pole-zero map and NTF with finite OTA gain

Its loop filter pole-zero map and NTF are shown in Fig. 3.3. In this case, the filter poles are not only shifted to the left half plane but also are

(a)

(b)
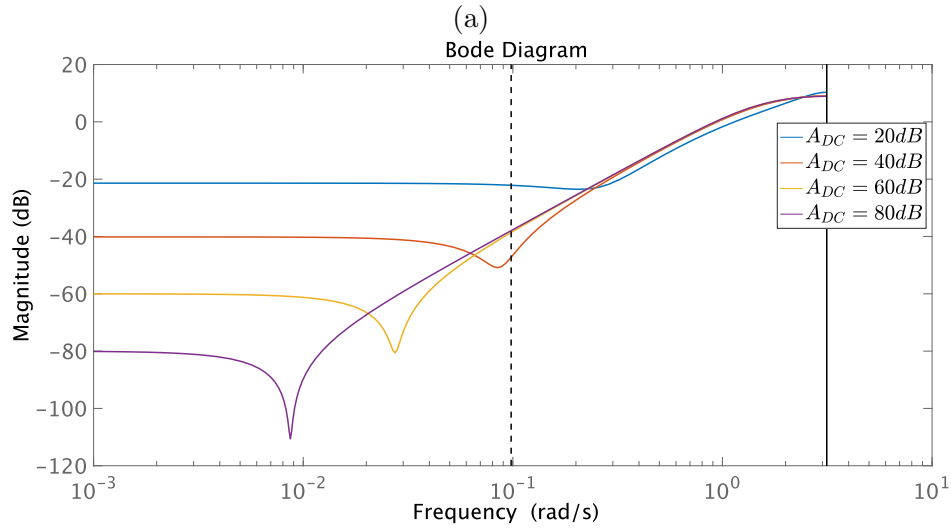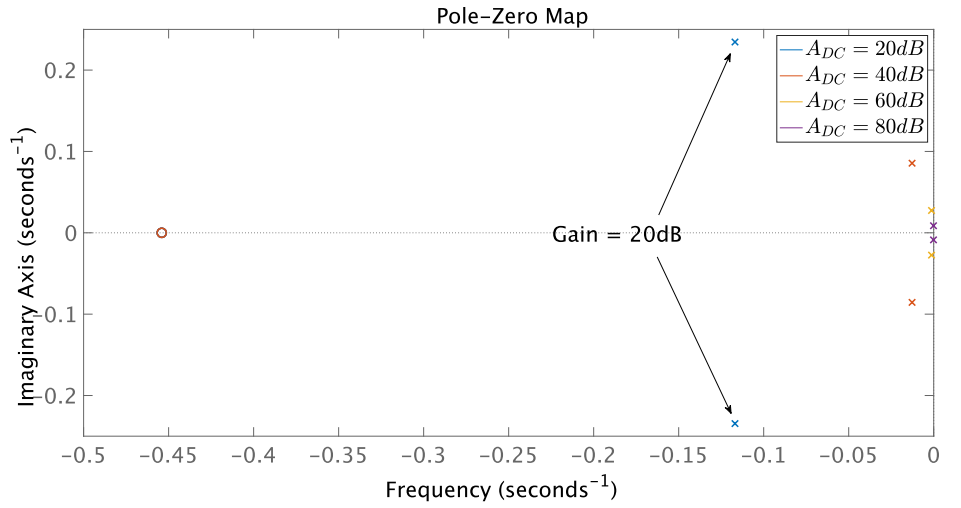
Figure 3.3: T network SAB- Loop filter pole-zero map and NTF with finite OTA gain

becoming a complex number. An interesting consequence of this is the appearance of peaking behavior in the loop filter transfer function. This loop filter peaking gets manifested in the NTF as a notch, similar to the case of a

18

modulator with optimized zeros. As a result, the SQNR first increases as the OTA gain reduces before it starts to fall for very low values for gain.

In case of an SC biquad, the transfer function can be written as-

$$H_{sc}(s) = \frac{A_{DC}(1 + sR_{2,sc}C_{sc})}{1 + s(2R_{1,sc}C_{sc} + R_{2,sc}C_{sc}) + s^2(1 + A_{DC})R_{1,sc}R_{2,sc}C_{sc}^2} \quad (3.8)$$

Since $R_{2,sc} = 4R_{2,t}$ and $C_{sc} = C_t/2$, the above equation is exactly the same as Equation 3.7. This implies that finite OTA gain effect is the same for both the biquad structures.

The SQNR plot against finite OTA gain for biquads and conventional architecture is given in Fig. 3.4. For high values of gain, biquads and conventional architecture result in similar values of SQNR. As the gain reduces, biquad SQNR starts to increase, as explained earlier, and displays a peak before rolling off. For this particular case, conventional architecture shows better SQNR than biquads at low values of gain. But a reasonable choice of OTA gain would be around 50dB, and at this operating point, both modulator architectures show similar performance.

3.2 Finite UGB Impact

For this analysis, OTA DC gain has been assumed to be infinite. Under this condition, its transfer function can be written as-

$$A(s) = \frac{A_0}{1 + s/\omega_0} \approx \frac{A_0\omega_0}{s} \quad (3.9)$$

19
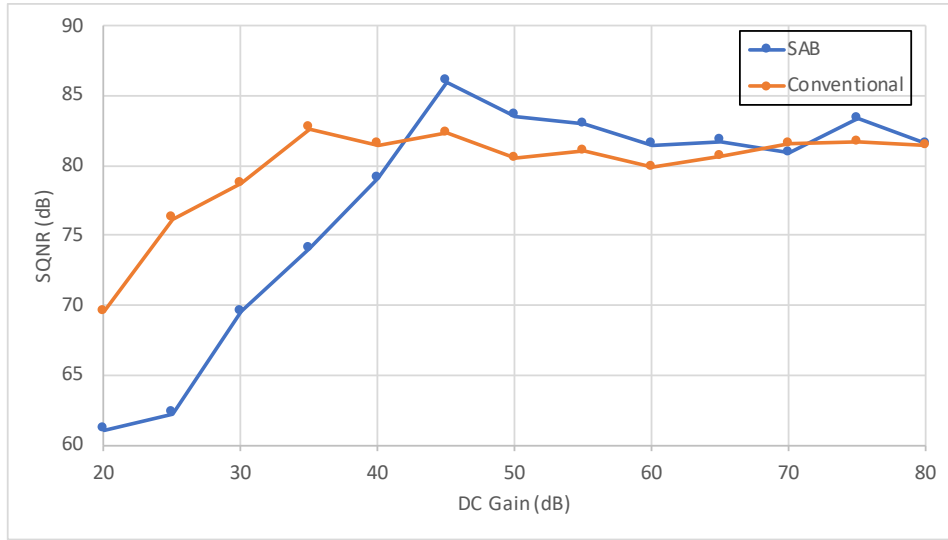
Figure 3.4: SQNR comparison with finite OTA gain

Using this model with the conventional loop filter, the transfer function can be expressed as-

$$H_c(s) = \frac{1 + sR_{3,c}C_{2,c}}{s^2 R_{1,c}R_{2,c}C_{1,c}C_{2,c}} E_{1,c}(s)E_{2,c}(s) \tag{3.10}$$

where,

$$E_{1,c}(s) = \frac{A_0\omega_0 R_{1,c}C_{1,c}}{1 + A_0\omega_0 R_{1,c1,c} + sR_{1,c}C_{1,c}} \tag{3.11}$$

$$E_{2,c}(s) = \frac{A_0\omega_0 R_{2,c}C_{2,c}}{1 + A_0\omega_0 R_{2,c}C_{2,c} + s(R_{2,c} + R_{3,c})C_{2,c}} \tag{3.12}$$

Fig. 3.5 shows the loop filter pole-zero map and the resulting NTF. Finite UGB does not change the location of filter poles. It only adds extra high frequency poles (not shown in the figure). As the above equation suggests, the overall effect of finite UGB is gain error and extra poles [16]. Consequently,

20

the NTF at low frequencies is not affected much, while at high frequencies, it starts to peak as the OTA UGB is reduced.
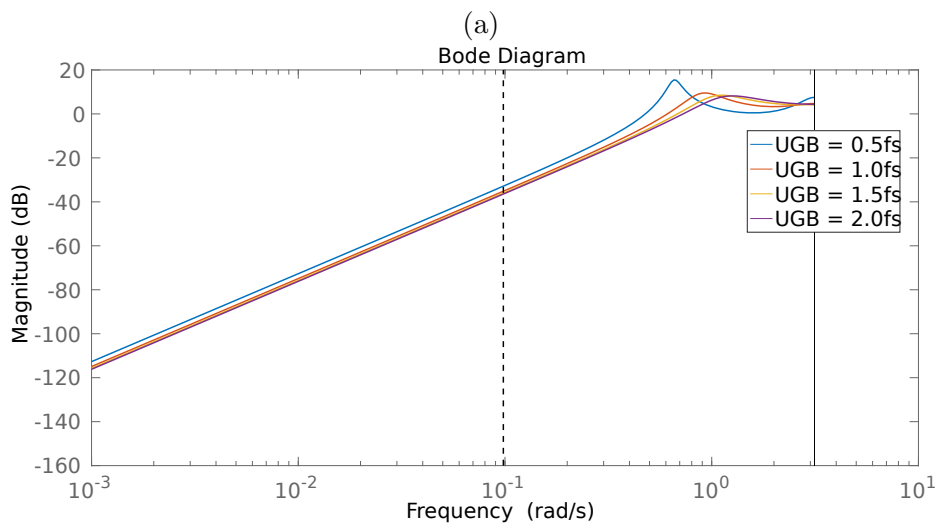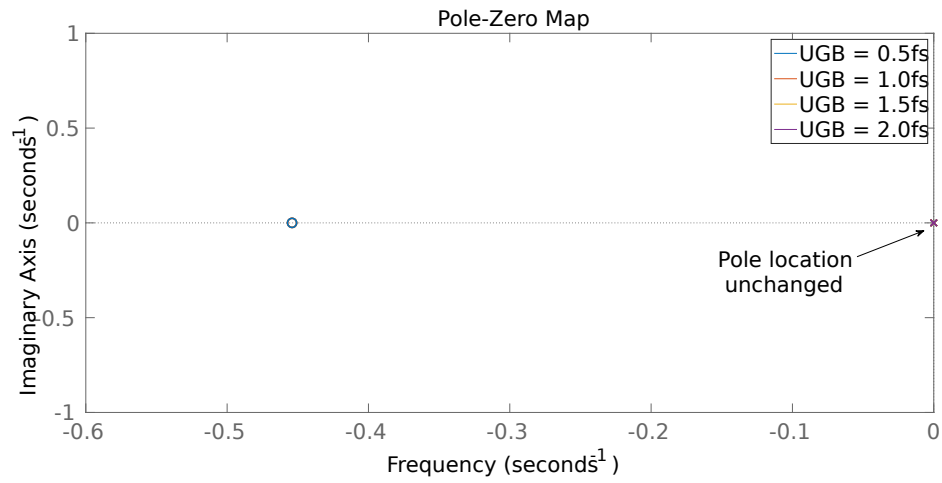

(a)

(b)

Figure 3.5: Conventional modulator- Loop filter pole-zero map and NTF with finite OTA UGB

For the T network SAB filter, the transfer function with OTA finite

UGB model is-

$$H_t(s) = \frac{1 + sR_{2,t}(C_{1,t} + C_{2,t})}{E_t(s)} \tag{3.13}$$

where

$$E_t(s) = \frac{s}{A_0\omega_0}[1 + s\{R_{1,t}C_{1,t} + R_{2,t}(C_{1,t} + C_{2,t}) + A_0\omega_0 R_{1,t}R_{2,t}C_{1,t}C_{2,t}\}$$
$$+ s^2 R_{1,t}R_{2,t}C_{1,t}C_{2,t}]$$

The pole-zero map and the resulting NTF for this case are shown in Fig. 3.6. As a consequence of finite UGB, one of the filter poles is moved to the left half plane. This results in an increase in the low frequency quantization noise since it experiences only first order shaping, as is evident from the NTF. With an increase in OTA UGB, the left half plane pole moves towards the origin as the transfer function becomes closer to the ideal.

For the SC SAB filer, the transfer function with OTA finite UGB is-

$$H_{sc}(s) = \frac{1 + sR_{2,sc}C_{2,sc}}{E_{sc}(s)} \tag{3.14}$$

where

$$E_{sc}(s) = \frac{s}{A_0\omega_0}[1 + A_0\omega_0 R_{1,sc}(C_{1,sc} - C_{2,sc}) + s\{R_{1,sc}(C_{1,sc} + C_{2,sc}) + R_{2,sc}C_{2,sc}$$
$$+ A_0\omega_0 R_{1,sc}R_{2,sc}C_{1,sc}C_{2,sc}\} + s^2 R_{1,sc}R_{2,sc}C_{1,sc}C_{2,sc}]$$

In finite UGB effect as well, the above transfer function is the same as that for a T network SAB (similar to the case of finite gain). One of the filter
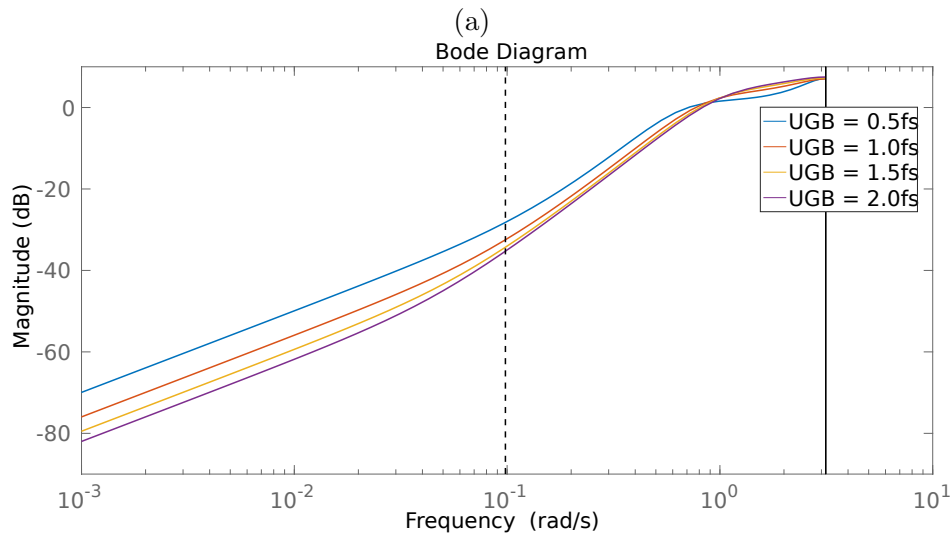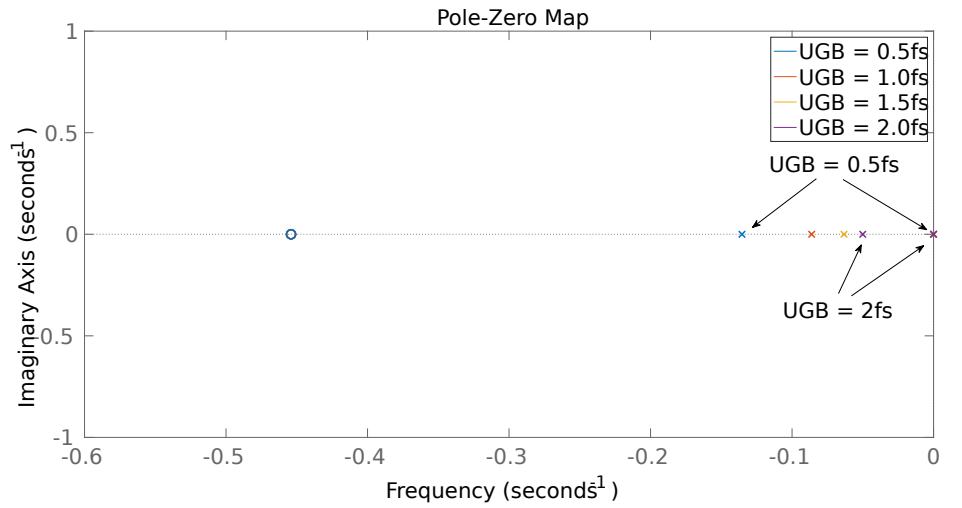
Figure 3.6: T network SAB- Loop filter pole-zero map and NTF with finite OTA UGB

poles is moved to left half plane from DC. But SC SAB uses a positive feedback path (formed with $R_{2,sc}$ and $C_{2,sc}$) in order to achieve the required transfer function. Therefore, it is possible to tune capacitor $C_{2,sc}$ to bring the left half

plane pole closer to DC for a given UGB. If NTF deviation at low frequencies is significantly impacting the SQNR, $C_{2,sc}$ can be made greater than $C_{1,sc}$. This will reduce coefficient of the first order term in the denominator of Equation 3.14, resulting in an improved shaping of low frequency quantization noise.

For this particular case of OSR=32 and second order filter, SNR comparison has been made at an OTA UGB of $1.5f_s$. The output PSD for conventional loop filter and SABs are shown in Fig. 3.7. Since $C_{2,sc}$ was not tuned, SAB output spectrum represents data for both T-network and SC biquads. With some tuning on ELD path gain, the conventional and SAB modulators achieved similar SNR performance of around 78dB for the same amount of thermal noise added to the modulator input.
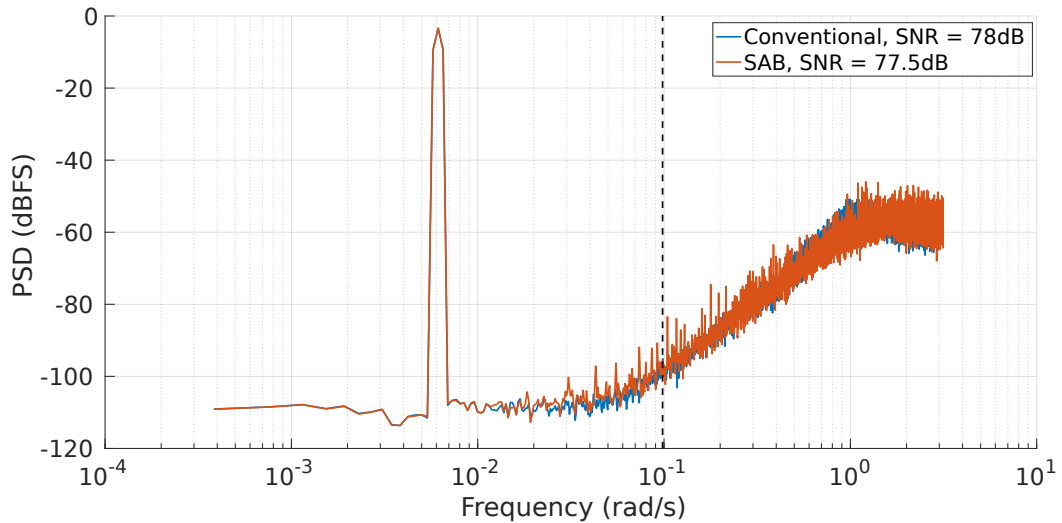

Figure 3.7: SNR comparison with finite OTA UGB ($1.5f_s$)

(a) T network SAB   (b) Self Coupled (SC) SAB
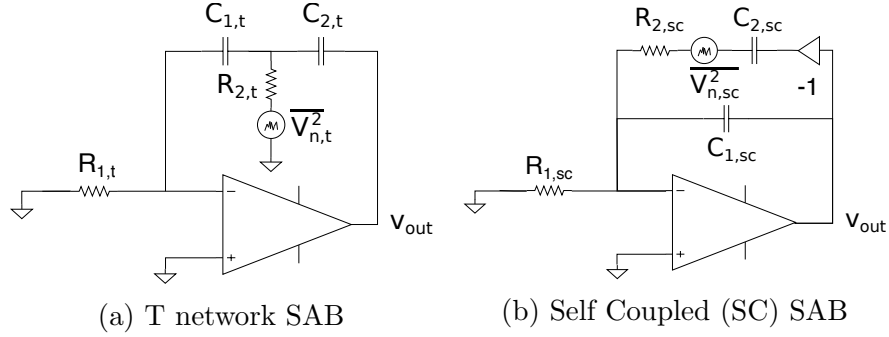
Figure 3.8: SAB thermal noise

3.3 Thermal Noise

When the SABs are being used at the front end, their thermal noise becomes an important consideration as it determines the final SNR of the system. In a conventional loop filter, main contributors to noise are the input resistors (R_1), the DAC and the first OTA. Noise from resistors R_2 and second OTA, when input-referred, is first order shaped and has minimal impact. For the SAB, Fig. 3.8 shows the noise source due to R_2. The input referred transfer function for the noise $\overline{V_{n,t}^2}$ of T network SAB is-

$$V_{n,in}^2(s) = \overline{V_{n,t}^2} \times \left| \frac{sR_{1,t}C_{1,t}}{1 + sR_{2,t}(C_{1,t} + C_{2,t})} \right|^2$$

Similarly, the input referred transfer function for the noise $\overline{V_{n,sc}^2}$ of SC SAB (assuming $C_{1,sc} = C_{2,sc}$) is-

$$V_{n,in}^2(s) = \overline{V_{n,sc}^2} \times \left| \frac{sR_{1,sc}C_{1,sc}}{1 + sR_{2,sc}C_{2,sc}} \right|^2$$

For both the SABs, R_2 noise is first order shaped and its contribution to total noise is thus minimized. Fig. 3.9 shows the SNR plots for the two

SAB filter based modulators. They compare the SNR with and without the R_2 noise, while the R_1 noise is added always. After the R_2 noise is added, it can be observed that the SNR is not affected much.
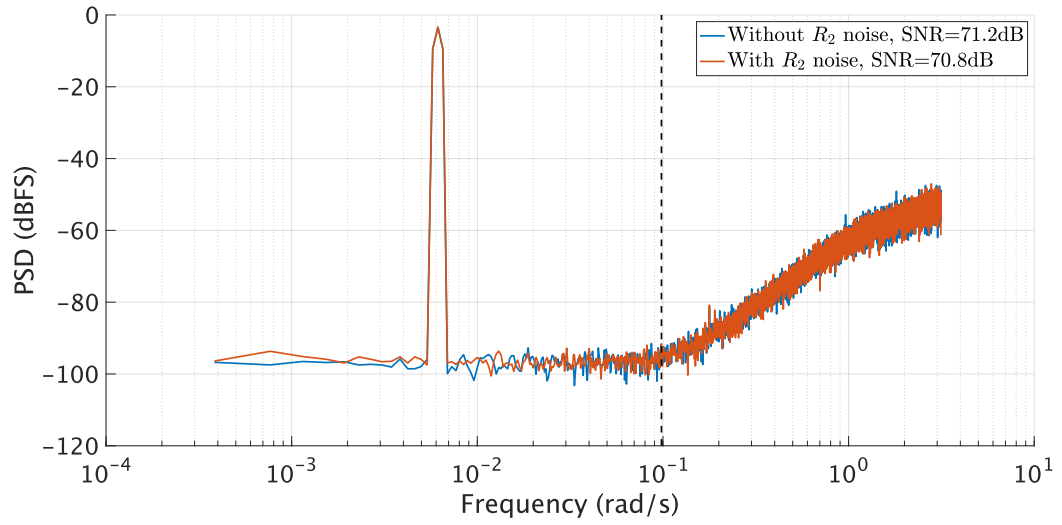
(a) T network SAB
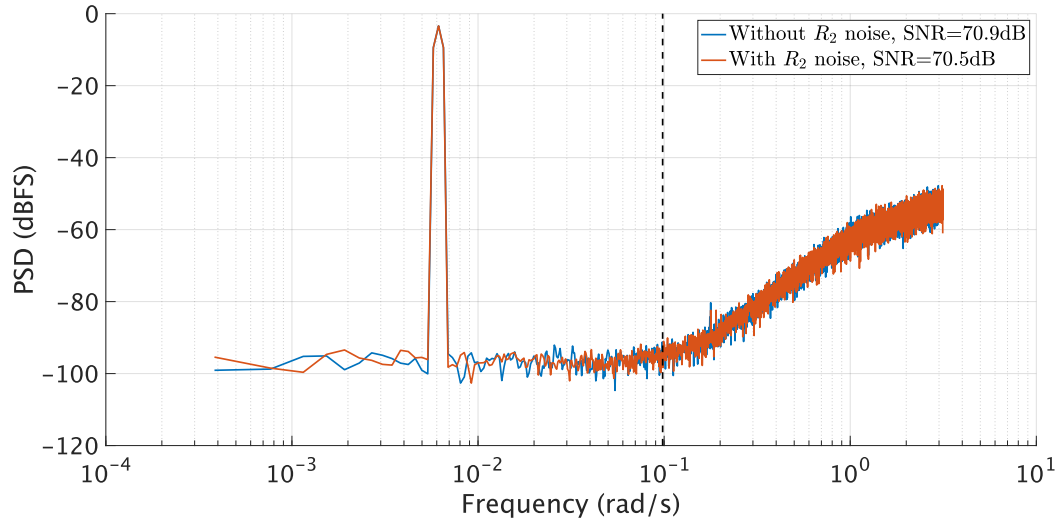
(b) Self Coupled (SC) SAB

Figure 3.9: SAB based modulator SNR with thermal noise

Chapter 4

Fourth Order Filter Implementation Using Extended T Network

By extending the T network filter, possibility of implementing a higher order transfer function was explored. The aim was to further reduce power consumption in the loop filter by cutting down on the number of active components. However, it was observed that a simple extension of T network is not sufficient to realize all possible transfer functions. In [17], filter input was fed-forward to the intermediate nodes of its extended T network for implementation of a third order system. In our case, a fourth order filter was designed using the topology shown in Fig. 4.1b, where the intermediate nodes are fed-forward and added using a summing amplifier. Fig. 4.1a shows the conventional implementation of the same filter.

4.1 Design Complexity

For the purpose of analysis, the fourth order filter was designed for an OSR of 15 with one pair of optimized zeros and a 4-bit quantizer. The ELD compensation path was assumed to be ideal. The normalized transfer function

27
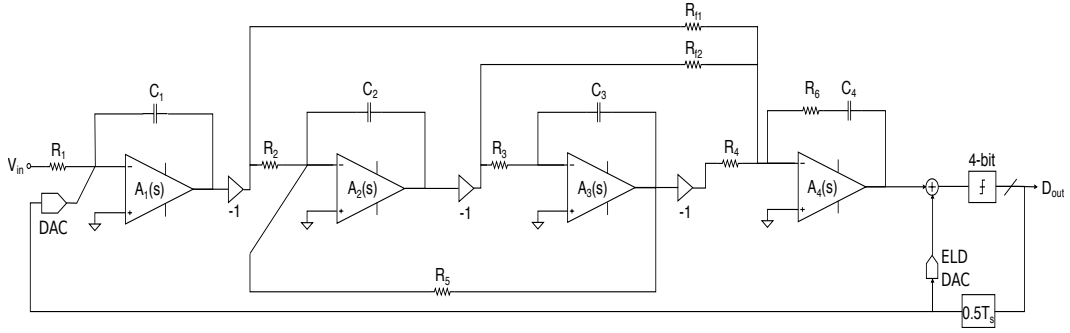
(a) Conventional Filter
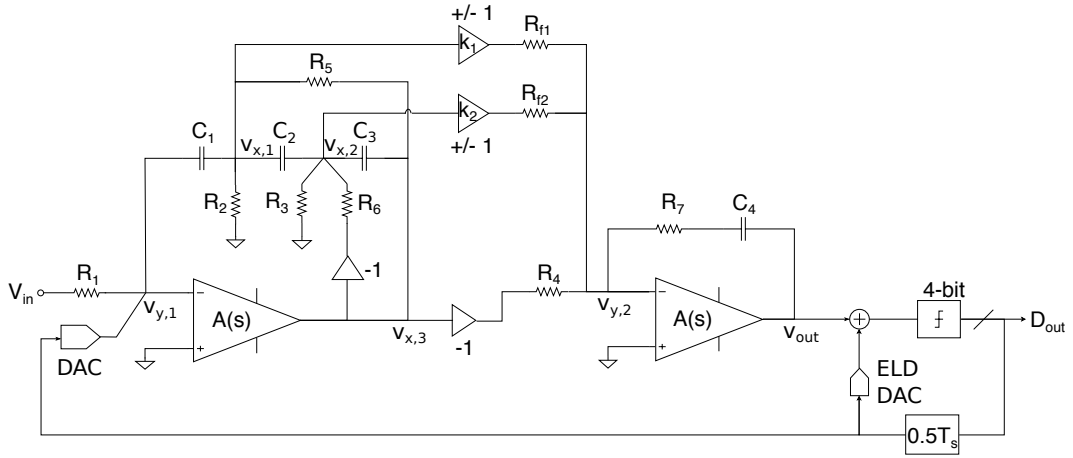
(b) Proposed topology: Extended T network based filter

Figure 4.1: 4th order filter implementations

for the filter (with half cycle ELD) is-

$$H(s) = \frac{0.135 + 0.619s + 1.337s^2 + 1.929s^3}{s^2(s^2 + 0.031)} \qquad (4.1)$$

From Fig. 4.1b, the first OTA is used to generate outputs which are a function of $1/s$, $1/s^2$ and $1/s^3$. The second OTA implements another integrator and also performs weighted summation of the first OTA outputs in order to realize the required transfer function. For zero optimization, the technique

28

presented in [6] was used. The positive feedback path with resistor R_6 is used to cancel the leakage terms in the transfer function. For this purpose, the filter has a matching requirement given by $R_6(C_2 + C_3) = R_5C_2$ (resonant condition). If this condition is satisfied, the transfer function to different intermediate nodes and output of the filter is-

$$\frac{v_{x,3}}{v_{in}} = \frac{R_5}{R_2'}\frac{1 + s[R_2'(C_1 + C_2) + R_3'(C_2 + C_3)] + s^2 R_2'R_3'[C_1C_2 + C_1C_3 + C_2C_3]}{sR_1C_1(1 + s^2 R_3'R_5C_2C_3)}$$

(4.2)

$$\frac{v_{x,2}}{v_{in}} = \frac{N(s)}{s^2 R_1 R_2' C_1 C_2 (1 + s^2 R_3' R_5 C_2 C_3)}$$

(4.3)

$$\frac{v_{x,1}}{v_{in}} = \frac{1}{sR_1C_1}$$

(4.4)

$$v_{out} = \left(v_{x,3} + v_{x,2}k_2\frac{R_4}{R_{f2}} + v_{x,1}k_1\frac{R_4}{R_{f1}}\right)\frac{1 + sR_7C_4}{sR_4C_4}$$

(4.5)

where

$$R_2' = R_2||R_5||R_{f1}$$

$$R_3' = R_3||R_6||R_{f2}$$

$$k_1, k_2 \in \{-1, +1\}$$

$$N(s) = -sR_3'(C_2 + C_3) - s^2[R_2'R_3'(C_1C_2 + C_1C_3 + C_2C_3) - R_3'R_5C_2C_3]$$

$$+ s^3 R_2'R_3'R_5(C_1 + C_2)C_2C_3$$

Unlike the conventional topology, in the case of extended T network filter the design process has more complexity. This is because the intermediate nodes cannot be segregated into $1/s$, $1/s^2$ and $1/s^3$ terms. Moreover, the resistors R_{f1}, R_5 and R_{f2}, R_6 load the nodes $v_{x,1}$ and $v_{x,2}$ respectively. This

increases constraints in the design process as these resistors have to be greater than the effective resistance required at the nodes.

4.2 Power

Power consumption in the OTAs is related to their UGB requirement. Therefore, analysis of finite UGB impact becomes important for estimating power. In order to do the same, comparison has been made to the UGB requirement in the OTAs of the conventional architecture (Fig. 4.1a). First, UGB for OTAs in the conventional architecture were reduced such that SQNR stays above 90dB. The same process was repeated for extended T network based filter. The two topologies could then be compared on the basis of UGB they required to achieve the same SQNR.

For the conventional architecture, the first and last OTA UGB were reduced to $2f_s$, and the second and third OTA UGB to f_s. Since finite UGB effect is similar to adding an extra delay, it can be compensated to some extent by coefficient tuning. Once the filter was designed assuming infinite UGB, coefficient tuning was performed to optimize the NTF. In this particular case, it was achieved by reducing value of capacitors C_1, C_4 and resistor R_{f1}. The ELD path gain was increased to reduce NTF peaking. Furthermore, the location of optimized zeros had changed due to finite OTA UGB. It was adjusted by tuning resistor R_5. Finally, resistor R_{f2} was tuned until the NTF peaking was sufficiently suppressed. With these modifications, the NTF pole-zero map and output PSD are shown in Fig. 4.2.
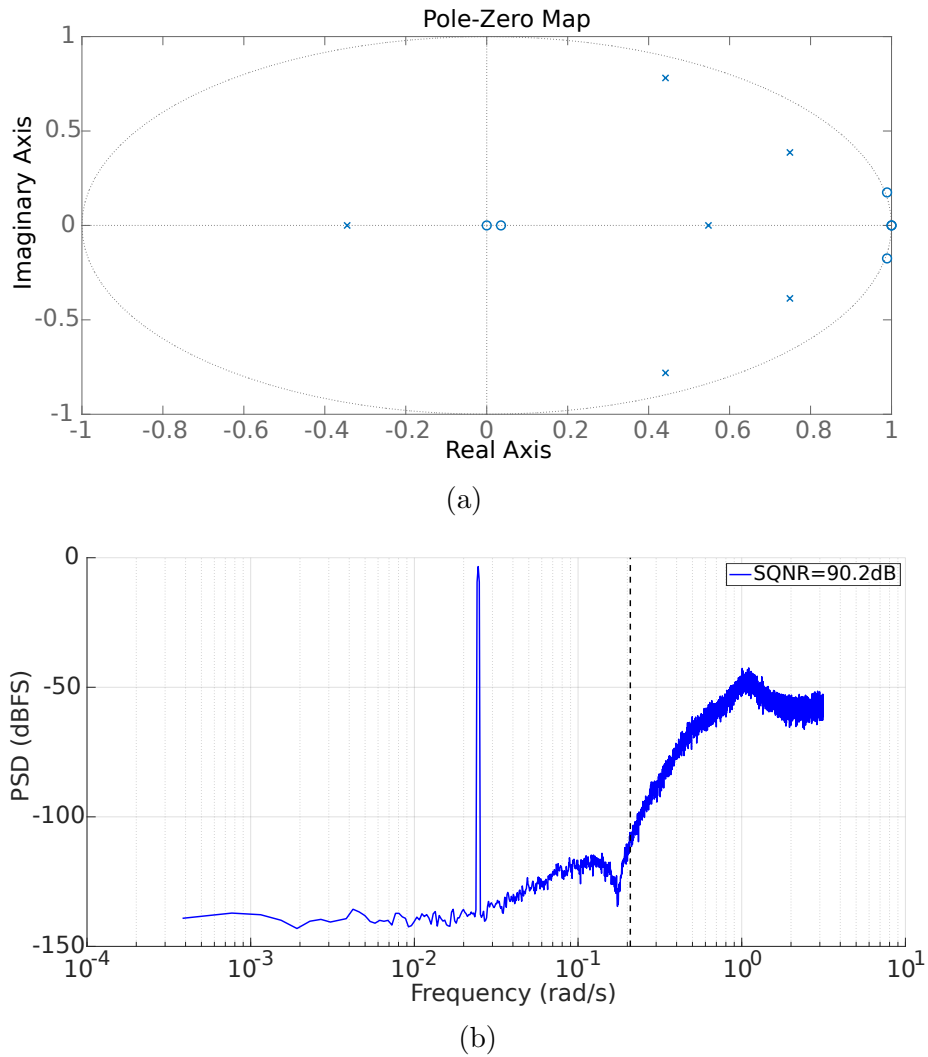
Figure 4.2: Conventional Modulator- NTF pole-zero map and output PSD with finite OTA UGB

In the case of extended T network filter, first the transfer function had to be determined with finite OTA UGB. For simplicity, node $v_{y,2}$ was assumed to be a perfect ground while calculating transfer function from input to the

nodes $v_{x,1}$, $v_{x,2}$ and $v_{x,3}$. The equations are given in appendix 1.

The equations were simulated in MATLAB for behavioral modeling of the filter. For tuning the coefficients, similar procedure was followed as for the conventional modulator. Capacitor C_1 and C_4 were reduced while resistor R_7 and ELD path gain were increased. In this case as well, the location of optimized zero had shifted with finite UGB. To compensate for it, capacitor C_2, C_3 and resistor R_5 were tuned. R_6 was also adjusted for ensuring the NTF notch quality. To have similar SQNR performance as the conventional modulator, the extended T network filter required a minimum of $2.2f_s$ as the UGB for both the OTAs. Therefore, this topology needed higher power to be burnt in the first and last OTA, while it saved the power needed in the second and third OTA. The NTF pole-zero map and output PSD with finite UGB are shown in Fig. 4.3.

4.3   Area

The proposed topology can be compared to the conventional modulator in terms of area by evaluating the capacitor values needed to implement a transfer function. As noise from later stages is shaped, their capacitor values can be scaled down in the conventional modulator. This decrease in capacitor values is accompanied by an increase in resistor values, which helps in saving power as well.

In the extended T network filter, scaling down the capacitor values was not feasible. Since the transfer function to the nodes $v_{x,1}$, $v_{x,2}$ and $v_{x,3}$ is

(a)

(b)
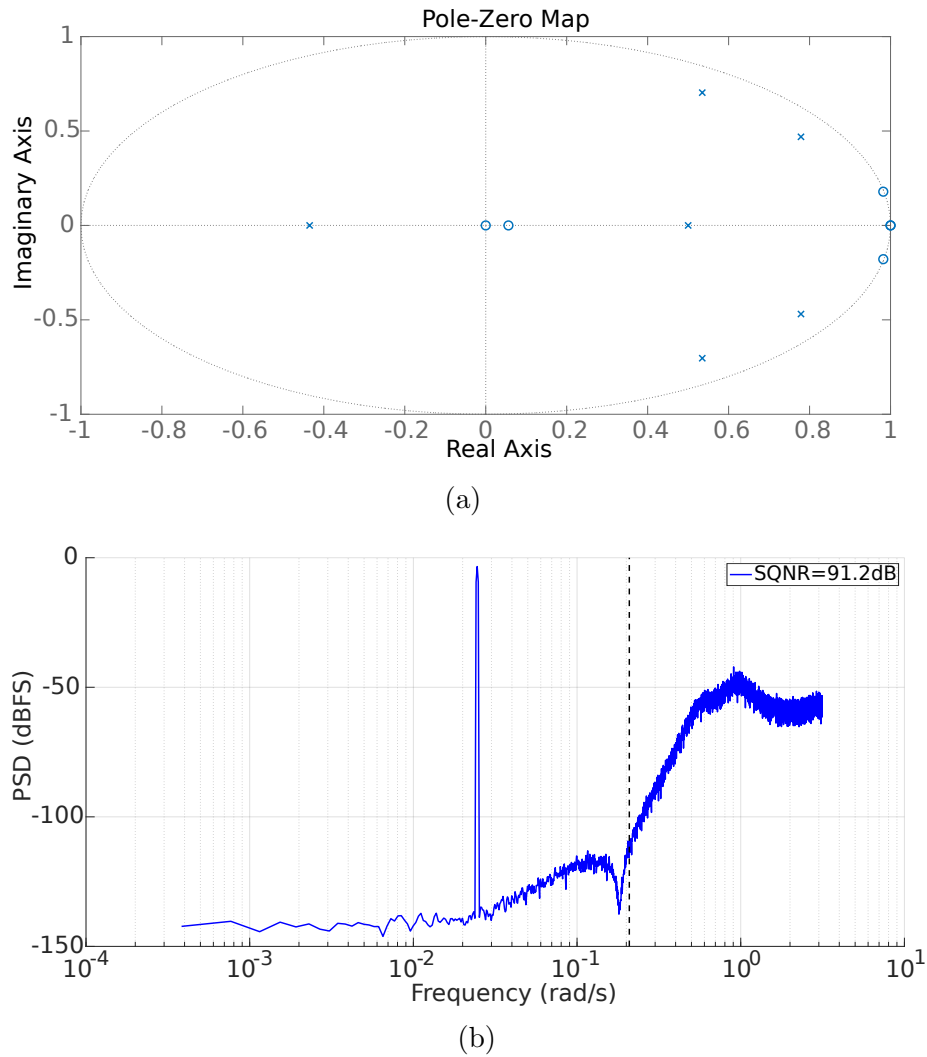
Figure 4.3: Extended T network Architecture- NTF pole-zero map and output PSD with finite OTA UGB $(2.2f_s)$

tightly coupled, it becomes difficult to individually control the resistance or capacitor values without affecting the overall transfer function. As a result, for realization of the transfer function given by Equation 4.1, capacitors C_2

and C_3 were greater than capacitor C_1. Furthermore, R_3' (effective resistance at node $v_{x,3}$) was less than R_2'. Since total capacitor size is a dominant factor which determines the chip area, the conventional modulator can be designed to occupy a smaller chip area than the extended T network filter.

Chapter 5

Conclusions and Future Work

In the first half of the report, two of the existing SABs were compared against the conventional filter for finite gain, UGB impact and thermal noise. Analysis showed that the use of SAB based filters did not burden the OTA and hence, could achieve similar performance as the conventional filter. The thermal noise of SAB filters was dominated only by the input resistor noise and the noise from the other resistor was first order shaped.

In the latter half of the report, an extension of T network biquad was proposed for implementing a fourth order filter. Upon comparing it with the conventional implementation, it was concluded that finite UGB had a higher impact on the proposed topology. This implied that even though the topology eliminated usage of two OTAs, higher power was needed in the ones being used for the implementation. Moreover, the proposed topology had a more complex design process and required more chip area.

For future work, the proposed topology can be improved on aspects like power consumption and area. For simplicity, ELD path was considered to be ideal in the analysis. Once this path is included in the filter, the power consumption in the second OTA might increase due to the settling requirement

of this path. All of this has to be accounted for in the final power dissipation of the filter. The design then has to be implemented at a transistor level for validation of the results obtained through behavioral simulations.

Appendix

Appendix 1

Extended T Network Filter with Finite UGB

For Fig. 4.1b, the transfer function has been derived below with finite OTA UGB and a front end R-DAC. It assumes for simplicity that the node $v_{y,2}$ is a perfect ground when calculating the transfer function to nodes $v_{x,1}$, $v_{x,2}$ and $v_{x,3}$.

$$v_{x,3} = v_{in}\frac{1 + s[R_2'(C_1 + C_2) + R_3'(C_2 + C_3)] + s^2 R_2' R_3'[C_1 C_2 + C_1 C_3 + C_2 C_3]}{2D(s)}$$

$$(1.1)$$

$$v_{x,1} = v_{in}\frac{1}{sR_1 C_1} - \frac{v_{x,3}}{A(s)}\frac{1 + sR_1' C_1}{sR_1' C_1}$$

$$(1.2)$$

$$v_{x,2} = v_{x,1}\frac{1 + sR_2'(C_1 + C_2)}{sR_2' C_2} - v_{x,3}\frac{1}{sR_5 C_2} + \frac{v_{x,3}}{A(s)}\frac{C_1}{C_2}$$

$$(1.3)$$

$$v_{out} = \left(v_{x,3} + v_{x,2}k_2\frac{R_4}{R_{f2}} + v_{x,1}k_1\frac{R_4}{R_{f1}}\right)\frac{\frac{R_4'}{R_4}(1 + sR_7 C_4)}{\frac{s}{A_0\omega_0}\left(1 + A_0\omega_0 R_4' C_4 + s(R_4' + R_7)C_4\right)}$$

$$(1.4)$$

where

$$A(s) = \frac{A_0\omega_0}{s}$$

$$R1' = R1/2$$

$$R_2' = R_2||R_5||R_{f1}$$

$$R_3' = R_3||R_6||R_{f2}$$

$$R'_4 = R_4||R_{f1}||R_{f2}$$

$$k_1, k_2 \in \{-1, +1\}$$

$$D(s) = \frac{s}{A_0\omega_0}\left(1 + A_0\omega_0 R'_1 C_1 \frac{R'_2}{R_5} + s\left[R'_3\left\{C_2 + C_3 - C_2\frac{R_5}{R_6}\right\}A_0\omega_0 R'_1 C_1 \frac{R'_2}{R_5}\right.\right.$$

$$\left.+ R'_1 C_1 + R'_2(C_1 + C_2) + R'_3(C_2 + C_3)\right] + s^2\left[A_0\omega_0 R'_1 R'_2 R'_3 C_1 C_2 C_3\right.$$

$$\left.+ R'_1 R'_2 C_1 C_2 + R'_1 R'_3 C_1(C_2 + C_3) + R'_2 R'_3(C_1 C_2 + C_1 C_3 + C_2 C_3)\right]$$

$$\left.+ s^3 R'_1 R'_2 R'_3 C_1 C_2 C_3\right)$$

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Vita

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