# An Adaptive Multi-Step Balancing Modulation Technique for Multi-Point Clamped Converters

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***Abstract*— In this paper, a new pulse-width modulation technique is proposed for the output voltage control and the DC-bus capacitors voltage balancing of a Multi-Point Clamped multilevel converter. The voltage equalization is achieved by allowing each converter's leg voltage to switch though multiple levels in a single modulation period (multi-step operation). The approach is generalized with respect to the number of levels and phases and can be applied regardless of the converter operating conditions. Nevertheless, the multi-step behaviour generally leads to an increase of the average switching transitions rate. In the proposed method, this drawback is mitigated with an online adaptive selection of the number of switching levels. The algorithm is validated through an extensive hardware-in-the-loop testing and compared to other approaches.**

***Keywords — Multi-Point Clamped Converters, Multilevel Converters, Voltage Balancing, Pulse Width Modulation.***

NOMENCLATURE

| | |
|---|---|
| $v$, $i$ | leg output voltage, current |
| $T_S$, $f_S$ | modulation period, frequency |
| $N$ | total number of converter voltage levels |
| $s_h$, $d_h$ | $h$-th device switching signal, duty-cycle |
| $i_{dc,h}$ | $h$-th DC-bus node current |
| $V_{dc}$ | total DC-bus voltage |
| $v_{dc,h}$ | $h$-th DC-bus capacitor's voltage |
| $\Delta v_{dc,h}$ | $h$-th DC-bus capacitor's voltage disbalance |
| $\delta_h$ | $h$-th DC-bus node duty-ratio |
| $\alpha_h$ | $h$-th DC-bus node balancing gain factor |
| $\sigma$ | balancing strength factor |
| $V_{\Sigma T}$, $V_{\Sigma B}$ | top, bottom equivalent balancing voltage |
| $M$ | restricted number of switching levels |
| $N_{Top}$, $N_{Bot}$ | maximum, minimum feasible switching level |
| $\Delta v_{dc,Top}$, $\Delta v_{dc,Bot}$ | top, bottom external DC-bus voltage disbalance |
| $C$ | DC-bus capacitances |
| $e$ | AC grid voltage |
| $f_{AC}$, $\omega$ | AC grid frequency, angular frequency |

## I. INTRODUCTION

At the present days, despite the great improvements in the semiconductor technology, the fully controllable power electronic devices show undesired limitations in terms of both the voltage and current they can sustain. As a result, the design of a power converter for high power applications is often carried out by connecting several devices in series and/or in parallel.

Multilevel converters allow, with relatively small changes in the hardware architecture, to enhance the series connection of multiple devices. Indeed, not only they allow to sustain higher voltages, but they also show additional benefits with respect to equivalent two-level converters. As an example, by increasing the number of voltage levels at the AC terminals, they can reduce the output voltage harmonic content and the average switching frequency, thus requiring smaller filtering devices and improving the overall efficiency [1-7].

The *Multi-Point Clamped* (MPC), first introduced in [8] for its three-levels structure (named *Neutral Point Clamped* or NPC), is one of the most widespread multilevel architectures for industry, traction and grid-tied applications [9-11]. Different hardware topologies can be addressed as MPC (e.g. Diode Clamped, T-Type, etc., see Fig. 1). They differ in some design aspects (like the number, or the voltage rating, of the semiconductor devices), but behave equivalently from the functional point of view. Generally speaking, an $N$-level MPC converter is built upon the series connection of $(N-1)$ DC capacitors and each phase leg output terminal can be linked to a desired capacitor terminal through a proper choice of the controllable devices' switching signals.

In standard applications, all the capacitors should always be equally charged; nevertheless, the DC nodes currents injected by the converter legs during their normal functioning alter their voltage and may lead to a severe drift from their rated value. This phenomenon, which has been deeply studied for NPC converters [12-13], is progressively intensifying for higher number of levels

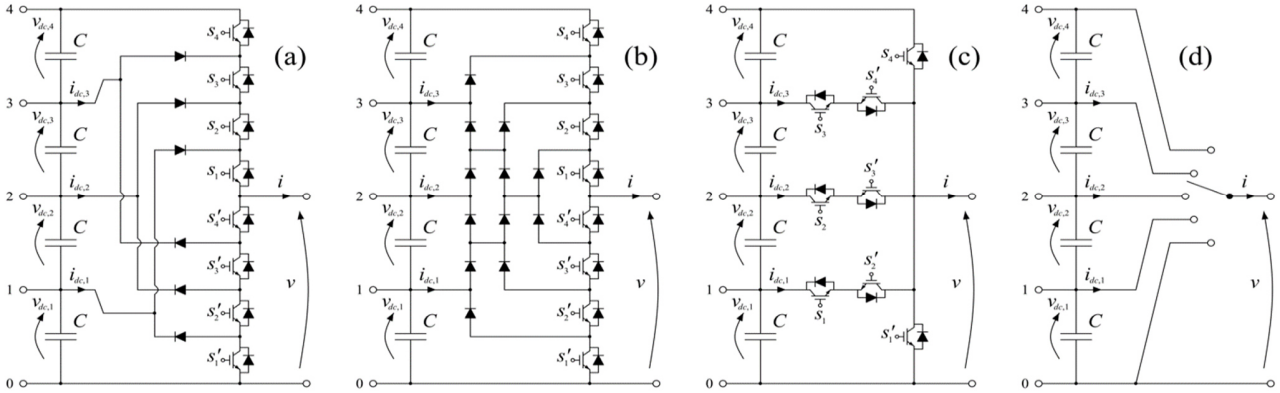


Fig. 1. Some common Multi-Point Clamped Converter leg architectures (5 levels):
a) Standard Diode Clamped; b) Pyramidal Diode Clamped; c) T-type; d) Ideal topology.

[14-15] and needs to be neutralized to guarantee a correct behaviour.

In many applications the voltage equalization is performed through additional hardware balancing circuits [16-22]. These circuits allow to stabilize the DC voltages independently from the main converter operating conditions and to exploit some standard Pulse-Width-Modulation (PWM) techniques to control the main structure [23-25], but add more complexity and generally lead to an increase of the overall losses. An alternative approach is instead based on a proper modification of the modulation technique in order to exploit some degrees of freedom of the structure to control the DC-bus capacitors' voltages without any need for auxiliary devices.

Usually the switching signals for the controllable devices of a converter leg are obtained through the comparison between a reference signal and several triangular carriers [9-10]. This single-reference/multiple-carriers technique constraints in each modulation period the output voltage to switch only among the two feasible levels closest to the desired reference, thus exhibiting a *Single-Step* switching mode. In this case the only degree of freedom for the DC-bus capacitors voltage equalization is the output common mode voltage which, in absence of a neutral connection, does not affect the output currents. However, as shown in [15], there is a theoretical limit regarding the effectiveness of this injection, which depends on the modulation index and on the power factor. In particular, for high modulation index values and power factors, the DC-bus capacitors voltage drift cannot be neutralized [15]. As a result, these techniques are often employed for systems with a small overall power absorption from the DC-bus, like for back-to-back configurations where the disbalance tendencies of the rectifier and inverter units have a potential to compensate each other [26-29].

To overcome this drawback, other approaches [30-35] employ a multiple-references/single-carrier comparison, which guarantees the independent control of each switching device and allows the output voltage to switch between many feasible levels in the same modulation period, thus exhibiting a *Multi-Step* behaviour. The main drawback here is represented by the increase of the switching losses and by a general worsening of the output voltage harmonic content, due to the presence of multiple switching transitions in each modulation interval.

This effect can be partially neutralized by adapting in real time the number of feasible switching levels to the converter's working conditions. This paper presents an improvement of the multi-step technique proposed by the authors in [35], where the adaptive choice of the switching levels was based on a feedback control loop acting on the worst DC-bus voltage disbalance. On the contrary, the adaptive technique described in the following is based on the real-time choice of the number of feasible switching levels in each modulation interval. This technique, performed independently for each converter leg, is aimed to achieve a desired trade-off between the equalization effectiveness and the reduction of the average switching transitions rate.

The proposed approach, described in Section II, has been particularized in Section III with respect to an MPC converter employed as an active High-Voltage-Direct-Current (HVDC) rectifier. The results, obtained through several Hardware-In-the-Loop (HIL) simulations, have shown how the proposed technique is able to sensibly reduce the switching transitions rate with respect both to the strategy proposed in [35] and to a baseline multi-step based approach discussed in [34], while at the same time supplying the desired average output voltages and keeping all the DC-bus capacitors voltages within a desired threshold. The conclusions of the work are drawn in Section IV.

## II. Proposed Multi-Step PWM Technique

### A. Mathematical Model of an MPC converter leg

As well known, a generic $N$-levels MPC leg, regardless of its topology (some of the most common architectures are depicted in Fig. 1 for a five-level converter), is built upon $2\cdot(N-1)$ controllable devices, and $(N-1)$ DC-bus capacitors. The multilevel behaviour of the output leg voltage $v$ is achieved by connecting the output node to any of the DC-bus nodes through a proper control of the switching devices.

The safe operation of the system imposes to drive some device couples (which depend on the chosen hardware topology), in a complementary fashion. Therefore, the system can be analysed with respect to a subset of $(N-1)$ switching signals $s_h \in \{0; 1\}$ (the complementary devices are always driven by $s_h' = 1 - s_h$). Consequently, from the functional point of view, the converter behaves as an ideal switching circuit schematically represented in Fig. 1d.

Furthermore, for any hardware configuration, the output leg voltage $v$ is fully decoupled from the corresponding phase current once the switching signals satisfy the condition $s_h \geq s_{h+1}$; in other words, the $(h+1)$-th device cannot be turned on unless the $h$-th one is already in conduction state. This condition restricts the number of feasible switching signals combinations from $2^{N-1}$ to just $N$. Once these constraints are satisfied and the power devices are assumed as ideal switches, the leg output voltage $v$ can be expressed as a linear combination of the DC-bus capacitors voltages $v_{dc,h}$:

$$v = \sum_{h=1}^{N-1} s_h \cdot v_{dc,h} \tag{1}$$

where, coherently with the notation adopted in Fig. 1, the index $h \in \{1, \ldots, N-1\}$ increases by counting from the negative to the positive DC-bus rail. The switching signals also allow for the computation of the DC-bus nodes currents, expressed as:

$$i_{dc,h} = (s_h - s_{h+1}) \cdot i = \Delta s_h \cdot i \tag{2}$$

Since the differential switching signals $\Delta s_h = s_h - s_{h+1}$ introduced in (2) have to be positive (given the condition $s_h \geq s_{h+1}$), each $i_{dc,h}$ sign is constrained to be equal to the sign of the output leg current $i$ (the reference directions of $i_{dc,h}$ and $i$ are referred accordingly to Fig. 1).

For simplicity, further on it is assumed that the MPC DC-bus consists of $(N-1)$ identical capacitors with capacitance $C$. Each $h$-th DC-bus node links the $h$-th and $(h+1)$-th capacitors; their voltage disbalance is denoted with $\Delta v_{dc,h}$ and is defined as:

$$\Delta v_{dc,h} = v_{dc,h} - v_{dc,h+1} \tag{3}$$

By applying Kirchhoff's current law to each DC-bus node ($h = 1, \ldots, N-2$), the dynamical model of the consecutive DC-bus voltage disbalances is obtained:

$$C \frac{\mathrm{d}}{\mathrm{d}t}\left[\Delta v_{dc,h}\right] = -i_{dc,h} = -(s_h - s_{h+1}) \cdot i = -\Delta s_h \cdot i \tag{4}$$

The main purpose of the proposed strategy is to guarantee the DC-bus capacitors voltage equalization, while at the same time supplying (on average) a desired output voltage $v^*$ with each converter leg. The equalization requirement obviously results in the condition $\Delta v_{dc,h} \rightarrow 0$ for each $h$-th DC-bus node.

If the switching signals $s_h$ are obtained by means of a carrier-based PWM technique, for which the switching instants are determined by comparing the leg duty-cycles $d_h \in [0; 1]$ to a common triangular-wave carrier signal varying in [0; 1] at the

modulation frequency $f_S$ (multiple-references/single-carrier), it is easy to verify that all the switching signal constraints are automatically satisfied once:

$$0 \le d_{N-1} \le \dots \le d_{h+1} \le d_h \le \dots \le d_1 \le 1 \qquad (5)$$

In particular, the condition $d_h \ge d_{h+1} \Rightarrow s_h \ge s_{h+1}$ is graphically exemplified in Fig. 2.

The difference between the duty-cycles of two adjacent devices is denoted as $\delta_h$ and defined as:

$$\delta_h = \Delta d_h = d_h - d_{h+1} \qquad (6)$$

This value (which, as per (5), is always non-negative) represents the average time for which the MPC leg output node is connected to the $h$-th DC-bus node in each modulation interval; therefore, it will be further on referred as $h$-th DC-bus node duty-ratio.

By using a standard averaging approach with a moving time window of length $T_S = 1/f_S$ and by neglecting the interactions of the high frequency contributions to the state variables, the averaged mathematical model of the converter can be derived. Equations (1) and (4) in the averaged model become:

$$\begin{cases} v = \sum_{h=1}^{N-1} d_h \cdot v_{dc,h} \\ C\frac{\mathrm{d}}{\mathrm{d}t}[\Delta v_{dc,h}] = -i_{dc,h} = -(d_h - d_{h+1}) \cdot i = -\delta_h \cdot i \quad (h = 1,\dots,N-2) \end{cases} \qquad (7)$$

Hence, the switching variables have been replaced with their average values over a modulation period. This modelling approach allows to refer the modulation procedure to the duty-cycles $d_h$ (which have a continuous nature) instead of the switching signals $s_h$ (which have a discrete nature).

### B. N-Levels Multi-Step Technique

From the control point of view, the first equation of (7) establishes an equality constraint for the unknown variables by forcing a desired output voltage $v = v^*$ which, naturally, must respect the condition $0 \le v^* \le V_{dc} = \sum_{h=1}^{N-1} v_{dc,h}$.

Standard single-step modulation techniques only allow a single $H$-th duty-cycle to be in the open interval $0 < d_H < 1$, while forcing all the other duty-cycles $d_h$ with $h < H$ to 1 and the ones with $h > H$ to 0. This choice results in a single equation with only one degree of freedom and, consequently, does not allow the active control of the DC-bus capacitors voltages once the reference voltage $v^*$ is set by other means.

Contrarily, by inspection of (7), it can be deduced that there are $(N-1)$ degrees of freedom (all the devices' duty-cycles), which can be exploited for the simultaneous control of the leg output voltage and of the $(N-2)$ DC-bus voltage disbalances. Therefore, at least theoretically, each voltage disbalance $\Delta v_{dc,h}$ could be forced to zero by a proper feedback control loop, whose output would be a reference DC-bus current to be injected by changing $\delta_h$ (see the second equation in (7)). However, the duty-cycles are subject to the constraints (5) meaning that the DC-bus currents $i_{dc,h} = \delta_h \cdot i$ cannot be imposed arbitrarily. Consequently, a proper criterion needs to be formulated in order to choose the best set of node currents in the context of the DC-bus voltage equalization process.

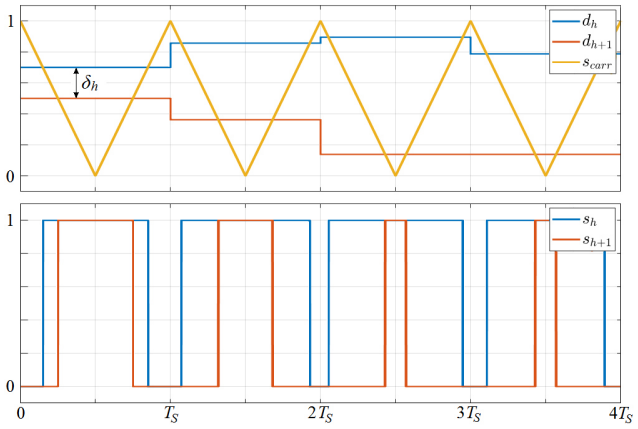


Fig. 2. Explicative behaviour of two consecutive duty-cycles and the resulting switching functions for a triangular carrier-based PWM.

Since the control is aimed to nullify each voltage disbalance, according to (7) a positive $\Delta v_{dc,h}$ would require a positive $i_{dc,h}$, while a negative $\Delta v_{dc,h}$ would require a negative $i_{dc,h}$. Therefore a balancing action can be performed only on the couples of adjacent capacitors for which $\Delta v_{dc,h} \cdot i_{dc,h} > 0$; since $i_{dc,h} = \delta_h \cdot i$, and $\delta_h \ge 0$, the condition can be rewritten as $\Delta v_{dc,h} \cdot i > 0$. When this product is negative, the only way to avoid a disbalancing effect is to set the corresponding $h$-th DC-bus node duty-ratio $\delta_h$ to zero. In the context of the proposed technique, if at least one converter node satisfies the condition $\Delta v_{dc,h} \cdot i > 0$, the equalization can be performed by choosing the duty-ratios of each $h$-th DC-bus node ($h = 1, \dots, N-2$) as:

$$\delta_h = \begin{cases} \alpha_h \cdot \sigma & \text{if } \Delta v_{dc,h} \cdot i > 0 \\ 0 & \text{if } \Delta v_{dc,h} \cdot i \le 0 \end{cases} \qquad (8)$$

where $\alpha_h$, named *Balancing Gain Factors* are per-node defined normalization coefficients satisfying the condition $\sum_{h=1}^{N-2} \alpha_h = 1$, while $\sigma$, named *Balancing Strength Factor* is a common gain which weights the overall balancing action strength and satisfies the condition $0 \le \sigma \le 1$ [20]. With this choice, the controller distributes the output current $i$ among all the $N$ DC-bus nodes. The strength factor $\sigma$ identifies the time for which the output node is connected to the $(N-2)$ internal nodes, while each gain factor $\alpha_h$ identifies the percentage of this time associated to the $h$-th node. As an example, a value of the strength factor $\sigma = 0.8$ means that the considered MPC leg output node is connected to the internal DC-bus nodes for 80% of the modulation period (and to either the positive or the negative DC rail for the remaining 20%). Then, if the $h$-th gain factor is $\alpha_h = 0.3$, the $h$-th DC-bus node is responsible for 30% of this time, meaning that its corresponding duty-ratio is $\delta_h = 0.3 \cdot 0.8 = 0.24$ (24% of the entire modulation period).

As in [35], the proposed approach imposes each $\alpha_h$ to be proportional to the corresponding disbalance $\Delta v_{dc,h}$. By denoting with the subscript $r$ the indexes of the voltage disbalances which can be equalized (i.e. $\Delta v_{dc,r} \cdot i > 0 \ \forall r$), it results that:

$$\alpha_r = \Delta v_{dc,r} \Big/ \left( \sum_{r'} \Delta v_{dc,r'} \right) \qquad (9)$$

Obviously, other strategies can be adopted instead of (9); they would still guarantee a stable equalization as long as the most disbalanced voltages are associated to the highest gain factors.

Once a criterion for the choice of the gain factors $\alpha_h$ is formulated (e.g. the proportionality strategy (9)), the equalization problem is reduced to a single degree of freedom optimization process, involving only the determination of the value of the strength factor $\sigma$ which maximizes the balancing action while supplying $v^*$ and satisfying the constraints imposed by (5).

By substituting (6) and (8) in the first equation of (7) and by grouping with respect to $\sigma$ and $d_1$ it results that:

$$v^* = d_1 \cdot V_{dc} - \sigma \cdot \left[ \sum_{h=1}^{N-2} \left( \alpha_h \cdot \sum_{k=h+1}^{N-1} v_{dc,k} \right) \right] = d_1 \cdot V_{dc} - \sigma \cdot V_{\Sigma T} \quad (10)$$

where $V_{\Sigma T}$ is named *Top Equivalent Balancing Voltage* [35]. Similarly, by grouping with respect to $\sigma$ and $d_{N-1}$, one gets:

$$v^* = d_{N-1} \cdot V_{dc} + \sigma \cdot \left[ \sum_{h=1}^{N-2} \left( \alpha_h \cdot \sum_{k=1}^{h} v_{dc,k} \right) \right] = d_1 \cdot V_{dc} + \sigma \cdot V_{\Sigma B} \quad (11)$$

where $V_{\Sigma B}$ is named *Bottom Equivalent Balancing Voltage* [35]. The condition $d_1 \leq 1$ applied to (10) imposes the constraint $\sigma \leq (V_{dc} - v^*)/V_{\Sigma T}$ while the condition $d_{N-1} \geq 0$ applied to (11) imposes the constraint $\sigma \leq v^*/V_{\Sigma B}$. Therefore, the optimal feasible value of the balancing strength factor (which leads to the fastest convergence rate) is given by the most stringent constraint condition between $d_1 = 1$ and $d_{N-1} = 0$, resulting into:

$$\sigma = \min \{ \; v^*/V_{\Sigma B} \; ; \; (V_{dc} - v^*)/V_{\Sigma T} \; \} \quad (12)$$

By noting that $V_{\Sigma T} + V_{\Sigma B} = V_{dc}$, this process can be recognized as an optimal multi-step voltage balancing of an equivalent three-levels NPC whose top and bottom DC voltages are $V_{\Sigma T}$ and $V_{\Sigma B}$ and whose neutral point duty-ratio is $\sigma$.

Once $\sigma$ has been chosen through (12), either $d_1$ or $d_{N-1}$ has been set and all the other devices' duty-cycles $d_h$ are easily obtained by back-substitution with the DC-bus duty-ratios $\delta_h$. In particular, if $v^*/V_{\Sigma B} < (V_{dc} - v^*)/V_{\Sigma T}$, the solution is given by:

$$d_{N-1} = 0, \; d_{N-2} = d_{N-1} + \sigma \cdot \alpha_{N-2}, \; \ldots, \; d_1 = d_2 + \sigma \cdot \alpha_1 \quad (13)$$

while, in the opposite situation, the solution is given by:

$$d_1 = 1, \; d_2 = d_1 - \sigma \cdot \alpha_1, \; \ldots, \; d_{N-1} = d_{N-2} - \sigma \cdot \alpha_{N-2} \quad (14)$$

### C. Adaptive Multi-Step Algorithm

The equalization procedure described in the previous paragraph is achieved through a multi-step switching behaviour and is the core of the algorithm developed by the authors in [35]. Although its effectiveness is guaranteed regardless of the MPC operating condition, since multiple devices per leg are allowed to switch in each modulation interval, the resulting transition rate might be very high and invalidate both the overall efficiency and the output voltage harmonic content.

To neutralize this drawback, the technique can be applied only to a subset $M \in \{2, \ldots, N\}$ of the converter levels, properly selected to reduce the transitions rate. In particular, in each modulation interval, $(M - 1)$ adjacent devices' duty-cycles can be chosen to be in the range (0; 1), while the remaining $(N - M)$ are either set to 0 or to 1. When $M = 2$, the modulation behaves as a standard single-step technique (i.e. without any balancing capability), while the condition $M = N$ corresponds to the fully deployed balancing action, which sets all the DC-bus node duty-ratios as per (8). This situation is equivalent to consider (in each switching period) an equivalent $M$-levels MPC whose positive and negative rails are connected to the overall DC-bus through the series connection of some external DC capacitors. With reference to Fig. 3, by denoting with $v_{dc,Bot}$ and $v_{dc,Top}$ the total voltage of the external bottom and top capacitors, and as $N_{Bot}$ and $N_{Top}$ the minimum and maximum feasible level (with $N_{Top} - N_{Bot} = M - 1$), it is possible to apply the relations (8)-(14) once the following substitutions are set:

$$\begin{array}{ll} N \rightarrow M \; ; & h \rightarrow h + N_{Bot} \; ; \\ v^* \rightarrow v^* - v_{dc,Bot} \; ; & r \rightarrow r + N_{Bot} \; ; \end{array} \quad (15)$$

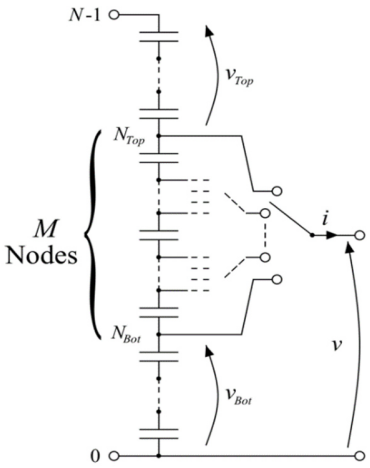

Fig. 3. Equivalent circuit of the MPC in $M$-levels operating mode.

The algorithm developed in this paper is based on the choice of the feasible switching levels in a way to explicitly consider the potential effects of the multi-step operation towards the external capacitors. Indeed, the previously described balancing technique, once applied to the partial $M$-levels subset, drives the available DC currents in a way to nullify the voltage disbalances of the internal capacitors, but does not apply any active control to the external ones (i.e. the capacitors above $N_{Top}$, and below $N_{Bot}$, Fig. 3). In other words, the currents absorbed from the DC-bus nodes corresponding to the top or the bottom feasible level are not chosen by the controller. While this phenomenon does not have any effect when these currents are absorbed by the positive or negative DC rail (which in the adopted formalism would correspond to $i_{dc,0}$ and $i_{dc,N-1}$), it might lead to an disbalancing behaviour when $M < N$.

By introducing the external voltage disbalances as:

$$\Delta v_{dc,Bot} = \begin{cases} v_{dc,N_{Bot}} - v_{dc,N_{Bot}+1} & \text{if} \quad N_{Bot} > 0 \\ 0 & \text{if} \quad N_{Bot} = 0 \end{cases} \quad (16)$$

$$\Delta v_{dc,Top} = \begin{cases} v_{dc,N_{Top}} - v_{dc,N_{Top}+1} & \text{if} \quad N_{Top} < N-1 \\ 0 & \text{if} \quad N_{Top} = N-1 \end{cases} \quad (17)$$

it is clear that the output current has an overall equalizing effect only if it simultaneously results $\Delta v_{dc,Bot} \cdot i \geq 0$ and $\Delta v_{dc,Top} \cdot i \geq 0$ (note that the nodes above $N_{Top}$ and below $N_{Bot}$ are not exploited and hence no disbalance can be caused on the corresponding voltages). These conditions are exploited by the adaptive technique to find the minimum value of $M$ which guarantees an overall equalization action in each switching period. At first, the modulation is configured as a single-step one, meaning that $M$ is set to 2 and $N_{Bot}$ is set in a way that:

$$\sum_{h=1}^{N_{Bot}} v_{dc,h} \leq v^* \leq \sum_{h=1}^{N_{Bot}+1} v_{dc,h} \quad \left( \text{with} \quad N_{Top} = N_{Bot} + 1 \right) \quad (18)$$

From this initial configuration, the procedure is iterated until the overall effect is self-balancing, thus following the adaptive rule:

$$\begin{array}{ll} \Delta v_{dc,Bot} \cdot i < 0 & \Rightarrow \quad N_{Bot} \rightarrow N_{Bot} - 1 \\ \Delta v_{dc,Top} \cdot i < 0 & \Rightarrow \quad N_{Top} \rightarrow N_{Top} + 1 \end{array} \quad (19)$$

These two conditions are independent from one another and can be evaluated sequentially. Each iteration increases $M$ by 1 and, as a result, the maximum number of iterations is $(M - 2)$.

The overall proposed technique follows the flow-chart depicted in Fig. 4; obviously, in case $M < N$, the equations (8)-(14) need to be applied with the substitutions from (15).

## III. Algorithm Validation

### A. Case study and control strategy

The proposed algorithm can be applied regardless of the

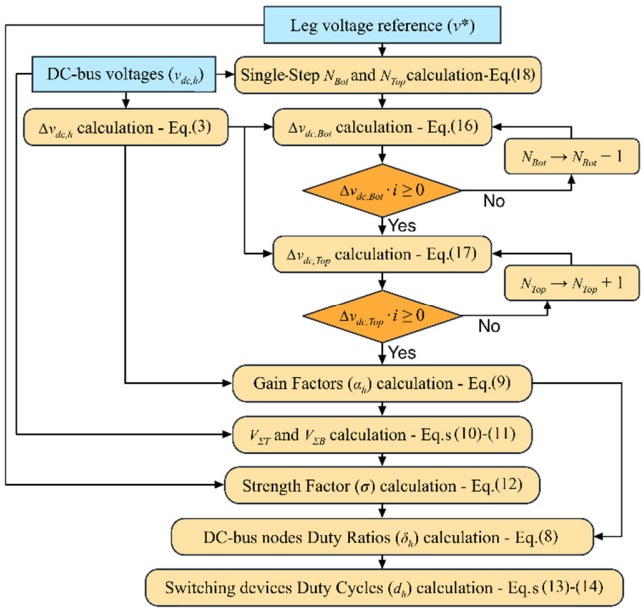


Fig. 4. Flow-chart of the proposed adaptive multi-step technique.

number of MPC legs connected to the same DC-bus capacitors. Naturally, given the system linearity, the capacitors' voltages dynamics result from the superposition of each leg contribution. The average number of switching transitions in an $n$-phase/$N$-level converter, working at a $f_S$ modulation frequency with an $M$-level multi-step modulation technique and supplying a set of sinusoidal voltages with fundamental frequency $f_{AC}$ (considering both the turn-on and the turn-off of all the semiconductor switches) can be approximately estimated as $N_{sw,avg} \approx 4 \cdot n \cdot (M-1) \cdot (f_S/f_{AC})$.

The effectiveness of the proposed technique has been validated with reference to a 9-levels, 3-phases, 3-wires MPC converter employed as an active rectifier between a 1.8 kV/50 Hz AC grid and a 3.3 kV DC line. The overall control scheme, together with the chosen hardware architecture, is shown in Fig. 5. The core of the proposed algorithm is synthetized in the "MOD" blocks, whose inputs are the reference leg voltages $v_k^*$ and the currents $i_k$ and whose outputs are the duty-cycles $d_{k,h}$ (with $k = 1,2,3$ denoting the phase and $h = 1, \ldots, N-1$ denoting the level). The corresponding switching signals are then obtained through the comparison with a common triangular carrier waveform, coherently with the multiple-references/single-carrier working principle [30-35].

The reference phase voltages are computed by a traditional two-stage cascaded control. The outer voltage loop regulates the total DC-bus voltage $V_{dc}$ by processing the error with respect to its reference value $V_{dc}^*$ through a PI regulator, while the inner currents loop operates on the $dq$ rotating frame and acts on the errors between the axis currents $i_d$, $i_q$ and their reference values $i_d^*$, $i_q^*$ by means of two decoupled PI regulators, whose outputs are the axis reference voltages $v_d^*$, $v_q^*$. The position $\vartheta$ and the angular frequency $\omega = 2\pi f_{AC}$ of the rotating $dq$ frame are calculated through a three-phase $dq$ Phase-Locked Loop (PLL) algorithm, which synchronizes on the fundamental positive sequence of the grid phase voltages. Naturally, since $i_q^*$ is set to zero, the phase reference currents lead to a set of sinusoidal and symmetrical currents, which absorb from the grid a constant average active power, proportional to $i_d^*$ and at unity power factor. Finally, the phase reference voltages $v_k^*$ are derived from $v_d^*$, $v_q^*$ by moving in the stationary reference frame and, only when needed, by injecting a common mode voltage $v_0^*$ to enhance the DC bus voltage exploitation (i.e. the common mode voltage injection is unrelated to the equalization procedure).

To further improve the switching frequency reduction, the increase of the number of switching levels via (19) has been applied only when the voltage disbalances $\Delta v_{dc,Bot}$ and $\Delta v_{dc,Top}$ are higher than a given multi-step threshold $\Delta v_{th}$. Contrarily, to always guarantee a fast and stable equalization, the algorithm sets $M = N$ when the maximum deviation of the capacitors' voltages from their average value overcomes a safety threshold (i.e. $\max_h\{ | v_{dc,h} - V_{dc}/(N-1) | \} > \Delta v_{N,th}$).

### B. Hardware-In-the-Loop Settings

The proposed balancing modulation technique has been validated through a Hardware-In-the-Loop simulation, realized through two dSpace platforms.

The first platform (ds1006 equipped with ds5203 and additional piggy-back modules) has been used to emulate the power circuit, consisting of the converter, the AC grid and the DC load (denoted in blue in Fig. 5). The main system parameters are summarized in Table I. The program has been executed with a 400 kHz rate. The switching signals have been supplied through the digital inputs of the system, while the measurements of the needed variables have been given through the analogue

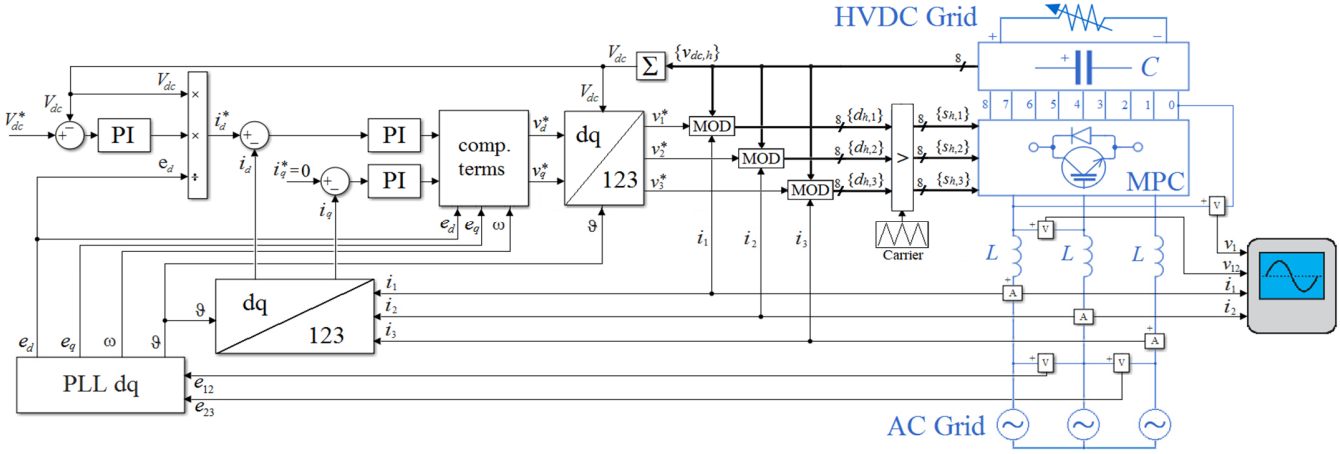


Fig. 5. Overall structure and control scheme for the examined AC/HVDC rectifier system.

TABLE I SYSTEM PARAMETERS

| Variable | Symbol | Value |
|---|---|---|
| Rated Power | $S_R$ | 1 MVA |
| Rated DC Voltage (Total) | $V_{dc,R}$ | 3300 V |
| Rated AC Voltage (ph-ph RMS) | $e_{ph\text{-}ph,R}$ | 1800 V |
| Rated AC Frequency | $f_{AC,R}$ | 50 Hz |
| AC Filtering Inductances | $L$ | 1 mH |
| Number of MPC Levels | $N$ | 9 |
| DC-bus Capacitances | $C$ | 10 mF |

TABLE II CONTROLLER PARAMETERS

| Variable | Symbol | Value |
|---|---|---|
| Modulation Frequency | $f_{carrier}$ | 4 kHz |
| Sampling Frequency | $f_S$ | 4 kHz |
| Adaptive multi-step threshold ($M \rightarrow M+1$) | $\Delta v_{th}$ | 1.5 % |
| $N$-levels multi-step threshold ($M = N$) | $\Delta v_{N,th}$ | 5.0 % |

outputs of the platforms. A standard diode clamped architecture (Fig. 1a) has been selected for the examined converter. The DC capacitances and the AC inductances have been simulated with a 1% random uncertainty from their rated value, while the conduction losses have been simulated through a series resistance of 50 mΩ in each phase. The DC side of the converter is connected to a power-controlled load aimed to emulate a varying power absorption.

The second platform (ds1103) has been used to execute the proposed control algorithm (denoted in black in Fig. 5), which follows the scheme presented in Section III and has been implemented through a C-language script. The main parameters for the equalization procedure are summarized in Table II.

Since the platforms run independently from each other (i.e. they are not synchronized) and the platform emulating the converter runs at 400 kHz, the sensed switching signals coming from the PWM can be subject to a sampling error of ± 2.5 µs, corresponding to an error of ± 1 % in the devices' duty-cycles.

### C. Results for Varying Power

The algorithm has been tested for a varying absorbed power. To validate its effectiveness in a wide loading scenario, the power absorbed from the converter DC side has been chosen as a piecewise-linear function with an initial step increase from 0 to 1 p.u. at 1 s and subsequent variations to 0.75 p.u., 0.5 p.u., 0.25 p.u. and 0 with a constant time derivative set to 0.25/s. The converter, therefore, operates either with a constant or with a slowly varying power flow. All these operating conditions last for 1 second. The results of the whole hardware-in-the-loop simulation results are depicted in Fig. 6, showing the absorbed power (top), the DC-bus capacitors voltages (middle) and the number of switching transitions in the whole converter, averaged in a moving time window of 20 ms length (bottom). The power is normalized by $S_R$, and the voltages by $V_{dc,R}/8$.

It can be noted that the total DC voltage $V_{dc}$ is kept practically constant by the feedback control loop, except for an undershoot of around 8.5% in correspondence of the initial power step variation, which is counteracted by the overshot in the net active power absorbed by the converter.

The proposed equalization technique is always able to keep all the DC voltages in the acceptable range of about $\Delta v_{N,th} \approx \pm 5$ % of the average voltage $V_{dc}/8$. The switching transitions rate is almost constant for the entire power range and, recalling that $N_{sw,avg} \approx 4 \cdot n \cdot (M-1) \cdot (f_S/f_{AC})$, they corresponds to an average number of 5 switching levels (middle region in Fig. 6). It must be pointed out that a lower multi-step

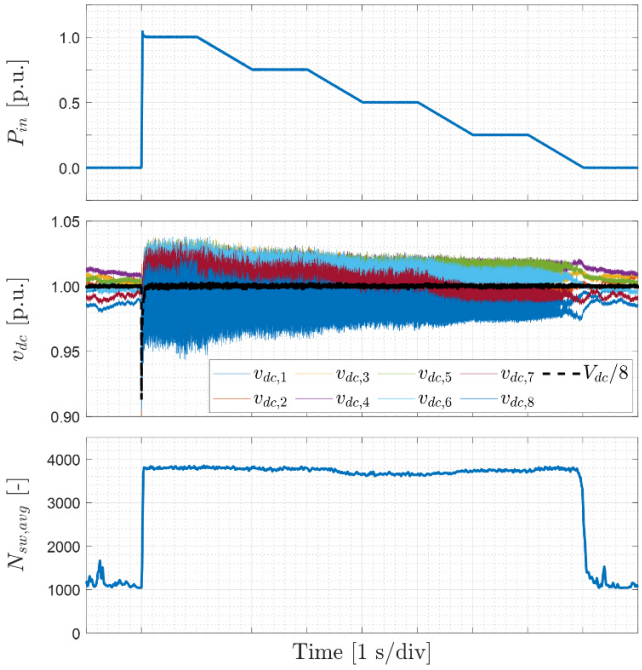


Fig. 6. Equalization technique response in the whole testing scenario. Absorbed power (top); DC-bus capacitors' voltages (middle); Average number of switching transitions (bottom).

threshold would have resulted in a higher transition rate. The value of 5% has been chosen as a good trade-off between the equalization effectiveness and the transition rate. As expected, when the converter is not loaded (i.e. in the first and in the last second in Fig. 6) there is practically no need for the capacitor voltage balancing and the number of switching levels (and the corresponding transition rate) are drastically reduced.

The steady state results for 100%, 50% and 0% rated power absorption are shown in Fig. 7 and compared with the adaptive technique proposed by the authors in [35] and with the modulation technique described in [34], which has been selected as a baseline multi-step approach capable of guaranteeing the DC capacitors equalization (but which does not actively address the switching transitions reduction). The yellow and green waveforms are the AC grid currents $i_1$ and $i_2$, the blue waveform is the line-to-line voltage $v_{12}$ and the red waveform is the leg voltage $v_1$.

The multi-step operation is clearly evident in the leg voltage waveforms (red). The baseline approach, which does not address the switching transitions rate reduction, always exploits either 8 or 9 levels. On the contrary, the adaptive techniques are capable of reducing the number of levels needed for the modulation while at the same time controlling the DC-bus capacitors voltages. It is worth noting that both the proposed technique and the approach [34] may lead to a non-uniform switching pattern, since in general the voltage equalization is not synchronous with the AC grid fundamental frequency. This is especially evident in the no-load leg voltage waveforms (top row in Fig. 7), where the multi-step algorithm is heavily affected by the measurement noises. Nevertheless, the voltage harmonics associated to this phenomenon (whose magnitudes are negligible with respect to the fundamental component) act as low frequency disturbances and, therefore, are drastically neutralized by the current controllers.

Fig. 8 shows the harmonic spectra of the leg voltage $v_1$ (top), the line-to-line $v_{12}$ (middle) and the AC grid current $i_1$ (bottom)

in the rated converter conditions. While the fundamental components are equal for all the modulation strategies, the main higher order harmonic contributions (which are centered around the integer multiples of the switching frequency) differ from case to case. The proposed technique, while being characterized by a larger bandwidth of higher order harmonics, shows reduced magnitudes with respect to the other two approaches. The low order harmonics in the leg voltages of the baseline

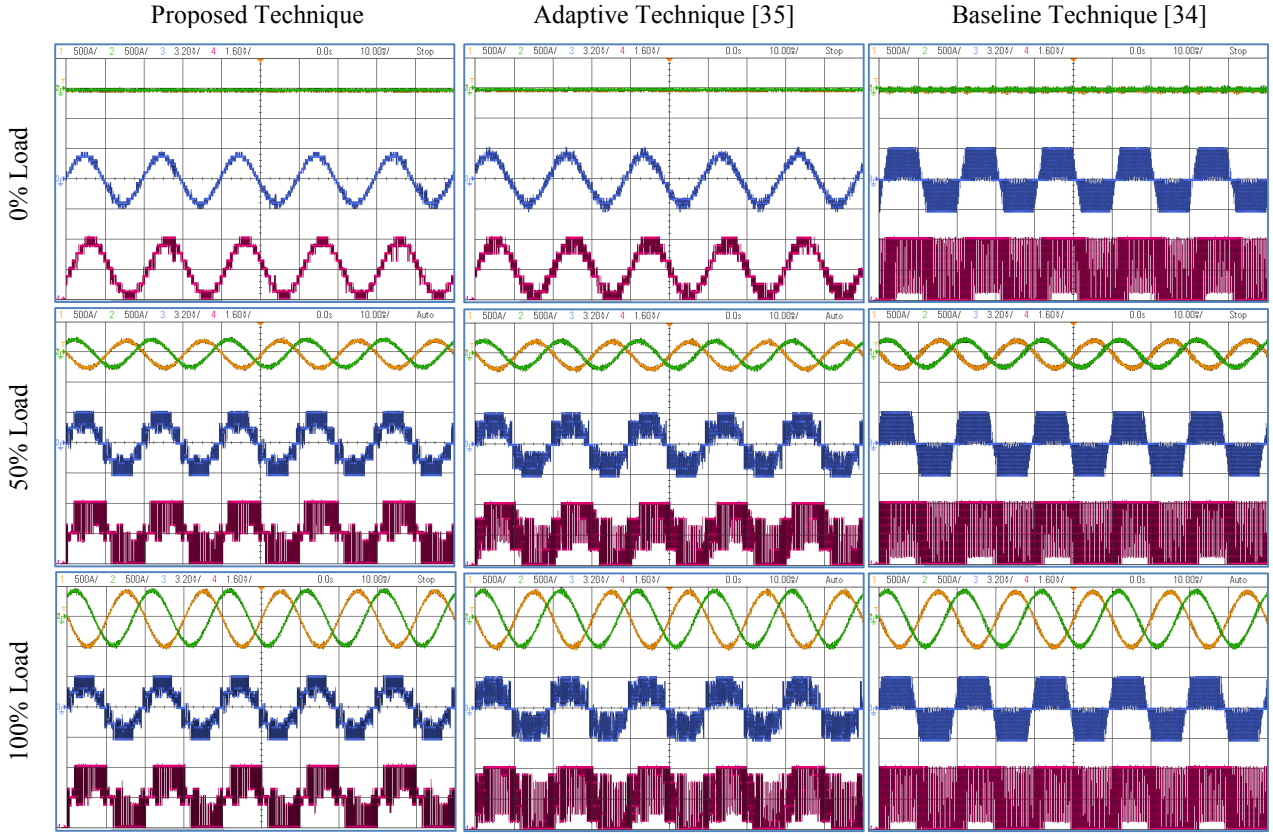


Fig. 7. Steady state results for varying power absorption and different modulation techniques.
(yellow: AC grid current $i_1$; green: AC grid current $i_2$; blue: MPC line-to-line voltage $v_{12}$; red: MPC leg voltage $v_1$)

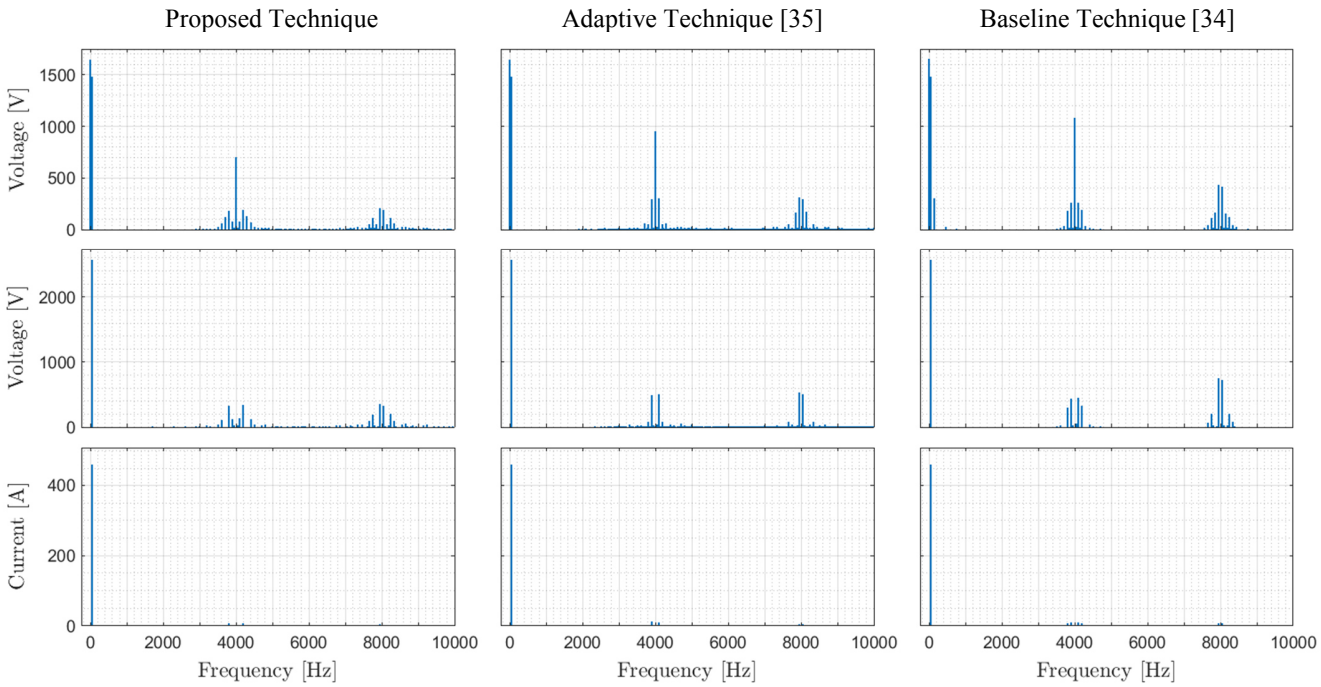


Fig. 8. Harmonic spectra of the MPC leg voltage $v_1$ (top), phase-to-phase voltage $v_{12}$ (middle) and phase current $i_1$ (bottom) in the converters' rated conditions (100% Load) for different modulation techniques.

TABLE III COMPARISON OF THE PROPOSED TECHNIQUE WITH OTHER MODULATION STRATEGIES FOR DIFFERENT POWER ABSORPTIONS

| | | Proposed Approach | Adaptive Technique [35] | Baseline Technique [34] |
|---|---|---|---|---|
| 0% Load | Number of Switching Transitions | 1150 | 2350 | 7372 |
| | Maximum DC Voltage Deviation | 1.92 % | 1.07 % | 1.03 % |
| | Leg Voltages THD | 0.216 | 0.607 | 1.028 |
| | Line-to-Line Voltages THD | 0.093 | 0.348 | 0.607 |
| 50% Load | Number of Switching Transitions | 3671 | 5145 | 7372 |
| | Maximum DC Voltage Deviation | 3.26 % | 2.34 % | 0.38 % |
| | Leg Voltages THD | 0.681 | 0.824 | 1.010 |
| | Line-to-Line Voltages THD | 0.421 | 0.502 | 0.593 |
| | AC Grid Currents THD | 0.070 | 0.085 | 0.103 |
| 100% Load | Number of Switching Transitions | 3820 | 6950 | 7372 |
| | Maximum DC Voltage Deviation | 5.01 % | 5.00 % | 0.35 % |
| | Leg Voltages THD | 0.728 | 0.923 | 1.003 |
| | Line-to-Line Voltages THD | 0.452 | 0.564 | 0.591 |
| | AC Grid Currents THD | 0.038 | 0.047 | 0.049 |

TABLE IV COMPARISON OF THE PROPOSED TECHNIQUE FOR DIFFERENT MODULATION INDEX VALUES

| | $m = 0.7$ | $m = 0.8$ | $m = 0.9$ | $m = 1.0$ | $m = 1.1$ |
|---|---|---|---|---|---|
| Total DC Voltage | 4230 V | 3700 V | 3300 V | 2965 V | 2700 V |
| Number of Switching Transitions | 3860 | 3870 | 3820 | 3690 | 3140 |
| Maximum DC Voltage Deviation | 4.07 % | 4.65 % | 5.01 % | 5.06 % | 5.07 % |
| Leg Voltages THD | 0.974 | 0.849 | 0.728 | 0.635 | 0.519 |
| Line-to-Line Voltages THD | 0.480 | 0.468 | 0.452 | 0.409 | 0.341 |
| AC Grid Currents THD | 0.043 | 0.040 | 0.038 | 0.038 | 0.034 |

technique [34] are due to the common mode voltage injection in all the converter phase legs and, indeed, are absent both in the line-to-line voltage and in the AC grid current spectra.

Table III summarizes some data of interest, like the average number of switching transitions, the maximum DC voltage deviation from the average value and the Total Harmonic Distortion (THD) of the leg voltages, the line-to-line voltages and the AC grid currents.

Given the aforementioned non-uniform operating pattern, the tabled values should be considered as the rounded average values over a sufficiently long time interval (several fundamental periods). Since the AC grid currents fundamental component is close to 0 when the converter is unloaded, the corresponding THD is not significant and has been omitted.

As can be observed, by allowing a small deviation of the DC-bus capacitors voltages from their rated values, both adaptive techniques are able to drastically reduce the average number of switching transitions in a fundamental period with respect to the baseline technique [34], generally resulting in a lower voltage and current THD. In all the operating conditions the proposed adaptive technique behaves better than the one described in [35], where the adaptation of the number of switching levels is based on a feedback loop acting on the maximum deviation between the DC capacitors voltages $v_{dc,h}$ and their average value $V_{dc}/8$.

### D. Results for Varying Modulation Index

The algorithm has been tested for a varying modulation index $m = 2\sqrt{2/3}\, e_{ph\text{-}ph}/V_{dc}$. The AC side of the converter has been kept the same in all the conditions (i.e. equal to the rated value $e_{ph\text{-}ph,R}$), while the total DC voltage has been changed to obtain different values of $m$. In all the operating conditions the converter is subject to the same power flow $S_R$, which corresponds to the same AC grid currents. The results obtained for $m = \{0.7; 0.8; 0.9; 1.0; 1.1\}$ are depicted in Fig. 9 and summarized in Table IV. It can be easily noted that, despite a small increase in the maximum DC-bus capacitors voltage disbalances (which have been normalized by their respective average value $V_{dc}/8$), the highest modulation index values are characterized by the lowest switching transitions rate. This effect can be explained by considering that the common mode voltage injection needed when $m > 1$ (which allows to extend the linear modulation region and, as previously stated, is completely unrelated to the equalization algorithm) produces in some intervals a clamping of the leg output voltages $v_k^*$ either to 0 or to $V_{dc}$, thus forcing the corresponding devices not to switch for several modulation periods. This behavior has also a positive influence on the both the voltages and the currents THD.

## IV. CONCLUSIONS

This paper presented a novel pulse-width modulation technique for multi-point clamped converters, aimed to carry out the voltage equalization between the DC-bus capacitors while preserving the desired average output voltage.

The approach is based on a multiple-references/single-carrier intersective method and is discussed with respect to a generic converter leg. It is intrinsically generalized with respect to the number of converter levels and, contrarily to most of the actual available techniques, does not rely on the injection of a common mode reference voltage, resulting in the independence of the balancing effectiveness from the AC side modulation index and power factor. The equalization process is achieved by allowing each leg output voltage to switch between more levels in the same modulation interval (multi-step behaviour). Then, the main drawback is represented by the increase of the average switching frequency of the converter devices, which can worsen the AC voltages/currents THD and increase the switching losses. A proper trade-off between the balancing capability and the switching behaviour has been achieved by dynamically adapting the feasible switching levels for each leg on the basis of the converter's instantaneous working conditions.

Several hardware-in-the-loop simulations of a 1.8 $kV_{AC}$/3.3 $kV_{DC}$ rectifier have shown the effectiveness of the

proposed technique, which is able to keep the capacitors balanced even in the heaviest transient operations, regardless of the active power absorbed by the AC grid. The algorithm has been evaluated both for a varying power flow and for a varying modulation index. It has also been compared to the adaptive technique presented by the authors in [35] and to the modulation technique discussed in [34]. In all the operating conditions, and especially for high modulation indexes, it has been proven to be an effective technique to limit the average switching transitions rate while keeping all the DC-bus capacitors' voltages within desired limits.

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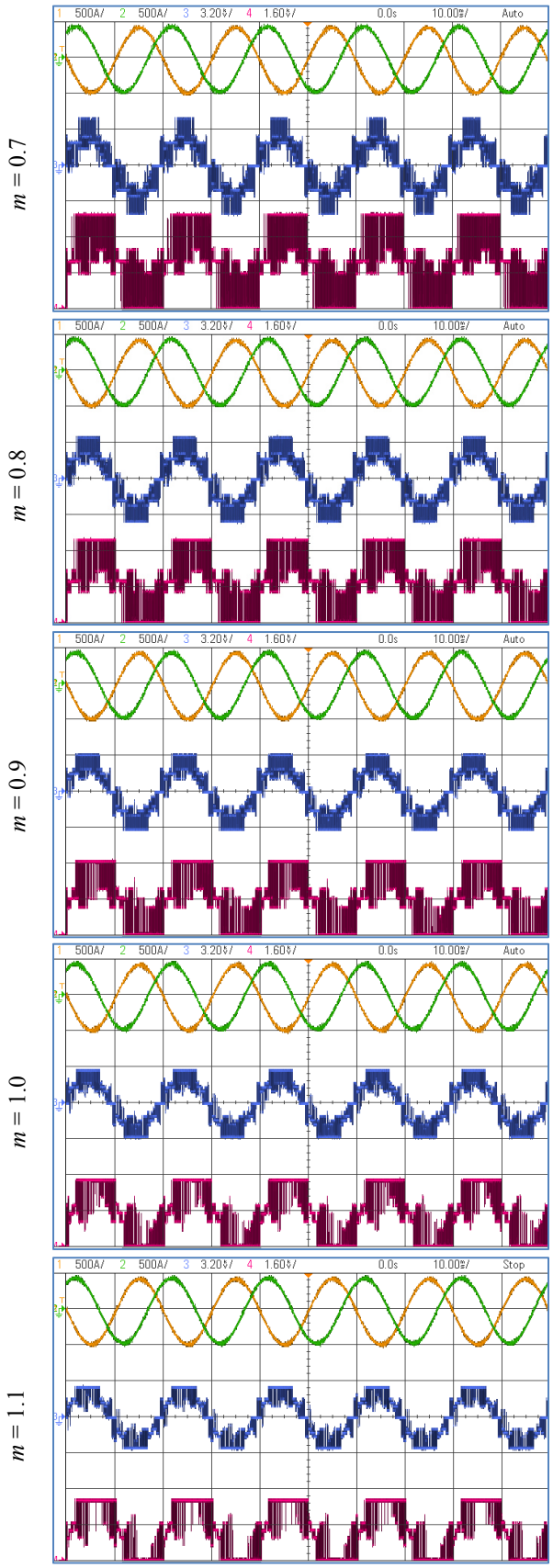


Fig. 9. Steady state results for varying modulation index values. (yellow: AC grid current $i_1$; green: AC grid current $i_2$; blue: MPC line-to-line voltage $v_{12}$; red: MPC leg voltage $v_1$)

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