JITTER TOLERANT HYBRID SIGMA-DELTA MODULATOR

A Thesis

by

HAIYUE YAN

Submitted to the Office of Graduate and Professional Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

Chair of Committee,	Jose Silva-Martinez
Committee Members,	Sebastian Hoyos
	Sunil P. Khatri
	Rainer J. Fink
Head of Department,	Miroslav M. Begovic

August 2019

Major Subject: Electrical Engineering

ABSTRACT

Commonly used in wireless applications and consumer products, Continuous-time (CT) Sigma Delta ($\Sigma\Delta$) Analog to Digital Converter (ADC) stands out for its high resolution, less input signal conditioning and large incorporating with digital signal processing. The clock jitter impact on CT $\Sigma\Delta$ ADC is a critical issue as it will directly increase the noise floor within signal bandwidth. Thus, reducing jitter sensitivity is beneficial for improving the performance of CT $\Sigma\Delta$ ADC.

This thesis presents a novel idea of reducing CT $\Sigma\Delta$ ADC jitter sensitivity by splitting one stage of continuous-time integrator into two parts - a gain stage and a digital low-pass filter. The gain stage remains prior to quantizer for compensating the loss of loop gain when removing the original continuous-time integrator. The digital filter is placed at the output of quantizer to suppress the out-of-band noise level. This hybrid $\Sigma\Delta$ ADC is implemented with two configurations in system level with TSMC 40nm CMOS technology at 20 MHz bandwidth and 640 MHz sampling frequency. The maximum SNR of the hybrid $\Sigma\Delta$ ADC is 69.18 dB. The proposed ADC achieves the maximum of 14 dB better SQNR than the conventional CT $\Sigma\Delta$ ADC at RMS jitter as high as 10% of the clock period. A negative resistor gain boosting single stage amplifier is also presented in this thesis.

ACKNOWLEDGMENTS

I would like to express my greatest gratitude to my advisor, Dr. Jose Silva-Martinez, for his patient guidance and solid support. My learning curve was exponential under his guidance. His extensive knowledge and devotion to research make him a role model for my future career in engineering.

Secondly, special thanks to my committee members: Dr. Sebastian Hoyos, Dr. Sunil P. Khatri and Dr. Rainer J. Fink for their valuable remarks and suggestions.

I would like to thank SungJun Yoon as a knowledgeable senior group fellow. I would also like to thank Zizhen Zeng for his generous help. Thanks to my friends and colleagues Po-Hsuan Chang, Li Guan and many more for making my time in TAMU wonderful.

Finally, I would like to express my deepest appreciation to my parents. Although we are thousands of miles apart, I can always feel their endless love. I am very grateful to have parents like them.

CONTRIBUTORS AND FUNDING SOURCES

Contributors

This work was supported by a thesis committee consisting of Professor Jose Silva-Martinez, Professor Sebastian Hoyos and Professor Sunil P. Khatri of the Department of Electrical and Computer Engineering and Professor Rainer J. Fink of the Department of Engineering Technology and Industrial Distribution.

The system block diagram depicted in Chapter 4.1.1 was designed in part by SungJun Yoon of the Department of Electrical and Computer Engineering. All other work conducted for the thesis was completed by the student under the advisement of Professor Jose Silva-Martinez of the Department of Electrical and Computer Engineering.

Funding Sources

Graduate study was supported by the one-time graduate merit scholarship in the Department of Electrical and Computer Engineering from Texas A&M University .

TABLE OF CONTENTS

Page

LIST OF FIGURES

FIGURE Page

LIST OF TABLES

TABLE Page

1. INTRODUCTION

1.1 Motivation

The recent trend in wireless communication system receiver front-end is to move ADCs toward antenna in order to take advantage of the low-cost, low-power and flexible digital processing. With lighter filtering in front, the ADCs are expected to have higher dynamic range to tolerant blocker residues, PAR and headroom [4]. Unlike Nyquist rate ADCs requiring high input signal conditioning and precise component matching, $\Sigma\Delta$ ADC eases the demanding on analog elements although complicated the favorable digital signal processing on output signal [7]. With the implicit anti-aliasing property that relaxing the requirement on high-order front filters, continuous-time $\Sigma\Delta$ modulators have become an attractive choice for building analog-to-digital converters (ADCs) for wireless systems [16].

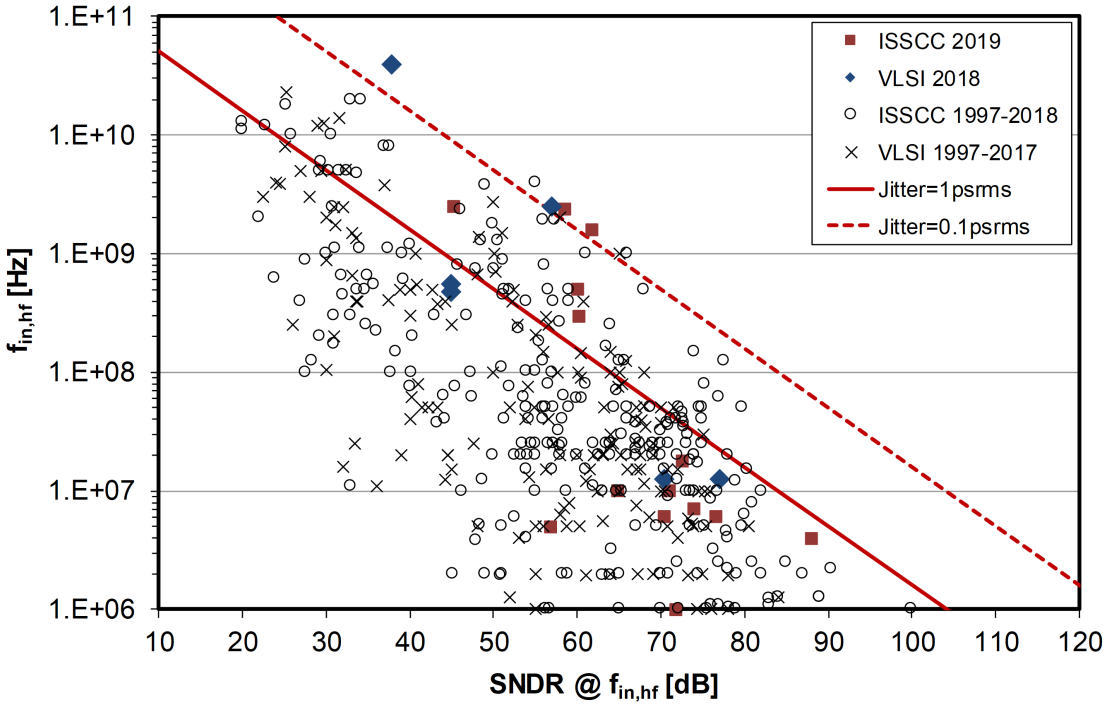


Figure 1.1: ADC survey 1997-2019.

Out of many non-idealities, clock jitter fundamentally sets the limitation on ADC performance and this concept is clearly illustrated in Figure 1.1 [8]. Even if the ADC is purely ideal, the jitter induced noise will set the boundary on maximum achievable SNDR. As a matter of fact, CT $\Sigma\Delta$ modulators are well-known to be sensitive to the clock jitter coming from digital-to-analog converter (DAC) [3]. The convolution of feedback DAC clock jitter and out-of-band quantization noise folds back onto signal band and increases the noise floor thus deteriorates the achievable SNR. This severe problem is considered one of the main drawbacks that prevents CT $\Sigma\Delta$ modulator being even wider used. Therefore, it is critical to minimize the CT $\Sigma\Delta$ ADC jitter sensitivity especially in broadband systems.

The thesis mainly introduces a novel technique to reduce jitter sensitivity in CT $\Sigma\Delta$ ADC for next-generation wireless communication systems. The main purpose of designing the ADC is to relax the requirements on clock generators (like Phase Lock Loops) that generating clock for the ADCs.

1.2 Thesis Organization

This thesis describes the system level design and simulation results of a new jitter tolerant hybrid $\Sigma\Delta$ modulator. This idea is implemented in both feedback and feedforward, fourth order and third order configuration at system level. A single stage gain boosting amplifier is also presented. The thesis is organized as follows.

The first chapter addresses the importance of CT $\Sigma\Delta$ modulator on wireless systems and briefly talks about the importance of reducing the jitter sensitivity for CT $\Sigma\Delta$ modulator.

The second chapter reviews some basics on the analog to digital converters in general, then focuses on CT $\Sigma\Delta$ modulator and its jitter effect is discussed in detail.

The third chapter presents the system level design of a fourth order jitter tolerant hybrid $\Sigma\Delta$ modulator in feedback configuration, the loop transfer function synthesis approach is described thoroughly and the simulation results are shown as well.

The fourth chapter provides a third order jitter tolerant hybrid $\Sigma\Delta$ modulator with feedforward-feedback configuration. The design of a single stage negative resistor gain boosting amplifier is

presented and the system level simulation with integrators implemented with this amplifier is also posted.

The last chapter concludes the thesis.

2. SIGMA DELTA ADC OVERVIEW

2.1 Analog to Digital Converter

Nowadays, an increasing number of signals are processed in digital so as to take advantage of its robustness and portability. Since the world stubbornly stays in analog, the Analog-to-Digital Converter (ADC) has become an indispensable part in signal processing. As can tell from its name, ADC refers to the block that converts the continuous analog signal into digital form that mostly consists of ones and zeros.

2.1.1 Sampling and Quantization

The converting from analog to digital signal is a two-step process which is the combination of sampling and quantization.

Sampling is defined as the time domain multiplication of continuous signal and the delta impulse train. The sampling of continuous signal $x(t)$ by a clock with period of T_s can be expressed as (2.1), where $x_s(nT_s)$ is the sampled output.

$$x_s(nT_s) = x(t) \sum_{n=-\infty}^{\infty} \delta(t - nT_s) \tag{2.1}$$

As we all know that time domain multiplication is frequency domain convolution, thus the sampled signal in frequency domain is given by:

$$X_s(f) = \frac{1}{T_s} \sum_{n=-\infty}^{\infty} X(f - nf_s), \tag{2.2}$$

where $X_s(f)$ denotes the sampled signal in frequency domain, f_s is the sampling frequency and $X(f)$ is the Fourier transform of $x(t)$. Thus sampling in frequency domain creates a series of replicas of the original continuous time signal spectrum centering around the integral multiple of sampling frequency.

The quality of clock directly determines the sampling results. Figure 2.1 is the track and hold

circuit that controlled by clock ϕ_1. Whenever the clock goes down, i.e. the tracking phase, the switch turns on and the output signal $V_{out}[n]$ closely follows the input signal $V_{in}(t)$; when the clock goes up, which is the hold phase, $V_{out}[n]$ holds the voltage at the clock raising edge. As shown in Figure 2.2, assume the clock edge at $t = t_0$ is the ideal clocking edge, while the clock at $t = t_0 + \Delta T$ is the edge of the jittery clock. Therefore, the difference between the two samples are jitter induced error, ΔV.

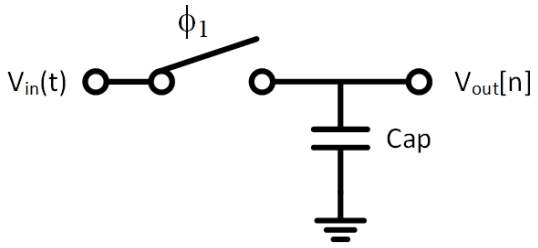


Figure 2.1: Track and hold circuit.

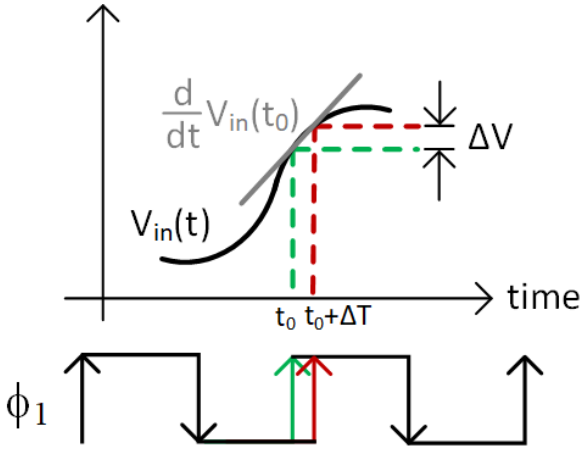


Figure 2.2: Time domain sampling.

Consider the case where $V_{in}(t) = V_{pk}sin(\omega_{in}t)$, the jitter induced error is given by

$$\Delta V = \Delta T\big[\frac{d}{dt}V_{in}(t_0)\big] = \big[V_{pk}\omega_{in}\Delta T\big]cos(\omega_{in}t_0) \tag{2.3}$$

where ω_{in} and V_{pk} are the frequency and the peak amplitude of the input sinusoidal signal, respectively.

Assume σ^2 is the variance of aperture uncertainty ΔT, thus the jitter induced noise power can be written as

$$\sigma^2_{jitter} = \frac{\big(V_{pk}\omega_{in}\sigma\big)^2}{2} \tag{2.4}$$

The jitter induced SNR is given by

$$SNR_{jitter} = \frac{P_{sig}}{\sigma^2_{jitter}} = \frac{1}{\big(\omega_{in}\sigma\big)^2} \tag{2.5}$$

According to (2.5), the SNR_{jitter} is a linear function of input frequency at logarithmic scale.

Ideal sampling is an honest replica of the original signal and introduces no error or distortion. Non-ideal sampling, where sampling frequency is lower than twice of the maximum signal frequency, produces no error as well, but it results in aliasing. It is the quantization that introduces errors.

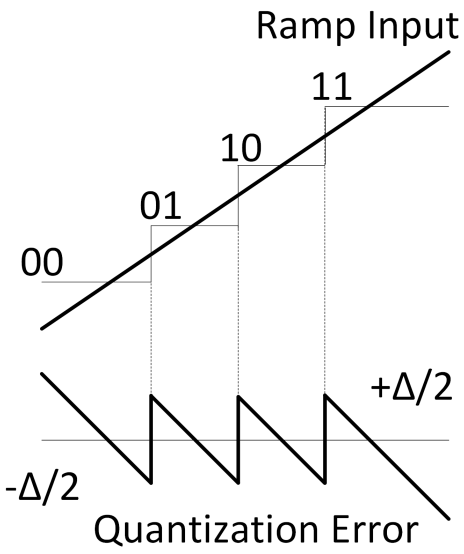


Figure 2.3: Ramp input and quantization error.

After continuous signal is sampled into discrete form, the discrete amplitudes are assigned to limited number of values according to the resolution of ADC. The difference between quantized level and the original signal amplitude is quantization error. As what shown in Figure 2.3, the case where ramp input signal is considered.

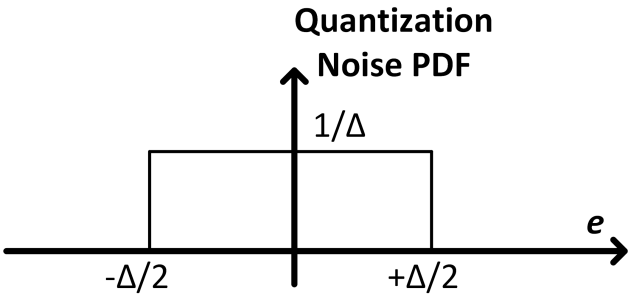


Figure 2.4: Quantization noise distribution.

If only consider the ramp input within linear range, the maximum quantization noise is $\pm\frac{\Delta}{2}$, where Δ represents the step size of the quantizer. Generally, when the input signal is random and

fast changing within quantizer linear range, the quantization noise can be regarded as having flat spectrum [15] and the probability density of quantization error has a uniform distribution within $\pm\frac{\Delta}{2}$ range as shown in Figure 2.4 [17]. The quantization noise density (at a bandwidth of 1 Hz) is given by [1]:

$$\overline{e^2} = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} e^2 de = \frac{\Delta^2}{12} \tag{2.6}$$

2.1.2 ADC Performance Measures

The ADC performance is often quantified by Signal-to-Quantization-Noise Ratio (SQNR). If we consider a sinusoidal input with peak-to-peak full-scale amplitude V_{FS}, which can be represented as $\Delta \cdot 2^N$, again Δ denotes the quantizer step size, the SQNR can be written as:

$$SQNR = \frac{P_{signal}}{P_{Qnoise}} = \frac{(\frac{V_{FS}}{2\sqrt{2}})^2}{\frac{\Delta^2}{12}} = 6.02N + 1.76\, dB, \tag{2.7}$$

where N stands for the number of bit of the ADC. Since there are other types of error and distortion in ADCs apart from quantization noise, therefore, Signal-to-Noise-plus-Distortion Ratio (SNDR) is defined to take all the other non-idealities into consideration.

$$SNDR = \frac{P_{sig}}{V_{noise}^2 + \sigma_{jitter}^2 + V_{\varepsilon}^2}, \tag{2.8}$$

where V_{noise}^2 denotes the noise power, including thermal noise and quantization noise, σ_{jitter}^2 is the jitter induced noise power and V_{ε}^2 is the distortion. An important metric, Effective-Number-of-Bits (ENOB), is defined based upon SNDR as:

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{2.9}$$

ENOB measures the effective resolution of an ADC considering all noise and nonidealities.

2.2 Nyquist Rate ADC and Oversampling ADC

Depending on the ratio between half of sampling frequency and signal bandwidth, the analog-to-digital data converters can be divided into two main categories: Nyquist-rate ADC and oversampling ADC.

For Nyquist rate ADC, Nyquist frequency is often right at or slightly higher than the edge of maximum signal frequency, whereas for oversampling ADC, the ratio between Nyquist frequency and signal bandwidth of which can be ten or even hundred. Therefore, since the maximum sampling frequency is often set by the technology, Nyquist rate ADCs usually work at a larger signal bandwidth comparing with oversampling ADCs for the same sampling frequency.

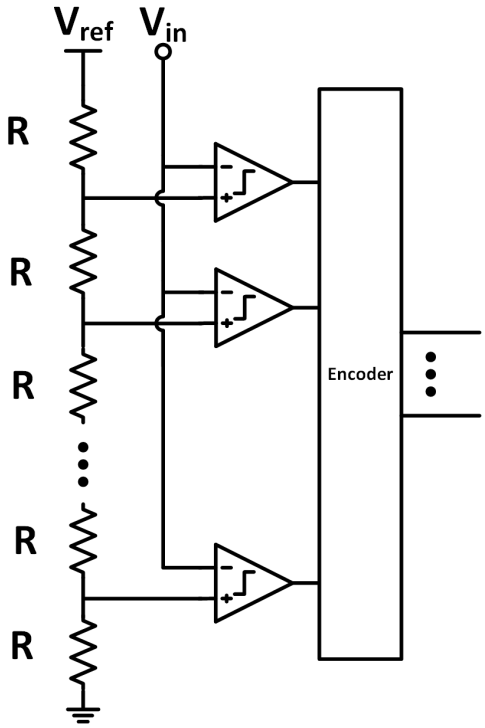


Figure 2.5: Flash ADC example.

There are different types of Nyquist rate ADC, like pipeline ADC, flash ADC, etc. A common character among Nyquist rate ADCs is that although they generally dominant at high frequency

applications, their resolutions can barely achieve higher than 12-bit [11], as the precision relies heavily on the matching between analog components. Taking flash ADC as an example. As shown in Figure 2.5, flash ADC consists of a resistor ladder and a bunch of comparators, the number of which equals to two to the power of the target resolution in bits minus one. Since the resistor ladder generates the reference voltages for the comparators, thus the quality of matching between resistors directly affects the resolution.

Unlike Nyquist rate ADC, oversampling ADC extricates itself from the limitation set by component matching, thus can obtain very high accuracy. As a matter of fact, oversampling ADC achieves high resolution by using the power of noise shaping, therefore the physical matching limit is eliminated in $\Sigma\Delta$ modulator. Oversampling ADC has proved to be very useful in applications where high resolution is required like radio applications, where the requirements on data converter resolution can be as high as 18 or even higher [15]. More details about $\Sigma\Delta$ ADC will be discussed in following sections.

2.3 Sigma Delta Modulator

The simplified $\Sigma\Delta$ ADC linearized model is shown in Figure 2.6. It consists of an analog loop filter, a quantizer and a feedback DAC. Analog loop filter is a high gain low-pass filter providing large loop gain to attenuate the in-band noise. It is often implemented with integrators which integrates the error between input signal and the signal coming from feedback DAC. Quantizers, built with low resolution ADCs, convert the continuous signal into digital form but introducing quantization noise in the meantime.

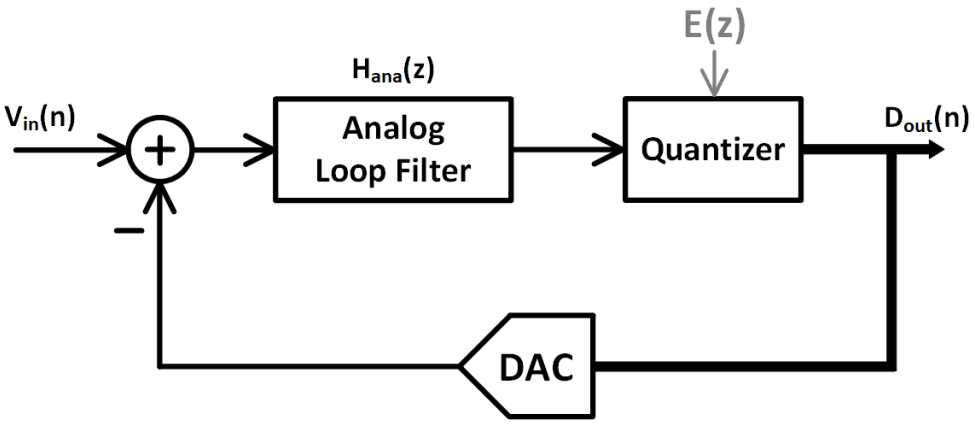


Figure 2.6: $\Sigma\Delta$ modulator linearized model.

According to Mason's rule, the output digital signal can be expressed as:

$$D_{out}(z) = \frac{H_{ana}(z)}{1 + H_{ana}(z)} V_{in}(z) + \frac{1}{1 + H_{ana}(z)} E(z) \tag{2.10}$$

The transfer function that input signal multiplying with is called Signal Transfer Function (STF) and the transfer function processing error signal is the Noise Transfer Function (NTF).

$$STF(z) = \frac{H_{ana}(z)}{1 + H_{ana}(z)} \tag{2.11}$$

$$NTF(z) = \frac{1}{1 + H_{ana}(z)} \tag{2.12}$$

STF has a low-pass shape with flat 0 dB gain within band-of-interest in order to maintain the original input signal, while NTF has a high-pass shape for moving the in-band quantization noise to out-of-band. The examples of STF and NTF of a conventional 3rd order $\Sigma\Delta$ modulator are shown in Figure 2.7 and Figure 2.8, respectively.

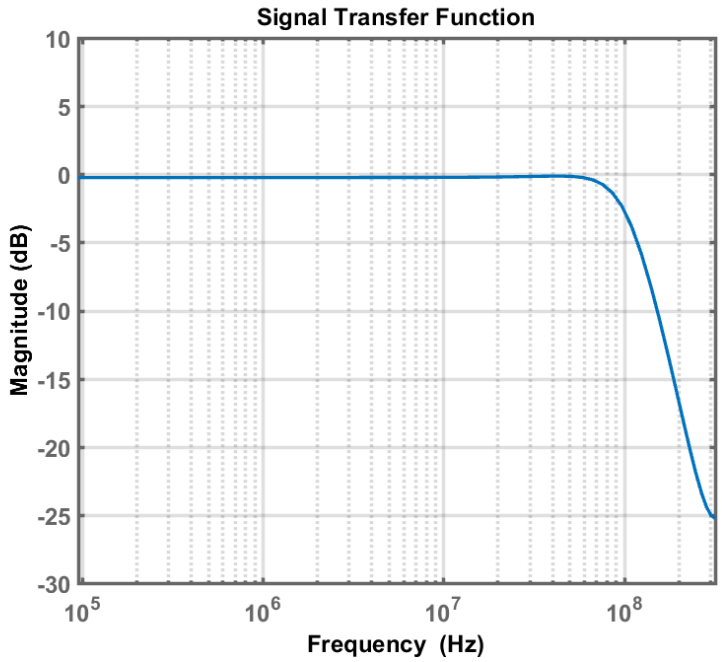


Figure 2.7: STF example of a conventional 3rd order $\Sigma\Delta$ modulator.

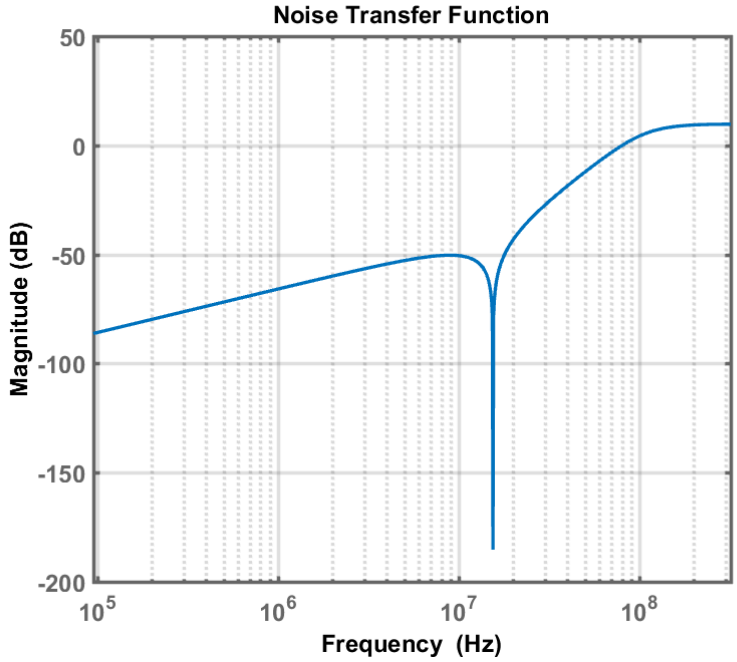
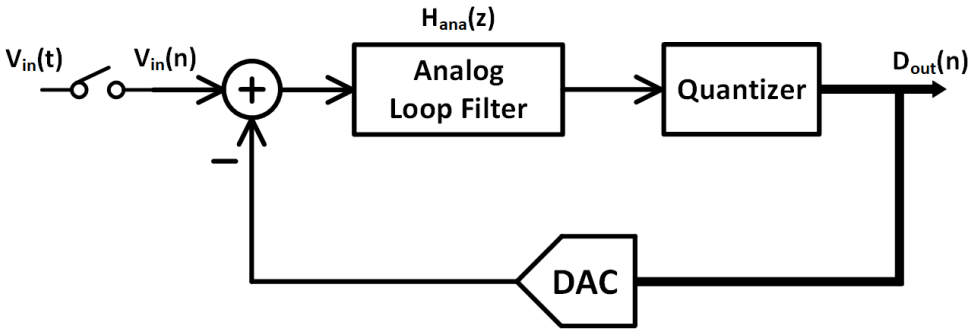
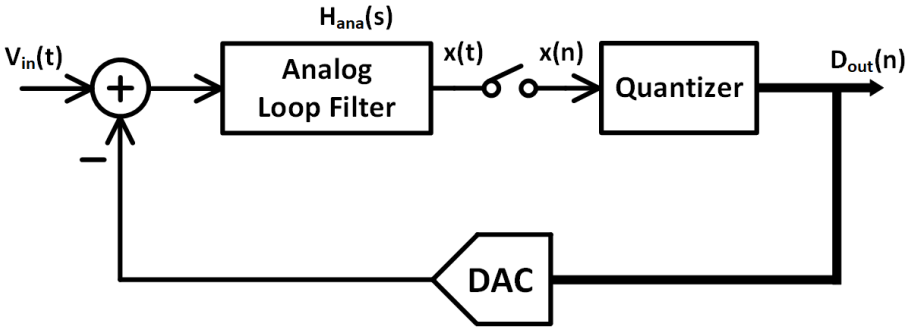


Figure 2.8: NTF example of a conventional 3rd order $\Sigma\Delta$ modulator.

Depending on the place sampling happens, $\Sigma\Delta$ ADC can be categorized into two main types, one is continuous-time (CT) $\Sigma\Delta$ ADC and another one is discrete-time (DT) $\Sigma\Delta$ ADC. The difference between CT $\Sigma\Delta$ modulator and DT $\Sigma\Delta$ modulator is illustrated in Figure 2.9 (a) and Figure 2.9 (b). Since DT $\Sigma\Delta$ modulator samples up-front, the analog filter should be implemented with discrete integrators, whereas in CT $\Sigma\Delta$ modulator sampling happens right before quantizer, thus the analog loop filter is in continuous version.



(a)



(b)

Figure 2.9: (a) DT $\Sigma\Delta$ modulator simplified schematic. (b) CT $\Sigma\Delta$ modulator simplified schematic.

The main advantage of DT $\Sigma\Delta$ modulator is that the integrators are implemented as switch-cap circuit where the coefficients equal to the ratio between capacitors. This relative ratio is very reliable and does not change much with PVT variation. Another desirable feature of DT $\Sigma\Delta$ modulator is that the design is more straightforward compared with its CT counterpart. For example,

important parameters, delay for instance, can be directly represented as discrete parameters and, in fact, normally CT $\Sigma\Delta$ modulator design procedure starts with generating discrete-time loop transfer function.

However, there are some drawbacks in DT $\Sigma\Delta$ modulator as well. To begin with, DT $\Sigma\Delta$ modulator is very demanding for the amplifiers inside integrators. Considering the fact that discrete-time integrator is often implemented with switch-cap circuit, thus the amplifier must be able to settle with decent accuracy within half of the clock period. That means, if the DT $\Sigma\Delta$ modulator were to work at a very high sampling frequency, the amplifier will consume a huge amount of power out of the whole ADC chip. Therefore, normally the DT $\Sigma\Delta$ modulator is often working at a sampling frequency no more than 300 MHz, while in continuous-time implementation, the requirement on the amplifier is way less stringent.

The most well-known advantage of CT $\Sigma\Delta$ modulator is that it has inherent anti-aliasing property, which may eliminate the necessity of adding a low-pass filter prior to the whole modulator. However, this assumption of getting rid of the anti-aliasing filter is only valid when the $\Sigma\Delta$ modulator bandwidth is very limited and the real input signal is ideally clean without any frequency components locating out of the signal band. Otherwise, the out-of-band blockers are very likely to be amplified by the out-of-band peaking in signal transfer function and the boosted signal may destroy the whole system.

CT $\Sigma\Delta$ modulator is easily affected by many non-idealities like feedback DAC clock jitter and excess loop delay. Since this paper focuses on the design that improving the jitter performance, the jitter impact is discussed thoroughly in Chapter 2.3.2.

2.3.1 Sigma Delta Modulator System Level Design Considerations

A typical third order conventional $\Sigma\Delta$ modulator block diagram in CIFB (Cascade of Integrators with Distributed Feedback) structure is shown in Figure 2.10 as a beginning for discussion. The input signal first goes into the analog filter (H_{ana}) consisting of three integrators, passes through a low resolution ADC and eventually is fed back to the analog filter by DACs.

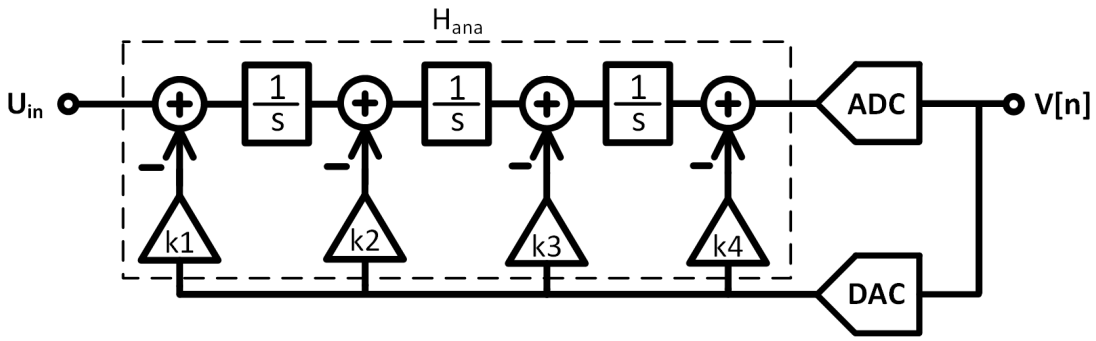


Figure 2.10: Conventional 3rd order CT $\Sigma\Delta$ modulator block diagram

Order

The order of $\Sigma\Delta$ modulator is generally defined as the number of integrators in the modulator. It is beneficial to have higher order for better noise shaping. However, in the cases where modulator with very high order number is implemented, the modulator is very complicated and it may not even be stable. In this project, a 3rd order and a 4th order $\Sigma\Delta$ modulators are implemented.

Number of Quantizer Level

The number of quantizer level also has impact on the achievable SNR as increasing quantizer level enhances the resolution of the whole $\Sigma\Delta$ modulator altogether [2]. The down side is, with higher quantizer level, the circuit complexity increases drastically, considering a typical case that quantizer is implemented with flash ADCs, the complexity of which is proportional to two to the power of quantizer resolution minus one. In the meantime, increasing quantizer level requires higher DAC resolution and DAC linearity decreases a lot with the increasing of its resolution.

Oversampling Ratio

Over-Sampling Ratio (OSR), defined as (2.13) characterizes how quick the Nyquist frequency compared with the maximum signal bandwidth.

$$OSR = \frac{f_s/2}{f_{bw}} \tag{2.13}$$

OSR represents the level of oversampling and, typically, OSR is within the range of 32 to 256 [2]. [15] points out that the maximum achievable SQNR is positive proportional to $2L + 1$ power of oversampling ratio, where L is the order number. Thus higher OSR means better SNR.

Noise Transfer Function

Noise transfer function (NTF) is the key transfer function that directly determines modulator performance. NTF defines as the transfer function from quantizer to the overall modulator output, which is the high-pass filter that process the quantization noise. Since the NTF has a high-pass shape in natural, the in-band low frequency noise is modulated in a way that part of it is shaped to out-of-band (OOB) and thus the OOB noise level can reach even higher than unity. The lower in-band NTF amplitude means the modulator has a higher ability to shape the in-band noise to out of band. However, lower in-band amplitude results in a higher OOB gain that may lead to an unstable modulator.

According to Mason's rule, the NTF for conventional $\Sigma\Delta$ modulator as shown in Figure 2.10 is given by:

$$NTF_{conv} = \frac{1}{1 + H_{ana}} = \frac{1}{1 + LG}, \tag{2.14}$$

where LG denotes the loop gain of modulator and in this case, LG equals to H_{ana}.

Signal Transfer Function

Signal transfer function (STF), as suggested by its name, is the filter that the signal goes through and it is generally defined as the transfer function from modulator input to output. Apart from this overall STF, the signal transfer functions from modulator input to each internal node are critical as well, like the nodes at the output of each integrator especially the one following with the quantizer. Since we don't want any attenuation at signal, so the ideal STF has a flat 0 dB amplitude within the band of interest. Designers have to be very careful that for in-band STF, any deviations from 0 dB, no matter positive or negative deviation, will directly affect the achievable signal-to-noise-ration (SNR). The reason is, if the in-band STF is lower than 0 dB, the signal level will be attenuated, whereas if the in-band STF at internal nodes have more than 0 dB gain, the amplified signal is very

likely to saturate the next stage integrator or quantizer, which leads to a decreasing in dynamic range (DR) or maximum achievable SNR.

The STF for conventional $\Sigma\Delta$ modulator as shown in Figure 2.10 can be expressed as (2.15), where LG again represents the loop gain of modulator.

$$STF_{conv} = \frac{H_{ana}}{1 + H_{ana}} = \frac{H_{ana}}{1 + LG} \tag{2.15}$$

2.3.2 Jitter Effect in Continuous-Time Sigma Delta Modulator

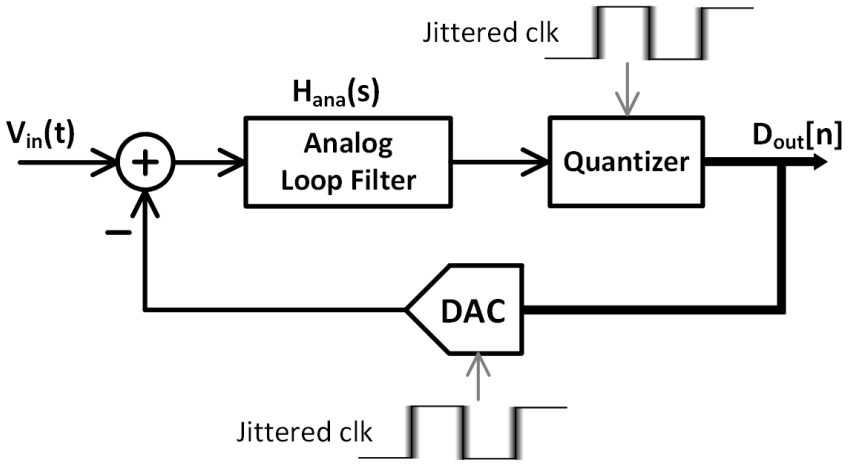


Figure 2.11: CT $\Sigma\Delta$ modulator linearized model.

In CT $\Sigma\Delta$ modulator, there are two blocks working with clock - quantizer and feedback DAC, which are shown in Figure 2.11. Fortunately, the only jitter noise coming from DAC is harmful to SNR. Consider the noise introduced by clock in quantizer, the transfer function it passing through is the noise transfer function, i.e. this noise will be shaped to out-of-band and does not affect the in-band noise level. However, the jitter from DAC is a different story. Unlike the noise from quantizer, the DAC clock jitter induced error is processed by signal transfer function, which means all the in-band noise components will remain filling the band-of-interest.

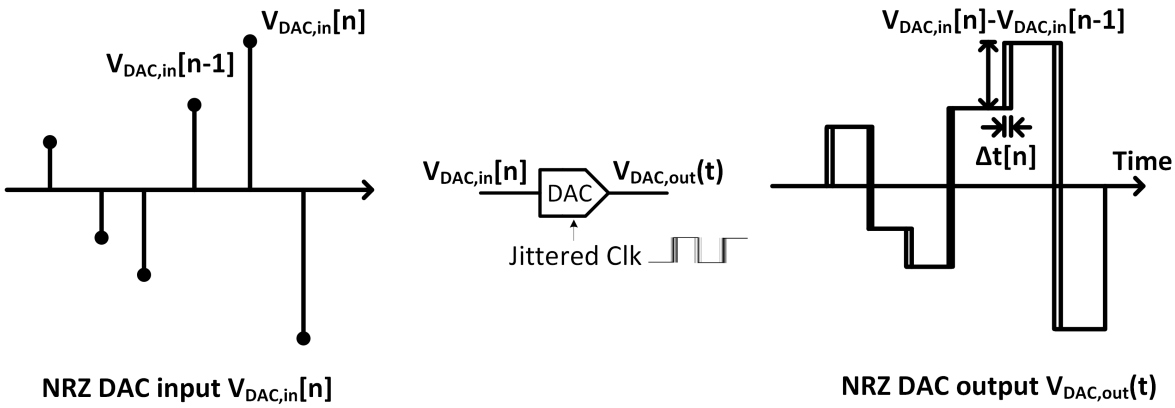


Figure 2.12: Time domain jitter effect.

Figure 2.12 [10] shows the NRZ DAC jitter effect on CT $\Sigma\Delta$ modulator in the time domain. Assume the DAC is working with a jittery clock, therefore the output signal time domain waveform does not have clocking edges as single straight lines. From the figure, jitter error can be expressed as:

$$J_e(t) = (\Delta t/T_s)(V_{DAC,in}[n] - V_{DAC,in}[n-1]), \tag{2.16}$$

where Δt denotes the aperture uncertainty of jittery clock and Ts is the clock sampling period.

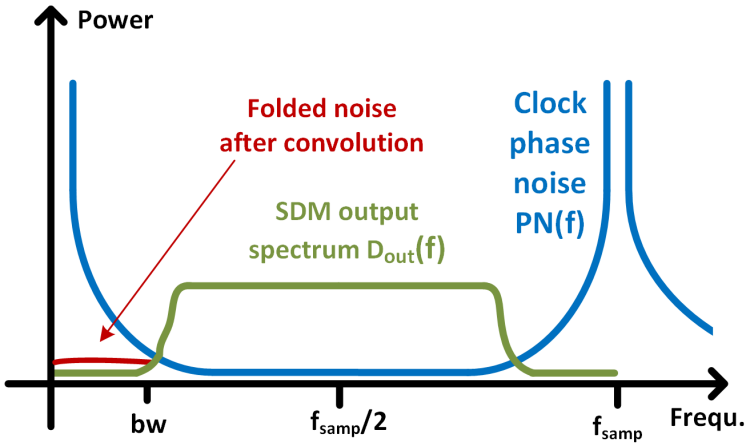


Figure 2.13: Frequency domain jitter effect.

Mapping the time domain equation into frequency domain:

$$J_e(f) = PN(f) * [(1 - z^{-1})V_{DAC,in}(f)]$$

(where $V_{DAC,in}(f)$ here and $D_{out}(f)$ in Figure 2.13 denote the same signal). Like what shown in Figure 2.13 [12], high out-of-band $\Sigma\Delta$ modulator output noise folds back to in-band after convolution with the phase noise (representation of jitter in frequency domain) centering at DAC clock frequency that eventually deteriorates the in-band SNR. The effect of $1 - z^{-1}$ is not shown in the plot for simplicity.

2.3.3 Literature Review on Continuous-Time Sigma Delta Modulator Jitter Effect

FIR Feedback DAC

Since the jitter error is directly proportional to the magnitude of each DAC input step ($V_{DAC,in}[n] - V_{DAC,in}[n-1]$), passing the signal through an FIR filter before it goes into DAC can effectively reduce the step size, which eventually results in lower jitter sensitivity, just like using multi-bit DACs. This effect can be best illustrated in the case where a single bit quantizer followed by a multiple-tap low-pass FIR filter, which is shown in Figure 2.14 [5]. In Figure 2.14, the 1-bit output of the CT $\Sigma\Delta$ modulator is filtered by an FIR filter $F(z)$, where the step size is successfully reduced before going into DAC [5].

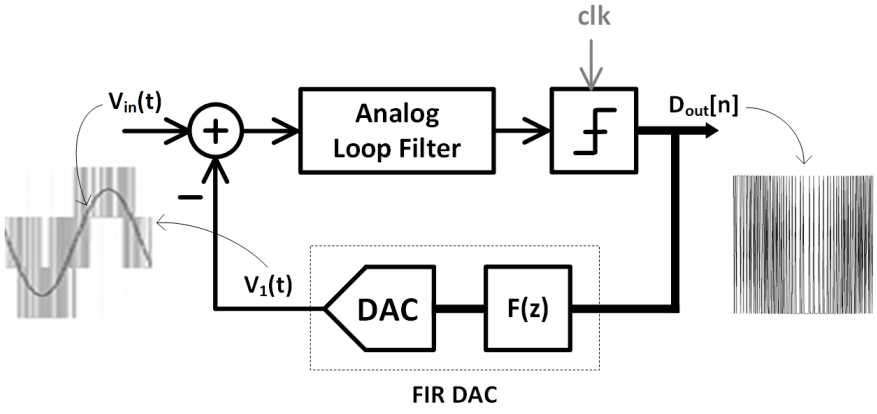


Figure 2.14: FIR DAC impact on CT $\Sigma\Delta$ modulator jitter sensitivity.

The main issue of having FIR filter in the loop is that it generates excess loop delay. The number of taps is directly associates with the number of delay cells, thus extra efforts are required otherwise the feedback system would be unstable. A typical way to stabilize the loop is by adding a fast path, but since the delay has to be minimized in fast path, thus it consumes more power.

NRZ vs RZ DACs

The major difference between Return-to-Zero (RZ) DAC and Non-Return-to-Zero (NRZ) DAC is that they have different pulse shape - RZ DAC has to return back to ground level at the second half period on each clock cycle, while NRZ simply does not. Since clock jitter is the clock edge deviation from the ideal transition point, thus having more transition unavoidably results in higher jitter sensitivity. Therefore, NRZ DACs are naturally more robust to jitter comparing with RZ DACs.

Although NRZ DAC is commonly used in CT $\Sigma\Delta$ modulator, it also has some disadvantages comparing with RZ DAC. NRZ DAC suffers from nonlinear transition error in practice because there is either a rising edge or a falling edge in each bit of the DAC waveform, thus the difference in rising time and falling time cannot compensate for each other within the same bit. While in RZ DAC, there are both rising and falling edges in one clock period, so the total error is almost zero overall [10].

Switched-capacitor Feedback DAC

Since feedback DAC pulse shape has a direct impact on jitter sensitivity, so except for NRZ and RZ, it is worthwhile to explore the other pulse shapes. The main idea is, as long as the variation of clock edges has less effect on the modulator performance, the pulse shape is beneficial to reduce jitter. Exponentially decaying pulse shape, for example, is such a good option. As shown in Figure 2.15, since most of the charges are already transferred before the clocking edge, thus jitter only affects very limited area as highlighted in blue.

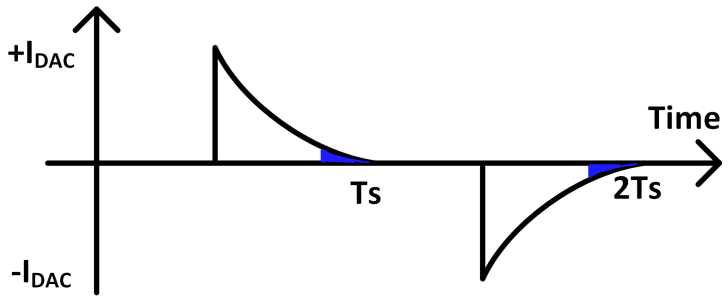


Figure 2.15: Exponentially decaying pulse shape impact on jitter sensitivity.

[6] claims that by using full clock period switched-capacitor-resistor (FSCR) feedback DAC, the SNDR only decreases by 2.3 dB when working with jittery clock at 1.0% of the clock period compared to the ideal clock case.

The drawback of employing switched-capacitor feedback DAC is the penalty of high power consumption. Compared to the often-used NRZ DAC pulse shape, the maximum current of switch-cap DAC can be five times of the NRZ case. Since the amplifier has to provide this considerable current, thus the requirement on its slew rate and gain-bandwidth product (GBW) is very stringent.

3. 4TH ORDER JITTER TOLERANT SIGMA DELTA MODULATOR SYSTEM LEVEL DESIGN

This chapter focuses on the system level design of a 4th order jitter tolerant $\Sigma\Delta$ modulator, which targeting at relaxing the requirements on blocks collaborating with ADCs like Phase Lock Loops (PLL) that generating clocks. First of all, the proposed jitter sensitivity reduction technique is discussed. The second section talks about the procedure of designing the proposed jitter tolerant $\Sigma\Delta$ modulator at a system perspective. The simulation results are posted in the end.

3.1 Jitter Sensitivity Reduction Technique

As we discussed earlier in section 2.3.2, it is the out-of-band noise that folds back to in-band after the convolution with clock phase noise. Therefore, if we can decrease the out-of-band noise, the jitter-induced noise floor will be reduced as well. Here we propose a method to lower the out-of-band noise and implement the idea with a fourth order hybrid $\Sigma\Delta$ modulator in system level.

The proposed hybrid $\Sigma\Delta$ modulator simplified conceptual block diagram is shown in Figure 3.1, where the conventional last stage integrator is split into one single-pole digital low-pass filter and one gain stage. The digital filter is placed at the output of quantizer in order to attenuate the high out-of-band noise. The loss of loop gain resulting from removing the last stage integrator is compensated by the extra gain stage (marked as "A" in Figure 3.1). The modulator output is taken from the digital filter output. The digital filter should have 0 dB gain in-band, so that the in-band signal remains the same, but with a -20 dB/dec roll-off out of band to suppress the out-of-band noise. Therefore, digital filter transfer function $H_{dig}(z)$ should have a shape as $\frac{1-\alpha}{1-\alpha z^{-1}}$ $(0 < \alpha < 1)$ to meet the requirements.

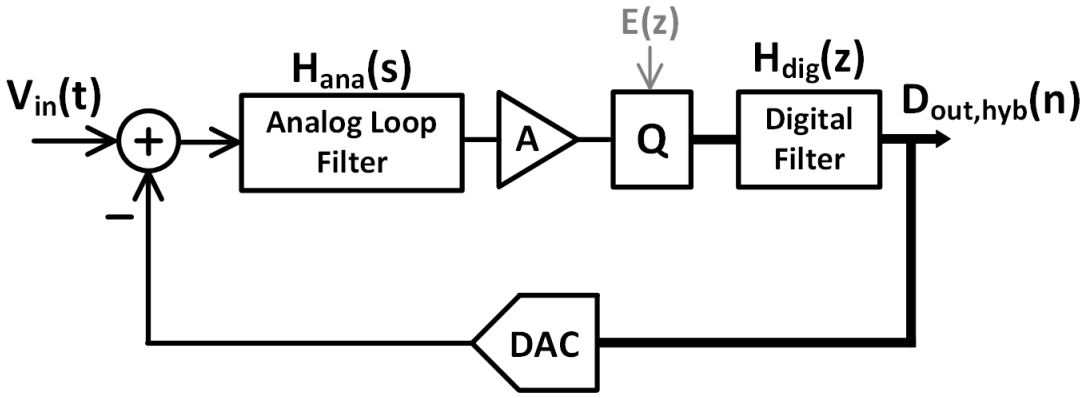


Figure 3.1: Proposed $\Sigma\Delta$ modulator conceptual system diagram.

The signal transfer function (STF), noise transfer function (NTF) and open loop gain (LG) of hybrid $\Sigma\Delta$ modulator can be expressed as:

$$STF = \frac{H_{ana}H_{dig}A}{1+LG} = STF_{conv} \tag{3.1}$$

$$NTF = \frac{H_{dig}}{1+LG} = H_{dig}NTF_{conv} \tag{3.2}$$

$$LG = H_{ana}H_{dig}A, \tag{3.3}$$

where LG is the system open-loop gain, H_{ana} and H_{dig} are the transfer functions of analog loop filter and digital filter, respectively. STF_{conv} and NTF_{conv} represent the conventional $\Sigma\Delta$ modulator signal and noise transfer functions where the output is taken directly at the quantizer output. Since the gain stage (A) taking care of the gain portion of the original integrator and the digital filter providing the single pole, thus ideally, the STF remains the same and one H_{dig} factor is multiplied to the conventional NTF.

From section 2.3.2, the jitter frequency domain equation can be derived as:

$$\begin{aligned} J_e(f) &= PN(f) * [D_{out,hyb}(z)(1-z^{-1})] \\ &= PN(f) * [(H_{dig}NTF_{conv}E + H_{dig}STF_{conv}V_{in})(1-z^{-1})] \\ &= PN(f) * [H_{dig}(z)D_{out,conv}(z)(1-z^{-1})] \end{aligned} \tag{3.4}$$

where $J_e(f)$ is the frequency domain jitter error, $PN(f)$ is clock phase noise centering around sampling frequency 640 MHz. From (3.4), it is clear that the digital filter directly shapes the out-of-band noise.

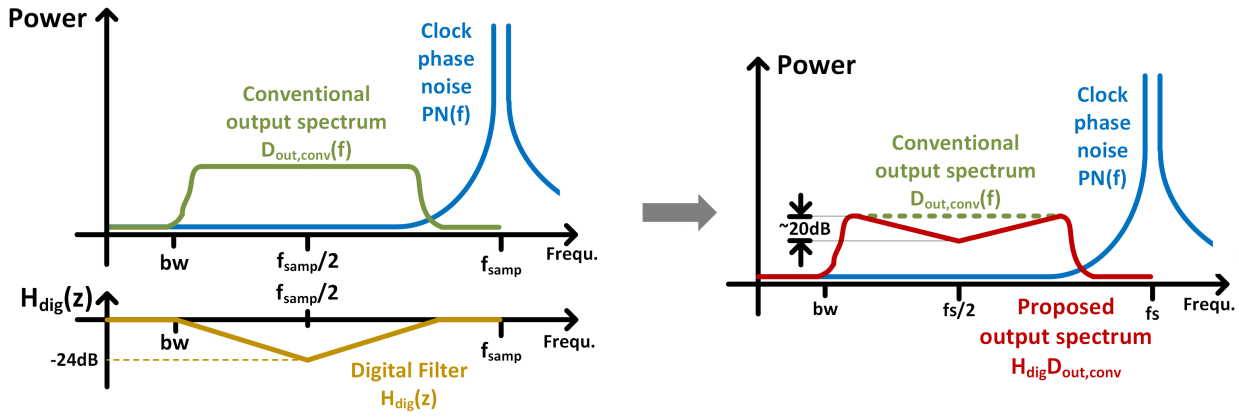


Figure 3.2: Frequency domain jitter sensitivity reduction.

Since H_{dig} is 0 dB within band of interest, STF equals to STF_{conv} in-band. For NTF, the in-band part remains the same as conventional case but out-of-band NTF is suppressed by digital filter at a slope of -20 dB/dec, which results in lower out-of-band noise thus less quantization noise folds back to signal bandwidth. This effect is clearly illustrated in Figure 3.2 [12] (the low frequency portion of phase noise is not shown in the figure for simplicity). On the left side of Figure 3.2, conventional $\Sigma\Delta$ modulator output spectrum and digital filter frequency response are shown separately. On the right plot, the curve with capital "M" shape represents the shaped quantization

noise at modulator output with digital filter. It is obvious that with the extra shaping, out-of-band noise is attenuated by around 20 dB at Nyquist rate compared with conventional case thus the ADC has better jitter tolerant.

3.2 System Architecture and Analysis

Table 3.1 lists the key system-level design specifications for the proposed $\Sigma\Delta$ modulator, which targeting at 11 bit Effective Number of Bits (ENOB) by implementing a fourth order analog filter at 20 MHz bandwidth.

Parameter	**Value**
Order	4
Bandwidth	20 MHz
Sampling frequency	640 MHz
Oversampling ratio	16
Quantizer level	4
Target ENOB	11 bit

Table 3.1: Key design specifications of proposed 4th order hybrid $\Sigma\Delta$ modulator.

3.2.1 NTF Realization

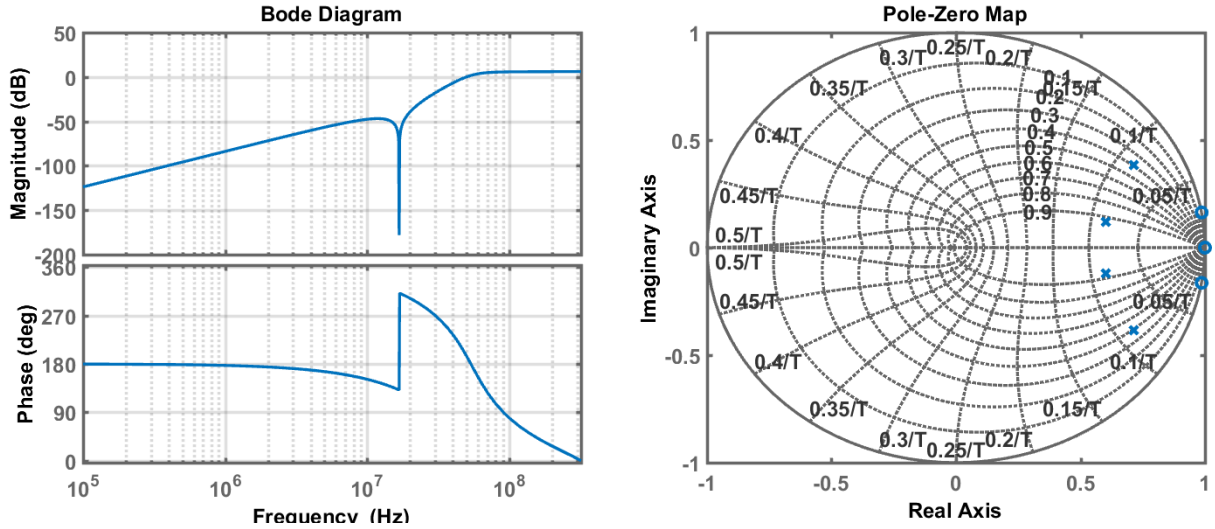
Generally, CT $\Sigma\Delta$ modulator design procedure starts with z domain transfer function, because many parameters like loop delays and sampling can be easily represented in discrete domain. Also, mapping from z domain to s domain by using impulse-invariant method is well developed in digital signal processing and there are lots of design tools available like the Delta-Sigma Toolbox in MATLAB [15].

A fourth order NTF with 16 over sampling ratio (OSR) is generated by using the aforemen-

tioned Delta Sigma Toolbox's 'synthesizeNTF' function. This discrete-time NTF is given by:

$$NTF(z) = \frac{(z-1)^2(z^2-1.973z+1)}{(z^2-1.201z+0.3753)(z^2-1.427z+0.657)} \tag{3.5}$$

The given NTF has a zero locating at DC and the rest two are a pair of complex conjugate zeros at 16.8 MHz. The bode plot and pole-zero map of this NTF is shown in Figure 3.3 (sampling frequency equals to 640 MHz).



(a) (b)

Figure 3.3: (a) NTF bode plot. (b) NTF pole zero map.

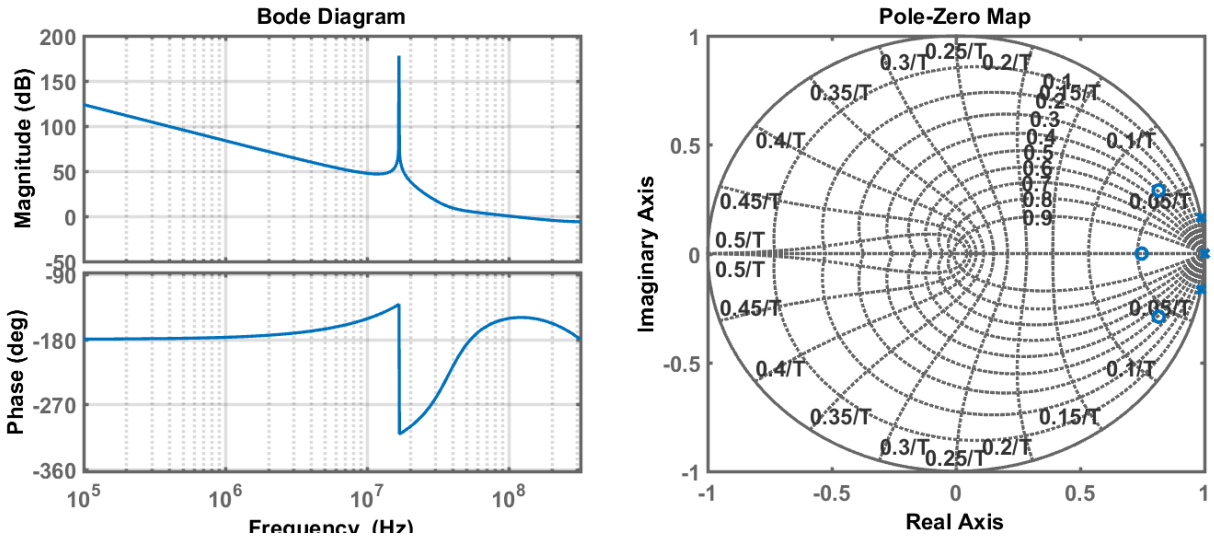
The system loop transfer function (LTF) can be calculated from NTF according to (3.6).

$$LTF(z) = \frac{1}{NTF(z)} - 1 \tag{3.6}$$

Thus LTF can be expressed as:

$$LTF(z) = \frac{1.3447(z-0.7473)(z^2-1.632z+0.7498)}{(z-1)^2(z^2-1.973z+1)} \tag{3.7}$$

LTF shares the same poles as NTF zeros - the complex conjugate poles locates at 16.8 MHz. LTF has one real zero at 29.7 MHz and a pair of complex conjugate zeros at 37.8 MHz. The bode plot and pole zero map of LTF are both presented in Figure 3.4.



(a) (b)

Figure 3.4: (a) LTF bode plot. (b) LTF pole zero map.

In order to move one continuous-time integrator to digital domain, before mapping LTF(z) into continuous-time, a $\frac{1-\alpha}{1-\alpha z^{-1}}$ $(0 < \alpha < 1)$ factor, as suggested earlier this chapter, has to be split from the origianl $LTF(z)$ and this part will be kept in discrete-domain. Therefore, firstly, $\frac{1}{1-z^{-1}}$ is factored out from $LTF(z)$, as illustrated in (3.8).

$$\begin{aligned} LTF(z) &= \frac{1.3447z^{-1}(1-0.7473z^{-1})(1-1.632z^{-1}+0.7498z^{-2})}{(1-z^{-1})^2(1-1.973z^{-1}+z^{-2})} \\ &= \frac{1}{1-z^{-1}} \frac{1.3447z^{-1}(1-0.7473z^{-1})(1-1.632z^{-1}+0.7498z^{-2})}{(1-z^{-1})(1-1.973z^{-1}+z^{-2})} \end{aligned} \tag{3.8}$$

The factor of $\frac{1}{1-z^{-1}}$ is approximately equal to $\frac{1}{1-\alpha z^{-1}}$ when α is close to 1 but smaller than 1. Since $\frac{1-\alpha}{1-\alpha z^{-1}}$ is the transfer function of a low-pass digital filter with 0 dB gain in band,

thus a $1-\alpha$ factor is multiplied and divided to have the transfer function mathematically remaining the same, as shown in (3.9).

$$\frac{1}{1-z^{-1}} \cong \frac{1-\alpha}{1-\alpha z^{-1}} \frac{1}{1-\alpha} \tag{3.9}$$

After plugging (3.9) into (3.8), the modified LTF for the proposed hybrid $\Sigma\Delta$ modulator is given by:

$$LTF_{proposed}(z) = \big[\frac{1}{1-\alpha} \frac{1.3447z^{-1}(1-0.7473z^{-1})(1-1.632z^{-1}+0.7498z^{-2})}{(1-z^{-1})(1-1.973z^{-1}+z^{-2})}\big]\big[\frac{1-\alpha}{1-\alpha z^{-1}}\big] \tag{3.10}$$

With the intention to compensate the excess loop delay [7], z^{-1} is taken out from the proposed LTF and the transfer function to be mapped to s domain is given by:

$$LTF_{ana}(z) = \frac{1}{1-\alpha} \frac{1.3447(1-0.7473z^{-1})(1-1.632z^{-1}+0.7498z^{-2})}{(1-z^{-1})(1-1.973z^{-1}+z^{-2})} \tag{3.11}$$

Discrete-time loop transfer function (3.11) is then converted into continuous-time by using MATLAB function 'd2c' with a method option of 'zoh' for assuming a NRZ DAC pulse shape [7]. The continuous-time equivalent of (3.11) can be written as:

$$LTF_{ana}(s) = \frac{1}{1-\alpha} \frac{1.3447(s+0.2586)(s^2+0.2555s+0.1154)}{s(s^2+0.02706)} \tag{3.12}$$

Take (3.12) into (3.10), the hybrid LTF can be expressed as:

$$LTF_{hyb} = \big[\frac{1}{1-\alpha} \frac{1.3447(s+0.2586)(s^2+0.2555s+0.1154)}{s(s^2+0.02706)}\big]\big[\frac{1-\alpha}{1-\alpha z^{-1}}\big] \tag{3.13}$$

Figure 3.5 presents the proposed hybrid $\Sigma\Delta$ modulator architecture and the coefficients are shown in Table 3.2. Unlike traditional fourth order CT $\Sigma\Delta$ modulator with four integrators, the proposed architecture only has three integrators and the last stage integrator is replaced by one gain stage and a digital filter. CRFB (Cascade of Resonators with Distributed Feedback) topology is adopt for robustness by using more hardware as four feedback DACs are required.

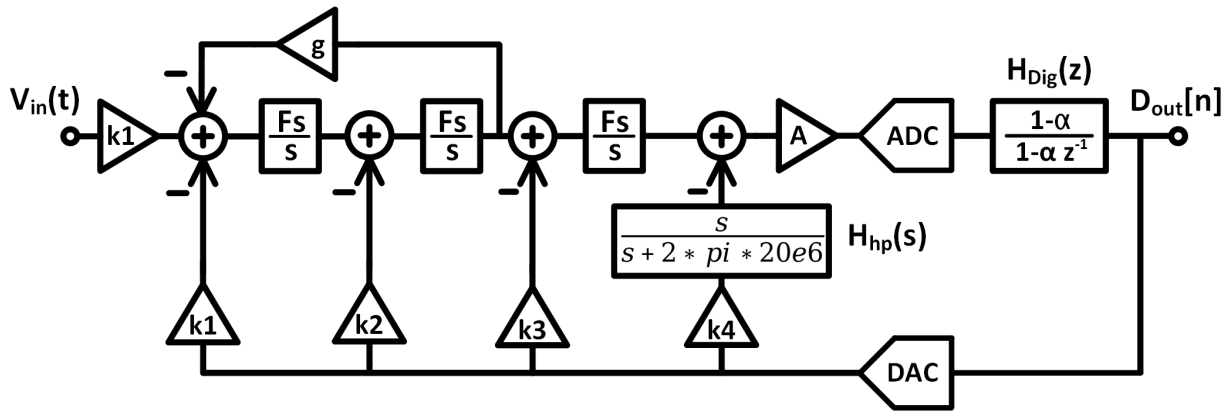


Figure 3.5: Proposed 4th order hybrid $\Sigma\Delta$ modulator.

Parameter	**Value**
k1	0.0401
k2	0.2838
k3	1.1
k4	1.45
g	0.0273
A	3.6
α	0.75 or 0.875

Table 3.2: Key system level coefficients of proposed 4th order hybrid $\Sigma\Delta$ modulator.

$DAC_1(k1)$ provides the main feedback signal. It controls the low frequency loop gain, thus it determines the low frequency noise level to the greatest extent compared to the other trajectories. The main DAC loop should target at high gain for achieving high SNR. The so-called fast-path is the loop where $DAC_4(k4)$ located and it exists for stability consideration. In order to better control the unity gain cross-over frequency, fast-path should have low but larger than 0 dB amplitude

at high frequency such that the loop can still maintain a decent phase margin in transistor level implementation with parasitics. Unlike the main loop, the fast-path should be designed with a focus on lower delay even at the expense of high power dissipation. The phantom zeros, generated by cascading feedback paths with different speeds, compensate the overall loop stability.

The loop with g coefficient generates a pair of complex conjugate poles at frequency slightly lower than signal bandwidth and it provides several dB SNR improvement compared with the case without resonator. According to Mason's rule, the loop gain of the fast-path appears at the numerator of STF from input to each integrator output, thus a high-pass filter is added at fast-path in order to limit the gain of these internal STFs within band-of-interest. With the effect of high-pass filter, the low frequency fast-path loop gain is attenuated and the signal swing at internal nodes wouldn't exceed full-scale amplitude. This first order high-pass filter should be implemented with passive components.

3.2.2 Architecture Analysis

This section presents the system level simulation results of the proposed fourth order hybrid $\Sigma\Delta$ modulator (Figure 3.5) in Simulink with ideal blocks.

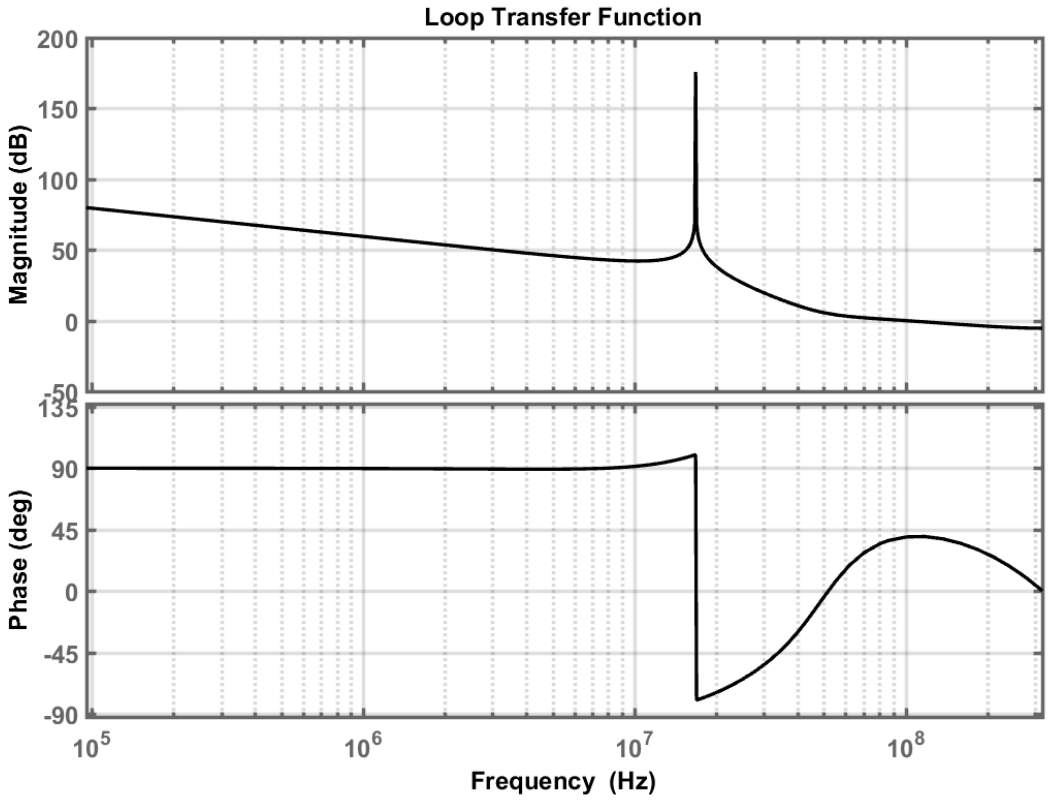


Figure 3.6: Loop transfer function of proposed 4th order hybrid $\Sigma\Delta$ modulator.

Figure 3.6 shows the open-loop bode plot of the proposed architecture. A pair of complex conjugate poles locate at 16.8 MHz. The gain margin is -4.2 dB and the phase margin is 44 degrees. Three continuous-time integrators in addition to one gain stage provides around 42 dB loop gain up to 20 MHz bandwidth.

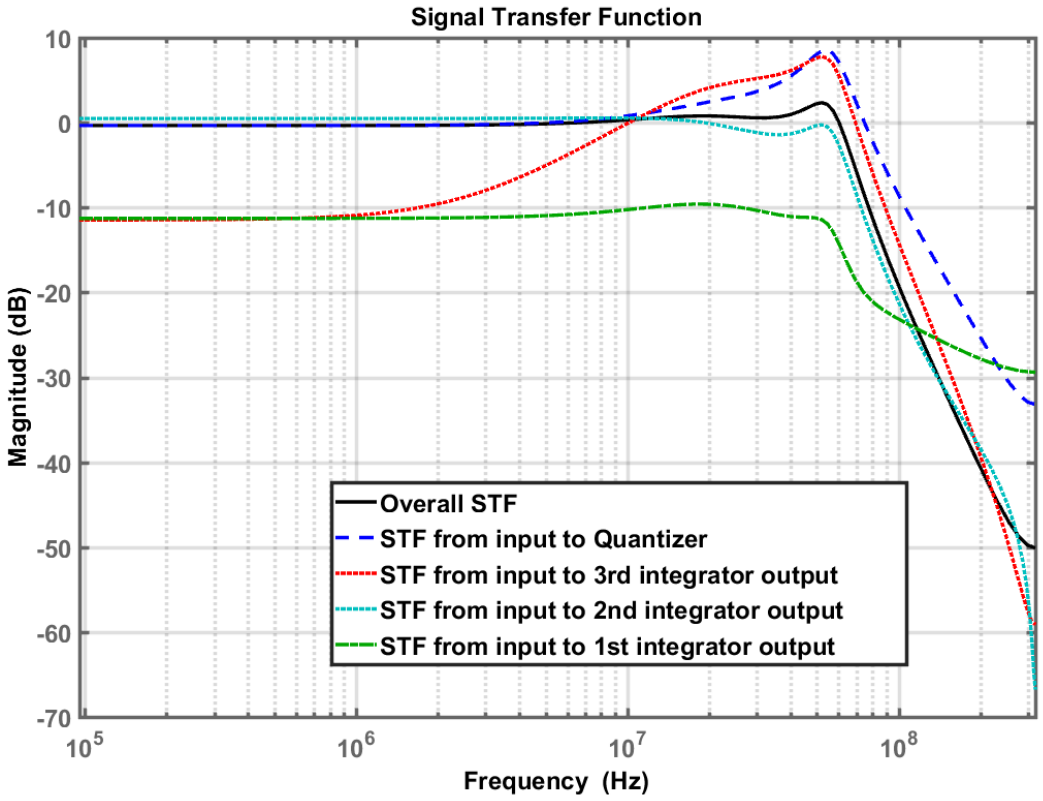


Figure 3.7: Signal transfer function of proposed 4th order hybrid $\Sigma\Delta$ modulator.

Signal transfer functions at internal nodes are shown in Figure 3.7. The in-band amplitude of STF at the output of third integrator is attenuated by high pass filter at the fast path, otherwise it has a very undesirable constant gain larger than 0 dB at low frequency. The overall STFs have a maximum of 4.4 dB within band of interest. All STF curves have out-of-band peaking which resulting from insufficient phase margin around peaking area. The solution to further attenuate the in-band STF level is discussed in Chapter 4.

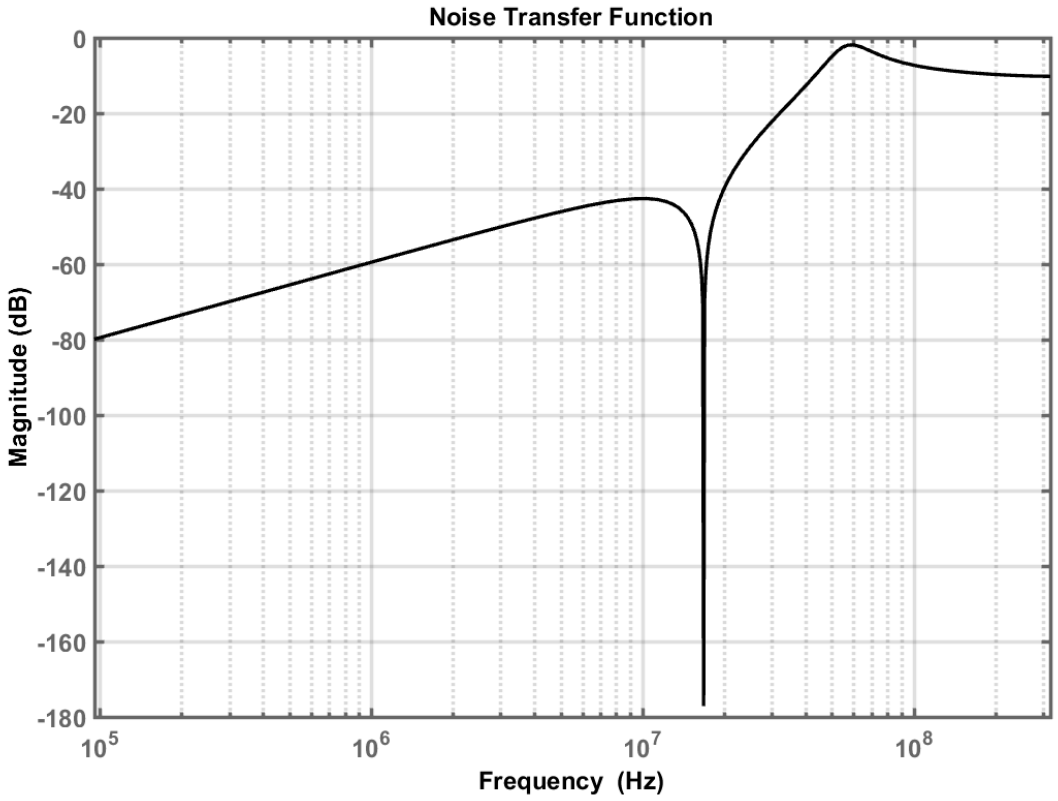


Figure 3.8: Noise transfer function of proposed 4th order hybrid $\Sigma\Delta$ modulator.

Figure 3.8 shows the noise transfer function of the proposed jitter tolerant $\Sigma\Delta$ modulator. The NTF brings about -42 dB quantization noise attenuation at signal bandwidth. The out-of-band noise is shaped by the low-pass digital filter to -10 dB at Nyquist frequency.

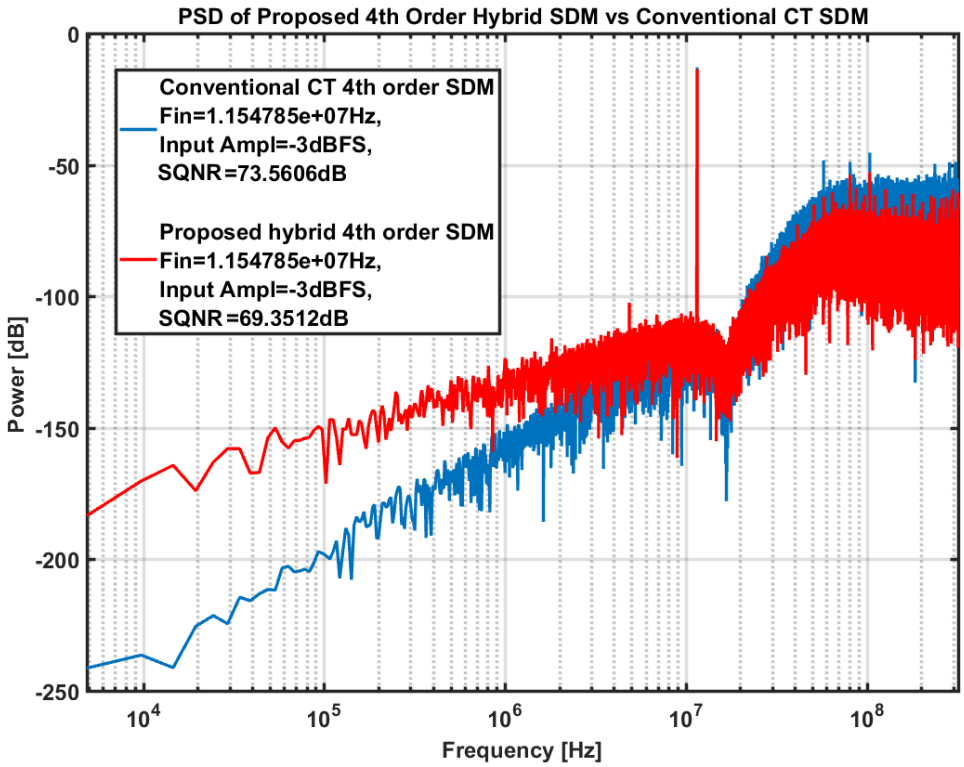


Figure 3.9: Power spectral density of the conventional CT and proposed hybrid 4th order $\Sigma\Delta$ modulator in Simulink.

Figure 3.9 presents the power spectral density of the proposed system level hybrid and conventional CT 4th order $\Sigma\Delta$ modulator. The proposed ADC achieves 69.3512 dB with amplitude of -3 dBFS sinusoidal input at 11.55 MHz. The out-of-band noise level is around -65 dB, which is more than 10 dB lower compared with the conventional case at Nyquist rate.

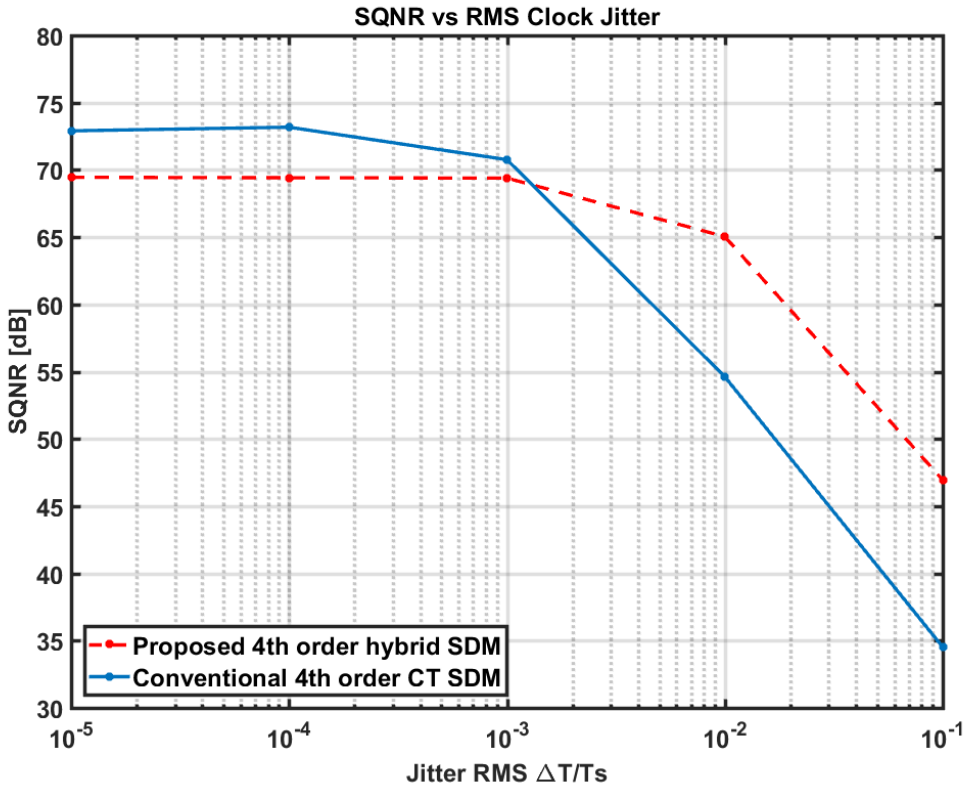


Figure 3.10: SQNR for of the conventional CT and proposed hybrid 4th order $\Sigma\Delta$ modulator at different jitter RMS.

The jitter performance comparison between of the proposed topology and the conventional CT $\Sigma\Delta$ modulator is shown in Figure 3.10. The additive jitter error model with NRZ DAC posted in [13] is used for the jitter simulation. The input signal is at 11.25 MHz with the amplitude of -3 dBFS. The proposed topology SQNR outweighs the conventional 4th order CT $\Sigma\Delta$ modulator with the same number of quantizer level by almost 12 dB at 10% clock period RMS jittery clock. From Figure 3.11, the SQNR of proposed topology almost remains the same with the variation of input signal frequency.

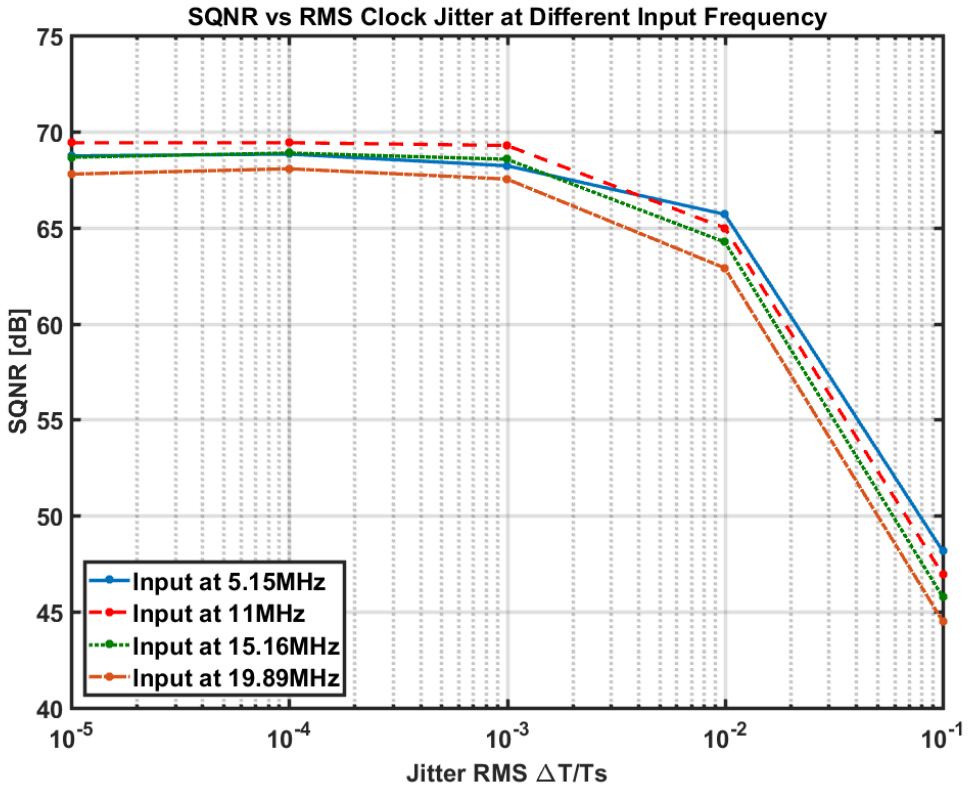


Figure 3.11: SQNR vs. jitter RMS for proposed hybrid 4th order ΣΔ modulator at different input frequency.

3.3 System Level Simulation Results

Since in this project, the entire system level topology is implemented with ideal macro-models, so only simulation results are posted in this chapter. Details on how to implement the loop filter is discussed in Chapter 4.1.3.

The schematic of proposed hybrid ΣΔ modulator loop filter with CRFB topology is shown in figure 3.12. The component values for proposed topology can be found in Table 3.3. The entire ΣΔ modulator is implemented with Verlog-A model in Cadence. The ideal OpAmps are set to have a DC gain of 40 dB and the dominant pole around 20 MHz. All DACs are implemented with NRZ pulse shape. The full scale input range is 1.6Vppd at 1.2V supply.

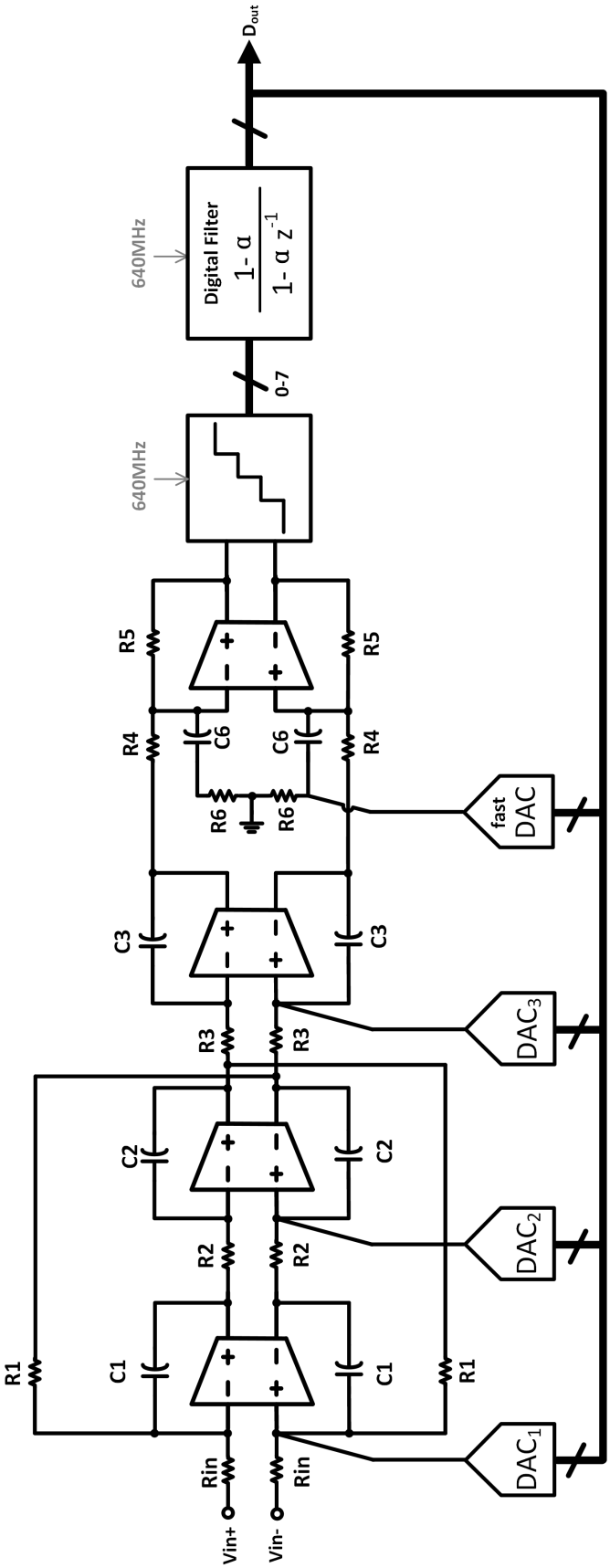


Figure 3.12: Proposed 4th order jitter tolerant hybrid $\Sigma\Delta$ modulator schematic.

Parameter	**Value**
Rin	800 Ω
R1	1975 Ω
C1	28.98 pF
R2	6 kΩ
C2	260.4 fF
R3	6 kΩ
C2	260.4 fF
R4	1667 Ω
R5	6 kΩ
C_{hp}	7.96 pF
R_{hp}	1 kΩ

Table 3.3: Component values of proposed 4th order hybrid ΣΔ modulator.

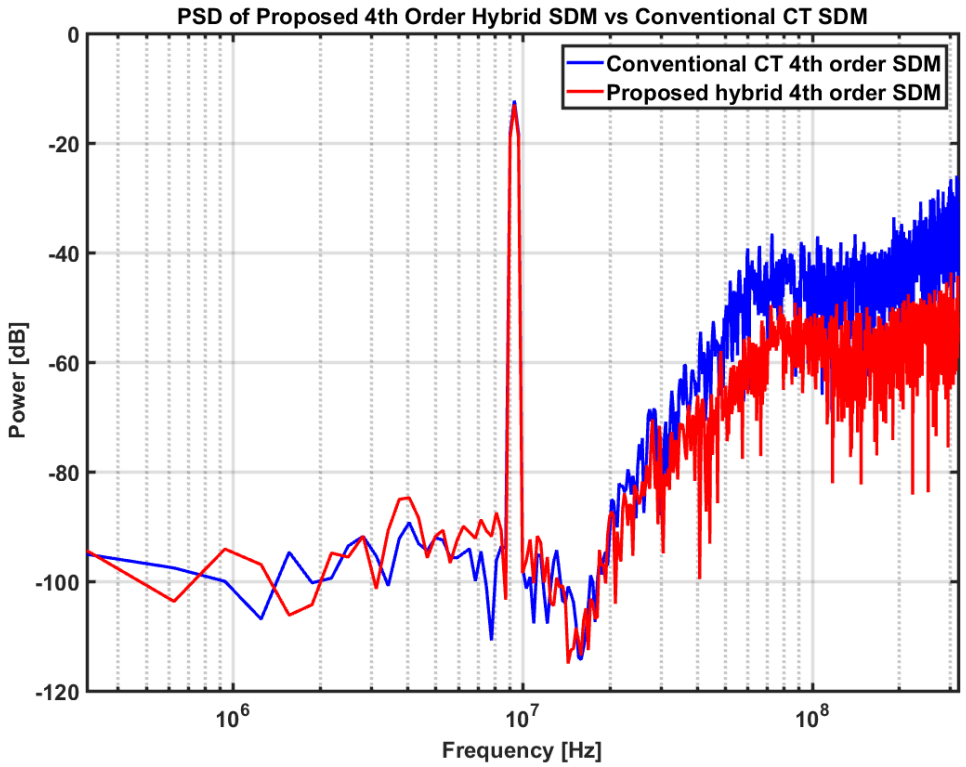


Figure 3.13: Power spectral density of the proposed hybrid and conventional CT 4th order $\Sigma\Delta$ modulator.

The power spectral density of proposed hybrid $\Sigma\Delta$ modulator and the conventional 4th order CT $\Sigma\Delta$ modulator in Cadence are shown in Figure 3.13 together. The proposed out-of-band noise level is around 20 dB lower than the conventional one at Nyquist rate. The hybrid $\Sigma\Delta$ modulator achieves 65.19 dB SQNR at 9.375 MHz sinusoidal input with -3 dBFS amplitude.

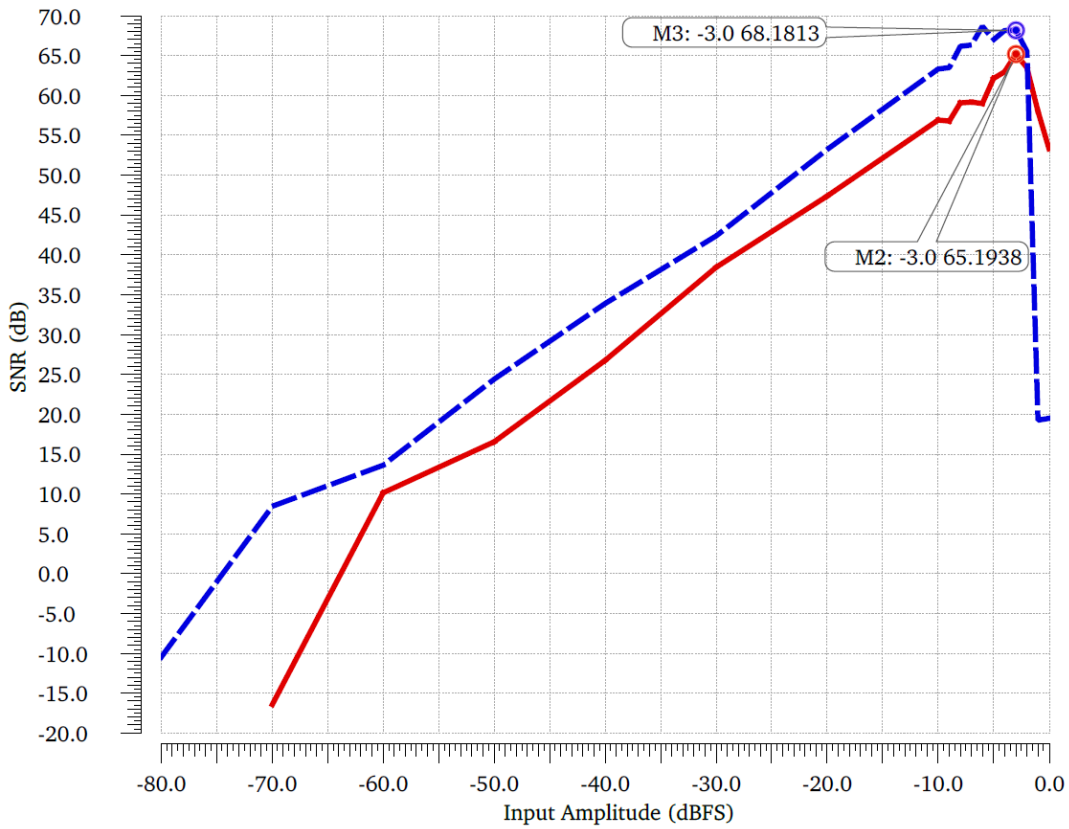


Figure 3.14: SNR vs input sinewave amplitude when α=0.75 (solid) and α=0.875 (dashed).

The plot of SNR vs. sinusoidal input signal amplitude in a unit of decibels relative to full scale is shown in Figure 3.14 at α is chosen as 0.75 and 0.875. The maximum achievable SNR is 65.1938 dB at α equals to 0.75 when input amplitude is -3 dBFS and the dynamic range is around 64 dB. In the case when α is 0.875, where the digital filter is a better representation of a continuous-time integrator, the maximum SNR is 68.1813 dB at -3 dBFS. Although the maximum achievable SNR increased, the SNR at -1 and 0 dBFS is worse than before. This is due to the fact that increasing α means raising the gain provided by the compensation gain stage as well, thus the signal swing at internal nodes increases and eventually saturates the quantizer at a lower input amplitude. The target of 11 bit ENOB is met at the case of α equaling to 0.875.

4.1 System Architecture and Analysis

The key system specifications of proposed third order hybrid $\Sigma\Delta$ modulator can be found in Table 4.1.

Parameter	**Value**
Order	3
Bandwidth	20 MHz
Sampling frequency	640 MHz
Oversampling ratio	16
Quantizer level	8
Target ENOB	11 bit

Table 4.1: Key system specifications of proposed 3rd order hybrid $\Sigma\Delta$ modulator.

Follow the similar procedure as described in Chapter 3, the z-domain loop transfer function and the corresponding hybrid loop transfer function to be implemented are given by:

$$LTF(z) = \frac{1.753(z^2 - 1.304z + 0.488)}{(z-1)(z^2 - 1.977z + 1)} \tag{4.1}$$

$$LTF_{hyb} = \Big[\frac{1}{1-\alpha}\frac{1.753(s^2 + 0.25932s + 0.1844)}{s^2 + 0.02706}\Big]\Big[\frac{1-\alpha}{1-\alpha z^{-1}}\Big] \tag{4.2}$$

4.1.1 Proposed Architecture

The proposed third order jitter tolerant hybrid $\Sigma\Delta$ modulator diagram is shown in Figure 4.1. Unlike the CRFB (Cascade of Resonators with Distributed Feedback) structure posed in Chapter

3, this topology is CRFF-B structure, a hybrid of CRFB and CRFF (Cascade of Resonators with Feed-Forward Summation) topology [10], which takes the advantage of both feedforward and feedback structures. Except for the obvious changes in the order number and structure, the other major differences between this design and the previous one are the anti-aliasing filter, digital filter sampling frequency. The key coefficients of proposed 3rd order hybrid $\Sigma\Delta$ modulator is listed in Table 4.2. These coefficients are first synthesized in the same way as described in Chapter 3 but with dynamic scaling [10] as well as coefficient sweeping to get the best SNR, so the modulator does not have the exact transfer function as suggested by (4.2) but it originates from (4.2).

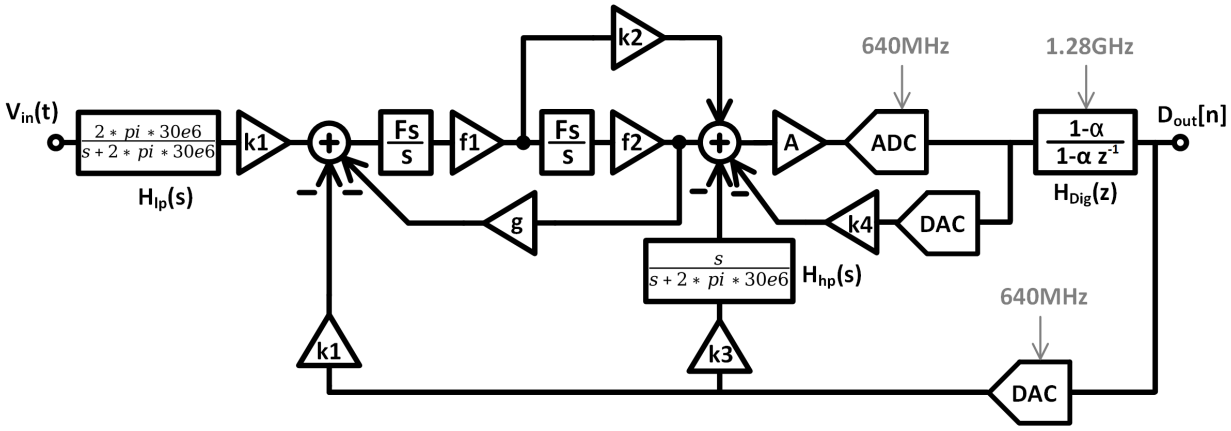


Figure 4.1: Proposed 3rd order hybrid $\Sigma\Delta$ modulator block diagram.

Parameter	**Value**
k1	0.9877
k2	1
k3	1.21
k4	0.0138
g	0.0210
A	7.2727
f1	1.1
f2	0.2857
α	0.875

Table 4.2: Key system level coefficients of proposed 3rd order hybrid $\Sigma\Delta$ modulator.

The main reason why feed-forward topology outweighs the feed-back as adopted in previous fourth order design comes from the noise consideration. In feedback topology, according to Mason's rule, transfer function from input to the output of first integrator has a term of the product of direct paths and their non-touching loops, thus the output swing is inherently large, which means that the gain of integrator at signal bandwidth cannot be scaled up. This is problematic because the gain of the first stage has to be at least larger than 10 dB at signal bandwidth, such that the noise from subsequent stages will be suppressed by this gain. The disadvantage of using pure feed-forward topology is that whatever out-of-band blockers will pass through the analog filter without much shaping, which eventually appearing at the input of quantizer that may saturate the quantizer or even undermining the system. Therefore, a topology with mixture of feedforward and feedback structures is employed in this project.

To alleviate the out-of-band blocker problem, one anti-aliasing filter, $H_{lp}(s)$, is added prior to the whole modulator. This low-pass filter has a single-pole and will be implemented passively. By adding this filter, out-of-band blocker will be firstly shaped before entering the modulator.

Another important difference compared to the previous design is that in this case, digital filter is sampled at twice of the sampling frequency. With doubled sampling frequency, the -20dB/dec slope of digital filter is now extended to f_s instead of $f_s/2$ in previous case. Therefore, the out-of-band noise level is further attenuated and the better jitter performance can be obtained. This concept is clearly illustrated in Figure 4.2.

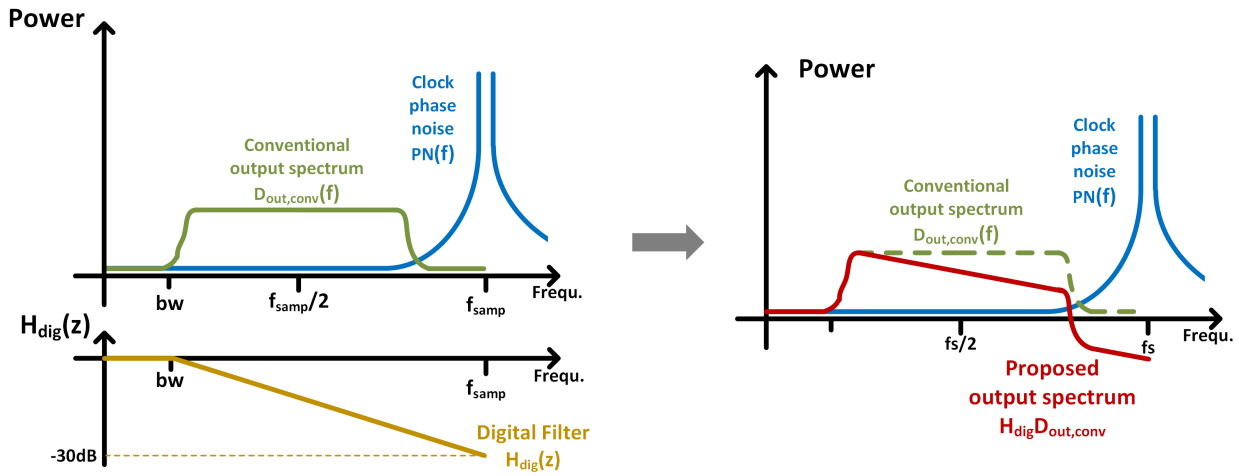


Figure 4.2: Improved jitter effect reduction technique.

The digital filter α factor is chosen to be 0.875. As we discussed before, since the digital filter is part of the continuous time integrator in conventional topology, thus the nearer the pole to origin, the more similar the digital filter to integrator, i.e the α factor should be designed to be smaller than 1 but close to 1. In addition, the digital filter will be implemented with IIR filter in a closed-loop feedback and the multiplication and division of numbers as a multiple of two can be done easily by shifting to the left or right in digital world. Therefore, considering the circuit complexity and accuracy, α equals to 0.875 is picked.

4.1.2 Architecture Analysis

In this section, the simulation results of the proposed hybrid 3rd order $\Sigma\Delta$ modulator as shown in Figure 4.1 with ideal blocks in Simulink are presented.

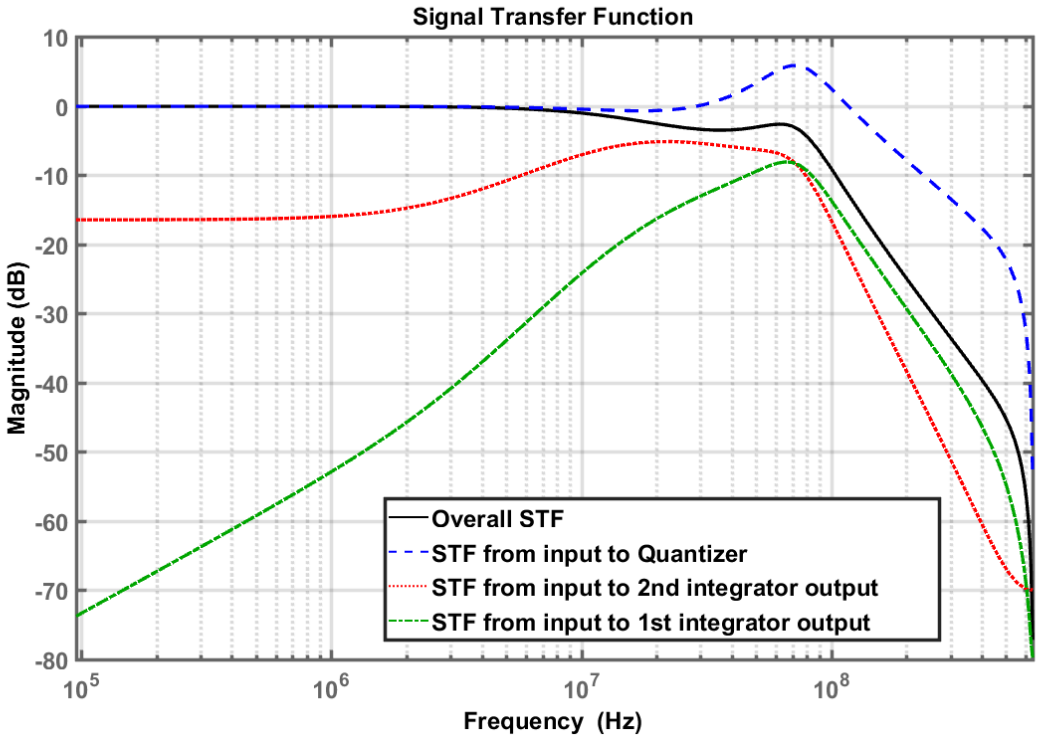


Figure 4.3: Signal transfer function of the proposed 3rd order hybrid $\Sigma\Delta$ modulator.

Figure 4.3 shows the signal transfer functions from modulator input to each internal nodes of the proposed hybrid $\Sigma\Delta$ ADC. The STF in-band amplitude is flat around 0 dB as expected and the out-of-band peaking level is at an acceptable level around 6 dB, which is a benefit of having low-pass filter in front of the modulator.

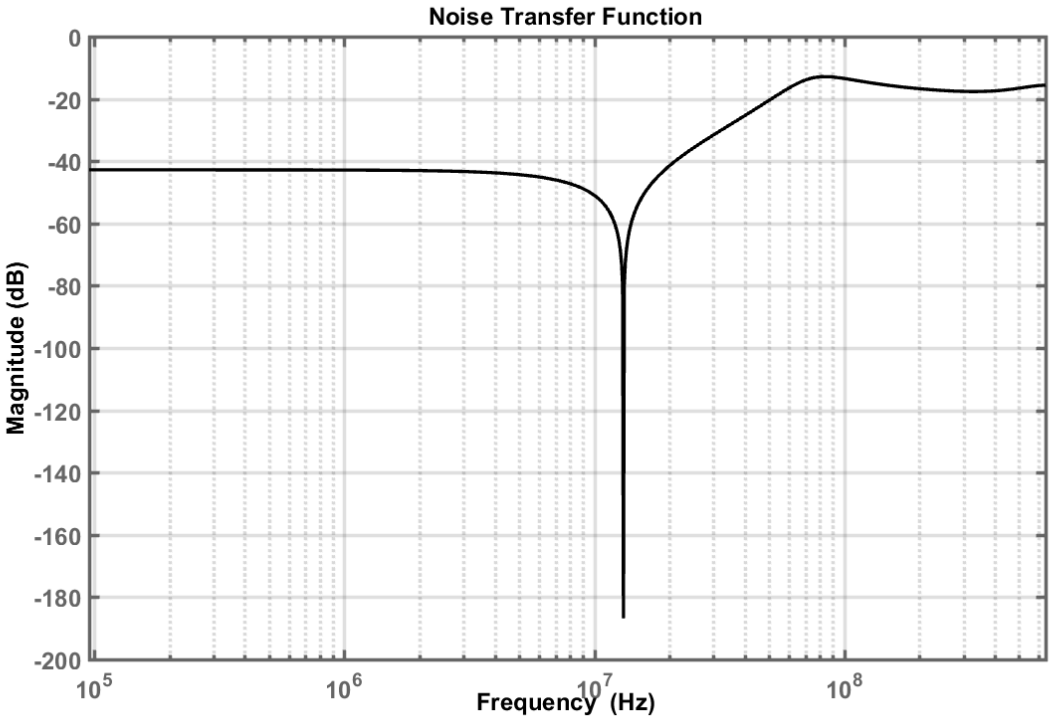


Figure 4.4: Noise transfer function of the proposed 3rd order hybrid $\Sigma\Delta$ modulator.

The modulator noise transfer function is shown in Figure 4.4. The out-of-band noise NTF amplitude is lower than 0 dB all the time, which means that the noise is successfully attenuated. The notch at 13.11 MHz is generated by the complex conjugate NTF zeros. The quantization noise suppression level at low frequency is -42.8 dB and thanks to the complex conjugate zeros, the noise attenuation at 20 MHz bandwidth is -41.5 dB.

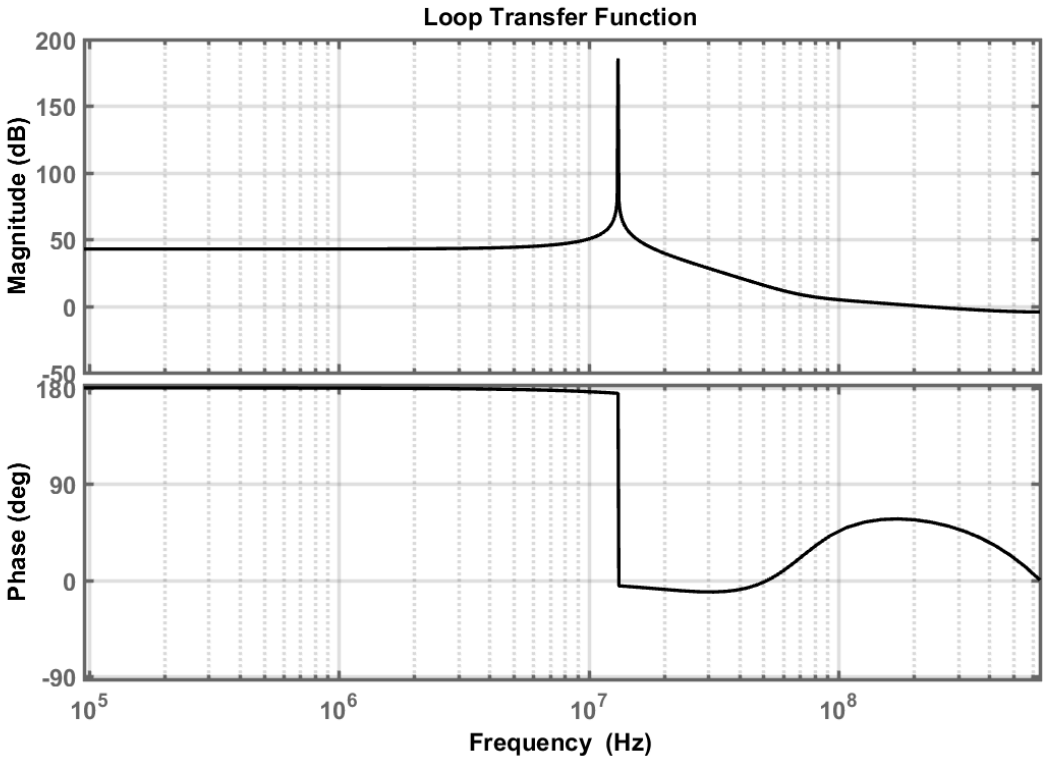


Figure 4.5: Loop transfer function of the proposed 3rd order hybrid $\Sigma\Delta$ modulator.

The Bode plot of loop transfer function is presented in Figure 4.5. Since LTF poles are NTF zeros, the NTF complex conjugate zeros generate a large LTF peaking at the same frequency. Phase margin is 56.1 degrees which is adequate for a stable system.

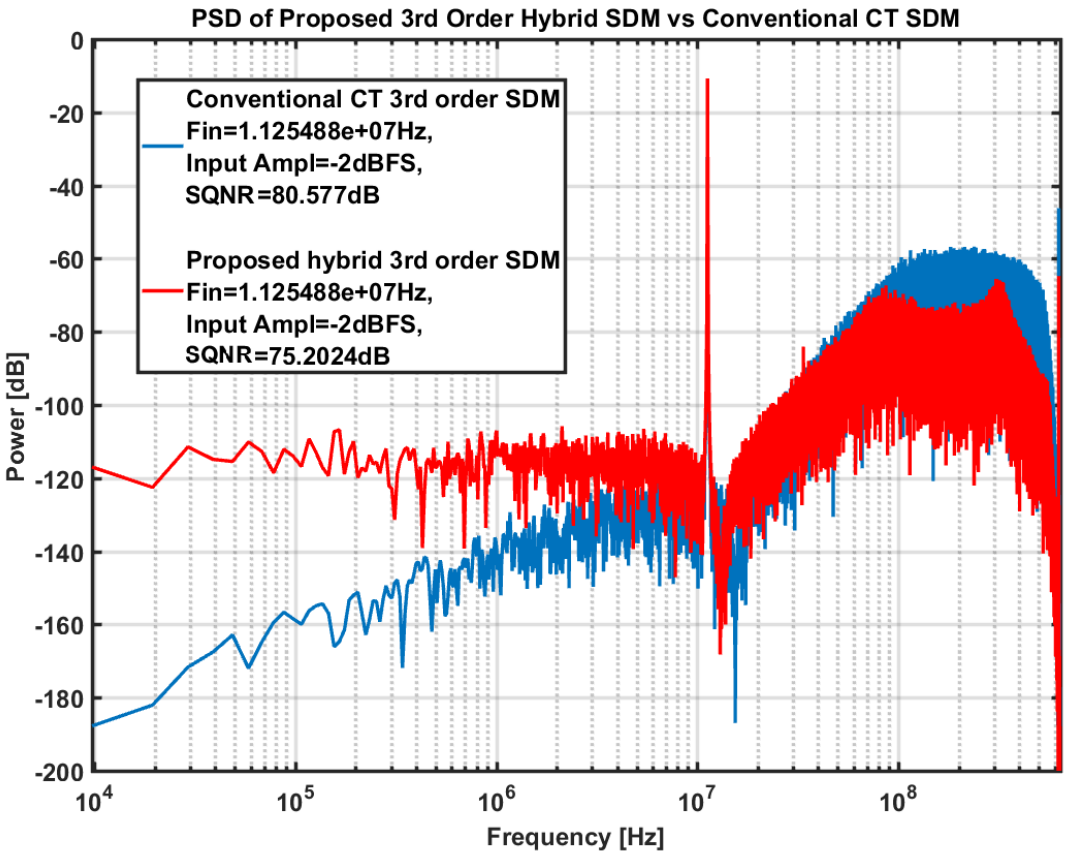


Figure 4.6: Power spectral density of the conventional CT and proposed hybrid 3rd order $\Sigma\Delta$ modulator in Simulink.

Figure 4.6 posts the power spectral density of the proposed system level hybrid and conventional CT $\Sigma\Delta$ modulator. The ADC achieves 75.2024 dB with -2 dBFS input amplitude at 11.25 MHz. The out-of-band noise level is around -70 dB. Obviously, compared with the conventional case, although SQNR is degraded, the out-of-band noise level is effectively attenuated as expected.

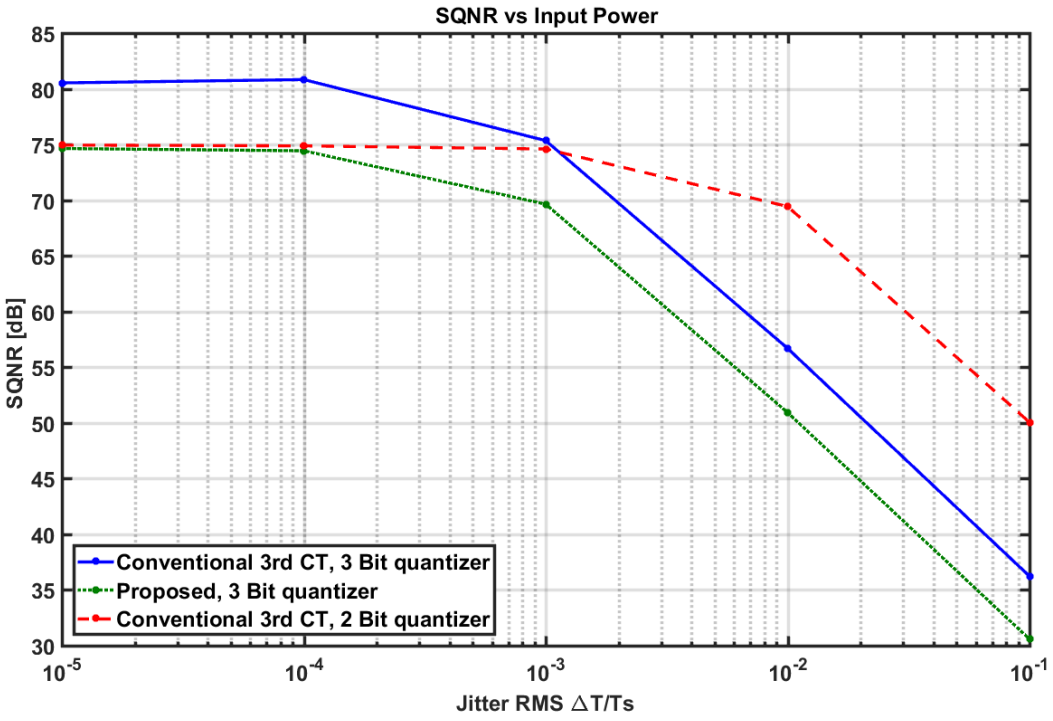


Figure 4.7: SQNR for of the conventional CT and proposed hybrid 3rd order $\Sigma\Delta$ modulator at different jitter RMS.

Figure 4.7 shows the SQNR vs input signal power at jittery clock with different jitter RMS values. Comparing to the conventional third order $\Sigma\Delta$ modulator with 3-bit quantizer, proposed topology achieves 14 dB better SQNR at 10% clock period RMS jittery clock. Conventional third order CT $\Sigma\Delta$ modulator with 2-bit quantizer, which provides the same amount of SQNR as proposed topology at low clock jitter, has a SQNR of almost 20 dB lower than the proposed hybrid $\Sigma\Delta$ modulator at 10% clock period RMS jittery clock. All three $\Sigma\Delta$ modulators share the same loop transfer function as (4.1) to guarantee a fair comparison.

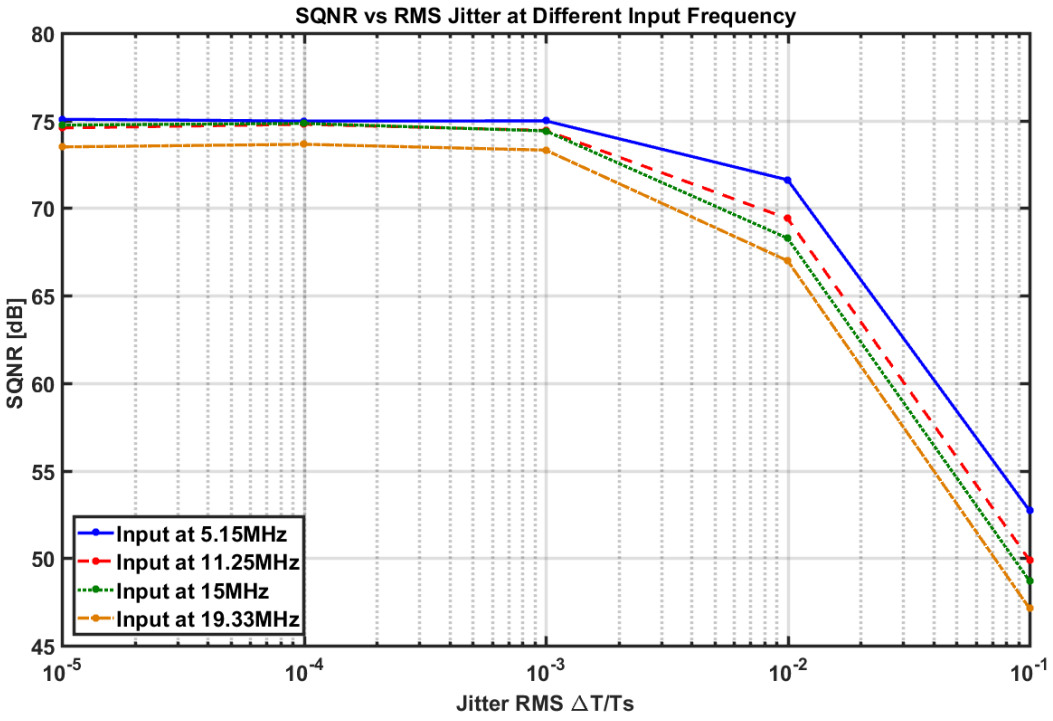


Figure 4.8: SQNR vs. jitter RMS for proposed hybrid 3rd order $\Sigma\Delta$ modulator at different input frequency.

Figure 4.8 presents the simulation result of SQNR vs RMS jitter at different input sinewave frequency of the proposed topology. The simulation results shows that the jitter tolerant ability of proposed $\Sigma\Delta$ modulator is preserved with the variation of input frequency.

4.1.3 Loop Filter Architecture

This section focuses on the way to implement analog loop filter from Simulink system level block diagrams to circuit level. The loop filter architecture and OpAmp design details are discussed thoroughly in this and the following sections.

The analog loop filter can be decomposed into two parts - a biquad filter and a summing amplifier.

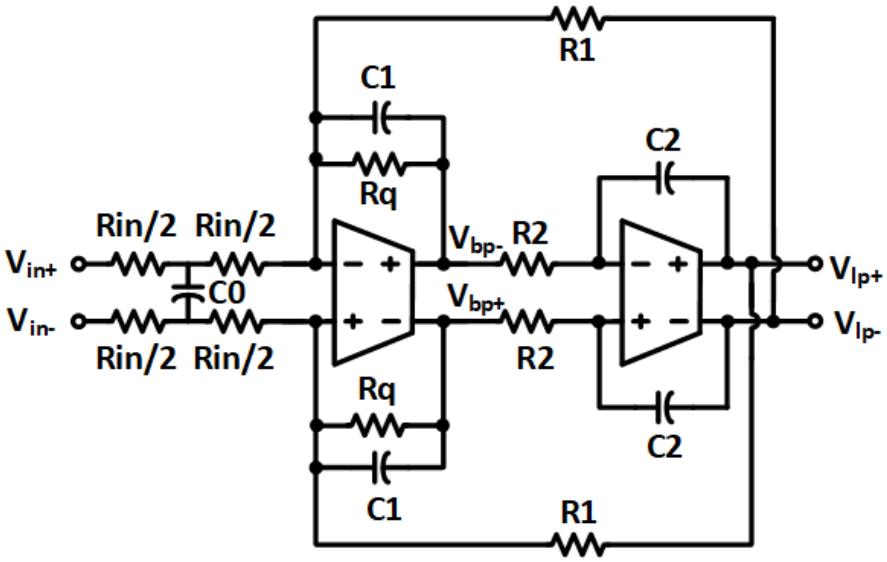


Figure 4.9: Biquad filter with front low-pass filter.

Figure 4.9 shows the differential biquad filter implemented in proposed hybrid $\Sigma\Delta$ modulator. The transfer function from biquad input to low-pass output node is given by (not considering the front low pass filter for now):

$$H_{lp}(s) = \frac{\frac{1}{R_{in}C_1R_2C_2}}{s^2 + s\frac{1}{R_qC_1} + \frac{1}{R_1C_1R_2C_2}} \tag{4.3}$$

Thus, comparing to the typical biquad transfer function, the resonant frequency ω_0, quality factor Q and DC gain A_{DC} can be computed as:

$$\omega_0^2 = \frac{1}{R_1C_1R_2C_2} \tag{4.4}$$

$$Q = \frac{R_q}{\sqrt{R_1R_2}}\sqrt{\frac{C_1}{C_2}} \tag{4.5}$$

$$A_{DC} = \frac{R_1}{R_{in}} \tag{4.6}$$

The component parameters can be calculated by using these equations. The low pass filter $R_{in}/2$ and C_0 product is chosen to be around the reciprocal of $2\pi * 30MHz$. The key parameters are listed in Table 4.3. The integrator coefficients do not match exactly with the system level design as shown in previous sections in order to accommodate the transistor level amplifiers that discussed in Chapter 4.1.5.

Parameter	Value
Rin	800 Ω
C0	13.263 pF
R1	6.021 kΩ
C1	4.494 pF
R2	6 kΩ
C2	364.6 fF
Rq	18.06 kΩ

Table 4.3: Component values of biquad filter.

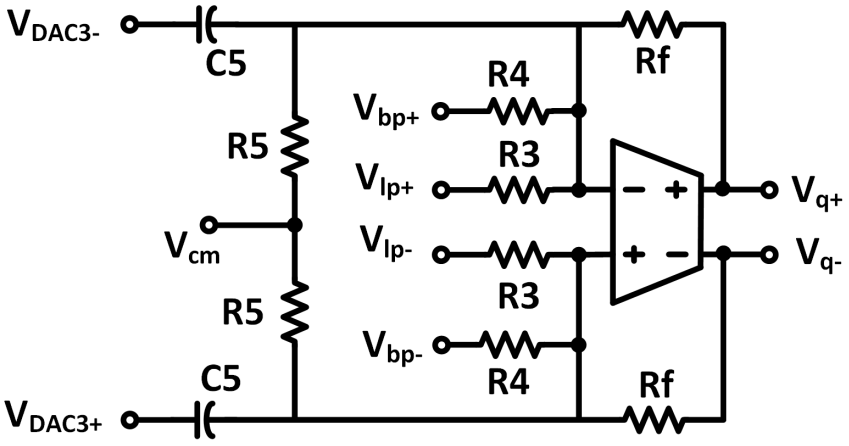


Figure 4.10: Gain stage and the passive high-pass filter.

Figure 4.10 shows the schematic of the last summing stage. The resistor ratios, $\frac{R_f}{R_3}$ and $\frac{R_f}{R_4}$, determine the gain and feedforward coefficient, separately. The high-pass filter has a corner frequency of 30 MHz as shown in Figure 4.1, thus the R_5C_5 product is close to the reciprocal of $2\pi * 30MHz$. The key component values can be found in Table 4.4. Likewise, the gain and coefficients are not exactly as system level design.

Parameter	Value
R3	8 kΩ
R4	3.24 kΩ
Rf	58.18 kΩ
R5	500 Ω
C5	10.62 pF

Table 4.4: Component values of summing stage.

4.1.4 OpAmp Design Considerations

Gain

For single loop $\Sigma\Delta$ modulators, [9] suggests that when OpAmp has infinite bandwidth, as long as the gain is comparable to the value of OSR, the noise floor remains around the ideal noise shaping level, i.e finite OpAmp gain does not introduce any extra noise. Here in this design, the OSR equals to 16, thus the minimal requirement of low frequency gain is around 25 dB and it is not difficult to meet.

GBW

OpAmp GBW is defined as g_m/C_L in the unit of rad/s and it is often quantified with respect to modulator sampling frequency in Hz. For discrete time $\Sigma\Delta$ modulators, the requirements on OpAmp GBW is usually quite high even, as switch cap circuits have to settle within a certain

accuracy in a short period of time. In continuous time implementation, however, the requirement on GBW is relaxed a lot compared to its discrete-time counterpart. Plenty of literature shows that the minimum GBW only needs to be comparable with sampling frequency and GBW like $1 \sim 1.5 f_s$ is adequate [9].

Linearity

When it comes to linearity, the first integrator is the most critical one to be considered. The distortion coming from all the other following stages will be suppressed by the respective loop gain [9]. Thanks to negative feedback, the integrator third order harmonic distortion is attenuated by cube of $1 + LG$, where LG denotes the loop gain of the feedback. Thus the open loop third order harmonic distortion of OpAmp in the first integrator will be suppressed by two negative feedback loops - one is the local feedback introduced by the resistor and capacitor incorporating the integrator and the global feedback of the $\Sigma\Delta$ modulator main feedback path. Thus, to avoid overdesign, it is reasonable to assume that the first stage OpAmp input at a very low amplitude.

[14] points out that the impact of feedback on distortion can be written as:

$$HD_{3,f} = \frac{HD_{3,ori}}{(1 + LG)^3} \tag{4.7}$$

where $HD_{3,f}$ is the feedback system third order harmonic distortion, $HD_{3,ori}$ stands for the original OpAmp third order harmonic distortion. Therefore, the loop gain further decreases the harmonics. Since we are targeting at 68 dB SNR, $HD_{3,f}$ for the first integrator has to be larger than 70 dB with margin.

4.1.5 Negative Resistor Gain Boosting Amplifier

A single stage OpAmp with negative resistor gain boosting is adopted in this design. The PMOS input pair is placed in parallel with NMOS input pair for current reusing and achieving higher total g_m.

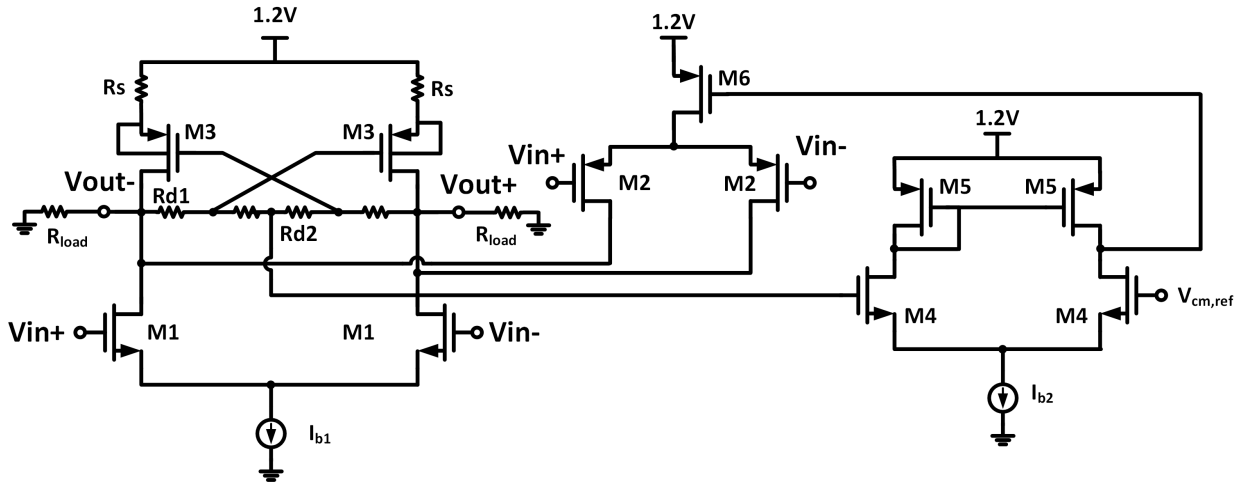


Figure 4.11: Negative resistor gain boosting OpAmp.

When positive and negative resistors are in parallel with each other, the total resistance can be computed as (4.8). If the positive resistance is smaller than the negative one but their ratio is close to unit, the parallel resistance will be boosted.

$$R_{pos} \parallel -R_{neg} = \frac{-R_{pos}R_{neg}}{R_{pos} - R_{neg}} = \frac{R_{pos}}{1 - \frac{R_{pos}}{R_{neg}}} \tag{4.8}$$

If the negative resistor is implemented by a PMOS cross couple pair, the negative resistance is given by $-\frac{1}{g_{mp}k}$, where k is the ratio of $\frac{R_{d2}}{R_{d1} + R_{d2}}$. Since g_m moves around 20% with PVT variation and system will be unstable if the denominator in (4.8) goes to negative, thus in order to relax the heavy dependency of negative resistance on g_m, a source degeneration resistor is added such that the negative resistor can be calculated by (4.9). Thus in the best case, if $g_{mp}R_s$ is much larger than unit, the negative resistor is only determined by R_s/k.

$$R_{neg} = \frac{1 + gm_pR_s}{g_{mp}k} \tag{4.9}$$

$$R_{pos} = (R_{d1} + R_{d2}) \parallel r_{ds1} \parallel r_{ds2} \parallel R_{load} \tag{4.10}$$

The transistor sizing and other important parameters are listed in Table 4.5:

Parameter	**Value**
M1	W/L = 50u/240n
M2	W/L = 30u/120n
M3	W/L = 150u/200n
M4	W/L = 20u/200n
M5	W/L = 16u/200n
M6	W/L = 90u/120n
RS	55 Ω
Rd1	11 kΩ
Rd2	3 kΩ
Rload	2.09 kΩ
Ib1	1 mA
Ib2	180 uA
Id6	550 uA

Table 4.5: Component values of OpAmp.

4.2 Simulation Results

4.2.1 OpAmp and Loop Filter Simulation Results

Parameter	Value
$r_{ds,n}$	3.9 kΩ
$r_{ds,p}$	6.3 kΩ
$g_{m,p}$	4.345 mS
$g_{m,n}$	9.79 mS
k	3/14

Table 4.6: Component values of OpAmp from simulation.

Table 4.6 shows the simulation results of main parameters that necessary to determine the positive and negative resistors for the OpAmp. The resistance can be calculated as:

$$R_{pos} = (R_{d1} + R_{d2}) \parallel r_{ds,n} \parallel r_{ds,p} \parallel R_{load} = 14k \parallel 3.9k \parallel 6.3k \parallel 2.09k = 1.04k\Omega \tag{4.11}$$

$$-R_{neg} = -\frac{1 + gm_p R_s}{g_{mp} k} = -\frac{1 + 4.345m \times 55}{4.345m \times 3/14} = -1.33k\Omega \tag{4.12}$$

Thus the ratio of $\frac{R_{pos}}{R_{neg}}$ equals to 0.78 and the total parallel resistance is 4.77 kΩ. Taking the 20% gm variation into account, the maximum ratio (gm is 20% higher than the typical value) is 0.903 correspond to a total resistance of 10.72 kΩ; the minimum ratio (gm is 20% lower than the typical value) is 0.65 correspond to a total resistance of 2.97 kΩ. The minimum gain in the whole range is around 29 dB, which is larger than the minimum requirement. The positive to negative resistor ratio and OpAmp gain vs. the sweep of gm from -20% to 20% is shown in Figure 4.12 and Figure 4.13 respectively. Thus the design is in the save zone.

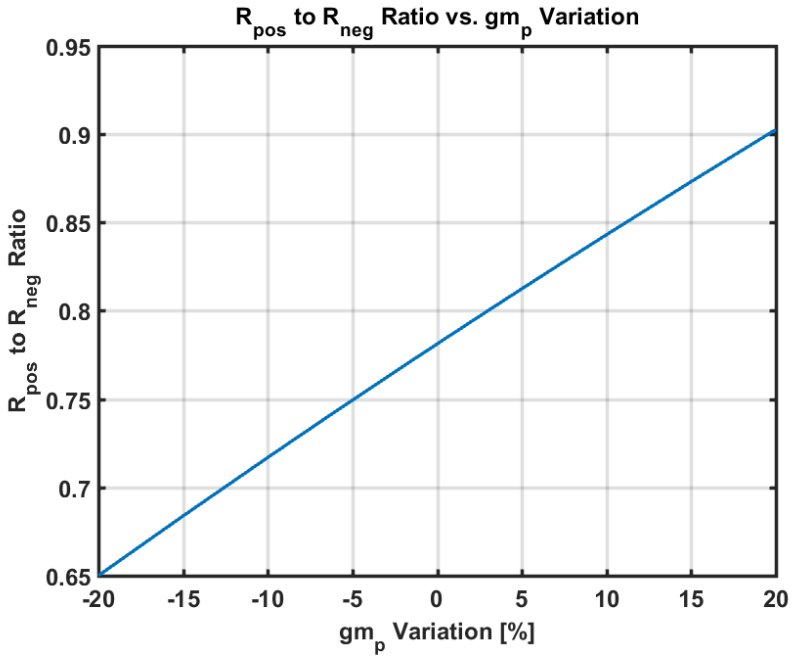


Figure 4.12: Positive resistor to negative resistor ratio vs. gm variation.

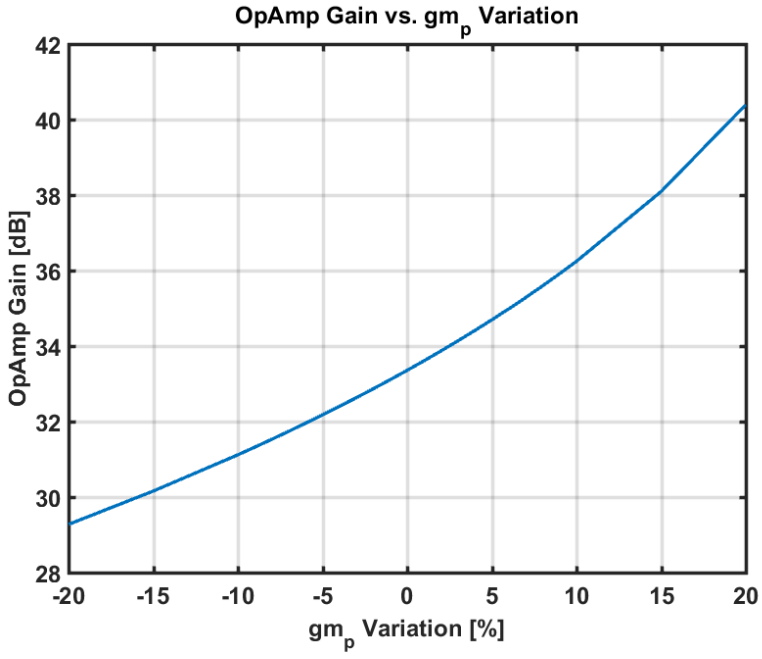


Figure 4.13: OpAmp gain vs. gm variation.

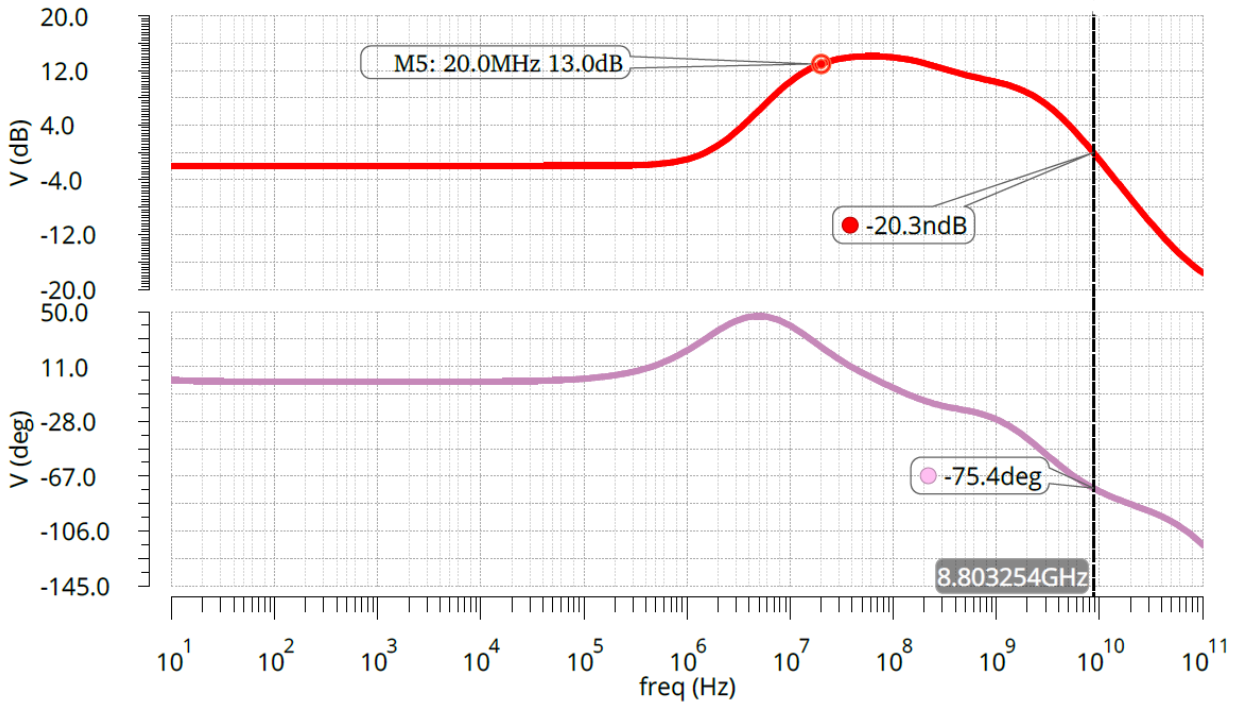


Figure 4.14: First stage integrator loop gain.

Figure 4.14 shows the loop gain of the first integrator. The feedback loop has 13 dB gain at 20 MHz bandwidth and the phase margin is 104.6 degree, thus the loop is stable. The testbench is shown in Figure 4.15.

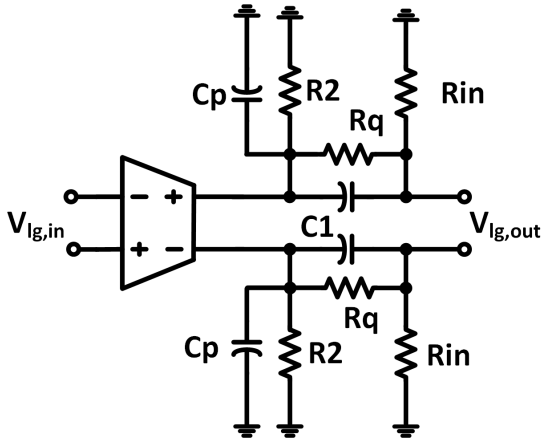


Figure 4.15: First integrator open loop circuit.

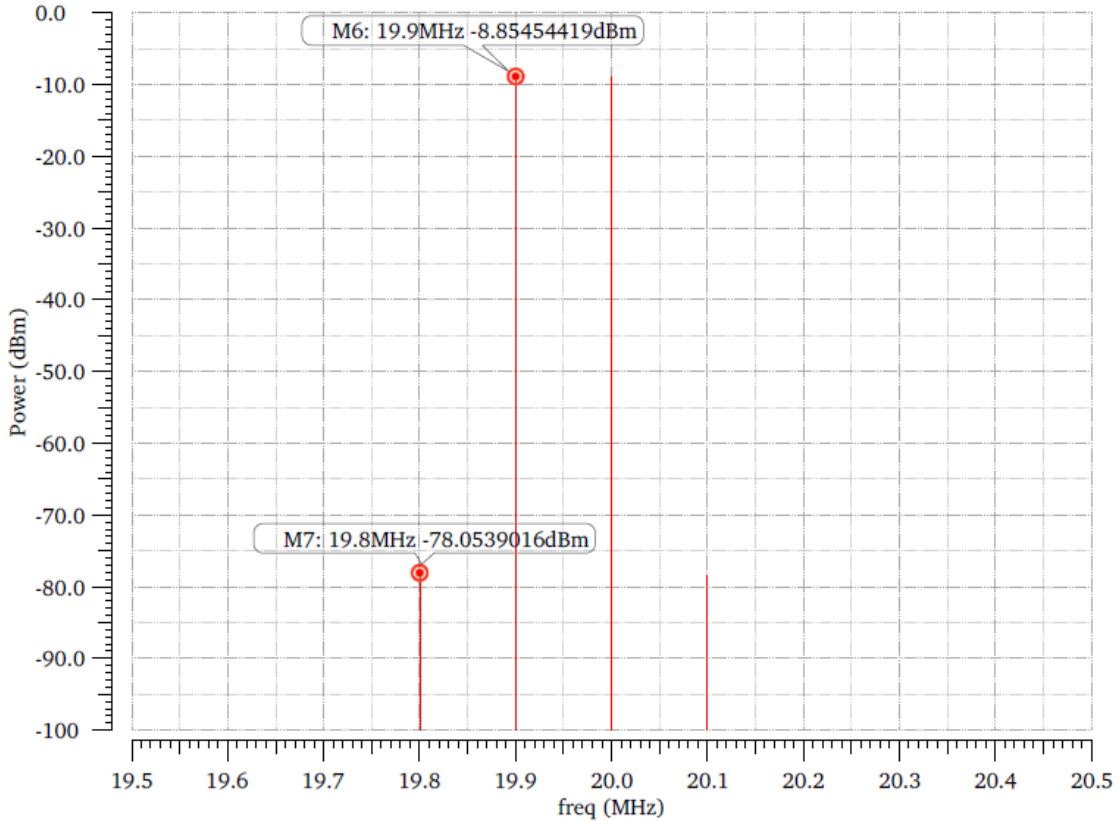


Figure 4.16: First integrator IM3.

Figure 4.16 shows two-tone test result of the first integrator. The closed-loop IM3 is 70 dB at around 20 MHz that meet the requirement. The integrator is simulated with loading of next stage input resistors. The output signal amplitude is around the maximum swing at this node.

The input referred noise vs. frequency of the biquad filter is shown in Figure 4.17. The total input referred noise within band-of-interest is 725.6p V^2. The full scale input amplitude is 1.4 V peak-to-peak differential, so the input referred noise introduced by biquad filter is around 79.26 dB below the full scale.

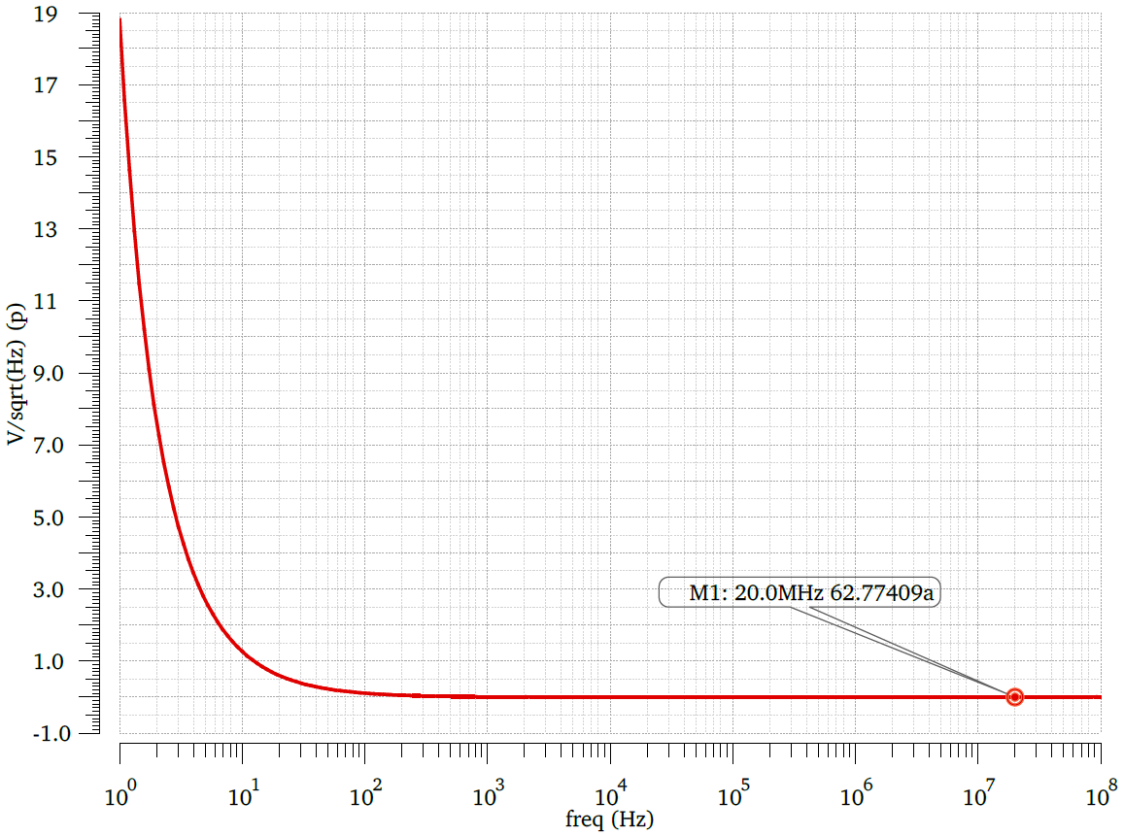


Figure 4.17: Biquad filter squared input referred noise vs. frequency.

4.2.2 System Simulation Results

The system level schematic of the proposed 3rd order $\Sigma\Delta$ modulator shown in Figure 4.18 is simulated in Cadence with the integrators implemented in transistor level. The summing stage is still in macro-model.

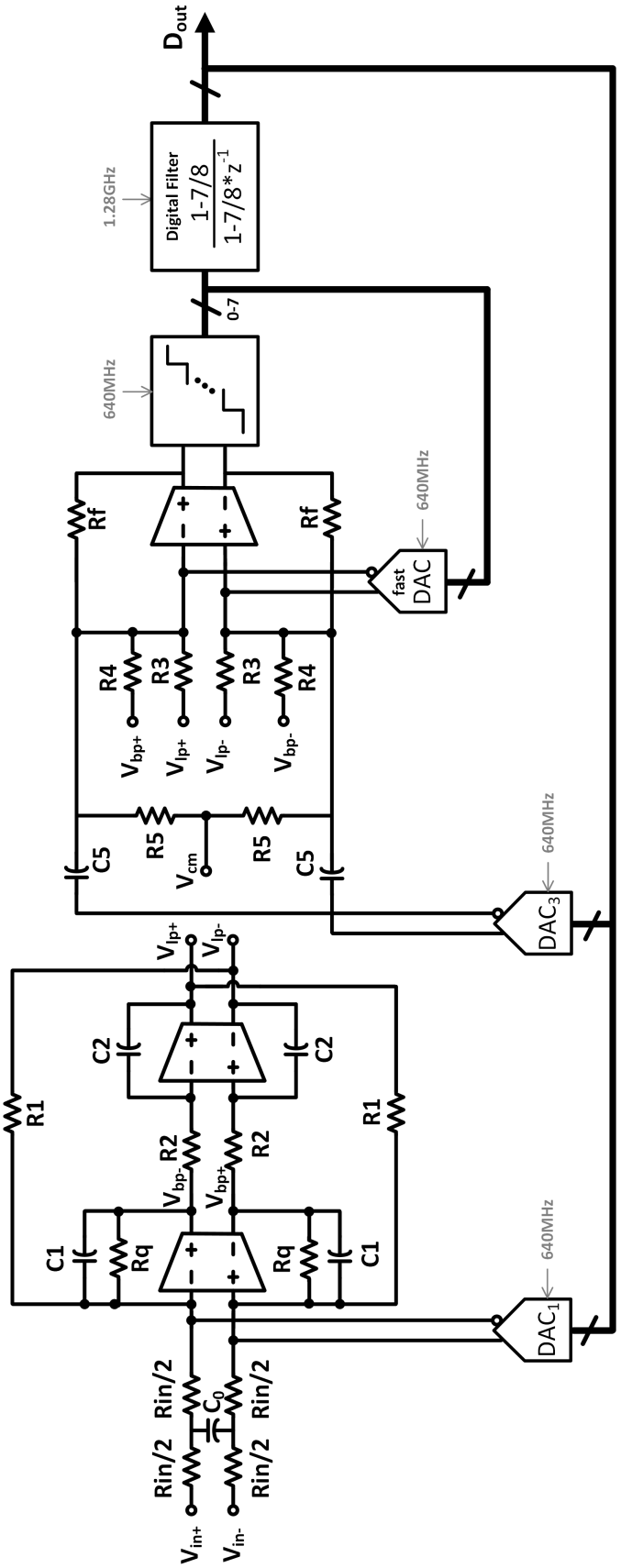


Figure 4.18: Proposed 3rd order hybrid jitter tolerant $\Sigma\Delta$ modulator schematic.

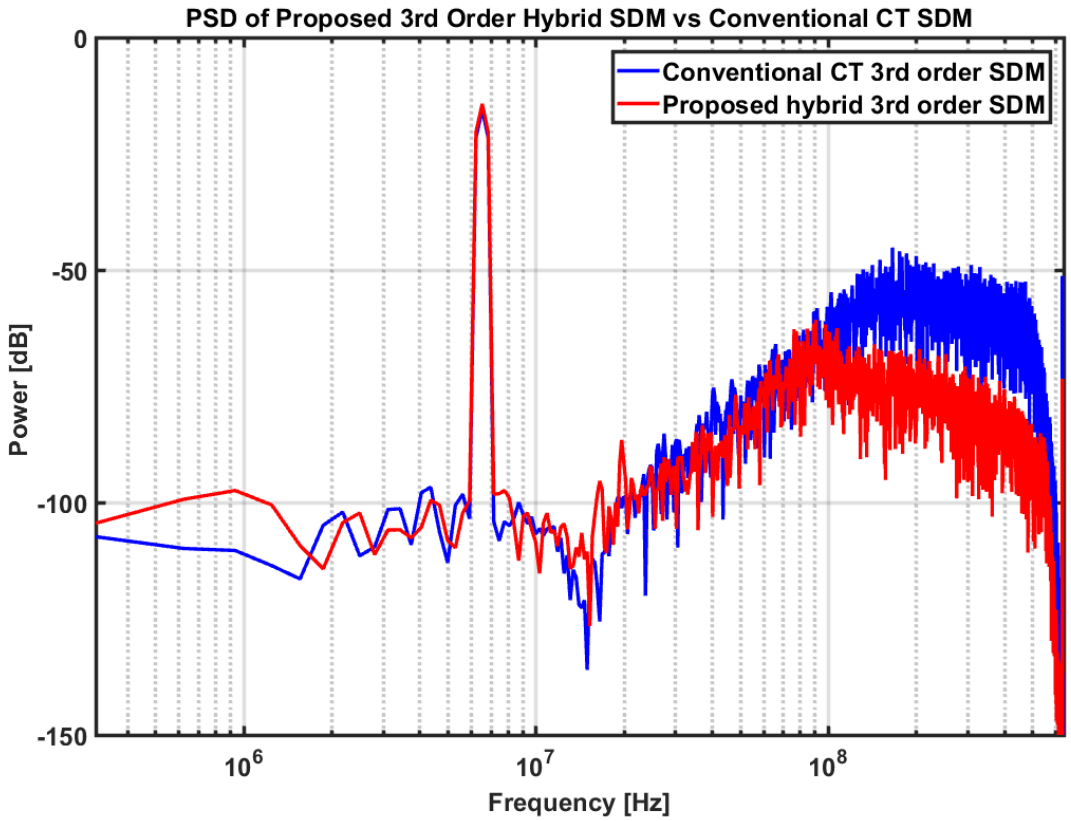


Figure 4.19: Power spectral density of the conventional CT and proposed hybrid 3rd order $\Sigma\Delta$ modulator in Cadence.

The power spectral density of the proposed and conventional ADCs simulated with sinusoidal input at amplitude of -4 dBFS and 6.5625 MHz is shown in Figure 4.19. SNR equals to 68.98 dB and maximum out-of-band noise level is 50 dB lower than signal level. The proposed out-of-band noise is around 30 dB lower than the conventional case on average. The input frequency is chosen to be the worst case where third harmonic is right at the edge of signal bandwidth.

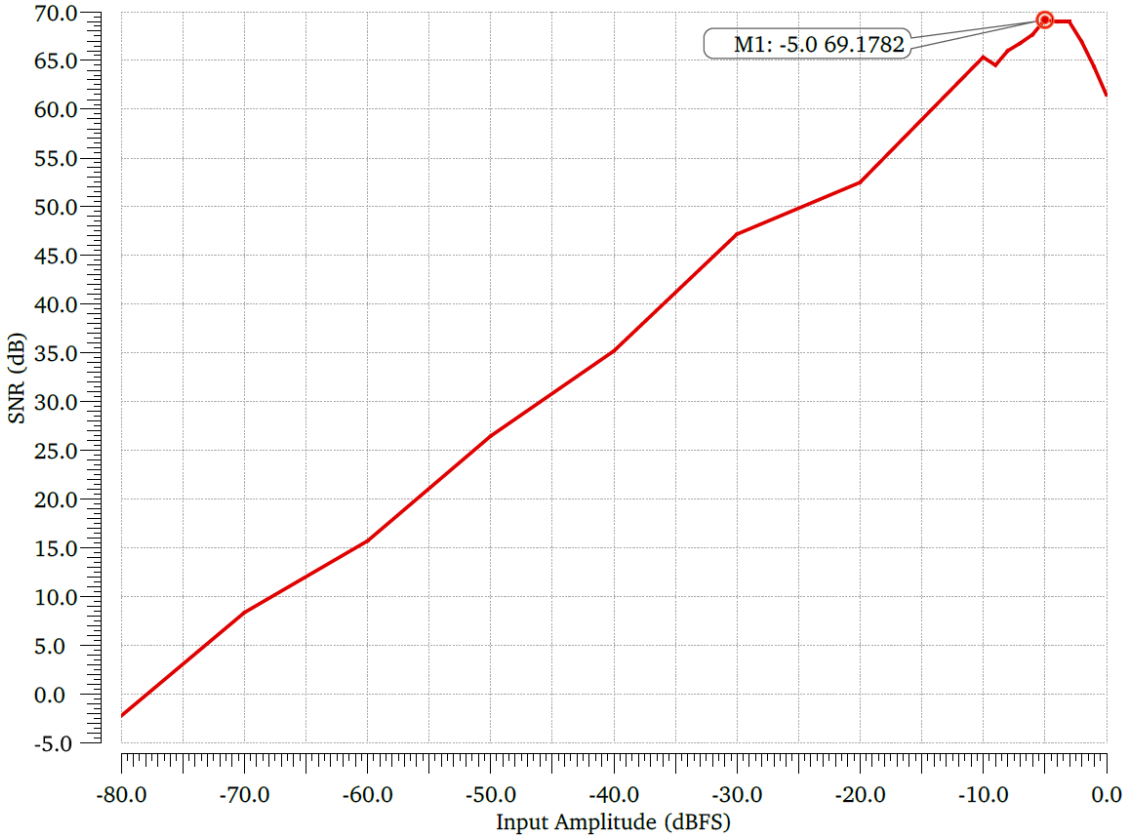


Figure 4.20: SNR vs. input sinewave amplitude of the proposed 3rd order hybrid $\Sigma\Delta$ modulator.

The SNR vs. input signal amplitude plot is shown in Figure 4.20 at input frequency equals to 6.5625 MHz. Dynamic range is 77.91 dB and maximum SNR is 69.1782 dB at -5 dBFS input amplitude.

5. CONCLUSION

In this thesis, a novel idea to reduce continuous-time $\Sigma\Delta$ ADC jitter sensitivity by splitting the last stage integrator into a digital filter and an analog gain stage is introduced. This concept is implemented in two configurations - the first is a fourth order hybrid $\Sigma\Delta$ ADC with 2-bit quantizer and the second one is a third order hybrid $\Sigma\Delta$ ADC with 3-bit quantizer. The design procedure is described in detailed. Both ADCs are implemented in TSMC 40nm CMOS technology and the maximum achievable SNR is 69.18 dB. The SQNR of the proposed hybrid $\Sigma\Delta$ ADC is 14 dB higher than the conventional CT $\Sigma\Delta$ ADC with the same quantizer levels if the rms clock jitter is as high as 10% of the clock period.

REFERENCES

[1] William Ralph Bennett. Spectra of quantized signals. *The Bell System Technical Journal*, 27(3):446–472, 1948.

[2] James A Cherry. *Theory, practice, and fundamental performance limits of high-speed data conversion using continuous-time delta-sigma modulators.* Ph.D. thesis, Carleton University, 1999.

[3] James A Cherry and W Martin Snelgrove. Clock jitter and quantizer metastability in continuous-time delta-sigma modulators. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 46(6):661–676, 1999.

[4] Sheng-Jui Huang and Yung-Yu Lin. A 1.2 v 2mhz bw 0.084 mm 2 ct $\delta\sigma$ adc with- 97.7 dbc thd and 80db dr using low-latency dem. In *2009 IEEE International Solid-State Circuits Conference-Digest of Technical Papers*, pages 172–173. IEEE, 2009.

[5] A. Jain and S. Pavan. Continuous-time delta-sigma modulators with time-interleaved fir feedback. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 65(2):434–443, Feb 2018.

[6] Jun-Gi Jo, Jinho Noh, and Changsik Yoo. A 20-mhz bandwidth continuous-time sigma-delta modulator with jitter immunity improved full clock period scr (fscr) dac and high-speed dwa. *IEEE Journal of Solid-State Circuits*, 46(11):2469–2477, 2011.

[7] G. Mitteregger, C. Ebner, S. Mechnig, T. Blon, C. Holuigue, and E. Romani. A 20-mw 640-mhz cmos continuous-time $\sigma\delta$ adc with 20-mhz signal bandwidth, 80-db dynamic range and 12-bit enob. *IEEE Journal of Solid-State Circuits*, 41(12):2641–2649, Dec 2006.

[8] B. Murmann. "adc performance survey 1997-2019," [online]. Available: `http://web.stanford.edu/~murmann/adcsurvey.html`.

[9] Maurits Ortmanns and Friedel Gerfers. *Continuous-time sigma-delta A/D conversion: fundamentals, performance limits and robust implementations*. Springer, 2006.

[10] Shanthi Pavan, Richard Schreier, and Gabor C Temes. *Understanding delta-sigma data converters*. John Wiley & Sons, 2017.

[11] Marcel JM Pelgrom, Aad CJ Duinmaijer, and Anton PG Welbers. Matching properties of mos transistors. *IEEE Journal of solid-state circuits*, 24(5):1433–1439, 1989.

[12] Negar Rashidi. *Low Noise, Jitter Tolerant Continuous-Time Sigma-Delta Modulator*. Ph.D. thesis, Texas A&M University, 2016.

[13] Ramy Saad, Sebastian Hoyos, and Samuel Palermo. Analysis and modeling of clock-jitter effects in delta-sigma modulators. In *MATLAB-A Fundamental Tool for Scientific Computing and Engineering Applications-Volume 1*. IntechOpen, 2012.

[14] Willy Sansen. Distortion in elementary transistor circuits. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 46(3):315–325, 1999.

[15] Richard Schreier, Gabor C Temes, et al. *Understanding delta-sigma data converters*, volume 74. IEEE press Piscataway, NJ, 2005.

[16] Jose Silva-Martinez, Aydin Ilker Karsilayan, and Hemasundar Mohan Geddada. Blocker and jitter tolerant wideband $\sigma\delta$ modulators. In *2012 IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pages 390–393. IEEE, 2012.

[17] Bernard Widrow. A study of rough amplitude quantization by means of nyquist sampling theory. *IRE Transactions on Circuit Theory*, 3(4):266–276, 1956.