In-body wireline interfacing platform for multi-module implantable microsystems

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***Abstract*—The recent evolution of implantable medical devices from single-unit stimulators to modern implantable microsystems, has driven the need for distributed technologies, in which both the implant system and functions are partitioned across multiple active devices. This multi-module approach is made possible thanks to novel network architectures, allowing for in-body power and data communications to be performed using implantable leads. This paper discusses the challenges in implementing such interfacing system and presents a platform based on one central implant (CI) and multiple peripheral implants (PIs) using a custom 4WiCS communication protocol. This is implemented in PCB technology and tested to demonstrate intrabody communication capabilities and power transfer within the network. Measured results show CI-to-PI power delivery achieves 70 % efficiency in expected load condition, while establishing full-duplex data link with up to 4 PIs simultaneously.**

I. Introduction

The field of implantable medical devices (IMDs) has a long history of successful examples, such as cardiac pacemakers, insulin pumps, and cochlear implants. More recently, neural prostheses have had a significant impact to the quality of life of millions of individuals, by connecting to the nervous system with neuromodulation techniques, e.g. Deep Brain Stimulation (DBS) for relief of Parkinsons disease tremors, epileptic seizures and Spinal Cord Stimulation (SCS) for chronic pain [1]. This has lead to the development of modern IMDs based on implantable microsystems, made feasible by novel advances on ultra-low-power, miniaturised, and smart microtechnology.

In parallel, the growing trend towards wearable consumer electronics for healthcare, together with the increasing interest on the emerging Internet of Things (IoT) framework, has introduced new types of network architectures, generally referred to as body area networks (BANs) or body sensor networks (BSNs) [2]. These are comprised of multiple communicating nodes/modules, in or on the body, continuously monitoring human physiology and feeding data to a nearby smart device. Also, an IEEE communication standard regarding both wearable and implantable BANs - IEEE.802.15.6 – has been formed.

Although current clinically-available IMDs are still single unit devices - housing the energy source and the active electronics, using long wires to reach the target location – a new generation of 'networked' implantable systems is now emerging: the need for i) more sensing and stimulating channels at multiple locations; ii) active electronics in close proximity with the biological tissue; and iii) closed-loop adaptive treatments (stimulation in response to monitoring) is driving distributed implantable technologies. This is based on one *central implant CI*, hub device, and multiple *peripheral implants PI*, distributed nodes, similarly to the BAN network

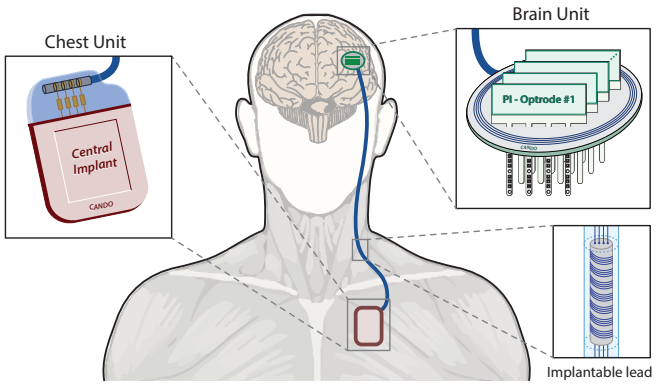

Fig. 1. Concept of the CANDO implant system with one *Central Implant* at the chest unit and multiple *Peripheral Implants* at the brain unit.

architecture. In our previous work [3] [1], we coined the term *multi-module approach* to classify such devices. This approach allows for front-end specific functions – recording/stimulation, signal conditioning, and data conversion to be effectively performed on-site by the PIs. On the other hand, high level computational functions, power management, and control are performed within the CI hub in a convenient location in the body. On the downside, having multiple active PIs raises the challenge of power and information transfer among implants, with as a result increased complexity and losses in the interfacing channel.

Despite extensive research both in academia and industry in developing wireless modalities, inter-module power and data transfer is typically achieved using wireline links. This is due to the high reliability and efficiency provided by physical wires and established implantable lead technology for medical applications. Examples include: advanced prosthetic systems [4] [5], Functional Electrical Stimulation (FES) systems [6], and brain implants [7].

This paper presents a novel in-body wireline interface implementation based on custom PCBs, the 4WiCS (4-wire communication system) protocol and previously developed Application Specific Integrated Circuit (ASIC). Supporting test results evaluate the capability of the platform to establish a data communication link between CI and PIs, whilst also facilitating power transmission. The remainder of this paper is organised as follows: Section II discusses challenges and techniques for interfacing between multiple implants; Sections III and IV describes the 4WiCS protocol, its use with a IMDs; and the custom platform implemented; Section V presents measured results; and Section VI concludes the paper.

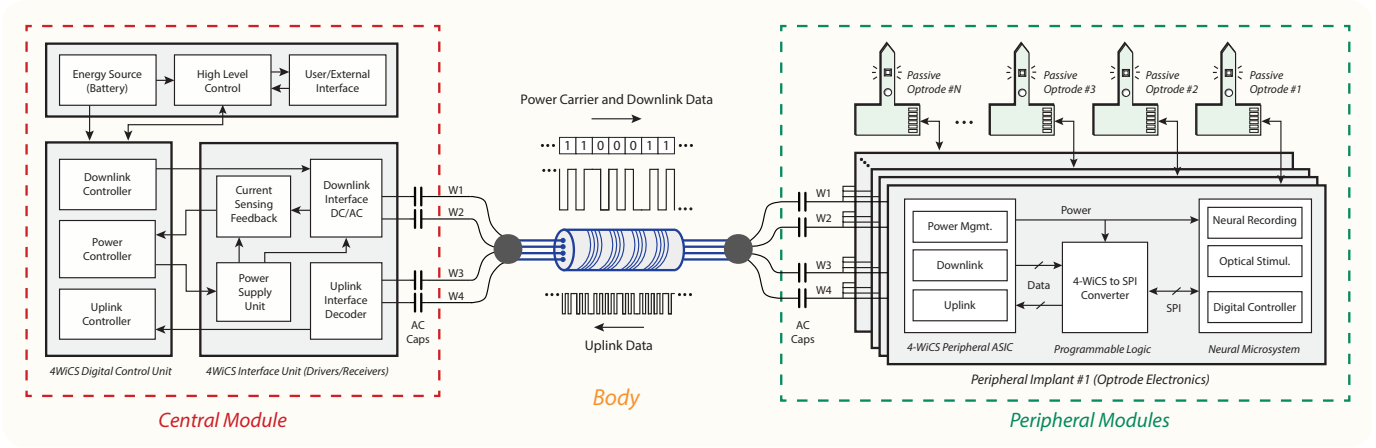

Fig. 2. Block Diagram of 4WiCS system interfacing with corresponding in-body modules at both central and peripheral end.

II. Interfacing between multiple implants

In a multi-module wireline implant system, the energy source (battery), is typically enclosed within the central implant and thus power needs to be transmitted to the active PIs to function. Since battery life is a key consideration in IMDs, achieving highly efficient CI-to-PI power delivery is crucial. This requires not only the power consumption of each module to be as low as possible, but also the optimisation of the end-to-end power delivery path. This means minimising losses in all components along the power path, including cables in the case of a wireline network.

The simplest method to transmit power across short distance cables is via DC. However, this is undesirable in implantable medical applications, as DC voltage bias across the conductors in the cable may accelerate corrosion, thus raising the risk of insulation failure and possibly compromising patient safety. The most common power delivery schemes for implantable systems are thus AC biased allowing for galvanic isolation and thus providing improved safety. Nonetheless, they need power domain conversion both at CI (DC/AC) and at PIs (AC/DC), with additional passive and active circuitry increasing complexity and power consumption.

AC signalling is also desirable compared to DC power transfer because of the opportunity of combining this with data communication using the same wires. As the PIs require information exchange with the central module, a bidirectional digital data link is established. Differently from the return link (PI-to-CI), the forward link (CI-to-PI) has the same direction of the power delivery carrier. Therefore, these can share the same physical channel and be combined in a single forward signal. Due to this, in-body communications are usually based on keying modulation techniques, such as frequency-shift keying (FSK) and phase-shift keying (PSK), which allow for data to be encoded in the frequency/phase variation of the power delivery carrier.

Standard serial communication protocols can be employed as inter-module link, e.g. SPI, I2C, and CAN. However, these do not typically meet requirements for implanted devices, e.g. differential signalling for noise immunity, AC coupling for safety, low complexity/component count. Therefore, the current approach is to adopt: (i) a customised protocol - optimised for the given function and adapted to the employed communication channel; with supporting (ii) interface ASICs.

III. 4-wire Communication System - 4WiCS

The in-body interfacing system presented in this paper follows the trends and considerations on power and data communication discussed above. Our custom protocol (called 4WiCS) was first described in [7]. An end-to-end platform employing such protocol is designed accordingly, by meeting the requirements set by our specific application, CANDO (Fig. 1). This proposes a closed-loop approach to suppressing seizures in patients suffering from focal Epilepsy. The therapy relies on 1) neural activity observed by front-end recording electrodes and 2) responding with realtime optogenetic neuromodulation achieved with μLED stimulation. The two functions are combined in a single active opto-electrode (optrode) device. Multiple optrodes are then distributed in an array configuration, hosted on a passive baseplate.

Fig.1 shows the multi-module implantable system the 4WiCS interface is designed to be part of. It is composed of a *chest unit* including a rechargeable battery and an embedded system with a processing unit. This is the CI of the implant network (acting as a master), receiving data from the PI modules and issuing control commands. The PIs are represented by the active optrodes at the *brain unit*, each with recording and stimulation capabilities. The 4WiCS interface facilitates a reliable end-to-end link between hub and nodes, by establishing full-duplex data transmission together with CI-to-PIs power delivery method. Square-waves are chosen as communication signals both for forward link (downlink) and return link (uplink) and the digital data is encoded with Manchester code, which allows for downlink data and power superposition on the same line (with no DC component).

The physical layer used to transmit the signals on the network is provided by a 4-wire subcutaneous lead: the medically approved Cooper cable. Two of the four Platinum-Iridium wires constituting the implantable lead are responsible for delivering the downlink (and power) signal, whilst the remaining pair is dedicated to the uplink signal. The frequency of the forward and return links are different from each other

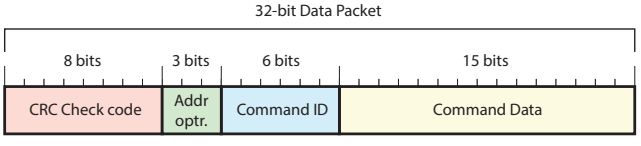

Fig. 3. Data packet of the 4WiCS protocol with (a) PI address, (b) command ID, (c) command data, and (d) an 8-bit CRC error-detecting code.

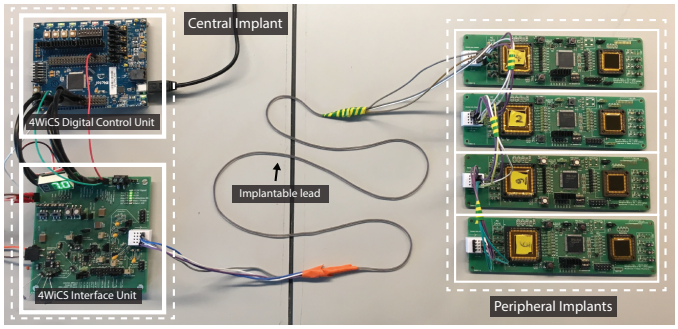

Fig. 4. End-to-End board-level platform with key implant modules annotated.

and depend on the maximum required data throughput in either direction. The downlink data rate is determined by the command packet size (Fig.3) and frequency. This has been set to 100 kHz. Given the maximum number of recording channels to be streamed, a higher datarate is needed for the data returning from the optrodes (i.e. the uplink), determined to be 1.6 MHz.

The system architecture of the 4WiCS in-body interfacing is outlined in the block diagram in Fig.2. An end-to-end interfacing platform, representing the whole implant system, is implemented to demonstrate system integration functionality and reliability, both on an inter-module and intra-module level.

IV. End-to-End Platform

As illustrated in the block diagram in Fig.2, for the CI and PIs to communicate with each other using the 4WiCS protocol, interface hardware is required at both ends.

A. Power and Data Path

At the central module, the commands to be sent to the optrodes are generated by a high level control unit and encoded by the downlink controller within the 4WiCS control unit. This in turn activates the DC/AC drivers that generate the downlink/power AC signal (100 kHz square wave), conditioned to the transmission channel by the power supply unit (PSU). AC coupling capacitors (on each wire) ensure there is no DC leakage from the cable. When reaching the peripheral modules, the AC signal undergoes two parallel conversions in each of the PIs: (i) the AC power is converted to DC domain by a rectification circuit; and (ii) the digital signal is decoded and both clock and data are recovered. A voltage regulation stage then adapts the DC power signal in order to be used by the neural microsystem circuitry to perform the core functions (recording or stimulation). Moreover, the digital data is processed further by a Finite State Machine (FSM, implemented using reconfigurable hardware) that is responsible for translating to and from standard SPI link – necessary to communicate via the SPI module in the neural microsystem controller. The translation is enabled only if the FSM recognises its own PI address code in the data packet.

When, for example a recording command is generated by the CI, the PI that is being addressed is requested to send information back through the 4WiCS link. The recorded neural signals, acquired by the front-end circuitry, are first converted from SPI to 4WiCS, encoded and signalled to the transmission line. Since the uplink data rate is higher than the downlink one, a higher frequency clock is generated with a phase-locked loop (PLL) circuit to achieve 1.6 Mbps. After passing through the cable and the galvanic coupling, the differential uplink

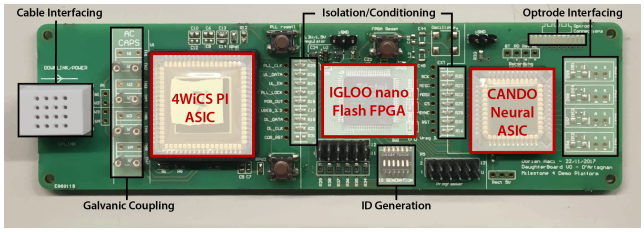

Fig. 5. Custom PCB representing the optrode architecture at the peripheral implant. Highlighted the 3 active components: (a) 4WiCS peripheral implant ASIC; (b) IGLOO nano flash FPGA; and (c) CANDO neural microsystem.

signal is converted to single-ended and decoded by the receiver circuit. The uplink controller processes the raw digital data representing the recorded neural signal and finally feeds it to the high level control unit for data interpretation.

B. Circuit Implementation

The end-to-end wireline platform presented in Fig.4 is implemented in PCB technology, with ASIC components integrated within the PCBs at peripheral end. Test chips have been previously designed and fabricated in a commercially-available CMOS 0.35 μm technology to demonstrate the functionality of the optrode architecture. The PCB platform meanwhile demonstrates system integration of these components within the multi-module implant system. A 50 cm-long Cooper cable is employed moreover as the end-to-end communication channel.

1) Central Implant: a PC-based graphical user interfaces (GUI) establishes high level control, command generation, and data monitoring. This connects through a UART/USB interface to the IGLOO Nano FPGA development board (AGL250V2-VQG100), on which the *4WiCS digital control unit* is implemented in VHDL language. A custom PCB representing the *4WiCS line interface unit* includes: (i) power management; (ii) downlink line drivers; (iii) uplink line receivers; and (iv) a current sensing feedback circuit used to provide adaptive power delivery depending on the peripheral load current, as described in more detail in [3]. All active and passive components utilised in the central implant PCBs are off-the-shelf components integrated within the embedded system.

2) Peripheral Implants: 4 identical custom PCBs represent the active circuitry of 4 different optrodes, as shown in Fig.4. These are connected in parallel to the implantable lead with AC coupling capacitors. Each peripheral board contains 3 active components: the first to interface at the lead end is the *4WiCS peripheral implant ASIC* described in [7]. This includes the circuitry responsible for: (i) the power management of the entire board, achieved via a full-wave rectifier and voltage regulators, (ii) the downlink path with decoder and data/clock recovery circuits, and (iii) the uplink path with encoder and line drivers. The second custom IC is the *CANDO Neural ASIC*, detailed in [8]. This establishes front end interfacing for neural signal recording and optical stimulation and comprises an on-chip FSM for local control and external serial communication. In order for the two ASICs to exchange data in the correct format, an interpreting logic is configured on a programmable device, the IGLOO nano flash FPGA. Such FPGA was chosen because of its capability to implement bidirectional parallel threads, despite its minimal number of logic elements. A fabricated peripheral PCB with assembled active and passive components is presented in Fig.5.

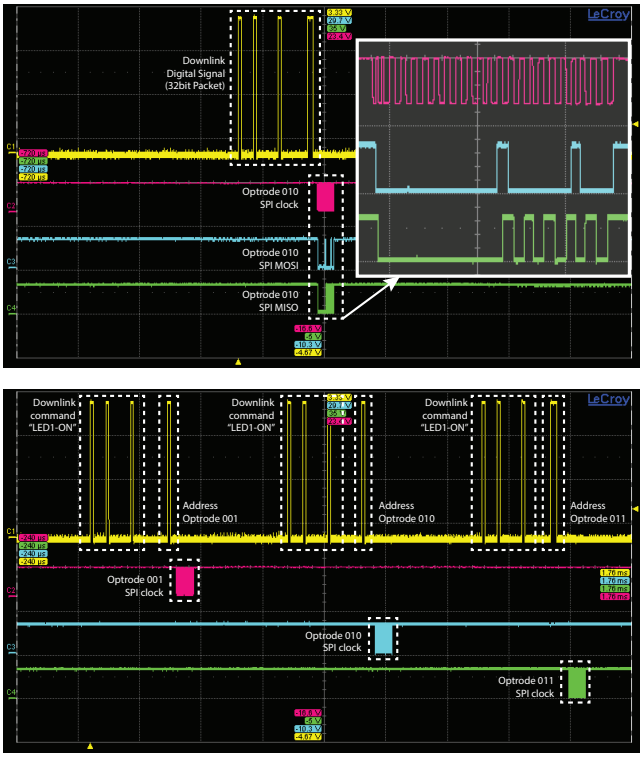

Fig. 6. Oscilloscope traces of: (top) downlink and SPI signals (SCK, MOSI, MISO) with acknowledgement response from a PI through SPI link; and (bottom) 3 PIs establishing SPI communication when addressed with respective ID codes.

V. Measured Results

A. Functional Testing

Functional tests of the platform are performed following a system testing sequence. At first, the central module is powered up and the voltage levels are inspected before generating the 100 kHz power delivery carrier. This is then activated from the GUI, initially with no downlink information encoded, while ensuring the current through the Cooper cable and the voltage levels at the peripheral end are within the correct range. This is achieved and measured via the current sensing feedback, allowing for fixed voltage levels at the peripheral implants. Accordingly, the downlink communication is enabled and commands are sent from CI to PIs. If the addressed PI recognises its ID in the 3-bit address code, the relative neural ASIC receives the command and promptly responds via the SPI link. The activation of the SPI MISO (master input slave output) signal with the acknowledgement packet demonstrates correct (i) reception of the command by the microsystem and (ii) generation of the uplink clock frequency (1.6 MHz), as shown in Fig.6-top. The response sent through the uplink path is received at the CI end and displayed on the PC GUI.

B. Performance Testing

Thanks to adaptive power delivery, the voltage level at the rectifier output is maintained at 5 V$\pm$300 mV in every PI; the voltage ripple is less than 200 mV for any variation of the optrode load within the permitted range (0-4 mA). The graph in Fig.7 shows the power transmission efficiency (PTE) calculated as the power sourced by the rectifier at a single PI (measured in different load conditions) with respect to the power delivered by the PSU at the CI. This has a high dependence on the I^2R loss on the lead wires and achieves a maximum value of 70 %.

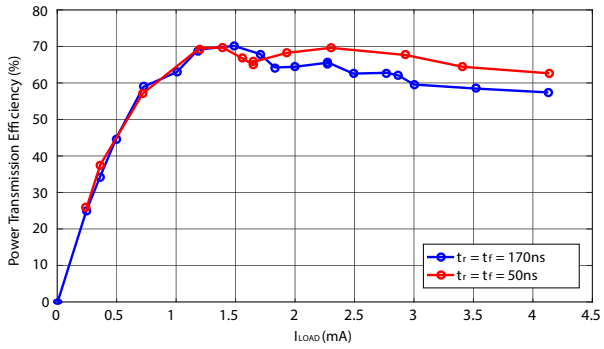

Fig. 7. Power transmission efficiency (PTE) of the power delivery to varying of load current. (Red) rise and fall time of power carrier square wave tr =tf= 50 ns; (blue) tr =tf= 170ns.

The platform demonstrates capability for the CI to address and communicate simultaneously with multiple PIs. Fig.6-bottom shows three different optrodes activating the SPI interface clock in response to the downlink packets with corresponding address.

VI. Conclusion

This paper has presented a novel end-to-end platform implementation and discussed the key challenges arising when moving from single-unit implant to multi-module IMDs. To perform their core function, these systems require both power to be delivered efficiently to each node of the network and reliable intermodule connectivity. A circuit implementation employing the 4WiCS interfacing protocol and existing custom CMOS ICs was designed using a PCB-based platform. Testing results have demonstrated the functional capability of the 4WiCS interface to delivery power and simultaneously communicate with up to 4 PIs from a single CI. Power efficiency measurements have shown that the PTE performance depends primarily on the electrical characteristics of the transmission line and on the PIs load condition. Ongoing and future work is focusing on the monolithic integration of the 4WICS interface together with the core PI neural functions, in addition to further improving the system performance and PTE.

Acknowledgement

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