



Title	Effects of a photo-assisted electrochemical etching process removing dry-etching damage in GaN
Author(s)	Matsumoto, Satoru; Toguchi, Masachika; Takeda, Kentaro; Narita, Tetsuo; Kachi, Tetsu; Sato, Taketomo
Citation	Japanese Journal of Applied Physics (JJAP), 57(12), 121001 https://doi.org/10.7567/JJAP.57.121001
Issue Date	2018-12
Doc URL	http://hdl.handle.net/2115/76058
Rights	©2018 The Japan Society of Applied Physics
Type	article (author version)
File Information	JJAP2018_TSato.pdf



[Instructions for use](#)

Effects of a photo-assisted electrochemical etching process removing dry-etching damage in GaN

Satoru Matsumoto¹, Masachika Toguchi¹, Kentaro Takeda¹, Tetsuo Narita², Tetsu Kachi³, and Taketomo Sato^{1*}

¹*Research Center for Integrated Quantum Electronics (RCIQE), and Graduate School of Information Science and Technology, Hokkaido University, Sapporo 060-8613, Japan*

²*Toyota Central R&D Labs. Inc., 41-1, Yokomichi, Nagakute, Aichi 480-1192, Japan*

³*Institute of Materials and Systems for Sustainability, Nagoya University, Furo-cho, Chikusa-ku, Nagoya 464-8601, Japan*

*Corresponding author, e-mail address: taketomo@rciqe.hokudai.ac.jp

Abstract

We investigated the ability of a photo-assisted electrochemical (PEC) etching process to remove the damage that dry etching causes in the near-surface region of GaN samples. The process consists of anodic oxidation of the GaN surface and subsequent dissolution of the oxide with a chemical treatment, and the extent of the PEC reactions depends on the total charge density transferred in them. The PEC process was conducted for samples prepared with various dry-etching conditions followed by fabrication of Schottky barrier diodes (SBDs) and metal-insulator-semiconductor (MIS) capacitors. The PEC process greatly improved the barrier height, ideality factor, and reverse leakage current of SBDs. Capacitance-voltage measurements of MIS capacitors revealed that the densities of interface states and discrete traps were both reduced by the PEC process. The results obtained here show that the PEC process can remove dry-etching damage from the GaN surface.

1. Introduction

Significant progress has been achieved in gallium nitride (GaN)-based electronic devices because of their excellent material properties, such as their high breakdown electric field (3.3 MV/cm), which is due to their wide bandgap (3.4 eV), and their high saturation electron velocity (2.7×10^7 cm/sec).^{1,2)} The AlGaN/GaN high-electron-mobility transistor (HEMT) is a typical example taking advantage of those features for high-frequency and high-power application.³⁾ High blocking voltage and low on-state resistance (R_{ON}) are simultaneously achieved by utilizing the high electron mobility (2000 cm²/V·sec) and high sheet charge density (1×10^{13} cm⁻²) yielded at the AlGaN/GaN hetero-interface. Recent remarkable advances in the crystal quality of GaN substrate have also resulted in the progress of vertical-type GaN power devices.^{4,5)} Trench-gate GaN MOSFETs potentially useful for high-power switching application have been reported by several groups.^{6,7)} Oka et al. have

reported a remarkably high blocking voltage, over 1 kV, and reduction of R_{ON} to less than $2.0 \text{ m}\Omega \cdot \text{cm}^2$ in trench-gate MOSFETs with a hexagonal cell structure.⁷⁾

Dry etching has been used for the fabrication of GaN-based electronic devices because the chemical stability of group-III nitrides precludes the use of wet etching, but dry-etched surfaces are negatively affected by various types of damage that can degrade device performance.⁸⁾ Dry-etching processes assisted by high-energy plasma irradiation or ion bombardment have been reported to cause nitrogen-vacancy defects and disordered atomic-bond arrangements.^{9,10)} These kinds of damage and defects induce high-density surface and interface states in the forbidden band, which leads to severe operational stability problems such as gate leakage, current collapse, and threshold voltage instability.¹¹⁻¹⁴⁾ Many attempts to recover the etching-induced surface damage by means of thermal annealing treatments have been reported,^{9,15-18)} but high-temperature annealing results in oxidation and nitrogen loss leaving the GaN surface nonstoichiometric. Terano et al. have recently reported that annealing GaN in the temperature range of 700–900 °C was very effective for recovering etching damage but the GaN was oxidized from its surface to a depth of 60 nm if the annealing temperature reached 900 °C.¹⁸⁾ The maximal performance of GaN-based devices thus cannot be obtained unless low-temperature and low-energy methods for removing surface damage are developed.

In this study we have investigated a photo-assisted electrochemical (PEC) etching process consisting of photo-assisted anodic oxidation of the surface-damaged layer and subsequent dissolution of the oxide by chemical treatment at room temperature.^{19,20)} We have succeeded in controlling of the oxidation and etching thickness by adjusting the total amount of charge transferred during the PEC process. To clarify the effects of the PEC process, we have evaluated the electrical properties of various Schottky barrier diodes (SBDs) and metal-insulator-semiconductor (MIS) capacitors fabricated on the dry-etched and PEC-etched GaN surface prepared with various etching conditions.

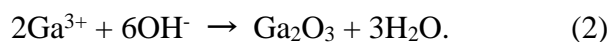
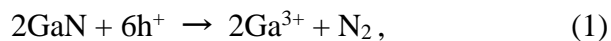
2. Experimental method

We used as the starting samples n-type GaN epitaxial layers (Si: $5 \times 10^{16} \text{ cm}^{-3}$) having a thickness of 3 μm grown by metal organic vapor phase epitaxy (MOVPE) on free-standing GaN substrates ($N_D > 5 \times 10^{17} \text{ cm}^{-3}$) whose threading dislocation density (TDD) was less than $5 \times 10^6 \text{ cm}^{-2}$. Figure 1(a) shows a schematic illustration of the process flow used in this study. To investigate the impact of damages induced by the dry-etching process, we used two kinds of dry-etching techniques: ECR-RIBE (electron cyclotron resonance reactive ion beam etching) and ICP-RIE (inductive coupled plasma reactive ion etching). ECR plasma for the ECR-RIBE was excited at a microwave frequency of 2.45 GHz, and a CH_4/H_2 -based gas mixture was used as the etching gas in the ECR-RIBE. A 150-V dc acceleration voltage was applied to the GaN substrate, and ions accelerated by the high-electric field directly collided

with the GaN surface. The plasma for the ICP-RIE was generated by a radio-frequency (13.56 MHz) power supply with an antenna power of 300 W. The bias power applied to the GaN sample was set to be 5 W or 30 W. A BCl_3/Cl_2 - based gas mixture was used as the etching gas in the ICP-RIE.

Firstly, 30 nm-thick GaN was etched with ECR-RIBE or ICP-RIE as an initial etching process. An ohmic contact (Ti/Au: 20 nm/50 nm) was formed on the backside of the samples by a conventional evaporation and annealing process. Then the n-GaN surface was etched by the PEC process consisting of anodic oxidation and subsequent alkali treatment. As shown schematically in Fig. 1(b), the PEC process was performed with a standard electrochemical cell having three electrodes. The n-type GaN working electrode (W.E.), Pt counter electrode (C.E.), and Ag/AgCl reference electrode (R.E.) were immersed in the electrolyte, which was a 3 wt % mixture of tartaric acid and propylene glycol whose pH was adjusted to 7.0 by adding NH_4OH solution. The potential of the W.E. with respect to that of the R.E. was precisely controlled by a potentiostat.

By applying the anodic bias in the electrolyte, n-GaN surface was oxidized as follows:¹⁹⁾



In this study an anodic bias of 4 V was constantly applied to the W.E. under irradiation of UV light from the topside of the n-GaN sample in order to supply holes, which are minority carriers in n-type GaN. Irradiation light with a wavelength of 360 nm, the wavelength of band edge absorption of GaN, was obtained by passing the light from a xenon lamp through an optical bandpass filter with a FWHM of 10 nm. An optical chopper was used to irradiate the pulsed light, and the anodic reaction proceeded only in the light-on periods between the dark intervals. The pulsed mode is very effective for producing a smooth surface morphology after anodic oxidation, since a density of holes is kept constant at the interface between the electrolyte and GaN via the hole-relaxation during the dark interval.²¹⁾ Horikiri et al. have recently reported that the GaN surface etched by pulsed PEC etching in which the surface roughness strongly depended on the evolution rate of product gasses and the concentration gradient of ions was almost flat.²²⁾ In this study the frequency and duty ratio of pulsed light were set to be 10 Hz and 50%, respectively. The light intensity was adjusted to 5.0 mW/cm² using a light-power meter. The oxide layer formed by the anodic reaction was removed at room temperature by immersion in an alkaline solution consisting of 2.4% tetramethylammonium hydroxide (TMAH). A summary of sample preparation in combination with the initial dry-etching process and PEC process is given in Table I. The thickness of the oxide films formed on GaN surface were evaluated from measurements of the step difference at the boundary between the oxide surface and the oxide-removed surface by an atomic force microscopy (AFM) using an SII Nano Technology Inc. Nano Navi L-trace II. The chemical

properties were analyzed by x-ray photoelectron spectroscopy (XPS) using a Perkin-Elmer PHI 1600 with a monochromatic Al $K\alpha$ source at 1486 eV. All spectra were obtained by adjusting the take-off angle to be 45°.

Before the fabrication of SBDs and MIS capacitors, the etched surface was chemically treated by a buffered hydroxide fluoride (BHF) solution consisting of HF (47%): NH₄F (40%) = 1:5 at room temperature. For the SBDs, Ni/Au (20 nm / 50 nm) electrodes 200 μ m in diameter were deposited directly on the processed surfaces by an electron-beam evaporation. For the MIS capacitors, Al₂O₃ films with thickness of 30 nm was deposited on the dry-etched and PEC-processed surfaces by using an atomic layer deposition (ALD) technique, after which Ni/Au electrodes were formed on the Al₂O₃ films. Current-voltage (I - V) and capacitance-voltage (C - V) measurements were conducted at room temperature to evaluate the effects of the etching process on the electrical properties of the SBDs and MIS capacitors.

3. Results and Discussion

3.1 Photoelectrochemical oxidation and etching

The structural and chemical properties of the oxide films formed by the PEC process were characterized by AFM and XPS techniques. Figure 2 shows a plot of the oxide thickness measured by AFM as a function of total charge density Q_{PEC} , which was given by the time integration of current flow during the PEC process. As expected from Faraday's law, the oxide thickness was linearly controlled by the charge density. After formation of the oxide films, the GaN samples were immersed in the alkaline solution based on TMAH for 1 min to remove the oxide films. After the TMAH treatment, we obtained a smooth GaN surface with a rms roughness only 0.7 nm over a 1 μ m \times 1 μ m area, where any local-etching was not observed. The PEC etching depth measured from the initial surface was about 40% of the oxide thickness before the TMAH treatment for all samples.

Figures 3(a) and 3(b) show the XPS spectra of Ga 3d and N1s core levels, respectively, each comparing the PEC-processed surface and the subsequent alkaline-treated surface. As shown in Fig. 3(a), the peak energies of Ga 3d were 21 and 20.5 eV for samples before and after TMAH treatment, corresponding to Ga-O and Ga-N bonds, respectively. In addition, a broad peak around 23–26 eV originated from the O2s core level was observed for only the sample before TMAH treatment. As shown in Fig. 3(b), the Auger signal of gallium oxide was observed around 397 eV on the PEC-processed surface. After TMAH treatment, a sharp N 1s peak corresponding to Ga – N binding core level was observed with satellite peaks corresponding to Ga Auger signals appeared in the low-energy region. Such features of Ga 3d and N 1s spectra obtained from the TMAH-treated sample were in good agreement with those of the corresponding spectra obtained from the surface of the MOVPE-grown sample.²³⁾

3.2 Electrical properties of Schottky barrier diodes (SBDs)

The electrical properties of SBDs formed on various processed surfaces were compared to evaluate the damage induced on GaN surface. Figures 4(a) and 4(b) show the forward and reverse I - V characteristics of samples formed on the dry-etched surface. As shown in Fig. 4(a), the values of the Schottky barrier height (SBH) ϕ_B^{TE} and the ideality factor n were obtained from the forward characteristics by a thermionic emission (TE) model. The forward current transport observed in the as-grown sample apparently follows the TE model with n value close to unity. On the other hand, the n values of the ICP samples increased with the etching power, and the ϕ_B^{TE} values of those samples were much smaller than that of the as-grown sample. The n and ϕ_B^{TE} values of the ECR sample were not obtained here because there was no longer a linear relation between the voltage and the logarithm of the current density.

As shown in Fig. 4(b), in the reverse bias region an excess leakage current flows even for the as-grown sample, in which current showed nearly exponential dependence on the applied bias. The deviation from the TE model could be well explained by a thermionic field emission (TFE) model,²⁴⁾ in which the reverse current increases with the additional transport due to the tunneling of thermally excited electrons. The theoretical fitting curves based on the TFE model are shown as dashed lines in Fig. 4(b). It was found that the experimental data were well reproduced by the TFE transport characteristics calculated using reasonable SBH values, ϕ_B^{TFE} . These features are consistent with the previous reports on the SBDs formed on homo-epitaxially grown GaN layers.^{25,26)}

The I - V curves of two ICP samples showed rectifying behaviors, but leakage currents were still much larger than those of the as-grown sample, as shown in Fig. 4(b). These results indicate that the dry-etching process induced surface damage on GaN, leading to the degradation of the I - V characteristics of SBDs. The degradation of SBDs after the plasma process has been reported by several groups.²⁷⁻²⁹⁾ One possible explanation for it is the generation of high densities of states that induce Fermi level pinning at Schottky interfaces.

The effects of the PEC process on the electrical properties of SBDs were obviously different from those seen in the dry-etched samples. Figures 5(a) and 5(b) show the forward and reverse I - V characteristics of SBDs formed after the PEC process conducted for the ECR and ICP samples. The I - V curves of the ECR sample showed the ohmic-like behavior having a larger leakage current with a same level of the forward current, as seen in Figs. 4. On the other hand, the clear rectifying behavior was observed on the PEC1 and PEC2 samples. The reverse I - V characteristics showed good agreement with the TFE model and the leakage currents were much smaller than those of the ECR sample. As the Q_{PEC} increased over 230 mC/cm² corresponding to the etching depth over 70 nm, the SBH and n values recovered to the as-grown level, as shown in Figs. 5(a) and 5(b). The effects of the PEC process were noticeable in the ICP samples. The forward and reverse I - V characteristics of the PEC5 and PEC6 samples recovered to the as-grown level by applying smaller Q_{PEC} as compared with

that for PEC2.

In order to further clarify the effects of PEC process, C - V measurements were conducted for the samples prepared with different Q_{PEC} . Figures 6(a) and 6(b) compare the carrier-profiles obtained by C - V measurements on the various PEC samples (whose sample names and corresponding PEC conditions are summarized in Table I). The C - V characteristics of the ECR sample were unmeasurable due to the large-leakage currents, as seen in Figs. 4(a) and 4(b), whereas those of all the other samples fabricated after the PEC process was used could be measured. As shown in Fig. 6(a) for the ECR surface, however, at depths 200 and 145 nm below the surface the carrier densities in PEC1 and PEC2 were lower than that in the as-grown sample. On the other hand, the decrease of the carrier profile was not observed in the measurable range for PEC3 and PEC4 prepared with larger Q_{PEC} . This result suggests that the ECR-RIBE induced defects that changed carrier profiles at sub-micron distances from the surface and that they were gradually removed by the PEC process. The result of conductance measurements (not shown here) also suggested that the increase of the leakage currents around at 0 V resulted in the abnormal C - V characteristics. This kind of damage has been observed in previous work,²⁹⁾ where the bombardment of GaN with ions accelerated by a high-electric field induced defects at sub-micron depths. The present results indicate that the PEC process is useful for removing the surface layer with damage induced by ECR-RIBE. Figure 7 shows a schematic illustration of the sample cross-sections comparing (i) PEC etching depth with (ii) the thickness of the anomalous region or unmeasurable region for three kinds of samples. The anomalous region observed in the carrier profiles was due to the damage induced by the ECR-RIBE process. The thickness of the damaged layer decreased in proportion to the Q_{PEC} that determined the etching depth measured from the initial surface. For example, the etching depth of PEC1 and PEC2 samples were estimated about 30 nm and 70 nm, respectively, from the oxide thickness before the TMAH treatment. As expected, the thickness of the anomalous region decreased with the increase of the etching depth, as seen in Fig. 6(a). Therefore the thickness of initial damaged layer was estimated from the summation of (i) and (ii) to be about 230 nm (Fig. 7).

On the other hand, as shown in Fig. 6(b) for the ICP-RIE samples, there was no anomalous region and no change of the carrier profiles in the samples before and after the PEC process. These results showed that the depth of the damaged-layer induced by the ICP-RIE was small, within the unmeasurable range, and the effects of the PEC process could not be evaluated by C - V measurements on SBDs.

3.3 Electrical properties of metal-insulator-semiconductor (MIS) capacitors

To quantitatively evaluate the effect of the PEC etching process, we fabricated MIS capacitors on dry-etched and PEC-etched surfaces and compared their C - V characteristics. For this purpose, the ICP2 surface prepared with 5-W bias power was used since its induced

damage is the smallest among surfaces prepared under the present ECR-RIBE and ICP-RIE conditions (see Figs. 4). Figure 8(a) compares the C - V characteristics of the MIS capacitors formed on the ICP2 surface with the ideal C - V characteristic calculated using Poisson's equation. The data were obtained at room temperature by changing the measurement frequency from 1 kHz to 1 MHz. As shown in Fig. 8(a), the experimental C - V curves showed large frequency dispersion and slopes less than that of the ideal C - V curve. These results suggest that the high-density of interface states were generated at the MIS interface, where the charging and discharging of electrons were followed by the ac-measurement signal.

As an additional process for the MIS capacitors, post-metallization annealing (PMA) was conducted at 300°C for 2 hours. Annealing has been widely used to improve their electrical properties MIS interfaces. Kaneki et al. have recently reported that PMA was effective for the $\text{Al}_2\text{O}_3/\text{GaN}$ interface, reducing the interface state density to the detection limit of the C - V technique.³⁰⁾ Figure 8(b) shows the C - V characteristics of a MIS capacitor formed on the ICP2 surface after PMA at 300°C. The slope of the C - V curve became steep and the frequency dispersion was reduced, but the deviation between the experimental curves and the ideal curve remained large. In addition to this, a bump-like behavior appeared around 0–1 V, which indicates the existence of a discrete level with relatively high density at the GaN surface. As shown in Fig. 8(c), the slope of C - V curves became much steeper in the PEC6 sample prepared with the PEC etching on ICP2 surface. The PEC etching made the experimental C - V curves are very close to the calculated curve shown in the dashed line, and no bump-like behavior without frequency dispersion were observed. As expected, the PEC process was effective in improving the C - V characteristics of MIS capacitors.

Figure 9 compares the distribution of interface state density of $\text{Al}_2\text{O}_3/\text{GaN}$ interfaces between three samples prepared with different process. These data were obtained by applying the Terman method to the 1-MHz C - V results shown in Figs. 8(a), 8(b), and 8(c). The ICP-etched sample exhibited relatively high state density in the range of $10^{12} \text{ cm}^{-1}\text{eV}^{-1}$. After PMA at 300 °C, the overall distribution decreased and a peak corresponding to a density of $2 \times 10^{12} \text{ cm}^{-1}\text{eV}^{-1}$ appeared around $E_C = -0.55 \text{ eV}$. Peaks like these 0.5–0.6 eV from the conduction band have been reported to be due to the nitrogen vacancy (V_N) acting as a donor-type defect near the surface.¹⁰⁾ These are very consistent with the picture of the underestimation of SBH values, as seen in Figs. 4, which can be explained by the Fermi-level pinning due to the existence of the high-density states. Further reduction of interface state density was achieved by the PEC process with PMA. The state density of the PEC sample was still larger than that of the un-etched sample³⁰⁾ but, with a value in the range of $10^{11} \text{ cm}^{-1}\text{eV}^{-1}$, was smaller than that of any of the other samples prepared in this study. These results show that the PEC process was effective for removing the surface-damaged from GaN and to reducing the interface state density without producing additional defects.

4. Conclusions

We investigated the effect of a PEC etching process on the GaN surface damaged by a dry-etching process. The results of XPS analysis showed that the gallium oxide formed on a GaN surface by a photo-assisted anodic reaction was removed by a TMAH treatment. The extent of such a PEC reaction could be controlled by adjusting the total charge density given by time integration of the anodic currents. I - V and C - V measurements were carried out for various SBDs formed on the ECR-RIBE-, ICP-RIE-, and PEC-processed surfaces. The ECR-RIBE and ICP-RIE samples showed degradation of electrical properties (such as large leakage currents), which were restored by the PEC process to the as-grown level. The effects of the PEC process were quantitatively discussed from the C - V analysis on MIS capacitors. The RIE sample showed large frequency dispersion and a bump-like feature in C - V curves, showing the existence of high-density interface states with defect-related traps in range of $10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. Applying the PEC process on the ICP surface reduced the interface state density by one order of magnitude and resulted in good C - V characteristics with no frequency dispersion and no bump-like feature. These results show that the PEC etching process was effective for removing surface damage from GaN without inducing additional defects.

Acknowledgments

We thank Prof. T. Hashizume and Dr. K. Nishiguchi for fruitful discussions on the C - V analysis of MIS capacitors. This work was supported by the MEXT program for Research and Development of Next-Generation Semiconductor to Realize Energy-Saving Society and by JSPS KAKENHI grants JP16H06421 and JP17H03224.

References

- 1) T. Ueda, M. Ishida, T. Tanaka, and D. Ueda, *Jpn. J. Appl. Phys.* **53**, 100214 (2014).
- 2) T. Kachi, *Jpn. J. Appl. Phys.* **53**, 100210 (2014).
- 3) M. Kuzuhara, J. T. Asubar, and H. Tokuda, *Jpn. J. Appl. Phys.* **55**, 070101 (2016).
- 4) M. Kanechika, M. Sugimoto, N. Soejima, H. Ueda, O. Ishiguro, M. Kodama, E. Hayashi, K. Itoh, T. Uesugi, and T. Kachi, *Jpn. J. Appl. Phys.* **46**, 3 (2007).
- 5) S. Chowdhury, M. H. Wong, B. L. Swenson, and U. K. Mishra, *IEEE Electron Device Lett.* **33**, 41 (2012).
- 6) M. Kodama, M. Sugimoto, E. Hayashi, N. Soejima, O. Ishiguro, M. Kanechika, K. Itoh, H. Ueda, T. Uesugi, and T. Kachi, *Appl. Phys. Express* **1**, 021104 (2008).
- 7) T. Oka, T. Ina, Y. Ueno, and J. Nishii, *Appl. Phys. Express* **8**, 5 (2015).
- 8) Z. Yatabe, J. T. Asubar, and T. Hashizume, *J. Phys. D: Appl. Phys.* **49**, 393001 (2016).
- 9) X. A. Cao, H. Cho, S. J. Pearton, G. T. Dang, A. P. Zhang, F. Ren, R. J. Shul, L.

- Zhang, R. Hickman, and J. M. Van Hove, *Appl. Phys. Lett.* **75**, 232 (1999).
- 10) T. Hashizume and R. Nakasaki, *Appl. Phys. Lett.* **80**, 4564 (2002).
 - 11) T. Mizutani, Y. Ohno, S. Kishimoto, and K. Maezawa, *IEEE Trans. Electron Devices* **50**, 2015 (2003).
 - 12) T. Hashizume and H. Hasegawa, *Appl. Surf. Sci.* **234**, 387 (2004).
 - 13) J.-C. Her, H.-J. Cho, C.-S. Yoo, H.-Y. Cha, J.-E. Oh, and K.-S. Seo, *Jpn. J. Appl. Phys.* **49**, 041002 (2010).
 - 14) N. Lee, M. Lee, W. Choi, D. Kim, N. Jeon, S. Choi, and K. Seo, *Jpn. J. Appl. Phys.* **53**, 04EF10 (2014).
 - 15) B. Molnar, C. R. Eddy, and K. Doverspike, *J. Appl. Phys.* **78**, 6132 (1995).
 - 16) C. Wang, A. J. Appleby, and F. E. Little, *J. Electrochem. Soc.* **148**, A762 (2001).
 - 17) H. . Hong, C. . Chao, J. . Chyi, and Y. . Tzeng, *Mater. Chem. Phys.* **77**, 411 (2003).
 - 18) A. Terano, H. Imadate, and K. Shiojima, *Mater. Sci. Semicond. Process.* **70**, 92 (2017).
 - 19) N. Shiozaki, T. Sato, and T. Hashizume, *Jpn. J. Appl. Phys.* **46**, 1471 (2007).
 - 20) Y. Kumazaki, K. Uemura, T. Sato, and T. Hashizume, *J. Appl. Phys.* **121**, 184501 (2017).
 - 21) J. M. Hwang, K. Y. Ho, Z. H. Hwang, W. H. Hung, K. M. Lau, and H. L. Hwang, *Superlattices Microstruct.* **35**, 45 (2004).
 - 22) F. Horikiri, Y. Narita, and T. Yoshida, *Jpn. J. Appl. Phys.* **57**, 086502 (2018).
 - 23) C. Ozgit-Akgun, E. Goldenberg, A. K. Okyay, and N. Biyikli, *J. Mater. Chem. C* **2**, 2123 (2014).
 - 24) F. A. Padovani and R. Stratton, *Solid State Electron.* **9**, 695 (1966).
 - 25) J. Suda, K. Yamaji, Y. Hayashi, T. Kimoto, K. Shimoyama, H. Namita, and S. Nagao, *Appl. Phys. Express* **3** (2010).
 - 26) H. Imadate, T. Mishima, and K. Shiojima, *Jpn. J. Appl. Phys.* **57** (2018).
 - 27) Z. Mouffak, A. Bensaoula, and L. Trombetta, *J. Appl. Phys.* **95**, 727 (2004).
 - 28) K. J. Choi, H. W. Jang, and J. L. Lee, *Appl. Phys. Lett.* **82**, 1233 (2003).
 - 29) C. Lee, H. Sekiguchi, H. Okada, and A. Wakahara, *Jpn. J. Appl. Phys.* **51**, 076503 (2012).
 - 30) S. Kaneki, J. Ohira, S. Toiya, Z. Yatabe, J. T. Asubar, and T. Hashizume, *Appl. Phys. Lett.* **109**, 162104 (2016).

Table I. Summary of sample preparation

Sample name	Surface preparation	Symbol in figures	Charge density Q_{PEC} (mC/cm ²)	Oxide thickness (nm)
As grown	As grown	×	-	-
ECR	ECR-RIBE processed @ 150 V	○	-	-
ICP1	ICP-RIE processed @ 30 W	□	-	-
ICP2	ICP-RIE processed @ 5 W	△	-	-
PEC1	PEC processed on ECR	●	108	72
PEC2	PEC processed on ECR	●	230	177
PEC3	PEC processed on ECR	●	471	268
PEC4	PEC processed on ECR	●	707	450
PEC5	PEC processed on ICP1	■	173	121
PEC6	PEC processed on ICP2	▲	203	128

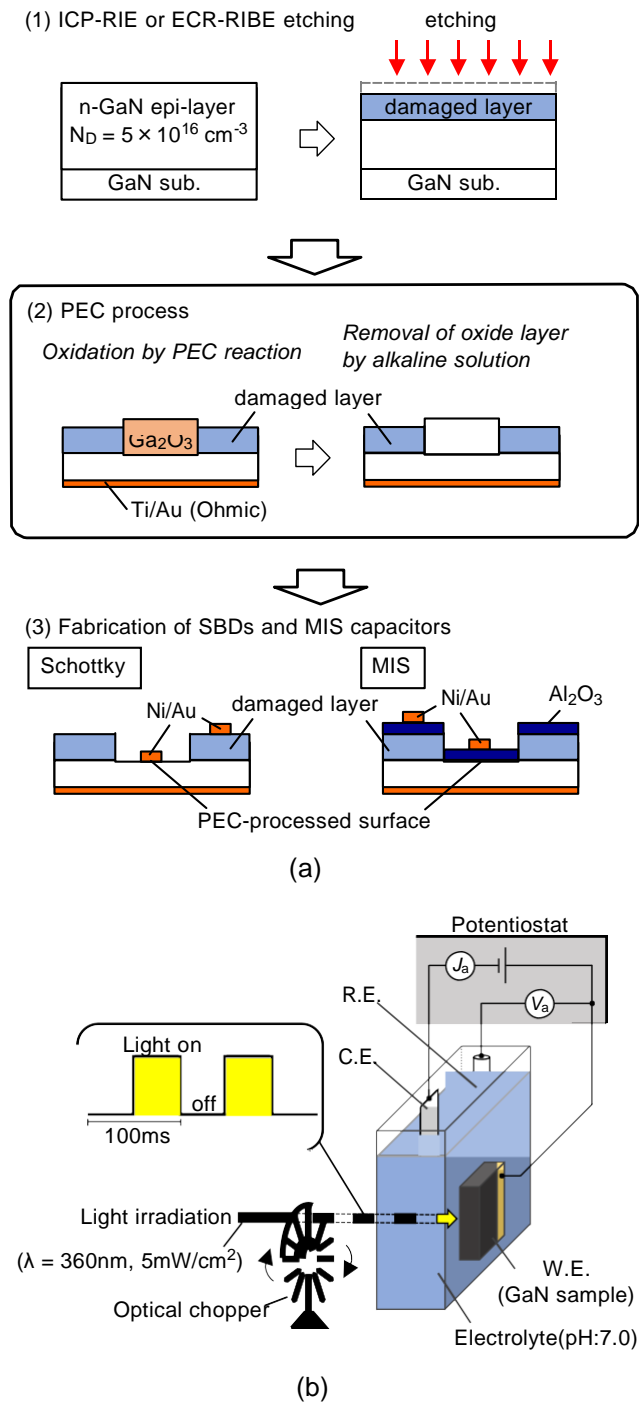


Fig. 1. (Color online) Schematic illustration of (a) experimental procedure and (b) setup of photoelectrochemical (PEC) process.

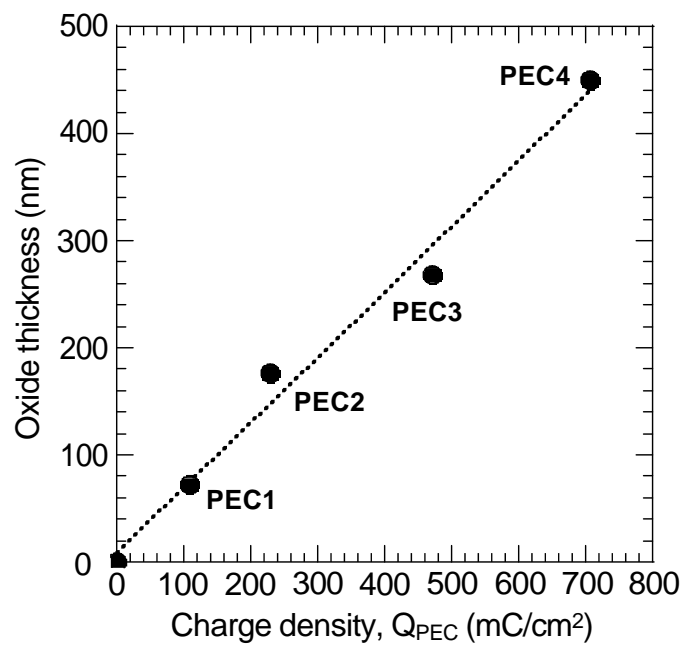
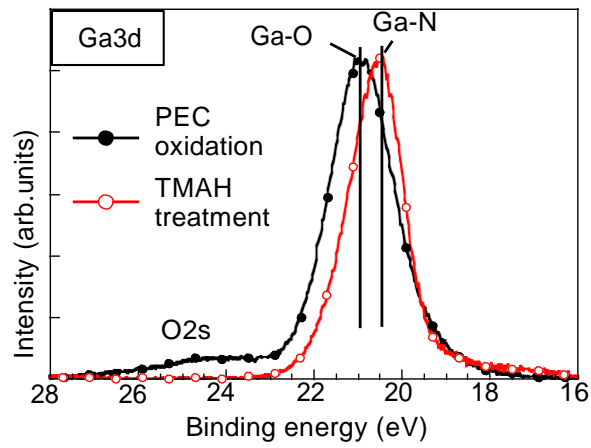
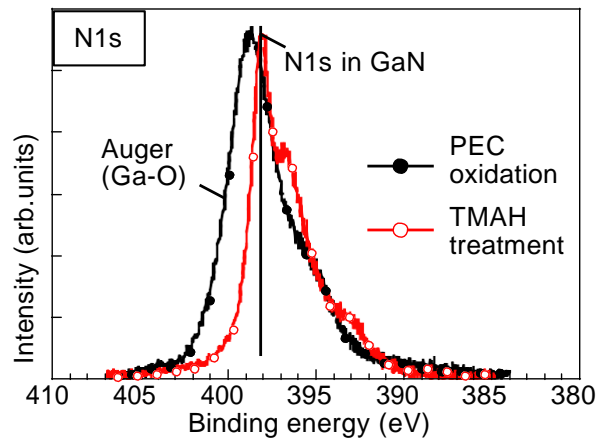


Fig. 2. Correlation between thickness of oxide films formed by PEC reaction and total charge density Q_{PEC} .



(a)



(b)

Fig. 3. (Color online) XPS spectra of (a) Ga 3d and (b) N 1s core levels obtained on the PEC-processed surface before and after TMAH treatment.

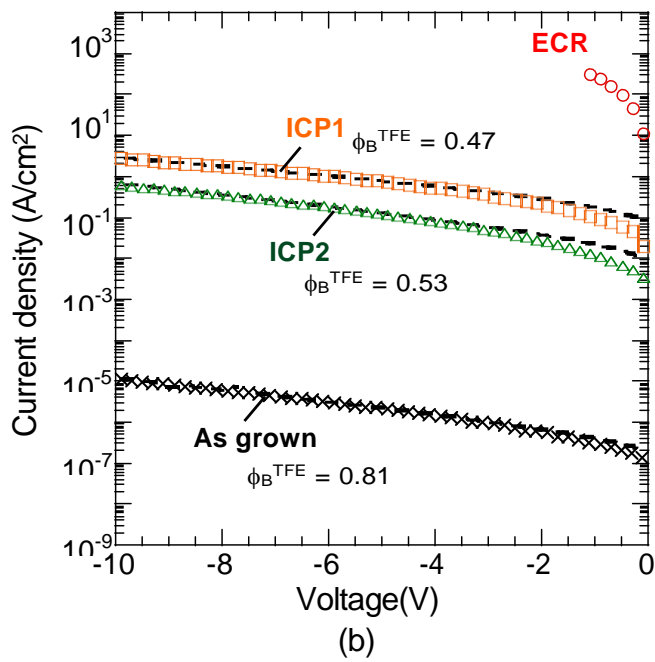
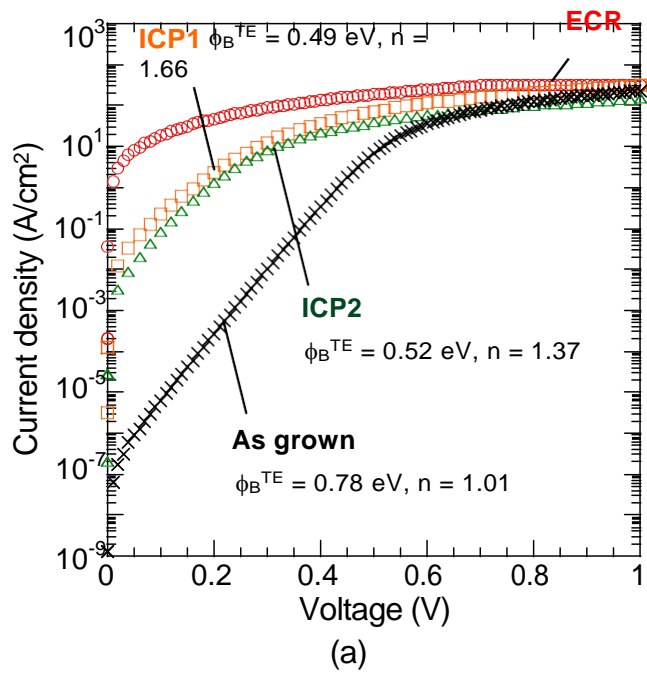


Fig. 4. (Color online) *I-V* characteristics of SBDs formed on ECR-RIBE and ICP-RIE processed surface: (a) forward and (b) reverse characteristics with curves calculated using TFE theory.

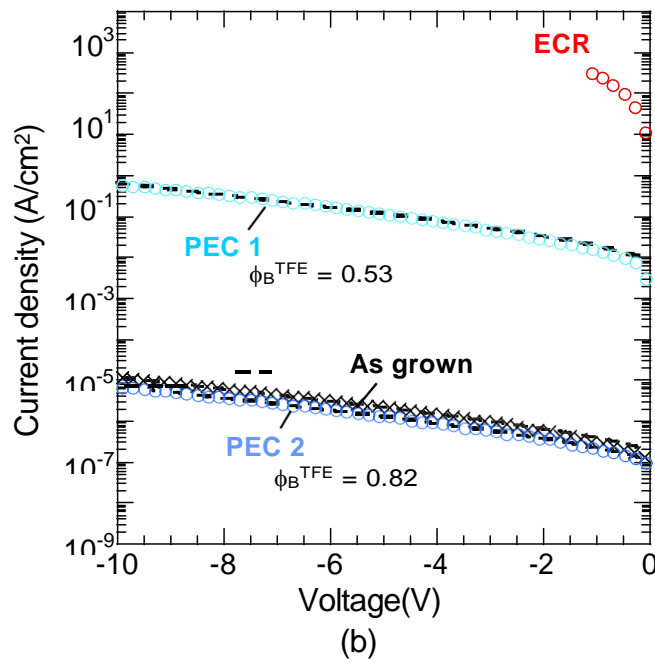
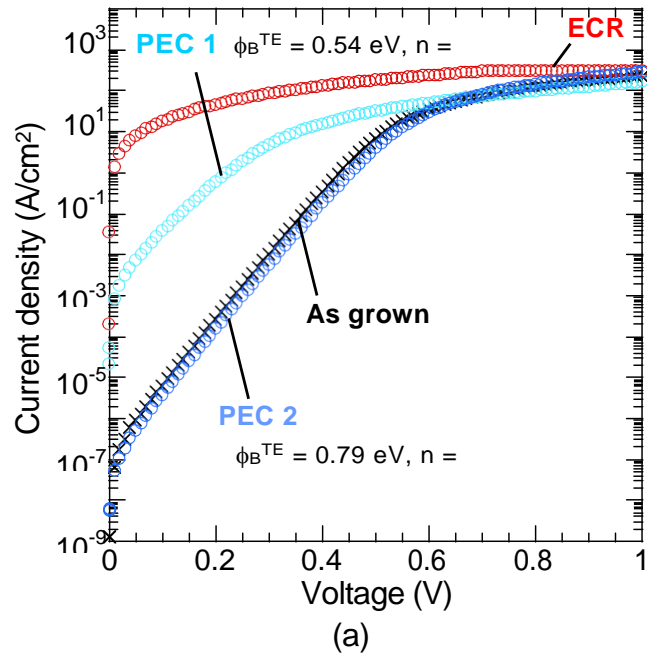


Fig. 5. (Color online) I - V characteristics of SBDs formed on PEC processed surface: (a) forward and (b) reverse characteristics with curves calculated using TFE theory.

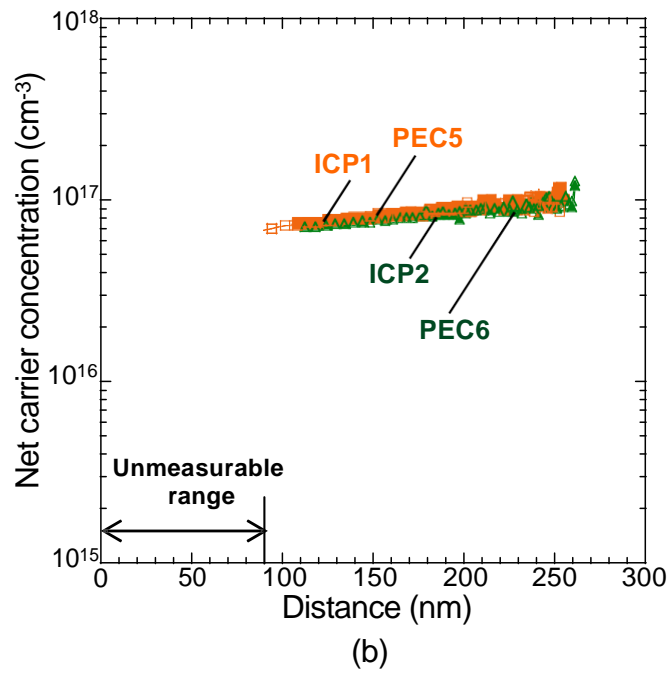
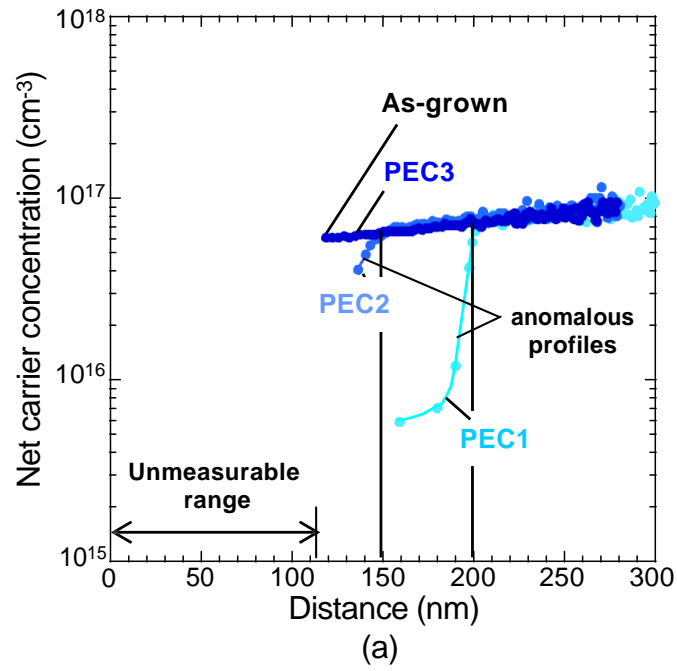


Fig. 6. (Color online) Carrier profiles obtained from C-V measurements on SBDs: (a) PEC-processed ECR samples and (b) ICP samples and PEC-processed ICP samples.

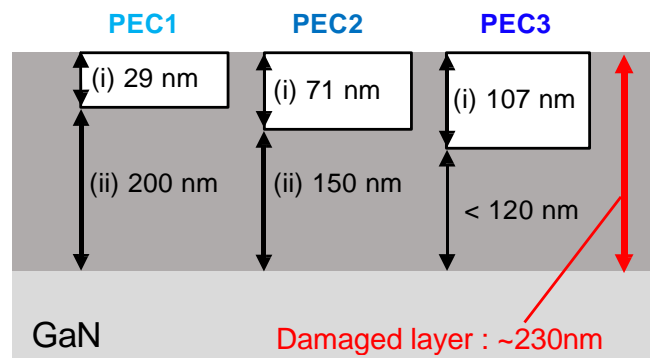
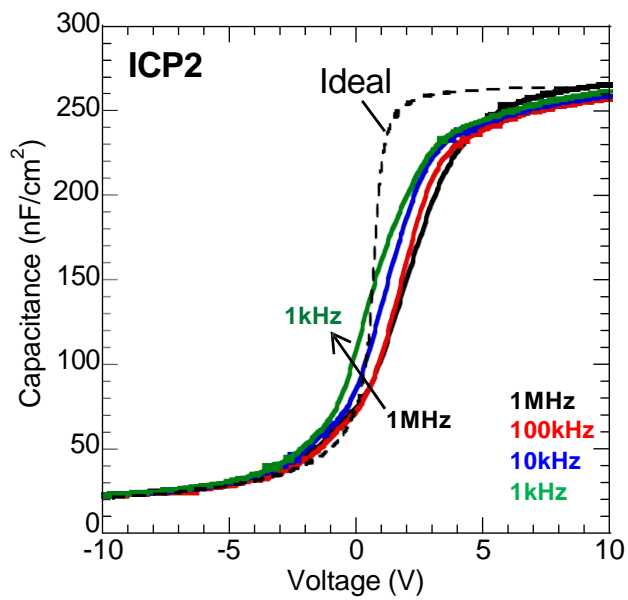
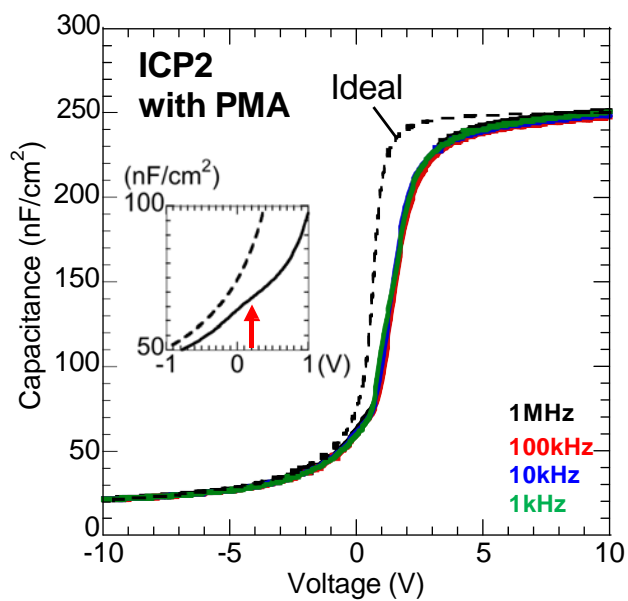


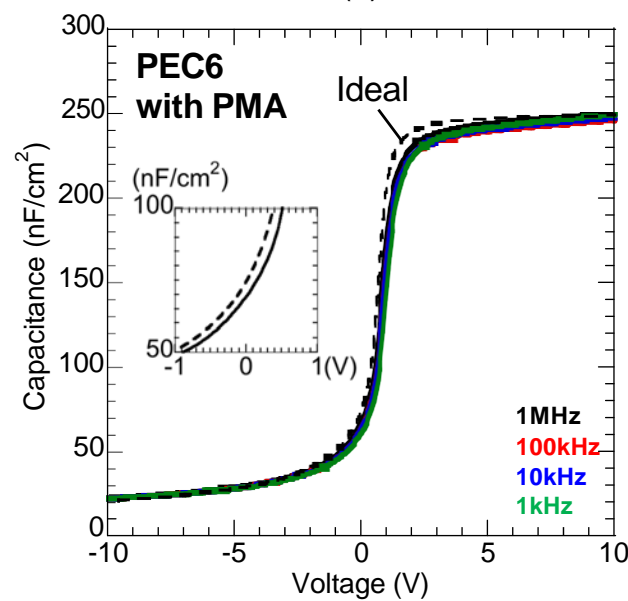
Fig. 7. (Color online) Estimated thickness of layer damaged by the ECR-RIBE process. It was obtained by summation of the thicknesses of (i) PEC etching and (ii) anomalous region in carrier profiles seen in Fig. 6(a).



(a)



(b)



(c)

Fig. 8. (Color online) C–V characteristics of MIS capacitors fabricated on (a) ICP-RIE processed surface (ICP2), (b) ICP2 with post-metallization annealing (PMA), and (c) PEC-processed surface (PEC6) with PMA.

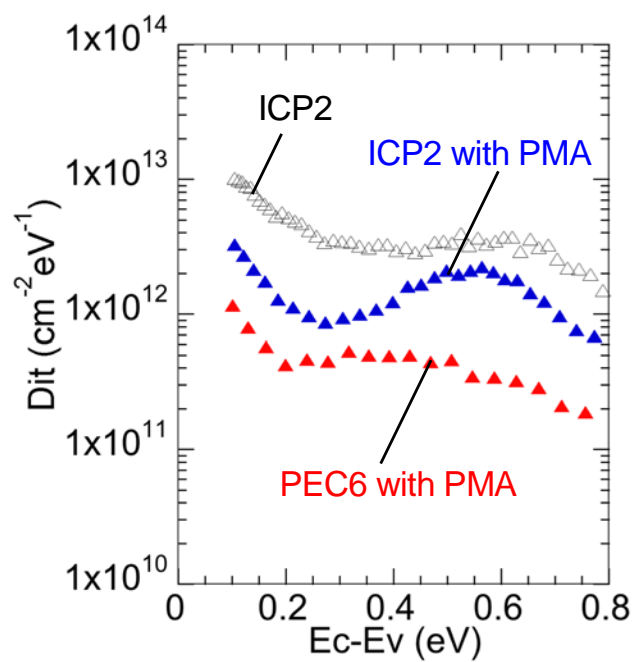


Fig. 9. (Color online) Interface state density (D_{it}) distributions determined by applying the Terman method to 1-MHz C-V results for MIS capacitors.