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Body Bias Generator Design for Ultra-Low Voltage Applications in FDSOI Technology

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Abstract

This thesis presents the derivation and validation processes of analytical models describing the dynamic and steady-state behaviors of CC-CP switched capacitor converters. The effects of FDSOI components in the implementation of such circuits is also addressed, studying their impact as compared to ideal models. Finally, the layout of a CMOS CC-CP in 28-nm UTBB-FDSOI technology is designed and tested against predicted functionality.

Acknowledgements

I wish to extend my thanks to Prof. Moll, whose unrelenting correction process and patience have been fundamental to shape this thesis into something more comprehensible to the casual (and avid) reader.

Also, I want to thank Dr. Barajas for his help and teachings during the layout design process. It would have been unfeasible otherwise.

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1. Introduction

1.1. Technological trends and FDSOI

Technological improvements, industrial trends and energy efficient management have always driven the direction of microelectronic design.

The reduction in size of microelectronic components, in an endeavor to achieve ever larger system complexity has merited, almost since its conception, a defined trend that became law (Moore's Law). In an effort to attain higher functioning speeds and ever decaying power consumption in digital circuits, billions of dollars are spent each year to reduce size, improve performance and reduce the cost of fabrication of transistors.

A reduction in transistor size is, however, accompanied by a myriad of challenges. Namely, a reduction in the channel length of MOS transistors leads to an increase of the electrical fields formed within the channel. As a consequence, the maximum voltage the device can withstand (breakdown voltage) is reduced with each technology reduction.

Also, as transistor size is reduced, more complex systems with a higher count of transistors can be implemented in the same die area. This leads to an overall increase of the power consumption, both dynamic and static.

Scaling the voltage supply then becomes a necessity both to allow functionality without surpassing the breakdown voltage and to reduce power consumption. In digital circuits, this reduction of the voltage supply produces a decreased Voltage overdrive (Vgs-Vth), which increases the equivalent switching resistance of transistors and limits the overall speed of the circuit.

To overcome these limitations, transistors must then be manufactured with lower Threshold voltages. But this presents other problems.

Both the reduction in channel length to sub-micron scales and the reduction of the Threshold voltage can significantly impact power losses due to leakage currents.

To overcome these limitations accompanied by size reduction, the last decades have seen the emergence of new technologies such as FIN-FETs and FDSOI transistors, with new "architectures" that provide solutions to the aforementioned problems.

FDSOI transistors in particular benefit from the addition of a fourth terminal that can be used to modify some of the properties of the transistors previously fixed during the manufacturing process.

The addition of an insulating layer below the channel limits the width of the junctions' depletion layer and allows the use of an undoped channel (Fig. 1.1), significantly improving short-channel effects, leakage currents and variations of the Threshold voltage along the channel. The reduction of junctions' depletion layer width decreases junction capacitances as well, reducing dynamic power consumption. At the same time, the architecture of FDSOI transistors allows biasing through a fourth terminal. Controlling the voltage applied to this fourth terminal, the Threshold voltage can be modified outside the manufacturing process to a certain degree. This, in turn, can be used to alter the operational speed, current gain, leakage current and consumption in idle states in low voltage circuits or otherwise. [1][2][3]

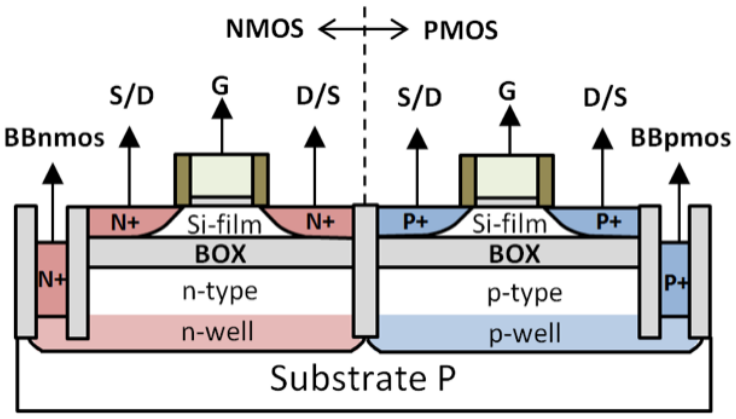


Fig. 1.1: Flipwell FDSOI transistor structure. The flipwells allow the NMOS and PMOS transistors to be biased through the BBnmos and BBpmos terminals with positive and negative voltage values respectively (forward body biasing). [4]

1.2. Ultra-Low Voltage and Energy Harvesting

On the other hand, with various industrial sectors (automobile, medical, weather) benefiting from the technological trend emerging from the IoT, some estimations point to a doubling in IoT nodes in the following five years (Fig. 1.2).

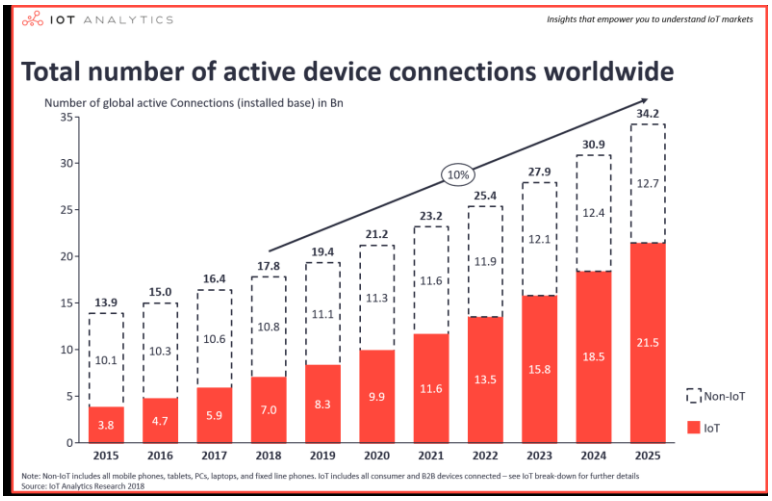


Fig. 1.2: Prospective increase in IoT devices.[5]

The philosophy behind IoT nodes (either remote locations or minimum human intervention once installation is complete) goes hand by hand with minimum power consumption either by having low frequency of operation (the device is active only for short periods of time during long inactive periods), and/or by consuming the minimum possible power during operation, so as to maximize the available active life of the device.

This, in turn, leads to the potential application of energy-harvesting solutions that could be used to either completely power the device or extend its available active life before having to relay to human intervention to either change the battery or the device.

Energy harvesting, on the other hand, tends to produce low voltages, low power output, or both, which might not be readily suitable to power any active device, requiring the presence of intermediate power converters or voltage multipliers.

Power converters have been a key element of electronic design since its conception. However, their reliance on inductors has been and, in some ways, continues to be, a problem for microelectronic design, given their poor performance in integrated circuit. Instead, inductorless power converters (switched-capacitor converters) have become one of the most widely used devices for this purpose in IC design. Switched-capacitor converters have been proven to exhibit similar properties and behavior to inductive power converters.

1.3. Motivation and outline of the thesis

The present study is part of research project funded by the MICINN ([Together] " DISPOSITIVOS, CIRCUITOS Y ARQUITECTURAS FIABLES Y DE BAJO CONSUMO PARA IOT", TEC2016-75151-C3-2-R (2016-2019)), where low voltage supply circuits are the focus of study, with implementation in FDSOI technology.

To improve or even allow the complete functionality of such circuits, a Back-biasing voltage higher to that of the supply voltage is needed, to be applied to the fourth terminal of the FDSOI transistors, thus decreasing the Threshold voltage of the transistors.

The objective of this study was to originally design a Cross-Coupled Charge Pump (CC-CP) [6] to perform this functionality. In the process of studying and analyzing the behavior of such circuits, a dynamical and steady-state models were derived to guide the design of such circuits in FDSOI technology (and otherwise).

As such, this thesis is a compendium of the models derived and the experiments followed to establish the validity of such models, presenting some design guidelines and a final design both with schematic and layout extraction.

This thesis is the culmination of a year-long project initiated during the first Semester of the academic year 2018-2019 through the Introduction to Research subject. Part of this work has been accepted for publishing as posters in two international conferences.[7][8]

2. Overview of the Cross-Coupled Charge Pump circuit

2.1. Principles of Switched-Capacitor Converters

Power converters are ubiquitous components in most electronic systems, portable or otherwise, tailoring power management requirements between energy sources and circuits.

Traditionally, inductive power converters (IPC), in which the temporary energy storage between switching phases is carried out by inductors, have dominated the field of power electronics. Most courses on the subject of power electronics still focus solely on these types of converters.

DC-DC IPC have been extensively studied and modelled for the better part of the last century. They provide ideal power efficiencies of 100 %, step-up and step-down capabilities and can provide continuous Vout/Vin conversion ratios based on switching frequency.

However, as VLSI technologies continue to scale down, implementation of power converters with inductive components becomes challenging and expensive, given their complex scalability (reduced Q factor, parasitic components, bulk and adjacent vias coupling).

For this reason, and given the ease of implementation of capacitors in VLSI technologies, Switched-Capacitor converters can become the better alternative in power management of IC systems.

In Switched-Capacitor Converters (SCC), capacitors become the temporary energy storage components. Similarly to IPC, SCC use switches controlled by different clock phases to redirect the flow of energy between components at different phases of operation.

SCC also present step-up and step-down capabilities, but their conversion ratios are intrinsically tied to the topology of the circuit, and is presented in ratios of integer numbers (i.e. Vout/Vin→ 2/1, 3/1, 4/3, 5/8…)[9].

On the other hand, the intrinsic losses associated with the charging or discharging of capacitors limit even the ideal efficiency of these converters, although practical applications show their feasibility [10].

Fig. 2.1 shows a Switched Capacitor voltage doubler in the equivalent topology of a Dickson Charge Pump. During phase 1, the top plate of capacitor C is connected to the input voltage source, and receives some charge. During phase 2, the bottom plate of capacitor C is connected to the input voltage source. Cload receives some charge from capacitor C at a voltage that is the superposition of Vin and the voltage across the terminals of capacitor C. With enough cycles of operation, Cload is eventually charged to 2*Vin.

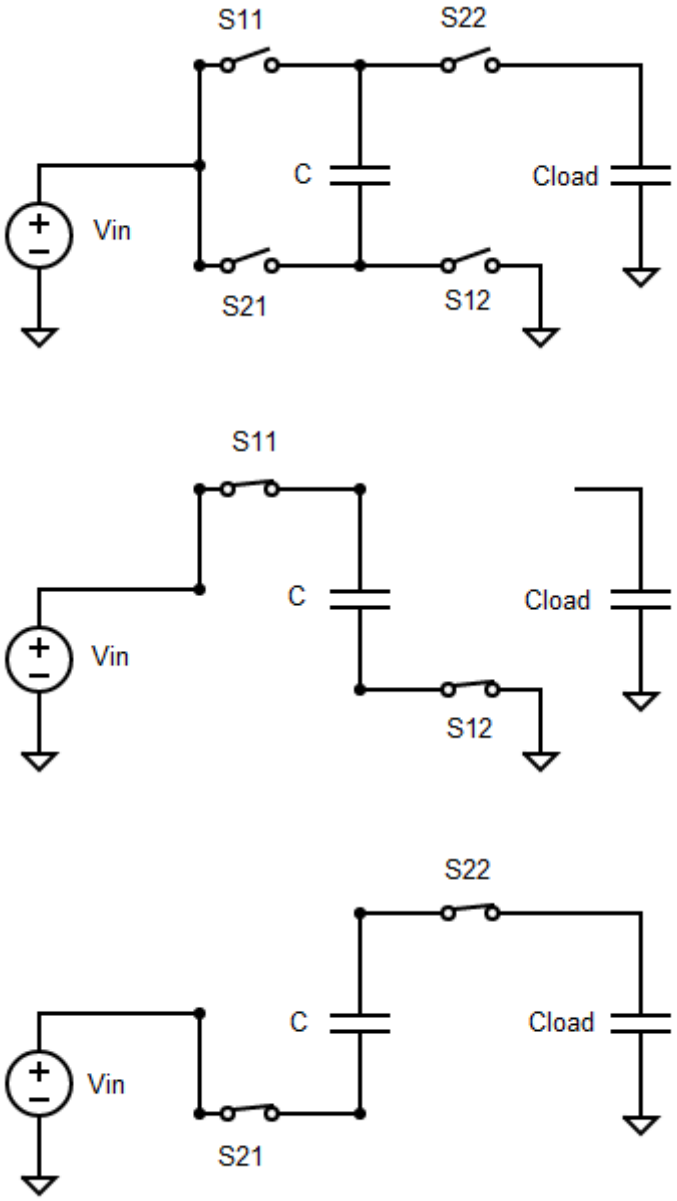


Fig. 2.1: 1-stage equivalent Dickson Pump (charge doubler). A) General Topology. b) Phase 1, C charging. C) Phase 2, C discharging with boosted voltage.

A Cross-Coupled Charge Pump (CC-CP) is a type of switched-capacitor converter, similar in operation to a Dickson Charge Pump. A CC-CP is an inductorless DC-DC boost converter that provides a voltage at the output N times higher than the voltage at the input, where N is an integer that depends on the topology (namely, on the number of stages of the circuit): The voltage at the output is boosted to n+1, where n is the number of stages of the circuit. It follows that:

$$N = \frac{V_{out}}{V_{in}} = n + 1 \qquad (1)$$

The functionality of a CC-CP (Fig. 2.2) is based on transfers of charge of ever-increasing voltage potentials between capacitors through a series of resistive paths governed by clock-controlled switches. These properties are more or less shared by all

switched-capacitor converters, and the analysis of the circuit follows the foundations of SC circuit analysis, with certain peculiarities.

Namely, the gate of the MOS transistors implemented as switches are directly tied to the top plate of the fly-capacitors. As subsequent analysis will show, this guarantees that the Vgs is constant across all transistors during circuit operation, meaning that the clock amplitude must not be tailored for stages where VD and VS are higher than the clock voltage.

2.2. Operation of the CC-CP

Fig. 2.2 depicts a 1-stage CC-CP. The circuit comprises 4 MOSFETs (2 NMOS and 2 PMOS) and 2 fly capacitors. Two non-overlapping clock signals are connected to the bottom plates of the fly capacitors. Each clock is active high during 50 % of the period of operation of the circuit. The clocks are operating at the same frequency, but with a 180 º phase difference (Fig. 2.3).

The MOSFET transistors are implemented to operate as resistive switches. They present a large off resistance and a comparatively low on resistance. The switching is controlled by the aforementioned clock signals, by connecting the top plate of the capacitors to the gate of the transistors lying opposite to them.

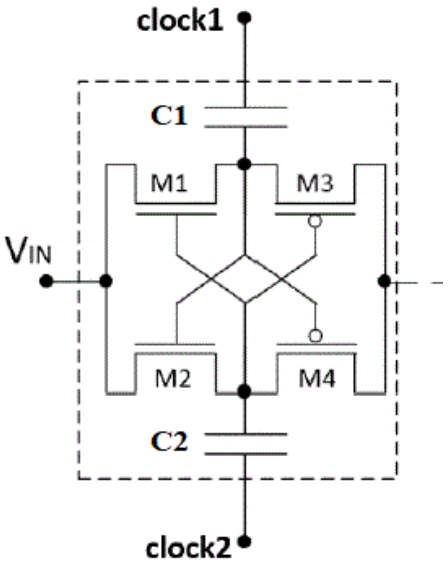


Fig. 2.2: 1-Stage CC-CP

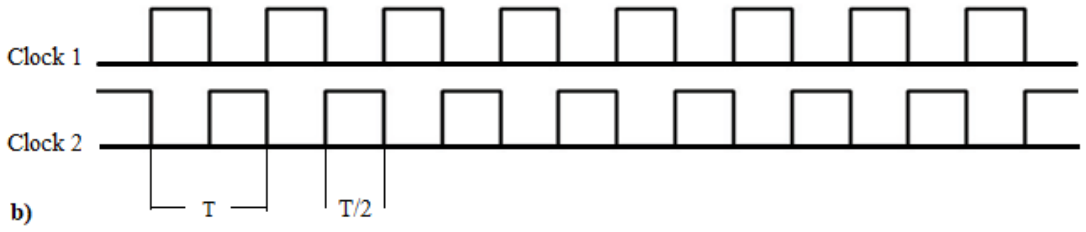


Fig. 2.3: Clock signals governing the behavior of CC-CP

When Clock 2 has a rising transition, the top plate of capacitor C2 will experience an initial voltage increase equal to the clock source amplitude, Vclk. This increase in voltage produces a decrease in the equivalent resistance of the NMOS transistor M1 lying opposite to C2 and, at the same time, increase the resistance of the PMOS transistor M3.

At the same time, as Clock1 has a falling transition, the top plate of capacitor C1 sees a decrease in voltage that produces the opposite effect on the NMOS transistor M2 (increasing its resistance) and on PMOS transistor M4 (producing a decrease in its resistance). This combined effect generates a series of high and low resistance paths that connect the capacitors to different nodes in the circuit, as depicted schematically in the form of open and closed switches in Fig. 2.4, depicting a 2-stage CC-CP.

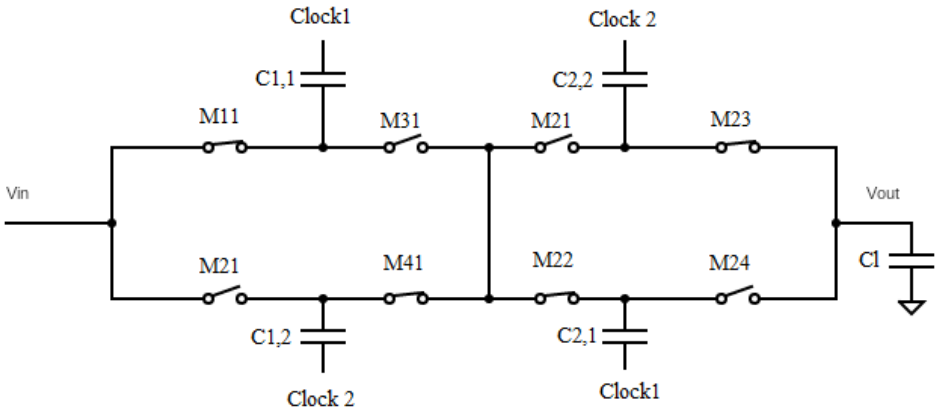


Fig. 2.4: 2-Stage CC-CP schematic representation. Clock 2 is active high.

When a path of low resistance is created between two capacitors, the capacitor the bottom plate of which is connected to a clock which has experienced a rising transition will have, at the top plate, a voltage equal to the clock signal amplitude plus the voltage across the terminals of the capacitor. This allows the capacitor with its bottom plate connected to an inactive clock to be charged, in subsequent periods, to a higher voltage than the preceding capacitor. Thus, as previously stated, the circuit acts as a boost-converter.

Assuming that the impedances of the open switches are much higher than the impedances of the closed switches, from a current perspective, the circuit operates as a sequence of transfers of charge between capacitors. These charge transfers can be modeled as simple RC circuits once the pertaining topologies have been identified.

Observing Fig. 2.4, it is possible to identify different resistive paths between:

- The input voltage source and capacitor C1,1.
- Capacitor C1,2 and capacitor C2,1
- Capacitor C2,2 and the load capacitor.

Careful consideration can lead to the observation that the last two resistive paths give rise to the same topology. Thus, a maximum of two different topologies arise during the circuit operation. These topologies are depicted in figure 5.

The first topology (Fig. 2.5.a) corresponds to the charging of the first fly capacitor by the input voltage source. In this topology, resistance R1 is comprises a single NMOS transistor. The second topology (Fig. 2.5.b) corresponds to the charging/discharging of any adjacent pair of capacitors. In this topology, resistance Ri comprises a series combination of 1 NMOS and 1 PMOS transistor. The final stage, where Ci+1 corresponds to the load capacitor Cload presents a resistance Ri formed by a single PMOS transistor (see Fig. 2.4)

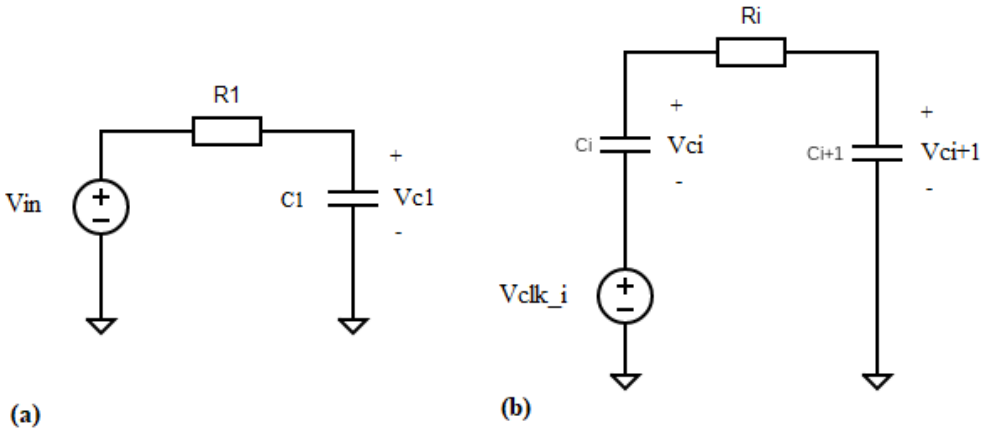


Fig. 2.5: a) Charging topology of the first fly-capacitor. B) Discharging topology of fly-capacitor i, charging topology of fly-capacitor (i+1).

These topologies can be easily analyzed through Kirchoff Voltage Law (KVL) in the frequency domain to obtain equations that relate the changes in the fly capacitors voltage through charge transfer during one period of operation.

2.3. Charge transfer equations:

In order to analyze the different topologies, various assumptions are taken with the aim of simplifying the procedure.

- The clocks are ideal and non-overlapping, with a period T and a duty cycle of 50 %.
- The clock signal amplitude (Vclk) is equal to the amplitude of the input voltage source (Vin).
- The MOSFETs are modeled as ideal switches in series with linear resistors.
- All fly-capacitors present the same capacitance. The load capacitor is also equal to the rest.
- There are no losses nor parasitic elements (These will be explored later).

These considerations lead to the ideal circuit depicted in Fig. 2.6, where the CC-CP has been simplified to depict a single path of current flow instead of the crossed, interwoven circuit with two parallel current paths.

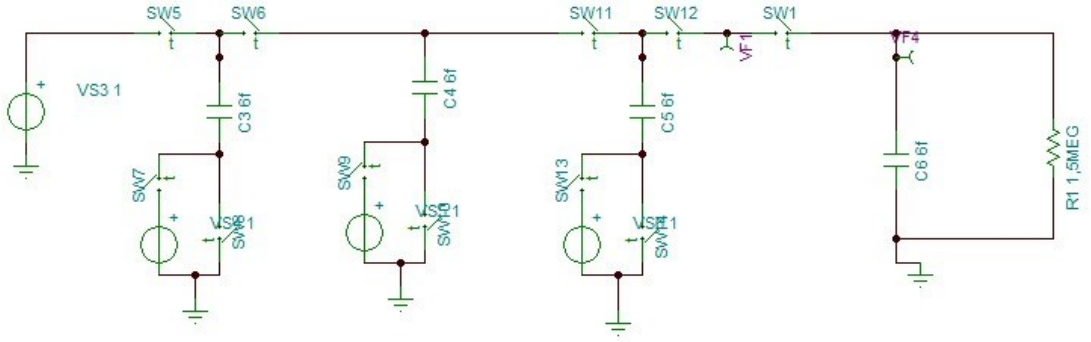


Fig. 2.6: Schematic representation of one branch of a 3-stage CC-CP with resistive load.

With these considerations in mind and the topologies depicted in Fig. 2.5, reflecting the different sub-circuits in the Laplace domain, KVL can be applied. Focusing on the first topology we obtain:

$$-\frac{V_{in}}{s} + I_1\left(R_1 + \frac{1}{Cs}\right) + \frac{V_1}{s} = 0 \tag{2}$$

$$I_1(s) = \frac{V_{in} - V_1}{R_1} * \left(\frac{1}{s + \frac{1}{R_1 C}}\right) \tag{3}$$

$$i_1(t) = \frac{V_{in} - V_1}{R} * e^{-\frac{t}{R_1 C}} \tag{4}$$

Analyzing the second sub-circuit yields the following results:

$$-\frac{V_{in}}{s} - \frac{V_i}{s} + I_2 * \left(R_i + \frac{1}{Cs} + \frac{1}{Cs}\right) + \frac{V_{i+1}}{s} = 0 \tag{5}$$

$$I_2(s) = \frac{V_{in} + V_i - V_{i+1}}{R_i} * \frac{1}{s + \frac{2}{R_i C}} \tag{6}$$

$$i_2(t) = \frac{V_{in} + v_i - v_{i+1}}{R_i} * e^{-\frac{2t}{R_i C}} \tag{7}$$

If we integrate both equations, knowing that each sub-circuit is operative for T/2:

$$\Delta Q_1 = \int_0^{\frac{T}{2}} i_1(t) * dt = \int_0^{\frac{T}{2}} \frac{V_{in} - V_1}{R_1} * e^{-\frac{t}{R_1 C}} * dt = C(V_{in} - v_1)\left(1 - e^{-\frac{T}{2R_1 C}}\right) \quad (8)$$

$$\Delta Q_i = -\int_0^{\frac{T}{2}} i_2(t) * dt = -\int_0^{\frac{T}{2}} \frac{V_{in} + v_i - v_{i+1}}{R_i} * e^{-\frac{2t}{R_i C}} * dt = -\frac{C(V_{in} + v_i - v_{i+1})}{2}\left(1 - e^{-\frac{T}{R_i C}}\right) \quad (9)$$

These equations represent the amount of charge that is transferred into capacitor 1 and from capacitor i respectively.

Alternatively, the equations can be expressed as voltage variations:

$$\frac{\Delta Q_1}{C} = \Delta V_1 \quad (10)$$

$$\frac{\Delta Q_2}{C} = -\Delta V_i = \Delta V_{i+1} \quad (11)$$

$$\Delta V_1 = (V_{in} - v_1)\left(1 - e^{-\frac{T}{2R_1 C}}\right) \quad (12)$$

$$\Delta V_{i+1} = -\Delta V_i = \frac{(V_{in} + v_i - v_{i+1})}{2}\left(1 - e^{-\frac{T}{R_i C}}\right) \quad (13)$$

These two equations represent the increase or decrease in voltage across the terminals of a capacitor after one semi-period of operation.

They depend on the clock/input voltage amplitude, the current voltage across the terminals of the capacitors involved and a constant involving an exponential that depends on circuit parameters.

This last constant parameter is not equal between equations (12) and (13). In intermediate topologies, the discharging and charging capacitors form a series association (equation 5). Under the assumption that all capacitors are equal, the equivalent capacitance of intermediate stages is reduced to C/2. It is of interest to have equal RC time constants for all topologies, so the exponential parameter can be simplified in subsequent analysis.

Thus, notice that by reducing the resistance of the first stage R1 to half the value of Ri ($R1 = Ri/2$), equation (12) becomes:

$$\Delta V_1 = (v_{in} - v_1)\left(1 - e^{-\frac{T}{2\frac{R_i}{2}C}}\right) = (v_{in} - v_1)\left(1 - e^{-\frac{T}{R_i C}}\right) \quad (14)$$

If we design the resistance of the first stage to be R1=Ri/2 we can ensure some mathematical simplifications that facilitate further analysis. At the same time, the equivalent resistance of the rest of stages must be the same. ($R_i = R, \forall\, i \neq 1$).

That way, the parameter

$$\left(1 - e^{-\frac{T}{R_i C}}\right)$$

is the same for both equations (13) and (14). Note that, given the periodic nature of the circuit, this term, equal for all topologies, becomes a constant that depends exclusively on design parameters. This constraint massively simplifies the developing of the following analysis.

Given that this term appears through most part of the analysis and that once the equivalent resistance is fixed, the term becomes constant (under the assumed constraints), the R_i notation will be dropped from now on, and will be substituted by simply R.

$$\left(1 - e^{-\frac{T}{RC}}\right)$$

3. Discrete-Time State-Space Model

3.1. Procedure to derive the Discrete-Time State-Space Model

If the values of the voltage across the different capacitors' terminals are known at a given period kT, the equations above derived allows us to determine the value at period (k+1)T. Each capacitor experiences a charging and a discharging during a period of operation of the circuit. For an arbitrary fly-capacitor *i* (see Fig. 2.5), we can write:

$$V_{Ci}\big((k+1)T\big) = V_{Ci}(kT) + \Delta V_{charging} - \Delta V_{discharging} \tag{15}$$

The charging and discharging terms correspond to equations (13) and/or (14) and, as above stated, depend exclusively on design parameters in the form of a constant term and, more importantly, on the current state of the circuit.

If the different capacitor voltages at a given time are treated as state-variables, given some initial conditions, these equations allow us to predict the evolution of the state-variables in time.

These state-variables present a continuous time evolution, but the discontinuities introduced by the switching nature of the circuit would severely impact the linearity of a continuous time model. It is, therefore, much simpler to conceive the state-variables evolving in discrete increments of time.

This leads to the foundations of a discrete-time state-space entity that can predict the dynamics of the circuit.

Consider a time-invariant system as represented by the generalized discrete-time state-space equations of the form:

$$\begin{aligned} \boldsymbol{X}[K+1] &= A * \boldsymbol{X}[K] + B * U[K] \\ Y[K] &= C * \boldsymbol{X}[K] + D * U[K] \end{aligned} \tag{16}$$

Where:

- X[·] is the state vector, in this case representing the fly- and load capacitor voltages. It is an (2*n+1)*1 vector, where n is the number of stages.
- Y[·] is the output vector. In this case, a scalar (1*1 vector) representing the load capacitor (output) voltage.
- U[.] is the input vector. The inputs signals are those of the input voltage source and the clocks. Under the assumptions presented (the input voltage and clock amplitudes are equal) this is a 1*1 vector, constant in time.
- A[·] is the state matrix, relating the current values of the state-variables to those of the next period. It is an N*N matrix.
- B[·] is the input matrix, an N*1 matrix relating the current value of the input vector to the state of the next period. Since U[·] is a constant scalar, B

comprises constant parameters. In fact, both A and B are constant, time-invariant matrixes.

- C[·] is the output matrix, a 1*N matrix.
- D[·] is the feedthrough matrix. In this case it is a zero matrix.

We wish to derive such a compact expression so as to be able to better analyze the properties of this circuit. We analyze a single branch of a CC-CP (Fig. 2.6) to showcase the procedure.

In order to do so, we divide each period into two separate sub-periods with their respective sub-circuits as depicted in Fig. 3.1. The components of the state vector are here represented as Vc1, Vc2, Vc3 and Vout.

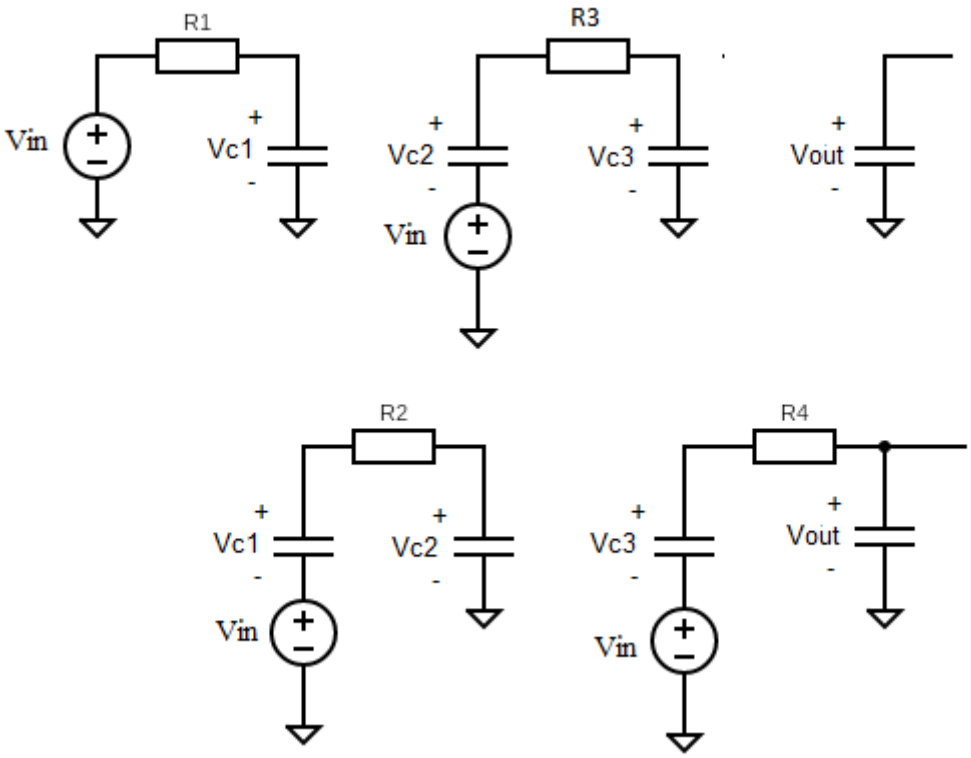


Fig. 3.1: Circuit topologies during the first semi-period of operation. Bottom) Topologies during the second semi-period.

We take as an example the voltage variations of capacitor C1 (Vc1) during the first semi-period of circuit operation (Fig. 3.1.top). It can be assumed that Capacitor C1 already has some charge stored, and that the circuit is at its *Kth* period after start-up. Capacitor C1, connected to the input voltage source, will gain some additional charge. After the first semi-period has been completed, the voltage across the terminals of C1 will be:

$$V_{C1}\left[K+\frac{1}{2}\right] = V_{C1}[K] + \Delta V_{C1} \tag{17}$$

As per equation (14):

$$V_{C1}\left[K+\frac{1}{2}\right] = V_{C1}[K] + \ (V_{in} - V_{C1}[K])\left(1 - e^{-\frac{T}{RC}}\right) \quad (18)$$

And, rearranging terms for ease of manipulation:

$$V_{C1}\left[K+\frac{1}{2}\right] = V_{C1}[K](1-a) + \ a * V_{in} \quad (19)$$

Where we have written $a = (1 - e^{-\frac{T}{RC}})$

We now take the same approach for capacitor C1 during the second semi-period of operation. In this instance, C1 is connected to C2 and will relay some charge onto it. That is, C1 will partially discharge and its voltage will decrease.

$$V_{C1}[K+1] = V_{C1}\left[K+\frac{1}{2}\right] - \Delta V_{C1} \quad (20)$$

As per equation (13):

$$V_{C1}[K+1] = V_{C1}\left[K+\frac{1}{2}\right] - \frac{\left(V_{in} + V_{C1}\left[K+\frac{1}{2}\right] - V_{C2}\left[K+\frac{1}{2}\right]\right)}{2}\left(1 - e^{-\frac{T}{RC}}\right) \quad (21)$$

Rearranging terms:

$$V_{C1}[K+1] = V_{C1}\left[K+\frac{1}{2}\right]\left(1-\frac{a}{2}\right) + V_{C2}\left[K+\frac{1}{2}\right] * \frac{a}{2} - V_{in} * \frac{a}{2} \quad (22)$$

Now we can substitute the term $V_{C1}\left[K+\frac{1}{2}\right]$ by the expression derived in equation (19).

$$V_{C1}[K+1] = (V_{C1}[K](1-a) + \ a * V_{in})\left(1-\frac{a}{2}\right) + V_{C2}\left[K+\frac{1}{2}\right] * \frac{a}{2} - V_{in} * \frac{a}{2} \quad (23)$$

The same procedure can be done for C2. That is, obtain an expression relating $V_{C2}\left[K+\frac{1}{2}\right]$ to $V_{C2}[K]$, and substitute it in all the instances of equations of the type $V_{Ci}[K+1]$. Thus, for each capacitor in a circuit with 2n+1 capacitors an expression is obtained of the form:

$$V_{Ci}[K+1] = ai1 * V_{C1}[K] + ai2 * V_{C2}[K] + \cdots + aii * V_{Ci}[K] + \cdots + aiN * V_{CN}[K] + bi * V_{in} \quad (24)$$

Where the different aij coefficients are the constant components of the ith row of the state matrix and the bi coefficient is the constant component of the ith row of the input matrix.

If we wish to represent the output of the state-space system as the voltage of the load capacitor, following equation (16), consider the following:

$$Y[K] = V_{CN}[K] = [c_1 \ c_2 \ \dots \ c_N] * \begin{bmatrix} V_1[K] \\ V_2[K] \\ \dots \\ V_N[K] \end{bmatrix} \quad (25)$$

It is readily observed that C is a vector where only the ith component of interest is 1, the rest being zero.

$$C = [0\ 0\ \ldots\ 1]$$

3.2. Parasitic capacitances effects on the dynamic model

Let's consider now the case in which the circuit presents some parasitic components; namely, parasitic capacitances along the main capacitors forming the charge pump.

Fig. 3.2 depicts a cross-section of capacitor implemented with VLSI technology, as well as the main parasitics that arise in such implementation. These are not to be taken as accurate representations of the parasitic capacitances arising in FDSOI technology, but as simple indications of the types of parasitics that can arise.

The following analysis ignores for the moment the bottom plate parasitic capacitances which, despite generally being the largest, an initial analysis and circuit simulation show little to no impact on either the dynamic or steady-state models. However, bottom plate parasitic capacitances do present effects that can alter real implementations. Namely, they introduce loading effects at the output of the clock drivers. This loading effect impacts both the power consumption of the drivers and the clock waveform, so they have to be taken into account when designing the drivers. These considerations are beyond the scope of this thesis, so they will not, at the moment, be taken into account.

Regarding top-plate parasitic capacitances, they can originate from various sources, such as top-plate to bulk couplings of the implemented capacitors (as seen in Fig. 3.2), the transistors (gate and junction capacitances), and nearby metal layers.

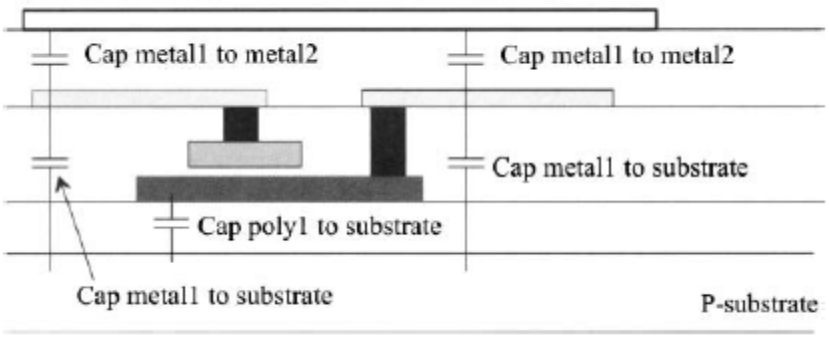


Fig. 3.2: : [From Baker et al.]: Cross-sectional view of a capacitor implemented with VLSI technology, including the various sources of parasitic capacitances.

3.2.1. Parasitic capacitances impact on voltage gain:

When an arbitrary capacitor C_i is charging (Fig. 3.3), its bottom plate is connected to ground (through the inverter), and so the capacitor C_i lies in parallel to the top plate parasitic capacitances (C_p).

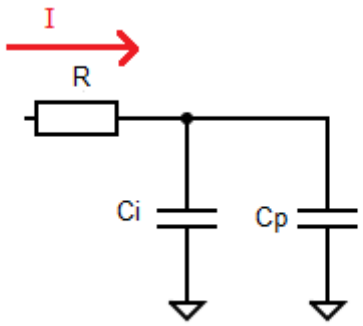


Fig. 3.3: Topology during a charging semi-period. The main capacitor lies in parallel with the equivalent parasitic capacitances.

At the end of a charging semi-period, both capacitors present the same voltage.

When the capacitor C_i is discharging (Fig. 3.4), its bottom plate is connected to the inverter (here depicted and analyzed as an ideal voltage source). The top plate parasitic capacitances are, however, still connected to ground at one end.

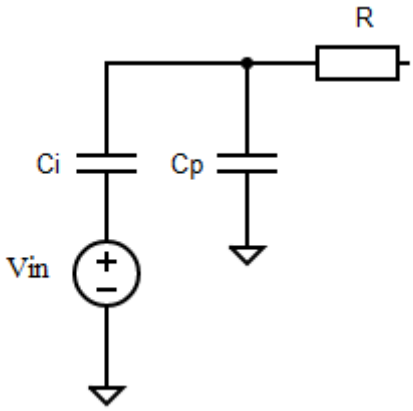


Fig. 3.4: Topology during a discharging semi-period. The parasitic capacitances are not directly affected by the inverter.

This generates a voltage difference between the top plates of both capacitors. This, in turn, initiates a charge redistribution between the two capacitors.

Assuming that the process of charge redistribution between capacitors takes place at a much higher rate than the discharge of capacitor C_i through the resistance R, the effect of the parasitic capacitances can be easily analyzed through the superposition principle and a capacitive voltage divider (Fig. 3.5).

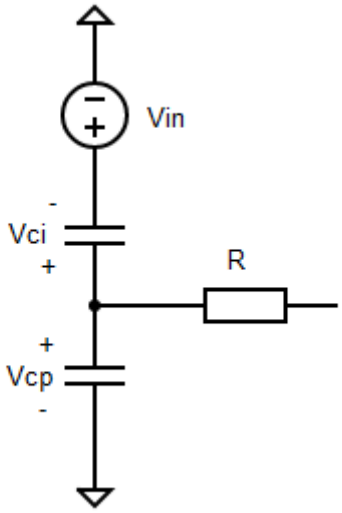


Fig. 3.5: Parasitic Voltage Divider

Applying the superposition principle, the node connected to the R equivalent resistance experiences two sources of voltage:

- The voltage across the terminals of either capacitor (V_{C_i}).
- The voltage contributed by the clock driver (V_{in}) in the form of a capacitive voltage divider.

The voltage at the node connected to R before initiating the discharge process becomes:

$$V_n = V_{C_i} + V_{in} * \frac{C_i}{C_i + C_p} \tag{26}$$

Ideally, the voltage gain of a stage of a CC-CP is V_{in}. This equation shows that the maximum voltage gain of a stage is reduced from the ideal to a fraction of this value, meaning that the maximum voltage attainable at the output once the steady-state has been reached is affected by the presence of top-plate parasitic capacitances. In later sections discussing the steady-state model a proof of the final impact of parasitics in the output voltage will be derived.

Regarding the dynamic model, this effect can be included in the discrete-time state space system. To that end equation (13) must be modified, becoming:

$$\Delta V_{i+1} = -\Delta V_i = \frac{\left(V_{in} * \frac{C_i}{C_i + C_p} + v_i - v_{i+1}\right)}{2}\left(1 - e^{-\frac{T}{RC}}\right) \tag{27}$$

However, there is another effect that must be taken into account before fully committing to the procedure derived in the previous section.

3.2.2. Parasitic effects on topology dynamics:

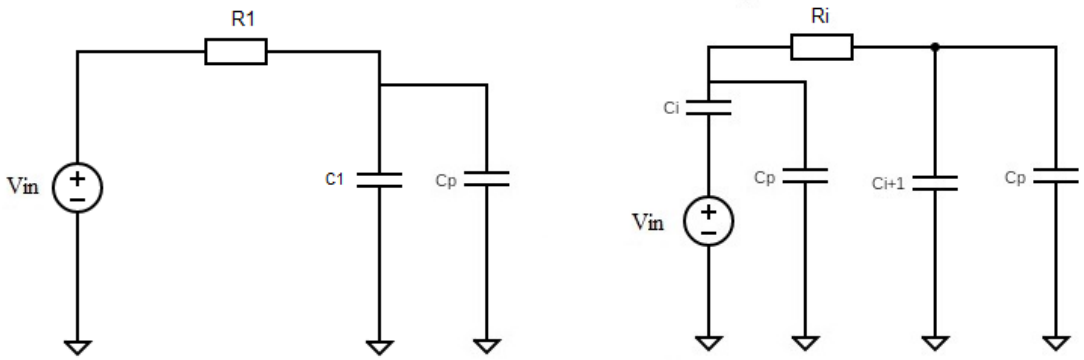


Fig. 3.6: CC-CP topologies with top-plate parasitic capacitances.

Although the procedures derived in section 2.3 still hold, the inclusion of parasitic capacitances in the model requires the consideration that they modify the value of the equivalent capacitances in each topology. Again, for simplicity we can consider that all fly-capacitors present the same value and that all parasitic capacitances also present the same value, albeit distinct from the value of fly-capacitors. These assumptions are not so rigorous as they might have been in previous sections (given that the size of transistors may vary from stage to stage), but they allow us to showcase the effect of parasitics.

Namely, the equivalent capacitance of the first stage topology (Fig. 3.6.left) is now the parallel association of capacitance C1 and Cp.

$$C_{eq} = C_1 + C_p \tag{28}$$

The same is true for the capacitances of intermediate stages. Since all fly-capacitances are equal and all parasitic capacitances are equal, all the resulting equivalent capacitances are equal.

Equations (13) and (14) must now be further modified.

$$\Delta V_1 = (v_{in} - v_1)\left(1 - e^{-\frac{T}{RC_{eq}}}\right) \tag{29}$$

$$\Delta V_{i+1} = -\Delta V_i = \frac{\left(v_{in} * \frac{C_i}{C_i + C_p} + v_i - v_{i+1}\right)}{2}\left(1 - e^{-\frac{T}{RC_{eq}}}\right) \tag{30}$$

3.3. Dynamic Model Validation:

The validation of the above derived models and equations is done in two steps. Firstly, a matlab script describing the model is written and tested. Secondly, using a

SPICE-based software (TINA-TI), an idealized version of the circuit is built and simulated, comparing the results obtained to the matlab results.

The matlab model has been created by generating a discrete-time state-space system. The transient response of such model has been simulated through the use of the Linear Simulation Tool, by applying a unit step function to the input.

Following the creation of the idealized circuit and its mathematical model, various transient analyses have been performed.The ideal circuit used to compare the results was built using the SPICE-based software from Texas Industries, TINA-TI. The circuit can be seen in Fig. 3.7.

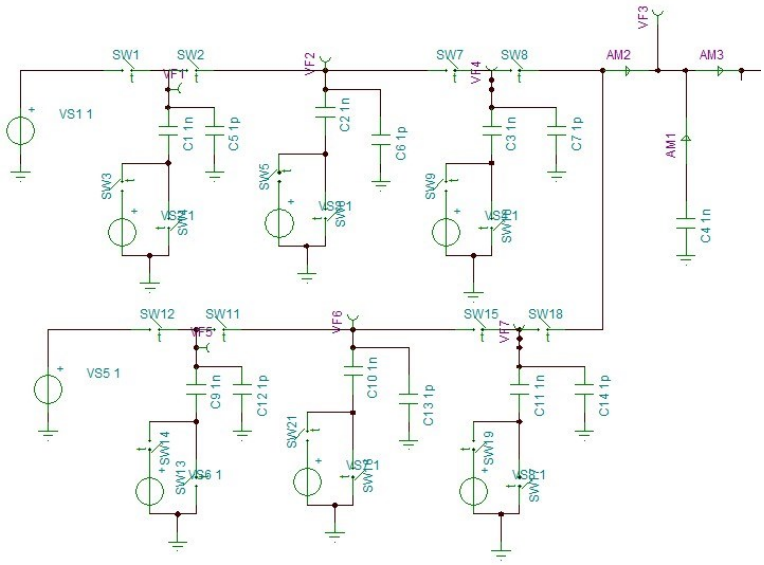


Fig. 3.7: Schematic form used for simulation of the CC-CP.

The model is simulated in a variety of cases. However, we present here only those with parameters shown in Table II, so as to simplify the presentation. The transient response of the output stage in those two cases, only differing in the presence of parasitic capacitances, is compared to a transient simulation of the circuit using the Texas Instruments SPICE-based software (TINA-TI).

All fly-capacitors and load capacitance are equal in value. Fig. 3.8 shows the superposition of the matlab model (black line) and the transient simulation of the SPICE circuit (red line). Table III presents the comparison of the steady-stage voltages reached as a consequence of the presence or absence of parasitic capacitances, given an ideal output voltage of 4V. The third column depicts the relative error between the model and the SPICE simulation.

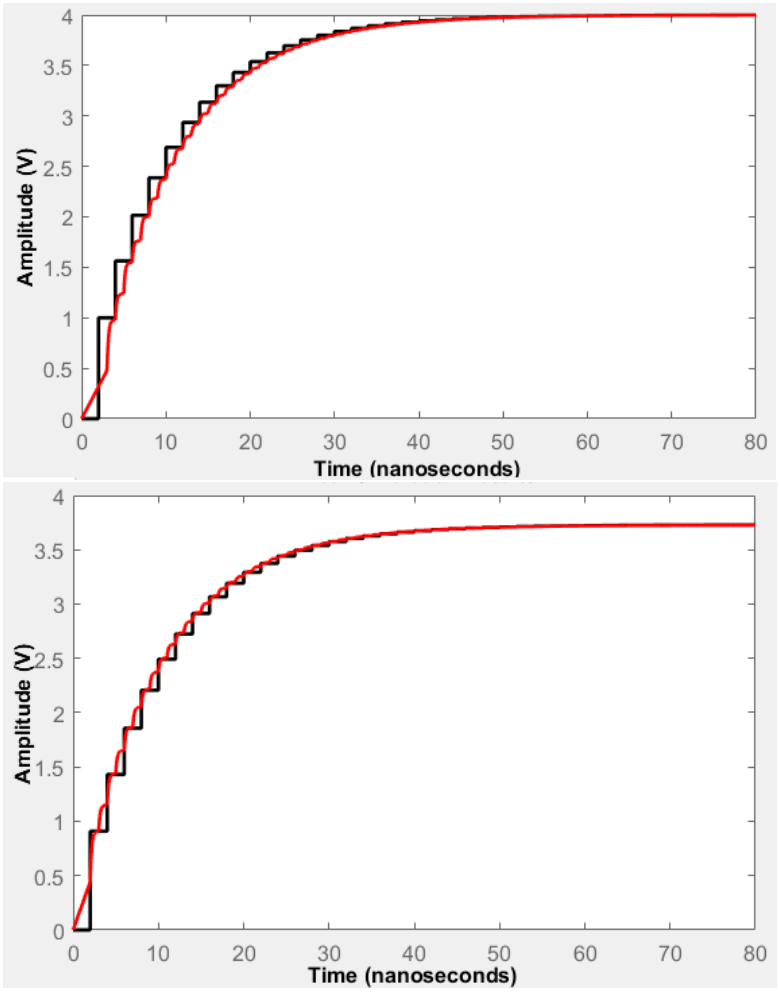


Fig. 3.8: Dynamic Model Simulation. Top) Case1. Bottom) Case 2. The black line corresponds to the Matlab script output. The red line, to the SPICE transient.

TABLE I: Parameters used during the simulation of the Dynamic Model

	C	Cp	R	f	Vin
Case 1	6 fF	0 F	50 kΩ	500 MHz	1 V
Case 2	6 fF	0.6 fF	50 kΩ	500 MHz	1 V

TABLE II: Steady-State voltages achieved as a consequence of parasitics

	Model (V)	SPICE (V)	%
Case 1	4	3.99	0.25
Case 2	3.73	3.727	0.08

It can be seen that both the transient and the steady-state output voltage coincide fairly well in both cases.

The advantage of the presented discrete time model is in calculation time. For large values of capacitances, the transient simulation in the SPICE based software can take several minutes, in some extreme cases (with capacitors in the picofarad range) up to

10-15 minutes. However, the Matlab model was able to produce results within 1-2 seconds of run-time for a varied range of capacitor values.

4. Steady-State Analysis: mean voltage values.

In a switched-capacitor converter of any type, the condition of steady-state is reached when, after a whole period of operation, the state-space vector value remains the same as that of the previous period. That is, $X[K+1] = X[K]$. What this means is that, for any capacitor: $V_{Ci}[K+1] = V_{Ci}[K]$. As per equation (15), this implies:

$$\Delta V_{charging} = \Delta V_{discharging} \tag{31}$$

That is, the increase in voltage during the charging semi-period must be equal to the decrease in voltage during the discharging semi-period.

A simple way to see this relation that allows to come up with an analysis equation is to consider that the increase in voltage of capacitor C_i during its charging semi-period must be equal to the increase in voltage of capacitor C_{i+1} during its own charging semi-period. This is only true if both capacitors present the same capacitance.

$$\Delta V_{Ci_{charging}} = \Delta V_{Ci+1_{charging}} \tag{32}$$

Restricting ourselves to the constraints imposed at the beginning of the analysis, we can forgo for the moment a generalized view and continue considering that all capacitances are equal. In this instance, equation (32) holds and, as per equations (13) and (14):

$$\left(V_{in} - \hat{V}_1\right) = \frac{V_{in} + \hat{V}_1 - \hat{V}_2}{2} \tag{33}$$

$$\frac{V_{in} + \hat{V}_i - \hat{V}_{i+1}}{2} = \frac{V_{in} + \hat{V}_{i+1} - \hat{V}_{i+2}}{2} \tag{34}$$

The symbol $\hat{}$ is indicative of the mean voltage value during steady-state. Here we work under the assumption that the ripple is superposed over a DC voltage value.

It is important to stress that the voltage values of the capacitors change during a semi-period of operation (the system is inherently time-continuous), but one can assume that, during steady-state, the mean value remains the same.

Consider a CC-CP with 3 stages. The Steady-State condition equations are:

$$\left(V_{in} - \hat{V}_1\right) = \frac{V_{in} + \hat{V}_1 - \hat{V}_2}{2} \tag{35}$$

$$\frac{V_{in} + \hat{V}_1 - \hat{V}_2}{2} = \frac{V_{in} + \hat{V}_2 - \hat{V}_3}{2} \tag{36}$$

$$\frac{V_{in} + \hat{V}_2 - \hat{V}_3}{2} = \frac{V_{in} + \hat{V}_3 - \hat{V}_{out}}{2} \tag{37}$$

The first equation can be rearranged to isolate the mean value of V1:

$$\hat{V}_1 = \frac{V_{in} + \hat{V}_2}{3} \tag{38}$$

V1 can be substituted in the second equation, and V2 can be isolated:

$$\hat{V}_2 = \frac{3 * \hat{V}_3 + V_{in}}{5} \tag{39}$$

And, finally, we can substitute V2 in the third equation, isolating V3.

$$\hat{V}_3 = \frac{5 * \hat{V}_{out} + V_{in}}{7} \tag{40}$$

These equations relate the mean voltage value of each capacitor to the contiguous one. These equations serve two purposes:

- From an analytical standpoint, they can be used to derive the ideal ratio V_{out}/V_{in}. One must only consider that capacitor C1 is fully charged, the circuit is unloaded, and there is no ripple. Then, $\hat{V}_1 = V_{in}$. Substituting, one obtains:

$$V_1 = V_{in}$$

$$V_2 = 2V_{in}$$

$$V_3 = 3V_{in}$$

$$V_{out} = 4V_{in}$$

$$\frac{V_{out}}{V_{in}} = 4$$

  Which is to be expected for a 3-stage CC-CP, partially validating equations (33) and (34)

- From a synthesis perspective, these equations allow the prediction of mean voltage values of each capacitor under non-idealized conditions. That is, when the output voltage is lower than the one predicted by the ideal relation Vout/Vin, be it because of parasitic effects, the presence of a load or both, the mean voltage of the fly-capacitors can still be predicted. From a design perspective, knowing these mean voltage values allows the proper sizing of the transistors working under the circuit's operating point.

4.1. Mean Voltage Value Validation

In order to determine the validity of equations (33) and (34), the circuit in Fig. 3.7 is loaded with different resistances. A transient simulation is then performed with circuit parameters equal to those of TABLE I, case 1, expect for the resistances' values. The mean voltage values of the output and each fly-capacitor is calculated grossly as $\frac{(V_{min}+V_{max})}{2}$ during a charging semi-period for all capacitors and annotated (see Fig. 4.1). The results can be seen in TABLE III.

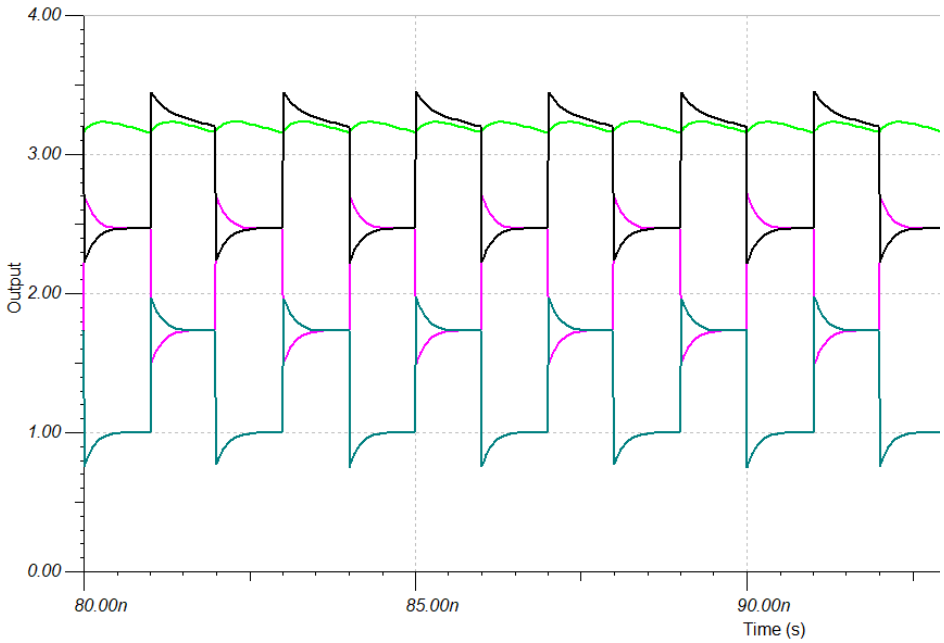


Fig. 4.1: Fly-capacitor waveforms in steady-state, Rload = 2MΩ. Green: output capacitor. Black: fly-capacitor 3. Purple: fly-capacitor 2. Blue: fly-capacitor 1. The mean value is extracted in their respective charging period.

TABLE III: Mean Voltage Values, Simulation Results

Simulation					
$\widehat{V_1}$ (V)	$\widehat{V_2}$ (V)	$\widehat{V_3}$ (V)	$\widehat{V_4}$ (V)	Vin (V)	Rload (Ω)
1	2	3	4	1	Open
0,93	1,72	2,5	3,34	1	2,5 M
0,88	1,66	2,4	3,22	1	2M
0,871	1,55	2,19	3	1	1,5M
0,803	1,37	1,93	2,67	1	1M

The values of V4 (Vout) are then introduced in equation (40) and the mean voltage value of each fly-capacitor is recursively calculated. TABLE IV presents the results obtained. TABLE V compares the results of both tables.

TABLE IV: Mean Voltage Values, Equations Results

Equations				
$\widehat{V_1}$ (V)	$\widehat{V_2}$ (V)	$\widehat{V_3}$ (V)	$\widehat{V_4}$ (V)	Vin (V)
1	2	3	4	1
0,91	1,72	2,53	3,34	1
0,89	1,67	2,44	3,22	1
0,86	1,57	2,29	3	1
0,81	1,43	2,05	2,67	1

TABLE V: Relative Error between simulation and equations

Relative error (%)		
$\widehat{V_1}$ (V)	$\widehat{V_2}$ (V)	$\widehat{V_3}$ (V)
0,000	0,000	0,000
-2,681	-0,166	1,130
0,965	0,343	1,754
-1,617	1,364	4,188
0,864	4,196	5,854

Note that the results are consistently under a 10% relative error. Also, it is important to note that as the value of the resistive load decreases, the ripple both at the output and each fly-capacitor increases. Given the exponential nature of ripple during a semi-period, it can be hard to properly determine the mean value of the curves by inspection. These results are then to be taken as approximations.

However, they might be enough to consider them useful from a synthesis perspective. When transistors are to be sized appropriately to present a desired equivalent resistance, the mean values of the fly-capacitors correspond to the mean operating points of Vd, Vs and Vg.These considerations will be explored in detail in the FDSOI implementation section.

5. Steady-State Analysis: Thèvenin Model and Ripple approximation.

The previous section analyzed the mathematical conditions that arise during steady-state and how they affect the mean voltage of the different fly-capacitors. However, no model has been derived yet to predict the output voltage under loaded conditions.

There are three phenomena that affect the output voltage. Namely:

- Resistive loses
- Parasitic capacitances
- Voltage dependent capacitors

The effect of parasitic capacitances has been already explored in section 3.2, and will only be slightly extended to consider the effect on the output voltage as related to the number of stages of a CC-CP.

Voltage dependent capacitors introduce some challenging effects, but under idealized conditions of linear capacitors, their effect can be ignored. Therefore, they will not be considered in this section. However, their effect will be presented in the sections regarding FDSOI implementations of the circuit.

5.1. Resistive losses – CC-CP equivalent resistance.

When a DC-DC converter is connected to a load, under steady-state conditions, a constant in average flow of current through the circuit will take place. If the converter can be modeled as a resistance under certain operation conditions, this flow of current will produce a voltage drop. This voltage drop will ultimately affect the voltage at the output of the converter. It is then necessary, in order to have a complete steady-state model, to model the equivalent resistance of the CC-CP.

It is a well-known fact [11] that the equivalent resistance of a switched-capacitor (Fig. 5.1) can be expressed as:

$$R_{eq} = \frac{1}{fC} \tag{41}$$

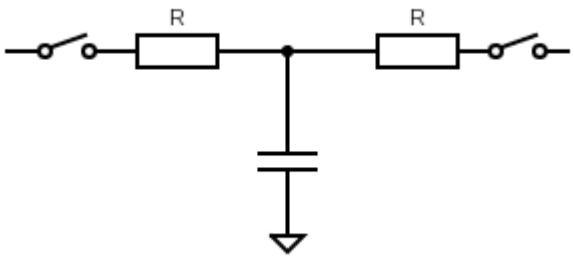


Fig. 5.1: Switched-Capacitor circuit representation.

Where f is the switching frequency and C the capacitance.

An extensive derivation of the generalized equivalent power resistance of a switched-capacitor circuit can be found in [11], presenting a more generalized equation applicable to a broader set of conditions.

$$R_{eq} = \frac{1}{fC}\coth\left(\frac{1}{2fR_{sw}C}\right) \tag{42}$$

Or, defining $\beta_1 = \frac{1}{fR_{sw}C}$

$$R_{eq} = \frac{1}{fC}\coth\left(\frac{\beta_1}{2}\right) \tag{43}$$

5.1.1. Fast vs Slow Switching limit

Equation (43) can take two limits (Fig. 5.2):

- When $|\beta_1| \to 0$. This is called the Fast Switching Limit (FSL)
- When $|\beta_1| \to \infty$. This is called the Slow Switching Limit (SSL)

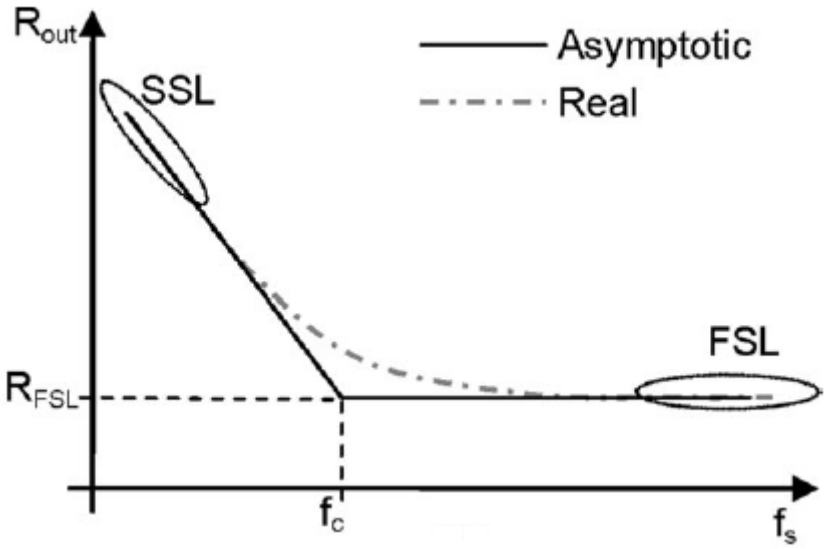


Fig. 5.2: Asymptotic and Real representations of equation (42), including their limits (from [12])

In the limit when β_1 tends to 0 (FSL), equation (43) can be simplified as follows:

$$R_{eq}\lim_{\beta_1\to 0} = \frac{1}{fC}\left[\frac{(1+(1-\beta_1))}{(1-(1-\beta_1))}\right] \tag{44}$$

$$R_{eq}\lim_{\beta_1\to 0} = \frac{1}{fC}\left[\frac{2}{\beta_1}\right] = \frac{1}{f_{sw}C}\left(\frac{2fR_{sw}C}{1}\right) \tag{45}$$

$$R_{FSL} = R_{eq}\lim_{\beta_1\to 0} = 2R_{sw} \tag{46}$$

Where we have used the fact that the Maclaurin series expansion of the exponential function e^x is $1 + x$ in a first order approximation.

In the limit when β_1 tends to ∞ (SSL), $\coth\left(\frac{\beta_1}{2}\right) \approx 1$ and:

$$R_{SSL} = R_{eq} \lim_{\beta_1 \to \infty} = \frac{1}{f_{sw} C} \tag{47}$$

Equation (46) tells us that when the frequency is sufficiently high, the equivalent resistance of a switched-capacitor is determined by the sum of the ON resistances of the switches at either side of the capacitor, while equation (47) tells us that if the switching frequency is low enough, the switch resistances bear no effect. These are, respectively, the fast and the slow switching limits (FSL and SSL).

Conventionally, the literature [12][13] considers the equivalent resistance of a switched-capacitor circuit can be approximated as:

$$R_{eq} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{48}$$

Where Rssl and Rfsl, described below, are the equivalent resistances of the whole circuit operating, respectively, at the aforementioned limits.

In the next section, we derive an expression for the equivalent resistance of a CC-CP as a simple linear combination of equation (43).

5.1.2. Equivalent resistance of a CC-CP of an arbitrary number of stages.

Equation (43) is based on a derivation based on the energy losses produced during the charging and/or discharging of a capacitor in a switched regime. Reference [14] offers a conceptual and physical insight into energy losses incurred during the operation of switched-capacitor circuits, remarking that it is the process of charging/discharging itself that is responsible for the equivalent power resistance.
That is, there are energy losses that can be modelled as resistances regardless of the presence of actual ohmnic resistors. This is notable enough to be stressed:

Switched-capacitor circuits with ideal switches presenting 0 ON resistances incur energy losses as a direct consequence of the process of charging/discharging of the capacitors.

Every time a capacitor is charged, there are energy losses. Every time a capacitor is discharged, there are energy losses.

Let's consider a 3-stage CC-CP with 2N fly-capacitors and 1 load capacitor, where N=n+1, and **n** is the number of stages (equation 1). The equivalent circuit can be found in Fig. 5.3 in schematic form.

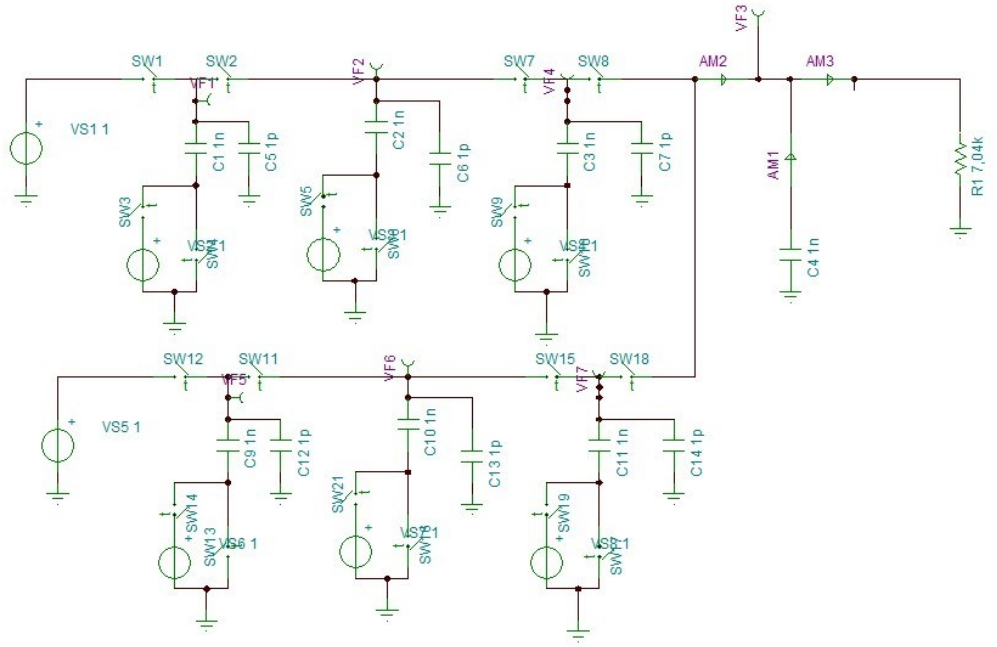


Fig. 5.3: Schematic representation of a 3-stage CC-CP with resistive load.

If we consider only one branch of the CC-CP, there are N fly-capacitors and 1 load capacitor. Each fly capacitor experiences charging and discharging, while the load capacitor experiences only a charging process through a switch.

Reference [15] introduces a methodology to derive the Rssl and Rfsl for SC circuits of arbitrary complexity. These Rssl and Rfsl are not to be confused with those of equations (46) and (47), as those refer to a single switched-capacitor. Reference [15] proposes a method to compute the overall RSSL and RFSL of the circuit as a whole.

In order to obtain the RSSL and RFSL of the circuit in Fig. 5.3, consider Fig. 5.4 and Fig. 5.5, depicting, respectively, phase 1 and 2 of operation, during which a packet of charge is transferred among capacitors.

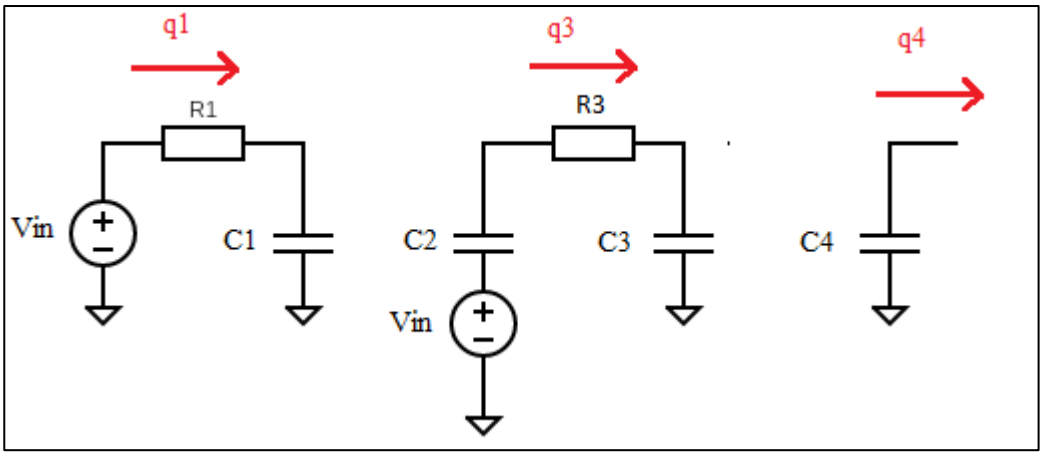


Fig. 5.4: Charge exchange during phase 1 of operation.

φ_1:

$$q_1 = q_{in} \tag{49}$$

$$q3 = q2 \tag{50}$$

$$\frac{qout}{2} = q4 \tag{51}$$

φ_2:

$$q2 = q1 \tag{52}$$

$$q3 = \frac{qout}{2} + q4 \tag{53}$$

Solving the system yields:

$$q1 = q2 = q3 = qout \tag{54}$$

$$q4 = \frac{qout}{2} \tag{55}$$

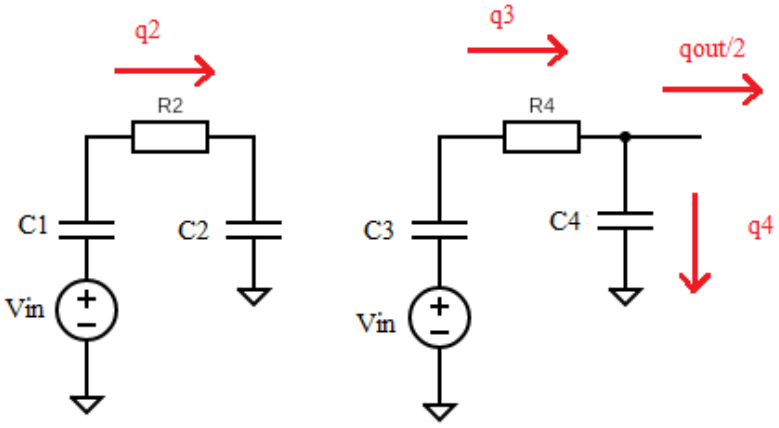


Fig. 5.5: Charge exchange during phase 2 of operation

These are the equivalent topologies formed during phase 1 and 2 respectively (see Fig. 3.1).

Following the nomenclature on [15], the Charge Multiplier Vector (CMV) has coefficients:

$$\vec{a}_c = \left[1\ 1\ 1\ \frac{1}{2}\right] \tag{56}$$

We can also define a capacitor vector:

$$\vec{C} = \left[\frac{1}{C_1}\ \frac{1}{C_2}\ \frac{1}{C_3}\ \frac{1}{C_{load}}\right] \tag{57}$$

And the equivalent RSSL resistance can be found as the vector product of the square of the CMV ($\vec{a}_c$) and the capacitor vector ($\vec{C}$), all divided by the switching frequency.

$$R_{SSL} = \frac{1}{f}\,\vec{a}_c^{\,2} \cdot \vec{C}' \tag{58}$$

$$R_{SSL} = \frac{1}{f} * \left(\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} + \frac{1}{4} * \frac{1}{C_{load}}\right) \tag{59}$$

Since we are assuming that all capacitances are equal:

$$R_{SSL} \approx \frac{13}{4}\frac{1}{fC} \tag{60}$$

In order to determine the RFSL resistance, a similar procedure is followed regarding the charge flow through the switches. From the previous analysis, the charge flowing through each resistor is equal to Qout. Normalizing the vector.

$$\vec{a}r = [1\ 1\ 1\ 1] \tag{61}$$

We can now build a vector with the values of the switches' resistances.

$$\vec{R}_{sw} = [R_{sw1}\ R_{sw2}\ R_{sw3}\ R_{sw4}] \tag{62}$$

The RFSL resistance can be computed as 2 times the vector product of $\vec{a}r$ squared and the $\vec{R}_{sw}$ vector.

$$R_{FSL} = 2 * \left(\vec{a}_r^{\,2} \cdot \vec{R}'_{sw}\right) \tag{63}$$

$$R_{FSL} = 2 * (R_{sw1} + R_{sw2} + R_{sw3} + R_{sw4}) \tag{64}$$

Remember that, in order to keep all the sub-circuits with equal RC constants, switches 2, 3 and 4 have equal resistance Ron, while switch 1 has a resistance of Ron/2.

$$R_{FSL} = 2 * \left(\frac{R_{on}}{2} + 3 * R_{on}\right) \tag{65}$$

$$R_{FSL} = 2R_{on} * \left(\frac{7}{2}\right) \tag{66}$$

$$R_{FSL} = 7R_{on} \tag{67}$$

Therefore:

$$R_{tot} \approx \sqrt{\left(\frac{13}{4}\frac{1}{fC}\right)^2 + (7R_{on})^2} \tag{68}$$

However, a CC-CP presents a comparatively simple topology (two branches of switched-capacitors connected in series, those two branches connected in parallel). This allows us to derive a more general expression, a linear combination of equation (43).

Based on the conceptual and physical insight presented in [11] and [14], we theorize that the equivalent resistance of a single switched-capacitor can be linearly associated, similarly to ideal ohmnic resistors. That is, several concatenations of switched-capacitors can form equivalent resistive series associations and parallel associations.

In order to analyze these associations, we begin with the most generalized form of equation (43)

$$R_{eq} = \frac{1}{2fC}\coth\left(\frac{\beta_1}{2}\right) + \frac{1}{2fC}\coth\left(\frac{\beta_2}{2}\right) \tag{69}$$

Equation (69) states that the equivalent resistance of a switched-capacitor converter comprises the linear association (sum) of two equivalent resistances.

Remembering that it is the charging and discharging processes which produce the energy losses that can be modelled as resistances, we can identify each resistance of equation (69), one pertaining to the charging process and one pertaining to the discharging process (Fig. 5.1). If the charging and discharging time constants are equal ($\beta_1 = \beta_2$), equation (69) reduces to equation (43).

This leads us to hypothesize that the indivisible unit of the equivalent resistance of switched-capacitor converter is:

$$R_{eq_{unit}} = \frac{1}{2fC}\coth\left(\frac{\beta}{2}\right) \tag{70}$$

This equation represents the instance of either a charging process or a discharging process.

In a single branch of a CC-CP (Fig. 2.6), the switched-capacitors lie in series. Working under the assumption that all capacitors have equal value and that the RC time constants of each topology are equal, we expect to be able to express the equivalent resistance as the sum of all the instances of equation (70).

To illustrate this process, consider Fig. 5.6. We can readily observe a total of 7 charging and discharging processes (as illustrated by the black arrows) during a complete period of operation.

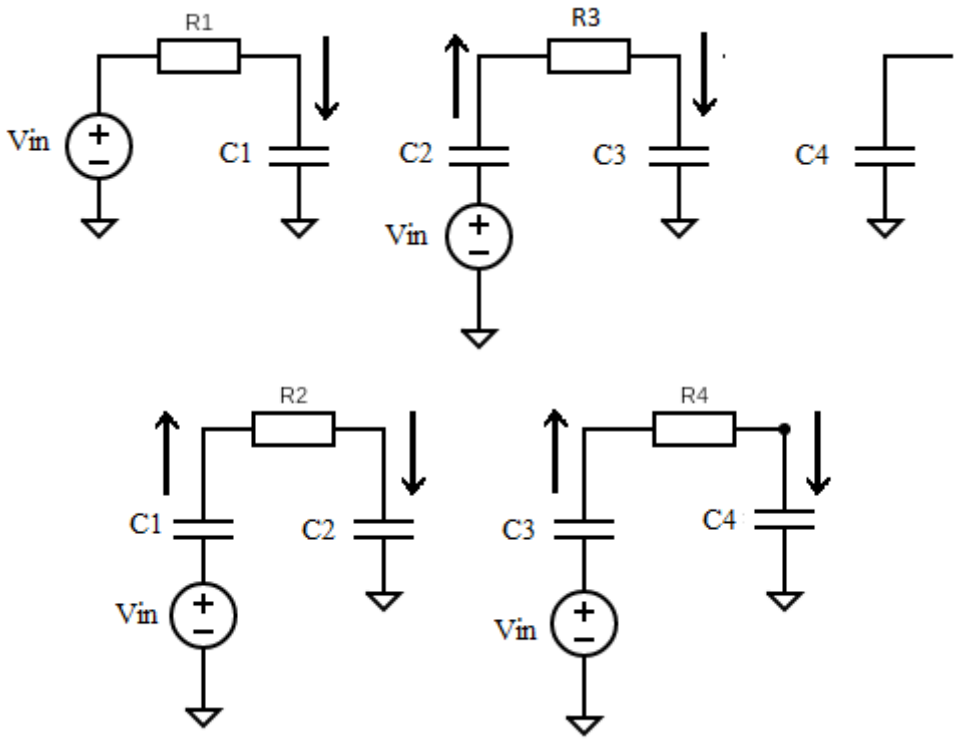


Fig. 5.6: Single Branch of a 3-Stage CC-CP. Top) Phase 1. Bottom) Phase 2. The black lines represent capacitive charging or discharging processes. We ignore discharging of Capacitor 4 (load capacitor) as it does not discharge in a switched manner.

Thus, we conclude that the equivalent resistance of a single branch of a 3-stage CC-CP is:

$$R_{eq} = 7 * \frac{1}{2fC}\coth\left(\frac{\beta}{2}\right) \tag{71}$$

We believe that this equation holds, generally, as long as all the topologies present an equal RC time constant and, if all capacitors have equal value, when R1=Ri/2.

Applying the limits above derived we can determine whether this expression coincides with the results of the CMV:

$$R_{SSL} = \lim_{\beta_1 \to \infty} \frac{7}{2}\frac{1}{fC}\coth\left(\frac{\beta_1}{2}\right) = \frac{7}{2}\frac{1}{fC} \tag{72}$$

$$R_{FSL} = \lim_{\beta_1 \to 0} \frac{7}{2}\frac{1}{fC}\coth\left(\frac{\beta_1}{2}\right) = 7\ R_{on} \tag{73}$$

The results of the RSSL resistance are not exactly equal, but they may suffice depending on the mode of operation. The RFSL coincides exactly (see equation (68)).

So far, we have calculated the resistance of one branch of a 3-stage CC-CP. To calculate the full resistance of a CC-CP, we can consider that the above resistances are simply halved (both for the CMV and our proposed method), there being two equivalent resistances in parallel. In the case of the Charge Multiplier Vector method, we can also analyze the circuit as a whole.

Table I compares the different resistances of a full CC-CP using the CMV method, according to these two possibilities (considering a parallel association, or applying the CMV to the circuit as a whole).

TABLE VI : 3-stage CC-CP Equivalent Resistances Method Comparison (Charge Multiplier Vector Method)

	Single Branch	Parallel Equivalent	CMV Method
R_{SSL}	$\frac{13}{4}\frac{1}{fC}$	$\frac{13}{8}\frac{1}{fC}$	$\frac{3}{2}\frac{1}{fC}$
R_{FSL}	$7R_{on}$	$\frac{7}{2}R_{on}$	$\frac{7}{2}R_{on}$

With our proposed method, for a 3-stage CC-CP where all RC constants are equal across topologies, we consider that the total resistance is simply the parallel association of two branches:

$$R_{eq} = \frac{7}{4}\frac{1}{fC}\coth\left(\frac{1}{2fR_{sw}C}\right) \tag{74}$$

For a n-stage CC-CP:

$$R_{eq} = \frac{(2n+1)}{4}\frac{1}{fC}\coth\left(\frac{1}{2fR_{sw}C}\right) \tag{75}$$

5.2. Parasitic Capacitances effect on the output voltage

Section 3.2.1 showed how the presence of parasitic capacitances affects the maximum gain of a single stage in a CC-CP, reducing it from V_{in} to $V_{in} * \frac{C_i}{C_i+C_p}$, where Ci was the capacitance of the $i\text{th}$ fly-capacitor and Cp was its corresponding top-plate parasitic capacitance.

From a steady-state perspective, this phenomenon can be utilized to compute the maximum steady-state voltage the circuit can attain in open circuit conditions when sufficient time has elapsed.

In steady-state, open circuit conditions, the first fly capacitor C1 will eventually reach, during the charging semi-period, a voltage equal to V_{in} (capacitor C1 will be fully charged). As the switches commutate, the bottom plate of capacitor C1 will see a rising transition from the clock and, as per Fig. 3.5, a voltage divider will ensue. The maximum voltage fly-capacitor C2 will then be able to reach is:

$$V_{C_1} = V_{in} + V_{in} * \frac{C_1}{C_1 + C_{P_1}} \tag{76}$$

Let's now assume that capacitor C2, at the end of its charging semi-period, is fully charged at the maximum voltage capacitor C1 can attain equation (76)

Again, when the clock signal experiences a rising transition, a voltage divider is formed, whose resulting voltage is superposed to the voltage value of capacitor C2.

$$V_{C_2} = V_{in} + V_{in} * \frac{C_1}{C_1 + C_{P_1}} + V_{in} * \frac{C_2}{C_2 + C_{P_2}} \tag{77}$$

The situation repeats itself for each stage. For an n-stage CC-CP, the output voltage would be:

$$V_{out} = V_{in} + V_{in}\frac{C_1}{C_1 + C_{P1}} + V_{in}\frac{C_2}{C_2 + C_{P2}} + \cdots + V_{in}\frac{C_n}{C_n + C_{Pn}} \tag{78}$$

If C1=C2=…=C(n+1), and their parasitics are similar or equal:

$$V_{C_n} = V_{in} + n * V_{in} * \frac{C}{C + C_p} \tag{79}$$

For a 3-stage charge pump:

$$V_{out} = V_{in} + 3V_{in} * \frac{C}{C + C_p} \tag{80}$$

5.3. Thèvenin Equivalent:

With derivations made in the previous sections we can now predict how the circuit would behave were it to be connected to a load. In fact, the circuit can be completely modelled as a Thèvenin-Equivalent of the form presented in Fig. 5.7.

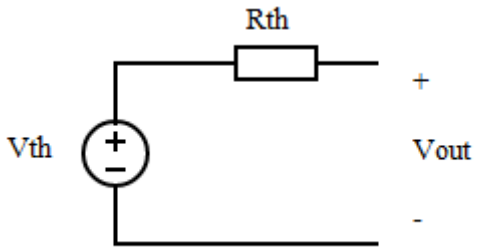


Fig. 5.7: Thèvenin Equivalent of a CC-CP.

We are going to ignore, for the moment, the effect of voltage dependent capacitors.

In a thèvenin equivalent model, we have two defining elements: the Thèvenin Voltage and the Thèvenin Resistance. We are going to consider the Thèvenin Voltage the maximum voltage attainable in the presence of parasistic capacitances. The Thèvenin Resistance is the equivalent resistance of the CC-CP. These have been derived above.

Thus, we can consider the Thèvenin Voltage:

$$V_{Th} = V_{in} + n * V_{in} * \frac{C}{C + C_p} \tag{81}$$

n being the number of stages, and where the assumption has been made that all stages present equal parasitic capacitances.

The Thèvenin Resistance is, likewise, already derived. Here we choose our proposed resistance.

$$R_{Th} = \frac{(2n+1)}{4} \frac{1}{fC} \coth\left(\frac{1}{2fR_{sw}C}\right) \tag{82}$$

This way, the behavior of the circuit becomes readily analyzable in a number of potential configurations.

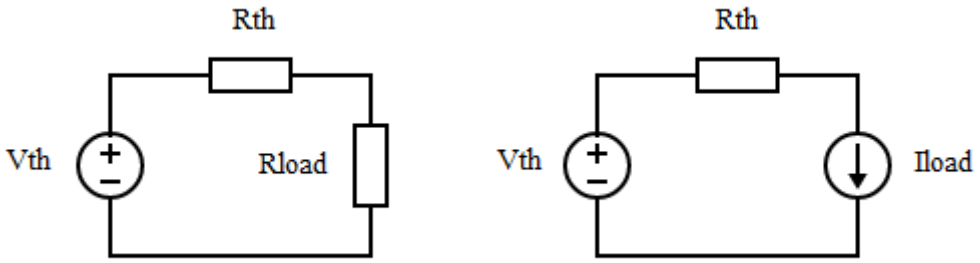


Fig. 5.8: Potential topologies of the Thèvenin Equivalent

For a resistive load, the output voltage would simply result from the voltage divider generated by the circuit resistances.

$$Vout = VTh * \frac{R_{load}}{R_{Th} + R_{load}} \tag{83}$$

Whereas for a load that is known to draw an approximately constant amount of current in a given voltage range, the following equation would be more suitable.

$$V_{out} = V_{TH} - R_{Th} * I_{load} \tag{84}$$

This is of particular interest in back-biasing circuits, where the load is a reverse PN junction.

These Thèvenin Equivalents are able to predict the operating point of the whole circuit. That is, they can be used to determine the output voltage and, through the equations derived at the beginning of this section, the operating points of the fly-capacitors.

However, these equivalent circuits tell us nothing about the dynamics of the CC-CP. The Discrete Time State-Space model can be used to predict the time response of the circuit. But, under certain circuit constraints, the circuit can be modeled as a simple RC circuit.

So far, we have considered that load capacitor has an equal value to the fly-capacitors. Nevertheless, in most cases the load capacitance is expected to be somewhat higher than the fly-capacitors. In those cases, the total contribution of the load capacitance to the equivalent resistance of the circuit can be neglected.

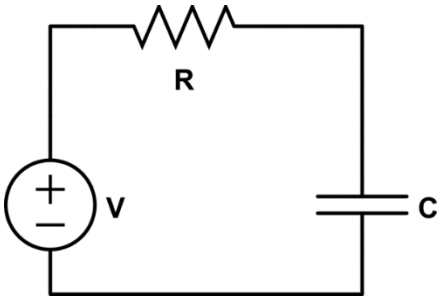


Fig. 5.9: Thèvenin Equivalent under certain constraints (namely, the capacitive load is much bigger than the fly-capacitors).

Also, when the load capacitances become high enough the charging time lengthens. When this happens, the fly-capacitors spend most of their time in a region of energy-efficient operation, where the equivalent resistance models above explained hold. [16] (Fig. 5.9)

Under those constraints, the circuit approaches operation similar to that of an RC circuit, with time constant:

$$\tau = R_{Th} * C_{load}$$

5.4. Thèvenin Equivalent validation

5.4.1. Effect of parasitic capacitances.

To validate the effect of parasitic capacitances on the output voltage, several transient simulations are performed on the circuit on Fig. 3.7, with different values of fly-capacitors and parasitic capacitances. The results are summarized in Table IV, where the simulated results are compared to the theoretical values obtained through equation (80).

TABLE VII: Parasitic capacitance effect summary.

C	Parasitics	Vout Theo (V)	Vout Sim (V)		Err Ab (V)		Err Rel (%)
1 nF	10 pF (1%)	3,970	3,97		0,000297		0,00748186
1 nF	50 pF (5%)	3,857	3,85		0,007143		0,18552876
1 nF	100 pF (10%)	3,727	3,72		0,007273		0,19550342
1 nF	200 pF (20%)	3,500	3,49		0,01		0,28653295
1 nF	300 pF (30%)	3,308	3,31		0,00231		0,0697188

2 nF	20 pF (1%)	3,970	3,97		0,000297		0,00748186
2 nF	100 pf (5%)	3,857	3,86		0,00286		0,0740192
2 nF	200 pF (10%)	3,727	3,73		0,00273		0,0731172
2 nF	400 pf (20%)	3,500	3,5		0		0
2 nF	600 pF (30%)	3,308	3,31		0,00231		0,0697188

5 nF	50 pF (1%)	3,970	3,97		0,000297		0,00748186
5 nF	250 pF (5%)	3,857	3,86		0,00286		0,0740192
5 nF	500 pF (10%)	3,727	3,73		0,00273		0,0731172
5 nF	1 nF (20%)	3,500	3,5		0		0
5 nF	1,5 nF(30%)	3,308	3,31		0,00231		0,0697188

It can be seen that it is the relative value of the parasitic capacitances to the fly-capacitor which determines the effect on the output voltage, as predicted in equation (76).

5.4.2. Equivalent resistance

To determine the validity of the equivalent resistance equations, we set the parameters of the circuit in Fig. 3.7 to:

$$C = C_{load} = 6\,fF$$

$$f = 500\,MHz$$

$$R_{sw}i, \forall\, i \neq 1 = 50\,k\Omega$$

$$R_{sw}1 = 25\,k\Omega$$

That means that the switch connecting the input voltage source to the first fly-capacitor has a resistance half that of the rest, maintaining equal RC constants across all topologies.

This sets the circuit in the Slow Switching Limit $(\coth(\frac{1}{2fR_{sw}C}) \approx 1)$.

We compare the results provided by equation (68) (CMV method), and (74).

With these parameter values, we compute the two different theoretical equivalent resistance, the one based on the CMV and the one derived in this thesis. For equation (68) and based on TABLE VI:

$$R_{CMV} = \sqrt{R_{SSL}^2 + R_{FSL}^2}$$

$$R_{CMV} = \sqrt{\left(\frac{3}{2}\frac{1}{fC}\right)^2 + \left(\frac{7}{2}R_{on}\right)^2} \approx 530\ k\Omega$$

And from equation (74):

$$R_{Thesis} = \frac{7}{4}\frac{1}{fC}\coth\left(\frac{1}{2fR_{sw}C}\right) = 584.82\ k\Omega$$

The circuit is then connected to an ideal current source, and both cases are simulated giving different values to the output current.

With parasitic capacitances set to 0, the expected output voltage is calculated as:

$$V_{out} = V_{th} - R_{Th} * I_{load}$$

TABLE VIII summarizes the results obtained, depicting the theoretical and simulated output voltages for a Thevenin resistance calculated through the CMV.

TABLE VIII: SPICE and equations result comparison of the Steady-Stage voltage under different current loads with RCMV.

I (A)	Vdrop Theo (V)	Vout Theo (V)	Vout Sim (V)		Abs Err (V)	Rel Err (%)
1,00E-06	0,530	3,470	3,5		0,030	0,850
1,50E-06	0,795	3,205	3,24		0,035	1,068
2,00E-06	1,059	2,941	3,01		0,069	2,308
2,50E-06	1,324	2,676	2,74		0,064	2,349
5,00E-06	2,649	1,351	1,51		0,159	10,510

TABLE VIII summarizes the results obtained, depicting the theoretical and simulated output voltages for a Thevenin resistance calculated using our proposed method.

TABLE IX: SPICE and equations result comparison of the Steady-Stage voltage under different current loads with RThesis.

I (A)	Vdrop Theo (V)	Vout Theo (V)	Vout Sim (V)		Abs Err (V)	Rel Err (%)
1,00E-06	5,85E-01	3,415	3,500		0,085	2,423
1,50E-06	8,77E-01	3,123	3,240		0,117	3,618
2,00E-06	1,17E+00	2,830	3,010		0,180	5,968
2,50E-06	1,46E+00	2,538	2,740		0,202	7,374
5,00E-06	2,92E+00	1,076	1,510		0,434	28,748

Our proposed equivalent resistance seems to deviate more from the simulations. It overestimates the resistance of the circuit when operating in SSL.

Further testing in a broader set of conditions determines that, as the circuit approaches the Fast Switching Limit, RThesis is more accurate than RCMV.

Setting $Ron = 200\ k\Omega$ and $I = 2\ \mu A$ (leaving the same values for the switching frequency and the capacitances).

TABLE X: Accuracy of distinct equivalent resistances in FSL operation

	Vdrop Theo (V)	Vout Theo (V)	Vout Sim (V)		Abs Err (V)	Rel Err (%)
RCMV1= 860 kΩ	1,72	2,28	2,355		0,075	3,185
RThesis=855 kΩ	1,71	2,29	2,355		0,065	2,760

Showing that Rthesis is more accurate in the Fast Switching Limit, while equation RCMV is more accurate in Slow Switching.

Fig. 5.10 shows how both resistance equations evolve as a function of frequency, showcasing how the linear combination equation presents higher values at lower frequencies.

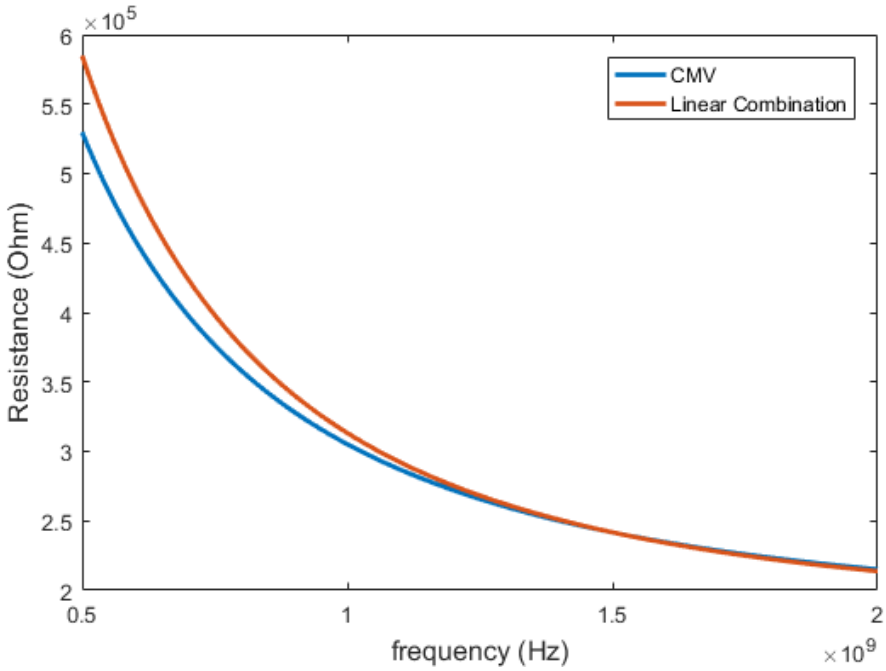


Fig. 5.10: Resistance vs frequency comparison of the two resistance equations above presented. Blue- CMV method (equation (68)). Orange- Linear combination (equation (74)).

5.5. Ripple Approximation

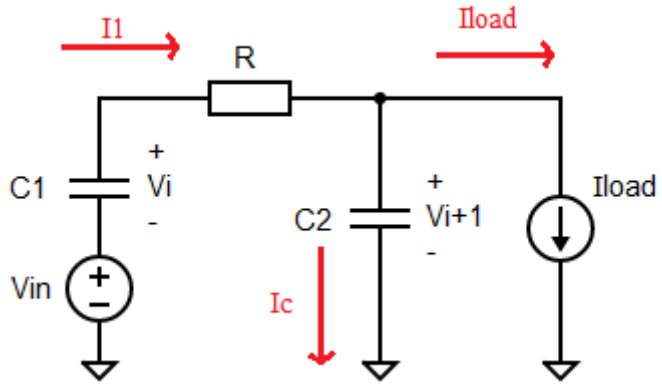


Fig. 5.11: Equivalent topology during one semi-period of operation at the load end.

In steady-state conditions it is also important to minimize the ripple at the output. However, in order to do so we must have an aiding equation to help orient the design. In this section such an equation is derived.

Consider the circuit in the above figure.

Let's assume that:

- R_{load} is large
- C_{load} (C_2) is large
- T is small
- The output current is constant and equal to:

$$I_{load} = \frac{V_{out}}{R_{load}} \tag{85}$$

Thus, we model the output current as an ideal current source for ease of analysis.

Analyzing the circuit with KVL yields the following equations (Where $C_{eq} = \left(\frac{1}{C_1} + \frac{1}{C_2}\right)^{-1}$):

$$-\frac{(V_i + V_{in})}{s} + I_1\left(R + \frac{1}{C_{eq}s}\right) - I_2\left(\frac{1}{C_2 s}\right) + \frac{V_{i+1}}{s} = 0 \tag{84}$$

$$I_1\left(s + \frac{1}{RC_{eq}}\right) = \frac{V_i + V_{in} - V_{i+1}}{R} + \frac{I_2}{RC_2} \tag{86}$$

Noting that:

$$I_2(s) = \frac{I_{load}}{s} \tag{87}$$

$$I_1(s) = \frac{V_i + V_{in} - V_{i+1}}{R} * \frac{1}{\left(s + \frac{1}{RC_{eq}}\right)} + \frac{I_{Load}}{RC_2} * \frac{1}{s\left(s + \frac{1}{RC_{eq}}\right)} \quad (88)$$

Using the partial fraction expansion method and transforming to the time domain:

$$i_1(t) = \frac{v_i + v_{in} - v_{i+1}}{R} e^{-\left(\frac{t}{RC_{eq}}\right)} + i_{load} * \frac{C_{eq}}{C_2}\left(1 - e^{-\left(\frac{t}{RC_{eq}}\right)}\right) \quad (89)$$

Where we can define:

$$i_{sw} = \frac{v_i + v_{in} - v_{i+1}}{R} \quad (90)$$

The current entering the loading capacitor (C_2) during a semi-period can be defined as:

$$i_c(t) = i_1(t) - i_{load} \quad (91)$$

$$i_c(t) = i_{sw} * e^{-\left(\frac{t}{RC_{eq}}\right)} + i_{load} * \frac{C_{eq}}{C_2}\left(1 - e^{-\left(\frac{t}{RC_{eq}}\right)}\right) - i_{load} \quad (92)$$

$$i_c(t) = i_{sw} * e^{-\left(\frac{t}{RC_{eq}}\right)} + i_{load} * \frac{C_{eq}}{C_2}\left(\left(1 - \frac{C_2}{C_{eq}}\right) - e^{-\left(\frac{t}{RC_{eq}}\right)}\right) \quad (93)$$

Let's define, for ease of algebraic procedure, $r = (1 - \frac{C_2}{C_{eq}})$

$$i_c(t) = i_{sw} * e^{-\left(\frac{t}{RC_{eq}}\right)} + i_{load} * \frac{C_{eq}}{C_2}\left(r - e^{-\left(\frac{t}{RC_{eq}}\right)}\right) \quad (94)$$

The value of i_{sw} is generally not readily accessible. However, we know that, in a CC-CP in steady-state conditions:

$$\int_K^{K+\frac{T}{2}} i_c(t)dt = 0 \quad (95)$$

Therefore:

$$\int_0^{\frac{T}{2}} i_{sw} * e^{-\left(\frac{t}{RC_{eq}}\right)} dt = \int_0^{\frac{T}{2}} -i_{load} * \frac{C_{eq}}{C_2}\left(r - e^{-\left(\frac{t}{RC_{eq}}\right)}\right) dt \quad (96)$$

$$i_{sw} RC_{eq}\left(1 - e^{-\left(\frac{T}{2RC_{eq}}\right)}\right) = i_{load} * \frac{C_{eq}}{C_2} RC_{eq}\left(1 - e^{-\left(\frac{T}{2RC_{eq}}\right)}\right) + i_{load} * \frac{C_{eq}}{C_2} * r * \frac{T}{2} \quad (97)$$

$$i_{sw} \approx i_{load} * \frac{C_{eq}}{C_2} - i_{load} * \frac{C_{eq}}{C_2} * r * \frac{1}{2fRC_{eq}} * \frac{1}{\left(1 - e^{-\left(\frac{T}{2RC_{eq}}\right)}\right)} \quad (98)$$

This way, ic can be approximated as:

$$i_c(t) = i_{load} * \frac{C_{eq}}{C_2} * r - i_{load} * \frac{C_{eq}}{C_2} * r \frac{1}{2fRC_{eq}} * \frac{1}{\left(1 - e^{-\left(\frac{T}{2RC_{eq}}\right)}\right)} * e^{-\left(\frac{t}{RC_{eq}}\right)} \quad (99)$$

Assuming symmetry -for simplification; the actual peak time depends both on the time constant of the topology and the values of the current- during a semi-period and stating that the maximum ripple takes place at t=T/4:

$$\Delta V = \frac{1}{C_{load}} \int_0^{\frac{T}{4}} i_c(t)\ dt \quad (100)$$

$$\Delta V = i_{load} \frac{C_{eq}}{C_2} * r * \frac{1}{4fC_{load}} - i_{load} \frac{C_{eq}}{C_2} * r * \frac{1}{2fC_{load}} * \frac{\left(1 - e^{-\left(\frac{T}{4RC_{eq}}\right)}\right)}{\left(1 - e^{-\left(\frac{T}{2RC_{eq}}\right)}\right)} \quad (101)$$

We can assume the worst-case scenario where:

$$\frac{\left(1 - e^{-\left(\frac{T}{4RC_{eq}}\right)}\right)}{\left(1 - e^{-\left(\frac{T}{2RC_{eq}}\right)}\right)} \approx 1 \quad (102)$$

The ripple equation then becomes:

$$\Delta V = i_{load} \frac{C_{eq}}{C_2} * r * \frac{1}{2fC_{load}} * \left[\frac{1}{2} - 1\right] \quad (103)$$

Noting that

$$\frac{C_{eq}}{C_2} * r = \left(\frac{C_{eq}}{C_2} - 1\right) < 0 \quad (104)$$

$$\Delta V = i_{load} \left(1 - \frac{C_{eq}}{C_2}\right) * \frac{1}{2fC_{load}} \left[1 - \frac{1}{2}\right] \quad (105)$$

Finally, we arrive at the expression:

$$\Delta V = i_{load} \left(1 - \frac{C_{eq}}{C_2}\right) * \frac{1}{4fC_{load}} \quad (106)$$

This equation is valid for SSL conditions. In FSL conditions, the simplifications made do not hold, but a comparatively simple analysis is possible.

From equation (89), we can interpret that the current drawn from the discharging capacitor (C_1) is a combination of exponential terms. In FSL conditions, we can make the assumption that the current drawn from the discharging capacitor by the current source is severely restricted by the time constraints imposed by the fast switching. Therefore, equation (89) reduces to:

$$i_1(t) = i_{sw} e^{-\left(\frac{t}{RC_{eq}}\right)} \tag{107}$$

Equation (91) still holds. Following a similar procedure, we can arrive at an expression for the ripple in the FSL:

$$\Delta V = i_{load} * \frac{1}{2fC_{load}} \left[\frac{\left(1 - e^{-\left(\frac{T}{4RC_{eq}}\right)}\right)}{\left(1 - e^{-\left(\frac{T}{2RC_{eq}}\right)}\right)} - \frac{1}{2} \right] \tag{108}$$

Where the exponential terms cannot be simplified.

5.5.1. Ripple equations validation

To establish the validity of the ripple equation (106), the original setting is adopted ($R_{sw} = 50\ k\Omega; C = 6\ fF; f = 500\ MHz$). The circuit is loaded with different magnitudes of current through a current source. This setting is used to determine the simulated ripple and compare it to that predicted by equation (106). TABLE XI summarizes these results

TABLE XI: SPICE and equations result comparison of the ripple under different current loads in SSL operation.

I (A)	Ripple Sim (V)	Ripple Theo (V)	Rel Err (%)
1,00E-06	0,0447	0,042	6,04%
1,50E-06	0,06	0,063	5,00%
2,00E-06	0,092	0,084	8,70%
2,50E-06	0,109	0,105	3,67%
5,00E-06	0,243	0,21	13,58%

For the study of the ripple in FSL, we increase the switching frequency from 500 MHz to 2 GHz and perform a similar comparison. This time, the theoretical values are calculated using equation (108).

TABLE XII: SPICE and equations result comparison of the ripple under different current loads in FSL operation.

I (A)	Ripple Sim (mV)	Ripple Theo (mV)	Rel Err (%)
1,00E-06	4,07	4,27	4,91%
1,50E-06	6,22	6,42	3,22%
2,00E-06	8,34	8,55	2,52%
2,50E-06	9,84	10,7	8,74%
5,00E-06	20,13	21,4	6,31%

6. FDSOI implementation

An implementation of a CC-CP based on the available FDSOI technology does not allow for a completely controlled environment such that one can freely choose the exact values of the parameters of interest. That is to say, a SPICE based software such as the one used in the previous sections allows for linear, voltage independent components (resistances and capacitances do not vary with the operating point of the circuit).

A real implementation is constrained in area, power consumption, and expected voltage at the output based on a load. In this thesis, though, we do not seek optimizing solutions, but rather to demonstrate the above derived models and what further effects arise when using non-ideal components; in this particular case, FDSOI components.

This section is divided in three parts. The first part explores the effect of voltage dependent fly-capacitors and how their behavior changes as they switch (how the same fly-capacitor behaves differently when it is being charged than when it is discharging) and at different stages (how voltage dependent fly-capacitors present different capacitances depending on the stage they are at). At the end of this part, some conclusions are drawn as to what behaviors are key in the implementation.

The second part explores the behavior of LVT FDSOI transistors, used to implement the switches, and their resistive characteristics at different stages. The last part of this section dwells on the procedures followed to adapt the characteristics of the components to a design perspective.

The FDSOI implementation has been carried out utilizing the 28 nm UTBB-FDSOI technology library from ST.

The FDSOI circuit studied and implemented is a 3-stage CC-CP with $V_{in} = V_{clk} = 0.3\ V$

6.1. Designing a test-bench / Experimental setting for the empirical analysis of voltage-dependent capacitors

The available technological library presents a variety of components that can be used as capacitors. Some are different architectures of stacks of metal vias, which present a predominantly linear, voltage independent behavior (MIM or MOM capacitors). And some are MOS based capacitors. In this section, we focus on the study of MOS capacitors, given their higher capacitance/area ratio. Specifically, we focus on the behavior of bulk MOS capacitors (that is, capacitors embedded in the bulk of the die) and LVT FDSOI MOSFETs designed to perform the function of capacitors.

Given that capacitance provided by MOS components depends heavily on the formation of the channel, we expect the capacitance of these components to vary intra-stage and inter-stage.

Since the voltage dependence and non-linear behavior cannot be directly analyzed through theoretical methods, we must perform empirical testing of the components.

This testing must be performed in such a way that it reflects the behavior of the components in implementations as fly-capacitors in a CC-CP.

For this purpose, we design a test-bench schematic on Cadence. The schematic is designed to evaluate the effect of the voltage operating points of the CC-CP on the capacitors themselves (how they affect the formation of the channel in MOS capacitors).

Each component is evaluated through two topologies. One reflecting the effect of the voltage operating points on charging fly-capacitors (Fig. 6.1), and one reflecting the effect of voltage operating points on discharging fly-capacitors (Fig. 6.2).

As discussed on section 2, a capacitor can be charged by an input voltage source or another capacitor (Fig. 2.5). In the schematic depicted in Fig. 6.1, both the clock-driver and the fly-capacitor connected to it are grouped into a single, ideal voltage source (named V_prev, as it reflects the voltage bias provided by the capacitor of the previous stage). The objective is not to analyze how the charging or discharging process takes place, but rather how the voltage bias provided by the different voltage sources (be them clock drivers and/or fly-capacitor), affect the capacitance of the charging MOS capacitor.

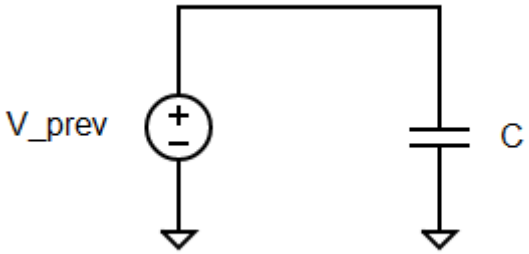


Fig. 6.1: Equivalent DC topology of a charging capacitor in steady-state (V_prev: Voltage of the Previous stage)

A similar procedure is followed to design the test-bench of discharging capacitors. Fig. 6.2 shows the topology of a discharging capacitor. Here, the clock-driver is represented, as in previous analysis, as an ideal voltage source (Vin), and the charging capacitor is also substituted by an ideal voltage source (named V_next to reflect the voltage bias provided by the capacitor of the next stage).

Once these test-benches are implemented, a parametric sweep of V_prev and V_next is performed. Both V_prev and V_next are swept from Vin and 0 V respectively, to the maximum-attainable, ideal voltage at the output and the capacitances displayed by the components are registered.

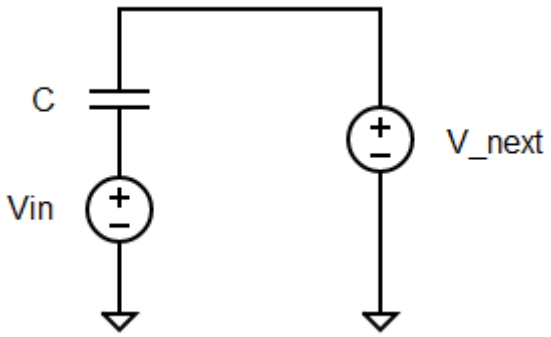


Fig. 6.2: DC equivalent topology of a discharging capacitor

We first analyze the behavior of LVTnFETs and LVTpFETs. These transistors are the same used as resistive switches. Fig. 6.3 and Fig. 6.4 depict the test-benches used for LVTnFET transistors for the charging and discharging topology respectively.

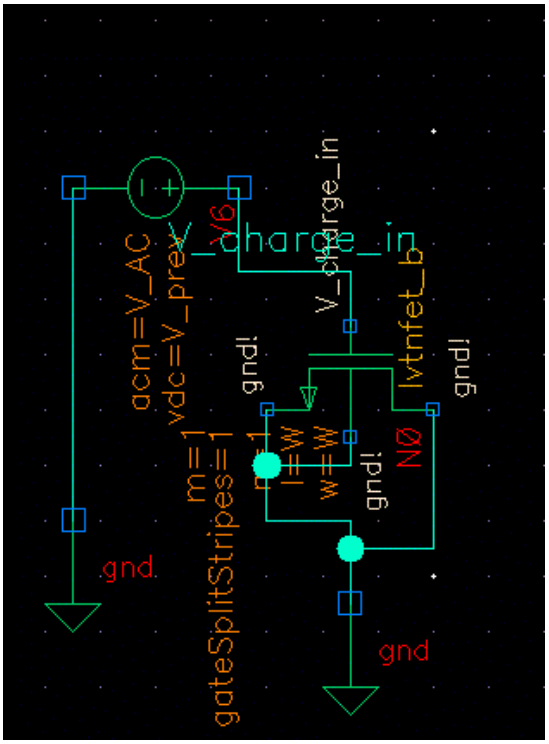


Fig. 6.3: Testbench. Lvtnfet implemented as a capacitor, charging topology. V_Charge_in represents V_prev (see Fig. 6.1).

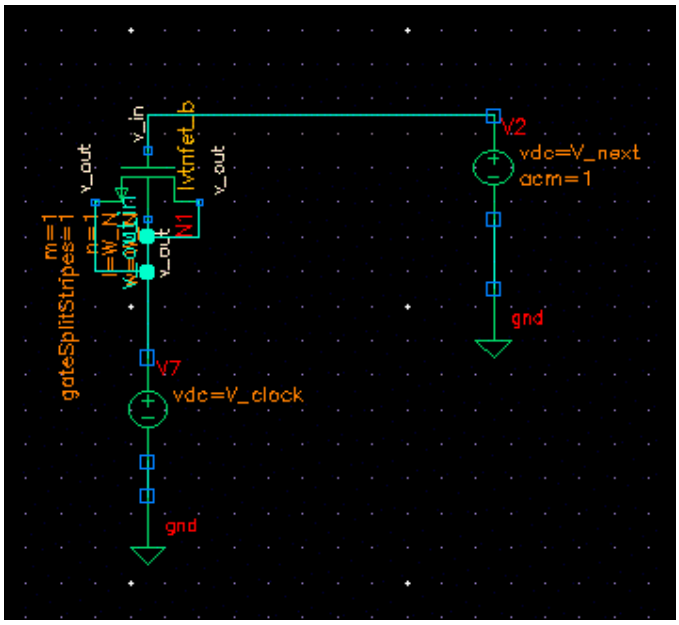


Fig. 6.4: Testbench. Lvtnfet implemented as a capacitor, discharging topology.

In the charging topology (Fig. 6.3), the voltage source implementing V_prev presents a DC (vdc=V_prev) component and an AC (V_AC= 1 V) component. The width of the transistor is set equal to the length.

$$W = L = 1\ \mu m$$

Initially, V_prev is set to 0.3 V

In order to determine the Capacitance, the voltage and current across the terminals of the component (in this case, the lvtnfet) are saved and used to compute the equivalent impedance, noted as Xc.

$$Xc(f) = \frac{\Delta V_c(f)}{I_c(f)} \tag{109}$$

We apply a dB20 function to this variable and save it so that it will be computed automatically. A frequency sweep is performed, obtaining a curve similar to the following one:

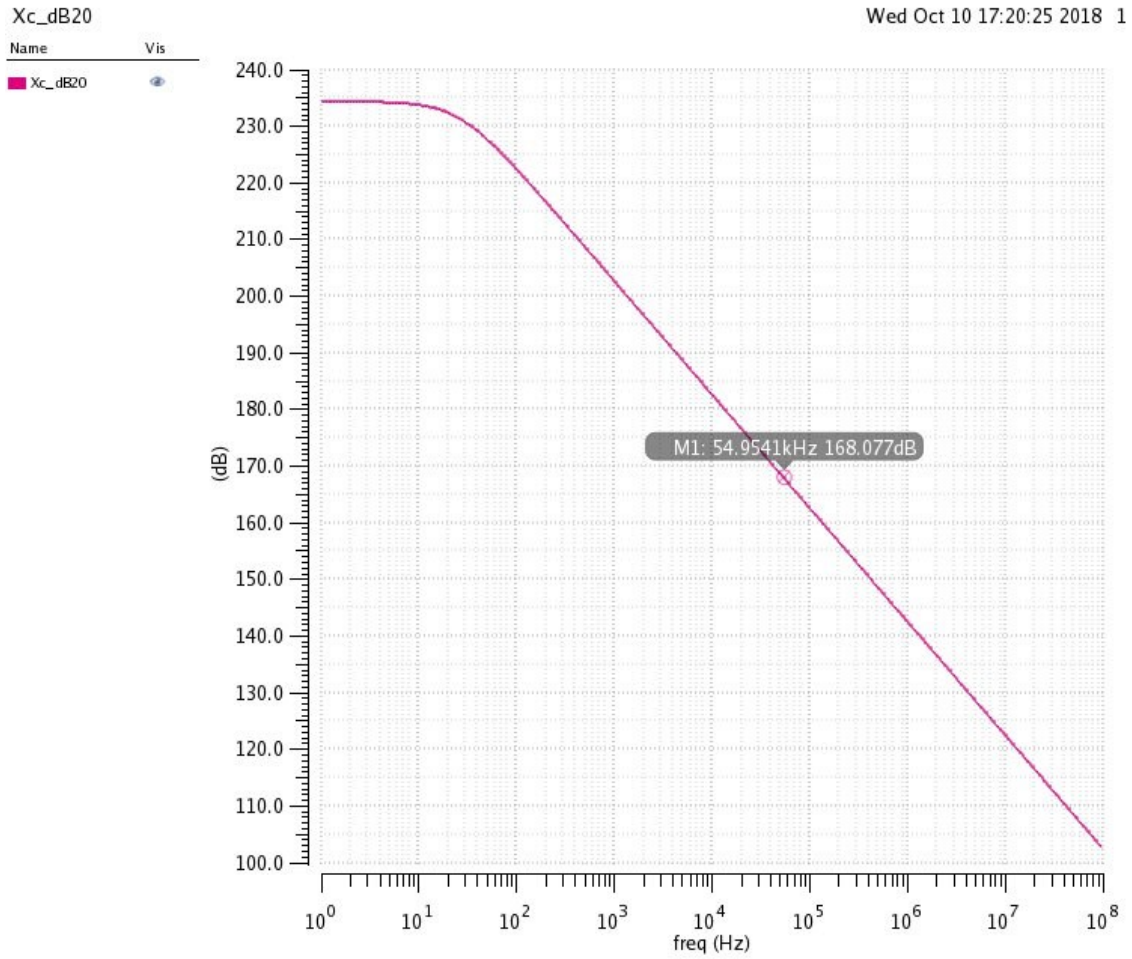


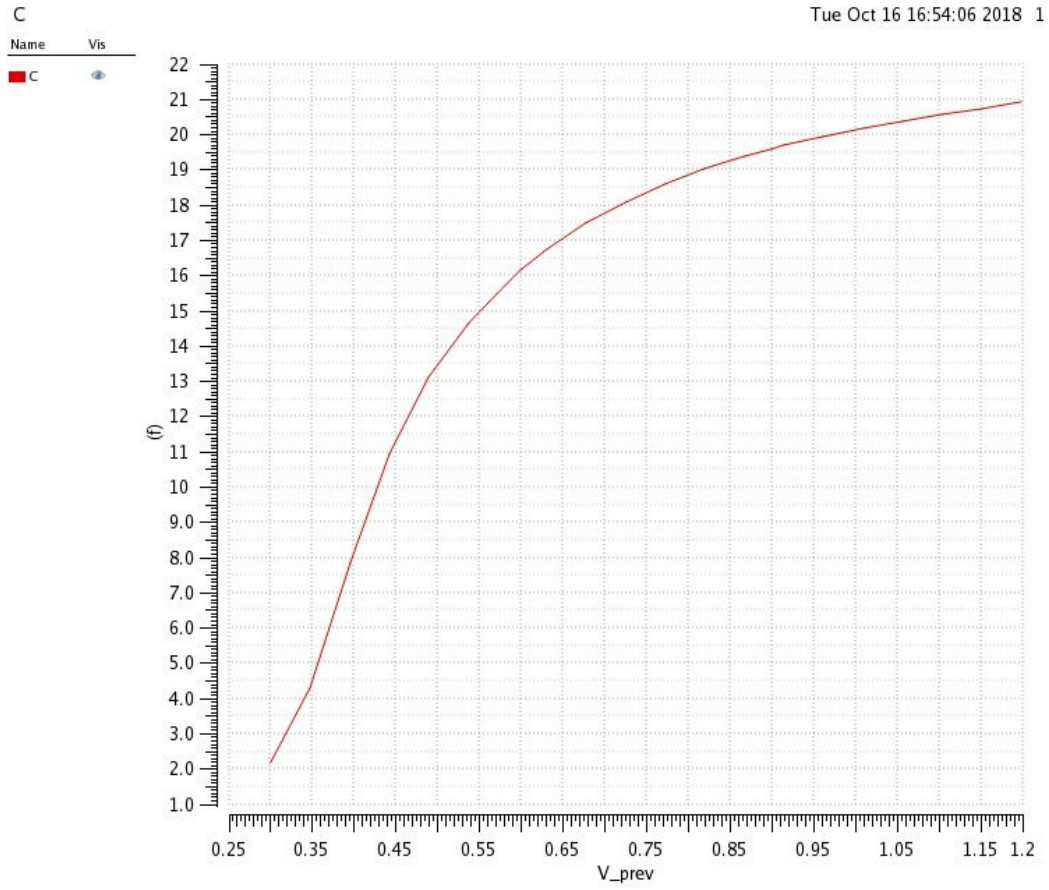
Fig. 6.5: dB20(Xc)

With this curve it is possible to extract the value of the capacitance at high frequencies, as resistive elements become negligible

A DC parametric sweep from 0.3 to 1.2 V (a case corresponding to a CC-CP with Vin= 0.3 V and 3 stages)

6.1.1. Lvtnfet / lvtpfet – Capacitive behavior

The following curve represents how the capacitance of the lvtnfet changes as a function of V_prev in charging topologies:



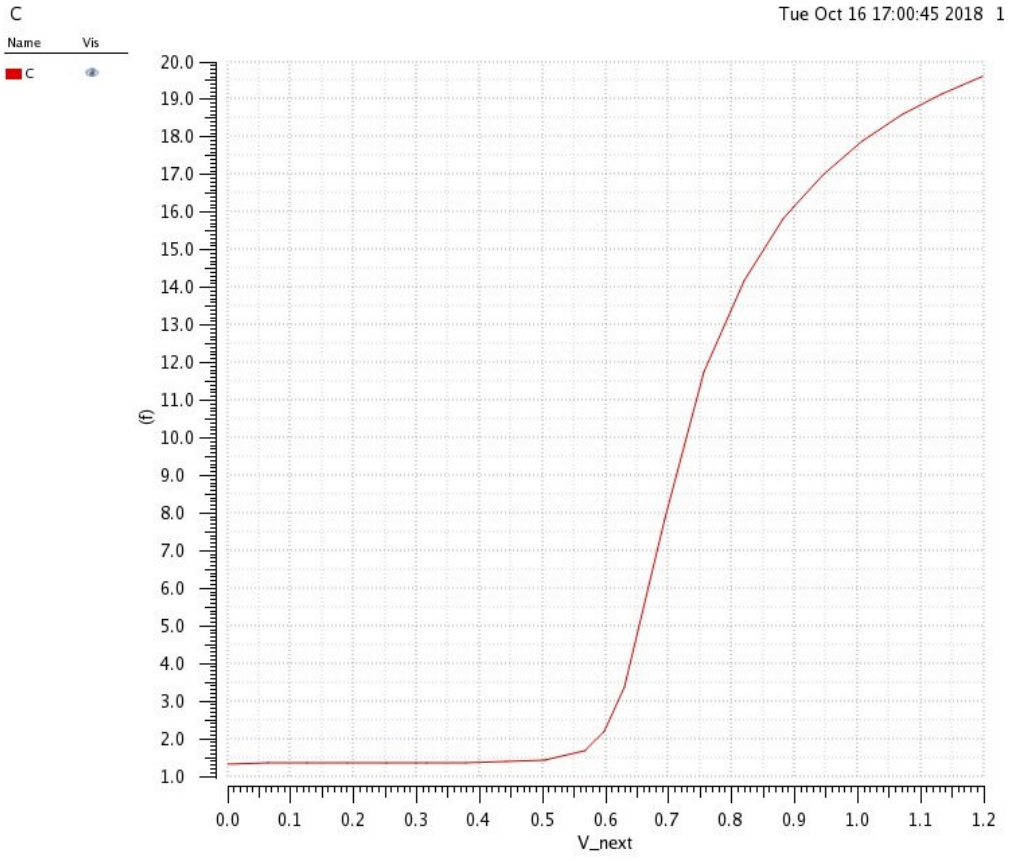


Fig. 6.6: Lvtnfet Voltage-Capacitance Characteristic. Top) Charging topology. Bottom) Discharging topology

For the discharging topology we perform a similar analysis, also depicted in the above figure.

We can see that both curves are similar. However, the discharging topology presents a shift to the right of approximately 0.3 V.

Although a similarly thorough analysis has not been carried out for the lvtpfet, preliminary testings show a similar behavior, probably due to the nature of the FET capacitance, related to the formation of a channel once conditions of strong inversion are reached.

That is, the connections of the FET terminals facilitate the formation of a channel during the charging semi-period. During a charging semi-period, Drain, Source and the back-gate are connected to ground, whereas during the discharging semi-period they are connected to the clock voltage, which might impede the formation of a channel, given that VGS is smaller in this configuration.

6.1.2. Egncap Behaviour

The following figures show the test benches employed to test the egncap capacitors:

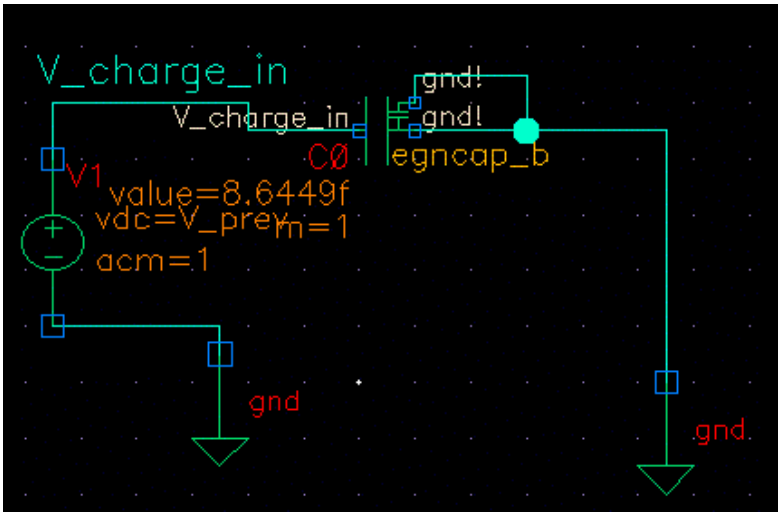


Fig. 6.7: Egncap Test Bench. Charging topology.

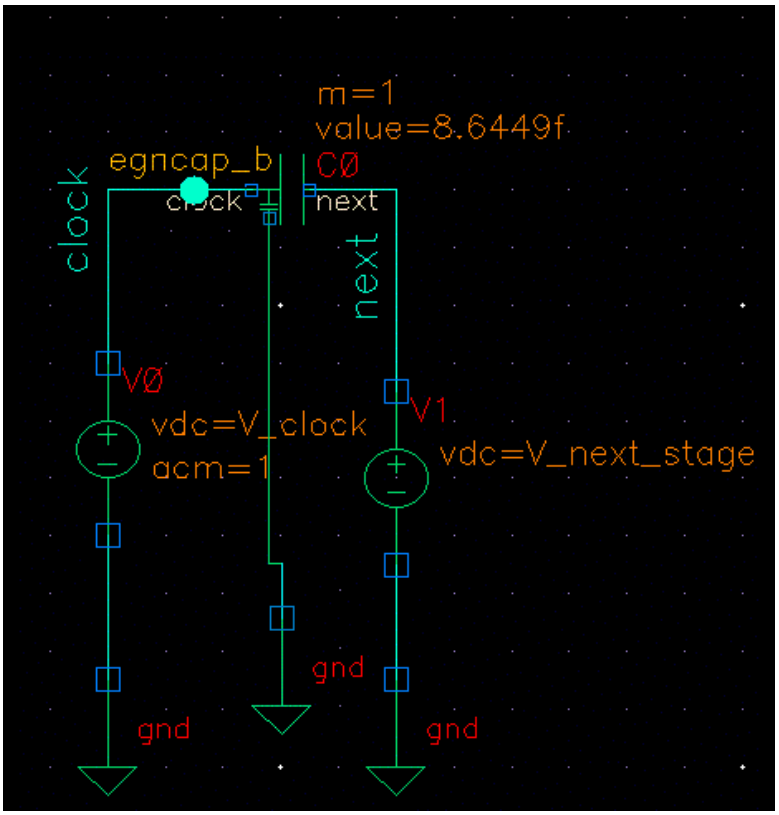


Fig. 6.8: Egncap Test Bench. Discharging topology.

The analysis made to extract values of the capacitance as a function of V_Prev and V_next_stage is the same as that for the FETs. Again, W=L=1 um

Note that the Egncap has a third terminal. This terminal corresponds with the bulk of the die and is, consequently, connected to ground.

Fig. 6.9 depicts the capacitance curve as a function of the charging voltage during the charging semi-period and the capacitance as a function of the V_next during the discharging semi-period.

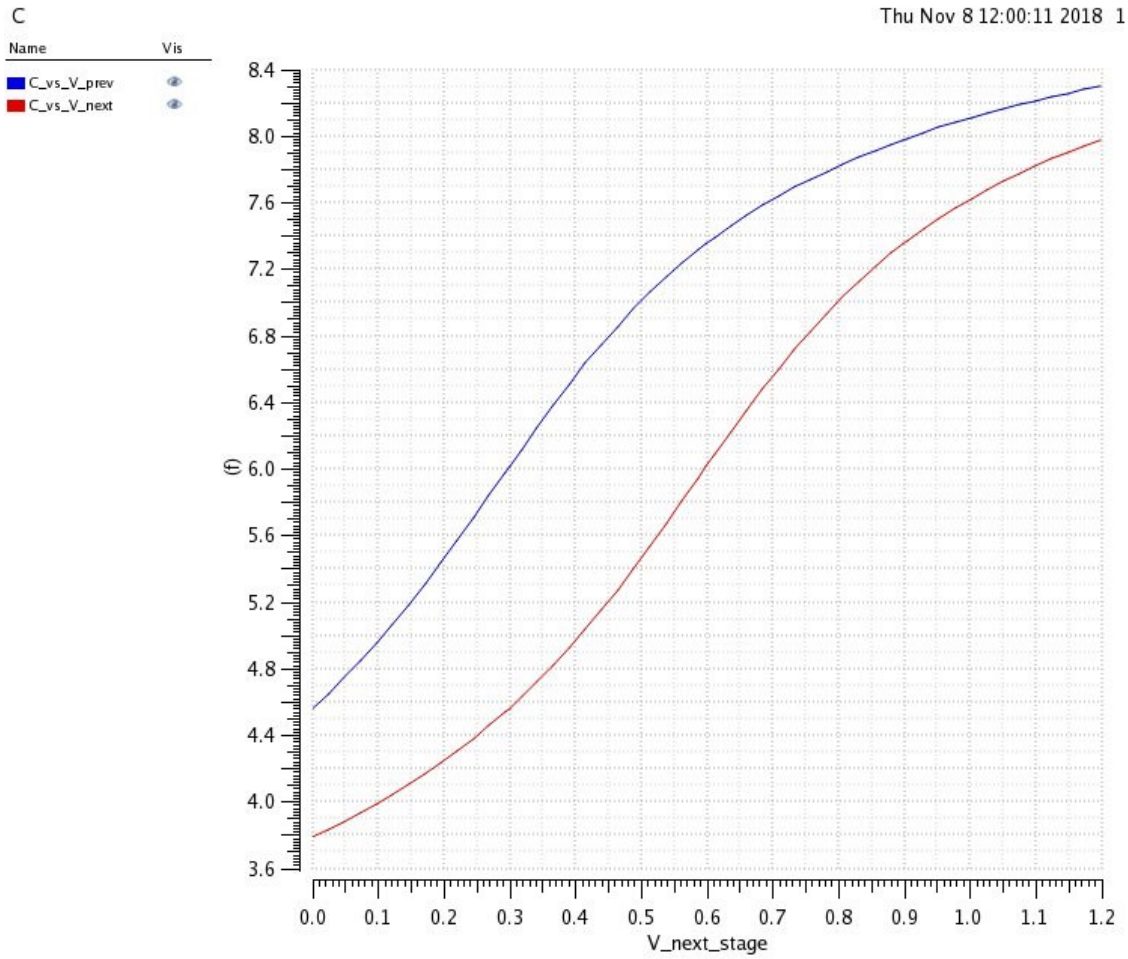


Fig. 6.9: Egncap Voltage-Capacitance characteristcs. In blue, capacitance in the charging topology. In red, in the discharging topology.

It can be seen that, for the same voltage values, the capacitances during the charging semi-period are always higher than the capacitances during the discharging semi-period. As we will see in the next section, this is the sought behavior.

Note also that, for the same width, fly-capacitors of later stages present a higher capacitance.

6.1.3. Effect of Voltage Dependent Fly-Capacitors

In the previous section we conducted an empirical analysis of the behavior of transistors implemented as fly-capacitors and saw that their capacitance can be different in charging and discharging topologies.

Given that, in a charge-pump, a capacitor can find itself in one of two states:

- It is being charged
- It is discharging

And given that in any of those states the operating point is different, two situations can arise for a particular capacitor.

- The capacitance is smaller in the charging state, larger in the discharging state.
- The capacitance is larger in the charging state, smaller in the discharging state.

Let's study the effects these two potential situations can have on the behavior of a charge-pump.

Let's assume that the charge-pump is operating in steady-state. We expect the voltages at all nodes to remain constant between periods, and to be similar between semi-periods. This means that the operating points of each capacitor will also remain constant during operation.

Let a capacitor be charged with a charge Q. During its charging, the capacitor presents a capacitance $C(V_Q)$, set by the DC operating-point. We know that the voltage across its terminals will be:

$$V_{C_{charging}} = \frac{Q}{C_{charging}} \tag{110}$$

At the end of the charging semi-period, the switches commute and the capacitor enters its discharging semi-period. During the discharging semi-period, the DC operating point is different. The capacitance is now Cdischarghing. (We are assuming perfect switching without charge loss).

Given that there cannot be charge redistribution between the plates of the capacitor, the voltage across its terminals now becomes:

$$V_{C_{discharging}} = \frac{Q}{C_{discharging}} \tag{111}$$

We divide both equations:

$$\frac{V_{C_{discharging}}}{V_{C_{charging}}} = \frac{\left(\frac{Q}{C_{discharging}}\right)}{\left(\frac{Q}{C_{charging}}\right)} = \frac{C_{charging}}{C_{discharging}} \tag{112}$$

$$V_{C_{discharching}} = V_{c_{charging}} * \frac{C_{charging}}{C_{discharging}} \tag{113}$$

From this equation we can extract the following conclusions:

- If Ccharging>Cdischarging, $V_{C_{discharging}} > V_{c_{charging}}$
- If Ccharging<Cdischarging, $V_{C_{discharging}} < V_{c_{charging}}$

Which means that there can be either a loss or gain of voltage value across the terminals of the capacitor when transitioning from the charging to the discharging semi-period.

This means that **the theoretical voltage gain of each stage is impacted by the change in value of the capacitances.**

Let's introduce a change of nomenclature for ease of operation:

- $V_{C_{charging}} \rightarrow V_C$

- $V_{C_{discharging}} \rightarrow V_C'$

And begin the analysis.

In an ideal CC-CP, with no parasitics and in open circuit, when steady-state is reached the output voltage at which capacitor C_{load} would stabilize is:

$$V_{C_{load}} = N * V_{in} \tag{114}$$

Where:

$$V_{C_{load}} = \left(V_{in} + V_{C(N-1)}\right) \tag{115}$$

We can recursively develop this equation:

$$V_{C_{Load}} = V_{in} + V_{C(N-1)} = V_{in} + V_{in} + V_{C(N-2)} =, \\ V_{in} + V_{in} + V_{in} + V_{C(N-3)} = \cdots = N * V_{in} \tag{116}$$

Where N is defined in equation (1).

If we now consider the effect of voltage dependent capacitances:

$$V_{C_{load}} = V_{in} + V'_{C(N-1)} \tag{117}$$

And as per equation (113)

$$V'_{C(N-1)} = V_{C(N-1)} * \left(\frac{C_{N-1}}{C_{N-1}'}\right) \tag{118}$$

$$V_{CN} = V_{in} + V_{C(N-1)} * \left(\frac{C_{N-1}}{C_{N-1}'}\right) \tag{119}$$

$$V_{C(N-1)} = V_{in} + V'_{c(N-2)} = V_{in} + V_{C(N-2)} * \left(\frac{C_{N-2}}{C_{N-2}'}\right) \tag{120}$$

Substituting:

$$V_{CN} = V_{in} + \left(V_{in} + V'_{c(N-2)}\right) * \left(\frac{C_{N-1}}{C_{N-1}'}\right) = V_{in} + \left(V_{in} + V_{C(N-2)} * \left(\frac{C_{N-2}}{C_{N-2}'}\right)\right) * \left(\frac{C_{N-1}}{C_{N-1}'}\right) =,$$

$$= V_{in} + V_{in} * \left(\frac{C_{N-1}}{C_{N-1}'}\right) + V_{C(N-2)} * \left(\frac{C_{N-2}}{C_{N-2}'}\right)\left(\frac{C_{N-1}}{C_{N-1}'}\right) \tag{121}$$

Developing the series:

$$V_{CN} = V_{in} * \left(\frac{C_{N-1}}{C_{N-1}'}\right)\left(\frac{C_{N-2}}{C_{N-2}'}\right) * \ldots * \left(\frac{C_1}{C_1'}\right) + V_{in} * \left(\frac{C_{N-1}}{C_{N-1}'}\right)\left(\frac{C_{N-2}}{C_{N-2}'}\right) * \ldots * \left(\frac{C_2}{C_2'}\right) + \cdots +,$$

$$+V_{in} * \left(\frac{C_{N-1}}{C_{N-1}'}\right) + V_{in} \tag{122}$$

$$V_{CN} = V_{in} + V_{in} * \sum_{i=1}^{N-1} \prod_{i}^{N-1} \frac{C_i}{C_i'} \tag{123}$$

Under no losses constraints, if, for all stages, Ccharging>Cdischarging, the output voltage of the charge pump will be higher than the theoretical output voltage vout>N*vin

The opposite is also true. If, for all stages, Ccharging<Cdischarging', the output voltage of the charge pump will be lower than the theoretical output voltage (Vout<N*Vin). This would be true regardless of losses. **That is, even operating the charge pump in open-circuit conditions under ideal circumstances, the maximum theoretical voltage attainable would never be reached.**

In the previous section, we observed that NMOS present the sought after behavior. Their capacitance is higher during charging and smaller while discharging. This is probably because during the discharging state, VGS and VGD is 0.3V smaller than during the charging state. This potentially shrinks the channel and decreases the capacitance.

Between the two available options, LVTNFET and Egncap, note that the capacitance of LVTNFET during discharging topologies presents, for a voltage range of (0-0.3 V) a capacitance several times smaller than Egncap capacitors for the same size. This is to be expected for a FDSOI capacitor as compared to a bulk one, given that the

PMOS transistors will present the opposite effect, what makes them unsuited for implementation as fly-capacitors.

These equations are very cumbersome to operate with, especially given that the capacitance might present non-linear relationships with Voltage. However, in subsequent sections a numerical analysis in the form of an algorithm is presented that can, in well-behaved Capacitance-Voltage curves, be used to extract the values of the Capacitances at the operating point of the circuit, and the maximum output voltage that can be attained.

6.1.4. Algorithm for the determination of the Thèvenin Voltage and capacitance values of voltage dependent capacitors

Let's assume that we have a charge pump in an open circuit configuration, with no losses and no parasitic capacitances.

Let's assume, like we have during all our previous derivations, that the input voltage is Vin, and the voltage provided by the clock is also Vin.

The first capacitor, in steady state under no-losses conditions will eventually be charged to a voltage Vin during the charging semi-period.

$$V_{c1} = Vin = \frac{Q}{C_1} \tag{124}$$

When a commutation takes place, the equivalent DC circuit that capacitor 1 sees is the one in Fig. 6.2.

If we manage to express the value of C_1' as a function of V_next (in this case, V_next is the voltage V_{C2}):

$$C_1' = f(V_{c2}) \tag{125}$$

KVL tells us that:

$$-V_{in} - \frac{Q}{f(V_{c2})} + V_{c2} = 0 \tag{126}$$

We can define a function $g(V_{c2})$ such that:

$$g(V_{c2}) = -V_{in} - \frac{Q}{f(V_{c2})} + V_{c2} \tag{127}$$

If we can find the value of V_{c2} that solves the equation:

$$g(V_{c2}) = 0 \tag{128}$$

We have found the DC operating point of capacitor 2 during its charging semi-period (Vc2Q). Having found Vc2, inputting this value in the function $f(V_{C2} = V_{C2}Q)$, gives us the value of C_1'

$$f(V_{C2}Q) = C_1' \tag{129}$$

We can now follow the same procedure to obtain the voltage and capacitance values of the next stage.

An approximate algorithm would be:

1. Set two test benches for the capacitive component under test; one for the charging semi-period, and one for the discharging semi-period.
2. Obtain the curves C(V_next) and C(V_prev)
3. Extract the data of those curves.
4. With a curve fitting tool, obtain the best available expression (polynomial, logarithmic, exponential…) for those curves. i.e: C(X)=a0*x^n+ a1*x^(n-1)+...+an
5. Start with the first stage:
    a. Steady State with no losses
    b. Vc1=Vin
    c. C1=C(V_prev=Vin)
6. Determine Q1:

$$Q1 = C1 * V_{C1} = C1 * V_{in} \tag{130}$$

7. Define g(Vc2)

$$g(V_{C2}) = -V_{in} - \frac{Q1}{C_1'(V_{C2})} + V_{C2} \tag{131}$$

8. Apply a numerical method to solve for g(Vc2)=0
9. Once the value of Vc2 is known, solve for C'1

$$C1' = C(V_{next} = V_{C2}) \tag{132}$$

10. Once C'1 is known, solve:

$$V_{C1}' = \frac{Q1}{C_1'(V_{C2})} = V_{in} * \frac{C_1}{C_1'} \tag{133}$$

11. Use the value of VC1' to determine the value of C2:

$$C2 = C\left(V_{prev} = V'_{C1}\right) \quad (134)$$

12. Repeat from step 6, this time setting:

$$Q2 = C2 * V_{C2} \quad (135)$$

Repeat until the Vout stage is reached. This is the Thèvenin Voltage.

This algorithm also provides a means to obtain the capacitance of the different fly-capacitors.

The algorithm can be expanded to include the effect voltage drop due to the presence of a load, and the effect of parasitic capacitances.

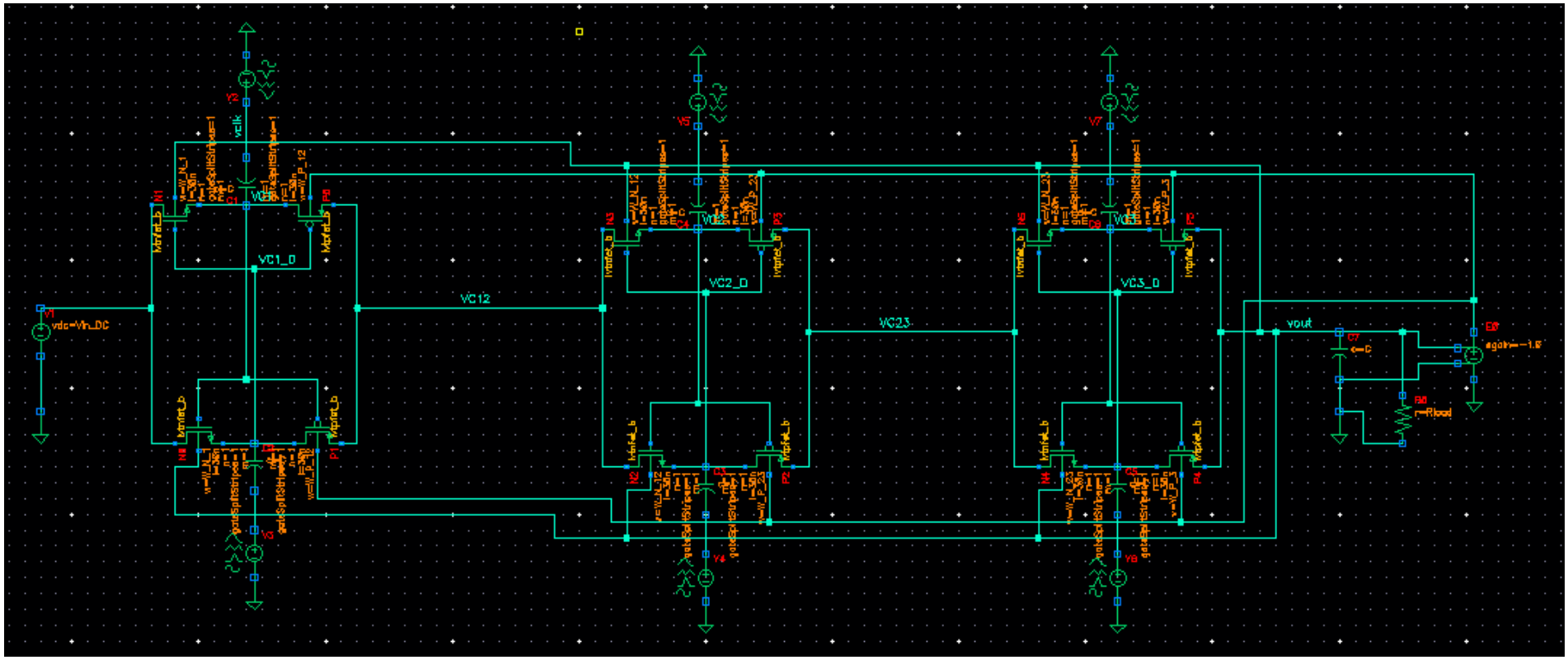


Fig. 6.10: CC-CP Schematic implemented with FDSOI technology. The Back Bias is provided by the output node. In the case of the PMOS transistors, an ideal voltage buffer with gain -1 is used (slightly altering the real effects of the circuit). The clocks are implemented with out of phase square-wave generators.

6.2. Exploring the behavior of Low Voltage Threshold FETs as resistive switches in an idealized test-bench.

In order to study the behavior of LVTFETs as resistive switches, we follow a procedure similar to that of section 6.1. That is, we design a test-bench representative of the transistor's behavior during circuit operation (Fig. 6.11) and perform parametric sweep of variables of interest.

Although we first test each transistor individually, some transistors form resistive pairs. That is, intermediate stages present resistive paths comprised of the series combination of NMOS and PMOS transistors. Their joint behavior is significant and is also explored.

Once the resistive characteristics of the components have been defined, the conclusions extracted are summarized in a design guide. Finally, an example case 3-stage CC-CP is built with Cadence, using LVTFETs as resistive switches and ideal fly-capacitors. By using ideal capacitors, the effect of voltage-dependent capacitors can be eliminated from the results. The circuit is shown in Fig. 6.10. This circuit is used to determine whether the equivalent resistance equations derived in section 5 hold when the implementation of the CC-CP is FSOI based.

6.2.1. LVTFET empirical analysis. Test-Benches and procedures.

Fig. 6.11 illustrates the test-bench implemented to perform the analysis on the resistive characteristics of the transistors. There are two variables of interest or, rather, two variables that can be controlled. Since we are considering minimum length transistors (30nm), those variables are the width of the transistors, and the back bias. These are the variables that will be swept.

Initially only the width of the different transistors is taken into account. The transistors are divided into two categories: PMOS and NMOS. They are then divided according to their stage.

- NMOS
  - Stage 1 (N1)
  - Stage 2 (N2)
  - Stage 3 (N3)
- PMOS
  - Stage 1 (P1)
  - Stage 2 (P2)
  - Stage 3 (P3)

The transistors that form resistive pairs are:

- N2+P1
- N3 + P2

Transistors N1 and P3 each operate as sole resistances (see Fig. 6.10).

For any transistor, VD, VS and VG are different and unique. These values can be approximated via the equations below if the expected output voltage is known.

$$\widehat{V_1} = \frac{V_{in} + \widehat{V_2}}{3}$$

$$\widehat{V_2} = \frac{3 * \widehat{V_3} + V_{in}}{5}$$

$$\widehat{V_3} = \frac{5 * \widehat{V_4} + V_{in}}{7}$$

	Low	High
V4	Vout	-
V3	(5*V4+Vin)/7	V3+ Vin
V2	(3*V3+ Vin)/5	V2+ Vin
V1	(V2+ Vin)/3	V1+ Vin

P3	
VD	V4
VS	V3+ Vin
VG	V3

N3	
VS	V3
VD	-
VG	V3+ Vin

P2	
VD	-
VS	V2+ Vin
VG	V2

N2	
VS	V2
VD	-
VG	V2+ Vin

P1	
VD	-
VS	V1+ Vin
VG	V1

N1	
VS	V1
VD	Vin
VG	V1+ Vin

The empty boxes illustrate a priori unknown VD values for the transistor pairs based solely on the provided equations. This is because the transistor pairs form a voltage divider.

Knowing that:

$$R_{ds}(N3) + R_{ds}(P2) = R$$

$$R_{ds}(N2) + R_{ds}(P1) = R$$

The node VD of each pair of transistors forms a voltage divider and its voltage value will depend on the value of the resistances on either side.

Since initially we do not know what the values of these resistances are, we can approximate the value of VD for either case.

So, for transistor pair N3-P2:

$$V_d = \frac{V_s(P_2) + V_s(N_3)}{2}$$

And for pair N2-P1:

$$V_d = \frac{V_s(P_1) + V_s(N_2)}{2}$$

This is especially valid when R is low, given that in that case we would expect the resistances on either side of node VD to be similar.

Otherwise it is necessary to decide beforehand an approximate value for the resistances on each side and calculate VD more accurately.

With these considerations in mind, VD, VS and VG are calculated for each transistor using the above equations for a value of Vout of 1.2 volts. VB is fixed at -1.2 V for the PMOS and 1.2 for the NMOS transistors (the ideal maximum output voltage attainable by a 3-stage CC-CP with Vin=0.3 V).

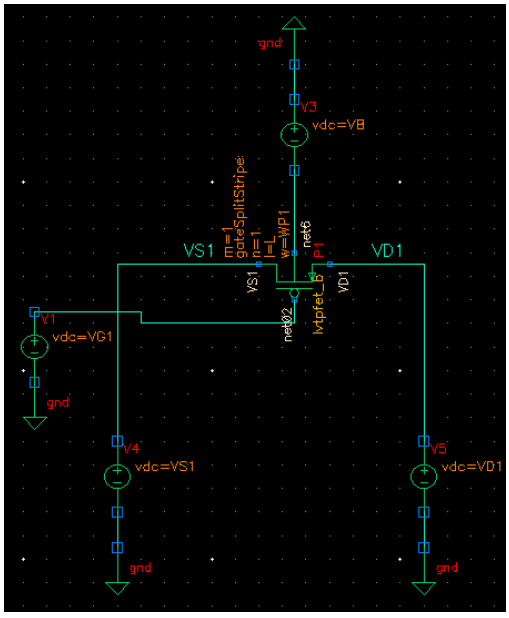


Fig. 6.11: Transistor implemented as a resistance.

A DC parametric sweep of the width of the transistors is made, obtaining the results described below, capturing the value of the transistor resistance and threshold voltage.

We observe that:

- NMOS

  Increasing stages imply increasing resistance and threshold voltage for a fixed width. This trend is consistent with behavior expected of longer transistors (Fig. 6.13), where:

$$R_{ds} \propto \frac{1}{W(V_{gs} - V_{th})}$$

  when $V_{ds} \ll (V_{gs} - V_{th})$.

  For each stage, VGS is approximately constant and equal to Vin (in this case, 0.3 V). However, Vth increases for each stage, potentially due to the body effect. Increased width also influences the Vth, causing its increase.

- PMOS

  The results obtained are similar, but evolve in the opposite fashion. For a fixed width, resistance decreases with each increasing stage (Fig. 6.14).

Fixing a transistor width, and performing a DC sweep of the Back Bias voltage for the different stages yields the following Resistance-Back Bias dependence:

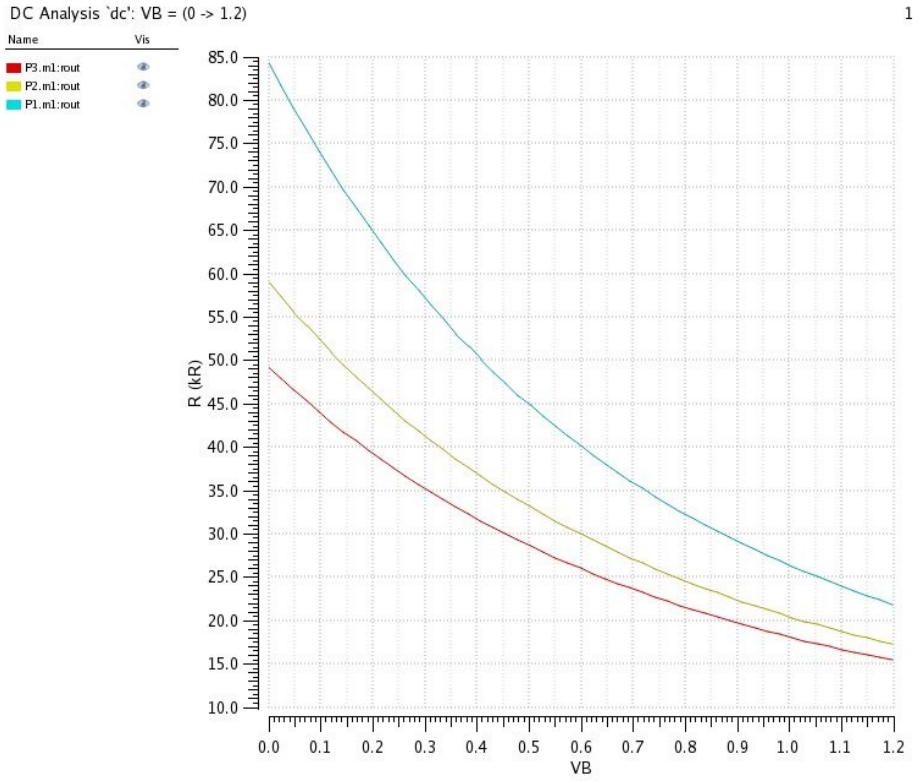


Fig. 6.12: Resistance vs Back Bias voltage for different stages (PMOS transistors)

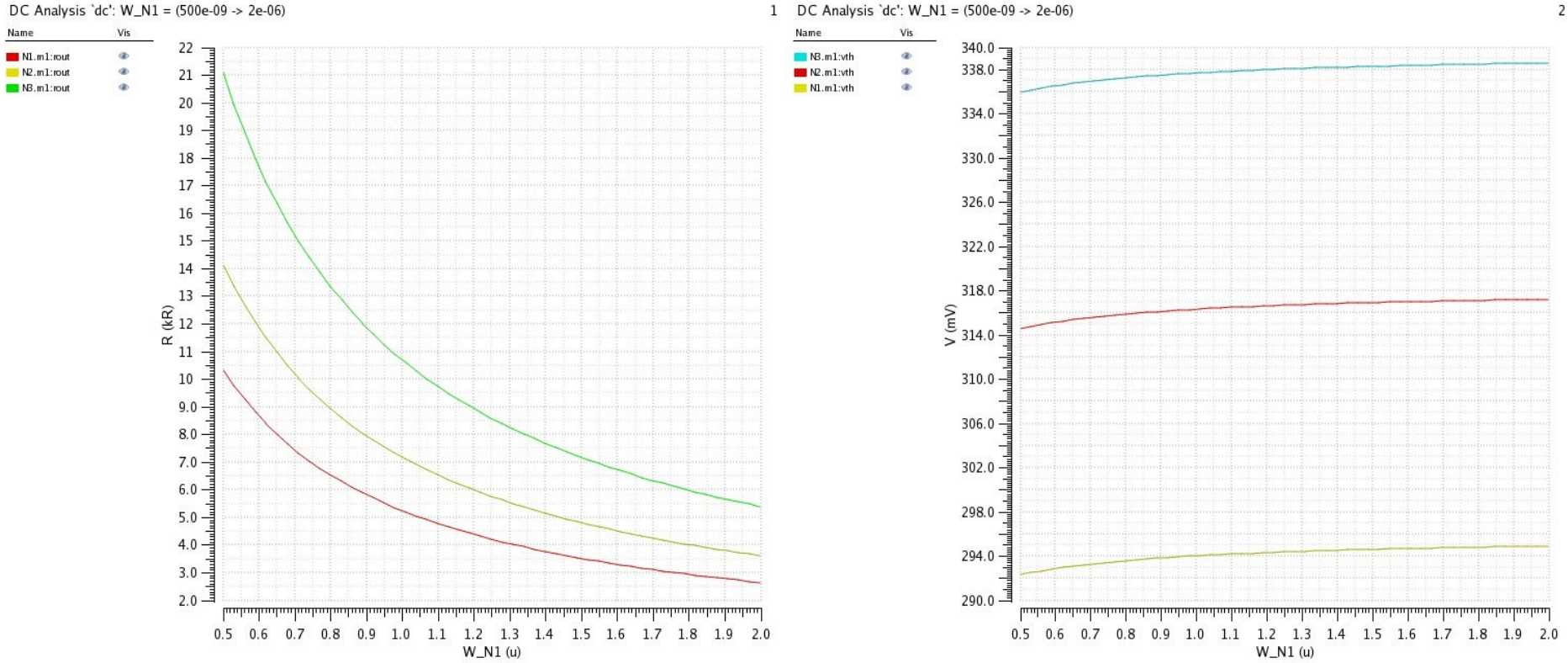


Fig. 6.13: Resistance and Vth as a function of width for the NMOS under approximately operating conditions for all stages (N1 corresponding to the NMOS of the first stage and so on).

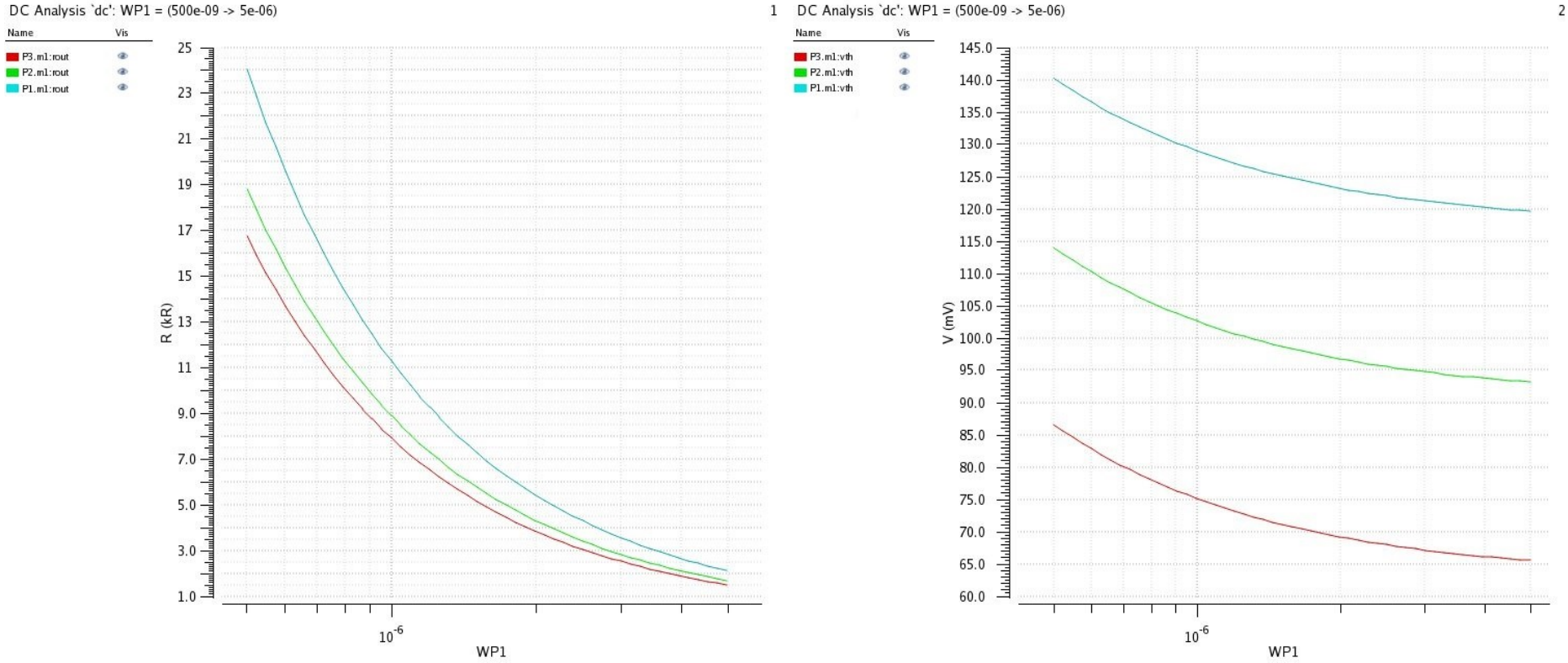


Fig. 6.14: Resistance and Vth as a function of width for the PMOS under approximately operating conditions for all stages.

From the figure above we see that, under operation conditions, decreasing the absolute value of the Back Bias increases the transistors resistance. This is valid for both types of transistors.

It is also of interest to study jointly the resistance curves of transistor pairs. Fig. 6.15 depicts, in the same plot, the resistance-width characteristic of transistor pair N2-P1 for a fixed Back-Bias. The effective resistance of the equivalent topology these transistors form will be the sum of their respective resistances.

It can be seen in Fig. 6.15 how both transistors present a similar trend in decreasing resistance with increased width, and a given offset separating both of them. In this case, transistor N2 presents an overall smaller resistance than transistor P1 for the same width values. However, this is not always the case.

Fig. 6.16 depicts the resistance-width characteristic of transistor pair N3-P2 for a fixed Back-Bias. In this case, the NMOS has an overall higher resistance than the PMOS for the same width values.

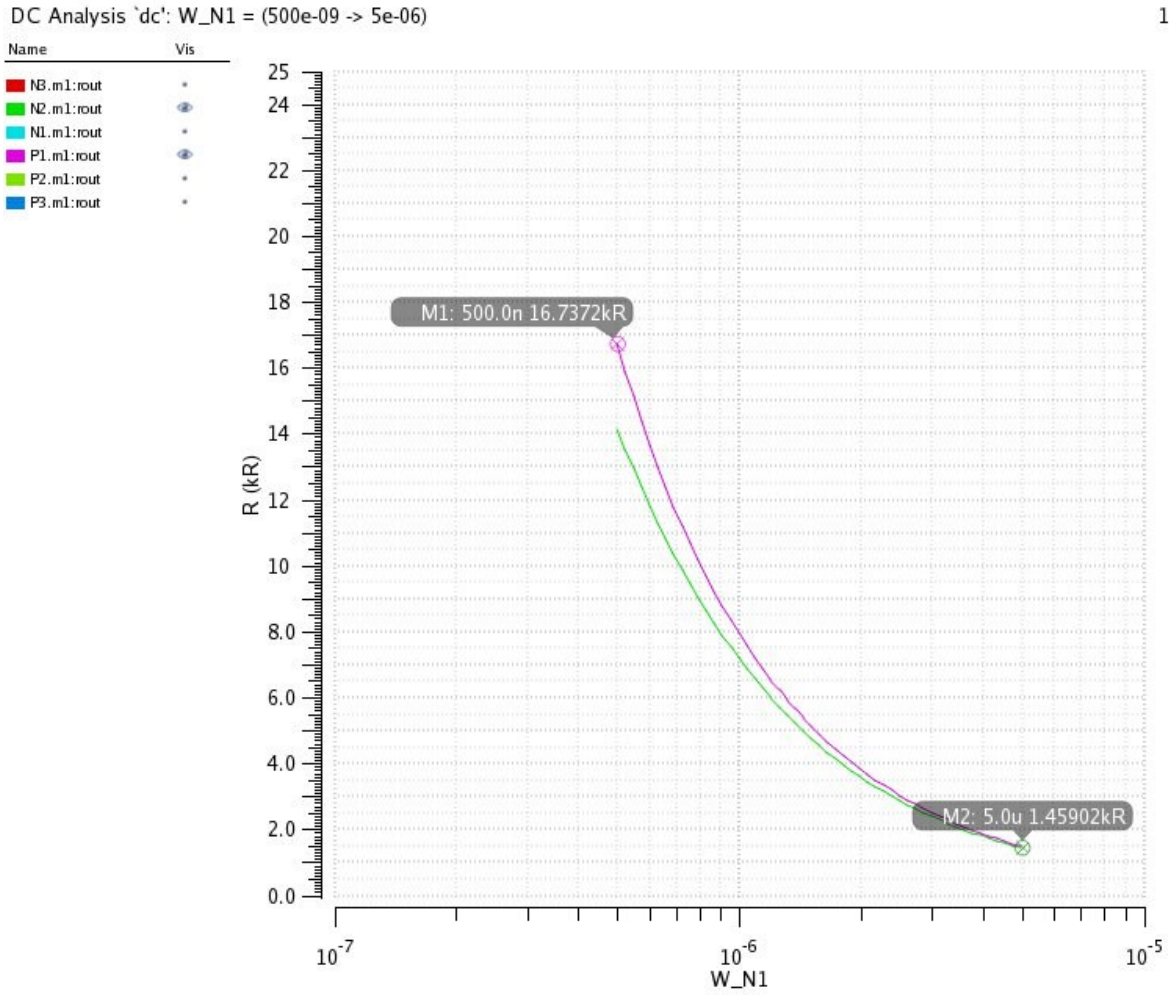


Fig. 6.15: Resistance vs Width of transistor pair N2-P1. In green, transistor N2. In purple, transistor P1.

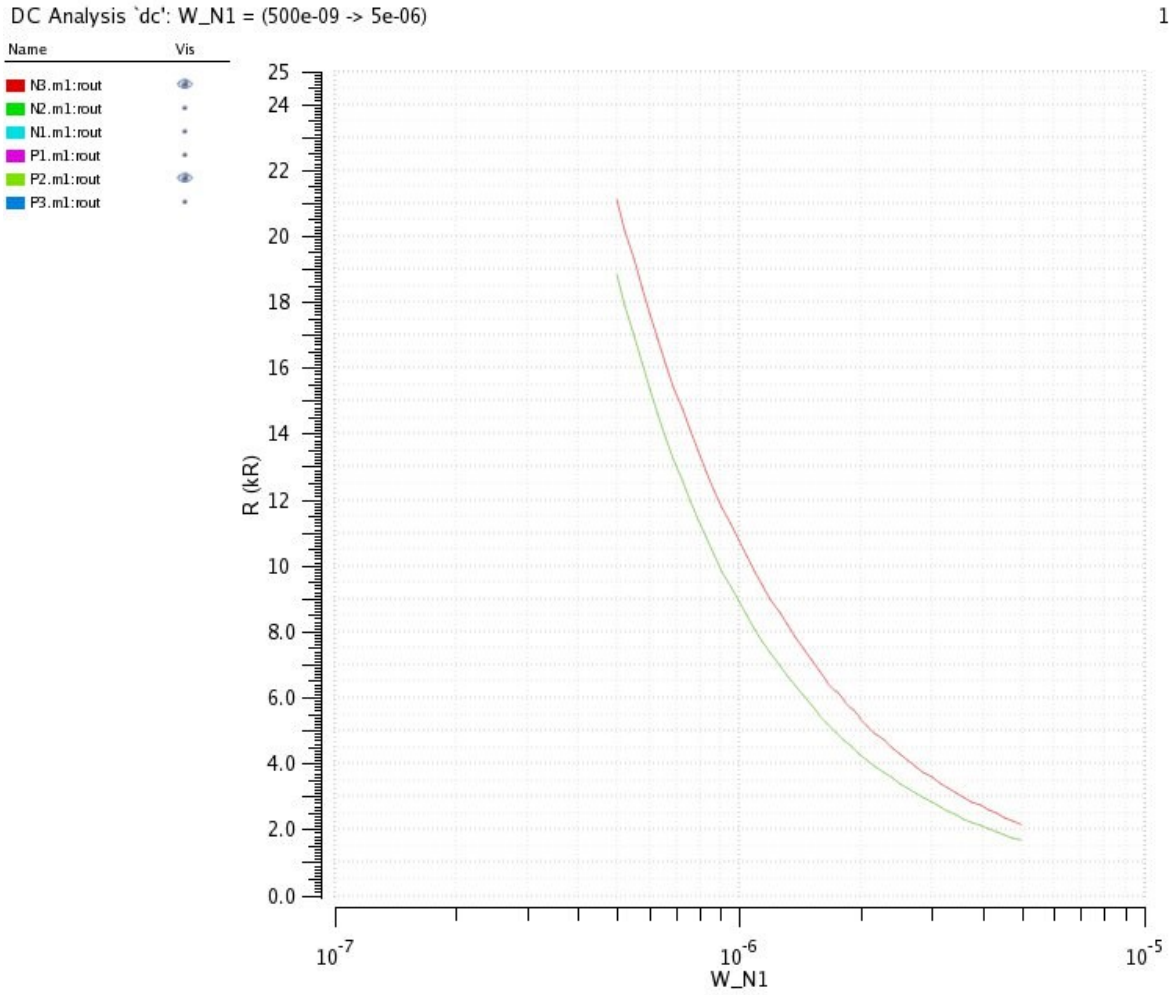


Fig. 6.16: Resistance vs Width of transistor pair N3-P2. In pink, transistor N3. In green, transistor P2.

These curves show that, due to the biasing within the CC-CP, in some stages, PMOS transistors can exhibit lower resistive values than NMOS, contrary to expectations. Because of this phenomenon, optimizing area (choosing the minimum transistor-combination width possible to reach a given resistance) can be different for each stage. And in some stages, it consumes less area to make PMOS transistors more conductive than NMOS.

6.2.2. Thèvenin equivalent validation procedure in an implementation with LVTFETs as resistive switches.

This section follows the procedures used to determine whether the theoretical analyses relating to the Thèvenin equivalent model as presented in previous sections still hold when applied to implementations in complex technologies. This section focuses on the effect of FDSOI LVTFET.

This section considers a 3-stage CC-CP, an implementation of which is performed considering the follow steps. The results of the implementation can be found at the end of this section.

1. Determine the input resistance/ leakage current of the circuit the charge pump will be connected to.
2. Determine the desired output voltage of the charge pump
3. Determine the value of the required Thèvenin Resistance of the circuit using the voltage divider equation.

$$V_{out} = V_{thèvenin} * \frac{R_{load}}{R_{Th} + R_{load}}$$

If technological parameters are available, consider the effect of the top plate parasitic capacitances and assume that the Thèvenin voltage is equal to:

$$V_{thèvenin} = V_{in} + 3V_{in} * \frac{C}{C + C_p}$$

Otherwise a worst case scenario where the parasitics represent the 20 % of the capacitances can be adopted.

4. Solve the equation of the equivalent resistance to obtain the needed switch resistances:

$$R_{Th} = \frac{7}{4} * \frac{1}{fC} * \coth\left(\frac{1}{2fR_{sw}C}\right)$$

$$R_{sw} = \frac{T}{2C * \coth^{-1}\left(\frac{4fR_{Th}C}{7}\right)}$$

(Note that the switch resistance of transistor N1 must be **half** this value).

5. Using the equations and tables presented in the previous section, calculate VG, VS and VD for all the transistors

6. Perform a parametric sweep of the width of each transistor.

7. Choose a width for transistor N1 so that $R_{ds} = \frac{1}{2}R_{sw}$. This value is unique under operating conditions

8. Choose a width for P3 so that $R_{ds} = R_{sw}$. This value is unique under operating conditions.

9. Choose a width for transistor N2 and one for transistor P1 so that

$$R_{ds}(N2) + R_{ds}(P1) = R_{sw}$$

10. Choose a width for transistor N3 and one for transistor P2 so that

$$R_{ds}(N3) + R_{ds}(P2) = R_{sw}$$

11. Steps 10 and 11 can be carried out in such a way that the desired resistance is obtained while minimizing the combined width.

12. Set the Charge Pump with the values obtained. Perform a transient analysis in open circuit (no load). Note the output voltage.

13. Perform a transient analysis with the load included. Note the output voltage.

14. If the output voltage with the circuit loaded is within acceptable values, the initial design is finished. Otherwise, repeat steps 3-14 considering the Thèvenin voltage to be that obtained in step 12.

Following the above steps, a first test-design is proposed. A 3-Stage CC-CP, with $V_{in} = 0.3\,V$ and an ideal Vout of 1.2 V. We are designing the circuit so as to have equal capacitances and RC time constants for all topologies.

- Resistive load of 200 kΩ (this value is chosen arbitrarily).
- Targeted output voltage when loaded of 1.11 V
- We assume that Back Bias voltage will be 1.10 V, a value slightly smaller than the targeted output voltage.
- Switching frequency of 2 MHz.
- All capacitances, equal to 500 pF. We use ideal capacitors and very large capacitive values to minimize the effect of parasitic capacitances.

Other that high capacitive values, the rest of parameters are somewhat arbitrarily chosen and serve only to showcase the validity of the theoretical and empirical analysis so far performed.

With these values, we assume the effect of parasitic capacitances negligible. The Thèvenin Voltage can then be approximated as the ideal 1.2 V.

Solving the voltage divider equation, we calculate the equivalent resistance needed to operate at 1.11 V.

$$V_{out} = V_{thèvenin} * \frac{R_{load}}{R_{Th} + R_{load}}$$

$$R_{Th} = 18.180\ k\Omega$$

With this value, it is possible to determine the required transistor resistances.

$$R_{sw} = \frac{1}{2fC * \coth^{-1}\left(\frac{4fR_{Th}C}{7}\right)}$$

$$R_{sw} = 5.180\ k\Omega$$

Which we approximate to 5 kΩ. Note that these values are not intended to be representative of real implementations. Rather, the purpose is to show that the models hold regardless.

We now design the transistors so that they exhibit an equivalent On resistance of 5 kΩ. As per the previous section:

- N1 → 2.5 kΩ
- N2+P1 → 5 kΩ
- N3+P2 → 5 kΩ
- P3 → 5 kΩ

We set test-benches as described in the previous section utilizing the equations for the mean voltages and the tables pertaining to each transistor. All values represent mean voltage approximations.

	Low	High
V4	1.11 V	-
V3	0,836 V	1,136 V
V2	0,561 V	0,861 V
V1	0,287 V	0,587 V

P3	
VD	1.11 V
VS	1,136 V
VG	0,836 V

N3	
VS	0,849 V
VD	0,861 V
VG	1,136 V

P2	
VD	0,836 V
VS	0,849 V
VG	0,561 V

N2	
VS	0,574 V
VD	0,587 V
VG	0,861 V

P1	
VD	0,561 V
VS	0,574 V
VG	0,287 V

N1	
VS	0,287 V
VD	0,3 V
VG	0,587 V

Where, for the transistor pairs N3-P2 and N2-P1, we have used:

$$V_d = \frac{V_s(P) + V_s(N)}{2}$$

With these values, the test-benches are set and parametric sweeps on the width of the transistors are performed, with a constant back bias of 1.1 V. The widths are chosen. TABLE XIII summarizes these results.

TABLE XIII: Transistors' width and resistances

	Width (um)	Resistance (kΩ)	Joint Resistance (kΩ)
N1	2,13	2,498	-
N2	2,9	2,487	4,993
P1	3,08	2,506	
N3	3,54	3,063	5,066
P2	4,23	2,003	
P3	2,16	4,994	-

The circuit is implemented with the above widths for each transistor and the parameters established at the beginning.

The circuit is then simulated without a load. The transient simulation stabilizes at an output voltage of 1.19688 V (Fig. 6.17). This represents a 0.26 % relative error with respect to the ideal output voltage of 1.2 V when unloaded. This could be due to the small parasitic capacitances introduced by the transistors.

Introducing the resistive load of 200 kΩ we finally obtain an output voltage of 1.114 V, a value slightly above that of the initially desired (Fig. 6.18).

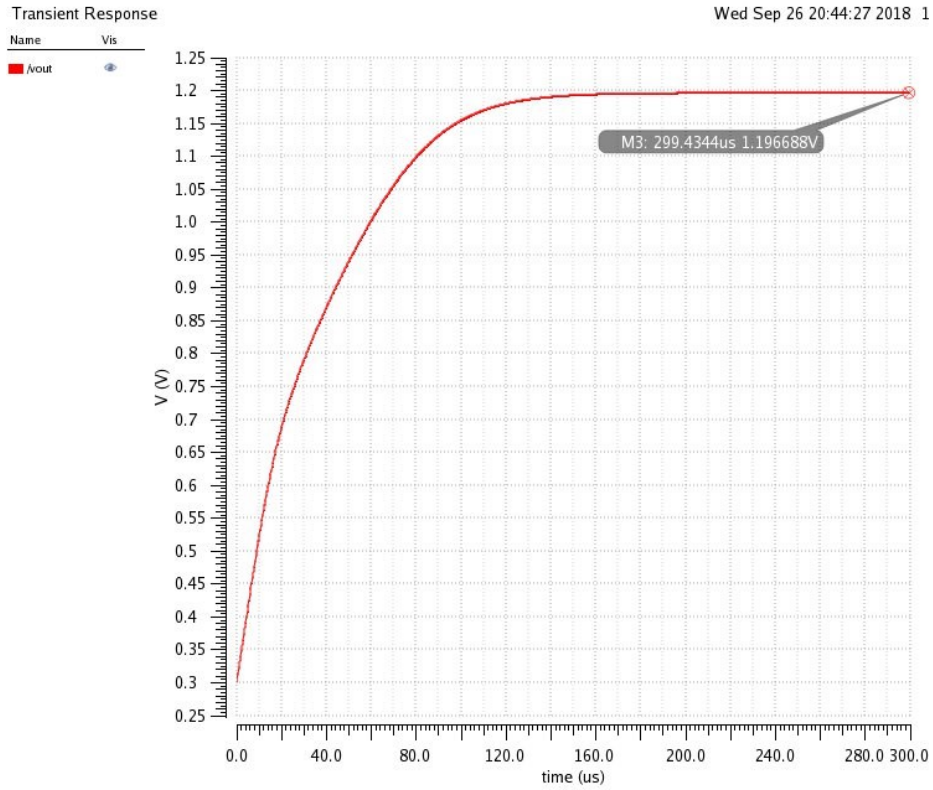


Fig. 6.17: Open circuit transient depicting the output voltage

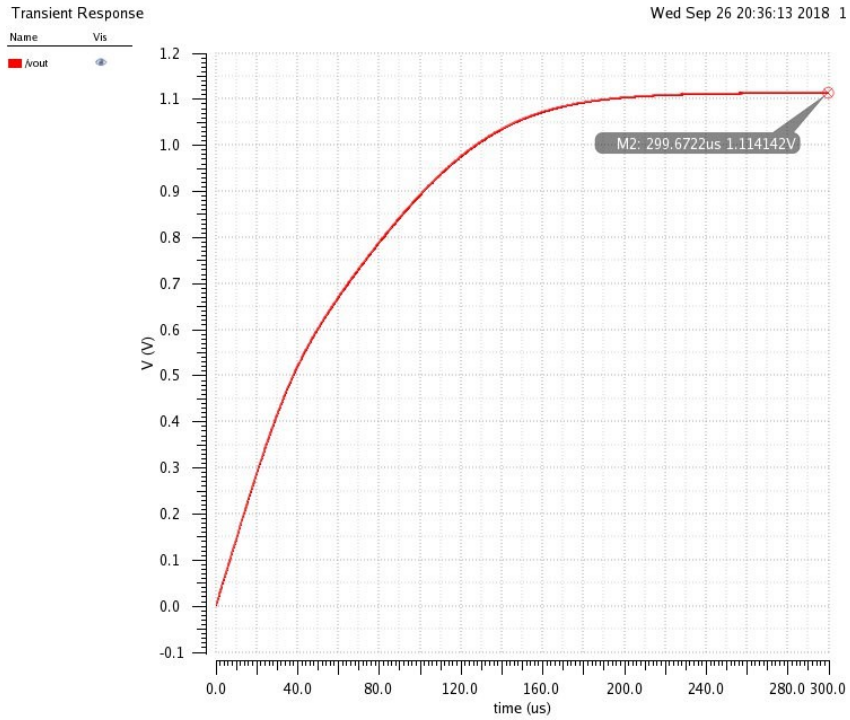


Fig. 6.18: Loaded Circuit transient depicting the output voltage.

7. Layout design

After various iterations of how best to start implementing a layout, the structure of an inverter is chosen as an initial building block. This allows for a simple, symmetrical design, where the inverter layout can be used as a standard-cell. Fig. 7.1shows the schematic representation of such and inverter.

At this point, it was deemed beneficial to use transistors of equal width for each stage, set at 500 nm. This is done to maintain a tightly symmetrical design, trying to avoid asymmetries from impacting the interpretation of the results obtained.

As per the previous figures regarding the on resistance of the transistors, a common 500 nm width would set the combined resistances of the different stages between 20-40 kΩ.

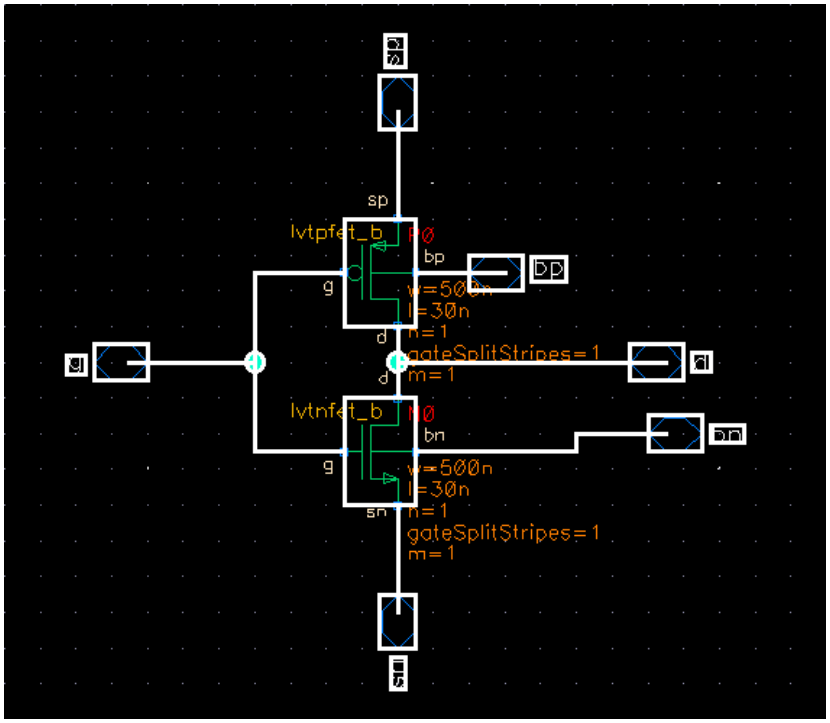


Fig. 7.1: Schematic representation of the inverter cell.

Fig. 7.2 shows the layout implementation of the inverter, where the gates are shared and the drains of both transistors are placed at the left, connected through metal 2 layers.

A second inverter is flipped and overlapped onto the previous one, and additional connections are made so as to cross-couple the inverters. Other metal layers are added to connect with the previous and next stages. Lateral connections are added for the capacitors.

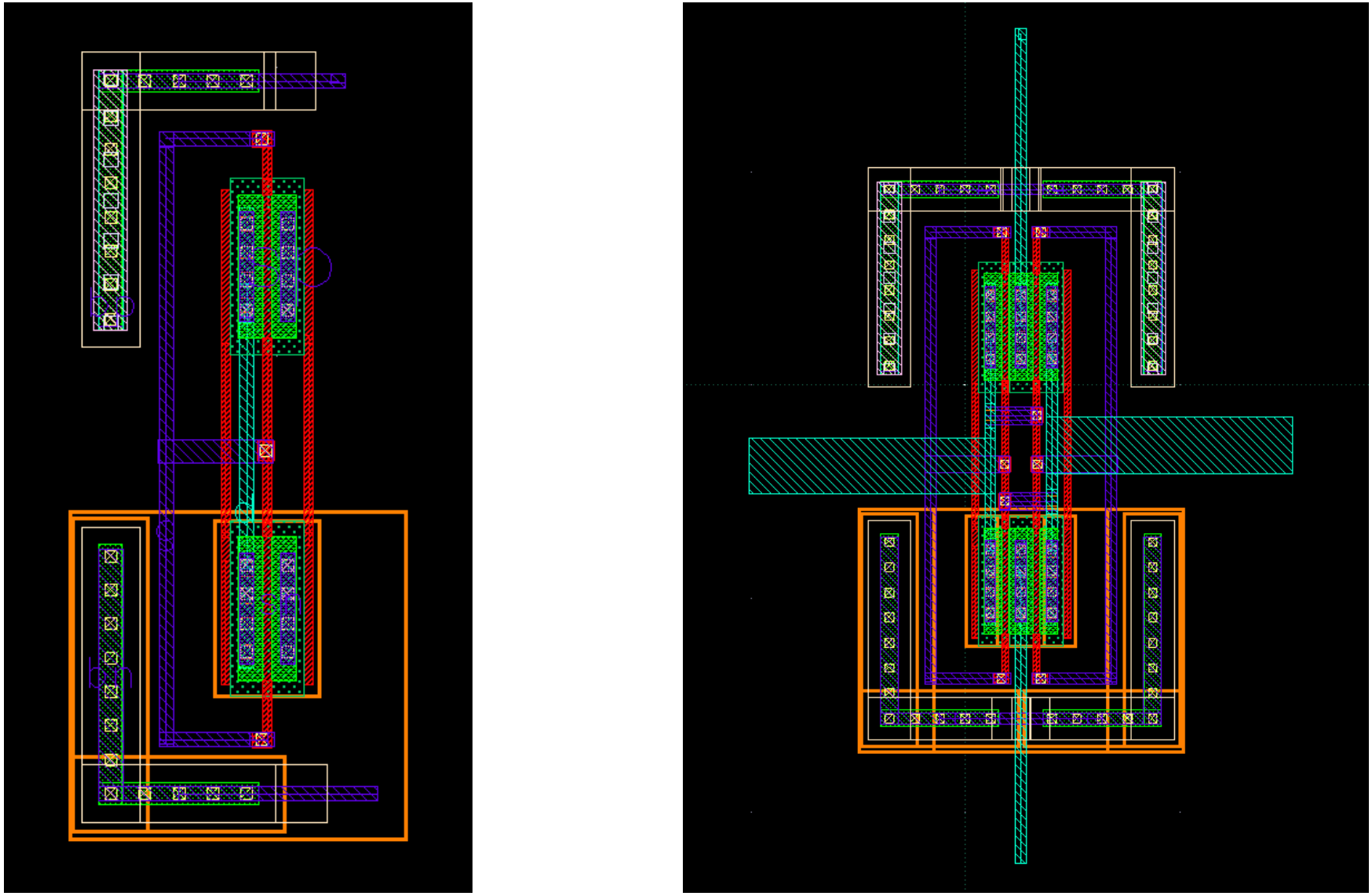


Fig. 7.2: Left) Inverter Layout. Right) Cross-coupled inverter using a flipped copy of the initial inverter. Added lateral metal layers for connection to the capacitors

Each cross-coupled cell represents a stage of the design. Keeping in line with the previous experiments and so as not to deviate too much from their results in this new step, a CC-CP of three stages is implemented (Fig. 7.3).

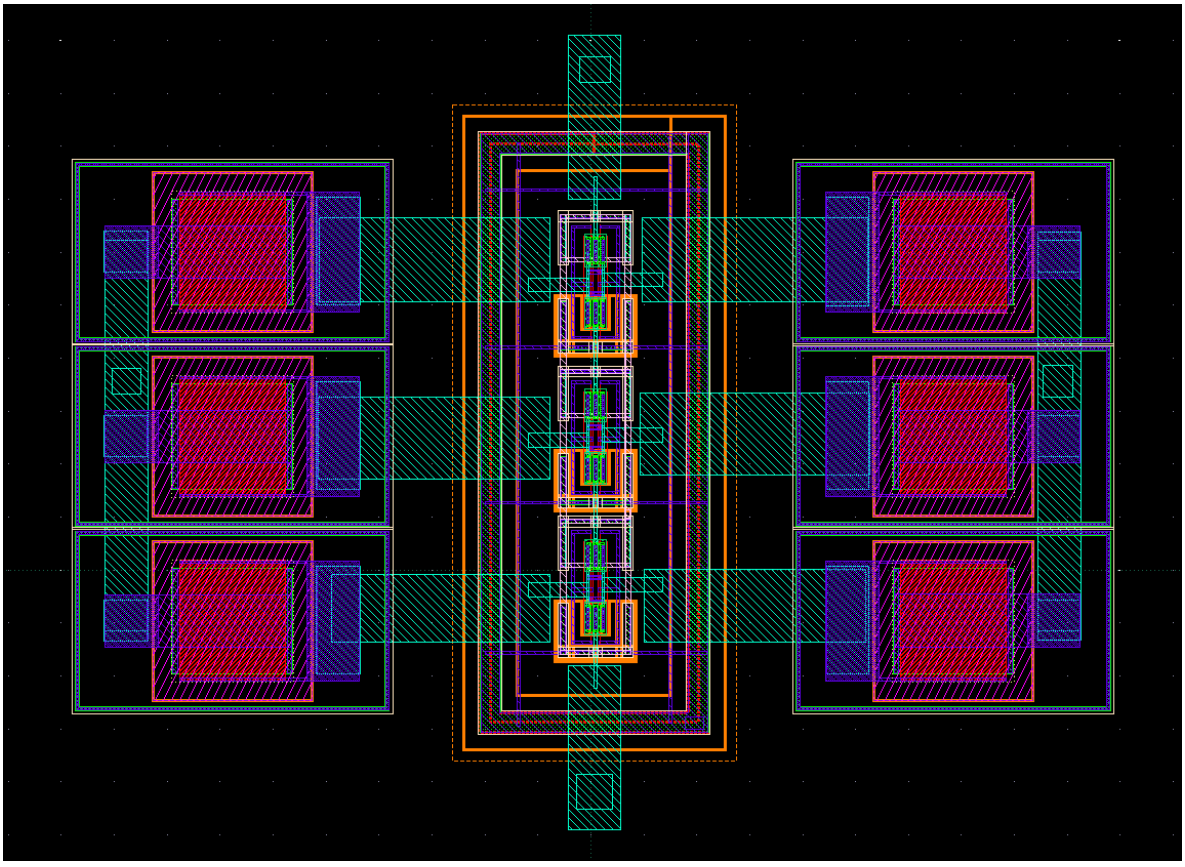


Fig. 7.3: Layout of a 3-stage CC-CP.

The outmost lateral structures represent the egncap capacitors, with a guard-ring connecting their bulk structure to the overall bulk of the die. The transistors are, meanwhile, embedded in a triple well that isolates them from the rest of the bulk, thus granting the possibility of feeding them a back-bias distinct from the die potential.

The overall size of the final structure gives rise to sufficient area so that the capacitors can have 2 um of square area. A new set of curves representing the capacitance-voltage dependency is needed to evaluate the final results. Fig. 7.4 and Fig. 7.5 depict this dependency and establish that the capacitance of the implemented capacitors is expected to be between 20 and 40 fF, depending on the stage.

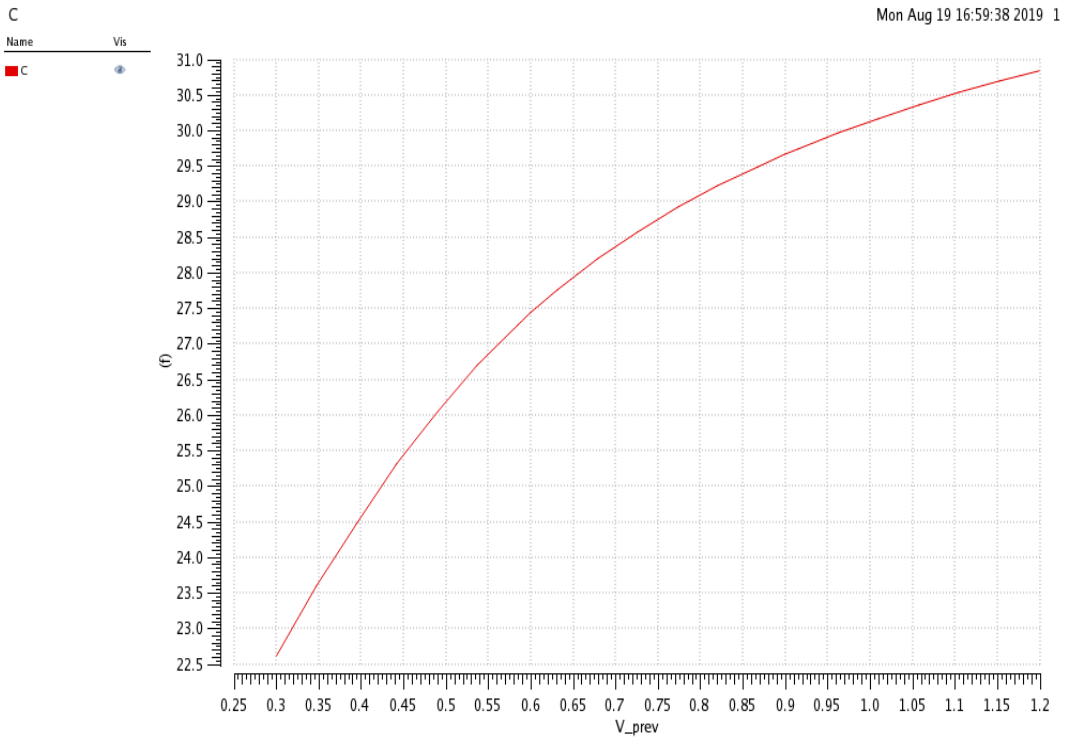


Fig. 7.4: Capacitance vs V_prev of a 2 um egncap

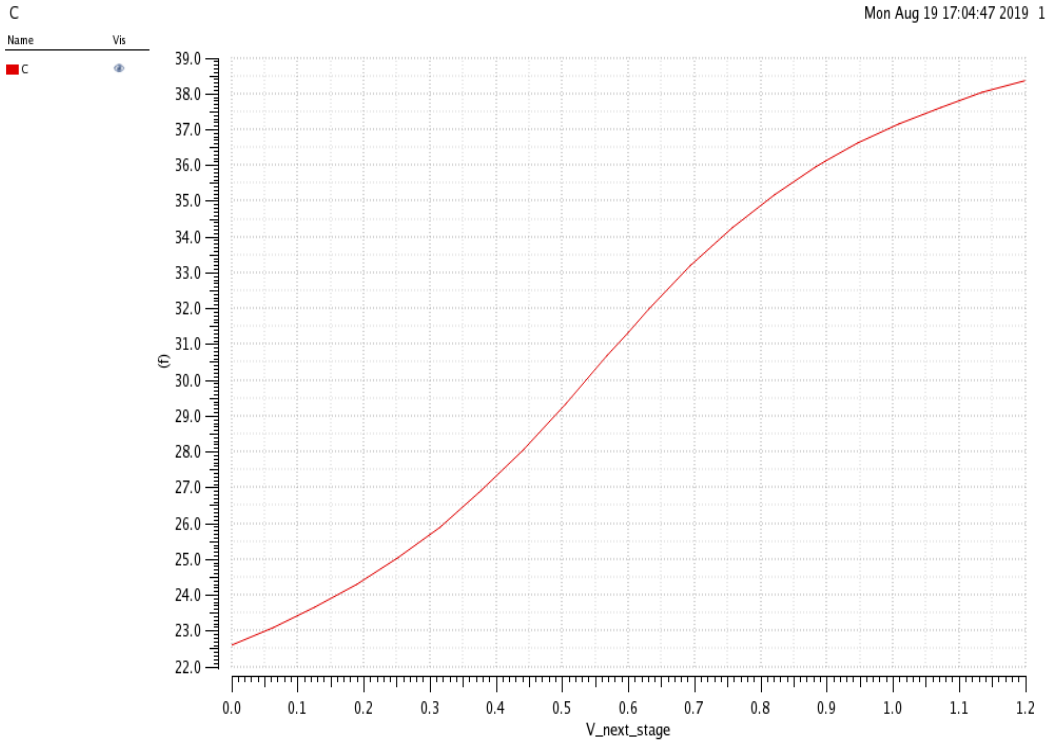


Fig. 7.5: Capacitance vs V_next of a 2 um egncap

The layout is finally extracted and implemented within a test-bench. The components of the test-bench are:

- Ideal clock at 500 MHz frequency.
- Capacitance load of 6 fF

These values are chosen to perform simulations in conditions similar to those of previous sections, so as to better interpret and compare the results obtained.

- Resistive load in parallel with the load capacitor of 1.17 MΩ (this is chosen retroactively, as it produces an output voltage of approximately 1 V in the schematic tests).
- The Back-Bias is set at |1.1| V with ideal voltage sources.

Under these conditions, both the schematic and the layout extraction are simulated. First in open circuit configuration and then with the aforementioned load.

7.1. Schematic results, open circuit configuration:

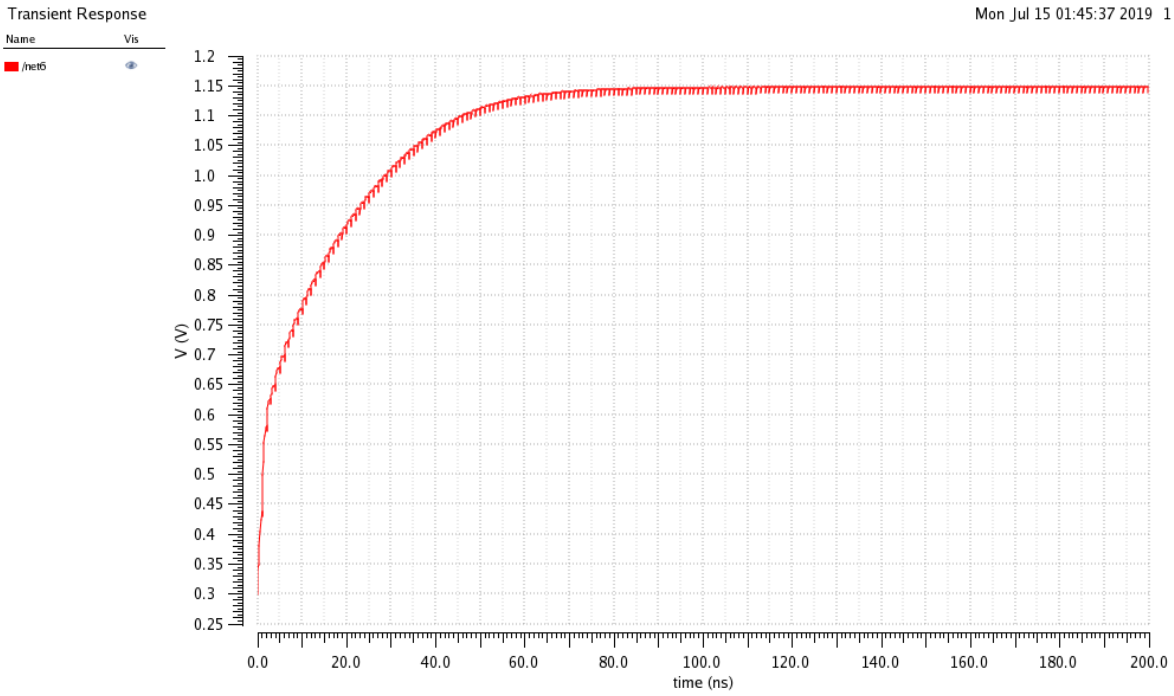


Fig. 7.6: Transient simulation, open circuit, of the schematic. Overview.

Fig. 7.6 shows the transient simulation of the schematic in open circuit configuration. The following figure illustrates the DC operating conditions, representative of the Thèvenin Voltage. Some ripple can be appreciated, specially in the form of downward voltage peaks. This is probably the result of some clock-overlapping and is the major contributor to ripple in this instance such that it can probably be considered an artifact.

The following table summarizes the results.

TABLE XIV: Schematic, open circuit results

Mean Voltage (V)	Max Volt	Min Volt	Ripple
1,148 V	1,148	1,137	11 mV

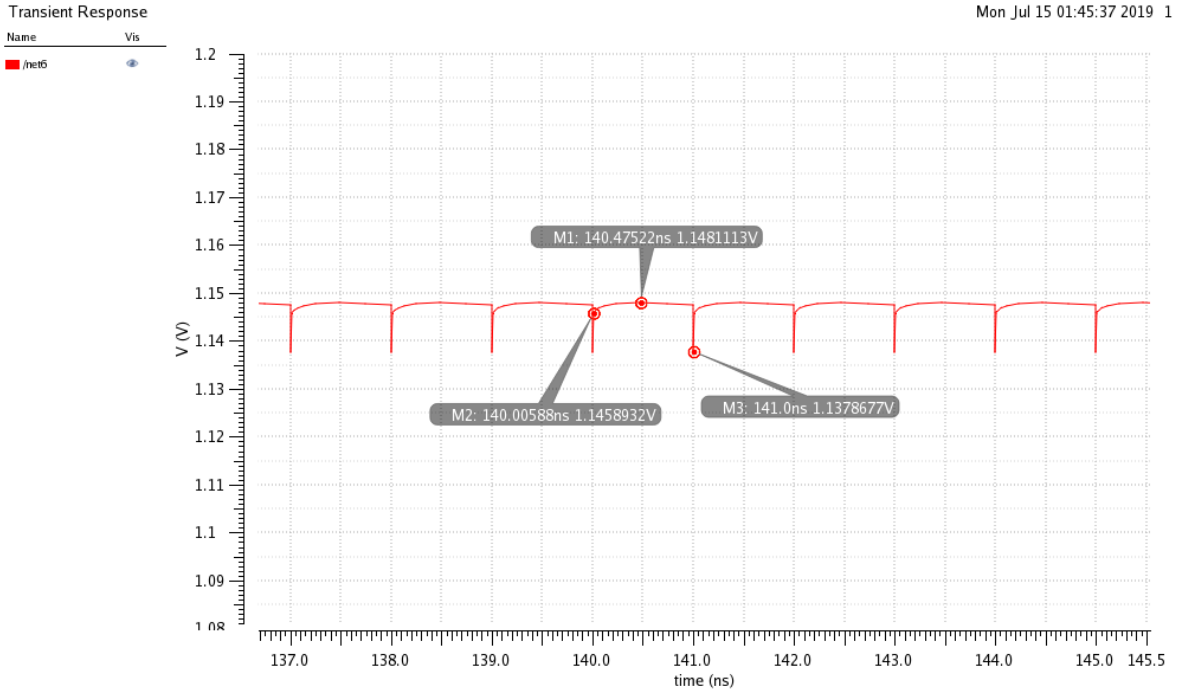


Fig. 7.7: Transient Simulation, schematic, open circuit. Zoomed in steady-state.

7.2. Schematic results, with load:

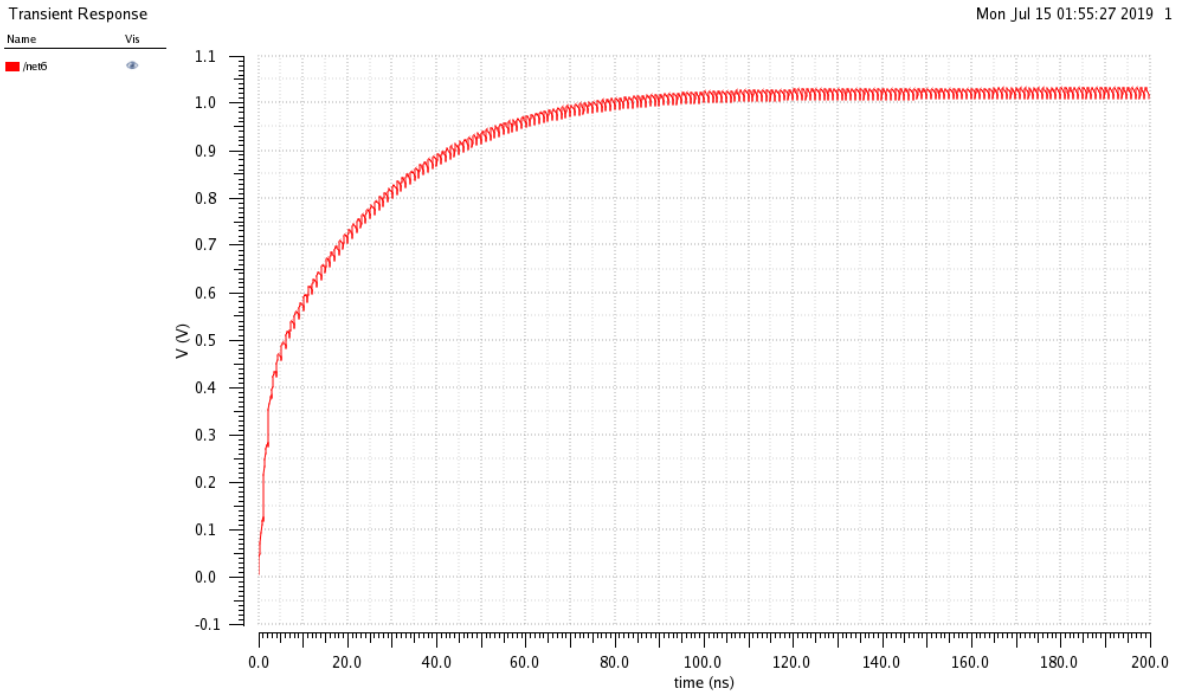


Fig. 7.8: Transient Simulation, Schematic. Loaded. Overview.

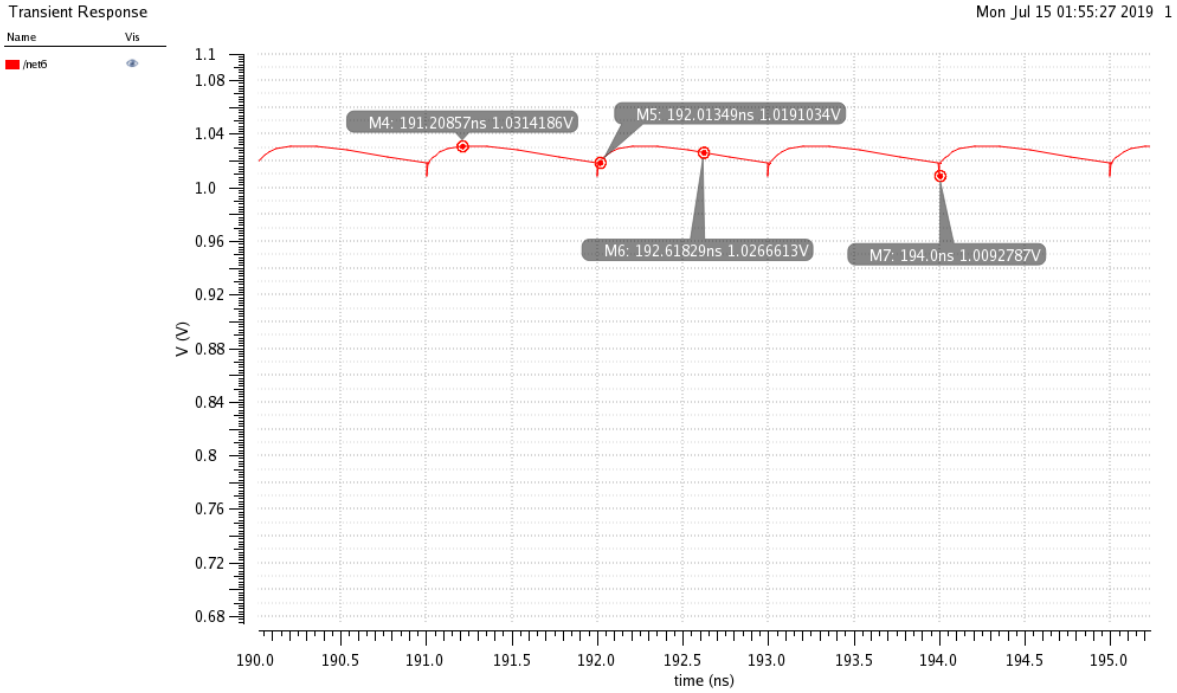


Fig. 7.9: Transient Simulation, schematic. Loaded. Zoomed.

TABLE XV: Schematic, Loaded. Results

Mean Voltage (V)	Max Volt	Mini Volt	Ripple
1,026 V	1,031	1,009	22 mV

The rise time also increases from approximately 70 ns to approximately 100 ns.

7.3. Layout, open circuit configuration.

The same remarks can be made for the results of the extracted layout simulation regarding ripple and voltage peaks. The slight overlapping clock creates downward voltage peaks that could potentially be mitigated, offering slightly better result.

The following table summarizes the results in open circuit configuration.

TABLE XVI: Layout, open circuit. Results

Mean Voltage (V)	Max Volt	Mini Volt	Ripple
1,083 V	1,085	1,075	10 mV

Note how the Thèvenin Voltage (mean voltage) is slightly inferior to that of the schematic (the mean voltages are determined through visual inspection of the plots in steady-state).

$$\Delta V_{Th} = 1.14 - 1.08 = 60\,mV$$

This is probably due to a combination of increased presence of parasitic capacitance at the critical nodes and resistive effects in combination with a slightly overlapping clock producing some forms of losses. However, the potential effect of clock-overlapping requires further study and remains, at this point, an hypothesis.

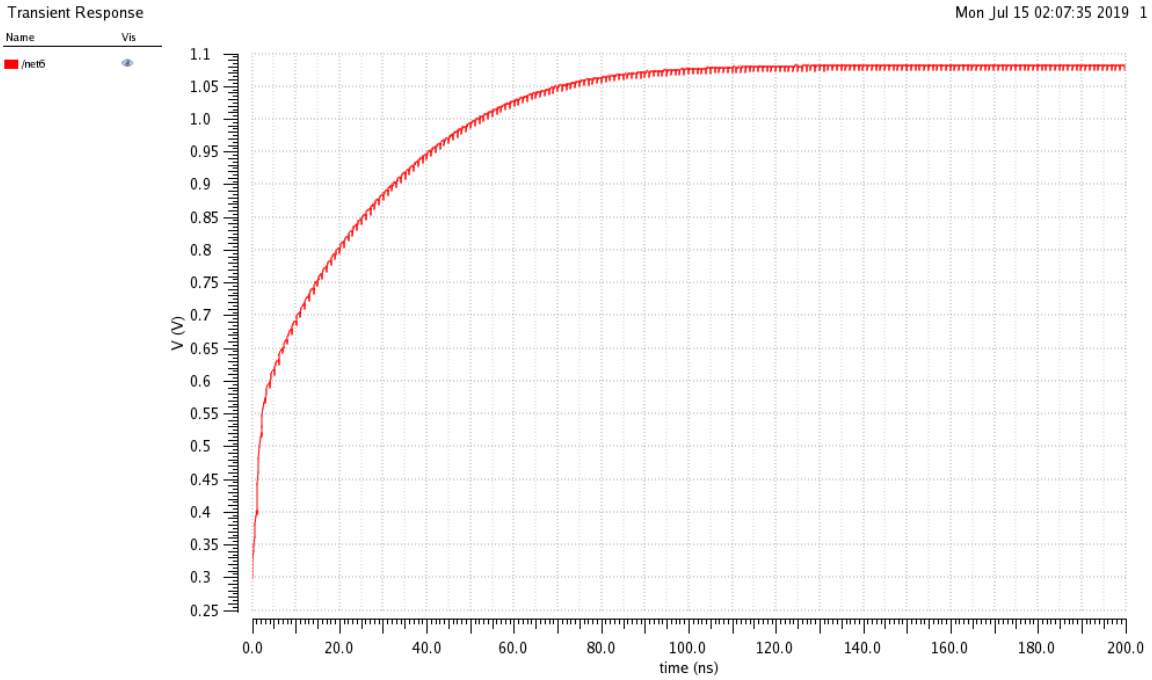


Fig. 7.10: Transient simulation. Layout, open circuit. Overview.

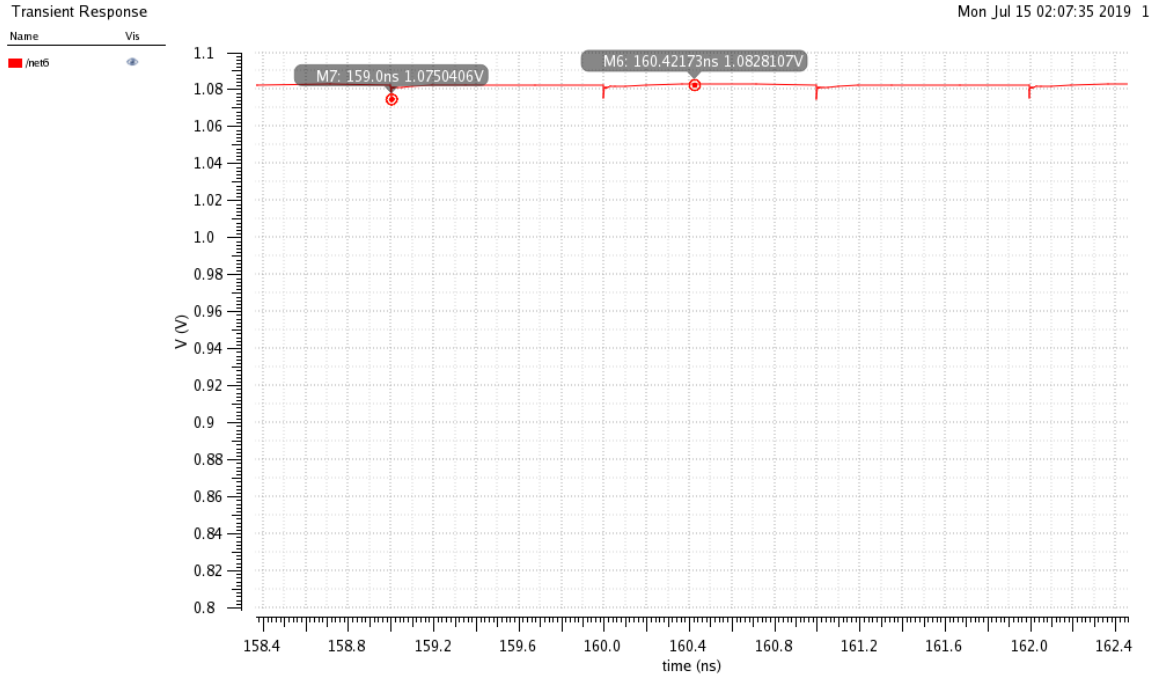


Fig. 7.11: Transient Simulation. Layout, open circuit. Zoomed.

Note also how the rising time has increased as compared to the unloaded schematic has increased from approximately 70 ns to approximately 90 ns.

7.4. Layout, loaded.

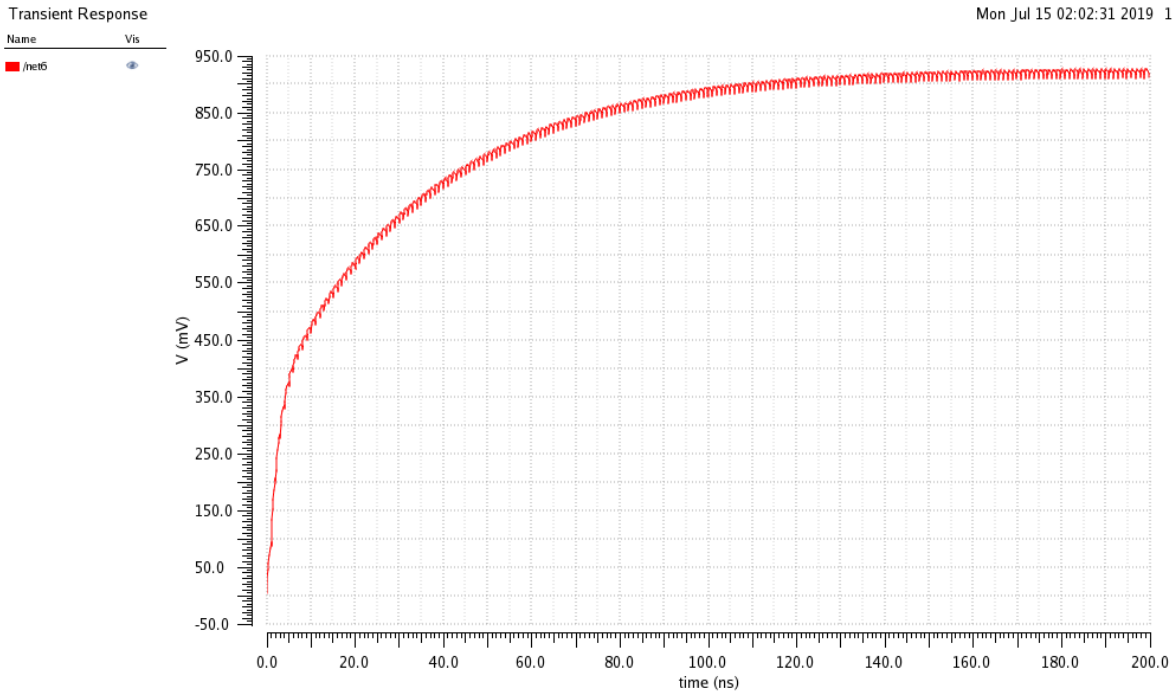


Fig. 7.12: Transient Simulation. Layout, loaded. Overview.

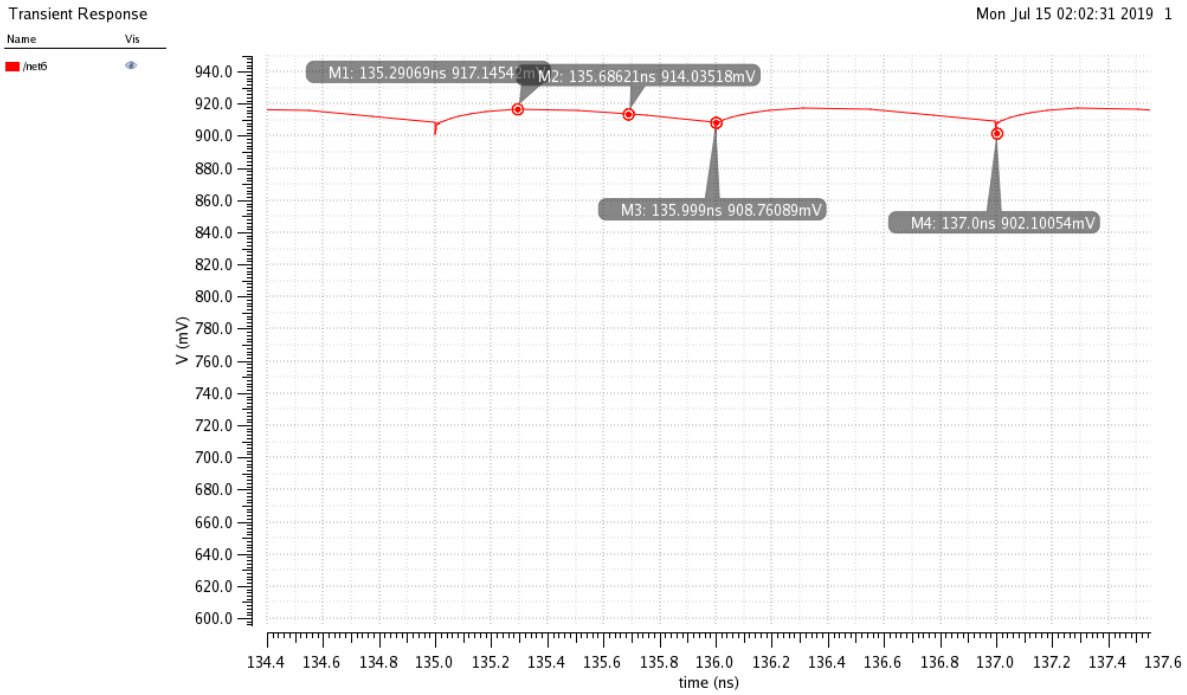


Fig. 7.13: Transient Simulation. Layout, loaded. Zoomed.

TABLE XVII: Layout. Loaded. Results.

Mean Voltage (V)	Max Volt	Mini Volt	Ripple
914 mV	917 mV	902 mV	15 mV

The difference between the output mean voltage of the schematic and the layout under loaded conditions is approximately:

$$\Delta V_{out} = 1.026 - 0.914 = 112\ mV$$

Or a 10 % relative error.

The ripple is, curiously, slightly smaller than that of the schematic, probably because a lower output voltage generates a lower output current given a resistive load.

If we use the Thèvenin model to reverse-engineer the resistance of the circuits:

$$V_{out} = V_{Th} * \frac{R_{load}}{R_{equivalent} + R_{load}}$$

Where the Thèvenin voltage is the mean voltage in open circuit configuration, we obtain:

$$R_{eqSchematic} = 139{,}12\ k\Omega$$

This result coincides fairly well with the theoretical value of the equivalent resistance calculated through the CMV method equation:

$$R_{eq} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \approx 135\ k\Omega$$

Where the values of the capacitances and the switch resistances have been obtained from the figures depicting the voltage dependence of egncaps with 2 um^2 area and the figures depicting the resistance-width relation of lvtn- and -pfets.

However, the results of the layout deviate slightly from these values, potentially due to increasing resistive (and capacitive) parasitic elements.

$$R_{eqLayout} \approx 184{,}90\ k\Omega$$

8. Conclusions

Switched-capacitor converters are the preferable alternative to Inductive Power Converters in IC design. FDSOI implementations are particularly apt for ultra-low power applications. However, the non-linear nature of switched-capacitor converters and the complex underlying physical characteristics of charging/discharging capacitors presents a variety of modelling challenges. This thesis focuses on the analysis of CC-CP, both from an ideal-circuit point of view and real implementations based on FDSOI technology.

A discrete-time state-space model is derived. The model is able to encapsulate the non-linear dynamics of a CC-CP in a linear, time-invariant set of matrices with great accuracy as compared to the transient behavior of idealized versions of the circuit and the effect of parasitic elements. These results can be achieved at a very low computational cost, reducing the simulation time from several minutes to seconds in cases with large capacitive values.

The dynamic model, as is, lacks some external validity, in the sense that real implementations of the circuit would present, as evidenced by section 6, varying values of resistive and capacitive components. These variations are not reflected in the original model derived, which only considers constant parameters of the exponential terms.

These limitations can be solved by a more refined algorithm where the values of the resistive and capacitive components are recomputed after each iteration.

A steady-state model is also derived, providing equations to determine approximations of the mean voltage operation points for each fly-capacitor. These equations can be useful during the design phase of the circuit, as they can inform of the biasing conditions of the different components during operation. Note, however, that optimization constraints (be them for efficiency or area) are not part of this study and might supersede these considerations.

The steady-state model is fully characterized by a Thèvenin equivalent circuit. The Thèvenin voltage is studied under the presence of parasitic capacitances and their effect on the maximum attainable voltage of the converter, deriving equations that provide high similarity to simulated results.

A Thèvenin resistance equation is derived as the linear combination of switched-capacitors' equivalent resistance. To validate the equation, it is compared to the results provided by pre-existing models (equation ()) and simulations, finding that depending on the mode of operation of the circuit (SSL or FSL), the resulting accuracy varies.

The Thèvenin equivalent circuit is characterized for a CC-CP with an arbitrary number of stages.

Regarding purely theoretical analysis, the CC-CP model is finalized with two ripple equations, one for each mode of operation (SSL and FSL). Both equations serve as good approximations to the ripple observed in transient simulations of the circuit.

As for FDSOI implementations of the circuit, empirical analyses are first conducted on MOS capacitors to elucidate their behavior as fly-capacitors. We conclude that voltage dependent capacitors vary in capacitance as they switch from charging to discharging

states. From these qualitative remarks, a theoretical analysis ensues, reaching an equation and a numerical algorithm that allows us to predict the effect of voltage dependent capacitors on the output voltage as well as the value of the capacitance of each fly-capacitor during operation. Difficulty in the design of a test-bench or simulation that can capture this effect limits these conclusions, at the moment, to a purely theoretical framework.

The study of FDSOI components continues with the empirical characterization of LVTFET's behavior as resistive switches, where the influence of transistor width, back bias and, specially, stage of the CC-CP in which the transistor is present are remarked in their effect on the resistance. An example circuit is built with LVTFET technology, using ideal capacitors, to further proof that the ideal models hold when implemented with more complex components.

Finally, a layout for a 3-stage CC-CP in FDSOI technology, with LVTFETs as resistive switches and bulk MOS capacitors as fly-capacitors is designed and its extraction tested against its schematic. The chosen design functionality is confirmed, albeit with slight performance differences to its schematic counterpart, due to the increased presence of parasitic elements.

Annexes

Generalized forms of Dynamic and Steady-State Models (including parasitics)

Generalized form of the mean voltage

In essence, these equations state the very fundamental principle of conservation of charge. In order for a capacitor to remain at the same voltage during a whole period of operation, the following equation must hold:

$$\Delta V * C = Q_{in} - Q_{out} = 0 \tag{31}$$

In a generalized model, with each capacitor having different capacitance values than the rest, the relation between voltage and charge is not the same. That is, the change in voltage of Capacitor Ci is only equal to that of Capacitor Ci+1 for a given amount of charge only if their capacitances are the same.

$$V1 = \frac{aV_2 + V_{in}(1-a)}{(1+a)} \tag{a.1}$$

$$V2 = \frac{b(1+a)V_3 + V_{in}\big(2 - b(1+a)\big)}{\big(1 + b(1+a)\big)} \tag{a.2}$$

$$V_3 = \frac{\Big(c\big(1+b(1+a)\big)\Big)V_4 + V_{in}\Big(3 - c\big(1+b(1+a)\big)\Big)}{\Big(1 + c\big(1+b(1+a)\big)\Big)} \tag{a.3}$$

$$a = \frac{c2}{c1 + c2} \tag{a.4}$$

$$b = \frac{c3(c2 + c1)}{c1(c3 + c2)} \tag{a.5}$$

$$c = \frac{c4(c2 + c3)}{c2(c3 + c4)} \tag{a.6}$$

Dynamic model expansion. Consideration of Inequal Capacitors, Inequal Time constants, introduction of parasitic effects.

The dynamics of the CC-CP had been found to be governed by the transfer of charge between different capacitors of the circuit. This phenomenon is conveyed by the solutions to two differential equations, each pertaining to one of the two potential topologies in which the circuit can be divided.

Each of these solutions expresses the rate by which charge either enters or leaves a capacitor pertaining to that particular topology. These equations are:

$$\Delta Q_1 = C_1(V_{in} - V_1)\left(1 - e^{-\frac{T}{2R1C}}\right) \qquad (a.7)$$

$$\Delta Q_i = C_{eq}(V_{clki} + V_i - V_{i+1})\left(1 - e^{-\frac{T}{2RiC_{eq}}}\right) \qquad (a.8)$$

Where C1 represents the capacitance of the first capacitor, while Ceq is the series combination of capacitances C_i and C_{i+1}.

$$C_{eq} = \left(\frac{1}{C_i} + \frac{1}{C_{i+1}}\right)^{-1} \qquad (a.9)$$

Since the Dynamic model originally derived contemplated, for the sake of simplicity, equal capacitances for each stage of the Charge Pump, the equivalent capacitance of the ith stage became, simply, one-half of the capacitance C1. Therefore:

$$C_{eq} = \frac{C_1}{2} \qquad (a.10)$$

And equation (a.8) became:

$$\Delta Q_i = \frac{C_1}{2}(V_{clki} + V_i - V_{i+1})\left(1 - e^{-\frac{T}{RiC}}\right) \qquad (a.11)$$

It was thus posible to stablish the following relation regarding the ith and the first resistance. If all the ith resistances were equal and resistance 1 was made to be half of them, the exponential terms became constants for all the topologies:

$$R_i = R \;\forall i \neq 1$$

$$R_1 = \frac{R}{2}$$

In this particular case, the term $\left(1 - e^{-\frac{T}{RiC}}\right)$ could be expressed by a single variable:

$$a = \left(1 - \mathrm{e}^{-\frac{\mathrm{T}}{RiC}}\right)$$

This way, all the model would be fully parametrized by this single variable.

However, when all capacitances are not equal, the model has to be modified to account for this fact.

Consider the case of inequal capacitances.

Equation (a.7) remains the same. Equation (a.8) must be modified.

Consider the charge that capacitor 1 loses as it discharges onto capacitor 2, which will be referred to as ΔQ_{12}:

$$\Delta Q_{12} = -\frac{C_1 C_2}{C1 + C2}(\mathrm{V_{in}} + \mathrm{V_1} - \mathrm{V_2})\left(1 - \mathrm{e}^{-\frac{\mathrm{T}}{RiC12}}\right) \qquad (a.11)$$

This equation is equal to the one expressing the charge that capacitor 2 gains as it is being charged by capacitor 1, with a -1 factor.

$$\Delta Q_{21} = -\Delta Q_{12} = \frac{C_1 C_2}{C1 + C2}(\mathrm{V_{in}} + \mathrm{V_1} - \mathrm{V_2})\left(1 - \mathrm{e}^{-\frac{\mathrm{T}}{RiC12}}\right) \qquad (a.12)$$

Noting that:

$$\Delta Vc_1 = \frac{\Delta Q_{12}}{C1} = -\frac{C_2}{C1 + C2}(\mathrm{V_{in}} + \mathrm{V_1} - \mathrm{V_2})\left(1 - \mathrm{e}^{-\frac{\mathrm{T}}{RiC12}}\right) \qquad (a.13)$$

$$\Delta Vc_2 = \frac{\Delta Q_{21}}{C2} = \frac{C_1}{C1 + C2}(\mathrm{V_{in}} + \mathrm{V_1} - \mathrm{V_2})\left(1 - \mathrm{e}^{-\frac{\mathrm{T}}{RiC12}}\right) \qquad (a.14)$$

It can be seen that, now, $\Delta Vc_1 \neq \Delta Vc_2$. These two equations are only equal (in absolute value) when $C_1 = C_2$, otherwise the parameters $\frac{C_2}{C1+C2}$ and $\frac{C_1}{C1+C2}$ have to be included in the model.

Scripts

Dynamic Model

```
c1=6e-15
c2=c1
c3=c1
c4=c1
c5=c1
c6=c2
c7=c3

c12=c2/(c1+c2)
c21=c1/(c1+c2)
c23=c3/(c2+c3)
c32=c2/(c2+c3)
c34=c4/(c3+c4)
c43=c3/(c3+c4)

c56=c12
c65=c21
c67=c23
c76=c32
c74=c34
c47=c43

R=25e3

f=500e6
T=1/(f)

bout=0


%ceq=c1*c2/(c1+c2)
ceq=(3.3e-15)

a=(1-exp(-1/(f*2*R*ceq)))

%%-------------   Parasitic effects
cx=6.6e-15
R1=25e3
a1=(1-exp(-1/(f*2*R1*cx)))
%a1=a
x=1-0.14
%x=1
%%-----------------



A=[((1-a1)*(1-c12*a)) (c12*a*(1-c23*a))  (a*a*c12*c23) 0 0 0 0;
```

```
    (a*c21*(1-a1)) (1-a*c23)*(1-a*c21) a*c23*(1-a*c21) 0 0 0 0;
    0 a*c32*(1-a*c34) (1-a*c32)*(1-a*c34) a*c34*(1-a*c47-bout) 0 0
a*a*c34*c47;
    0 a*a*c43*c32 a*c43*(1-a*c32) (1-a*c47-bout)*(1-a*c43-bout) 0
0 a*c47*(1-a*c43-bout);
    0 0 0 0 (1-a1)*(1-a*c56) a*c56*(1-a1) 0;
    0 0 0 a*a*c67*c74 a*c65*(1-a*c67) (1-a*c65)*(1-a*c67)
a*c67*(1-a*c74);
    0 0 0 a*c74*(1-a*c76) a*a*c76*c65 a*c76*(1-a*c65) (1-
a*c74)*(1-a*c76)]

B=[a*(1-a*c12)*x-a*a*c12*c23*x-a*c12 0;
   -a*c23*(1-a*c21)*x+a*a*c21+a*c21*x 0;
   x*(a*c32*(1-a*c34)+a*a*c34*c47-a*c34);
   (a*c47*(1-a*c43-bout)+a*a*c43*c32+a*c43)*x;
   -a*c56*(1-a)*x+a 0;
   x*(a*c65*(1-a*c67)-a*a*c74*c67-a*c67) 0;
   x*(-a*c74*(1-a*c76)+a*a*c76*c65+a*c76) 0]


C=[0 0 0 1 0 0 0]
D=[0]

sys = ss(A,B,C,D,T)


lsim(sys)
```

Voltage dependent capacitors

```
E=0.3
C_vs_V_prev=load('C_vs_V_prev.sfit','-mat')

%v.savedSession.AllFitdevsAndConfigs{1, 1}.Fitdev.Fit
p=coeffvalues(C_vs_V_prev.savedSession.AllFitdevsAndConfigs{1,
1}.Fitdev.Fit)


c_prev= @(x) p(1)*x^5 + p(2)*x^4 + p(3)*x^3 +p(4)*x^2+p(5)*x+p(6)


C_vs_V_next=load('C_vs_V_next.sfit','-mat')

p=coeffvalues(C_vs_V_next.savedSession.AllFitdevsAndConfigs{1,
1}.Fitdev.Fit)

c_next=@(x) p(1)*x^5 + p(2)*x^4 + p(3)*x^3 +p(4)*x^2+p(5)*x+p(6)

c_charging=zeros(1,4)
c_discharging=zeros(1,4)
vc=zeros(1,4)
vc_e=zeros(1,4)
vc(1)=E
c_charging(1)=c_prev(E)
j=0
while j<=10

for i=2:4
    v_next= @(x) -E-(vc(i-1)*(1-0.13)*c_charging(i-1))/c_next(x)
+x
    vc(i)=fsolve(v_next,0)
    c_discharging(i-1)=c_next(vc(i))
    Q=c_charging(i-1)*vc(i-1)
    vc_e(i-1)=(Q/(c_discharging(i-1))+E)
    c_charging(i)=c_prev(vc_e(i-1))
end

cap1=[1 1 1 1]*transpose(c_charging.^-1)
cap2=[1 1 1]*transpose(c_discharging(:,1:3).^-1)

total_cap=(cap1+cap2)^-1

f=500e6

I=1e-9

Req=(7/4)*(1/(f*total_cap))

vc(4)=vc(4)-(7/4)*I/(f*total_cap)
```

```
%% assume initially coth(x) = 1, the disparity between capacitors
is not significant
%calculate the new V4 considering losses at the output,
%introduce the new VC vector, complete the loop, form the error
formula

vc(3)=vc(4)-E

vc(2)=(3*vc(3)+E)/5

vc(1)=(E+vc(2))/3

j=j+1
end
```

```
// Generated for: spectre
// Generated on: Aug 19 17:34:52 2019
// Design library name: CHARGEPUMP_EXTR
// Design cell name: CP_4N
// Design view name: config
simulator lang=spectre
global 0
parameters delay Vclk_DC period tr pwidth Vin V_bp V_bn Cload
Rload
include "/home/kenneth/fdsoi2/corners.scs"

// Library name: CHARGEPUMP
// Cell name: CC_N_inverters
// View name: av_extracted
// Inherited view list: SimMosfetStandard SimCapacitorStandard
//SimVaractorStandard SimBipolarStandard SimMosfetrfStandard
//SimMosfetrfSeg SimMosfetAccurate SimResistorAccurate
SimEsddiodeNova
//SimEsdmosfetStandard SimEsdmosfetNova SimCapaStd SimCapaAcc
spectre
//auCmos_sch cmos_sch cmos.sch ads_schematic schematic auGate_sch
//auGate.sch extracted ahdl veriloga
subckt CC_N_inverters_av_extracted bbn bbp cap_ground clk1 clk2
vin vout
I2\|I0\|P0 (\33\:net5 \36\:net6 \1\:vout bbp) lvtpfet_acc w=5e-07
l=3e-08 \
        nf=1 sa=76.0n sb=76.0n sd=114n ptwell=0 par=1 sca=-1 scb=-
1 scc=-1 \
        pre_layout_local=0 p_la=0 lpccnr=0 covpccnr=0 ngcon=1
wrxcnr=0 \
        nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1 \
        mismatch=1 m=1 xpos=-1 ypos=-1 plorient=1 plsnf=0
pcpastrx_top=-1 \
        pcpastrx_bot=-1 mx=1 my=1 deltax=0 deltay=0
I2\|I1\|P0 (\10\:net6 net5 \6\:vout bbp) lvtpfet_acc w=5e-07 l=3e-
08 nf=1 \
        sa=76.0n sb=76.0n sd=114n ptwell=0 par=1 sca=-1 scb=-1
scc=-1 \
        pre_layout_local=0 p_la=0 lpccnr=0 covpccnr=0 ngcon=1
wrxcnr=0 \
        nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1 \
        mismatch=1 m=1 xpos=-1 ypos=-1 plorient=1 plsnf=0
pcpastrx_top=-1 \
        pcpastrx_bot=-1 mx=1 my=1 deltax=0 deltay=0
I1\|I0\|P0 (\33\:net11 \36\:net12 \7\:net9 bbp) lvtpfet_acc w=5e-
07 \
        l=3e-08 nf=1 sa=76.0n sb=76.0n sd=114n ptwell=0 par=1
sca=-1 \
        scb=-1 scc=-1 pre_layout_local=0 p_la=0 lpccnr=0
covpccnr=0 \
```

```
        ngcon=1 wrxcnr=0 nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1
swshe=0 \
        swrg=1 mismatch=1 m=1 xpos=-1 ypos=-1 plorient=1 plsnf=0 \
        pcpastrx_top=-1 pcpastrx_bot=-1 mx=1 my=1 deltax=0
deltay=0
I1\|I1\|P0 (\10\:net12 net11 \12\:net9 bbp) lvtpfet_acc w=5e-07
l=3e-08 \
        nf=1 sa=76.0n sb=76.0n sd=114n ptwell=0 par=1 sca=-1 scb=-
1 scc=-1 \
        pre_layout_local=0 p_la=0 lpccnr=0 covpccnr=0 ngcon=1
wrxcnr=0 \
        nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1 \
        mismatch=1 m=1 xpos=-1 ypos=-1 plorient=1 plsnf=0
pcpastrx_top=-1 \
        pcpastrx_bot=-1 mx=1 my=1 deltax=0 deltay=0
I0\|I0\|P0 (\33\:net17 \36\:net18 \7\:net15 bbp) lvtpfet_acc w=5e-
07 \
        l=3e-08 nf=1 sa=76.0n sb=76.0n sd=114n ptwell=0 par=1
sca=-1 \
        scb=-1 scc=-1 pre_layout_local=0 p_la=0 lpccnr=0
covpccnr=0 \
        ngcon=1 wrxcnr=0 nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1
swshe=0 \
        swrg=1 mismatch=1 m=1 xpos=-1 ypos=-1 plorient=1 plsnf=0 \
        pcpastrx_top=-1 pcpastrx_bot=-1 mx=1 my=1 deltax=0
deltay=0
I0\|I1\|P0 (\10\:net18 net17 \12\:net15 bbp) lvtpfet_acc w=5e-07
l=3e-08 \
        nf=1 sa=76.0n sb=76.0n sd=114n ptwell=0 par=1 sca=-1 scb=-
1 scc=-1 \
        pre_layout_local=0 p_la=0 lpccnr=0 covpccnr=0 ngcon=1
wrxcnr=0 \
        nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1 \
        mismatch=1 m=1 xpos=-1 ypos=-1 plorient=1 plsnf=0
pcpastrx_top=-1 \
        pcpastrx_bot=-1 mx=1 my=1 deltax=0 deltay=0
I2\|I0\|N0 (\34\:net5 \37\:net6 net9 bbn) lvtnfet_acc w=5e-07
l=3e-08 nf=1 \
        sa=76.0n sb=76.0n sd=114n ptwell=0 par=1 sca=-1 scb=-1
scc=-1 \
        pre_layout_local=0 p_la=0 lpccnr=0 covpccnr=0 ngcon=1
wrxcnr=0 \
        nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1 \
        mismatch=1 m=1 xpos=-1 ypos=-1 plorient=1 plsnf=0
pcpastrx_top=-1 \
        pcpastrx_bot=-1 mx=1 my=1 deltax=0 deltay=0
I2\|I1\|N0 (\5\:net6 \3\:net5 \6\:net9 bbn) lvtnfet_acc w=5e-07
l=3e-08 \
        nf=1 sa=76.0n sb=76.0n sd=114n ptwell=0 par=1 sca=-1 scb=-
1 scc=-1 \
        pre_layout_local=0 p_la=0 lpccnr=0 covpccnr=0 ngcon=1
wrxcnr=0 \
        nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1 \
```

```
        mismatch=1 m=1 xpos=-1 ypos=-1 plorient=1 plsnf=0
pcpastrx_top=-1 \
        pcpastrx_bot=-1 mx=1 my=1 deltax=0 deltay=0
I1\|I0\|N0 (\34\:net11 \37\:net12 net15 bbn) lvtnfet_acc w=5e-07
l=3e-08 \
        nf=1 sa=76.0n sb=76.0n sd=114n ptwell=0 par=1 sca=-1 scb=-
1 scc=-1 \
        pre_layout_local=0 p_la=0 lpccnr=0 covpccnr=0 ngcon=1
wrxcnr=0 \
        nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1 \
        mismatch=1 m=1 xpos=-1 ypos=-1 plorient=1 plsnf=0
pcpastrx_top=-1 \
        pcpastrx_bot=-1 mx=1 my=1 deltax=0 deltay=0
I1\|I1\|N0 (\5\:net12 \3\:net11 \6\:net15 bbn) lvtnfet_acc w=5e-07
l=3e-08 \
        nf=1 sa=76.0n sb=76.0n sd=114n ptwell=0 par=1 sca=-1 scb=-
1 scc=-1 \
        pre_layout_local=0 p_la=0 lpccnr=0 covpccnr=0 ngcon=1
wrxcnr=0 \
        nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1 \
        mismatch=1 m=1 xpos=-1 ypos=-1 plorient=1 plsnf=0
pcpastrx_top=-1 \
        pcpastrx_bot=-1 mx=1 my=1 deltax=0 deltay=0
I0\|I0\|N0 (\34\:net17 \37\:net18 \1\:vin bbn) lvtnfet_acc w=5e-07
l=3e-08 \
        nf=1 sa=76.0n sb=76.0n sd=114n ptwell=0 par=1 sca=-1 scb=-
1 scc=-1 \
        pre_layout_local=0 p_la=0 lpccnr=0 covpccnr=0 ngcon=1
wrxcnr=0 \
        nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1 \
        mismatch=1 m=1 xpos=-1 ypos=-1 plorient=1 plsnf=0
pcpastrx_top=-1 \
        pcpastrx_bot=-1 mx=1 my=1 deltax=0 deltay=0
I0\|I1\|N0 (\5\:net18 \3\:net17 \6\:vin bbn) lvtnfet_acc w=5e-07
l=3e-08 \
        nf=1 sa=76.0n sb=76.0n sd=114n ptwell=0 par=1 sca=-1 scb=-
1 scc=-1 \
        pre_layout_local=0 p_la=0 lpccnr=0 covpccnr=0 ngcon=1
wrxcnr=0 \
        nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1 \
        mismatch=1 m=1 xpos=-1 ypos=-1 plorient=1 plsnf=0
pcpastrx_top=-1 \
        pcpastrx_bot=-1 mx=1 my=1 deltax=0 deltay=0
    C7 (cap_ground \1\:bbn) capacitor c=2.67569e-17
    C8 (bbn bbp) capacitor c=8.59546e-16
    C9 (cap_ground bbp) capacitor c=1.90157e-17
    C10 (\1\:bbn bbp) capacitor c=9.04988e-17
    C11 (bbp \32\:net17) capacitor c=5.42586e-17
    C12 (cap_ground \32\:net17) capacitor c=6.46762e-16
    C13 (\1\:bbn \32\:net17) capacitor c=8.05578e-16
    C14 (bbp net17) capacitor c=7.60091e-17
    C15 (cap_ground \32\:net5) capacitor c=6.73292e-16
    C16 (\1\:bbn \32\:net5) capacitor c=8.64712e-16
```

```
C17 (bbp \32\:net5) capacitor c=2.4248e-16
C18 (\950\:bbn net5) capacitor c=1.31016e-18
C19 (\32\:net17 \32\:net11) capacitor c=2.95202e-17
C20 (bbp \32\:net11) capacitor c=2.24833e-16
C21 (\32\:net5 \32\:net11) capacitor c=3.05998e-17
C22 (cap_ground \32\:net11) capacitor c=6.49082e-16
C23 (\1\:bbn \32\:net11) capacitor c=8.45614e-16
C24 (bbp net11) capacitor c=7.22088e-18
C25 (\35\:net5 \35\:net11) capacitor c=2.56293e-18
C26 (\35\:net17 \35\:net11) capacitor c=2.55919e-18
C27 (net5 \27\:net6) capacitor c=2.60057e-16
C28 (bbp \27\:net6) capacitor c=2.52856e-16
C29 (cap_ground \27\:net6) capacitor c=6.9367e-16
C30 (\1\:bbn \27\:net6) capacitor c=8.55613e-16
C31 (\32\:net5 \37\:net6) capacitor c=1.89991e-16
C32 (\3\:net5 \5\:net6) capacitor c=4.32621e-17
C33 (\33\:net5 \36\:net6) capacitor c=4.38836e-17
C34 (\33\:net6 \33\:net12) capacitor c=2.41026e-18
C35 (\27\:net6 \27\:net12) capacitor c=3.00129e-17
C36 (bbp \27\:net12) capacitor c=2.33257e-16
C37 (net11 \27\:net12) capacitor c=2.5865e-16
C38 (cap_ground \27\:net12) capacitor c=6.69401e-16
C39 (\1\:bbn \27\:net12) capacitor c=8.39075e-16
C40 (\32\:net11 \37\:net12) capacitor c=1.89985e-16
C41 (\3\:net11 \5\:net12) capacitor c=4.38194e-17
C42 (\33\:net11 \36\:net12) capacitor c=4.42129e-17
C43 (\33\:net12 \33\:net18) capacitor c=2.41026e-18
C44 (net17 \27\:net18) capacitor c=2.63514e-16
C45 (bbp \27\:net18) capacitor c=8.06981e-17
C46 (\27\:net12 \27\:net18) capacitor c=2.96248e-17
C47 (cap_ground \27\:net18) capacitor c=6.49881e-16
C48 (\1\:bbn \27\:net18) capacitor c=7.82397e-16
C49 (\32\:net17 \37\:net18) capacitor c=1.91185e-16
C50 (\3\:net17 \5\:net18) capacitor c=4.40474e-17
C51 (bbp \36\:net18) capacitor c=4.52604e-17
C52 (\33\:net17 \36\:net18) capacitor c=4.39003e-17
C53 (\35\:net5 \1\:clk2) capacitor c=1.1431e-15
C54 (cap_ground \70\:clk2) capacitor c=8.87739e-17
C55 (\35\:net11 \23\:clk2) capacitor c=1.14367e-15
C56 (cap_ground \72\:clk2) capacitor c=9.54132e-16
C57 (\35\:net17 \45\:clk2) capacitor c=1.14477e-15
C58 (\33\:net6 \7\:clk1) capacitor c=1.14136e-15
C59 (\33\:net12 \29\:clk1) capacitor c=1.14181e-15
C60 (cap_ground \4\:clk1) capacitor c=1.04538e-15
C61 (\33\:net18 \51\:clk1) capacitor c=1.14332e-15
C62 (\32\:net17 vin) capacitor c=9.43264e-17
C63 (bbp vin) capacitor c=7.04837e-19
C64 (\27\:net18 vin) capacitor c=8.81872e-17
C65 (cap_ground vin) capacitor c=1.65709e-16
C66 (\1\:bbn vin) capacitor c=4.5574e-16
C67 (bbp vout) capacitor c=6.97454e-17
C68 (\32\:net5 vout) capacitor c=7.93798e-17
C69 (\27\:net6 vout) capacitor c=8.42335e-17
```

```
    C70 (cap_ground vout) capacitor c=1.67468e-16
    C71 (\1\:bbn vout) capacitor c=4.66196e-16
    C72 (\37\:net12 \6\:net15) capacitor c=3.76139e-17
    C73 (bbn \6\:net15) capacitor c=3.44818e-17
    C74 (\3\:net11 \6\:net15) capacitor c=3.69176e-17
    C75 (cap_ground \6\:net15) capacitor c=4.24668e-18
    C76 (bbp \12\:net9) capacitor c=8.01792e-17
    C77 (\32\:net11 \12\:net9) capacitor c=1.15488e-16
    C78 (\27\:net12 \12\:net9) capacitor c=1.20037e-16
    C79 (cap_ground \12\:net9) capacitor c=4.4481e-18
    C80 (bbp net15) capacitor c=1.07858e-17
    C81 (\32\:net11 net15) capacitor c=8.78914e-17
    C82 (\27\:net12 net15) capacitor c=8.07508e-17
    C83 (\1\:bbn net15) capacitor c=2.46464e-17
    C84 (\3\:net5 \6\:net9) capacitor c=3.69101e-17
    C85 (\37\:net6 \6\:net9) capacitor c=3.76126e-17
    C86 (bbn \6\:net9) capacitor c=3.78325e-17
    C87 (\32\:net5 net9) capacitor c=8.86695e-17
    C88 (\27\:net6 net9) capacitor c=8.15831e-17
    C89 (\1\:bbn net9) capacitor c=2.54763e-17
    C90 (\3\:net17 \6\:vin) capacitor c=3.66319e-17
    C91 (\37\:net18 \6\:vin) capacitor c=3.73544e-17
    C92 (net5 \6\:vout) capacitor c=3.72423e-17
    C93 (\36\:net6 \6\:vout) capacitor c=3.68237e-17
    C94 (\32\:net17 \12\:net15) capacitor c=1.15555e-16
    C95 (\27\:net18 \12\:net15) capacitor c=1.20103e-16
    C96 (bbp \12\:net15) capacitor c=6.35705e-17
    I6\|C0 (\35\:net5 \1\:clk2 cap_ground) egncap l=2e-06 w=2e-06
nf=1 \
        nrep=1 rsx=50 setres=0 setind=-2 soa=1 m=1
    I7\|C0 (\35\:net11 \23\:clk2 cap_ground) egncap l=2e-06 w=2e-
06 nf=1 \
        nrep=1 rsx=50 setres=0 setind=-2 soa=1 m=1
    I8\|C0 (\35\:net17 \45\:clk2 cap_ground) egncap l=2e-06 w=2e-
06 nf=1 \
        nrep=1 rsx=50 setres=0 setind=-2 soa=1 m=1
    I3\|C0 (\33\:net6 \7\:clk1 cap_ground) egncap l=2e-06 w=2e-06
nf=1 \
        nrep=1 rsx=50 setres=0 setind=-2 soa=1 m=1
    I4\|C0 (\33\:net12 \29\:clk1 cap_ground) egncap l=2e-06 w=2e-
06 nf=1 \
        nrep=1 rsx=50 setres=0 setind=-2 soa=1 m=1
    I5\|C0 (\33\:net18 \51\:clk1 cap_ground) egncap l=2e-06 w=2e-
06 nf=1 \
        nrep=1 rsx=50 setres=0 setind=-2 soa=1 m=1
    Rm_3_48 (\34\:net17 net17) resistor r=24734.5 tc1=0 tc2=0 c=0
    Rm_3_47 (net6 \33\:net6) resistor r=0.7584 tc1=0 tc2=0 c=0
    Rm_3_46 (\7\:net15 \6\:net15) resistor r=231.757 tc1=0 tc2=0
c=0
    Rm_3_45 (\1\:vin \6\:vin) resistor r=8.5802 tc1=0 tc2=0 c=0
    Rm_3_40 (\32\:net17 \34\:net17) resistor r=30.584 tc1=0 tc2=0
c=0
```

```
    Rm_3_39 (\33\:net6 \27\:net6) resistor r=6.6078 tc1=0 tc2=0
c=0
    Rm_3_38 (\33\:net18 \27\:net18) resistor r=6.8587 tc1=0 tc2=0
c=0
    Rm_3_37 (\7\:clk1 \2\:clk1) resistor r=0.5295 tc1=0 tc2=0 c=0
    Rm_2_48 (\34\:net17 \3\:net17) resistor r=6010.4 tc1=0 tc2=0
c=0
    Rm_2_47 (\10\:net12 \37\:net12) resistor r=27485.1 tc1=0 tc2=0
c=0
    Rm_2_46 (\12\:net15 \6\:net15) resistor r=231.757 tc1=0 tc2=0
c=0
    Rm_2_45 (\6\:vin vin) resistor r=59.902 tc1=0 tc2=0 c=0
    Rm_2_40 (\32\:net17 \3\:net17) resistor r=234.371 tc1=0 tc2=0
c=0
    Rm_2_39 (\27\:net6 \37\:net6) resistor r=962.341 tc1=0 tc2=0
c=0
    Rm_2_38 (\27\:net18 \37\:net18) resistor r=962.341 tc1=0 tc2=0
c=0
    Rm_2_37 (\29\:clk1 \4\:clk1) resistor r=0.5295 tc1=0 tc2=0 c=0
    Rl14 (net17 \3\:net17) resistor r=476.044 tc1=0 tc2=0 c=0
    Rl13 (\37\:net12 \36\:net12) resistor r=472.566 tc1=0 tc2=0
c=0
    Rl5 (net15 \6\:net15) resistor r=8.2933 tc1=0 tc2=0 c=0
    Rl15 (\1\:vin vin) resistor r=59.902 tc1=0 tc2=0 c=0
    Rl6 (\34\:net5 \32\:net5) resistor r=30.584 tc1=0 tc2=0 c=0
    Rl8 (\27\:net6 \10\:net6) resistor r=30.5967 tc1=0 tc2=0 c=0
    Rl7 (\27\:net18 \10\:net18) resistor r=30.5967 tc1=0 tc2=0 c=0
    Rl1 (\4\:clk1 \6\:clk1) resistor r=0.9976 tc1=0 tc2=0 c=0
    Rk_1_215 (\34\:net5 net5) resistor r=24734.5 tc1=0 tc2=0 c=0
    Rk_1_218 (\10\:net12 \36\:net12) resistor r=7905.41 tc1=0
tc2=0 c=0
    Rk_1_203 (\7\:net9 \12\:net9) resistor r=8.2912 tc1=0 tc2=0
c=0
    Rk_1_206 (\950\:bbn \507\:bbn) resistor r=10.5599 tc1=0 tc2=0
c=0
    Rk_1_209 (\32\:net5 \33\:net5) resistor r=30.0324 tc1=0 tc2=0
c=0
    Rk_1_212 (\27\:net6 \5\:net6) resistor r=29.9812 tc1=0 tc2=0
c=0
    Rk_1_64 (\27\:net18 \5\:net18) resistor r=29.9812 tc1=0 tc2=0
c=0
    Rk_1_67 (\6\:clk1 \51\:clk1) resistor r=0.5295 tc1=0 tc2=0 c=0
    Rk191 (\34\:net5 \3\:net5) resistor r=6010.4 tc1=0 tc2=0 c=0
    Rk16 (net12 \33\:net12) resistor r=0.7583 tc1=0 tc2=0 c=0
    Rk17 (\7\:net9 net9) resistor r=233.377 tc1=0 tc2=0 c=0
    Rk18 (\507\:bbn bbn) resistor r=280.861 tc1=0 tc2=0 c=0
    Rk19 (\32\:net5 net5) resistor r=964.506 tc1=0 tc2=0 c=0
    Rk20 (\27\:net6 \36\:net6) resistor r=276.794 tc1=0 tc2=0 c=0
    Rk21 (\27\:net18 \36\:net18) resistor r=276.794 tc1=0 tc2=0
c=0
    Rk22 (\2\:clk1 clk1) resistor r=0.6966 tc1=0 tc2=0 c=0
    Rj29 (net5 \3\:net5) resistor r=476.044 tc1=0 tc2=0 c=0
```

```
    Rj30 (\10\:net18 \37\:net18) resistor r=27485.1 tc1=0 tc2=0
c=0
    Rj31 (\12\:net9 net9) resistor r=233.377 tc1=0 tc2=0 c=0
    Rj4 (\950\:bbn bbn) resistor r=1212.01 tc1=0 tc2=0 c=0
    Rj5 (\32\:net5 \35\:net5) resistor r=4.2343 tc1=0 tc2=0 c=0
    Rj6 (\27\:net6 net6) resistor r=4.7215 tc1=0 tc2=0 c=0
    Rj41 (\27\:net18 net18) resistor r=4.9009 tc1=0 tc2=0 c=0
    Rj38 (\4\:clk1 clk1) resistor r=0.3011 tc1=0 tc2=0 c=0
    Ri10 (\34\:net11 net11) resistor r=24734.5 tc1=0 tc2=0 c=0
    Ri3 (\37\:net18 \36\:net18) resistor r=472.566 tc1=0 tc2=0 c=0
    Ri20 (\7\:net9 \6\:net9) resistor r=233.377 tc1=0 tc2=0 c=0
    Ri1 (bbn \1\:bbn) resistor r=0.5847 tc1=0 tc2=0 c=0
    Ri2 (\32\:net5 \3\:net5) resistor r=234.371 tc1=0 tc2=0 c=0
    Ri21 (\33\:net12 \27\:net12) resistor r=6.6215 tc1=0 tc2=0 c=0
    Ri4 (\1\:clk2 \70\:clk2) resistor r=0.5296 tc1=0 tc2=0 c=0
    Rv_11 (\34\:net11 \3\:net11) resistor r=6010.4 tc1=0 tc2=0 c=0
    Rv_12 (\10\:net18 \36\:net18) resistor r=7905.41 tc1=0 tc2=0
c=0
    Rv_13 (\12\:net9 \6\:net9) resistor r=233.377 tc1=0 tc2=0 c=0
    Rv_14 (\507\:bbn \1\:bbn) resistor r=1.2968 tc1=0 tc2=0 c=0
    Rv_15 (\34\:net11 \32\:net11) resistor r=30.584 tc1=0 tc2=0
c=0
    Rv_16 (\27\:net12 \37\:net12) resistor r=962.341 tc1=0 tc2=0
c=0
    Rv_17 (\23\:clk2 \72\:clk2) resistor r=0.5296 tc1=0 tc2=0 c=0
    Rv_21 (net11 \3\:net11) resistor r=476.044 tc1=0 tc2=0 c=0
    Rv_22 (net18 \33\:net18) resistor r=0.7565 tc1=0 tc2=0 c=0
    Rv_23 (net9 \6\:net9) resistor r=8.2912 tc1=0 tc2=0 c=0
    Rv_24 (\950\:bbn \1\:bbn) resistor r=1.0562 tc1=0 tc2=0 c=0
    Rv_25 (\32\:net11 net11) resistor r=964.506 tc1=0 tc2=0 c=0
    Rv_26 (\27\:net12 \10\:net12) resistor r=30.5967 tc1=0 tc2=0
c=0
    Rv_27 (\72\:clk2 \74\:clk2) resistor r=0.9966 tc1=0 tc2=0 c=0
    Rv_31 (\10\:net6 \37\:net6) resistor r=27485.1 tc1=0 tc2=0 c=0
    Rv_32 (\7\:net15 \12\:net15) resistor r=8.2933 tc1=0 tc2=0 c=0
    Rv_33 (\1\:vout \6\:vout) resistor r=8.5736 tc1=0 tc2=0 c=0
    Rv_34 (\35\:net17 \32\:net17) resistor r=4.327 tc1=0 tc2=0 c=0
    Rv_35 (\32\:net11 \33\:net11) resistor r=30.0324 tc1=0 tc2=0
c=0
    Rv_36 (\27\:net12 \5\:net12) resistor r=29.9812 tc1=0 tc2=0
c=0
    Rv_37 (\45\:clk2 \74\:clk2) resistor r=0.5296 tc1=0 tc2=0 c=0
    Rv_433 (\37\:net6 \36\:net6) resistor r=472.566 tc1=0 tc2=0
c=0
    Rv_434 (\7\:net15 net15) resistor r=231.757 tc1=0 tc2=0 c=0
    Rv_435 (\6\:vout vout) resistor r=60.5543 tc1=0 tc2=0 c=0
    Rv_436 (\32\:net17 net17) resistor r=964.506 tc1=0 tc2=0 c=0
    Rv_425 (\32\:net11 \35\:net11) resistor r=4.2063 tc1=0 tc2=0
c=0
    Rv_426 (\27\:net12 net12) resistor r=4.7314 tc1=0 tc2=0 c=0
    Rv_427 (\70\:clk2 clk2) resistor r=0.7249 tc1=0 tc2=0 c=0
    Rv_533 (\10\:net6 \36\:net6) resistor r=7905.41 tc1=0 tc2=0
c=0
```

```
    Rv_534 (\12\:net15 net15) resistor r=231.757 tc1=0 tc2=0 c=0
    Rv_535 (\1\:vout vout) resistor r=60.5543 tc1=0 tc2=0 c=0
    Rv_536 (\32\:net17 \33\:net17) resistor r=30.0324 tc1=0 tc2=0
c=0
    Rv_525 (\32\:net11 \3\:net11) resistor r=234.371 tc1=0 tc2=0
c=0
    Rv_526 (\27\:net12 \36\:net12) resistor r=276.794 tc1=0 tc2=0
c=0
    Rv_527 (\72\:clk2 clk2) resistor r=0.2714 tc1=0 tc2=0 c=0
ends CC_N_inverters_av_extracted
// End of subcircuit definition.

// Library name: CHARGEPUMP_EXTR
// Cell name: CP_4N
// View name: schematic
// Inherited view list: SimMosfetStandard SimCapacitorStandard
// SimVaractorStandard SimBipolarStandard SimMosfetrfStandard
// SimMosfetrfSeg SimMosfetAccurate SimResistorAccurate
SimEsddiodeNova
// SimEsdmosfetStandard SimEsdmosfetNova SimCapaStd SimCapaAcc
spectre
// auCmos_sch cmos_sch cmos.sch ads_schematic schematic auGate_sch
// auGate.sch extracted ahdl veriloga
I0 (net3 net2 0 net5 net4 net7 net6) CC_N_inverters_av_extracted
Clk2 (net4 0) vsource type=pulse delay=delay val0=0 val1=Vclk_DC \
        period=period rise=tr fall=tr width=pwidth
Clk1 (net5 0) vsource type=pulse delay=0 val0=0 val1=Vclk_DC
period=period \
        rise=tr fall=tr width=pwidth
V2 (net7 0) vsource dc=Vin type=dc
V1 (net2 0) vsource dc=V_bp type=dc
V0 (net3 0) vsource dc=V_bn type=dc
C0 (net6 0) capacitor c=Cload
R0 (net6 0) resistor r=Rload
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12
temp=27 \
    tnom=25 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5
maxwarns=5 \
    digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \
    dochecklimit=no checklimitdest=both
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub subcktprobelvl=2
```

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