FOSS EKV2.6 Verilog-A Compact MOSFET Model

Wladek Grabinski[1], Marcelo Pavanello[2], Michelly de Souza[2], Daniel Tomaszewski[3], Jola Malesinska[3], Grzegorz Głuszko[3], Matthias Bucher[4], Nikolaos Makris[4], Aristeidis Nikolaou[4], Ahmed Abo-Elhadid[5], Marek Mierzwinski[6], Laurent Lemaitre[7], Mike Brinson[8], Christophe Lallement[9], Jean-Michel Sallese[10], Sadayuki Yoshitomi[11], Paul Malisse[12], Henri Oguey[13], Stefan Cserveny[13], Christian Enz[10], François Krummenacher[10] and Eric Vittoz[10]

[1] *MOS-AK Association (EU)*, [2] *Centro Universitario FEI, Sao Bernardo do Campo (BR)*, [3] *Institute of Electron Technology, Warsaw (PL)*, [4] *Technical University of Crete, Chania (GR)*, [5] *Mentor Graphics (USA)*, [6] *Keysight Technologies (USA)*, [7] *Lemaitre EDA Consulting*, [8] *London Metropolitan University (UK)*, [9] *ICube, Strasbourg University (F)*, [10] *EPFL Lausanne (CH)*, [11] *Toshiba (J)*, [12] *Europractice/IMEC (B)*, [13] *CSEM S.A., Neuchatel (CH)*

***Abstract*—The EKV2.6 MOSFET compact model has had a considerable impact on the academic and industrial community of analog integrated circuit design, since its inception in 1996. The model is available as a free open-source software (FOSS) tool coded in Verilog-A. The present paper provides a short review of foundations of the model and shows its capabilities via characterization and modeling based on a test chip in 180 nm CMOS fabricated via Europractice.**

Keywords—EKV2.6 model, compact/SPICE model, Verilog-A

I. Introduction

Initial work on low power/current compact models for analog integrated circuit (IC) design applications dates back to the early '80s. H. J. Oguey and S. Cserveny published a series of reference papers [1-3]. The proposed models emerged as a viable alternative to available V_{th}-based MOSFET compact models, which demonstrated increasing complexity for scaled MOSFETs that became computationally inefficient. Subsequently, in 1995, Enz, Krummenacher and Vittoz published an analytical compact MOSFET model [4], referred to later as the EKV model. This compact model had the unique feature of referencing the device terminal voltages to the MOSFET substrate, thereby stressing the device's symmetry. Furthermore, a clear framework of normalization of drain current and voltages was introduced, where device quantities were expressed as symmetric functions of forward and reverse normalized currents [4]. The main goal of the EKV model was low-power analog IC design support using a single analytical expression valid in all modes of device operation which in turn provided accurate modeling of the moderate and weak inversion regimes. The same framework was subsequently exploited in the development of a charge-based version of the model. The charge-based model concept, as introduced in the EKV2.6 compact model [5,6], is based on the linearization of the inversion charge Q_i with respect to the surface potential. The drain current I_{DS} expression is related to the continuous g_m/I_{DS} ratio characteristics [7], which is recognized as a fundamental property of the MOS transistors. The model quantities, such as drain current, transconductances, transcapacitances, noise etc. are all expressed in terms of mobile charge density, what gives the name of charge-based model class.

II. EKV2.6 Compact Model

The FOSS EKV2.6 MOSFET model [5] is a scalable compact model for analog-RF design and circuit simulation derived from fundamental physical properties of the MOS device structure. Fig. 1 gives a non-linear electrical equivalent circuit of the model and its schematic symbol. A set of thirteen parameters for the intrinsic model, plus a number of extrinsic model parameters, determine the operation of the device, including aspects such as noise and mismatch.

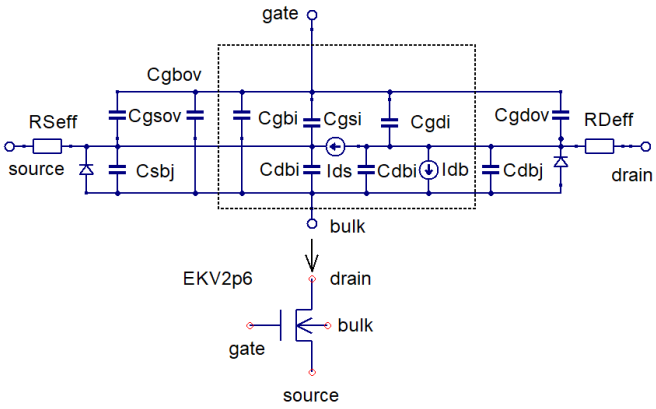

Fig. 1. The EKV2.6 electrical equivalent circuit (simplified) and nMOS schematic symbol: intrinsic EKV2.6 elements are within the dotted box.

III. Test Chip Design

The test chip developed for EKV2.6 model characterization consists of a series of individual n- and p-channel MOSFETs with individual substrate contacts, including multi-finger structures, square and fingered diodes, a CMOS inverter and a ring oscillator. The design parameters for each of the test devices are listed in Table I. The test chip has been fabricated with a 180 nm technology from UMC. A viewgraph of the test chip is shown in Fig. 2.

IV. Electrical Characterization

For assessment of the devices and extraction of the EKV2.6 model parameters, a set of electrical measurements were made. These are outlined in the following subsections.

TABLE I. Design Parameters of Selected Test Devices

Type of devices	Parameters
n-channel MOSFETs p-channel MOSFETs T(N/P)1-14	W=0.24 µm; L=0.18 µm (min.size devices) W=3 µm; L=0.18, 0.24, 0.3, 0.4, 0.6, 1.0 µm W=0.24, 0.3, 0.5, 1.0 µm; L=1.0 µm W=10 µm; L=10 µm (max.size devices) 10 parallel fingers of W=5 µm, L=10 µm W=50 µm, L=10 µm (wide devices)
CMOS inv. INV	W_N=0.24 µm, W_P=0.24 µm, L_N= L_P =0.18 µm
CMOS ring osc. OSC1	W_N=0.24 µm, W_P=0.24 µm, L_N= L_P =0.18 µm 31 stages
n^+-pwell, p^+-nwell diodes D(N/P)1-2	W=L=100 µ W=10 µm, L=100 µm (10 fingers)

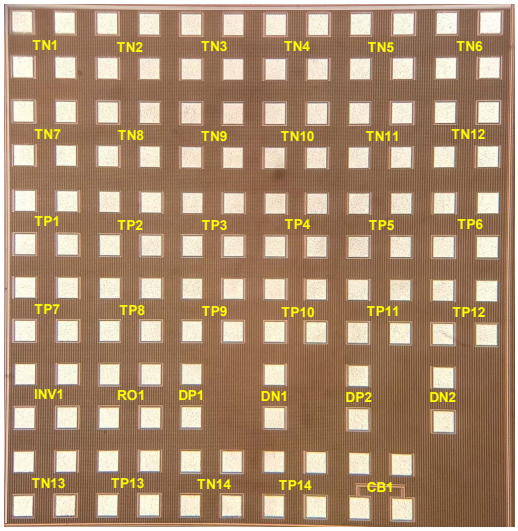

Fig. 2. The test chip layout

A. DC/AC Model Parameter Extraction Procedure

The extraction procedure for the EKV model [8] features varying device sizes, measured characteristics, different bias conditions (SI: strong, MI: moderate, WI: weak inversion, co.: conduction, sat.: saturation) and extracted parameters plus fine tuning. The steps are summarized in Table II.

This extraction procedure benefits significantly from its simple formulation and small number of the EKV2.6 model parameters. Only a small set of 13 intrinsic parameters is required for complete model extraction and characterization, This small parameter set is unique to the EKV model, and accounts for a full range of first and second order device effects. Parameter extraction [8] is performed sequentially starting with DC measurements, which require at least three different device W/L geometries. Technological parameters e.g. gate capacitance COX and junction depth XJ are assumed to be known from a preliminary parameter extraction. The pinch-off voltage measurement V_P vs. V_G is used to extract the core EKV parameters from a long and large device as previously described [8]. The overall efficiency of the nonlinear optimization algorithms used throughout the extraction parameter steps strongly depends on the amount of data used and the complexity of the model equations to be evaluated. Hence. further simplifications of the model equations may be required. Howeve, in such cases the extraction process reverts to a technique which is similar to a 'direct extraction' method.

TABLE II. SIZES, CHARACTERISTICS, CONDITIONS AND PARAMETERS FOR TEST DEVICES.

Device sizes	Characteristics	Conditions	Parameters
Parameter Extraction			
wide/long	I_{DS} vs.V_S V_P vs. V_G I_D vs. V_G	SI sat. MI sat. SI sat.@V_S	I_S, VTO, GAMMA, PHI, KP, THETA
wide/short	I_{DS} vs.V_S V_P vs. V_G I_{DS} vs. V_D	SI sat. MI sat. SI co.-sat.	I_S, LETA, UCRIT, LAMBDA
narrow/long	I_{DS} vs.V_S V_P vs. VG	SI sat. MI sat.	I_S, WETA
W/L matrix	R vs. L_{eff} 1/R vs. W_{eff}	SI co.	DL, DW, RS+RD
Parameter Fine Tuning			
wide/short	log(I_{DS}) vs. V_G I_{DS},log(gds) vs. V_D	WI@V_S SI co.-sat.	LETA, DL, RS+RD,XJ
narrow/long	I_{DS} vs.V_G I_{DS},log(g_{ds}) vs. V_D	WI@V_S SI co.-sat.	WETA, DW

For extraction of the AC model parameters the C-V characteristics of the large size MOSFETs and of the source/drain-substrate junctions are to be made.

B. DC/CV measurements and parameter extraction

For the extraction of the DC model parameters, a series of n- and p-channel MOSFETs (see Table I) were measured at different bias conditions. Next, the EKV2.6 model parameters were extracted. Typical measured I-V data together with the model characteristics are shown in Fig. 3-5. a very good fit between the experimental and model characteristics is visible.

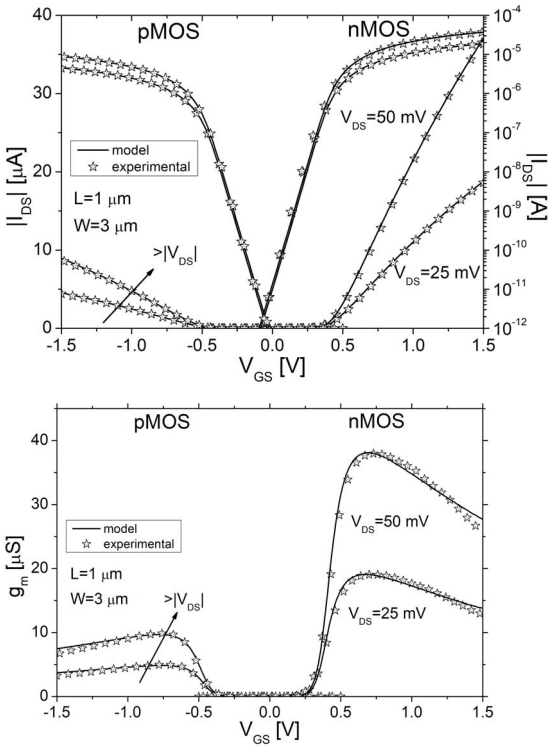

Fig. 3. EKV2.6 transfer I_{DS}-V_{GS} and g_m-V_{GS} characteristics in linear range.

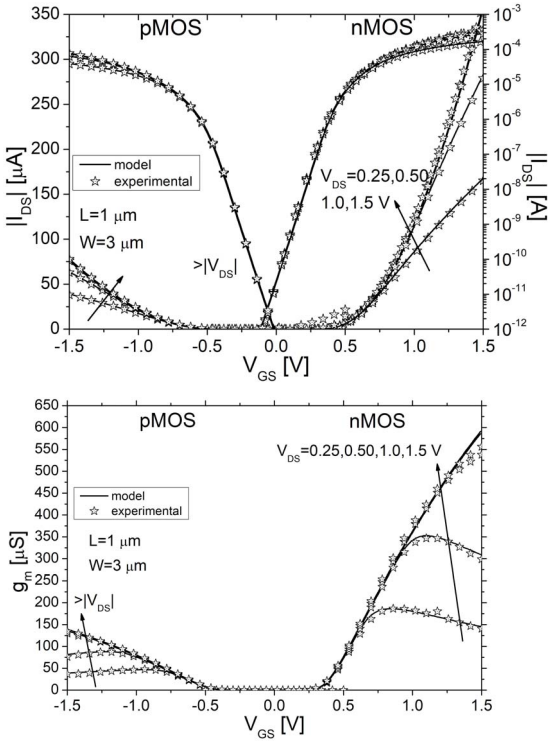

Fig. 4. EKV2.6 transfer I_{DS}-V_{GS} and g_m-V_{GS} characteristics in linear and saturation range.

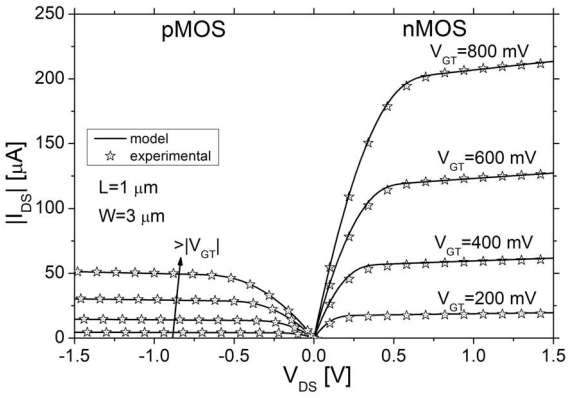

Fig. 5. EKV2.6 output I_{DS}-V_{DS} characteristics.

For the extraction of the AC model parameters, the large area n- and p-channel MOSFETs (see Table I) were measured. The measurement results together with the estimated threshold voltage, flat-band voltage and gate capacitance per unit area are shown in Fig. 6. The gate capacitances, together with the CGSO, CGDO, and CGBO overlap/fringing capacitances determined based on the C_{gs}, C_{gd}, and C_{gb} data in accumulation range, are listed in Table III.

C. CMOS Inverter Characterization.

Within the characterization of the process under consideration for digital IC design, measurements of the CMOS inverter characteristics were done. The transfer curvesfor two different supply bias conditions are shown in Fig. 7. Asymmetry of the MOSFET characteristics is visible.

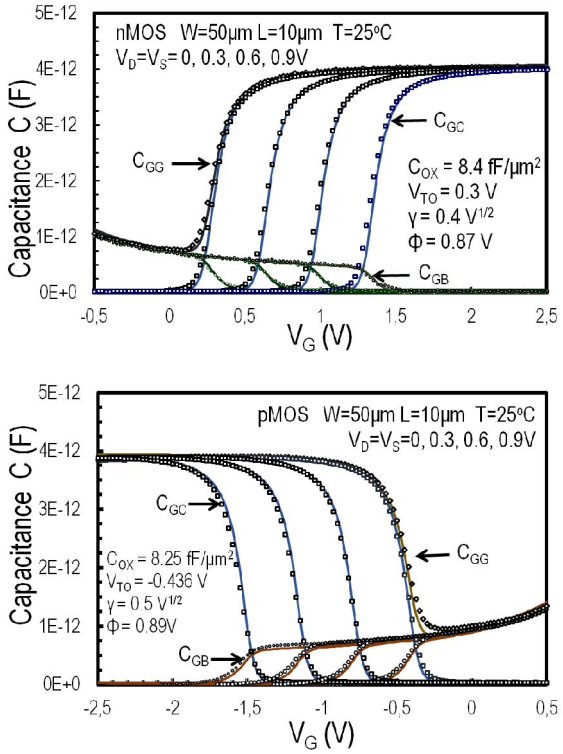

Fig. 6. Extraction of the thresholdvoltage, flatband voltage and gate capacitance in n- and p-channel MOSFETs based on C-V measurements.

TABLE III. AC MODEL PARAMETERS

Param. / Dev.type	COX (fF/µm²)	CGSO (fF/µm)	CGDO (fF/µm)	CGBO (fF/µm)
nMOSFET	8.40	1.33	1.44	81.4
pMOSFET	8.25	1.49	1.64	65.2

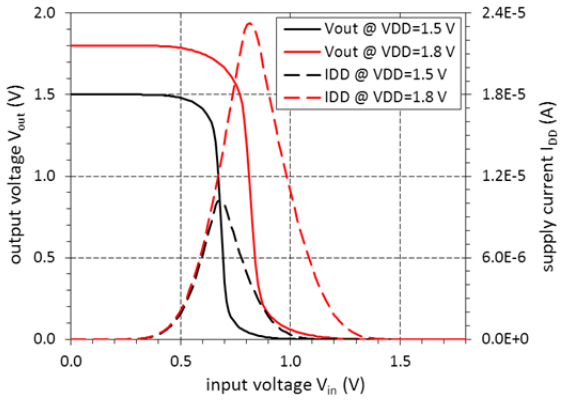

Fig. 7. CMOS inverter characteristics

D. Noise Characterization and Modeling

The EKV2.6 model includes thermal noise as well as low frequency noise. Thermal noise uses a charge-based expression without parameters, while low frequency noise model is of the 1/f noise type and uses three parameters [9]. Measured noise spectra at low frequencies are shown in Fig. 12 for N- and P-MOSFETs, together with respective models.

V. VERILOG-A STANDARDIZATION

The ADMS tool (Automatic Device Model Synthesizer) [10] offers an excellent modeling environment that allows rapid development of advanced simulation models and fast implementation in FOSS, as well as commercial, IC design CAD/EDA tools. ADMS reduces the compact device modeling implementation effort into a process centred on writing a Verilog-AMS model description. ADMS has been designed specifically for analogue compact model development. However, besides those sections of the Verilog-A subset of Verilog-AMS hardware description language that are required for analogue model design and simulation, also many language extensions specifically designed for compact model construction are included. Interfacing ADMS and a circuit simulator is done through XML script files which generate C++ code for the model under construction. These XML scripts are different for each circuit simulator model interface. After translation from Verilog-A to C++ the ADMS generated C++ is compiled and linked to the main body of a circuit simulator code using the C++ toolset available with a given operating system. Existing models could be smoothly extended to include important effects such as thermodynamic effects [11]. Furthermore, developers of new compact models) now have access to a coherent and highly reliable modeling framework, simplifying model evaluation procedures and verification

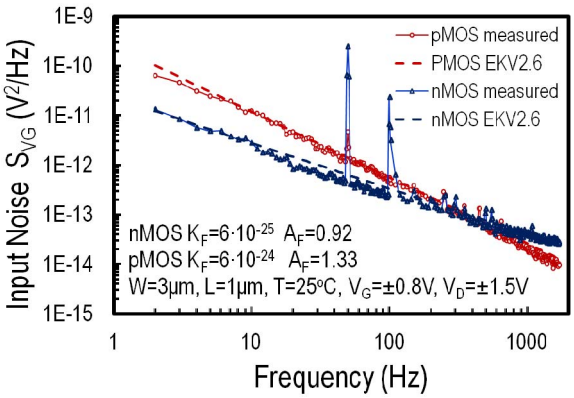

Fig. 8. Input power spectral density $S_{VG}(f)$ for n- and pMOSFETs.

tasks across different simulation platforms and operating systems. Comparisons between the different implementations are straightforward. Similarly, software bug fixes found in one implementation can be easily propagated to other implementations. The procedurę briefly described above was used for implementation of the EKV2.6 model in the Qucs program [12], which is a very efficient circuit simulation and modeling tool.

A. Example EKV2.6 simulation data

To demonstrate the performance of the FOSS EKV2.6 compact MOS model a series of test simulations based on the fundamental long channel MOS device were undertaken, using typical extracted parameter data. Illustrated in Fig. 9,10 are a set of long channel nMOS simulation data obtained using Qucs and a typical set of extracted EKV2.6 parameters.

SUMMARY

The paper presents joint efforts of a number compact modeling groups, which is aimed at providing the Verilog-A code of the EKV2.6 model of the MOS transistors, and distribute/share it with the FOSS CAD/EDA community to support EKV as the Standard Model for ultra low power analog/RF IC design applications.

In order to demonstrate this state-of-the art compact modeling approach consisting in Verilog-A coding and synthesis, we have presented implementation of the EKV2.6 model in the Qucs simulation program, which is the widely recognized simulation and modeling FOSS EDA tool. In order to enable a reliable use of Qucs with the the EKV2.6 model calibrated for the deeply-submicrometer CMOS process. the DC, AC, noise parameters of the EKV2.6 model have been extracted for UMC 180nm CMOS process. The resulting model characteristics remain in a good agreement with the measurement data. This illustrates the efficiency and flexibility of the EKV model.

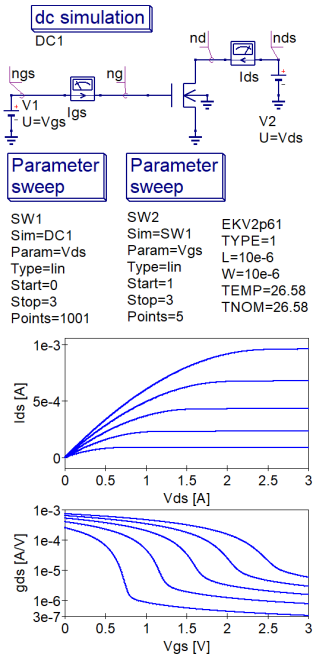

Fig. 9.Qucs EKV2.6 nMOS long channel output characteristic

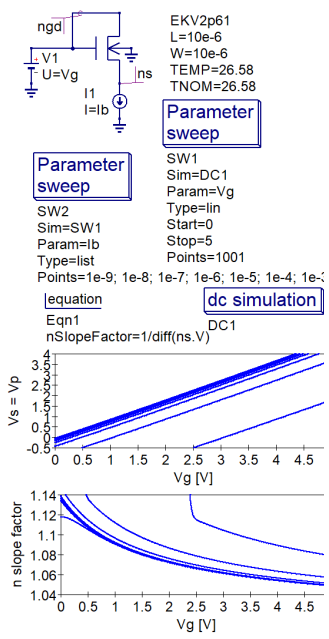

Fig. 10. Qucs EKV2.6 nMOS long channel pinch-off voltage simulation

ACKNOWLEDGMENTS

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