Silicon-Based 0.45-0.47 THz Series-Fed Double Dielectric Resonator On-Chip Antenna Array Based on Metamaterial Properties for Integrated-Circuits

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***Abstract* –The antenna array designed to operate over 0.45-0.47 Terahertz comprises two dielectric resonators (DRs) that are stacked vertically on top of each other and placed on the surface of the slot antenna fabricated on a silicon substrate using standard CMOS technology. The slot created in the silicon substrate is meandering and is surrounded by metallic via-wall to prevent energy dissipation. The antenna has a maximum gain of 4.5dBi and radiation efficiency of 45.7% at 0.4625 GHz. The combination of slot and vias transform the antenna to a metamaterial structure that provides a relatively small antenna footprint.**

***Keyterms*—CMOS, dielectric resonator antenna (DRA), millimeter wave, terahertz, on-chip antenna, silicon.**

I. Introduction

Wireless system-on-chip (SOC) applications are becoming prevalent with the advancement of low-cost silicon technology [1]-[3]. To eliminate the need for external off-chip antenna connections and the associated package processing the interest in implementing on-chip antennas have become of great interest. The consequence of on-chip antenna is to circumvent gain loss and overall size increase [4]. On-chip antennas fabricated using a standard CMOS technology however suffer from poor radiation efficiency (<10%) and poor gain (<10 dBi) performance resulting from high substrate loss and surface wave effects [5], [6].

Several techniques have been previously investigated to improve on-chip antenna performance, which include high-resistivity silicon substrate [7], micro-machining [8], and artificial magnetic conductor [9]. With these techniques the antenna gain is limited to 1.5dBi, and in some cases the design and fabrication process is significantly more complex. Other techniques such as a dielectric lens-based on-chip antenna [10] and an on-chip horn antenna [11] have raised the radiation efficiency to 60% and the gain up to 8dBi. The shortfall of these techniques is the need for an external back-end-of-line (BEOL) process and a larger chip footprint.

In this paper, the feasibility of a low-cost on-chip dielectric resonator antenna (DRA) is investigated. With the proposed technique the radiation efficiency achieved is 45.7% and the gain of 4.5dBi. The antenna is simple to assemble and has a relatively small footprint of 400×400×135 μm^3. The stacked dielectric resonators (DRs) improve the frequency bandwidth and the radiation performance over the frequency range of 0.45-0.47 Terahertz.

II. Proposed THz Double-DR On-Chip Antenna Array Based on MTM

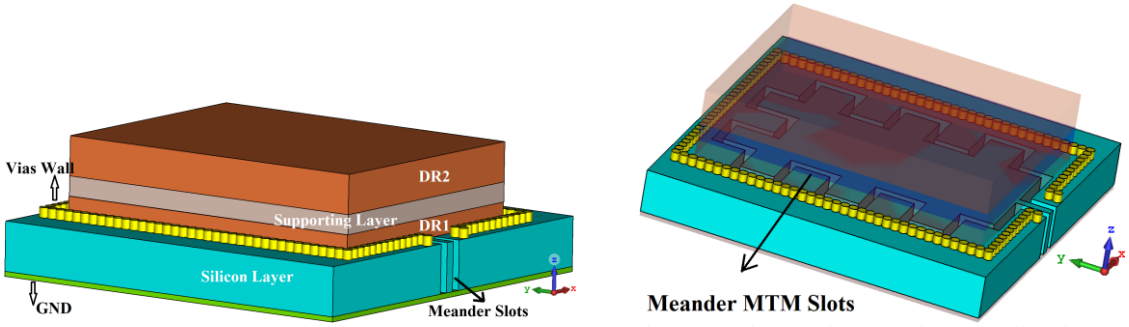
Fig.1 shows the configuration of the proposed on-chip stacked *DRA* array. It consists of a silicon base with a ground-plane layer, two dielectric resonators (DRs), and a supporting layer that sandwiches the two DRs. The structures are secured with Epoxy glue. The feed structure is a meandering slot with a width of 10μm that is fabricated in the silicon base, which has a thickness of 50μm. It is shielded by the bottom ground plane conductor and connected to a 50-ohm grounded coplanar waveguide (GCPW) with line width of 10μm. The meandering slot is surrounded by a rectangular metal wall made of stacked vias to prevent energy dissipation. The meander slots and metallic via wall act as series left-handed (*LH*) capacitors (C_L) and shunt *LH* inductances (L_L), respectively, to actualize metamaterial properties and thereby reduce the antenna dimensions and improve its performance [12][13].

The first dielectric resonator (DR1) is mounted on the surface of the substrate to form a traditional on-chip DRA. Second dielectric resonator (DR2) is arranged above the antenna in the vertical direction (x-axis) forming a series-fed linear array. The dielectric constant of the dielectric resonators is selected to be ε_r=10. Instead of the air gap, a low permittivity support layer is placed between DR1 and DR2 to help minimize the influence of the electromagnetic distribution between the DRs, shown in Fig.1. For multiple DR antenna structures, additional DRs can be stacked in the vertical direction (refer to Fig.1), with low permittivity supporters inserted between the DRs. In the proposed array design, the two DRs resonate at the same frequency of f_0=455 GHz, i.e. the dominant mode ($TE_{\delta 11}{}^x$ mode). With the specified design frequency, f_0=455 GHz, the dimensions of each DR having a dielectric constant of ε_r can be determined using the traditional truncated dielectric waveguide model [16] or a simplified engineering formula presented in [17]. Dimensions of the on-chip antenna structure comprising the series-fed double dielectric resonator antenna arrays are tabulated in Table I.

TABLE I. STRUCTURAL PARAMETER DIMENSIONS

Series Feed On-Chip Antenna size	Si-Layer thickness	GND thickness	Via diameter	Via thickness	DR1 thickness	SL thickness	DR2 thickness	Wslots
400×400×135 μm^3	50 μm	5 μm	5 μm	10 μm	20 μm	20 μm	40 μm	10 μm

In the proposed series-feed antenna array most of the electromagnetic (EM) energy is initially coupled to DR1 from the on-chip meandering slot feeding structure. DR1 radiates its dominated mode $TE_{\delta 11}{}^x$ with high efficiency thereby acting as a traditional on-chip DRA. A portion of this energy is serially coupled to the upper DR2 to excite the $TE_{\delta 11}{}^x$ mode. The series coupling excitation leads to 180° phase change of the electromagnetic waves between the two dielectric resonators.



(a) Isometric view (b) View of the meander MTM slot in the silicon layer

Fig.1. Layout of the proposed series fed double DR on-chip antenna array based on MTM.

The S-parameter response of the reflection coefficient of the proposed series-fed double DR on-chip antenna array is shown in Fig. 2. The proposed on-chip antenna operates over a wide frequency range from 0.450 to 0.475 THz for S_{11}<-15dB, which corresponds to a fractional bandwidth of 5.4%. The average impedance match over its operational frequency range is around 30dB.

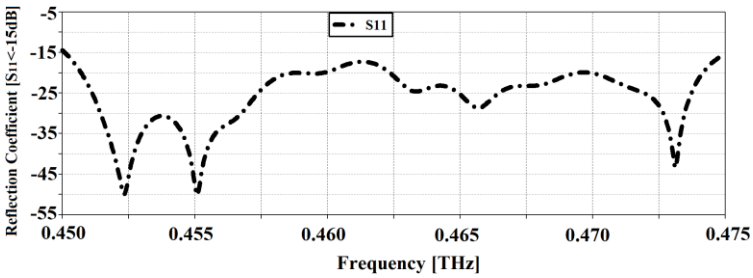


Fig.2. Reflection coefficient response. The impedance bandwidth is defined for S_{11}<-15dB.

The radiation-gain and efficiency response of the proposed on-chip antenna versus frequency are shown in Fig. 3. Maximum gain and efficiency occur at around 0.4625 THz, which are 4.5dBi and 45.7%, respectively. Over the antenna's operating frequency range the minimum gain and efficiency are 3.5dBi and 38.6%, respectively, and the average gain and efficiency are ~3dBi and ~41.5%, respectively. The radiation E- and H-

planes patterns of the proposed on-chip antenna at operating frequency of 0.4625 THz are shown in Fig. 4. The antenna radiates predominately unidirectionally in both E- and H-planes with similar 3 dB beamwidth.

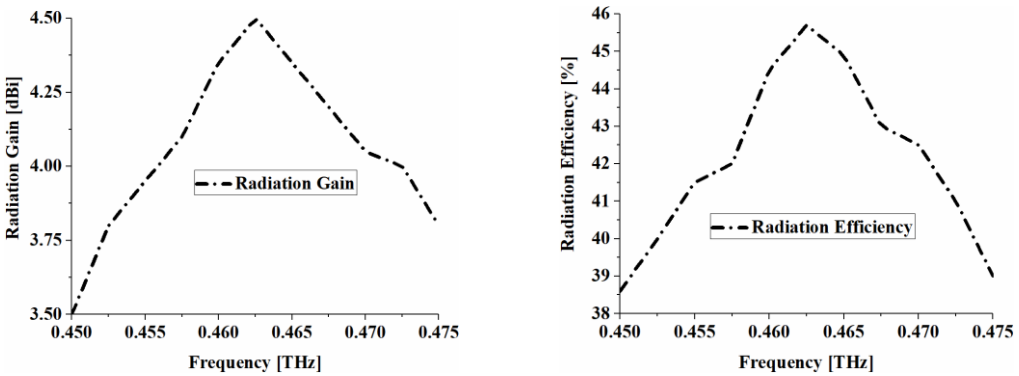


Fig.3. Radiation gain and efficiency response over the antenna's operating frequency range.

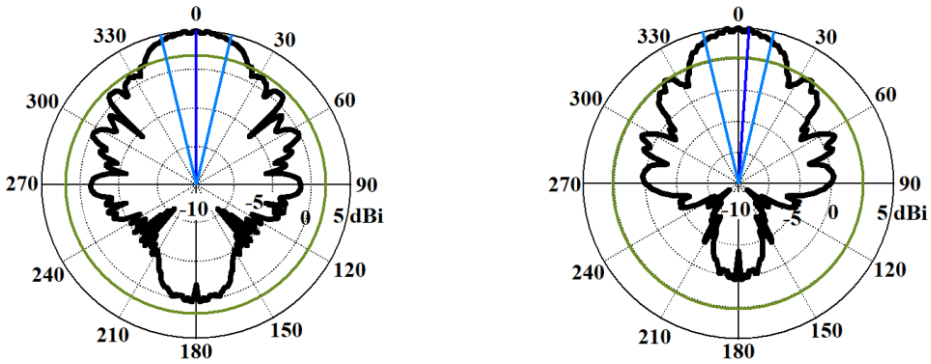


Fig.4. Radiation patterns in the E- and H-planes at 0.4625 THz.

III. Conclusion

An on-chip antenna design is shown to exhibit an optimum gain and efficiency of 4.5dBi and 45.7%, respectively, at 0.4625 THz. The proposed antenna was fabricated using a standard CMOS technology. The proposed antenna array consisted of stacked dielectric resonators on top of a silicon substrate with meandering slot feed-line and the periphery of the silicon substrate is surround with metallic to prevent substrate loss and surface wave effects.

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