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Impact of high-k gate dielectric with different angles of coverage on the electrical characteristics of gate-all-around field effect transistor: A simulation study

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ABSTRACT

In this paper, we consider the electrical performance of a circular cross section gate all around-field effect transistor (GAA-FET) in which gate dielectric coverage with high-k dielectric (HfO_2) over the channel region has been varied. Our simulations show the fact that as high-k dielectric coverage over the channel increases, I_{ON}/I_{OFF} ratio and transconductance over drain current (g_m/I_D) will be enhanced. Moreover, we investigate the impact of channel length scaling on these devices. The obtained results show that subthreshold slope (SS), drain induced barrier lowering (DIBL) and threshold voltage (V_{TH}) roll-off will be reduced as a result of scaling. In this work TCAD simulator was concisely calibrated against experimental data of a GAA-FET from IBM. The Schrödinger equation is solved in the transverse direction and quantum mechanical confinement effects are taken into account.

Introduction

The demand of low power consumption in the integrated circuits, has led to tremendous scaling of transistors during last decades [1,2]. From one perspective, scaling causes improvements in terms of power consumption, speed, functionality, cost per device and device density per chip [3,4]. But as device length reaches to tens of nanometers, some undesirable effects like threshold voltage roll-off, DIBL, increasing leakage current and subthreshold slope appear in the electrical characteristics of device [5–13]. To overcome these short channel effects along with continuing scaling, several strategies have been proposed by experts and pundits of device including of fully depleted-silicon on insulator (FD-SOI) MOSFET [14–17], tunnel FET [18–29], FinFET [30,31], GAA-FET [32,33] and alternative materials like 2D materials [34–55] and III-V compounds [56,57]. Although short channel effect in FD-SOI MOSFETs reduces, but subthreshold characteristics of these devices are not well enough for deep scaling. Due carrier injection in tunnel FETs is based on quantum band to band tunneling mechanism, these devices have excellent subthreshold characteristics in terms of OFF-current and subthreshold slope (less than 60 mV/dec), but drive current is not high enough and they suffer from ambipolar conduction [58]. Presence of fin in the structure of a FinFET helps wrapping gate region over the channel from three sides and this improves gate control over the channel in this device [59–61]. Recently a lot of interesting researches have been done on development of GAA-FET which gate region has completely wrapped over the channel of their structure [62,63]. GAA-FETs are expected of promising candidates for future scaling technology nodes and short channel resistance compared to omega gate, double gate and single gate structures [62,64]. High leakage current and subthreshold slope are of drawbacks of GAA-FETs which make them unsuitable for low power application and steep switching applications [62].

In this work we consider the case in which high-k gate dielectric wrapping around the channel perimeter of a circular GAA-FET varies and its effect on subthreshold slope, drive current, leakage current and short channel effects like threshold voltage roll-off along with DIBL is being studied. The basic structure has been inspired from IBM GAA-FET sample which was concisely calibrated in ATLAS simulator. In order to achieve more reliable results we have considered quantum models. Schrödinger equation along with Poisson's equation have been solved self-consistently to calculate carrier concentration and potential in transverse direction. Carrier quantum mechanical confinement effect is obviously observed in the electron carrier counterplots.

The rest of this paper has been set in the following form. In section II

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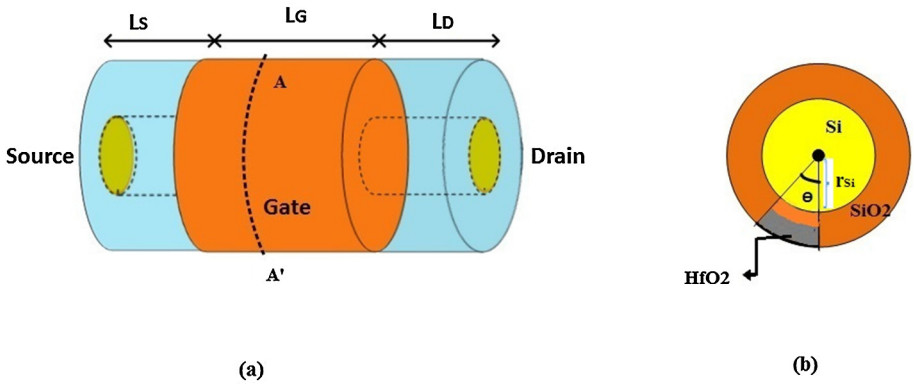

Fig. 1. (a) Schematic view and (b) cross section from AA' of GAA-FET under study.

Table 1
Parameters of GAA-FET under study.

Parameter		Value
Gate oxide thickness	SiO_2 dielectric	0.5 nm
	HfO_2 dielectric	1 nm
Circular silicon channel radius (r_{Si})		6.4 nm
Channel Length (L_G)		22 nm
Source/Drain extended length (L_S/L_D)		20 nm
Lateral Gaussian doping fall off in drain/source		0.02
Source/Drain doping		$5*10^{19}$ cm^{-3}
Gate Workfunction		4.512 eV
HfO_2 permittivity		22 [66]
SiO_2 permittivity		3.9 [66]

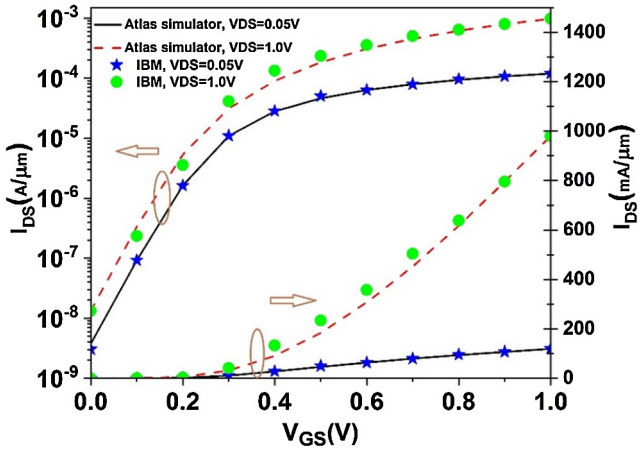

Fig. 2. Calibration of Atlas simulator against experimental results reported in [59] and [67].

we explain the device parameters and simulator settings. In section III the extracted results are discussed and section IV focuses on a comprehensive conclusion about this paper.

Device parameters and simulation settings

Fig. 1 show a schematic view of GAA-FET under study. The circular cross section of this device in Fig. 1(b) depicts gate oxide is comprised of two layers: SiO_2 (thinner layer close to Si channel) and HfO_2 (thicker layer) which is deposited on top of SiO_2.

$HfO_2/SiO_2/Si$ is formed by the following process. First, Si substrate is cleaned by a conventional RCA method and then immersed in HF solution to remove native oxide layer from surface. Afterward HfO_2 is directly deposited on the H-terminated silicon substrate by pulsed laser deposition at room temperature. The HfO_2/Si is then annealed at

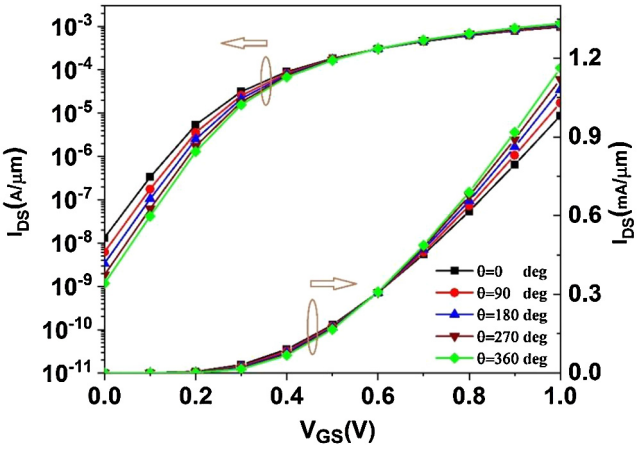

Fig. 3. Logarithmic (left axis) and linear (right axis) transfer characteristics of GAA-FET under study for different theta at V_{DS} = 1.0 V.

various temperatures (500–800 C) in oxygen flow by a quartz tube furnace to form SiO_2 in between. X-ray photoelectron spectroscopy measurement is carried out in order to characterize the sample and annealing condition for growing SiO_2 [65].

Theta depicts the maximum angle which HfO_2 dielectric has covered the channel perimeter. All other parameters related to GAA-FET under study are presented in Table 1.

All simulations in this work have been performed by 3D Atlas simulator, version 5.22.1.R. Atlas simulator can predict the electrical characteristics of semiconductor devices at a specific bias conditions based on physics models enabled. To simulate the GAA-FET under study, we enabled Schrödinger along with drift-diffusion mode-space (DD_MS) models. Schrodinger model calculates eigenfunctions and eigenenergies of the subbands in the transverse direction. Solving Schrödinger's equation along with Poisson's equation can predict carrier concentration and the potential in the device. In other word, once electron concentration is calculated using eigenenergies in each subband by the following equation [66]:

$$n_{vb} = 2\frac{K_B T}{A\pi h^2}\sum_{v}\ln\left[1+\exp\left(-\frac{E_{vb}-E_{F,vb}}{K_B T}\right)\right]\sqrt{m_1^{vb} m_2^{vb}} \quad (1)$$

where n_{vb}, E_{vb}, $E_{F,vb}$, $m_{1,2}$ refer to electron concentration, electron energy, quasi-Fermi level, electron effective mass in subband v with effective mass b. Also, K_B, T, h and A denote Boltzmann's constant, absolute temperature, Planck's constant and normalized area, respectively. Calculated electron concentration from Eq.1 is substituted in the charge part of Poisson's equation and then the potential is extracted. Afterward, the calculated potential substituted back to Schrödinger equation to calculate the wavefunctions and associated electron

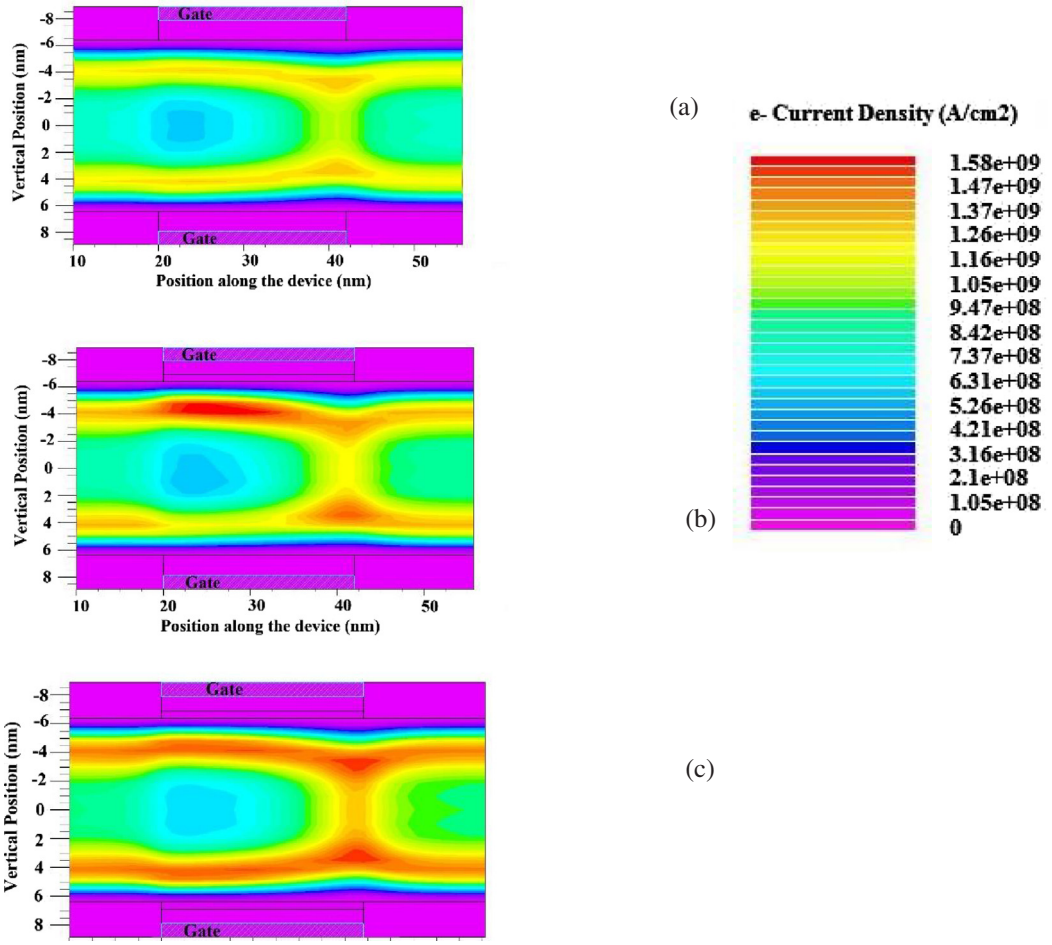

Fig. 4. Electron current density of GAA-FET under study for (a) theta = 45, (b) theta = 180 and (c) theta = 360 degrees at V_{DS} = V_{GS} = 1.0 V.

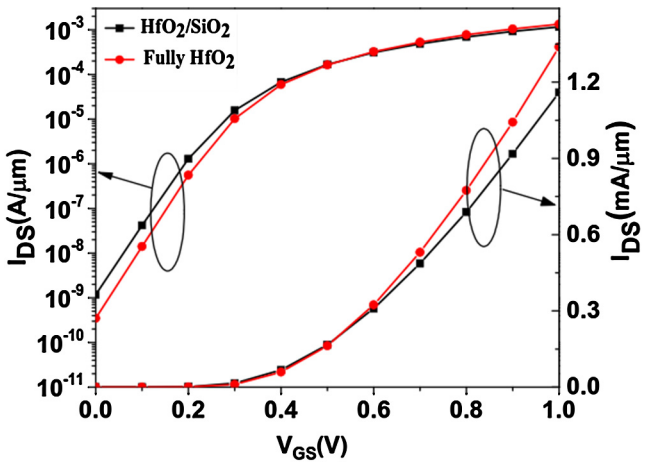

Fig. 5. Logarithmic (left axis) and linear (right axis) transfer characteristics of GAA-FET under study for the case where gate dielectric is only HfO_2 in comparison with the gate dielectric of HfO_2/SiO_2 at V_{DS} = 1.0 V.

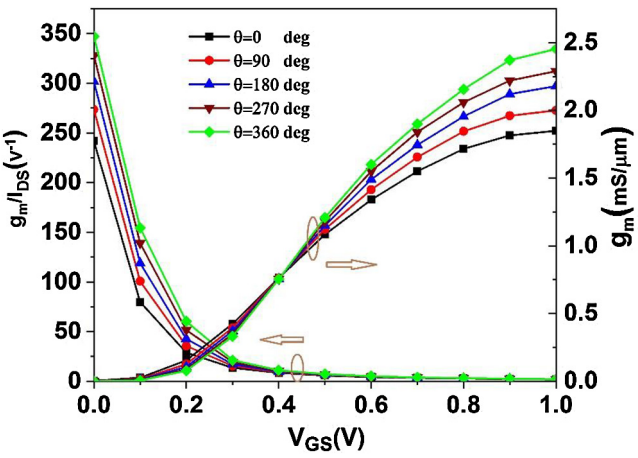

Fig. 6. transconductance over drain current ratio (left axis) and transconductance (right axis) of GAA-FET under study at V_{DS} = 1.0 V.

concentration. This alternating process between Schrödinger's equation and Poisson's equation continuous until convergence and a self-consistent solution between two equations is achieved. Also, DD_MS model is a semi classical transport approach for devices with strong confinement in the transverse direction and it is an alternative to fully quantum approach mode space NEGF (NEGF_MS), which models ballistic quantum transport in a semiconductor device. In fact, by incorporating DD_MS model, classical drift-diffusion equation is solved in the transport direction, while quantum effects can be captured in the transverse direction along with usual ATLAS models for mobility and recombination [66].

By incorporating abovementioned models we calibrated ATLAS simulator against a GAA-FET sample from IBM which was reported in [59] and [67] using carrier mobility and effective mass as fitting parameters. During calibration the non-uniform geometry channel perimeter of 40.21 nm was estimated by a circular cross section with radius r_{Si} = 6.4 nm like literature [59] Fig. 2 depicts that there is a

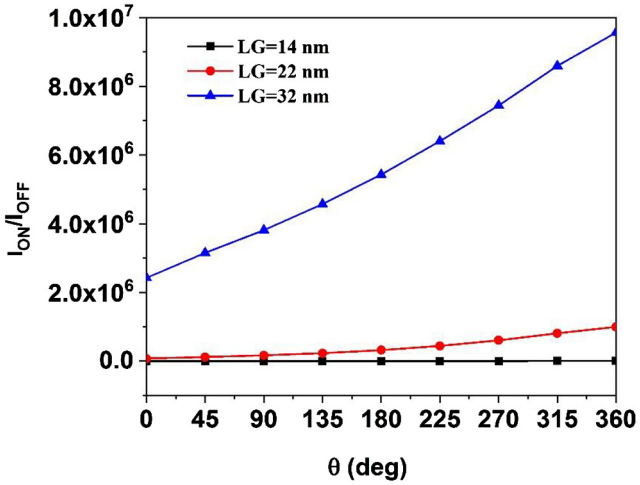

Fig. 7. I_{ON}/I_{OFF} ratio versus theta of GAA-FET under study for different channel lengths of 14, 22 and 32 nm.

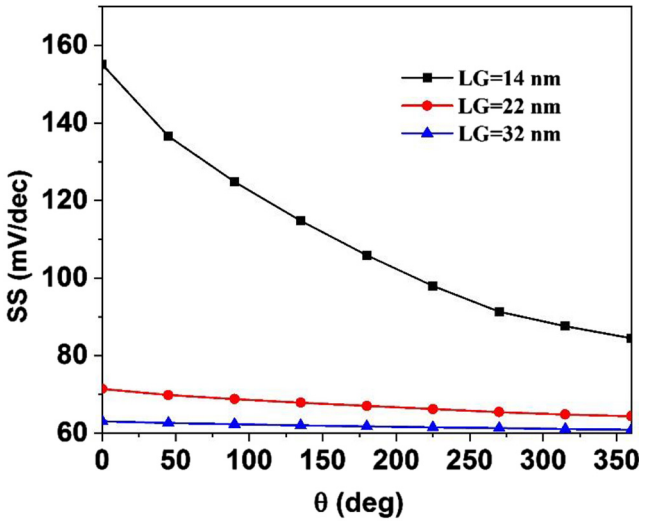

Fig. 8. Subthreshold slope versus theta of GAA-FET under study for different channel lengths of 14, 22 and 32 nm.

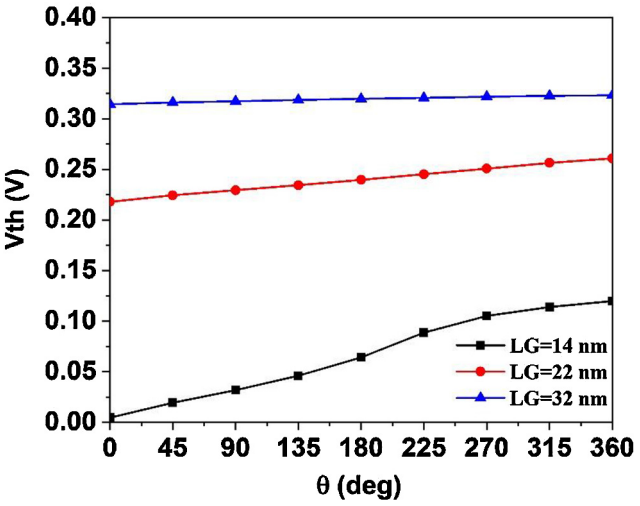

Fig. 9. Threshold voltage versus theta of GAA-FET under study for different channel lengths of 14, 22 and 32 nm.

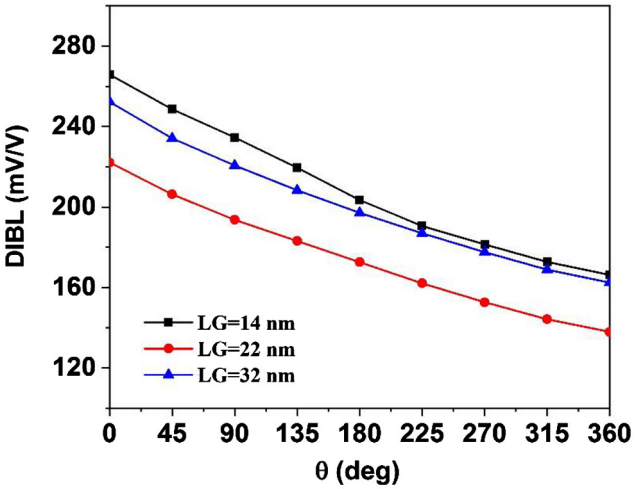

Fig. 10. DIBL versus theta of GAA-FET under study for different channel lengths of 14, 22 and 32 nm.

good agreement in the transfer characteristics (I_{DS}-V_{GS}) obtained by simulator and experimental results from IBM at bias V_{DS} = 0.05 V and V_{DS} = 1.0 V.

Results and discussion

Fig. 3 depicts the transfer characteristics of under study GAA-FET for different theta of 0, 90, 180, 270 and 360 degrees in linear and logarithmic views. It is obtained from this figure that entirely wrapping HfO_2 around the channel region causes one order of reduction in OFF current and about 200 μA enhancement of drive current at V_{DS} = V_{GS} = 1.0 V. This improvement in the device characteristics for higher theta is indebted to better electrostatic controlling of the channel region by gate in GAA-FET with high-k dielectric material which can both reduce OFF-current at low gate voltages and enhance ON-current at higher gate biases.

In Fig. 4 which shows electron current density contour plot for theta of 0, 180 and 360 degrees, quantum mechanical confinement effect is well observed. According to this figure the maximum current density happens about two nanometers far from Si-SiO_2 interface where electrons energy are quantized based on quantum theory [3,68] and as theta increases, electron current density also intensifies due to permittivity increment in the gate dielectric material by HfO_2. This is due to the fact that the electron current density is proportional to electron concentration at the channel which in turn is a function of gate electrode or oxide capacitance (Cox) [15]. Therefore, utilizing a material with higher dielectric constant leads to increased amount of electron current density in the transistor.

To have a view on the transfer characteristic of the GAA-FET device for the case when gate dielectric is fully HfO_2 and assuming HfO_2-Si interface has the same quality of SiO_2-Si, we compare the device performance in two cases where gate dielectric is fully HfO_2 and when the gate dielectric is stack of HfO_2/SiO_2. It is shown in Fig. 5 that when gate dielectric is fully made of HfO_2, subthreshold characteristic improves and drive current increase due to better charge control of gate by utilizing high-k material in the gate oxide. However, it should be noted that using HfO_2/SiO_2 instead of HfO_2 gives a better interface between the silicon and the gate insulator which is caused by better matching of silicon with its native oxide (SiO2) and the process of thermal oxide growth. This is due to the fact that SiO_2–Si has an excellent interface characteristics compared with HfO_2-Si interface due to low interface state and low fixed charge densities [15,30]. As a result, the main benefit of utilizing a high-k dielectric (HfO_2) on top of SiO_2 is to improve transistor performance while controlling interface characteristics.

In other words, using two types of dielectric (high-k over low-k) boosts transistor performance while it yields better control of the properties of interfacial layer.

Transconductance (g_m) in a device means how much drain current is influenced by the gate voltage; or in another words it determines amplification rate. This parameter is a figure of merit in analogue and digital circuits. Also, g_m/I_D ratio reveals how much of energy dissipation (I_D) has led to amplification (g_m) in a device. As Fig. 6 shows, the GAA-FET under study with theta = 360 degree (entirely HfO_2 around the channel) has the best amplification along with efficiency. This improvement indeed is indebted to incorporation high-k dielectric in the gate which reduces OFF current at subthreshold region and enhances drive current at high gate biases.

In another investigation we studied the effect of theta on the I_{ON}/I_{OFF} ratio, SS, V_{TH} and DIBL by scaling in three technology nodes of 32, 22 and 14 nm. Fig. 7 shows that I_{ON}/I_{OFF} ratio enhances by theta due proportionality of drive current with gate dielectric permittivity and this enhancement is much more for channel length of L_G = 32 nm. In fact, by reducing the channel length, leakage current increases and this leads to reduction in I_{ON}/I_{OFF} ratio by scaling in this figure.

Subthreshold slope in a device means how fast the drain current in subthreshold region increase by gate voltage and it is considered by unit of mV/dec. According to Fig. 8, SS parameter reduces by theta and by scaling the device length down, it degrades due to increasing the leakage current and lowering of gate effect on the device performance. It is observed from this figure that SS is very close to ideal value of 60 mV/dec for the channel length of L_G = 32 nm.

Threshold voltage is of important device parameter and in this study it is measured by constant current method. We considered $I_D = 1*10^{-5}$ A, as a criterion and measured the gate voltage related to this current to finding threshold voltage value. Fig. 9 depicts the amount of V_{TH} roll-off reduces by theta which means the device stamina against this short channel effect improves. According to this figure, by scaling down the V_{TH} variation increases with theta which is mostly due to leakage current increment rate in this device.

Drain induced barrier lowering is another short channel effect which reveals how much channel region is influenced by drain bias. In order to calculate this parameter we utilized following relation:

$$DIBL = \frac{V_{g1} - V_{g2}}{V_{DS2} - V_{DS1}} \quad (3)$$

V_{g1} and V_{g2} are gate biases which their correspondence drain currents are $I_{DS} = 5.5*10^{-5}$ A at V_{DS1} = 1.0 V and V_{DS2} = 0.05 V respectively. The mentioned drain current is quite arbitrarily has been chosen. Fig. 10 shows DIBL phenomenon reduces for three technology nodes by theta, which it means better electrostatic control over the channel by high-k material can immune the device from this undesirable short channel phenomenon.

Conclusion

The influence of high-k dielectric coverage over the channel perimeter of a GAA-FET was investigated on the electrical parameters like I_{ON}/I_{OFF}, g_m/I_D, threshold voltage, subthreshold slope and DIBL. Based on simulation results, as HfO_2 covers more channel perimeter, gate electrostatic control over the channel increases and then subthreshold characteristics including off-state current along with SS were reduced while drive current, g_m/I_D ratio and device stamina against short channel phenomenon were increased. The GAA-FET under study was concisely calibrated against experimental data of an IBM counterpart sample. It was predicted that incorporation high-k dielectric in the gate can reduce off-state current down to one order of magnitude and enhance drive current up to 200 μA. Furthermore, a comprehensive simulation was carried out to study the impact of channel length scaling on the device figures of merit.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.rinp.2019.102823.

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