Design of Integrated Mixer for 5G Radio Transceiver

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ABSTRACT OF THE
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The increased demand of high data rate, low latency and wider bandwidth is pushing the wireless communication towards higher frequencies. 3GPP (third generation partnership project) allocated NR (new radio) FR2 (frequency range 2) n257 (26.5 - 29.5 GHz) and n258 (24.25 - 27.5 GHz) bands for high-speed communication. It is challenging to achieve high linearity at higher frequencies with low supply voltage and smaller size devices.

This thesis presents design, implementation and simulation results of integrated downconversion mixer for modular 5G radio transceiver. The first stage downconversion mixer, implemented in GF FDSOI 22 nm process will be used in super-heterodyne double downconversion transceiver, operates at 28 GHz input frequency and provides 6-7 GHz intermediate frequency (IF). The pre-layout and post-layout simulation results of double-balanced mixer topologies optimized for high linearity are compared in terms of conversion gain (CG), input third-order intercept point (IIP3), double sideband (DSB) noise figure (NF), LO-to-IF leakage, and dc power consumption. The mixer topologies, including Gilbert cell and variants of Gilbert cell with resistive and inductive degeneration, and mixer with transformer input, show trade-off between conversion gain, linearity, dc power consumption, and area. Under 0.8-V supply voltage, the transformer input mixer achieves highest IIP3 of +16.34 dBm while dc power consumption including LO buffer is 5.7 mW and NFdsb is 13.7 dB.

Keywords: Mixer, Active mixer, Passive mixer, Gilbert cell mixer, Transformer input mixer, Inductive source-degeneration

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Bilal Bashir

Contents

Abbreviations

3GPP	third-generation partnership project
4G	fourth generation
5G	fifth generation
AM	amplitude modulation
CG	conversion gain
CMOS	complementary metal-oxide semicondutor
dB	decibel
dc	direct current
DCR	direct conversion receiver
DSB	double sideband
EM	Electro-magnetic
FDSOI	fully depleted silicon-on-insulator
FET	field effect transistor
FR1	frequency range 1
FR2	frequency range 2
GHz	giga Hertz
HD2	second-order harmonic distortion
HD3	third-order harmonic distortion
IF	intermediate frequency
IIP3	input referred third order intercept point
IIP2	input referred second order intercept point
IP_1dB	input referred 1-dB compression point
IM2	second-order intermodulation
IM3	third-order intermodulation
I/Q	in-phase / quadrature
LO	local oscillator
LNA	low noise amplifier
LTE	long term evolution
MOSFET	metal oxide semiconductor field-effect transistor
mmW	millimeter wave
P1dB	input referred 1-dB compression point
PSD	power spectral density
NF	noise figure
nm	nano meter
NR	new radio
RF	radio frequency
SFDR	Spurious-free dynamic range
SNR	Signal-to-noise ratio
SNDR	Signal-to-noise-and-distortion ratio
SSB	single sideband
SLVT	super low threshold voltage
TIA	transimpedance amplifier
Tx/Rx	transmitter / receiver

1 Introduction

In recent years, millimeter wave (mmW) communication at 28 GHz radio frequency band has obtained great importance for 5G (fifth generation) wireless communication and radar applications [1]. The existing technologies, such as the 4th generation (4G) mobile communication known as LTE (Long Term Evolution), are not able to cater the growing needs of high data rate, low latency and wider bandwidth. A more advanced generation of wireless broadband communication is resulting in 5G [2]. Recently, 3GPP (third-generation partnership project) allocated new radio (NR) frequency bands for 5G communication. The frequency bands are splitted into frequency range 1 (FR1) and frequency range 2 (FR2), which include 0 - 6 GHz and above 24 GHz, respectively. The bands of interest in this thesis are n257 band (26.5 - 29.5 GHz) and n258 band (24.25 - 27.5 GHz) [3].

The demand for high data rate is increasing rapidly for industrial, medical, virtual and augmented reality, and 8K video streaming applications [4]. It is forecasted that wireless data traffic would increased 10,000 times in the next 20 years, mainly due to increased use of smartphones, tablets, and internet of things [5]. Recently, the radio frequency band at 28 GHz has received much attention due to its potential use in autonomous vehicles by automotive industry [4]. Short range radars are extensively used in the automotive industry to develop safe and intelligent self-driving cars, which will provide basis for safe and intelligent transport system [6]. The 5G communication standard will provide low latency, ultra-high mobile broadband, high reliability and less energy consumption for applications such as high definition audio/video streaming, e-health and IoT [4]. Low latency means less delay, which becomes more important when applications require quick response times, such as autonomous vehicles and medical operation theaters.

In recent years, research activity to develop high-frequency devices at 28 GHz band with smaller dimensions has grown rapidly. Smaller dimensions reduce power consumption and silicon area at the cost of integration complexity. Devices for the 60 GHz frequency band have been researched and developed extensively because the 60 GHz radio frequency band was allocated for high speed data rate, high capacity and high quality video streaming [7],[8].

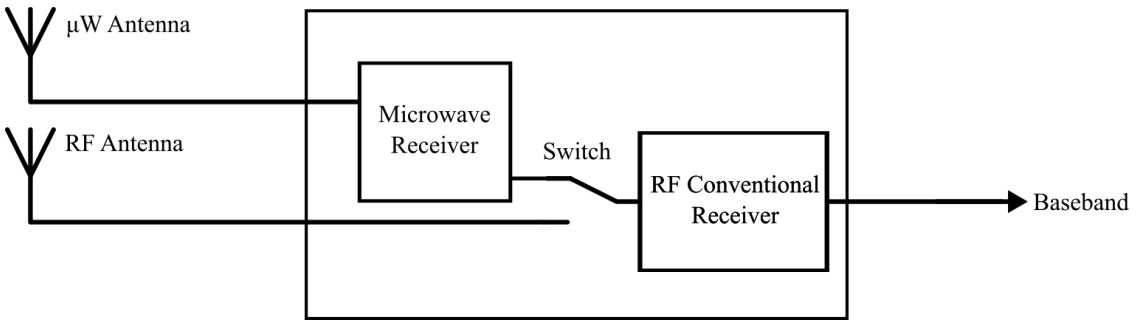


Figure 1: 5G NR FR2 modular radio receiver

Recently, the research focus has shifted toward the 28 GHz band. A modular design for a 5G NR (New Radio) FR2 (Frequency Range 2) radio receiver is proposed

in Fig. 1. It consists of two antennas: one for a microwave receiver operates at 26.5 - 29.5 GHz frequency and the other for an RF conventional direct conversion receiver (DCR) operates at 0 - 6 GHz frequency. A switch is used to select the appropriate RF frequency for the receiver. The microwave receiver down-converts the frequency to an intermediate frequency (IF), which is then down-converted to a baseband frequency by the direct conversion receiver. The structure can be considered as a super heterodyne double downconversion receiver.

The aim of this thesis is to design and simulate an integrated mixer for 5G radio transceiver front-end at 28 GHz frequency in 22 nm FDSOI technology and compare the performance of different mixer topologies in terms of performance metrics. Since the downconversion mixer is one of the most important block of receiver front-end design [9] because overall linearity and noise figure is limited by the mixer [10]. The receiver front-end, including the downconversion mixer, has been extensively researched and developed in 28 nm, 45 nm, and 65 nm complementary metal-oxide semicondutor (CMOS) technology. However, the downconversion mixer at 28 GHz band in 22 nm fully depleted silicon-on-insulator (FDSOI) technology has not yet researched. Since the performance of downconversion mixer is measured by its high linearity and less sensitivity to noise, the noise of circuits increase and linearity degrades as the technology shrinks. Therefore, the prime focus of this thesis is to compare the linearity performance of mixer topologies.

1.1 Millimeter wave Receiver Front End

Fig. 2 shows the proposed 28-GHz receiver chain architecture. At 28 GHz frequency, which is a lower edge of millimeter wave communication [2], both double conversion and direct conversion transceiver architectures can be employed with a trade-off between performance metrics. The double-conversion transceiver in [11] uses sliding-IF with a 28 GHz RF obtaining 8 GHz internal IF and 3-GHz baseband frequency. The double-conversion transceiver has the advantage of low LO frequency, i.e. 21 GHz used in this thesis. Other advantages of the double-conversion transceiver architecture are lower I/Q mismatch, easy power combining/splitting at IF, and higher linearity can be achieved at the cost of an extra mixer. The direct conversion architecture of [12] has the advantage of low noise figure and high linearity performance, inherent advantage of simple Tx/Rx chains and no problem of image signal filtering, which is essential in double conversion transceiver.

In the design of downconversion mixer for 5G transceiver, different mixer topologies are compared and results obtained for the most suitable design topology at 28 GHz frequency in 22 nm FDSOI technology. The proposed mixer design ensures high linearity and less sensitivity to noise, which are basic requirements for high-speed communication.

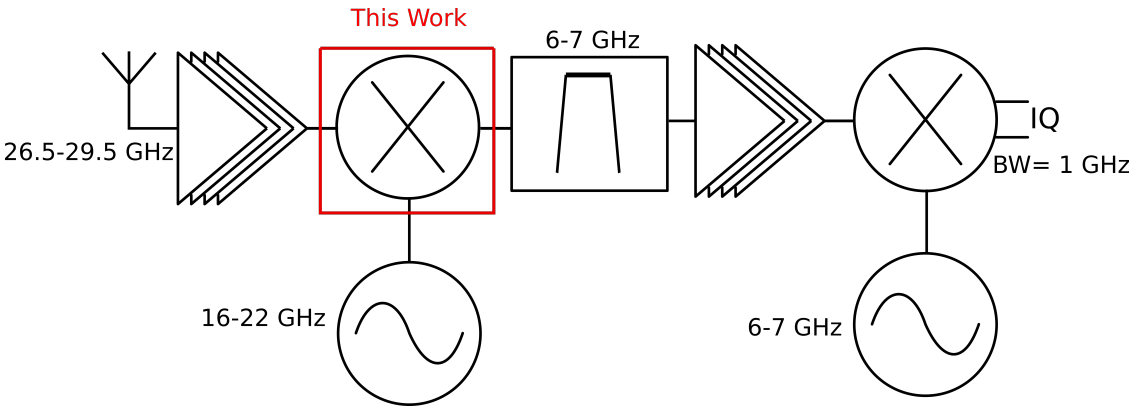


Figure 2: Millimeter wave receiver front-end architecture

The remainder of the thesis is organized as follows. Chapter 2 reviews the literature covering the methods used in the design process. Chapter 3 describes the primitive mixers. Chapter 4 presents the development of design and simulation results. Finally, Chapter 5 summarizes the work and presents the most important conclusions drawn from the comparison of pre- and post-layout simulation results.

2 Radio Frequency Receiver Front-End

This chapter briefly describes the modern transceiver architecture used in high frequency communication and discusses in detail the architectures of mixers. The performance of mixers is determined by performance parameters that include: conversion gain, noise and noise figure, gain compression, third order non-linearity (IIP3), second-order non-linearity (IIP2), RF-to-IF and RF-to-LO feedthrough, LO-to-IF and LO-to-RF feedthrough. The chapter follows as: Section 2.1 describes the basics of frequency mixer/multiplier, Section 2.2 discusses the performance parameters required to understand the performance of mixer, Section 2.3 gives the overview of balanced mixers, Section 2.4 focuses on passive downconversion mixer design, and Section 2.5 is dedicated to active downconversion mixer topology.

2.1 Frequency Mixer/Multiplier

A mixer is the building block of Transmitter (Tx)/Receiver (Rx) front end design. The mixer translates one frequency to another frequency by multiplying two waveforms in the time domain. The mixer has three distinct ports. In a receiver architecture, the downconversion mixer receives input signal at an RF port, local oscillator (LO) waveform at the LO port and gives the output waveform called the intermediate frequency (IF)/baseband frequency at the IF/baseband port. Similarly, in transmitter design, up-conversion mixer takes the input signal at the IF port and output signal is transmitted through the RF port, while the LO waveform is applied at the LO port [13] [14] [15].Fig. 3 shows the basic diagram of up-conversion and downconversion mixers.

Since frequency translation cannot be achieved with linear, time-invariant systems, thus the mixers must be either time-varying or nonlinear to provide frequency translation. A mixer can be realized with an ideal switch toggling between 0 and 1, i.e. OFF and ON and a load resistance. Fig. 4 shows a basic mixer circuit with ideal switch. Let us consider that V_{LO} = A cos $\omega_1 t$ and V_{RF} = B cos $\omega_2 t$, then the output of the mixer can be expressed as:

$$V_{IF} = A\ cos\omega_1 t\ *\ B\ cos\omega_2 t \tag{1}$$

(a) downconversion mixer **(b)** Up-conversion mixer

Figure 3: Block diagram (a) downconversion mixer, (b) Up-conversion mixer

$$V_{IF} = \frac{AB}{2}\left[cos(\omega_1 + \omega_2)t + cos(\omega_1 - \omega_2)t\right] \quad (2)$$

where A and B are amplitudes of LO and RF waveform, ω_1 and ω_2 are frequencies of LO and RF waveform, respectively, and t represents the time. The right hand side of Eq. 2 contains two frequency components, the sum $\omega_1 + \omega_2$ and the difference $\omega_1 - \omega_2$ frequency. The sum is selected for the transmitter and difference is selected for the receiver. In addition, spurious components called "mixing spurs" are also produced when a sinusoid is applied to the nonlinear system, not shown in Eq. 2. It is always desired that the LO provides abrupt switching to achieve better gain and lower noise, while the mixing spurs occur due to high nonlinearity of the LO port. However, in practical cases it is not always possible to achieve abrupt switching of LO signal [15] [16].

The circuit of Fig. 4 is single-ended mixer, which is rarely used in practical radio frequency applications. During the period of time when the switch is in *on*, the IF output is the same as the RF input signal and discards the RF signal during other half of the LO period. Mixers are mainly divided into two categories: 1) passive mixers and 2) active mixers [15]. Their balanced structures are available and commonly used in RF circuits known as single-balanced and double-balanced discussed in Section 2.4.

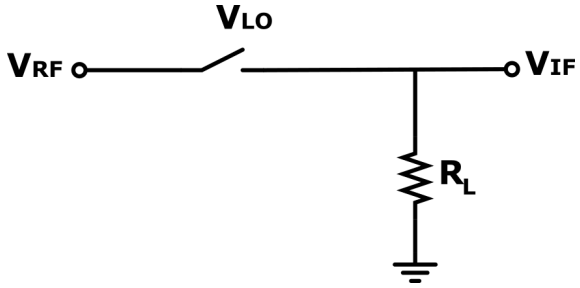


Figure 4: Basic mixer circuit with ideal switch

The performance of mixers is determined by performance parameters, such as, linearity, conversion gain, port-to-port isolation, and noise figure. In this chapter, general concepts of mixer are developed with discussion on performance parameters. The detailed discussion of mixer topologies is covered in Section 2.4. In addition, passive and active downconversion mixers are analyzed in perspective of high-frequency 5G bands.

2.2 Performance Metrics

The performance of mixer is determined by performance parameters like all other devices involved in the front end design. Performance metrics for mixer are: conversion gain, nonlinearity, noise and noise figure, gain compression and port-to-port isolation. In this section, the terms of performance parameters are defined and discussed to understand the mixer discussion in Section 2.4 and Chapter 4.

2.2.1 Conversion Gain

One important metric of performance is the conversion gain (or loss) of the mixer. It is defined as the ratio of the IF output to the value of the RF input or more specifically, the ratio of the rms (root mean square) voltage at the IF output to the rms voltage at the RF input. It is usually desired that the conversion gain of a mixer be greater than unity to suppress the noise contribution in the subsequent stages of receiver front end.

The conversion gain of active mixer can be expressed as power quantity, however, passive mixer be better expressed in voltage or current conversion gain. Generally, voltage conversion gain is preferred in modern RF designs because the impedances are not always equal and mostly imaginary, thus make it difficult to use power quantities.

Active mixers provide amplification along with frequency translation, thus the conversion gain of active mixers is generally greater than unity. Since the technology is shrinking and supply voltage is decreasing, this limits the conversion gain of active mixers to retain the same linearity. The conversion gain of passive mixers cannot be greater than unity and typically less than -3 dB but passive mixer offer superior linearity performance. The voltage conversion gain of a downconversion mixer can be measured by applying a sinusoidal signal at RF port and measuring the signal amplitude at the IF port [15] [16].

2.2.2 Linearity

Linearity is an important parameter of performance measurement because it defines how large signal is handled by the system and sets the upper limit for the large input signals. In an ideal linear system, the output of the system linearly depends on the input. [16]. A linear static system that does not depend on the past values of input or output (a system without any memory) can be described as:

$$v_{OUT} = \alpha(v_{IN}) \tag{3}$$

where v_{OUT} is the output of the system, v_{IN} is the input to the system, and α is the function of time for time-variant system [15].

A mixer is linear if the IF output is proportional to the amplitude of the RF input signal. However, in reality the transfer function is lot more complicated, either due to active and passive components in the system or due to power supply that limits the signal swing. The input-output relationship of a nonlinear system can be mathematically expressed with a power series expansion as:

$$v_{OUT} = \sum_{n=0}^{N} \alpha_n(v_{IN}) \tag{4}$$

where N represents the nth-order nonlinearity. The above equation can be expanded using the power series expansion.

$$v_{OUT} = \alpha_0 + \alpha_1(v_{IN}) + \alpha_2(v_{IN})^2 + \alpha_3(v_{IN})^3 + ... \tag{5}$$

Nonlinearity requires infinite terms to be described perfectly, however, in most practical applications, first three terms are sufficient. The output in Eq. 5 contains: DC terms, harmonics of fundamentals, and intermodulation products of those harmonics. The desired components are first-order mixing terms and all other higher order terms are undesired in mixer design. The undesired spectral components include second- and third-order harmonic distortion (HD2 and HD3), second- and third-order intermodulation terms (IM2 and IM3), and intermodulation of harmonic components [16] [17].

The presence of two or more signals (tones) in a nonlinear circuit generates intermodulation products. Suppose that the input consists of two tones: $vIN = A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t)$, then the output will be:

$$v_{OUT} = \alpha_1 \Big[A_1 cos(\omega_1 t) \ + \ A_2 cos(\omega_2 t) \Big] \ + \ \frac{3\alpha_3 A_1^2 A_2}{4} cos(2\omega_1 - \omega_2)t + \frac{3\alpha_3 A_2^2 A_1}{4} cos(2\omega_2 - \omega_1)t \ + \ ... \quad (6)$$

In the frequency domain, third-order products are the intermodulation distortion products between one of the fundamental signals and the second harmonic of the other signal. Many of the spurious tones are out-of-band and cause no problems. However, the third-order intermodulation products $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$ are near to the fundamental frequency and likely to fall in the passband of intermediate frequency adding distortion to the output signal.

Third-order intercept point (IP3) is a metric or figure of merit for linearity that is used to describe the intermodulation performance of a mixer. Two-tone third-order intermodulation products can be used to characterize the linearity of mixer. Apply two signals at the input of the mixer having equal amplitudes and normally one channel apart.

To find the IP3 point, plot the desired or fundamental output and third-order intermodulation (IM3) output as a function of input power level. The fundamental output grows 20 dB/decade and IM3 output grows 60 dB/decade. In other words, the slope of the fundamental output and IM3 output is 1 and 3, respectively. The intersection point (an imaginary point) can be found by extrapolating the two curves as shown in the Fig. 5 . The intersection point gives the input referred third-order intercept point (IIP3) and output referred third-order intercept point (OIP3).

A second-order intercept point (IP2) is also a metric of performance measurement and important in direct downconversion receiver design. It occurs due to second-order distortion products and can be defined similar to the third-order intercept point. The second-order intermodulation terms rise at 40 dB/decade and intersect the fundamental output when the curves are extrapolated [17] [18].

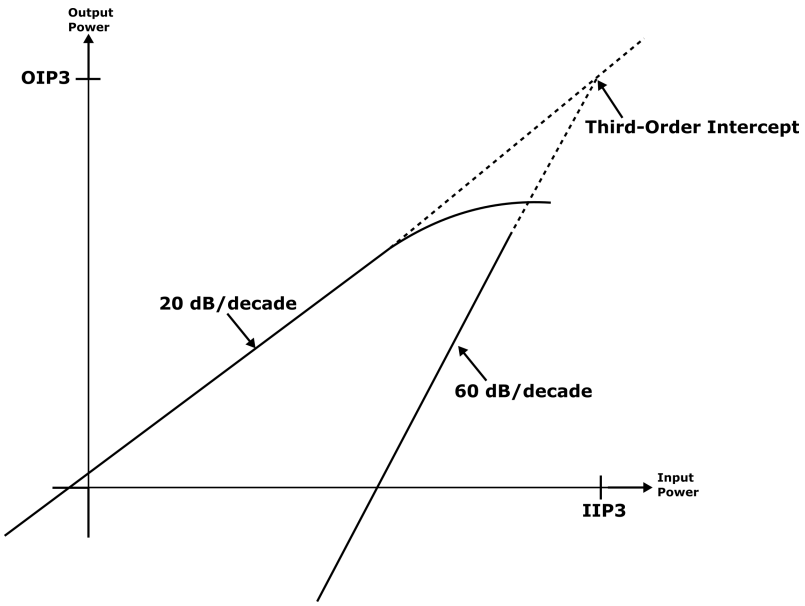


Figure 5: Mixer linearity parameters

2.2.3 Gain compression

Another way to characterize the linearity of mixer is finding the compression point. Since, compression and IP3 are numerically related, so identifying components that cause compression also identify components that cause IP3 problems. The measurement of compression point also requires one tone instead of two tones (required for IP3)

Just like real amplifiers cannot achieve infinite gain and experience compression at some point, real mixers have some limit beyond which output cannot follow the input linearly. The point where the output power drops by 1-dB compared to the power if the device would have been linear is the 1-dB compression point (P_{1dB}). The 1-dB compression point can be expressed mathematically as:

$$20\ log_{10}\left(\frac{v_{OUT}}{v_{OUTi}}\right)\ =\ -1\ dB \tag{7}$$

where v_{OUT} is the actual output voltage and v_{OUTi} is the ideal output voltage.

2.2.4 Noise Figure

Noise figure (NF) is a figure of merit that determines the quality of a signal in the receiver front end. It is defined as ratio of sigal-to-noise ratio (SNR) at the input (RF) port to the SNR at the output (IF) port.

$$NF = \frac{SNR_{RF}}{SNR_{IF}} \tag{8}$$

The noise figure can be single sideband (SSB) and double sideband (DSB). Before defining SSB noise figure and DSB noise figure, it is important to understand the downconversion mixing process. The mixer takes two input frequencies and generates

an intermediate frequency. One is the desired RF signal and the other is unintended image signal. Since the intermediate frequency is the magnitude of the difference between the RF and LO frequencies. The mixer translates the input signal, the noise in the input signal band and the noise in the image band to the intermediate frequency (ω_{IF}). The mixer gives $\omega_{IF} = \omega_{RF} - \omega_{LO}$ and $\omega_{IF} = \omega_{Image} - \omega_{LO}$ frequencies. Thus, the IF contains the desired RF signal and the undesired image signal.

The noise figure quantity is called the SSB noise figure when the desired signal exists only on one side of the local oscillator (LO) frequency, and the quantity is called DSB noise figure when the desired signal exists on both sides of the LO frequency. The SSB noise figure of a mixer is generally 3 dB higher than the DSB noise figure. Since, both have the same IF noise but in SSB the signal power resides only on single sideband i.e. ouput SNR is half the input SNR (if the two noise components have equal powers).

Noise figure of mixers is considerably higher than those of amplifiers because noise from frequencies other than the desired RF frequency can mix down to the intermediate frequency. Because the mixer is a noisy component, a low noise amplifier (LNA) is employed to amplify the signal levels well above the noise of mixer and subsequent stages.

2.2.5 Port-to-Port Isolation

Port-to-port isolation among three ports of the mixer is important because the signal leak from one port to another port can corrupt the desired signal. The leakage of signal occur through the capacitances present in the MOSFET device, for example, gate to drain and gate to source capacitance. However, the degradation of performance of mixer due to port to port feed-through depends on the type of architecture used. Consider a downconversion mixer as shown in Fig. 6.

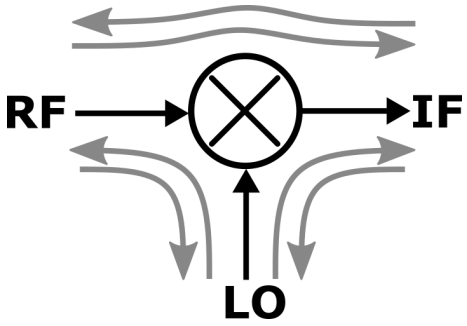


Figure 6: Port-to-port feed-through in a mixer

LO-to-RF Feedthrough The LO signal is a large signal and in direct down-conversion receiver it can leak to the RF port and reach to the antenna and radiate from the antenna, which is very undesireable. The LO leakage can also cause dc offset at the output of the mixer because the LO leakage can add to the RF input and then translated to IF. The problems of LO radiation and dc offset at the output can be eliminated with symmetric mixer design (including devices) and LO waveforms.

The phenomenon of offset is also known as LO self-mixing due to the fact that the leaked LO signal add to the RF input signal and mixed with the LO waveform. The output dc offset also disappears if the source resistance becomes zero, usually not the case. In case of heterodyne receiver, the LO-to-RF leakage is not important because LO lies outside the RF band and attenuated by the LNA, the band-select filter and the antenna.

RF-to-IF Feedthrough The RF to IF isolation is usually high in both direct conversion receiver and heterodyne receiver architecture. However, RF-to-IF leakage can corrupt the baseband signal by the beat component resulting from even order distortion in the RF path.

LO-to-IF Feedthrough The LO to IF feed-through in direct conversion receivers can cause problems for the stage following the mixer, however, low-pass filter is usually employed to pass the desired frequency and blocking all high frequencies. In the case of heterodyne architecture the LO feed-through can desensitize the following mixer (causing dc offset in the baseband) if ω_{IF} and ω_{LO} of the second stage mixer are very close to each other.

2.3 Balanced Mixer Design

2.3.1 Single-Balanced Mixer

The mixer shown in Fig. 4 is a simple single-ended mixer design that can be realized with a MOSFET and a load resistance as depicted in Fig. 7. It operates with a single-ended RF input and single-ended LO signal. The RF input is applied at the source/drain terminal and LO is connected ot the gate terminal of the transistor. Since the LO signal remains unavailable during one half of LO cycle, thus the RF input signal is discarded during that period of time. The information is lost in the process. An efficient topology is to employ a differential LO input that commutates the RF input during each half of the LO cycle and results differential output. Since LO port is balanced but RF input is still single-ended, thus the topology named as "single-balanced mixer" topology shown in Fig. 8 [13] [15] . The single-balance topology provides double the gain of the single-ended mixer.

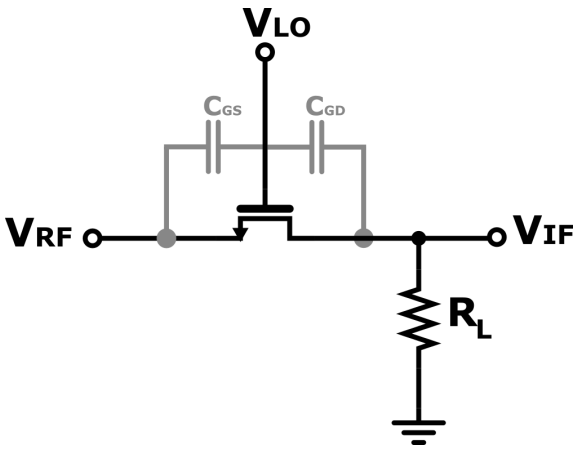


Figure 7: MOS implementation of simple mixer

Both passive and active mixers exist in single-balanced configuration as shown in Fig. 8. However, in modern transceivers single-balanced topology is not commonly used.

The problem with single-balanced mixer is LO leakage that occurs due to capacitances present in the MOSFET. The LO leakage creates LO-to-IF feedthrough which corrupts the desired signal [15]. The solution to the problem is described in the next section.

2.3.2 Double-balanced Mixer Design

To solve the problem of LO-to-IF feedthrough, connect two single-balanced mixers in such a way that alternate outputs of single-ended mixer are tied together, which results in differential output. The topology is called double-balanced because both RF input and LO waveforms are balanced/differential signals. The double-balanced topology eliminates the output LO feedthrough and the output signals remain unaffected. Fig.

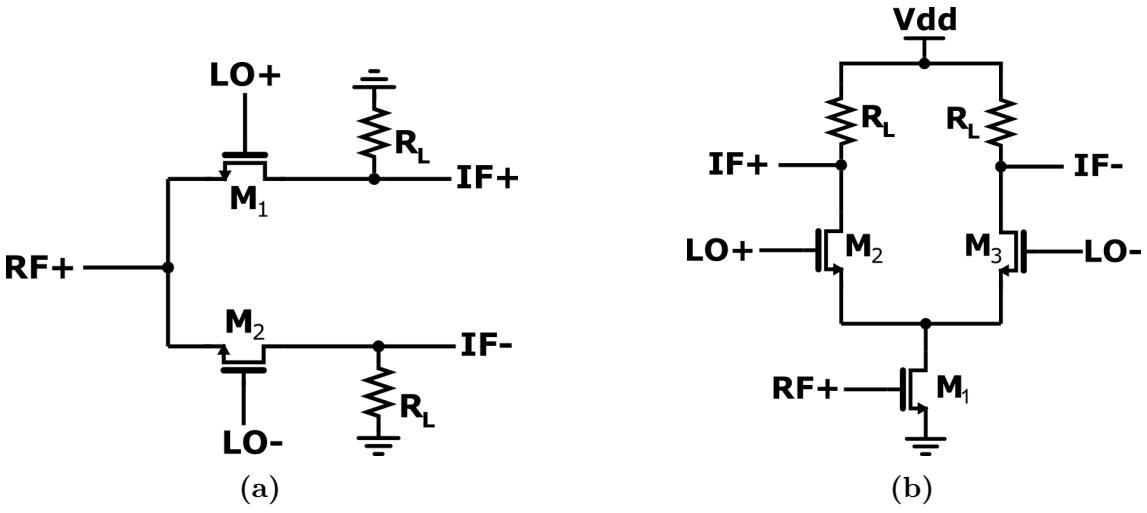


Figure 8: (a) Single-balanced mixer, (b) single-balanced active mixer

9 shows the passive double-balanced mixer and active double-balanced mixer designs. The feedthrough introduced by $LO+$ and $LO-$ are cancel out at the output due to opposite polarity. The conversion gain of double-balanced mixer is half of the single-balanced mixer. In addtion, input noise of single-balanced is less than the double-balanced topology [15] [14].

The subsequent sections discuss the construction, operation and performance of both passive double-balanced and active double-balanced mixers.

2.4 Downconversion Mixer

This thesis focuses on the first downconversion mixer that provides IF with center frequency at 7 GHz when the RF varies from 26.5-29.5 GHz.

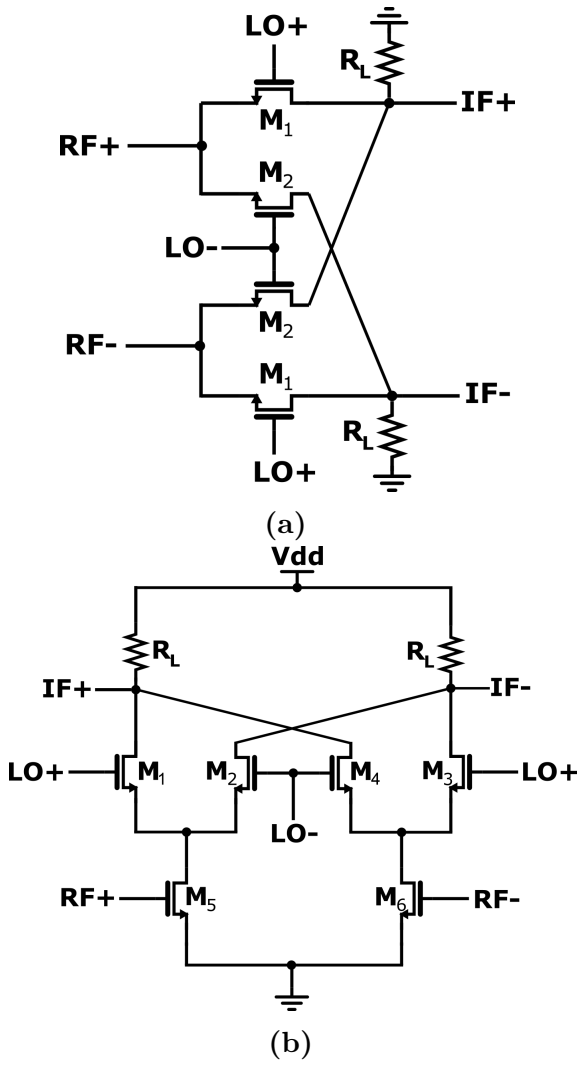


Figure 9: (a) double-balanced passive mixer, (b) double-balanced active mixer

2.5 Passive Downconversion Mixer

Passive mixers are employed where supply voltage is a constraint and high linearity is requirement [19]. In passive mixers, dc current does not flow through the mixing FETs (Field Effect Transistor). Passive mixer can be seen as a "folded" version of active mixer. The passive mixers are classified as: voltage-mode passive mixer and current-mode passive mixer. In voltage-mode, the input and output of the mixer are voltages. To ensure the voltage mode operation, a high input impedance buffer is connected at the output of the mixer, and a high output impedance amplifier typically LNA is employed at the input of the mixer. When input impedance of the buffer following the mixer is very high i.e. $Z_{in(buffer)} \gg R_{SW}$, the mixer exhibits a voltage conversion loss of $2/\pi$ assuming abrupt LO switching, where R_{SW} is the switch resistance. While on the other hand, input and output is current in current-mode passive mixer, a transconductance amplifier is required at the input of the mixer to convert the voltage into current and a transimpedance buffer follows the mixer to convert the output current back to voltage [18]. Fig. 10 and Fig. 11 show the voltage-mode passive mixer and current mode passive mixer, respectively. In the remainder of this section detailed structure of voltage-mode passive mixer and current-mode passive mixer is discussed.

2.5.1 Voltage Mode Passive Downconversion Mixer

A voltage-driven double-balanced passive mixer is shown in Fig. 10. The double-balanced passive mixer operates in voltage-mode driven by the local-oscillator (LO) with 50% duty cycle. To achieve high mixer conversion gain and low noise, abrupt LO switching is required. However, at high operating frequency such as 28 GHz to obtain an IF of 6-7 GHz the LO frequency should be 21-22 GHz. Generation of square-wave local-oscillator waveform at 21-22 GHz to achieve abrupt switching (toggling between 0 to 1) is practically very difficult [15]. Thus, the sinusoidal or quasi-sinusoidal LO waveform is the only suitable choice and possesses the inherent advantage of less harmonics generation.

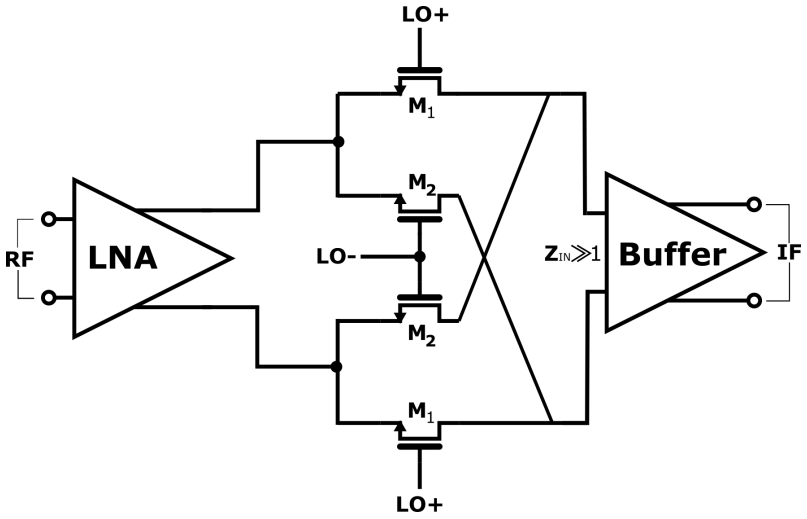


Figure 10: Voltage-mode passive downconversion mixer

The operation of the mixer in Fig. 10 can be understood as: the mixer samples the RF input in one cycle of the LO period that requires 50% of LO signal. The RF input of the mixer is connected to the output (IF) during that period of time and the transistor behaves as a transparent switch. No current flows through the switch. However, the transistors present *on* resistance to the signal that reduces the gain of mixer. For voltage mode passive mixer operation, ideally a voltage buffer with infinite input impedance is considered at the output of the mixer [18]. The passive mixer offers good isolation between I and Q channels because only one path from RF to IF is closed at one time [19]. The term conversion loss is typically used instead of conversion gain due to the fact that the passive mixer does not amplify the signal, so the output is always less than the input [16]. Conversion loss in a double-balanced topology with a square LO waveform is $2/\pi$. The linearity of the mixer depends on the output signal swing and the type of load at the output [19].

2.5.2 Current Mode Passive Downconversion Mixer

The operation of passive mixers is based on *on/off* switches that ideally dissipate no power. However, in practice, passive mixer involve several active components that lead to a non-zero power dissipation. The primary requirement for high performance of passive mixers is abrupt switching to turn *on* and *off* the transistors which act as switches. A current mode passive mixer can be drawn from active mixer as shown in the Fig. 11. The three stages, voltage-to-current (V-I) conversion, current commutation, and current-to-voltage (I-V) conversion are cascaded and decoupling capacitors are placed in the signal path to ensure that the switches are zero dc biased. A common-mode feedback circuit can also be used instead of decoupling capacitors to ensure that the dc levels are equal on both sides of the switches that guarantees no dc flows through the switches. The arrangement of Fig. 11 shows that the voltage is converted to current and commutation happens in the current mode and then the current is converted to voltage again. This arrangement also eliminates the flicker noise that appears in low frequency circuits.

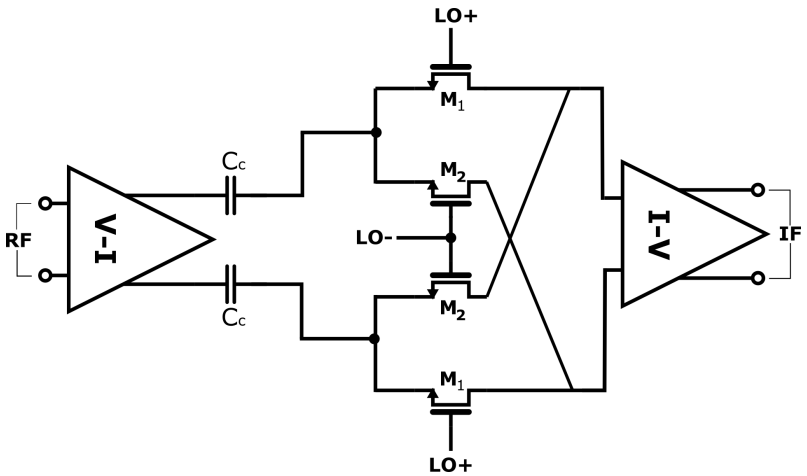


Figure 11: Current-mode passive downconversion mixer

To ensure that the mixer operates in current-mode the input impedance of the stage following the mixer must be very small. Usually a transimpedance amplifier (TIA) is incorporated to convert the current into voltage while presenting very low input impedance to the mixer switches [18].

Conversion Gain The LO waveform has great impact on the conversion gain of passive current-mode mixer. First consider the single-balanced current mode passive mixer with ideal current source (typically LNTA) and ideal TIA preceding and following the mixer, respectively as shown in the Fig. 11. With non-overlapping LO waveforms having 50% duty cycle the output current i_o is equal to the RF current i_{RF} multiplied by the effective LO waveform. So, the current conversion gain of the mixer can be given as

$$A_I = \frac{2}{\pi}\, cos\frac{\omega_{LO}\tau}{2} \tag{9}$$

where $\omega_{LO} = 2\pi/T$ is the LO angular frequency, T is the time period of the LO waveform, and τ is the overlap time of the LO waveforms, which can be positive and negative as shown in Fig. 12.

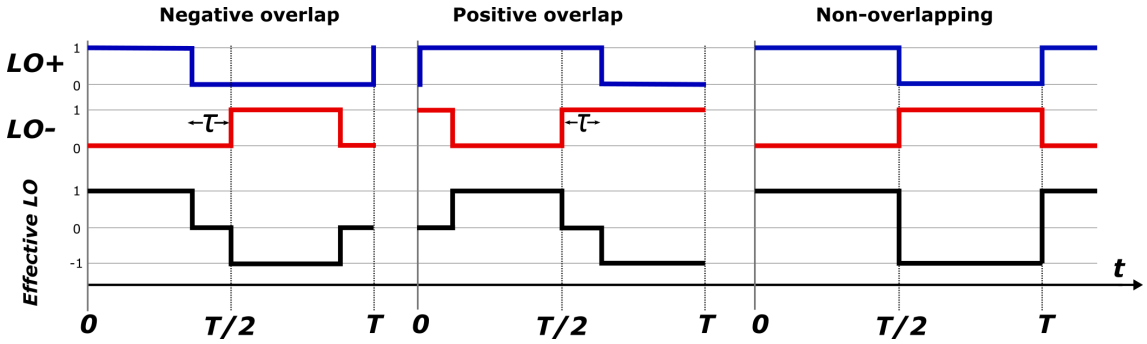


Figure 12: LO waveforms with overlaps

The gain in Eq. 9 is the maximum current conversion gain for 50% duty cycle LO waveform. The duty cycle smaller than or larger than 50% will result in overlap of LO waveforms, thus the RF current either does not appear at all or appeara as common-mode at the output. The conversion gain will be maximum when τ is zero.

For the case of quadrature LO waveform, i.e. LO with 25% duty cycle. With non-overlapping LO waveforms the current conversion gain can be given as

$$A_I = \frac{2\sqrt{2}}{\pi} \tag{10}$$

The 25% duty cycle of non-overlapping LO waveforms improve the conversion gain by 3 dB and consequently the noise figure also improves by 3 dB. However, in practical cases where the LO waveforms are not ideal and suffer from phase error or jitter, which results in overlapping of LO waveforms, the conversion gain is typically less than the ideal current conversion gain. The gain also reduces due to the parasitic capacitance of the transconductor and parasitic capacitance of the switches appear

at the input of the mixer. The parasitic capacitance of the switch arise from the junction or gate-source capacitance. The other disadvantage of overlapping LO waveform is the cross-talk between I and Q channels. It degrades the noise and linearity performance of the mixer.

Noise in Passive Mixers Noise degrades the signal-to-noise ratio and resultantly overall noise figure and sensitivity of the mixer. There are two contributors of noise: 1) flicker noise ($1/f$ noise) and 2) white noise or thermal noise. The flicker noise is important at low frequencies and becomes equal to thermal noise at cut-off frequency. From that point onward only thermal noise contributes to the overall noise.

In general, passive mixers do not suffer from flicker noise because passive mixer only commutates the ac signal currents and dc of the switches is zero. Blocking capacitors are used to isolate the FET switches from the transconductor to stop the flow of dc. However, flicker noise appears at the output, if blocker (undesired signal) is present nearby the signal of interest. In narrowband applications, faraway blockers are removed and mixer will not create any baseband flicker noise, but in wideband systems it appears at the baseband. Flicker noise also appears due to the nonzero rise and fall times of the LO waveforms because all four FETs of mixer core are *on*. Large size transistor lower the output flicker noise as long as their parasitic capacitance do not limit the bandwidth. There are many sources of noise in mixer but all of them are not important and since the band of interest in our design of mixer is 5.5-8.5 GHz which does not affect by flicker noise. Thus, the rest of the discussion is about white noise. Chehrazi *et al* presented a detailed discussion on noise in [20].

White noise is present in all the transistors and resistors. The FET transistors of the switching core cause noise because of their finite resistance. Transconductance stage and the buffer following the mixer also contribute to the white noise, however, in this thesis the focus of discussion is switch noise of the core FETs.

White noise appears at the output either directly or after folding due to frequency translation. The FET in deep triode behaves as a resistor and contributes to the white noise. The resistance of the switch is proportional to the length of channel and increases with increasing the channel length. The noise contribution is only during the overlap time when both switches are *on*. The MOSFET switch white noise depends on the effective voltage of switch and sizing of the MOSFET. The single-sided noise power spectral density (PSD) of the switch can be given as

$$S_{i_n} = \frac{4kT\gamma}{g_{ds}} \tag{11}$$

where k is the Boltzmann constant, T is the temperature, γ is the excess noise factor and g_{ds} is the on conductance of the transistor.

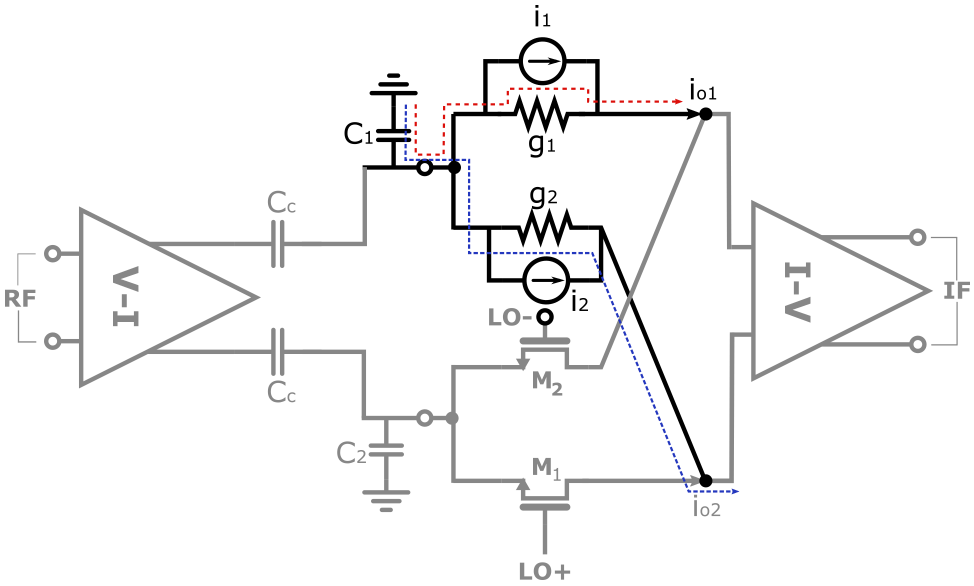


Figure 13: Equivalent circuit for noise during overlap time

The noise power of the double-balanced mixer is twice that of a single-balanced design, so for convenience, the single-balanced mixer is analyzed here. The equivalent circuit can be drawn by replacing the FETs with noise current sources S_{i_1}, S_{i_2} and channel conductances as g_1 and g_2 as shown in Fig. 13. The output differential noise current, $i_{ndiff} = i_{o1} - i_{o2}$. After substituting the values of g_1 and g_2, and, S_{i_1} and S_{i_2}, we get

$$S_{i_{ndiff}} = 2(4kT\gamma)\ \mu C_{ox}\frac{W}{L}\Big(V_{eff} - \frac{V_{LO}^2}{V_{eff}}\Big) \tag{12}$$

where $V_{eff} = V_G - V_B - V_{th}$ is the effective bias voltage of the transistor and V_{LO} is the overlap LO voltage. Another noise source is the parasitic capacitance, C1, shown in Fig. 13 which is discussed by Chehrazi *et al* in [20]. Since the white noise of the switches occur due to overlap (when both transistors are *on*) of LO waveforms that can be reduced by reducing the rise and fall times of the LO waveform.

The noise PSD of a cyclostationary (a random process whose statistics are periodic functions of time) process can be calculated by taking average over a period, for example, from the edges of the overlap time. The PSD of such a cyclostationary noise for the half circuit can be given as

$$S_{i_{no}} = \frac{16(4kT\gamma)}{3S\ *\ T_{LO}}\ \mu C_{ox}\frac{W}{L}V_{eff}^2 \tag{13}$$

where, k is Boltzmann's constant, T is temperature, γ is the excess noise factor of the transistor, S is the slope of LO during the transition, T_{LO} is the time-period of LO waveform, V_{eff} is the effective dc voltage of the transistor switch, and μ, C_{ox}, W and L are the channel mobility, gate oxide capacitance, width and length of the transistor, respectively. Definitely the noise of double-balanced mixer would be twice the half mixer [20]. The overall noise at the differential output of the mixer is dominated by flicker noise at low frequencies and by thermal noise at higher frequencies.

Linearity of Passive Mixers The nonlinearity of passive current commutating CMOS mixers depends on: the rise and fall times of the LO waveform, nonlinear capacitances C_{gs} and C_{gd} of the MOSFET, and the nonlinear relationship between drain current, I_D, and drain-source voltage, V_{DS}. In addition, source impedance Z_S and load impedance Z_L of the mixer also effect the linearity of the passive mixers.

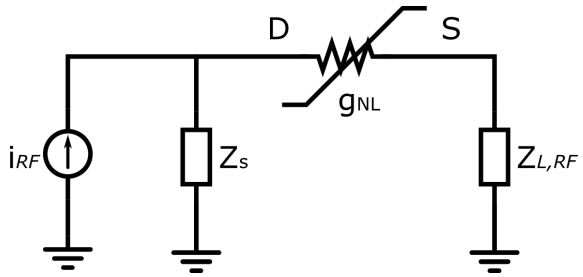


Figure 14: Half circuit equivalent model of a mixer

The source impedance is the output impedance of an ideal LNA and load impedance is the input impedance of an ideal transimpedance amplifier (TIA). MOSFET of the mixer can be modeled as a weakly nonlinear conductance g_{NL} in series with an ideal switch. The half circuit of double-balanced current-mode passive mixer can be modeled as shown in Fig. 14, where i_{rf} is the ideal current source shunted by Z_S source impedance and $Z_{L,RF}$ the load impedance seen at the input of ideal switches. To analyze the linearity of mixer, assume that the LO is an ideal square wave with 50% duty cycle having zero rise and fall times. The large-signal current can be given as

$$\begin{aligned} i_D = {} & g_1 v_D + g_{2_D} v_D^2 + g_{3_D} v_D^3 + ... \\ & - g_1 v_S + g_{2_S} v_S^2 + g_{3_S} v_S^3 + ... \\ & + g_{2_{D\&S}} v_D v_S + g_{3_{2D\&S}} v_D^2 v_S + g_{3_{D\&2S}} v_D v_S^2 + ... \end{aligned} \quad (14)$$

where v_D and v_S are the large-signal drain and source voltages referred to the bulk, respectively. The current i_D is a function of v_D and v_S instead of large signal drain-source voltage v_{DS}. Higher order terms are ignored in Eq. 14. Khatri *et al* calculated the second- and third-order distortion using Voltera series in [21].

It is also shown in [21] that IIP2 and IIP3 are functions of source, Z_S and load, Z_L impedances. In addition, the mixer input impedance depends on input frequency ω_{in} and LO frequency ω_{LO} for capacitive load at the output of the mixer [21]. When $\omega_{in} = \omega_{LO}$, a large reactive impedance appears at the mixer input [22], while on the other hand, when ω_{in} is very small inductive impedance appears at the mixer input. To achieve high IIP2 and IIP3, source impedance $|Z_S(\omega_1 - \omega_2)|$ should be as large as possible, which is typically achieved by placing a blocking capacitor between LNA and mixer [23]. ω_1 and ω_2 are the two tones with equal amplitudes and small frequency difference such that their selectivity/transfer characteristics are same [24]. It is also required that the load impedance of the mixer should be as small as possible to maximize IIP2 and IIP3.

At high LO frequency reactive impedance of gate-source capacitance C_{gs} and gate-drain capacitance C_{gd} approaches switch resistance $1/g_1$ and degrades linearity

due to nonlinear charging and discharging of capacitors [20], [21]. However, if the transit frequency, f_T, of the MOSFET (frequency where the current gain of transistor is equal to unity) is extremely high compared to the operating frequency of the circuit, the effect of C_{gd} and C_{gs} will be small [21].

2.6 Active Downconversion Mixers

Passive mixers are lossy circuits whose conversion gain is theoretically less than zero decibels. Passive mixers also suffer from LO-to-RF feed-through due to lack of isolation between ports [25] and also cause problems such as overloading of baseband amplifier.

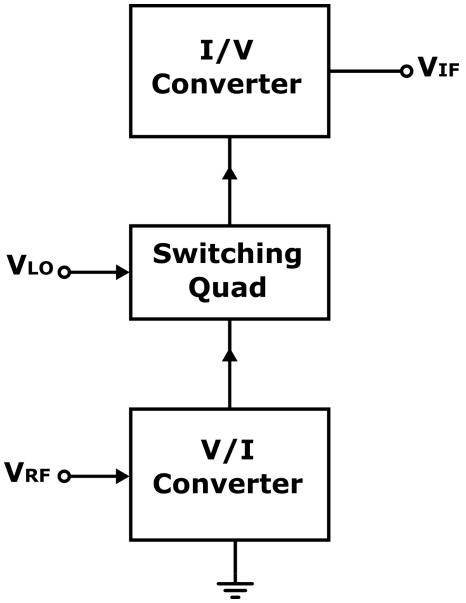


Figure 15: Active mixer operation (transconductance, switching, and transresistance stages)

To solve these problems active mixers are a sound choice. Active mixers provide frequency translation and achieves conversion gain greater than at least 0 dB. In active mixers the conversion gain is achieved in one stage and frequency multiplication is done in the other stage. The operation is described in Fig. 15, where frequency translation stage (switching stage) is preceded by voltage-to-current conversion and followed by current-to-voltage conversion. In other words, the RF input voltage is converted to current, frequency translation happens in the current domain, and then the IF current is converted back to voltage [15].

These mixers provide superior performance because they ideally generate only the desired intermodulation product. double-balanced mixer topology provides high degree of isolation because inputs to the mixer are at separate ports with two transistors in between [16]. Second-order intermodulation products are also reduced because ever-order distortion terms cancelled out [26]. Furthermore, the advantage to use active mixers is that the switching quad does not need rail-to-rail LO swings [15].

This section discusses the active downconversion mixers particularly Gilbert cell mixer, its conversion gain, gain compression, noise performance and linearity.

2.6.1 Gilbert Cell Mixer Topology

Gilbert cell mixer topology is a double-balanced topology, first introduced by B. Gilbert in his article "A Precise Four-Quadrant Multiplier with Subnanosecond Response" in 1968. The nonlinerity of the bipolar transistor is exploited to achieve highly linear systems [27]. The FET version of Gilbert cell mixer can be obtained by replacing the bipolar transistors with MOS field-effect transistors.

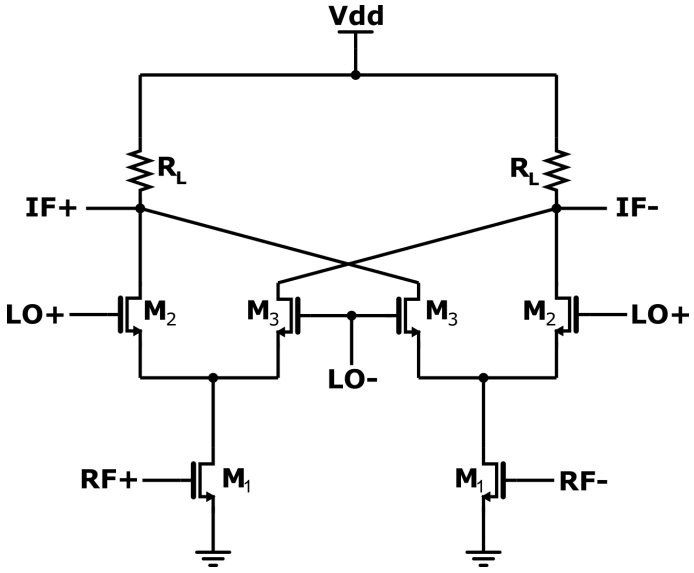


Figure 16: Gilbert cell mixer

The Gilbert cell double-balanced mixer can also be obtained by connecting two single-balanced mixers in such a way that the outputs of the two mixers are cross-coupled as shown in Fig. 16. The input stage of the mixer is differential represented by $RF+$ and $RF-$. The output of the mixer is also differential denoted by $IF+$ and $IF-$. The load resistance R_L in double-balanced topology is half of the single-balanced mixer to keep the same voltage headroom. If the resistor values remain the same as of single-balanced design then the total bias current flowing through each resistor is doubled that leads to decrease in voltage headroom. The double-balanced topology rejects the amplitude noise in the LO waveform which is an advantage over single-balanced mixers [15].

2.6.2 Conversion Gain

The voltage conversion gain of the double-balanced mixer is half of the single-balanced counterpart. We calculate the conversion gain of the single-balanced mixer and deduce the gain of the double-balanced design. Fig. 17 shows a single-balanced mixer with input voltage V_{RF}, complementary LO signals ($LO+$ and $LO-$) and output voltage V_{IF}. With input voltage V_{RF}, the input transistor M_1 produces a drain current I_{RF}

equal to $g_{m1}V_{RF}$. Consider that LO is square wave toggling between 0 and 1, the switching transistors M_2 and M_3 behave as an ideal switch.

Since $LO+$ and $LO-$ are complementary square waves, (i.e. when $LO+$ is 1 $LO-$ will be 0 and vice versa), thus produce a square wave toggling between +1 and -1. The current I_{RF} is multiplied by that square wave and the output voltage V_{IF} can be given as

$$V_{IF} = V_{DD} \ - \ I_1 R_L \ - (V_{DD} \ - \ I_2 R_L) \tag{15}$$

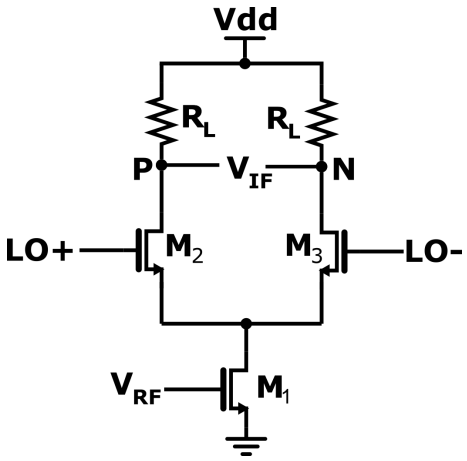


Figure 17: Single-balanced active mixer

The fundamental amplitude of a square wave toggling between +1 and -1 is $4/\pi$ because the peak amplitude of the first harmonic of a square wave is greater than the peak amplitude of the square wave. This results the output as

$$V_{IF} = I_{RF}(t)R_L \ . \ \frac{4}{\pi} \cos \ \omega_{LO}t \ + ... \tag{16}$$

Since $I_{RF}(t) = g_{m1}V_{RF}cos\omega_{RF}t$, thus the output can be written as

$$V_{IF} = \frac{4}{\pi} g_{m1}R_L V_{RF} \ . \ cos\omega_{RF}cos\omega_{LO}t \ + ... \tag{17}$$

where ω_{RF} is the frequency of the input signal and ω_{LO} is the frequency of the LO waveform. The voltage conversion gain of a single-balanced active mixer is equal to

$$\frac{V_{IF}}{V_{RF}} = \frac{2}{\pi} g_{m1}R_L \tag{18}$$

where V_{IF} is the output voltage, V_{RF} is the input voltage, g_{m1} is the transconductance of the transistor M_1 and R_L is the load resistance.

The conversion gain of active mixer trades with linearity and voltage headroom. Since the technology is shrinking and supply voltage scales down with technology, active mixers usability has a down trend. The reduction of supply voltage reduces the voltage headroom for amplifying stage transistor that results the decrease of conversion gain. The linearity of the mixer depends on the overdrive voltage, $V_{GS}-V_{th}$, of the input transistor. Third-order intercept point (IP3) decreases with reduction

in overdrive voltage, $V_{GS1} - V_{th1}$. Thus, the minimum drain to source voltage, $V_{DS1,min} = V_{GS1} - V_{th1}$. The transconductance of M_1, $g_{m1} = 2I_{D1}/(V_{GS1} - V_{th1})$ is limited by the bias current I_{D1} and IP3. The value of R_L is limited the maximum allowable dc voltage accross it. Thus, the conversion gain in Eq. 18 decreases when the supply voltage scales down and linearity requirement increases.

To calculate the maximum voltage conversion gain, we can write load resistance as

$$R_L = \frac{V_{R,max}}{I_{D1}} \tag{19}$$

By substituting the value of g_{m1} and R_L from Eq. 19, the maximum voltage conversion gain is

$$A_{v,max} = \frac{4}{\pi} \frac{V_{R,max}}{V_{GS1} - V_{th1}} \tag{20}$$

where $V_{R,max}$ is the maximum allowable dc voltage across load resistor and $V_{GS1} - V_{th1}$ is the input transistor overdrive voltage. The above equation shows that the conversion gain of active mixers severely limited by the supply voltage.

The conversion gain also depends on the LO swing and decreases if the LO swing is reduced. Since the RF current produced by M_1 splits equally between M_2 and M_3 switching transistors when they are near equilibrium. During that period of time the current appears as a common-mode current, thus reducing the conversion gain.

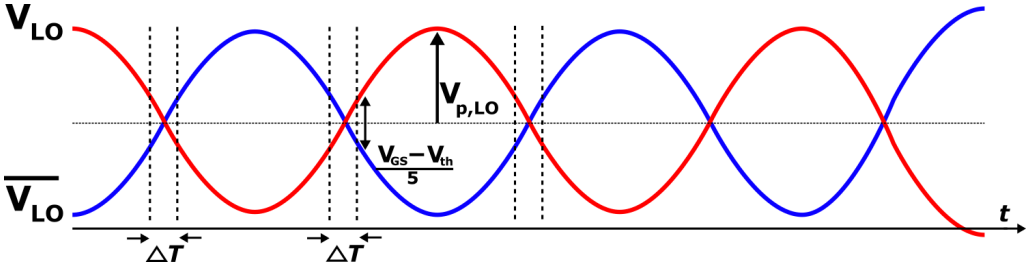


Figure 18: Effect of sinusoidal LO waveform

Effect of Sinusoidal waveform on Conversion Gain The effect of sinusoidal waveform on conversion gain is discussed in [15]. Since, the generation of pure square wave at milli-meter wave frequencies is practically a highly challenging task. Now consider that the LO port is operating at 21 GHz with sinusoidal waveform. The peak amplitude of a single-ended LO waveform is $V_{p,LO}$. Both switching transistors M_2 and M_3 remain on during a period of time, ΔT, when the LO waveforms are crossing each other as shown in Fig. 18, and reduce the conversion gain of the mixer because the output current appears as common-mode. The current of M_1 passes through the differential pair transistors M_2 and M_3. Assuming that the drain currents are equal for a period of time when V_{LO} and $\overline{V_{LO}}$ cross each other in time $\Delta T/2$, where $\Delta T/2$ is

$$\Delta T/2 = \frac{(V_{GS} - V_{th})}{5} \cdot \frac{1}{2V_{p,LO}\omega_{LO}} \tag{21}$$

Multiply by 4 to account for the rising and falling edges and normalizing to LO period, the overall conversion gain becomes

$$A_v = \frac{2}{\pi}\, g_{m1} R_L \Big(1 - \frac{2\Delta T}{T_{LO}}\Big) \tag{22}$$

$$A_v = \frac{2}{\pi}\, g_{m1} R_L \Big(1 - \frac{(V_{GS} - V_{th})}{5\pi V_{p,LO}}\Big) \tag{23}$$

The gain of active mixer also reduced due to total capacitance seen at the drain of the input transistor. Consider the abrupt LO switching, one of the transistors from M_2 and M_3 will remain off during half of the LO cycle. When $LO+$ is high, M_2 is on and M_3 is off and capacitance seen at node X is $C_X = C_{DB1}+C_{GS2}+C_{GS3}+C_{SB2}+C_{SB3}$. Due to the capacitance C_X from node X to ground, the current of M_1 divides between C_X and the resistance seen at the source of M_2. The current division reduces the conversion gain that can be given as

$$A_v = \frac{2}{\pi}\, g_{m1} R_L \Big(1 - \frac{(V_{GS} - V_{th})}{5\pi V_{p,LO}}\Big)\, \frac{g_{m2}}{\sqrt{C_X^2\omega^2 + g_{m2}^2}} \tag{24}$$

where ω is the RF frequency and g_{m2} is the transconductance of the switching transistor M_2 [15].

2.6.3 Noise in Active Mixers

Noise in active mixers is usually higher than their passive counterparts. The overall noise in active mixer contributed from the transconductance or driver stage, the switching quad, and the LO source. Although, the LO source is not part of the active mixer, but it is difficult to analyze the noise of mixer and LO source separately at the output of the mixer. The noise in active mixer arises due to non-zero rise and fall times of the LO waveform (when all transistors of the switching quad are *on* at the same time i.e. during zero crossing) and inherent noise of the transistors.

Since the mixer is not a linear time-invariant circuit, the conventional noise analysis techniques can not be applied to analyze the noise behavior. The noise in the mixer has periodically time-varying statistics because the operating point of transistors changes periodically with time, and the output noise also has periodically time-varying characteristics due to frequency translation. The noise of the mixer is cyclostationary process i.e. a process whose statistics are period functions of time. If the noise of a device with a fixed operating point is white then the noise produced due to time-varying characteristics is also white [28]. The noise calculation can be started with the ideal LO waveform and extended to the real sinusoidal or quasi-square waveform.

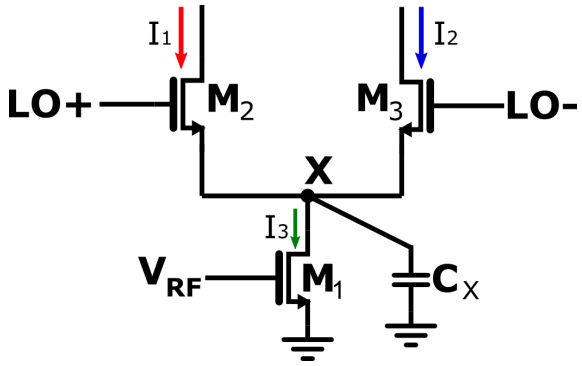


Figure 19: A single-balanced active mixer

Assume that the LO waveform is an ideal square-wave, so the current of the transconductor passes through one of the switching transistor and other transistor remains in the off state. Fig. 19 shows a half circuit that can be analyzed and results can be extended to the double-balanced Gilbert cell mixer. The LO is assumed to has a 50% duty cycle. During first half of the LO period M_2 is *on* and M_3 is *off*. Since, the parasitic capacitance appears at the node X is $C_X = C_{GD1} + C_{DB1} + C_{SB2} + C_{SB3} + C_{GS3}$ due to which M2 contributes some noise and similarly M3 during the next half cycle. The noise of M_2 or M_3 is multiplied by the noise current of M_1 and appears at the output. The total noise at the IF output can be estimated by adding the contribution of each noise source and input-referred noise voltage can be evaluated by dividing the total noise with overall conversion gain of the mixer. The output noise due to M_1 and M_2 at node P is

$$\overline{V_{n,P}^2} = \frac{1}{2}(\overline{I_{n,M1}^2} + \overline{V_{n,M2}^2} C_X^2 \omega^2)\ R_D^2 + 4kTR_L \tag{25}$$

where $\overline{I_{n,M1}^2}$ is current noise of M_1 and $4kTR_L$ is the thermal noise of resistor R_L [15]. It is interesting to note that the output noise of mixer consists of noise contribution from all the sidebands with highest contribution by the fundamental sideband [28]. The PSD of current thermal noise generated by M_1 (in saturation) can be given as

$$\frac{\overline{I_{n,M1}^2}}{\Delta f} = 4kT\gamma g_{m1} \tag{26}$$

where k is Boltzmann's constant, T is the absolute temperature, and g_{m1} is the transconductance of M_1 [28].

The noise of M_3 at node N can be accounted by doubling the noise power calculated in Eq. 25. Afterwards, substitute Eq. 26 and divide the total noise power by square of the conversion gain of the mixer, it results the input-referred noise voltage as

$$\overline{V_{n,in}^2} = \frac{\left(4kT\gamma g_{m1} + \frac{4kT\gamma}{g_{m2}}\ C_X^2\omega^2\right)\ R_L^2 + 8kTR_L}{\frac{4}{\pi^2}\ g_{m1}^2 R_L^2\ \frac{g_{m2}^2}{C_X^2\omega^2 + g_{m2}^2}} \tag{27}$$

where the term in the denominator is the conversion gain of the mixer with abrupt LO switching taken from Eq. 24 by discarding the sinusoidal part. If the parasitic

capacitances are negligible Eq. 27 can be reduced to

$$\overline{V_{n,in}^2} = \pi^2 kT\Big(\frac{\gamma}{g_{m1}} + \frac{2}{g_{m1}^2 R_L}\Big) \tag{28}$$

For a realistic case, when the LO has non-zero rise and fall time, both transistors remain *on* during a part of LO period, ΔT. The switching transistors contribute noise to the output as a differential pair. The transistor M_1 contributes little noise due to the common-mode. The output noise of the differential pair can be given as

$$\overline{V_{n,diff}^2} = 2(4kT\gamma g_{m2|3} R_L^2 + 4kTR_L) \tag{29}$$

where g_{m2} and g_{m3} are the transconductances of the the switching transistors. The input referred noise voltage for the sinusoidal or quasi-square wave can be be obtained by multiplying $\overline{V_{n,diff}^2}$ with $2\Delta T/T_{LO}$ and multiplying numerator of Eq. 27 by $1 - 2\Delta T/T_{LO}$ and finally dividing with conversion gain calculated in Eq. 24.

$$\overline{V_{n,in}^2} = \frac{8kT(\gamma g_{m2|3} R_L^2 + R_L)\frac{2\Delta T}{T_{LO}} + \Big[4kT\gamma\Big(g_{m1} + \frac{C_X^2\omega^2}{g_{m2}}\Big)R_L^2 + 8kTR_L\Big](1 - \frac{2\Delta T}{T_{LO}})}{\frac{4}{\pi^2}\ g_{m1}^2 R_L^2\ \frac{g_{m2}^2}{C_X^2\omega^2 + g_{m2}^2}(1 - \frac{2\Delta T}{T_{LO}})^2} \tag{30}$$

where $2\Delta T/T_{LO}$ is period of time when both transistors are *on* and $1 - 2\Delta T/T_{LO}$ is the time excluding the overlap time that is equal to $(1 - \frac{(V_{GS} - V_{th})}{5\pi V_{p,\,LO}}$. The noise relations are derived in [15] with greater detail.

2.6.4 Linearity and Compression of Active Mixers

The linearity of active mixers has a direct relation with overdrive voltage of the input transistor. The IIP3 increases with rising the overdrive voltage of the input transistor which is in common-source configuration. The switching transistors offer better linearity performance than the input transistor. The noise and non-linearity of active mixer have a direct trade-off because

$$\overline{V_{n,in}} = \frac{4kT\gamma}{2I_D}\ (V_{GS} - V_{th}) \tag{31}$$

It is also important to understand that if the switching transistors enter into the triode region the linearity of the mixer be degraded.

Gain compression is another important parameter that determines the performance of mixers. Generally, input-referred 1-dB compression (P1dB) point is measured by sweeping the input power at a particular IF frequency. The P1dB is a point where the gain of the mixer drops by 1-dB from its maximum value at a given input power. On the contrary, it is also possible that the circuit becomes compressed at the output instead of at the input, if the output swings become very large. In that case, the switching transistors cause non-linearity and results compression while the input transistor has not reached compression [15].

3 Analysis of Primitive Mixers

In this chapter primitive mixers are explored to understand the basic framework behind modern day mixer circuits. It is important to learn the fundamentals of mixer before begin to design of actual circuits. This chapter starts with theory of diode mixer which then allows to build very basic mixer circuits such as single-diode mixer and extended to build modern singly-balanced diode mixer, and doubly-balanced diode mixer. The theory explains the frequency translation process using the small signal equivalent model of diode, where linear, time-varying, small signal conductance and capacitance result the frequency conversion. It is assumed that the local-oscillator voltage only vary the small signal parameters to characterize the devices used in mixer circuits. In addition, performance parameters including conversion gain/loss, port-to-port isolation, noise and noise figure, and other performance limiting mechanisms such as effect of source and load impedance, production of spurious signal tones, and intermodulation products, are discussed to get insight of frequency mixing.

The single-diode mixers are typically used at millimeter-wave frequencies, however, they are fundamental to all mixer designs, such as multiple-diode mixers. It is pertinent to understand the phenomenons occur in single-diode mixer because any balanced mixer can be reduced to a single-diode mixer equivalent by suitable scaling of source and load impedances, the LO levels, and by changing the impedances occur at certain mixing frequencies.

Along with the advantages of single-diode mixer, there are some disadvantages which limit their use. The main difficulty is the injection of LO signal that leads to the balanced mixer designs. The balanced mixer possesses better power-handling abilities and has advantage of rejecting LO noise and spurious signals. The only drawback of balanced mixers is the lower conversion gain.

3.1 Diode Mixer Design

This section deals with diode mixer theory which is, in fact, essential to design a mixer for particular application. To begin with the analysis we make some assumptions. First, the RF signal is always smaller than the LO signal, which is usually the case. Second, the diode mixer is stable under large- and small-signal conditions. A diode-mixer is designed to be sensitive to the operating frequency but it is also sensitive to other frequencies that include the well-known *image* frequency present on opposite side of the LO frequency relative to the RF. It is also sensitive to the undesired LO harmonics exist on both sides of the LO frequency called the sidebands.

When the small-signal voltage is applied to the diode mixer at any one of these frequencies, the currents and voltages are produced in the junction at all frequencies, including sideband frequencies. These frequencies are called the small-signal mixing frequencies and can be written as

$$\omega_n = \omega_0 + n\omega_p \tag{32}$$

where ω_n is the RF frequency, ω_p is the LO frequency, ω_0 is the output or intermediate frequency, and $n = ... -3, -2, -1, 0, 1, 2, 3, ...$. The current or voltage or both exist

in the diode at each mixing frequency without discriminating the excitation frequency. The diode can be short-circuited at one frequency to remove the voltage at that frequency, but current still exists. On the contrary, the current components can be removed by making the diode open-circuit, but the voltage remains.

In theory, infinite number of harmonics and their mixing products exist, but practically n is limited to some maximum number to obtain the results in simulations. The microwave mixers are explained with greater detail in [29].

3.1.1 Large Signal Analysis

Large signal analysis of the diode mixer starts with the equivalent circuit of diode shown in Fig. 20. It consists of a series resistance R_s, a junction capacitance $C(V)$, and a current source $I(V)$. The current source and junction capacitance are functions of junction-voltage.

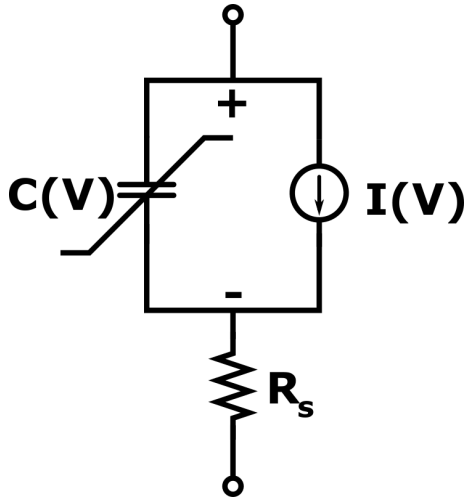


Figure 20: Equivalent circuit of diode

The current-voltage characteristic equation of a diode is

$$I(V) = I_0 \ (e^{\frac{qV}{\eta kT}} \ - 1) \tag{33}$$

where I_0 is the reverse satuation current, q is the charge of electron, η is ideality factor (typically less than 1.25), k is Boltzmann's constant, and T is the absolute temperature.

The small-signal junction conductance is equal to the first derivative of current with respect to the voltage and can be given as

$$g(V) = \frac{d}{dV} I(V) \approx \frac{q}{\eta kT} I(V) \tag{34}$$

and junction capacitance can be given as

$$C(V) = \frac{C_0}{\left(1 - \frac{V}{\phi_{bi}}\right)^{\gamma}} \tag{35}$$

where C_0 is the zero voltage junction capacitance, ϕ_{bi} is the built-in voltage of the junction, and γ is a uniformity factor and has a typical value of 0.5. To avoid any discrepancy between large-signal capacitor current and small-signal capacitor current, it is clarified that the large signal capacitor current is

$$I_c(t) = \frac{dQ_d}{dt} = C(V(t))\frac{d}{dt}V(t) \tag{36}$$

where $C(V) = dQ_d/dV$. The above expression defines the capacitance as an incremental capacitance in large-signal case. However, in small-signal case the capacitance is treated as a linear, time-varying quantity. So

$$C(t) = C(V(t)) \tag{37}$$

and the small-signal current is

$$i_c(t) = \frac{d}{dt}C(t)v(t) = C(t)\frac{d}{dt}v(t) + v(t)\frac{d}{dt}C(t) \tag{38}$$

where $v(t)$ is the small-signal junction voltage. In any type of mixer design, it is always desirous to reduce the LO power, which is typically high at higher frequencies. In linear circuits, LO power requirement is minimum when the source and load are conjugate matched. Since the diode is a nonlinear element, impedance cannot be defined precisely. However, quasi impedance can be defined as

$$Z_d(j\omega_p) = \frac{V_d(\omega_p)}{I_d(\omega_p)} \tag{39}$$

where Z_d is the diode impedance, $V_d(\omega_p)$ is the fundamental frequency voltage and $I_d(\omega_p)$ is the fundamental frequency current. $Z_s(j\omega_p)$ should be equal to $Z_d^*(j\omega_p)$ for optimum transfer of power from LO source to the diode. It also depends on LO level and diode bias. The dissipation of LO power by the diode is given by

$$P_d = \frac{1}{T}\int_0^T V_d(t)I_d(t)dt - V_dcI_dc \tag{40}$$

where $T = 2\pi/\omega_p$. In millimeter-wave mixers the conversion gain performance is limited by the LO drive because rail-to-rail LO waveform is almost impossible to achieve [29].

3.1.2 Small Signal Analysis

Frequency translation happens in a diode mixer due to the time-varying nature of junction-conductance and junction-capacitance. The conductance and capacitance vary with the LO waveform. The conductance comes from the current-voltage characteristic of the diode junction and capacitance forms due to the depletion layer of the junction. Since the conductance of the diode is a highly nonlinear quantity due of exponential dependence of current on voltage. The junction-capacitance does not vary largely, typically by a factor of three to four and the performance of mixer mainly depends on its average value rather than the time-varying value. However, the conductance value vary from nearly short-circuit to open-circuit and plays dominant role in conversion loss and noise figure.

3.2 Balanced Diode Mixers

Single-diode mixers are preferred in millimeter-wave applications because of low LO drive requirement. However, the injection of LO requires a filter diplexer or some similar kind of device which limit their use. The balanced mixers not only solve the problem of LO injection but also possess other capabilities that make them superior. The advantages of balanced mixers include rejection of spurious products and signals and cancellation of LO noise. On the down side, balanced mixer require high LO power to drive more diodes and results in poor conversion gain. The poor conversion gain is due to the embedding network impedances and inability of dc biasing because of anti-parallel configuration of diodes.

Like other mixer topologies discussed in Chapter 2, diode mixer designs are also available in singly-balanced and doubly-balanced structures. The variants of singly-balanced structures are 90-deg hybrid and 180-hybrid structures. The doubly-balanced mixers come in ring and star configuration. The ring diode double-balanced mixer configuration is most commonly used at microwave frequencies. The main difference in balanced-mixers is the design of hybrids, otherwise all mixers have almost the same operation principle. The discussion of hybrids is beyond the scope of this thesis, so the singly-balanced and doubly-balanced configurations of mixers are discussed. It is great to our benefit that all mixers can be reduced to single-diode equivalent circuit.

3.2.1 Singly-balanced Mixers

Both single-balanced designs: 90-deg (quadrature) and 180-deg hybrid use two diodes. The hybrid consists of four ports and all ports are matched which are mutually isolated from each other. In 180^o hybrid the output differs by 0^o or 180^o and in 90^o hybrid the output differs by 90^o. Each diode is connected to a different port as shown in Fig. 21. The point where anode of one diode and cathode of the other diode combines is the IF output of the mixer. The difference in performance of mixers come from: the type of hybrid, matching circuits and/or use of dc bias.

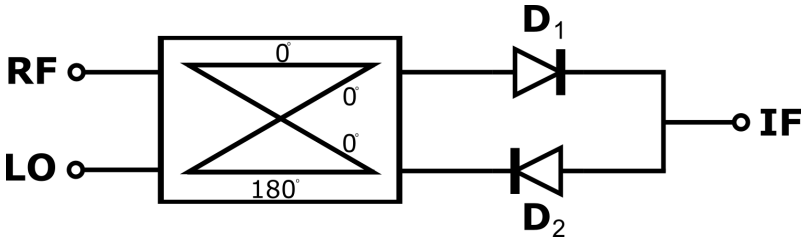


Figure 21: singly-balanced mixer using 180-deg hybrid

The properties of balanced-mixers are: 1) rejection of LO noise and intermodulation products due to RF and LO phases at the diodes that requires specific orientation of diodes. The specific orientation of diodes makes the use of dc bias impossible, however, ways to circumvent this problem exist, 2) AM noise (due to noisy LO sources) rejection necessary in mmW mixers is limited by the balance of the hybrid. If the hybrid is ideal the rejection will be perfect. 3) spurious response

rejection is a great property of balanced mixers, but not all the spurious products can be rejected by the same mixer. It is possible that one mixer can reject the even order but not the odd order.

3.2.2 180-deg Hybrid Mixer

Fig. 21 shows a 180^o hybrid mixer. The LO and RF inputs are applied at different ports of hybrid, so the LO-to-RF isolation is the same as that of the hybrid itself. Conversion loss and noise performance of the mixer can be approximated by I-V characteristics of the diodes. When the LO is applied at the delta port, phase difference of the LO voltage at the two diodes is 180 degrees as shown in Fig. 21. RF input is applied at the sigma port which is in phase at the diodes. The *delta* port represents the difference in voltage at other two ports and *sigma* port represents the sum of input voltages at other two ports namely port 1 and 2. The conductance of the diodes are also in phase because the diodes are connected in anti-parallel configuration. The small-signal current of 180-deg hybrid mixer can be given as

$$i(t) = g(t)\ v(t) \tag{41}$$

where $v(t)$ is the total small-signal voltage across the diode and $g(t)$ is the time-varying conductance of the diode. The current and voltage at the IF are in phase because RF voltage and diode conductances are in phase , thus the currents combined at the IF node. While the LO noise voltages are in phase with the LO voltages

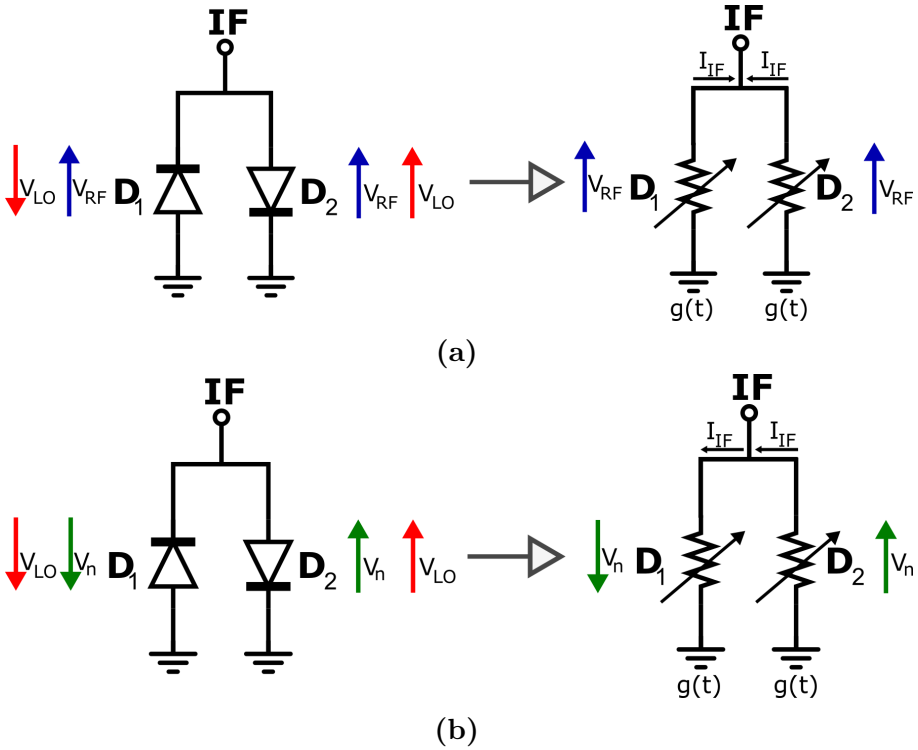


Figure 23: LO and RF phases in singly-balanced mixer: (a) RF and LO phases, (b) AM noise from the LO

and out-of-phase at the diodes, thus in result cancellation of AM noise and spurious signals in the ideal condition as shown in Fig. 23. The voltages across diodes can be written as

$$V_1 = -V_{LO}cos(\omega_p t) \ + V_{RF}cos(\omega_p t) \tag{42}$$

$$V_2 = V_{LO}cos(\omega_p t) \ + V_{RF}cos(\omega_p t) \tag{43}$$

where V_1 and V_2 are the total ac voltages (RF voltage plus LO voltage) across the diodes. The currents after expanding with power series are:

$$I_1 = a_1 V_1 \ + a_2 V_1^2 \ + a_3 V_1^3 + a_4 V_1^4 ... \tag{44}$$

$$I_2 = -a_1 V_2 \ + a_2 V_2^2 \ - a_3 V_2^3 + a_4 V_2^4 ... \tag{45}$$

Negative sign in Eq. 45 shows that the applied voltage is reversed. The current at the IF node can be written as

$$I_{IF} = I_1 \ - I_2 \tag{46}$$

From the above results it can be concluded that all intermodulation products ($f_{IF} = mf_{RF} + nf_{LO}$, where $m, n = 0, \pm 1, \pm 2, ...$) are eliminated when: m and n are even and when m is even and n is odd, but the converse is not true [29].

3.2.3 Doubly-Balanced Ring Diode Mixer

Double-balanced mixers possess the advantages of LO noise cancellation, isolation between all ports, rejection of spurious signals and their intermodulation products. Doubly-balanced diode mixer require higher LO drive due to more number of diodes and their conversion loss is also poorer than the singly-balanced designs. The operation of diode ring mixer is convenient to understand if the diode is considered as a switch driven by the LO waveform. The diode ring mixer consists of two center-tap transformers and four diodes connected in a ring shape as shown in the Fig. 24. Schottky diodes are usually used because of their low *on* resistance and high-frequency response. The LO signal is applied at the primary winding of one transformer and center-tap of the secondary winding is grounded. The RF signal is applied at the primary winding of other transformer and center-tap of secondary winding is used to take the IF output.

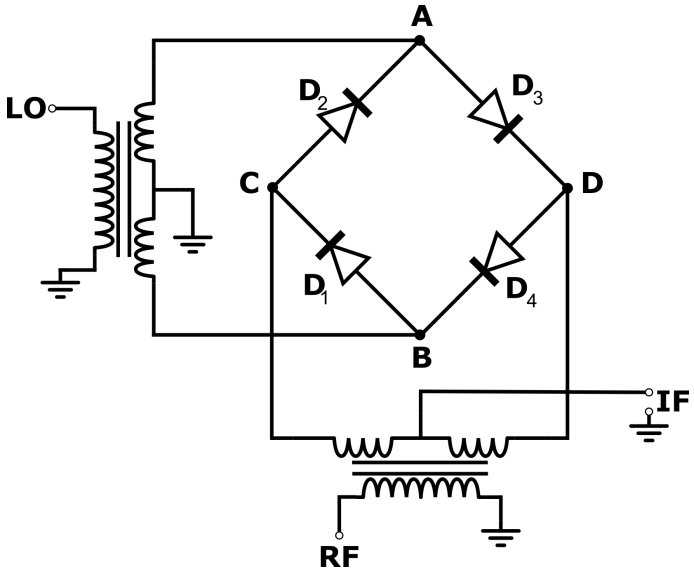


Figure 24: Ring diode mixer

It is better to understand the operation of a center-tapped transformer before getting into the details of ring diode mixer. Fig. 25 shows a center-tapped transformer that has ideal and identical windings and configured such that all the ports are matched. Thus the resistances at ports 3 and 4 are half the ports 1 and 2. When the port 4 is excited the current and voltage appear across each port are: same voltage appear across primary and secondary windings, if the current at port 4 is I then at port 1 and 2 is $I/2$ and zero at port 3 to comply with conservation of power. In practical cases, the center tap is usually grounded, thus there is no current flow. The center-tapped transformer also called transformer hybrid has very wide bandwidth that is limited by the winding capacitance and inductance in high frequency design.

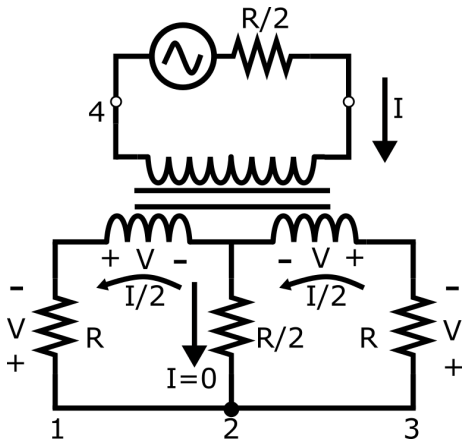


Figure 25: Transformer hybrid

The center-taps of the transformers are virtual ground when the identical load is connected to the two secondaries. Thus, the points where the secondaries are connected to the diodes are also virtual ground. The points A and B are virtual grounds for the LO input, and points C and D are virtual grounds for the RF input.

When the LO signal is applied, say A is positive and B is negative the diode D3 and D4 conducts and other two diodes are reverse biased, thus become open-circuit. Since it is assumed that the diodes are switches, so the junction and series resistance of the diodes can be ignored. Node B is connected to the node C and D which are RF virtual ground points, thus the node B is also grounded. The secondary S_{RF1} is connected to the IF node that gives the IF output. In the next half of the LO cycle the diode D1 and D2 conducts and node A is connected to the C and D node and becomes ground. At this moment of time, the secondary S_{RF2} is connected to the IF output.

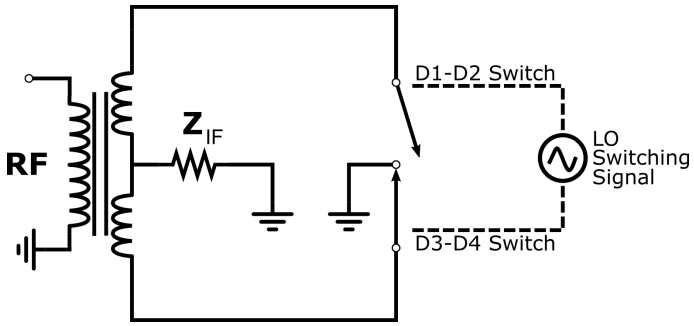


Figure 26: Equivalent circuit of ring diode mixer

The equivalent circuit of diode ring mixer is shown in Fig. 26. The polarity of RF voltage appeared at the IF output changes periodically with the LO frequency. This results the frequency conversion through the multiplication of RF signal and LO waveform [29] [30].

The conversion gain of diode ring mixer can be calculated by assuming that the input signal is $Asin\omega_{RF}t$ and the output is tuned to $|\omega_{RF} - \omega_{LO}|$, the output of the mixer will be

$$\frac{2}{\pi}Acos(\omega_{RF} - \omega LO) \tag{47}$$

Thus, the conversion gain of the mixer is $2/\pi$. The CG is less than one, however, is independent of the LO amplitude, unless it is turning the diodes on and off properly [18].

The drawback of using diode mixer is that they require: special type of hybrid structures, high LO signal power that results in increased leakage of LO signal to the IF port, and diode mixers contain transformers that require a large area, which limits their use in modern RF integrated circuits.

4 Design Description

To compare the performance of different design topologies of downconversion mixer, the circuits have been implemented in Global Foundries (GF) 22 nm fully-depleted silicon-on-insulator (FDSOI) design kit with minimum gate length of 20 nm. All the mixer designs have been generated using flipwell (nMOS on n-well and pMOS on p-well) super-low voltage threshold FETs (slvtfet) having supply voltage equal to 0.8 V. The structure of FDSOI MOSFET is different than the conventional MOSFETs. Fig. 27 shows the structure of FDSOI FET. The FDSOI technology has several advantages over SOI and bulk transistor technologies such as lower leakage of carriers, less variation across the chip due to lower doping effort, and capability of body biasing required in specific circuits. In addition, threshold voltage of the FET can be manipulated through biasing at the back-gate contact and source/drain are insulated from the well which avoids the source/drain-well junction. The MOS capacitors are preferably used because of their compact size and small required capacitance (in the range of 100s of femto farads).

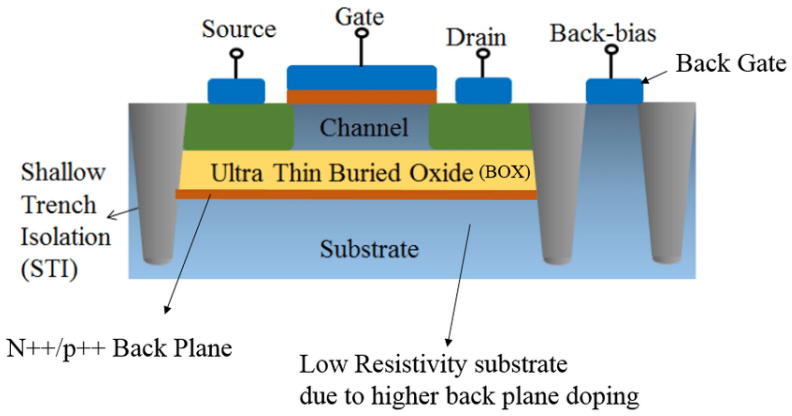


Figure 27: FDSOI MOSFET structure [31]

The designs implemented in GF FDSOI technology are: transformer input mixer, Gilbert cell mixer, modified Gilbert cell with resistive degeneration and modified Gilbert cell with inductive degeneration. This chapter discusses the structure of downconversion mixers, pre-layout simulation results, physical layout design, and post-layout simulation results. The results are compared and analyzed to choose a suitable mixer for 28 GHz frequency applications.

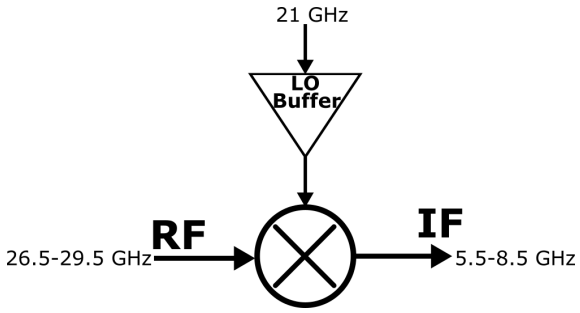


Figure 28: Block-level diagram of mixer

The results in all mixer topologies are obtained by sweeping the RF frequency from 26.5 to 29.5 GHz while keeping the LO frequency constant at 21 GHz as shown in Fig. 28. The schematic of the LO buffer is shown in Fig. 29. The differential LO buffer circuit is constructed by cascading two inverters in each chain. The resistor R_f is the feedback resistance used to bias the drains of the inverter transistors, controls the gain and enhances the bandwidth of the inverter, the resistor R_m is used for impedance matching, and $C1 - C2$ are the dc blocking capacitors also used for matching purposes. The inverter circuit consists of an nMOS (15 μm/24 nm) and a pMOS (30 μm/24 nm) with 20 fingers of 0.75 μm and 20 fingers of 1.5 μm, respectively. The pre-layout and post-layout waveforms at the output of the mixer are shown in Fig. 34.

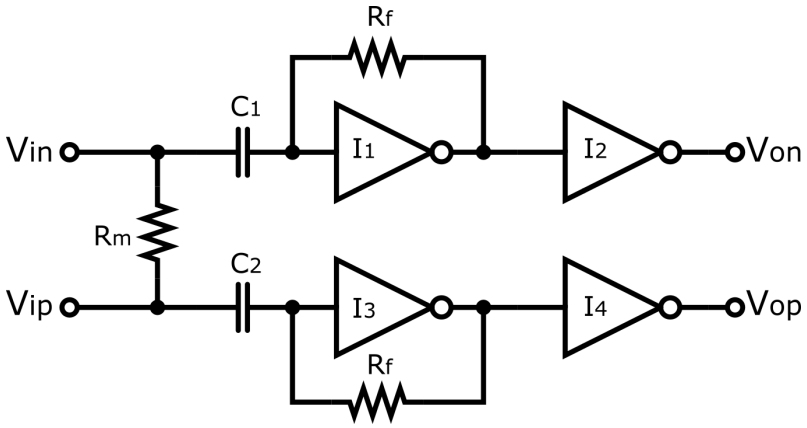


Figure 29: Schematic diagram of LO buffer

4.1 Mixer with tranformer input

The transformer input mixer comprised of a center-tapped transformer, two pairs of switching transistors for double-balanced output and two load resistors. Fig. 30 shows the schematic design of transformer input downconversion mixer. The primary winding of the transformer is connected to the RF input voltage and two secondaries are connected to each pair of switching transistors. The center-tap of the transformer is grounded that stops the current to flow in a loop and provides the ground path to the sources of FETs. The switching pair transistors provide the required frequency translation by multiplication of input signal with LO waveform. The LO signal is applied at the gates of switching transistors to switch the transistors at LO frequency. The applied LO has a 50% duty cycle i.e. when $LO+$ is high $LO-$ is low and vice versa. During a period of time when the $LO+$ is high, the transistor $M1$ and $M3$ conduct and pass the RF signal to the IF output. Similarly during the period when $LO-$ is high, the transistor $M2$ and $M4$ conduct and pass the RF signal to the IF output. This structure gives the differential output at the IF port. The next stage following the mixer is modelled with capacitors not shown in the diagram. In direct downconversion the stage following the mixer is usually an amplifier that offers the capacitive load. However, in superheterodyne structure the IF frequency is further down converted by a second stage mixer to the baseband frequency, where the

baseband amplifier amplify the signal and then the digital processing is performed. The second stage mixer can be active or a passive mixer. If the second stage mixer is active mixer, i.e. Gilbert cell or modified Gilbert cell mixer, the IF signal would be the input of transconductance stage and capacitively load the IF stage mixer. In case the passive mixer is employed the IF signal is connected to the source or drain terminal of the mixing FETs. Since the transistors of passive mixer are transparent when they are *on* and offer ideally infinite resistance when *off*, thus the stage following the second stage mixer would be the load of IF stage mixer. However, usually an amplifier is employed between the first stage and the second stage mixer whose load is capacitive in nature.

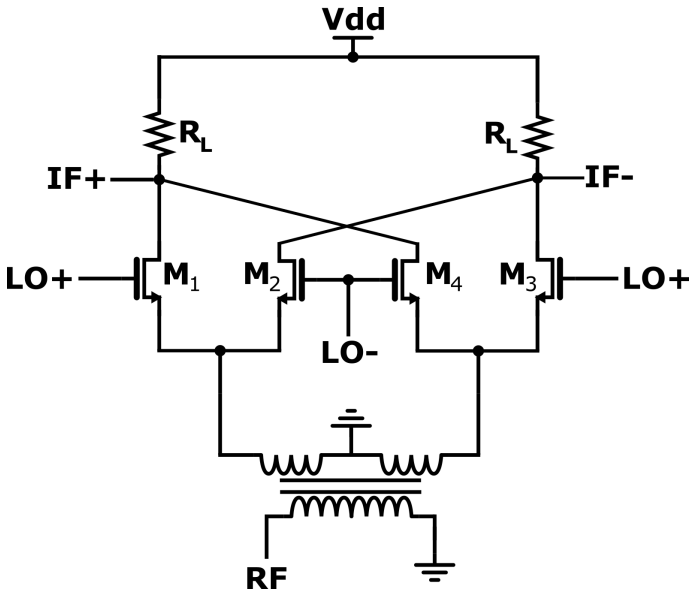


Figure 30: Transformer input mixer

A monolithic transformer is a passive component that does not produce noise and the noise introduced by the input RF signal cancels out due to the differential system. The transformer also increases the isolation between RF and LO ports so that LO signal may not leak through the RF port to the antenna. The transformer also offers wide bandwidth because the bandwidth is limited by the capacitance and inductance of the transformer windings made up of metal layer strip lines. Monolithic transformers operate on the same principle of mutual inductance between two or more conductors as the conventional transformer does. The mutual coupling between the conductors or windings is determined by the k-factor as

$$k_m = \frac{M}{\sqrt{L_p L_s}} \tag{48}$$

where M is the mutual inductance between the primary and secondary windings, L_p and L_s are the self-inductance of the primary and secondary windings, respectively. The voltage and current transformation is related by turns ratio as

$$n = \frac{v_s}{v_p} = \frac{i_p}{i_s} = \sqrt{\frac{L_s}{L_p}} \tag{49}$$

where i_p, v_p, i_s and v_s are the primary current, primary voltage, secondary current and secondary voltage, respectively. It is also interesting to note that the bandwidth increases and Q-factor improves when the transformer is excited deferentially rather than grounding the one port and applying signal at the other i.e. single-ended excitation. It happens due to the parasitic resistance and capacitance which are half in the differential excitation than the single ended excitation [32].

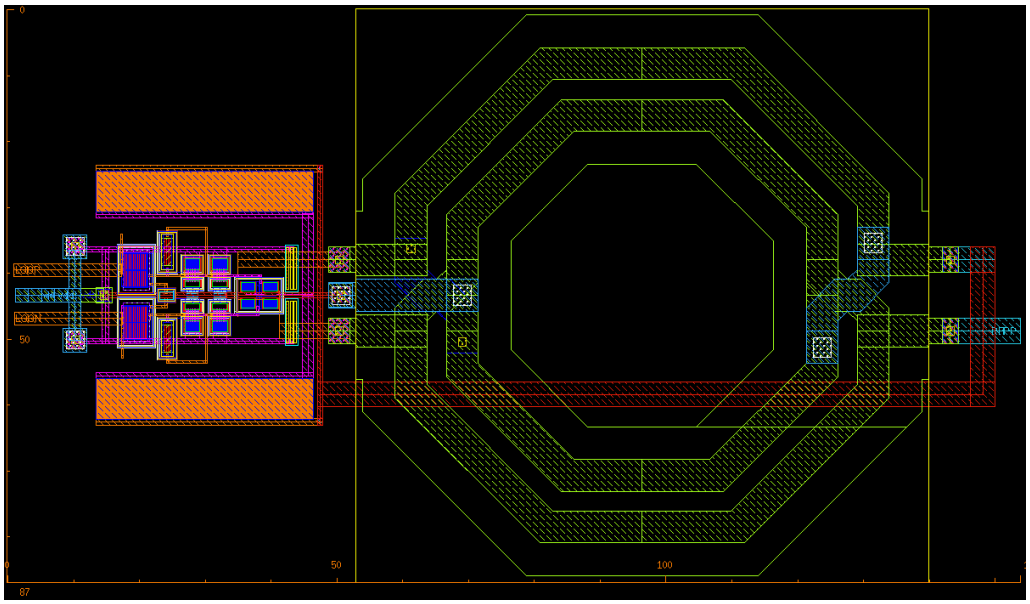
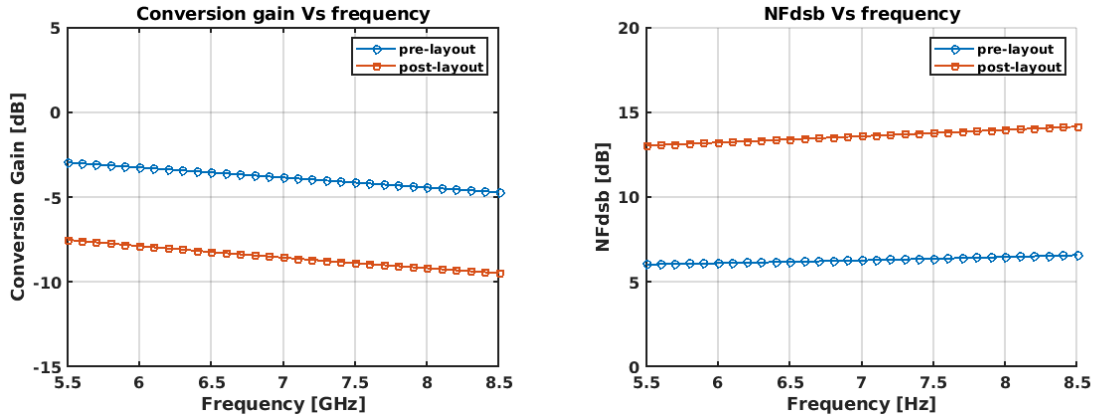


Figure 31: Layout of transformer input mixer

The layout of the LO buffer, switching quad, and center-tapped transformer is shown in Fig. 31. The total area of the mixer including LO buffer and transformer is 0.014 mm^2. The circuit has been simulated using Cadence SPECTRE RF simulator. Fig. 32a shows the simulated conversion gain versus IF frequency of the mixer optimized after varying the width of the transistors. It has been found that transistors



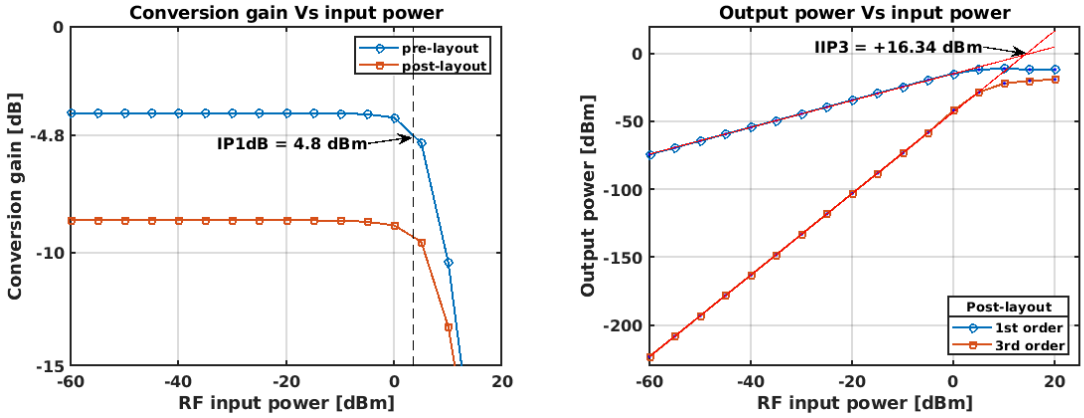
(a) (b)

Figure 32: (a) Voltage conversion gain versus IF frequency, (b) Noise figure versus IF frequency

with wider width have better conversion gain but further increase in width does not change the gain significantly. The transistors with 22.5 μm width having 18 fingers and 24 nm length are used in the design. The lines with circles and squares show the pre-layout and post-layout simulation results, respectively. The conversion gain at center frequency (7 GHz) is -3.8 dB and -8.5 dB for pre-layout and post-layout simulations, respectively. Since the mixer shown in Fig. 30 does not has an amplifying stage, the gain of mixer is equal to the amplitude of the fundamental harmonic minus the losses occur due to transformer coupling and parasitics. In post-layout simulation the gain decreased by 4.7 dB due to the parasitics of the layout and the coupling loss of the transformer. In addition, the amplitude of the LO waveform decreased and rise and fall times increased in post-layout simulation which increased the common-mode output and decreases the overall gain of the mixer. The common-mode output occur when both transistors of the switching pair are *on*, in turn waste the input signal.

The transformer input reduces the noise and improves the linearity of the mixer when compared with the Gilbert cell mixer whose transconductance stage contributes more noise. The double sideband noise figure (NFdsb) plotted in Fig. 32b which is 6.2 dB and 13.6 dB for pre-layout and post-layout simulations at center frequency of 7 GHz, respectively. The switching quad transistors $M_1 - M_4$ and load resistors are the main contributors of noise but the noise in the post-layout simulation accrued from the noise of transformer windings, noise of transistors because of their finite *on* resistance, load resistors, and noise due to the parasitic effects. The noise of the mixer also increases due to the overlap time (when both transistors of switching pair are on) and reduced LO swing. It is expected that the signal loss due to mutual coupling of the transformer also resulted in higher noise figure.

Fig. 33a illustrates the CG versus RF input power that estimates the IIP3 value of the mixer which is typically 10 dB higher than the 1-dB compression point. The linearity of the mixer is limited by the switching quad and linearity of the switching quad depends on the LO drive available at the gates of switching transistors $M1 - M4$. Fig. 34 shows the pre-layout and post-layout LO waveforms



(a) (b)

Figure 33: (a) Conversion gain versus input power sweep, (b) Output power versus input power sweep

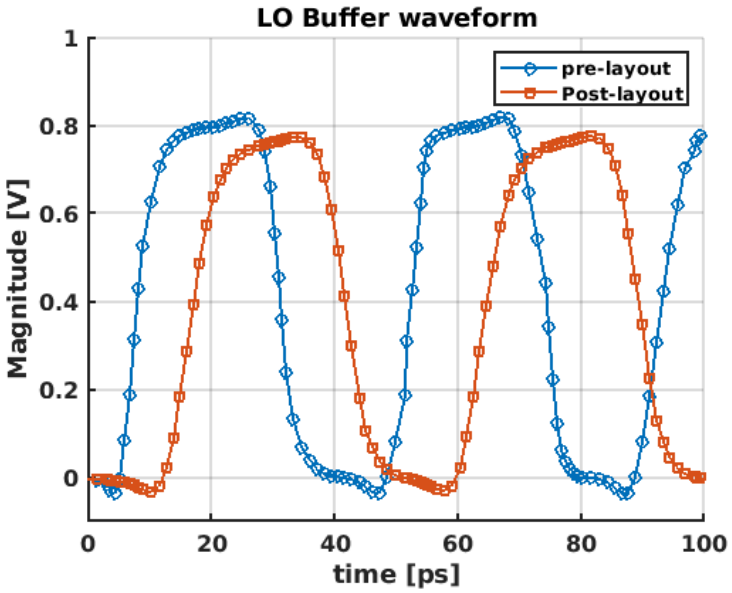


Figure 34: LO buffer output waveform

with 50% duty cycle used to drive the mixer. The LO drive is limited by the supply voltage of the technology used i.e. 0.8 V. In addition, linearity of the mixer depends on the nonlinear capacitances C_{gd} and C_{gs} of the MOSFET, and source and load impedances. The source and load impedance of the mixer is optimized as 50 Ω. The reactive impedance of C_{gd} and C_{gs} is very high compared to the on resistance of the FETs, so the capacitances do not degrade the linearity of the mixer. The IIP3 simulation preformed with two tones and with frequency 28 GHz ± 0.3 GHz is shown in Fig. 33b. The IIP3 value shows good agreement with the value estimated in Fig. 31. The linearity of the transformer input mixer is significantly high with input third order intermodulation point (IIP3) at +16 dBm.

4.2 Gilbert Cell Mixer

The Gilbert cell mixer can be obtained by replacing the transformer with the differential pair transistors in the transformer input mixer of Section 4.1. Now the RF input signal is connected deferentially between bottom transistors as shown in Fig. 35. The operation of the Gilbert cell mixer is explained in Section 2.6.1. The complementary LO signals $LO+$ and $LO-$ are applied at the gates of the switching quad MOSFETs. The drains of switching quad transistors are cross-coupled and connected to the supply through load resistors R_L. The differential IF output is obtained from the drains of the cross-coupled transistors.

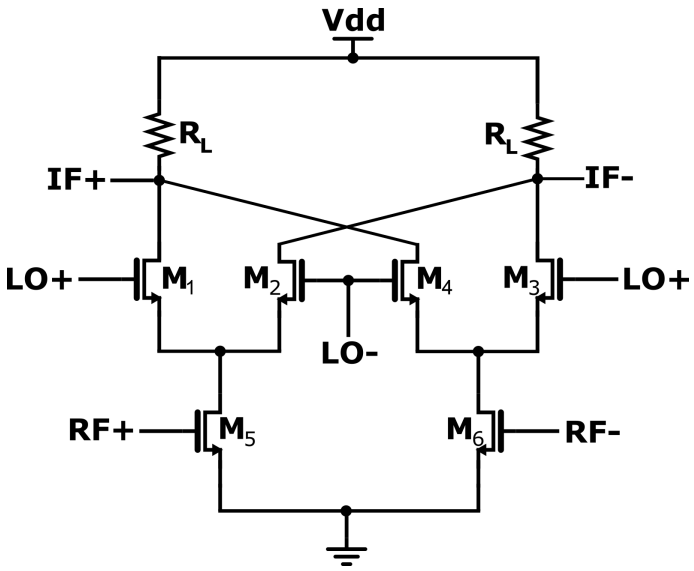


Figure 35: Gilbert cell mixer

The layout of the Gilbert cell mixer is drawn in GF 22 nm FDSOI technology and shown in Fig. 36. The width of input (bottom) transistors is 27.5 μm with 22 fingers and switching quad transistors are 22.5 μm wide with 18 fingers, and the length of all transistors is 24 nm. The resistance of load resistors R_L is 145 Ω optimized to satisfy the headroom requirement of transconductance stage transistors. The input transistors are biased at 320 mV dc and power of the input signal is -30 dBm. Total area of the mixer including the wiring interconnects, LO buffer circuit and resistors used to model the next stage is 882 μm^2, and total power consumption is 5.6 mW from 0.8 V supply.

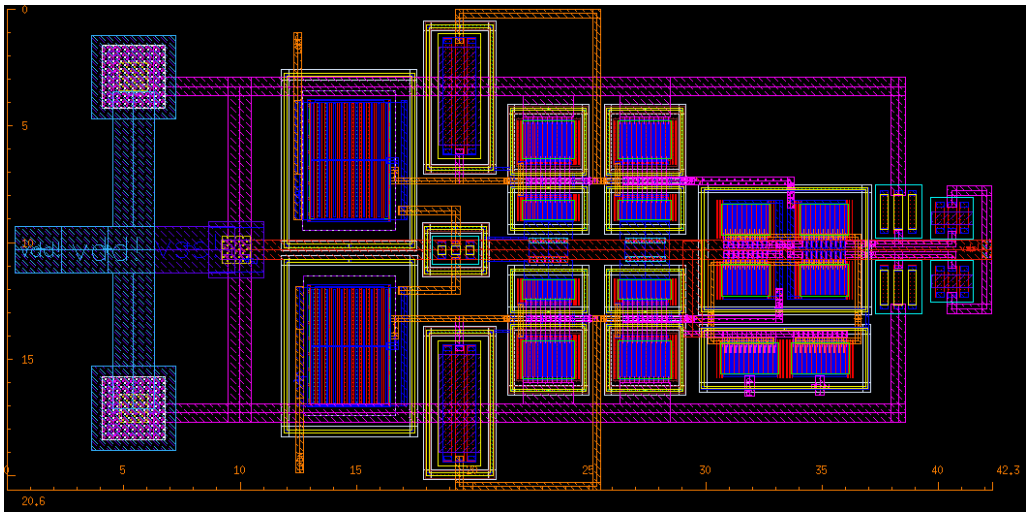


Figure 36: Layout of Gilbert cell mixer

The pre-layout and post-layout conversion gain and noise figure versus IF frequency are plotted in Fig. 37. The conversion gain of Gilbert cell mixer is usually high and primarily depends on g_m of the input transistor and value of the load resistor. In addition, it depends on the LO swing, shape of the local-oscillator waveform,

and the parasitic capacitance appears at a node where drain of input transistor and sources of switching transistors combined. The CG is 13.3 dB and 7.4 dB at 7 GHz IF for pre-layout and post-layout simulations. The decrease of conversion gain in post-layout simulation is due to the reduced LO swing, increase in rise and fall times of the LO waveform, increase of load resistance R_L and impedance of the next stage. The conversion gain versus load resistance at 7 GHz IF frequency is plotted in Fig. 38. The conversion gain increases with the increase of resistance and peaked at 200 Ω with a smaller peak at 500 Ω and then decreases monotonically.

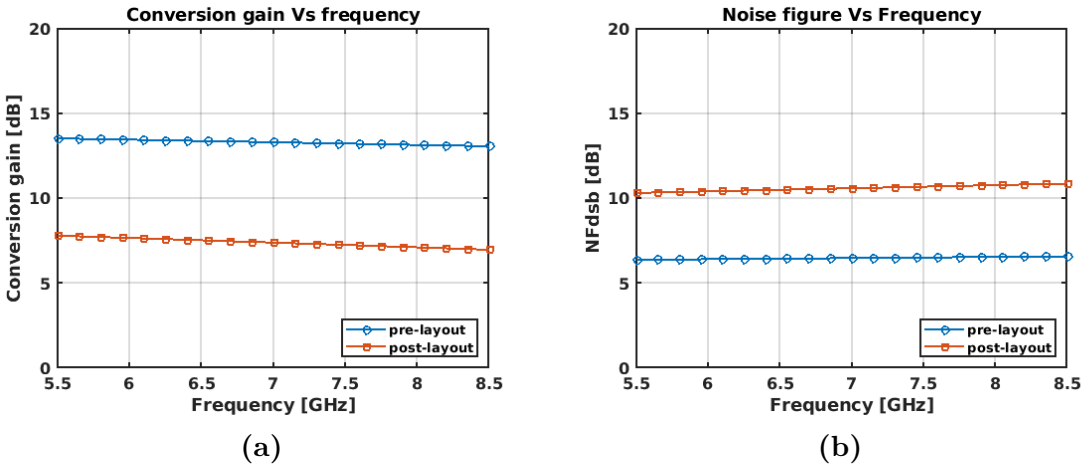


Figure 37: Gilbert cell mixer, (a) Voltage conversion gain versus IF frequency, (b) Noise figure versus IF frequency

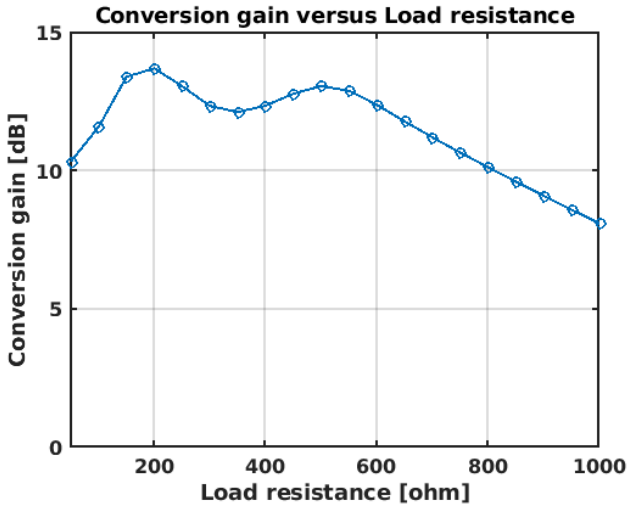


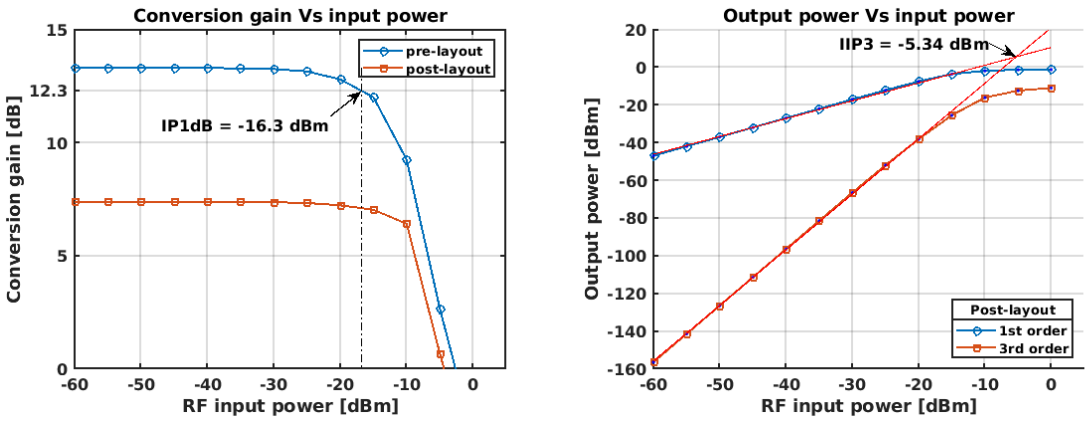
Figure 38: Conversion gain versus load resistance

The decrease of CG is also due to the reduction in voltage headroom and subsequently g_m of the input transistor. Fig. 39 shows the conversion gain versus input power sweep and IIP3 plots. Generally, the conversion gain and IP3 of mixer are proportional to the square root of input stage bias current. The linearity of

Gilbert cell mixer depends on the input transistor's overdrive voltage $V_{GS} - V_{th}$. The input transistors are biased at 320 mV to optimize the linearity of the mixer while compromising the conversion gain that can potentially be 20 dB. The IIP3 of the mixer is -5.34 dBm and 1-dB compression point occur at -13.78 dBm at 28 GHz RF frequency. The IIP3 obtained using two tone simulation with 28 GHz RF input frequency and 28.3 GHz in-band blocker frequency.

4.3 Modified Gilbert Cell Mixer with Resistive Degeneration

The linearity of Gilbert cell mixer can be improved by degenerating the sources of input transistors with resistors. This configuration forms a feedback circuit and controls the current through the input transistor that enhances the linearity of the mixer at the cost of reduced conversion gain and higher noise figure. Fig. 40 shows the circuit of modified Gilbert cell with resistive degeneration. The switching quad is similar to the Gilbert cell mixer of Section 4.2. The common-source transconductance stage ($M5$ and $M6$) is modified by adding source-degeneration resistors ($R1$ and $R2$). The size of switching quad transistors ($M1 - M4$) is 22.5 μm with 18 fingers and transconductance stage transistors ($M5$ and $M6$) are 27.5 μm with 22 fingers. All transistors have identical length of 24 nm. The resistance of degenerating resistors ($R1$ and $R2$) is 153 Ω, and those of load resistors R_L is 290 Ω. The strange resistance value 153 Ω come from N+ polysilicon silicided having 360 nm stripe length and 1.6 μm width. The load resistance value 290Ω is optimized for conversion gain and linearity of the mixer. The input transistors ($M5$ and $M6$) are biased at 400 mV. The resistors $R1$ and $R2$ controls the current flow through the transistors $M5$ and $M6$, thus enhances the linearity of the transconductance stage, which subsequently increases the linearity of the overall mixer.



(a) (b)

Figure 39: Gilbert cell mixer (a) Conversion gain versus input power sweep, (b) Output power versus input power sweep

The layout of the modified Gilbert cell mixer with resistive degeneration is shown in Fig. 41. The layout shown in Section 4.2 has been modified by adding the polysilicon resistors at the sources of $M5$ and $M6$.

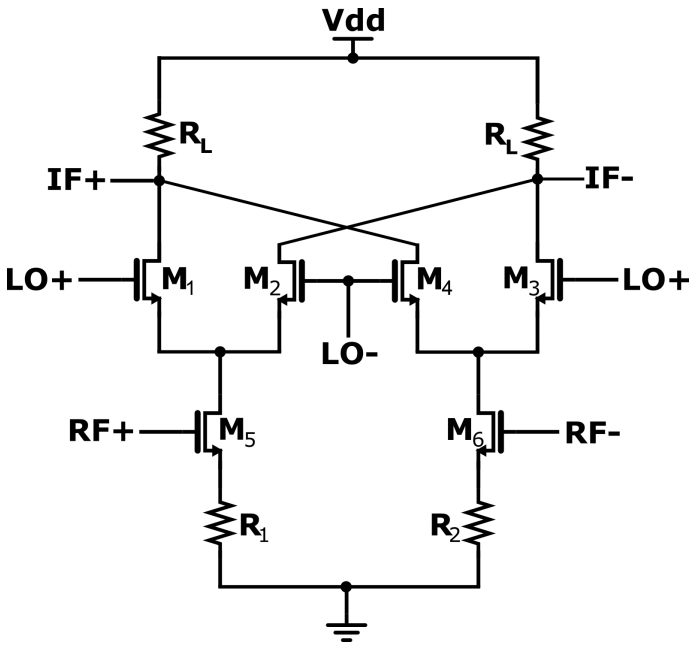


Figure 40: Modified Gilbert cell mixer with resistive degeneration

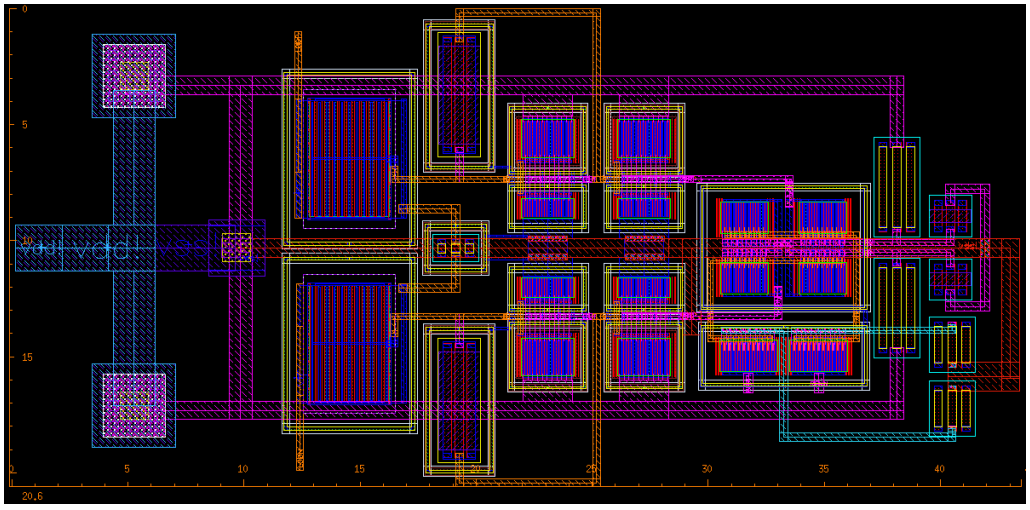
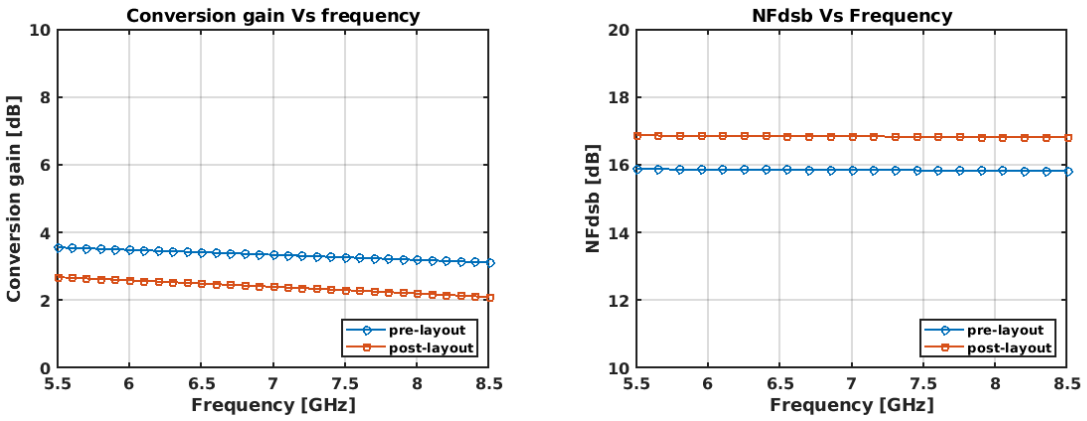


Figure 41: Layout of modified Gilbert cell mixer with resistive degeneration

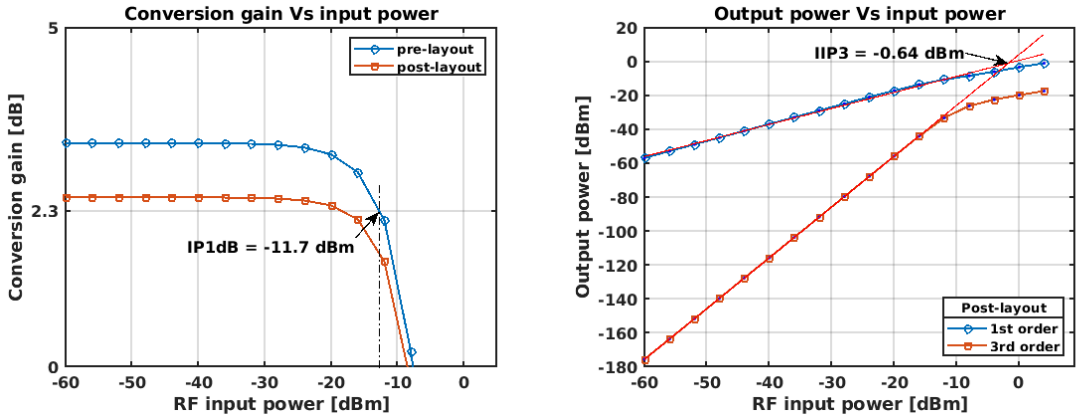
In the process of linearity enhancement the conversion of the mixer degraded because $R1$ and $R2$ limit the $g_{m5|6}$ of the input transistors. The CG and NFdsb versus IF frequency are plotted in Fig. 42. The conversion gain and noise figure shows good agreement in pre- and post-layout simulations. The conversion gain slightly decreased from 3.4 dB to 2.4 dB at 7 GHz IF, while on the other hand the noise figure slightly increased from 15.85 dB to 16.85 dB. The overall noise figure of the mixer with resistive degeneration is quite high because of the noise contribution



(a) (b)

Figure 42: Modified Gilbert cell with resistive degeneration, (a) Voltage conversion gain versus IF frequency, (b) Noise figure versus IF frequency

of $R1$ and $R2$, and increased noise of load resistors due to increase in their size. However, linearity of the mixer is improved significantly with IIP3 at -0.64 dBm as shown in the Fig. 48, which is 5 dB higher than the Gilbert cell mixer. The 1-dB compression point of the mixer can be estimated from the conversion gain versus input power plot that is -9.78 dBm.



(a) (b)

Figure 43: Modified Gilbert cell with resistive degeneration, (a) Conversion gain versus input power sweep, (b) Output power versus input power sweep

4.4 Modified Gilbert Cell Mixer with Inductive Degeneration

The linearity of the mixer becomes more important at higher frequencies such as 28 GHz because the linearity of the mixer can limit the linearity of the whole receiver. The linearity of the switching quad is typically higher than the transconductance stage.

So the transconductance stage of the active mixer usually determines the overall linearity of the mixer. Therefore, it is important to linearize the transconductance stage to improve the overall linearity of the downconversion mixer. The linearity of the transconductance stage can also be improved by source-degeneration with inductors that can be implemented on chip as well [8].

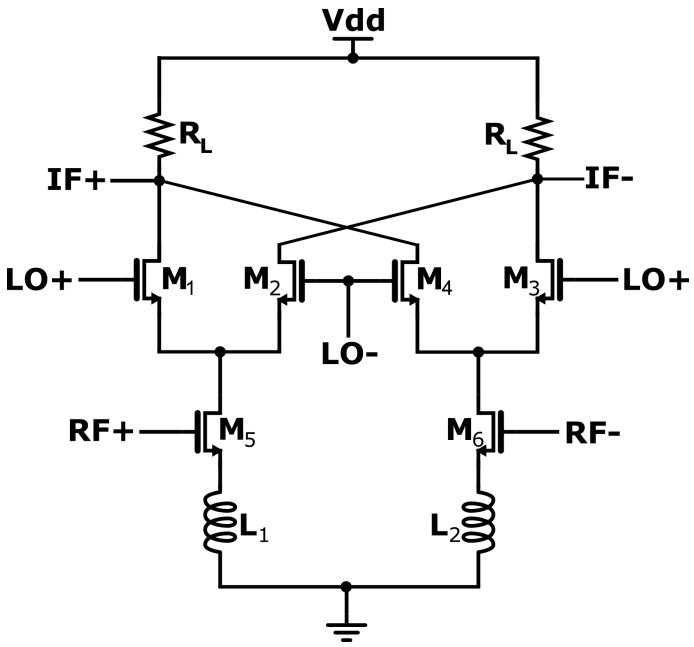


Figure 44: Modified Gilbert cell mixer with inductive degeneration

The schematic of the modified Gilbert cell mixer is shown in Fig. 44. The mixer consists of a switching quad, a transconductance stage, and degeneration inductors. A differential RF signal is applied at the gates of the transconductance stage transistors $M5$ and $M6$. Since the Gilbert cell consists of two symmetric singly-balanced mixers, so the devices used in singly-balanced mixer are identical. The sources of $M5$ and $M6$ are connected with inductors $L1$ and $L2$ that cause source degeneration. The transistors $M5$ and $M6$ of the transconductance stage are 27.5 μm with 22 fingers and 24 nm channel length. The size of switching quad transistors is 22.5 μm with 18 fingers and 24 nm length. The input transistors are biased at saturated region. The degeneration inductors are 2 nH which enhance the linearity of the transconductance stage. The switching core transistors $M1 - M4$ are 22.5 μm with 18 fingers and no biasing applied because the amplitude of the LO buffer wave form is just below the supply voltage i.e. 0.8 V. The LO waveform is quasi-square wave shape and provides semi-abrupt switching. The duty cycle of the LO waveform is 50%. The supply 0.8 V is connected to the load resistors which are connected to the drains of cross-coupled transistors $M1 - M4$. Total area of the mixer is 0.027 mm^2 and total power consumption is 6.0 mW from a 0.8 V supply.

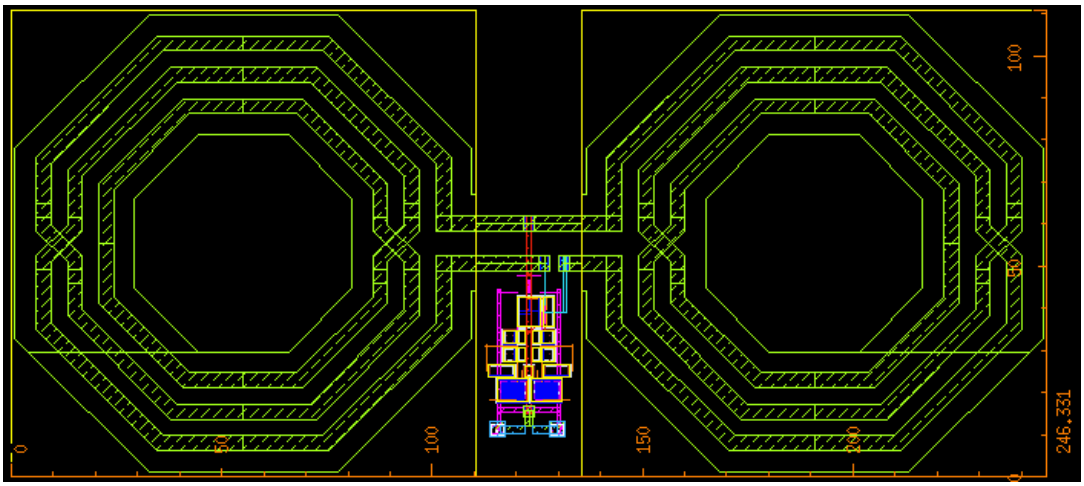


Figure 45: Layout of modified Gilbert cell mixer with inductive degeneration

Fig. 45 shows the layout of the modified Gilbert cell mixer with inductive degeneration. The layout of the mixer is drawn using the inductors calibrated by the foundry. The inductors are optimized for maximum Q-factor and minimum resistance. The inductance, Q-factor and resistance of the inductor at 28 GHz frequency is shown in Fig. 46. The two inductors are drawn on each side of the mixer circuit to make the symmetric design.

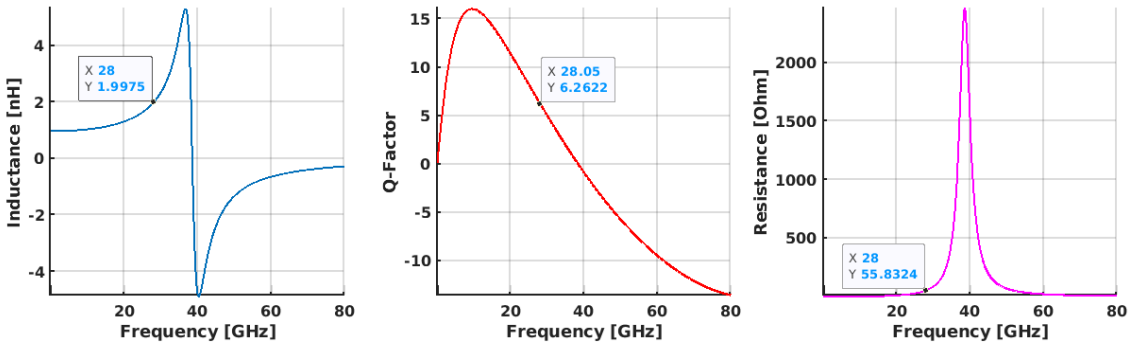
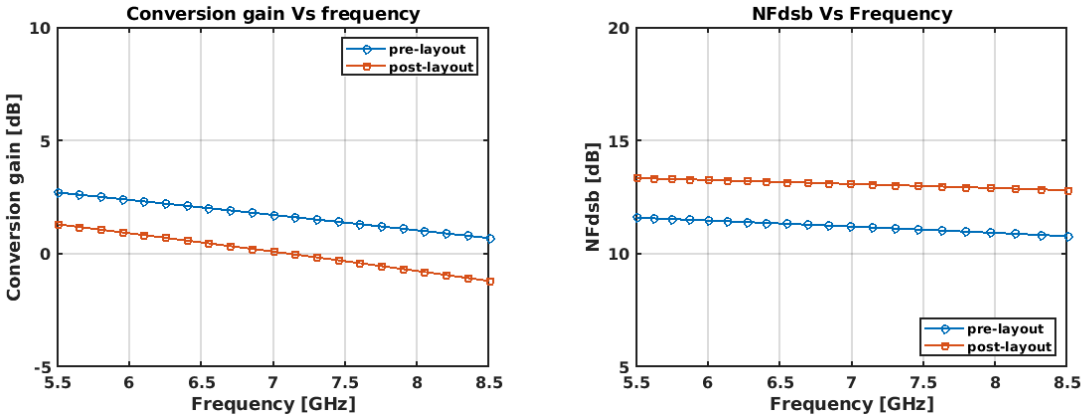


Figure 46: Characteristics of inductor

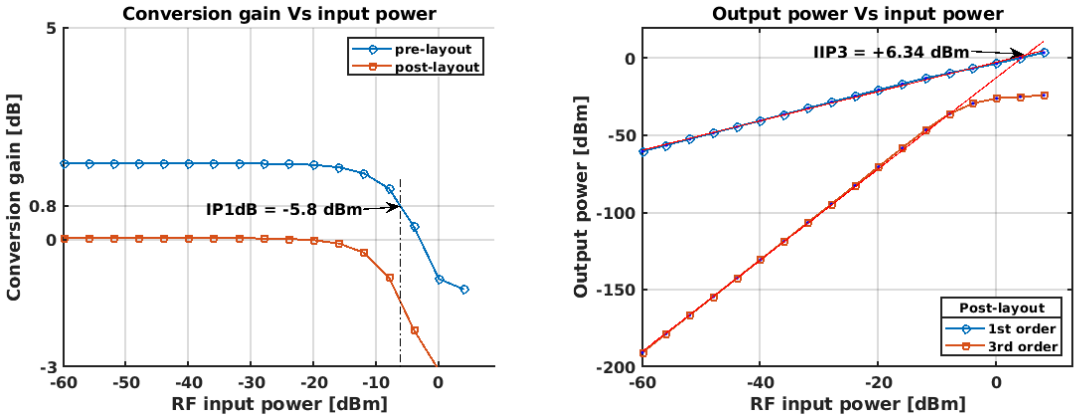
The source degeneration inductors enhance the linearity of the transconductance stage while sacrificing the conversion gain. However, the noise figure of the mixer does not increase significantly due to inductive source degeneration. The CG at center frequency is 1.72 dB and 0.1 dB for pre- and post-layout simulations, respectively. Due to the bandwidth limit of the inductor the CG dropped by 2 dB from 5.5 GHz to 8.5 GHz. The noise figure increased significantly relative to the reduction in conversion gain because of the noise contribution of inductor parasitics in the post-layout simulation.

Inductive source-degeneration enhanced the linearity of the mixer significantly as compared to the resistive source-degeneration. The IIP3 occur at 6.34 dBm which is 7 dB higher than resistive source-degeneration mixer and approximately 13 dB higher than Gilbert cell mixer.



(a) (b)

Figure 47: Modified Gilbert cell with inductive degeneration, (a) Voltage conversion gain versus IF frequency, (b) Noise figure versus IF frequency



(a) (b)

Figure 48: Modified Gilbert cell with inductive degeneration, (a) Conversion gain versus input power sweep, (b) Output power versus input power sweep

4.5 Performance Comparison

The performance of mixer topologies is compared in Table 1. All circuits are implemented in GF 22 nm process node with maximum supply voltage of 0.8 V. The RF frequency is swept from 26.5 - 29.5 GHz to obtain an intermediate frequency of 5.5 - 8.5 GHz with a center frequency at 7 GHz. The table clearly shows that the conversion gain decreases from left to right and IIP3 and IP1dB increases from left to right that indicates the trade off between conversion gain and linearity. In addition, there is also a trade off between CG and dc power consumption because the power consumption decreases with the decrease of CG.

Since, the noise figure is affected by physical resistances and parasitic resistances. The noise figure of resistively degenerated mixer is highest of all due to the noise contribution of resistors used for degeneration. In modified Gilbert cell with inductive degeneration NF increased due to the parasitic resistance of the inductors and for very similar reasons the NF of transformer input mixer is also high. The Gilbert cell shows minimum noise figure because the noise is only contributed by the MOSFETs and load resistors, while the effect of parasitic resistances is smaller than other mixer topologies.

Table 1: Performance comparison of mixer topologies

Topology / Parameter	Gilbert Cell	Modified Gilbert cell with resistive degeneration	Modified Gilbert cell with inductive degeneration	Transformer Input
Process(nm)	22	22	22	22
Supply(V)	0.8	0.8	0.8	0.8
Frequency (GHz) RF/IF	26.5 - 29.5 / 5.5 - 8.5	26.5 - 29.5 / 5.5 - 8.5	26.5 - 29.5 / 5.5 - 8.5	26.5 - 29.5 / 5.5 - 8.5
CG (dB)	7.4 ± 0.5	2.4 ± 0.3	0.1 ± 1.0	-8.5 ± 1.0
NFdsb (dB)	10.6	16.8	12.8	13.7
IIP3 (dBm)	-5.3	-0.6	6.3	16.3
IP1dB (dBm)	-13.9	-9.2	-3.3	6.6
LO-IF (dB)	-38.6	-37.9	-38.0	-61.1
Area (mm^2)	0.0008	0.0008	0.027	0.013
dc Power (mW)	8.0	5.5	6.0	5.7

It is clearly visible that the area of the mixer with highest linearity is also large but smaller than the inductive degeneration mixer because the on chip tranformer can be fabricated by stacking different metal layers on top of each other. However, the Gilbert cell mixer surrounds the smallest area. It must be noted that the area of the LO buffer is also included in the total area of mixer. It reveals that there is also a trade off between area, linearity and conversion gain.

5 Conclusion

This thesis has implemented and simulated integrated mixers for downconversion of NR FR2 n257 (26.5−29.5 GHz) band to 7 GHz IF, and performance was measured to choose appropriate mixer topology for use in the 5G radio transceiver front end. The downconversion mixer would be used in a modular receiver that operates in radar mode for the n257 band and as a conventional receiver for 6-7 GHz radio frequency. The conventional receiver also act as a second downconversion stage during radar mode operation. The circuits were implemented in GF FDSOI 22 nm process technology. The mixer topologies that include Gilbert cell mixer, modified Gilbert cell mixer with resistive and inductive degeneration, and mixer with transformer input are optimized for high linearity. Other performance parameters were determined and improved by varying the size of transistors and bias voltage of transconductance stage.

Pre-layout and post-layout simulations were performed to find the performance parameters, such as conversion gain, noise figure, IIP3, IP1dB, LO-to-IF feedthrough and dc power consumption. The Gilbert cell mixer consisting of a transconductance stage, switching quad, and load stage showed good voltage conversion gain and low noise figure. However, the linearity performance was poor and dc power consumption was high. The linearity was improved by modifying the Gilbert cell with resistive and inductive degeneration at the cost of reduced conversion gain and increased noise figure. The degeneration of sources of the transconductance stage transistors with resistors and inductors improved the IIP3 by 5 dB and 11 dB, respectively. The highest linearity (IIP3 = +16.3 dBm) was achieved when the transconductance stage was replaced with a center-tapped transformer, which resulted in a mixer with transformer input. The conversion gain and NFdsb of transformer input mixer was -8.5 dB and 13.7 dB, respectively for post-layout simulation. The dc power consumption of the mixer including LO buffer was 5.7 mW. However, the area of the mixer was large due to the on-chip transformer.

The results of post-layout simulations were tabulated and compared with respect to conversion gain, IIP3, IP1dB, noise figure, and power consumption. It has been concluded that mixer topologies have trade-offs mainly between conversion gain, linearity, area and power consumption. Thus, the choice of mixer depends upon the requirements of the system where it would be used. In addition, it has been found that the parasitic effects degrade the performance of mixers at high frequency. The performance of active mixers was also limited by the supply voltage, i.e. 0.8 V for 22 nm super low threshold voltage (SLVT) device, which reduces with the shrinkage of technology. Compared with other downconversion mixers [33],[34] in millimeter wave frequency range, the transformer input mixer showed better linearity and consumes less dc power.

With the advancement in 5G radio communication and autonomous automotive industry, higher frequency bands will become increasingly important. In future, the performance of the mixers can be improved by modifying the layout design to reduce the parasitic resistances and capacitances and performing EM simulations to account for the parasitic inductances.

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