Ultra-Low-Power Wake-up Clock Design for SoC Applications

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ABSTRACT OF THE
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This thesis studies how to design an ultra-low-power wake-up clock circuit for SoC applications that essentially consists of a resistor based reference circuit, switched-capacitor branch, an ultra-low-power amplifier, a VCO and a non-overlapping clock phase generator circuit. The circuit is designed in 180-nm CMOS technology using CAD software for circuit design, layout design, pre and post-layout simulations. At first, a brief study of different clock-generation circuit architectures is made, wherein their merits and de-merits are discussed. This is followed by a study of an ultra-low-power amplifier, ring-oscillator-based VCO, non-overlapping clock circuits, the bias generation circuit and the current reference circuit. Additionally, a reference current chopping technique that further improves temperature stability is also described. Later, the report discusses the design and simulations of the actual implementation. Analysis of the design with regards to power consumption, temperature stability and layout area are carried out. The circuit operates at 8.254kHz consuming 70.4nW with a temperature stability of 7.35ppm/°C in the temperature range of -40°C to 75°C. The final layout takes an area of 0.153mm^2. The final design is analysed for its functionality at various process, voltage and temperature corners. Future improvements in the current design are also discussed at the end of this report.

Keywords: ultra-low-power, clock design, wake-up timer, low temperature coefficient, frequency locked loop

Preface

I would like to start the Preface by thanking Al-Mighty Allah for all his blessings and particularly the blessing of pursuing a Master's Degree through writing a Master's Thesis. I am grateful to my parents Jameela Ashraf and Ashraf Kanakkacherry who were always there to offer a helping hand through out my thesis.

This thesis was carried out from March 2018 to August 2018 and my experience and passion towards low-power design led me to choose this topic as my thesis. This work received funding from "Towards Digital Paradise" project granted by Business Finland. I am most grateful to Prof. Kari Halonen, my thesis supervisor, who gave me the chance to do this thesis in the Department of Electronics and Nanoengineering at Aalto University, Finland. I would also like to extend my thanks to Jarno Salomaa who guided me during the period. This preface would be incomplete if I concluded without extending my thanks to my colleagues Mika Pulkkinen, Tuomas Haapala and Mohammad Mehdi Moayer. I would like to express my sincere gratitude to them for their assistance.

Otaniemi, 29.09.2019

Jaisal Ashraf

Contents

Symbols and abbreviations

Symbols

A_V	Voltage gain of the amplifier
BW	Bandwidth
C	Capacitor
C_{OUT}	Output capacitance
C_{ox}	Transistor gate oxide capacitance density
C_{SW}	Switched capacitor
E	Energy
G	Gain
g_m	Transconductance
g_{ds}	Channel conductance
f	Frequency
F_{OUT}	Output frequency
$F_{OUT.MAX}$	Maximum output frequency
$F_{OUT.MIN}$	Minimum output frequency
I	Current
I_D	Drain current
I_{EFF}	Effective current
I_{leak}	Leakage current
I_{REF}	Reference current
K_{VCO}	VCO gain
L	Length of the transistor
LC	Inductor-Capacitor
N	Number of VCO stages
L_n, L_p	Length of the NMOS transistor, Length of the PMOS transistor
P	Power
R	Resistor
RD	Relative difference
R_{eq}	Equivalent resistance
R_{NTC}	Negative temperature coefficient resistor
R_{off}	Off-resistance of the transistor
R_{on}	On-resistance of the transistor
R_{OUT}	Output resistance of the amplifier
R_{PTC}	Positive temperature coefficient resistor
TC_R	Temperature coefficient of resistor
TR	Temperature range
t_d	Propagation delay
V	Voltage
V_{DD}	Supply voltage
V_{gs}	Transistor gate to source voltage
V_{MAX}, V_{MIN}	Maximum voltage, Minimum voltage
V_{ov}	Overdrive voltage
V_T	Thermal voltage
V_{TH}	Transistor threshold voltage
W	Width of the transistor
W_n, W_p	Width of the NMOS transistor, Width of the PMOS transistor
μ	Charge carrier mobility

Abbreviations

AC	Alternating Current
CFI	Constant Frequency Injection
CI	Chirp Injection
CMOS	Complementary Metal-Oxide-Semiconductor
DC	Direct Current
DFI	Dithered Frequency Injection
FLL	Frequency Locked Loop
FoM	Figure of Merit
GBW	Gain-Bandwidth Product
HVT	High Threshold Voltage
IC	Integrated Circuit
IoT	Internet of Things
IP	Intellectual Property
MEMS	Micro-Electro-Mechanical Systems
NMOS	N-type Metal-Oxide-Semiconductor
NOC	Non-Overlapping Clock
NTC	Negative Temperature Coefficient
OTA	Operational Transconductance Amplifier
PTC	Positive Temperature Coefficient
PLL	Phase Locked Loop
PMOS	P-type Metal-Oxide-Semiconductor
PPM	Parts Per Million
PTI	Precise-Timed Injection
PVT	Process Voltage Temperature
RBM	Resistorless Beta Multiplier
RF	Radio Frequency
RFLO	Resistive Frequency Locked Oscillator
SoC	System-on-Chip
TC	Temperature Coefficient
THD	Total Harmonic Distortion
ULP	Ultra-Low-Power
VCO	Voltage Controlled Oscillator
VCRO	Voltage Controlled Ring Oscillator
5G	Fifth-Generation

1 Introduction

System on Chip (SoC) consists of different building blocks which perform various functions. These functional blocks can be either digital circuits or analog circuits. As far as sequential digital circuits are concerned, they cannot function without a clock signal. The major part of the SoC functional blocks are digital blocks which require a clock signal which are provided by circuits called clock generators. In the era of Internet of Things (IoT), SoCs are widely used in IoT applications such as energy-harvesting circuits, sensor-based applications etc. One of the requirements of such SoCs is that the circuitry must be kept in ON-state for a long time. For instance, an event-based application circuit will have to keep sensing node ON all the time to ensure that the circuit will not miss out occurrence of any event, meaning that the clock associated with the sensing node will also have to be kept in ON-state all the time. The clock that is generally used for such an application is the main clock or system clock that works at a high frequency range in the order of MHz or even GHz. This makes the clock distribution network to consume an ample amount of power. This is because the power consumption increases with increased frequency of operation. In fact, the clock distribution network consumes more than 60-70 % [1] of the total SoC power. This is in the order of microwatts or even milliwatts in conventional designs.

To save power, we shut down the main functional blocks including the system clock of the SoC and use another clock called the start-up clock or wake-up clock that will wake the main clock up from the off-mode upon occurrence of an event. This wake-up clock is designed such that it consumes less power. It is acceptable to reduce the clock frequency for the start-up clock to kHz range or even to the sub-Hz range, since the clock is used to provide timing to the always ON blocks whose timing is not critical. This will reduce the power consumption to the nano-watt range. The main circuits, which include main functional blocks essentially have two modes of operation: the active mode with the main circuits in ON state, and the inactive or sleep mode wherein the system clock and main power supply are shut down via various techniques. Clock gating and power gating are well known techniques to achieve this. Clock gating and power gating are techniques wherein the clock and power supply circuits of a chip are shut down when not in use. The circuitry with timing provided by an ultra-low-power wake-up clock will continuously check every few milliseconds if any new event is occurring. The main circuit is activated upon the arrival of an event. Figures 1 and 2, respectively, show the start-up timer application in an SoC and the percentage SoC power it consumes. As depicted in Figure 1, the timing for the always ON circuits are provided by the wake-up clock.

In this thesis work an ultra-low-power start-up clock circuit has been designed that works in the kHz frequency range with few tens of nano-watts of power consumption. It is a fully integrated resistive frequency locked oscillator employing an ultra-low-power amplifier, a voltage controlled ring oscillator and a non-overlapping clock generator. Simulations were carried out in order to check stability including voltage sensitivity and temperature stability. The layout was drawn and post layout simulations including parasitic extraction, were done for the proposed design. The Cadence

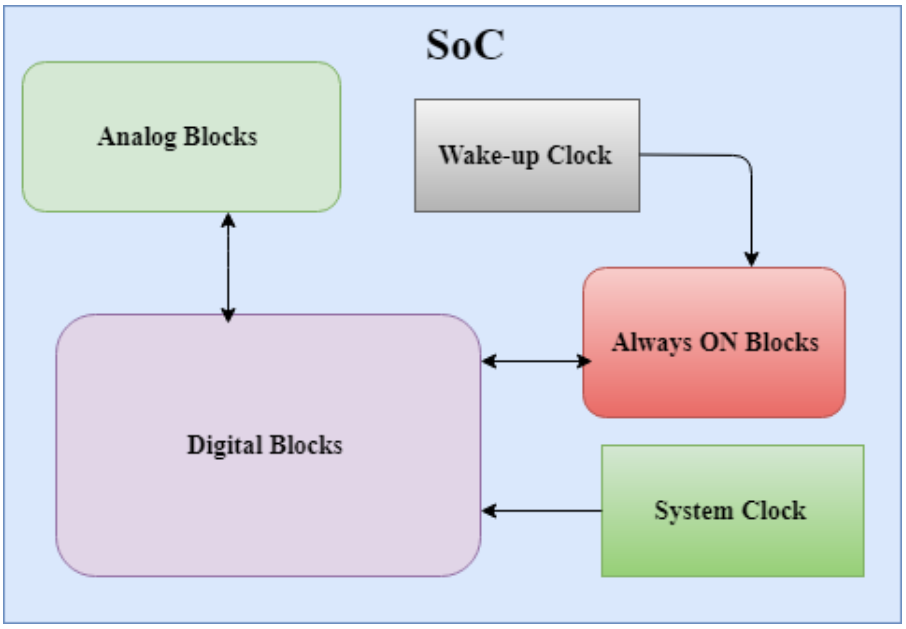

Figure 1: Block diagram showing application of wake-up timer

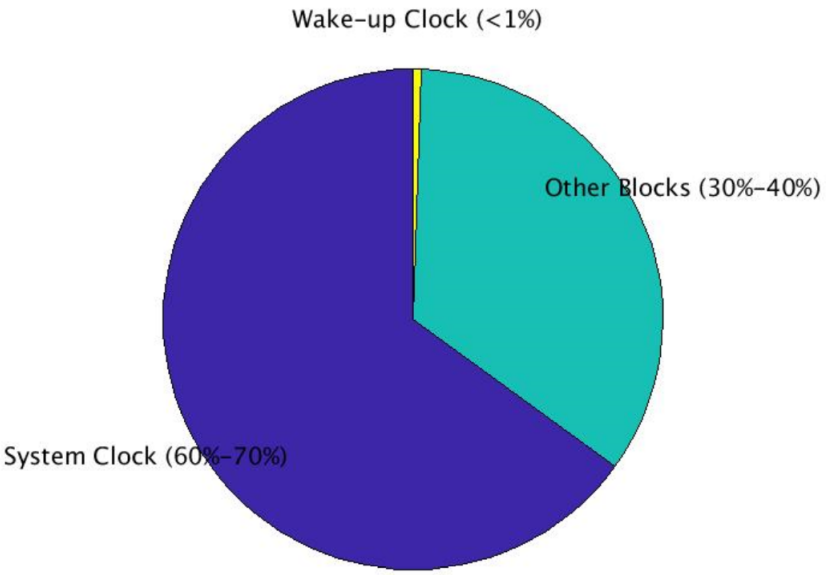

Figure 2: Chart showing power consumption breakdown in an SoC

Virtuoso tool was used for the design and simulations. The circuit was designed in 180 nm CMOS process technology. Care has been taken to minimize the supply and temperature variations of the clock.

2 Wake-up Clock Architecture

Clock design has been one of the important design topics and different topologies have been proposed by various designers. When it comes to the wake-up clock, the main concerns are power consumption and stability. Since the circuit is in ON-state for most part of the operation, it is essential that the power consumption is made as low as possible. In addition, the temperature dependency of the circuit has to be minimal. Long term stability should be high whereas Allan deviation which is proportional to system noise should be zero ideally.

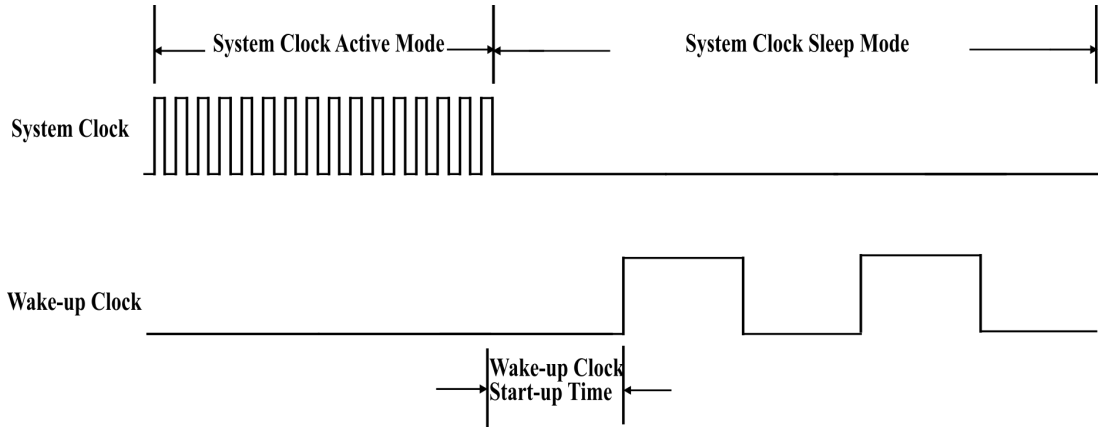

Figure 3: System and wake-up clock signals

The waveform of a system clock running at a MHz or GHz frequency is shown in Figure 3 along with the waveform of the wake-up clock running in the kHz frequency range. The time duration when the system clock and the major blocks of the SoC are ON is called the active mode. The circuitry that uses wake-up clock wakes the main clock whenever the SoC has to go to active. For example, in a radio receiver the wake-up clock and associated circuitry wake the system clock up when the potential signal for data reception is detected. As shown in Figure 3, it takes a small amount of time for the wake-up timer to turn ON and become stable. This is due to the internal delay of the wake-up clock. This time is known as start-up time of the wake-up clock. Some of the main wake-up clock architectures are discussed in the following section.

2.1 CMOS Timer

CMOS(Complementary Metal-oxide Semiconductor) timers are built using CMOS transistors and passive elements like capacitors and resistors. In CMOS timers a capacitor voltage, while the capcaitor is charged using a constant current source is compared with a reference voltage. The frequency of the clock generated depends on the time taken for the capacitor to charge to the reference voltage and hence on the value of the charging current.A CMOS timer without a comparator is introduced in reference [2]. Generally CMOS timer suffers from poor temperature stability and

large frequency deviation [45]. Nevertheless, this topology can generate clock signals ranging from the sub-Hz upto GHz range consuming only a few tens of picowatt power [2]. An example for CMOS timer is ring oscillator [21].

2.2 Crystal Timer

A quartz crystal works based on the principle of piezoelectric effect. The crystal determines the frequency of the clock generated. Unlike CMOS timers, crystal timers show excellent stability against temperature fluctuations and a low noise level. Since crystal is an off chip element the overall timer consumes significant area. Typically crystal based clock generator are used for a system clock due to their excellent stability characteristics. However, recently nanowatt crystal clock generators has also been developed which are also suitable for wake-up clock [49]. References [4] show example topologies which uses high-quality oscillators with precisely timed energy injection technique to speed up the timer startup.

2.3 MEMS Timer

Wake-up timers can also utilize with Micro-Electro-Mechanical Systems (MEMS) technology.MEMS oscillator has stronger temperature dependence and higher noise than crystal oscillators, and therefore it is often stabilized using phase-locked loop(PLL). The MEMS-oscillators have a better support for high integration than crystal oscillator. In some technologies it is even possible to implement on a chip. The MEMS resonator is temperature dependent with temperature dependence of around 500ppm [51]. But the timer can be desensitised against temperature fluctuation using several techniques and can be made highly temperature stable. This makes it suitable for the system clock for an SoC. They are available with the frequency ranging from kHz to GHz with power consumption of nanowatts to milliwatts based upon the frequency of operation and circuit complexity. Examples for MEMS timers are presented in references [6] that uses frequency scan technique to achieve startup of the timer and, hence, lock for the phase locked loop.

2.4 RC Timer

The operation principle of RC-timers is based on the RC time constant. A classical RC-timer is the relaxation oscillator in which the capacitor is charged through the resistor. When the capacitor is charged a comparator turns a switch on to discharge the capacitor and the capacitor charging is started again. In a relaxation oscillator the capacitor charging can be performed also by a constant current. When the capacitor voltage is compared with a voltage generated by driving a constant current through a resistor the oscillation frequency will again depend on the RC time constant. In relaxation oscillator the offset, noise and delay of the comparator are the main sources of inaccuracy. To minimize the delay and noise of the comparator leads to increased power consumption. Also the temperature dependence of the resistor needs to be compensated for to increase long term stability of the oscillation frequency.

2.5 FLL Timer

A stable clock signal can be generated by using a frequency locked loop (FLL). FLL can be implemented with a frequency -to-voltage converter, loop filter and VCO connected in a loop. In ref. 7 the frequency-to-voltage converter is implemented with a switched capacitor which is toggled with the VCO output signal and is driven with a constant current source. The equivalent resistance and the voltage of the switched-capacitor depends on the VCO oscillation frequency. By comparing the voltage of the switched-capacitor to a voltage of a reference resistor driven also with a constant current the oscillation frequency is determined by the RC time constant of the reference resistor and the capacitor. This timer can be fully integrated on-chip and shows high frequency stability against process, voltage and temperature variations. Also, a low power implementation is possible, however, this is limited by the size of the reference resistor. In ref. [7] they have achieved Allan deviation lower than 7 ppm and temperature stability of 32ppm/°C with power consumption of only 110nW.

2.6 LC Timer

On-chip LC-oscillators are mainly used at GHz-frequencies as on the chip we can implement inductors of few nanoHenries and capacitors of some picofarads. These oscillators are manily used in RF systems. When the oscillators are designed at lower frequencies, then external bulky inductors and capacitors are needed, which is unpractical for a wake-up clock generation. Reference [13] shows an example of a LC-based timer topology that uses series LC tan, with additional control circuitry for quick strat-up. An LC timer circuit generates the clock whose frequency depends on the values of the inductor and capacitor. The use of off chip inductor and associated noise make this type of timer nonsuitable for our timer application. But this class of timers can achieve upto a few tens of GHz clock frequency and are generally suited for main system clock.

2.7 Architecture Selection

The comparison of different timer architectures against performance parameters is shown in Table 1. After a thorough study of different architectures and their performance parameters, a FLL-based clock design was chosen for the design of the wake-up timer. The FLL based-design is an improvement over an RC timer with all desired qualities meeting the design specifications. The crystal and MEMS timer designs require off-chip components which in turn make the implementation complex. The reason for not selecting an LC-based clock circuit is because of frequency, power and area constraints. In order to achieve lower frequency of operation, a high value inductor has to be used resulting in requirement of larger area in the layout. Moreover, the inductor integration techniques are complex compared to that of other passive components. The above listed performance parameters meeting the requirements are achieved by using a resistive frequency locked loop timer.

Table 1: Comparison of different start-up timer architectures [47].

	CMOS	**Crystal**	**MEMS**	**RC**	**LC**	**FLL**
Frequency	Hz-GHz	kHz-MHz	kHz-GHz	kHz-MHz	GHz	kHz-MHz
CMOS process	Good	Bad	Bad	Good	Good	Good
Off-chip components	No	Yes	Yes	No	No	No
Power	pW-mW	nW-mW	nW-mW	<1mW	1mW	nW
Temperature Stability	Very Bad	Very Good	Very Good	Bad	Bad	Good
Noise Stability	Bad	Very Good	Good	Bad	Bad	Good
Suitable for system clock	No	Yes	Yes	No	No	Yes
Suitable for wake-up clock	Yes	Yes	Yes	Yes	No	Yes

Figure 4 shows the circuit diagram of the conventional method of clock-generation using an RC relaxation oscillator. The conventionally used RC relaxation oscillators consists of two current sources which are identical to each other, one being connected to a switched-capacitor(SC) (that has a reset switch) and the other to a resistor on the other branch. Voltages generated across the resistor and the capacitor are compared with a comparator. Whenever the capacitor voltage rises over the resistor voltage, the switch turns on and the capacitor discharges. This process creates a clock pulse whose frequency depends on the values of the resistor and the capacitor.

The minimum output clock period is determined by the sum of the delays of the transistor switch, comparator delay and the delay of the buffer. As far as temperature stability of the circuit is concerned,a series connection of negative temperature coefficient(NTC) and positive temperature coefficient(PTC) resistors can be used to minimise the temperature dependency on the resistor branch. In the other branch, the MIM-capacitor has negligible temperature effects. However, the temperature variation of the comparator and buffers remains a main source of instability in the circuit. The design presented in reference [11] proposes an offset cancellation technique wherein the comparator input polarity is switched every half cycle of the period in order to avoid drift in the comparator offset voltage with respect to temperature. However, in this technique, as the comparator input voltages are close to each other, the comparator switches its output frequently increasing rail-to-rail leakage of the comparator current and power consumption.

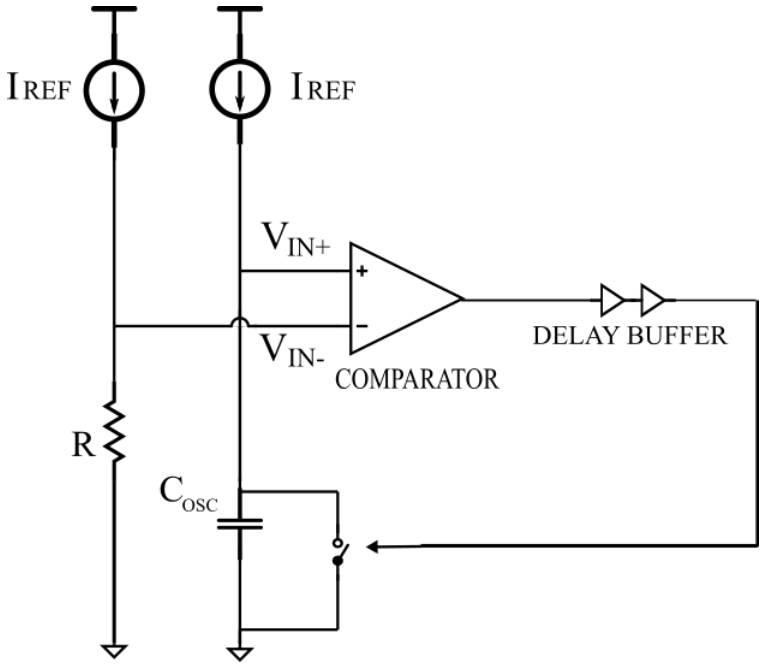

Figure 4: Schematic of conventional RC oscillator[7].

3 Overview of the Wake-up Clock Design

The proposed design, which is based on reference [7] is shown in Figure 5. The design essentially consists of a resistor and switched-capacitor branch followed by an ultra-low-power (ULP) amplifier, voltage controlled oscillator (VCO) and a non-overlapping clock generator circuit. The resistor and capacitor branches provide the reference and capacitor voltages respectively, which are fed into the amplifier. The output of the amplifier is a DC voltage which is fed to the VCO that produces a square wave signal. The non-overlapping clock generator produces two non-overlapping clock signals from the VCO output signal. These two non-overlapping clock signals control the switching of the capacitor. A more detailed description of the design is given in the following sections.

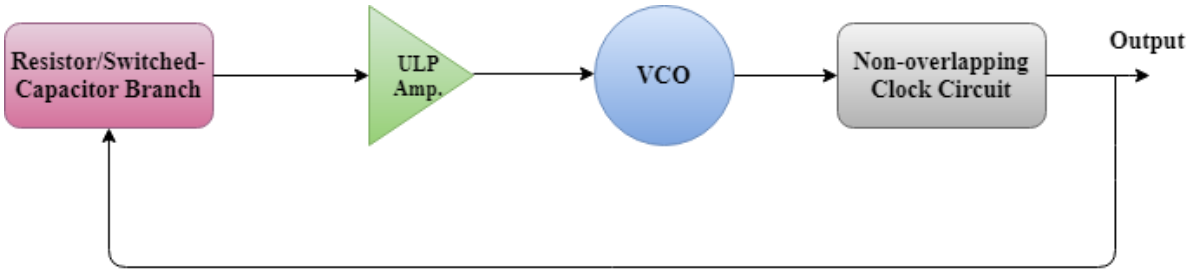

Figure 5: Overview of proposed architecture

3.1 Design Specifications

The following are the design specifications of the wake-up timer.

- Frequency: Few kHz
- Power consumption: Few tens of nanowatts
- CMOS process: 180 nm
- Supply voltage : 1.2 V
- Temperature Range : -40°C to 75°C
- Temperature stability: 100s of ppm/°C
- Supply voltage range: 1.2 V +/- 10%
- Layout Area : minimum possible area

3.2 Resistive Frequency Locked Oscillator

In this work a resistive frequency locked loop oscillator (RFLO) based ultra-low-power wake-up clock which is based on the design in reference [7] is implemented. This design eliminates the drawbacks of the RC relaxation oscillator-based design discussed in the section 2.7. This RFLO is essentially designed based on the principle that a switched capacitor can function as a resistor controlled by voltage controlled oscillator (VCO) [11], [15]. Unlike the conventional design this structure consists of an ultra-low-power(ULP) amplifier that acts as a solution to the power hungry comparator in the conventional RC-based relaxation oscillator. The equivalent resistance of the switched-capacitor is tuned by the feedback loop to be equal to the temperature compensated resistor [7].

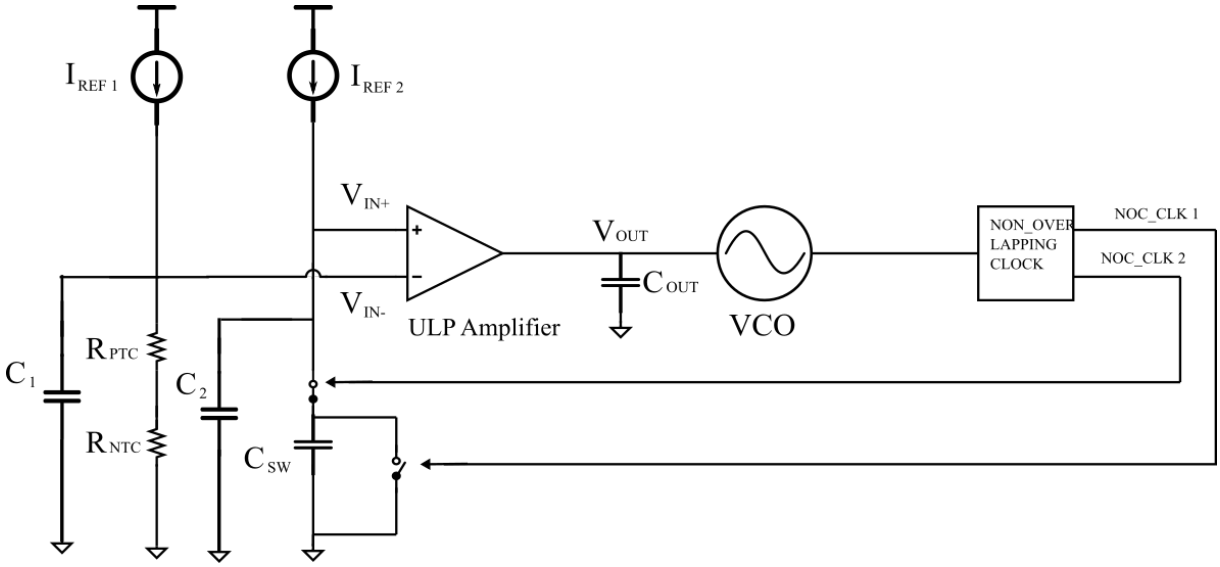

Figure 6: Resistive frequency locked loop wake-up clock design

Figure 6 shows the simplified circuit diagram of the RFLO timer. The inverting input terminal of the ULP amplifier is connected to the temperature-compensated resistive reference circuit which is fed with a constant current of 5nA. The constant current reference used is a resistor-less beta multiplier [41]. The non-inverting input terminal of the amplifier is connected to the the switched-capacitor circuit as can be seen [7].

3.3 Operation Principle of Resistive Frequency Locked Loop

The RFLO operates based on the principle that matching the equivalent resistance of a switched-capacitor circuit to a temperature-compensated reference resistor (R_{ref}) will generate a constant frequency clock. The positive temperature coefficient resistor and the negative temperature coefficient resistor are denoted as R_{PTC} and R_{NTC} respectively. The combination of R_{NTC} and R_{PTC} resistors provides a resistance

value of 29.26 MΩ. Since the current source is 5 nA, the reference voltage across the resistor combination is 146 mV. This is the voltage indicated as V_{IN-} in Figure 6 . The voltage across the switched-capacitor circuit, indicated as V_{IN+} (see Figure 6) and is connected to the non-inverting terminal of the amplifier [7].

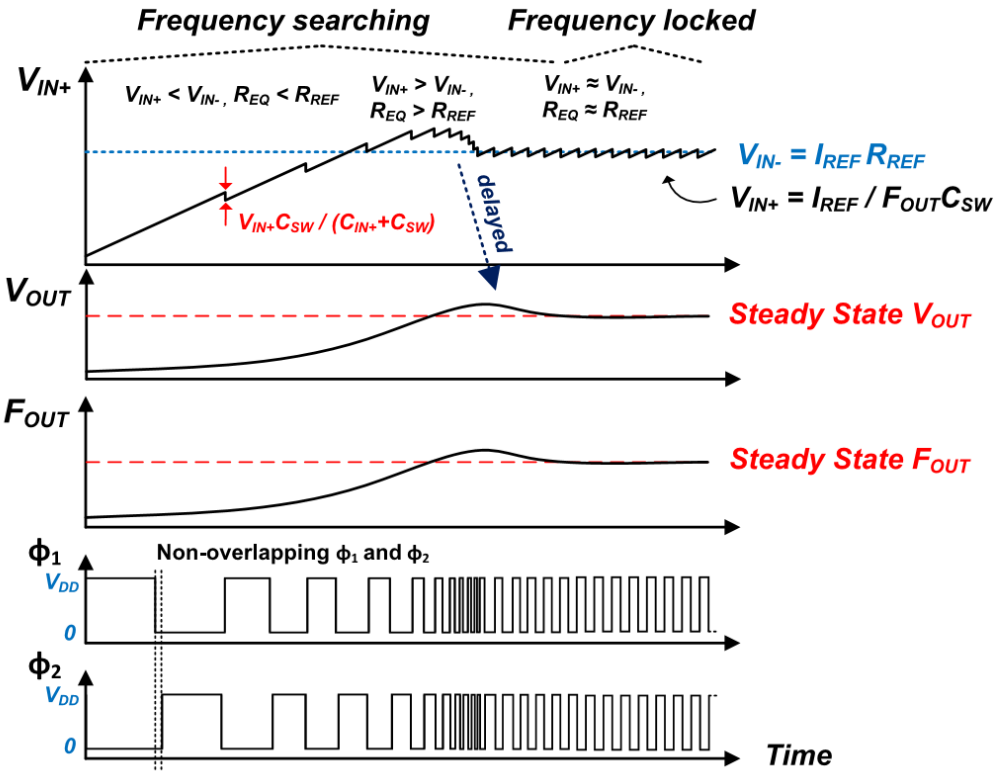

Figure 7: The conceptual operating waveforms of RFLO [7]

Figure 7 shows the expected waveforms of the RFLO, the loop trying to match both the V_{IN+} and V_{IN-} at the input of the ULP amplifier. Both the values gradually builds up to the reference value (146mV) as seen from the plot. When $V_{IN+} < V_{IN-}$, the amplifier output forces the switch control signal to switch at lower frequency allowing C_2 charges to higher voltages. This continues until voltages V_{IN+} and V_{IN-} are equal. The voltage V_{IN+} can be expressed as [7]

$$V_{IN+} = \frac{I_{REF}}{C_{SW} F_{OUT}} \tag{1}$$

where $1/SC_{SW}F_{OUT}$ is the equivalent resistance of the switched-capacitor circuit. When the frequency is locked, $V_{IN+} = V_{IN-}$ $(= I_{REF}R_{REF})$. The frequency F_{OUT} at which the VCO runs is given by [7]

$$F_{OUT} = \frac{1}{R_{REF} C_{SW}} \tag{2}$$

Here,

$$R_{REF} = (R_{NTC} + R_{PTC}) \tag{3}$$

Hence,

$$F_{OUT} = \frac{1}{(R_{NTC} + R_{PTC})C_{SW}} \tag{4}$$

While $V_{IN+} < V_{IN-}$, the oscillation frequency F_{OUT} increases until V_{IN+} overcomes V_{IN-}. Due to the delay of the loop, overshoot and ringing happens until V_{IN+} reaches V_{IN-} and frequency searching is finished (see Fig. 7).

3.4 Frequency response of RFLO

A more quantitative analysis can be made by considering the V_{IN+} impedance (Z_{VIN+}). Since C_1 and C_2 are equal in size, we consider,

$$C_1 = C_2 = C \tag{5}$$

The partial derivative of the Z_{VIN+} with respect to F_{OUT} can be derived as [7]

$$Z_{VIN+} = \frac{1}{sC} \parallel \frac{1}{C_{SW}F_{OUT}} \tag{6}$$

$$\frac{dZ_{VIN+}}{dF_{OUT}} = \frac{-C_{SW}}{(sC + C_{SW}F_{OUT0})^2} = \frac{-C_{SW}}{(sC + \frac{1}{R_{REF}})^2} \tag{7}$$

The frequency response of the RFLO is derived as [7]:

$$F_{OUT}(s) = A_V \frac{\frac{1}{sC_{OUT}}}{R_{OUT} + \frac{1}{sC_{OUT}}} K_{VCO} I_{REF} \cdot (-\frac{-C_{SW}}{(sC + \frac{1}{R_{REF}})^2}) \tag{8}$$

$$= A_V \frac{1}{1 + sC_{OUT}R_{OUT}} K_{VCO} I_{REF} \cdot (-\frac{-C_{SW}}{(sC + \frac{1}{R_{REF}})^2})$$

Here, A_V is the gain of the amplifier, R_{OUT} is the output resistance of the amplifier, C_{OUT} is the capacitance at node V_{OUT} and K_{VCO} is the VCO gain.

The value of R_{OUT} from the simulation is 147 MΩ, and the value of C_{OUT} is 10 pF. The RFLO has 3 poles, one pole is at -1/$C_{OUT}R_{OUT}$ and another two poles at -1/CR_{REF}. The ratio of the C_{SW} to C_2 is 0.1 (4.13 pF/40.93 pF). The ripples caused due to switching of the switched-capacitor circuit are averaged out by the a high value averaging capacitor C_2. The ultra-low-power amplifier essentially works as an operational transconductance amplifier (OTA) with a low frequency bandwidth. This will act as a low pass filter(LPF) and blocks high frequency ripples from affecting the frequency oscillation F_{OUT}. The DC gain of the amplifier is 76 dB. The changes

in the OTA input appears at the output only after a certain delay due to the fact that the amplifier is band limited.

The switched capacitor branch shows a temperature dependence of 24 ppm/°C. This is caused by the switch transistor leakage. The transistors used are high threshold voltage (HVT) that have lower leakage compared to normal transistors. Since the capacitor used is the MIM-capacitor, the temperature dependence of the capacitor itself is at its minimum in the order of nV/°C. The voltage at the node to which C_2 is connected (see Figure 6) in the RFLO loop is shown in Figure 8. Initially the voltage across the capacitor C_2 is charged to V_{DD}, with constant current of 5 nA. This voltage eventually drops down and settles to the voltage following the resistor reference voltage through feedback. The settling time is around 12 milliseconds.

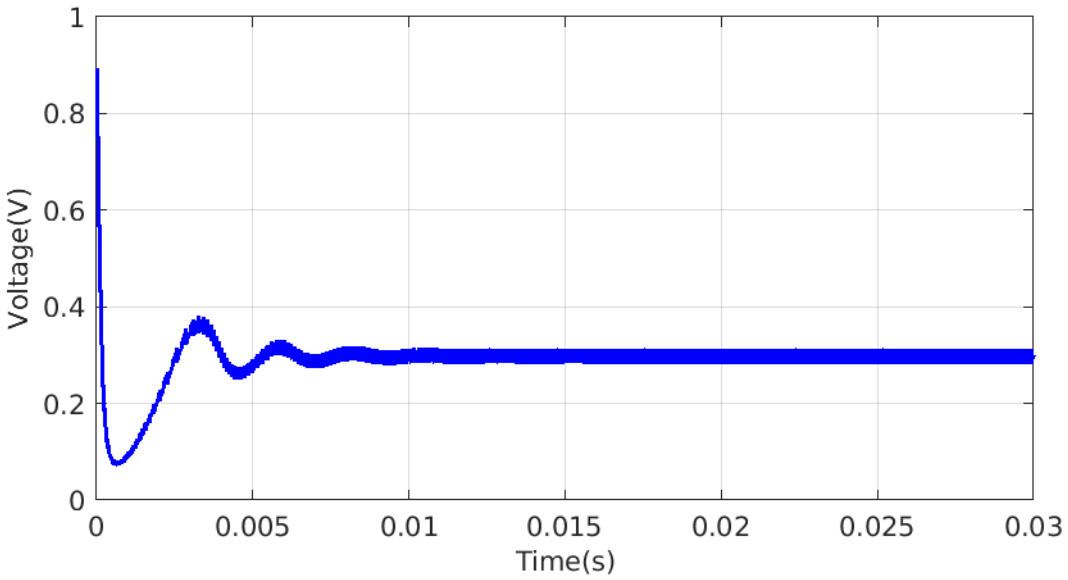

Figure 8: Switched-capacitor circuit response in RFLO

3.5 Advantages of RFLO

The primary advantage of using the RFLO for clock generation is that the circuit replaces the traditional power hungry comparator with an ultra-low-power amplifier, hence removing the effect of power and temperature instability caused by a traditional comparator based solution. Secondly, the OTA always tries to make both the input (V_{IN+} and V_{IN-}) equal, hence making the output stable. Once the clock becomes stable, the only source of instability is from temperature variation that will cause the VCO frequency to drift. This is essentially tracked by the amplifier. In addition, since the variation in temperature is slow, the ULP amplifier can have a low-bandwidth. In a traditional RC relaxation oscillator, the circuit resets every cycle and for this reason the relation between the charge in the current cycle with respect to the previous

cycle is lost. The RFLO carries change in the charge (ΔQ_i) from one cycle to other and accumulates it on the C_2 node for N cycles which is given by [7].

$$V_\Delta = \sum_{i=0}^{N} \frac{\Delta Q_i}{C_2} \tag{9}$$

Random noise is the main source of the error, and the sum of Q_i becomes zero over many cycles. The amplifier error compensation nullifies the error by adjusting the frequency even if the ΔV is non-zero. On the other hand, the clock has a long term frequency instability. The main reasons for instability are: flicker noise and long-term drifts in the values of resistors, and capacitors. Also, there is a variation in the amplifier offset over the time [7].

4 Sources of Temperature Instability and Its Solution

Various reasons for temperature instability in the RFLO circuit and it's solution are explained in this section. As we discussed earlier, the output frequency F_{OUT} of the clock is dependent only on R_{REF} and C_{SW}, and is given by $F_{OUT} = 1/R_{REF}$ .C_{OUT}. The equation remains valid only in the ideal conditions. In actual scenario, the delay of each component in the path has to be taken in to account while determining F_{OUT}. A Metal-Insulator-Metal (MIM) capacitor which generally has a very low temperature coefficient is used in the switched capacitor circuit [7].

4.1 Temperature Dependence of Switched-Capacitor Branch

Figure 9 shows the circuit diagram of the switched-capacitor circuit. The current reference circuit (I_{REF2}) provides a constant 5nA current to the circuit. The capacitor C_{SW} holds the charge based on the switching of transistors controlled by the NOC_CLK1 and NOC_CLK2 signals from the non overlapping clock generator. The voltage across the C_{SW} is determined by switching of the high threshold voltage (HVT) transistors. The use of HVT transistors reduces the effect of leakage current in the circuit. The dimension of the switching transistors is minimum (220 nm/180 nm), so that the gate capacitance is minimum, and the leakage is minimum. The purpose of the capacitor C_2 is to average out the voltage at the node where the C_{SW} is connected to, and hence a constant voltage which is equal to the voltage across the resistor branch (through a feedback loop) is obtained across C_2 [7].

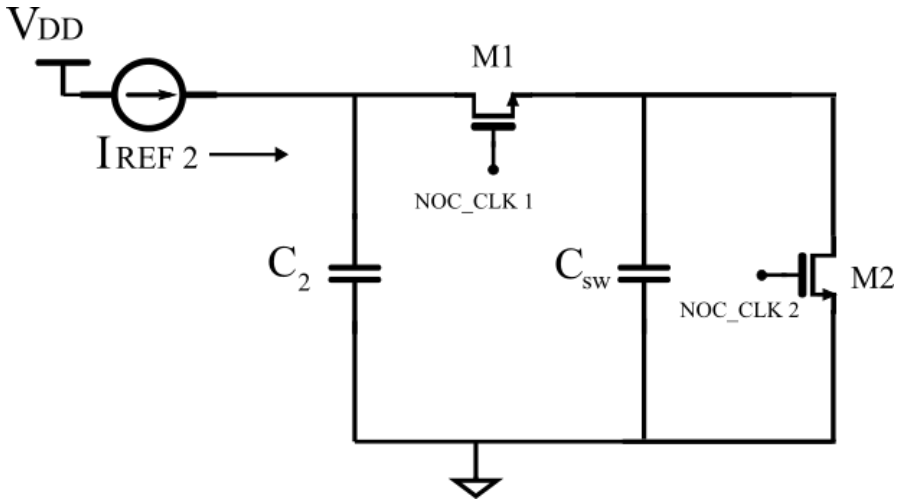

Figure 9: Schematic of switched-capacitor circuit

The graph in the Figure 10 shows the response of the switched-capacitor circuit across temperature. This plot is obtained when a constant 5nA current is supplied to the circuit shown in Figure 9. The temperature response is taken from -40°C to 85°C.

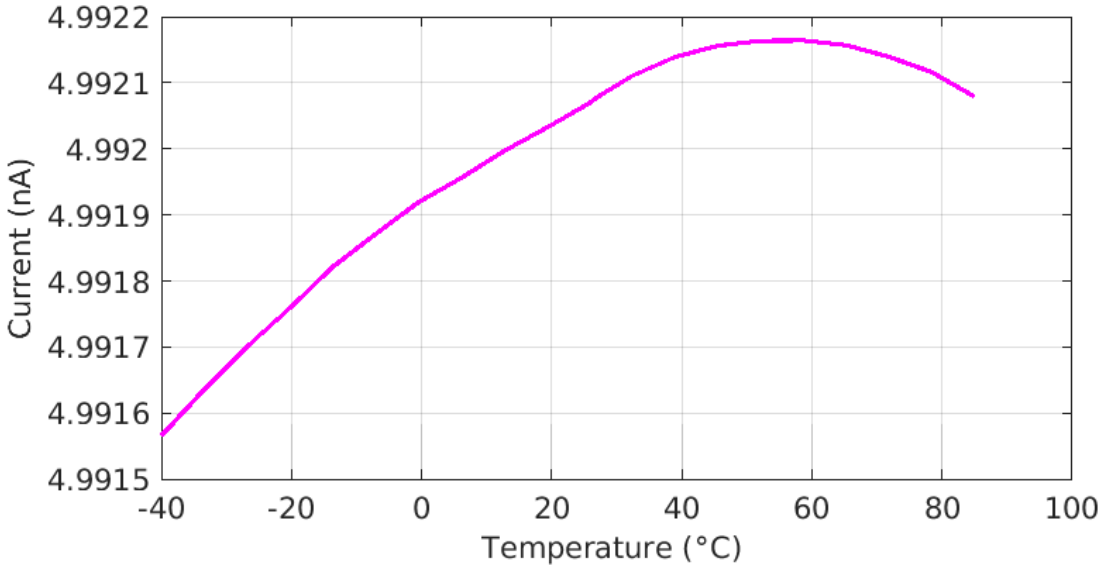

Figure 10: Temperature dependence of switched-capacitor circuit

4.2 Temperature Dependence of Resistive Branch

In the resistive reference branch of the RFLO based clock circuit, a constant current source of 5 nA is connected to a series resistor combination. A MIM capacitor of 40 pF is connected in parallel with the resistors to bypass high frequency variations in the current source. As the resistor is a temperature-dependent discrete component, it is therefore difficult to achieve stable operation over a wide temperature range (-40°C to 85°C). But there are resistors with either negative temperature coefficient (NTC) or positive temperature coefficient (PTC) characteristics. The NTC resistors are the ones whose resistance reduces with respect to temperature, and the PTC resistors are the ones whose resistance increases as temperature increases.

Various series combinations of different types of PTC and NTC resistors are simulated to find the temperature dependency and the total silicon area needed. A current of 5nA is applied to the net resistance of 29MΩ to produce a reference voltage of 146mV. Two resistors, one with NTC and the other with PTC, are connected in series such that the ratio of their values effectively cancels the temperature effects.

The temperature dependency of the resistor is measured in parts per million(ppm) and is given by

$$TC_R = \frac{RD}{TR} \tag{10}$$

where,

$$RD = \frac{(V_{MAX} - V_{MIN}) \times 2}{V_{MAX} + V_{MIN}} \tag{11}$$

here, RD is the relative difference and TR is the temperature range (-40°C to 85°C)

After careful consideration of all the resistor combinations available, combination of a p type resistor and a n type resistor gives the best performance. This combination takes a silicon area of 92250 μm^2. The resistor value corresponding to this resistor combination is 29.26 MΩ. The temperature coefficients of the switched-capacitor branch and resistor branch are selected in such a way that they are minimum and they will cancel each other at the input of the ultra-low-power amplifier. Since the temperature coefficient of switched-capacitor circuit is negligible, the resistor combination is chosen to get same temperature coefficient, thus the effect of temperature got cancelled.

The graphs in the Figure 11, 12 and 13 respectively demonstrates the temperature dependency of the PTC, NTC and combination of the PTC and the NTC resistors connected in series with certain ratio of resistance value. The voltage value along the y-axis of all the three graphs indicates the voltage deviation with respect to temperature across the PTC, NTC and combination of the NTC and the PTC resistor for a given value of the resistance and the constant 5nA current. For the selected p-type PTC resistor, the temperature coefficient is 159 ppm/°C and for the selected n-type NTC resistor, the temperature coefficient is 808 ppm/°C. When the series combination of the NTC and the PTC resistors were used, the temperature coefficient of 0.0277 ppm/°C is achieved for the resistor pair.

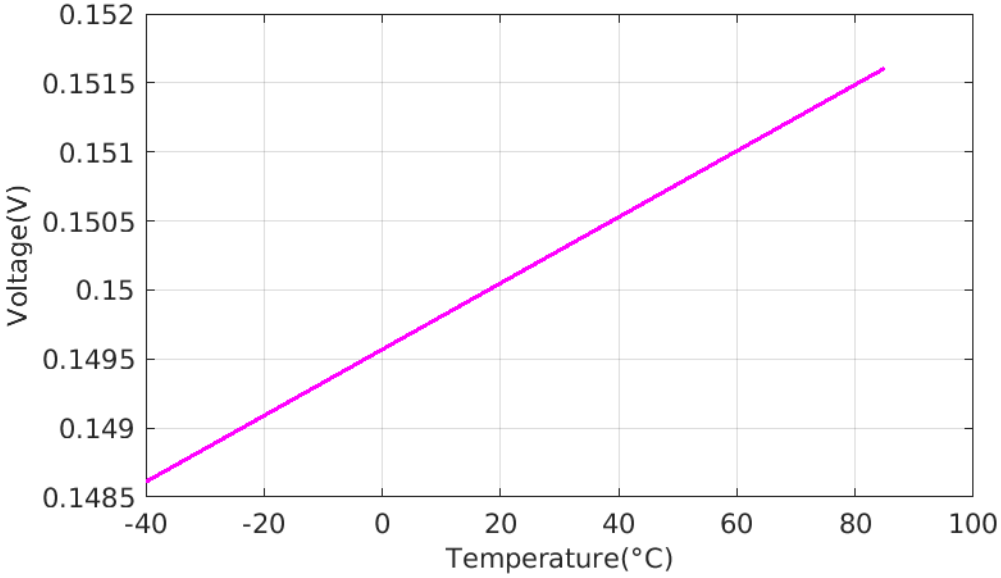

Figure 11: Temperature Dependence of PTC Resistor

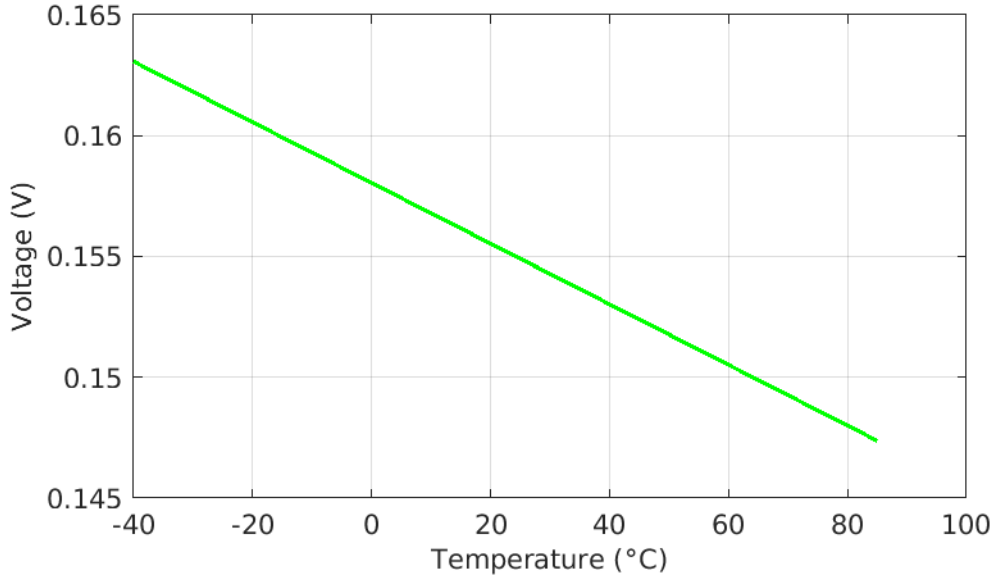

Figure 12: Temperature Dependence of NTC Resistor

4.3 Current Chopping Technique

Mismatch in the current will not result in any effect on the temperature stability of the circuit if the mismatch is constant with respect to temperature. On the other hand, if the current mismatch is not constant and keeps varying with respect to the temperature, the temperature stability of F_{OUT} is effected. This issue is resolved

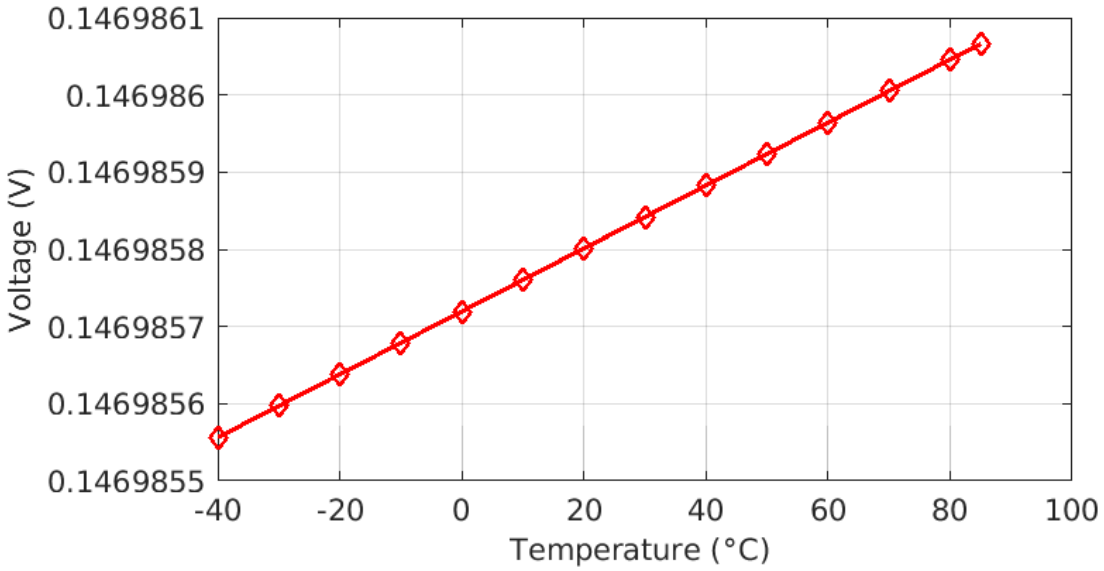

Figure 13: Temperature Dependence of PTC and NTC resistor combination

with the help of a technique called current chopping as explained in Reference [7].

Figure 14 and 15 shows the circuit diagram of the RFLO using the current chopping technique. The current supplied by each source I_{REF1} and I_{REF2} is chopped and fed to each branch based upon the switching of the transistor switches. The transistor used here for switching is high threshold voltage (HVT) transistors so that they will have less leakage. The current which is averaged out to the resistive branch is given by I_{EFF1}, and that to switched-capacitor circuit is given by I_{EFF2} wherein EFF denotes effective current. The I_{EFF1} and I_{EFF2} are equal and are given by

$$I_{EFF1} = I_{EFF2} = \frac{I_{REF1} + I_{REF2}}{2} \tag{12}$$

During phase 1 of operating time, the I_{REF1} flow through resistor branch constitutes the first half of the I_{EEF1} and the I_{REF2} flow through switched-capacitor branch constitutes the first half of the I_{EEF2}. Similarly, During phase 2 operating time, the I_{REF2} flow through resistor branch constitutes the second half of the I_{EEF1} and I_{REF1} flow through switched capacitor branch constitutes the second half of the I_{EEF2}.

The switching of the transistors is controlled by the control signal which is the same as both NOC_CLK1 and NOC_CLK2 signals. The problem of using a non-overlapping clock signals for controlling transistor switching in the current chopping technique is that there is a small period of time (10μs) for which both transistors are OFF and no current flows to either of the branches. Nonetheless the time for which the transistor is OFF is negligible in that it does not impact the overall performance of the circuit [7].

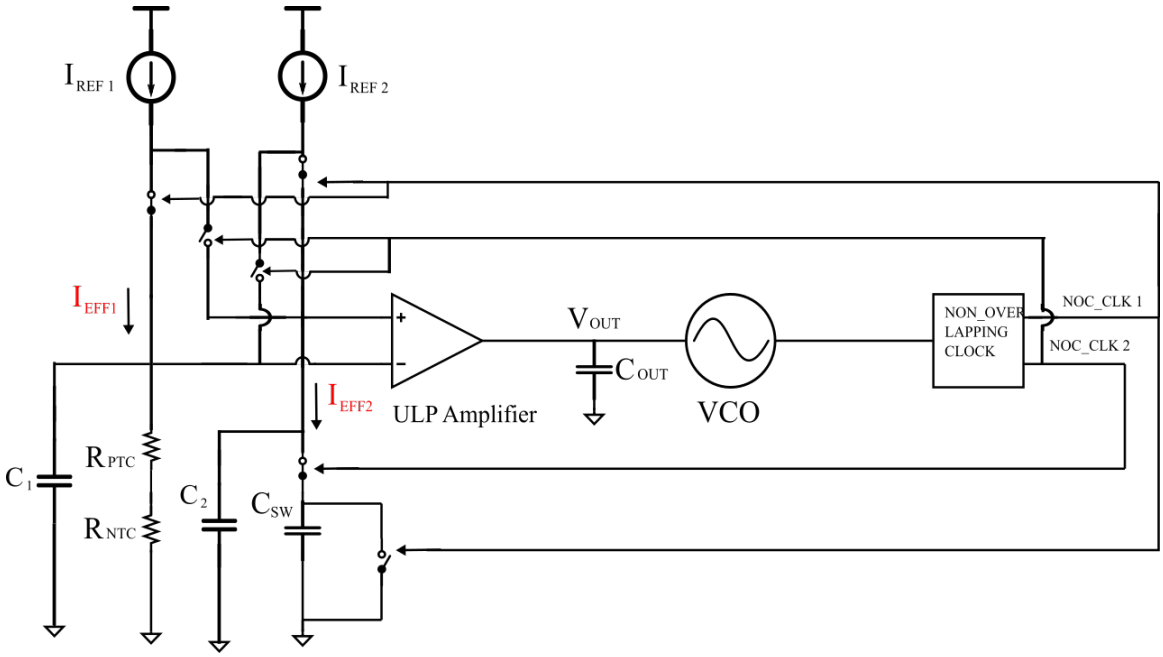

Figure 14: Schematic of current chopping technique (Phase 1)

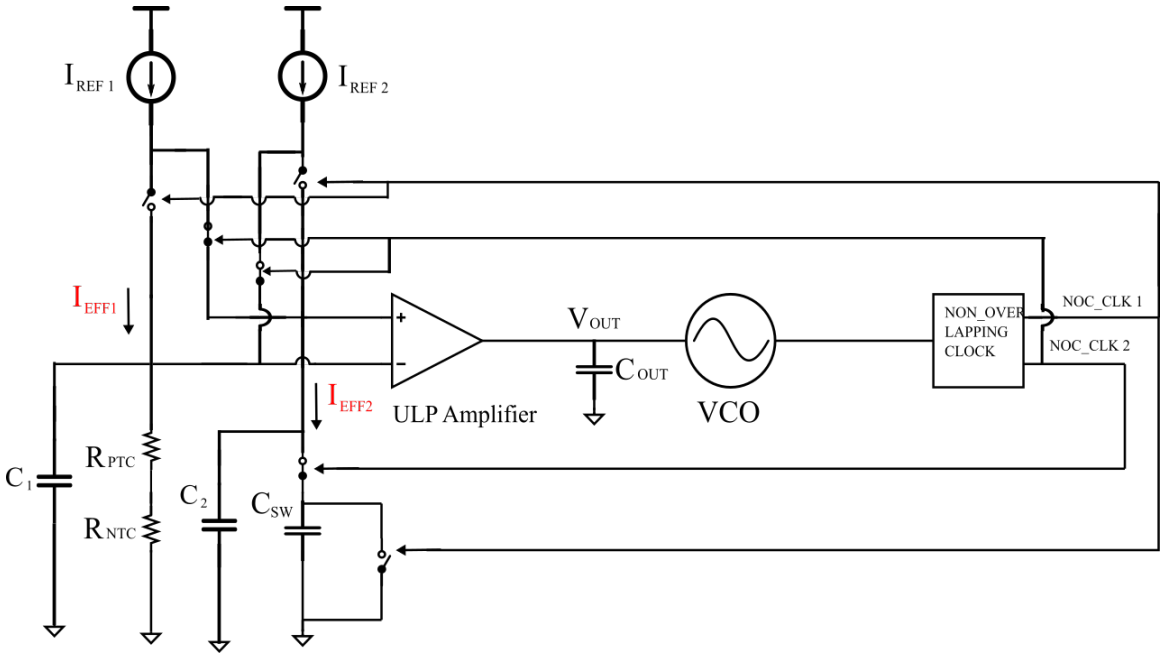

Figure 15: Schematic of current chopping technique (Phase 2)

4.4 Effect of Switch Leakage Current in the Circuit

The in overall closed loop, transistor switch causes a leakage current (I_{leak}) in the switched capacitor circuit. This causes the output clock frequency to decrease slightly lower than the nominal value. Following equations summaries how the switch leakage current causes errors on frequency accuracy [7]. The voltage drop over R_{REF} is

$$V_{IN-} = (\frac{I_{REF1} + I_{REF2}}{2}) \cdot R_{REF} \tag{13}$$

and the voltage across the switched capacitor is given by

$$V_{IN+} = \frac{\frac{I_{REF1}+I_{REF2}}{2} - I_{leak}}{F_{OUT} \cdot C_{SW}} \tag{14}$$

As the V_{IN+} and V_{IN-} are equal when the loop has stabilized, by equating 13 and 14, we obtain the oscillation frequency to be,

$$F_{OUT} = \frac{\frac{I_{REF1}+I_{REF2}}{2} - I_{leak}}{(\frac{I_{REF1}+I_{REF2}}{2}) \cdot R_{REF} \cdot C_{SW}} \tag{15}$$

Hence, the above equations clearly demonstrate that the switch leakage current reduces F_{OUT} [7].

5 Design Description

5.1 Non-overlapping clock

An FLL based ultra-low-power oscillator requires at least one pair of non-overlapping clocks for ensuring no charge loss in the switched-capacitor branch. The non-overlapping clocks are the ones that determine the charge transfer in switched capacitor circuits. Non-overlapping clock (NOC) generator shown in Figure 16 essentially consists of a NOT gate, two NOR gates and two buffers that determine the non-overlapping time of the clock signals. The output signals of an NOC generator are two clock signals which are never high at the same time. Moreover there is a short instant of time, called non-overlapping time, when both the output signals of NOC are low, which is essential for switched-capacitor operation.

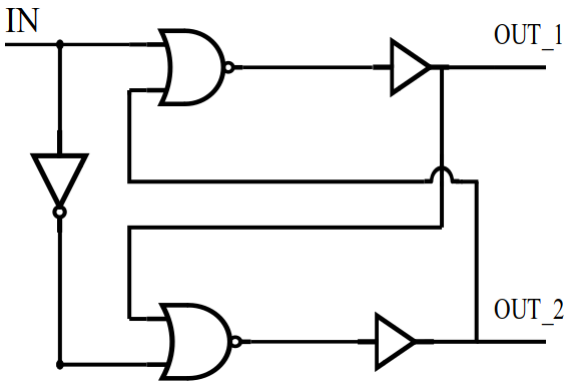

Figure 16: Simplified circuit diagram of non-overlapping clock

Figure 17 shows the input and output waveforms of the non-overlapping clock. As can be seen from the waveforms, the two clock signals OUT_1 and OUT_2 have a non-overlapping time.

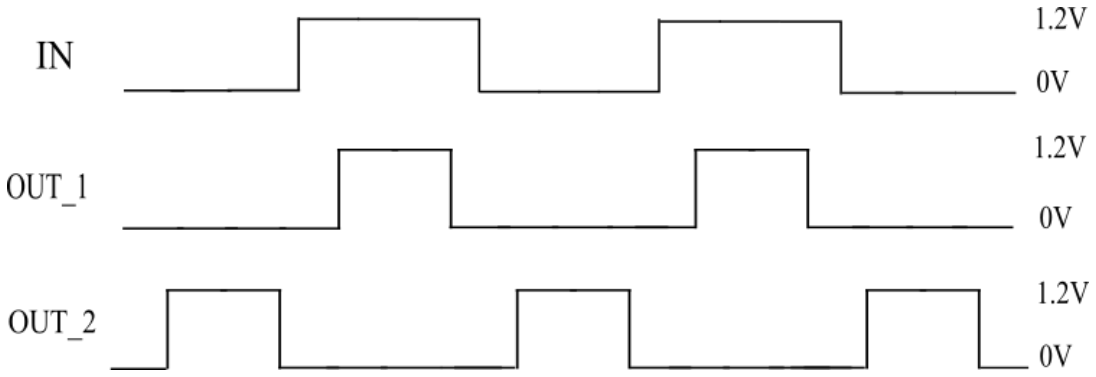

Figure 17: Non-overlapping clock waveform

The actual implementation of the circuit is as shown in Figure 18. The non-overlapping clock generator is realized using combination of NOT and NOR gates

and the delay buffers. The NOC have an active low enable pin which is connected to 0V for NOC operation. The delay buffer in the circuit provides a delay for the clock signal, to realize the non-overlapping time in the clock outputs.

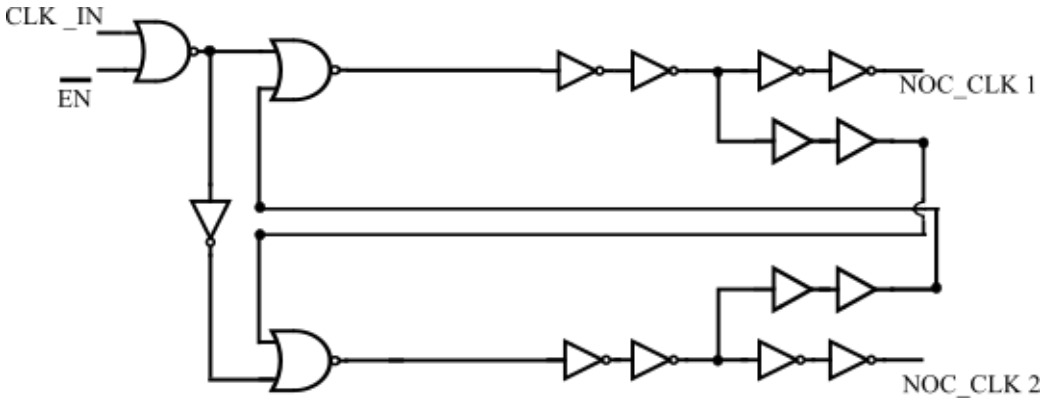

Figure 18: Non-overlapping clock circuit used in wake-up timer

In order to demonstrate the non-overlapping period of the non-overlapping clock signals, the NOC_CLK_1 and NOC_CLK_2 output of the non-overlapping clock is plotted in the Figure 19. The t_{noc} shows the non-overlapping time of the non-overlapping clock which is 10μs.

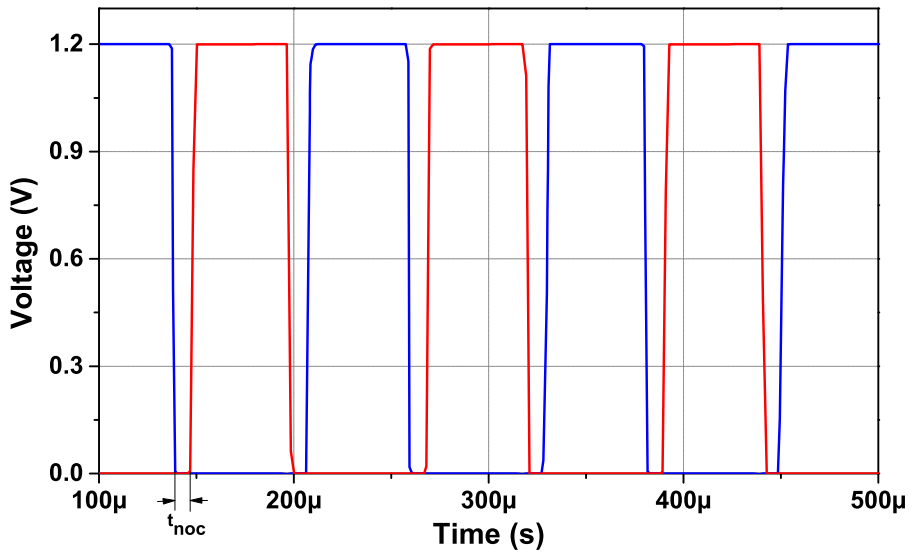

Figure 19: Plot showing non-overlapping period of clock

5.2 Ultra-Low-Power Amplifier

An operational amplifier is one of the essential building blocks of the analog circuits. The design of the amplifier becomes more complex with new CMOS technologies with reduced transistor length and decreased power supply voltage. The ultra-low-power amplifier in the proposed wake up timer acts as an error amplifier which detects the difference between the switched capacitor voltage and a reference voltage. The amplifier output acts as a control voltage for the VCO. There are many topologies for the amplifier design such as telescopic, folded cascode and two stage designs among which folded cascode topology was chosen for the design of amplifier in the RFLO loop.

5.2.1 Folded Cascode Amplifier

In many cases CMOS operational amplifiers are designed to drive capacitive loads [40]. It is difficult to build an operational amplifier, especially in lower supply voltages, which has low output impedance and can support larger swings. In such cases, the amplifier need not have to be necessarily a voltage amplifier. It can be a transconductance amplifier as well. The folded cascode design is a prominent topology for the amplifier which gives sufficiently large open loop gain, good output swing, convenient choice of common mode range and high output impedance. The operational transconductance amplifier (OTA) used in the design is a differential input single ended output amplifier.

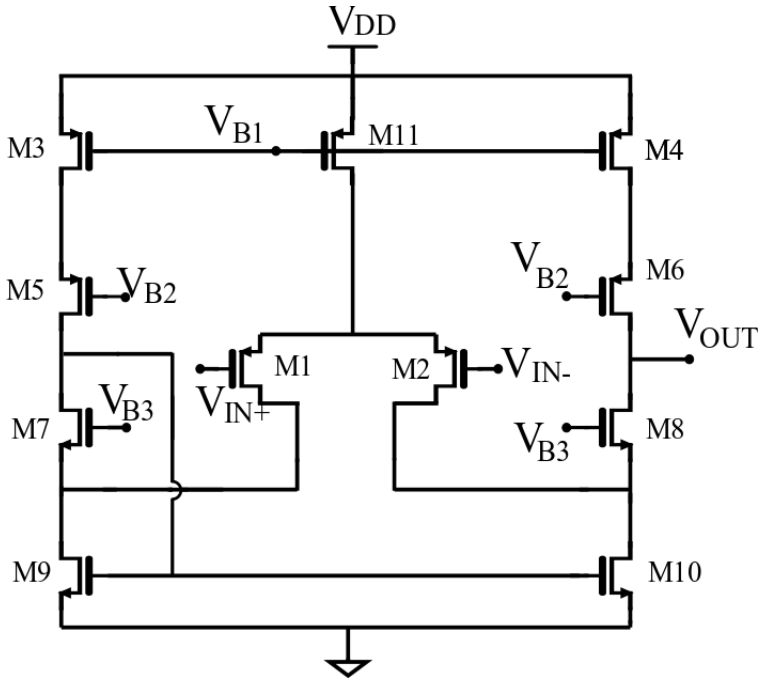

Figure 20: Folded cascode operational transconductance amplifier.

Figure 20 shows the circuit diagram of a PMOS input folded cascode operational

transconductance amplifier with bias voltages V_{B1},V_{B2} and V_{B3}. The bias voltages are provided by bias voltage generator that is discussed later.

5.2.2 Design of Folded Cascode Amplifier

The gain bandwidth product(GBW) of the amplifier is given by

$$GBW = \frac{g_{m1}}{2\pi C} \tag{16}$$

where g_{m1} is the transconductance of transistor M1 and C is the load capacitance The slew rate is given by

$$SR = \frac{I}{C} \tag{17}$$

where, I is the dc bias current of input transistors M1 and M2 and C is the load capacitance.

For an NMOS transistor operating in sub-threshold region, the drain current is given by [43].

$$I_D = A_n exp\left[B_n\left(V_{GS} - V_{TH}\right)\right]\left[1 - exp\left(\frac{-V_{DS}}{V_T}\right)\right] \tag{18}$$

where,

$$A_n = \mu_n C_{ox}\frac{W}{L}(m_n - 1){V_T}^2$$

$$B_n = \frac{1}{m_n V_T}$$

where $V_T = \frac{kT}{q}$ is the thermal voltage and m_n is a factor greater than one which is related to sub threshold slope and body-effect.Here W is the width of the transistor channel, L is the length of the transistor channel, μ_n is the electron mobility, C_{ox} is the transistor gate oxide capacitance density, V_{TH} is the threshold voltage V_{GS} is the transistor gate to source voltage and V_T is the thermal voltage.

For $V_{DSn} \geq 4V_T$, the current I_D can be assumed to be independent of V_{DS}. Then equation (18) can be simplified to (19).

$$I_D \approx A_n exp\left[B_n\left(V_{GS} - V_{TH}\right)\right] \tag{19}$$

The transconductance of the input transistor in weak inversion region is given by

$$g_m = \frac{I_D}{m_n V_T} \tag{20}$$

which is also the transconductance of the OTA.
The DC gain of the folded cascode amplifier is given by,

$$A_V = \frac{g_{m1}}{\frac{(g_{ds4}g_{ds6})}{g_{m6}} + \frac{g_{ds8}(g_{ds2}+g_{ds10})}{g_{m8}}} \tag{21}$$

where g_{mi} is the transconductance of transistor Mi and g_{dsi} is the output conductance of transistor Mi.

Compared to a telescopic amplifier, a folded cascode amplifier gives better output swing. Moreover, building a telescopic topology in lower supply voltage makes the design stringent. A folded cascode design relaxes this situation along with the convenient choice of input common mode voltage. For example, the input common mode for a PMOS pair in a folded cascode design can be as low as 0 V and that for an NMOS pair can be as high as V_{DD}. A PMOS input pair is preferred over NMOS pair in order to have minimum 1/f noise. The 1/f noise of the PMOS transistor is two to five times lower than the NMOS one. The amplifier is designed to have a DC output common-mode voltage of 420 mV, that will act as control voltage for the VCO. The PMOS transistor M1 and M2 form the differential input pair, and the bias current for the differential pair is given by M11. The load is a self cascode load comprising of transistors M7, M8, M9 and M10 which gives a single ended output. If the bias voltages V_{B2} and V_{B3} are generated to have maximum output swing, then the output swing of the amplifier at the output node can be expressed as

$$\Rightarrow V_{OUT\_SWING} \leq V_{DD} - (|V_{dsat4}| + |V_{dsat6}| + |V_{dsat8}| + |V_{dsat10}|) \tag{22}$$

where V_{dsati} is the drain to source saturation voltage of transistor Mi.
Approximately 22 can be written as

$$V_{OUT\_SWING} \leq (V_{DD} - 4V_{OV}) \tag{23}$$

where V_{OV} is the overdrive voltage of the transistor

Figure 21 shows the frequency response of the ultra low power amplifier. It has a unity gain bandwidth of 240 kHz and a DC gain of 77 dB. The output voltage swing is nearly 0.3 V and the maximum swing is calculated from total harmonic distortion(THD) analysis. 1 % THD is allowed at the output to determine the swing.

Table 2: Parameters of the designed amplifier

Technology	0.18 μm CMOS
Supply Voltage	1.2 V
Open Loop DC Gain	77 dB
GBW	240 kHz
Pole frequency(C_L=0.1 pF)	40 Hz
Output Voltage Swing	[0.15 V, 0.45 V]
Power	14.46 nW

The settling time of the RFLO loop depends on the settling of the OTA output. Initially the output of the amplifier increases abruptly to 750 mV. The amplifier then settles to 550 mV after number of oscillations. The output voltage of the ultra-low-power amplifier is the control voltage of the VCO. Hence, the VCO runs at frequency of 8.254 kHz at control voltage of 550 mV.

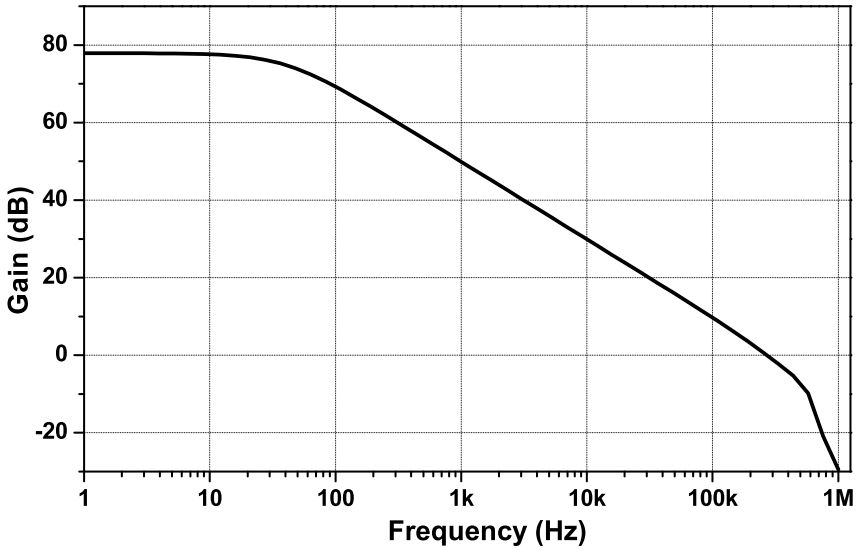

Figure 21: Frequency response of the amplifier

5.3 Voltage Controlled Ring Oscillator

Out of many VCO topologies, the one which is well known for its easy integration into integrated circuit is voltage controlled ring oscillator (VCRO). Phase locked loop(PLL), integrated frequency synthesizer [21],[22], among others are applications where the VCRO is used. A ring oscillator consists of N number of delay stages, with output feedback and in our case value of N is three. Here N is the number of stages providing propagation delay(t_d). In the ideal case, in order for a circuit to work as an oscillator, Barkhausen criteria have to be satisfied: each delay stage must provide π/N phase shifts and the loop gain must be unity. Hence the phase shift provided by loop in VCRO designed here is $\pi/3$. An odd number of delay stages are necessary in a ring oscillator to ensure a proper phase shift. The frequency of oscillation of a ring oscillator is given by [44]

$$f_0 = \frac{1}{2Nt_d} \tag{24}$$

The drain current I_D flowing through the VCRO is given by [46]

$$I_D = N \cdot V_{DD} \cdot C_{total} \cdot f_0 \tag{25}$$

$$\Rightarrow f_0 = \frac{I_D}{N \cdot V_{DD} \cdot C_{total}} \tag{26}$$

where C_{total} is the total gate capacitance of all the transistors in the ring oscillator which is given by

$$C_{total} = \frac{C_{ox}(W_p L_p + W_n L_n)}{2} \tag{27}$$

where C_{ox} is the gate oxide capacitance, W and L are the width and length of the gate of PMOS and NMOS transistors.

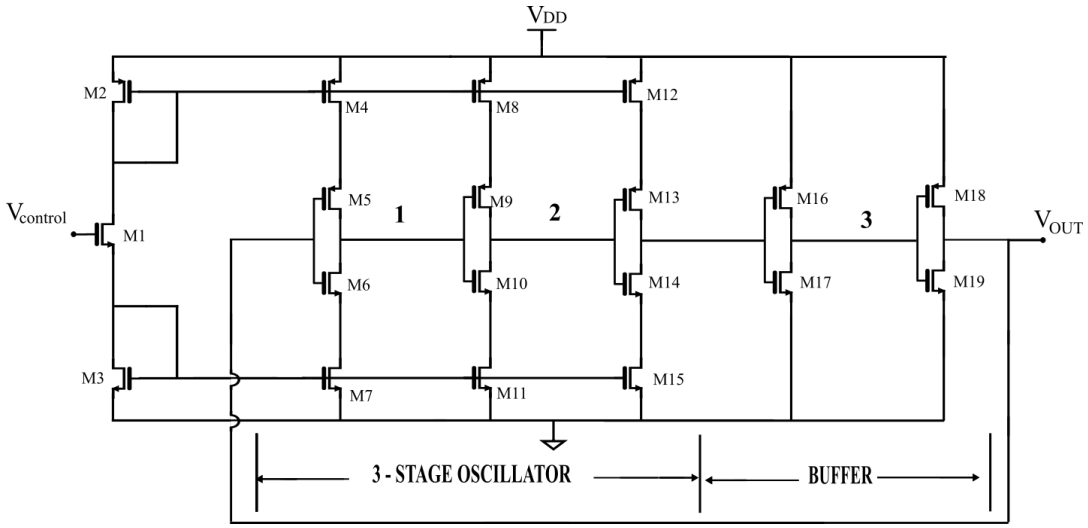

Figure 22: Schematic of voltage controlled current-starved ring oscillator

Figure 22 shows the schematic of voltage controlled current-starved ring oscillator. Here the ring oscillator design consists of three stages of inverters followed by a buffer for slew recovery. The circuit is essentially a current-starved VCRO whose power consumption is 8.01nW at the nominal operating frequency of 8.254 kHz with a control voltage of 550mV. The principle of the working of a current starved VCO is similar to that of a ring oscillator. The PMOS transistor M5 and NMOS transistor M6 in the 3-stage oscillator operate as an inverter whereas the upper PMOS transistor M4 and the lower NMOS transistor M7 operate as current sources. These current sources are mirrored from bias transistors PMOS transistor M2 and NMOS transistor M3 and they limit the current available to the inverter, hence the inverters are starved for current. All the upper PMOS transistors and the lower NMOS transistors in the 3-stage ring oscillator are mirrored from the M2 and M3 transistors in the input of the VCO. The drain current of all the three bias transistors PMOS transistor M1, M2 and NMOS transistor M3 are the same and are controlled by the input control voltage $V_{control}$.

Figure 23 shows the plot of the signal obtained at various nodes of the VCO. In the circuit, the intermediate node within the '3-stage ring oscillator' is the Node 1. The output waveform at this node is an irregular waveform with spikes. The next node within the '3-stage ring oscillator' marked as 2 is the Node 2. The signal available at this node is fed to the buffer which is basically a series connection of two inverters. The waveform obtained in the intermediate node of the buffer (Node 3) is also plotted. Finally, a square-shaped waveform is obtained at the V_{OUT}. The VCO output waveform is almost rectangular in shape which is obtained after the slew recovery buffer at the output of the VCO.

The graphs in Figure 24 and 25 demonstrates various VCO responses with respect

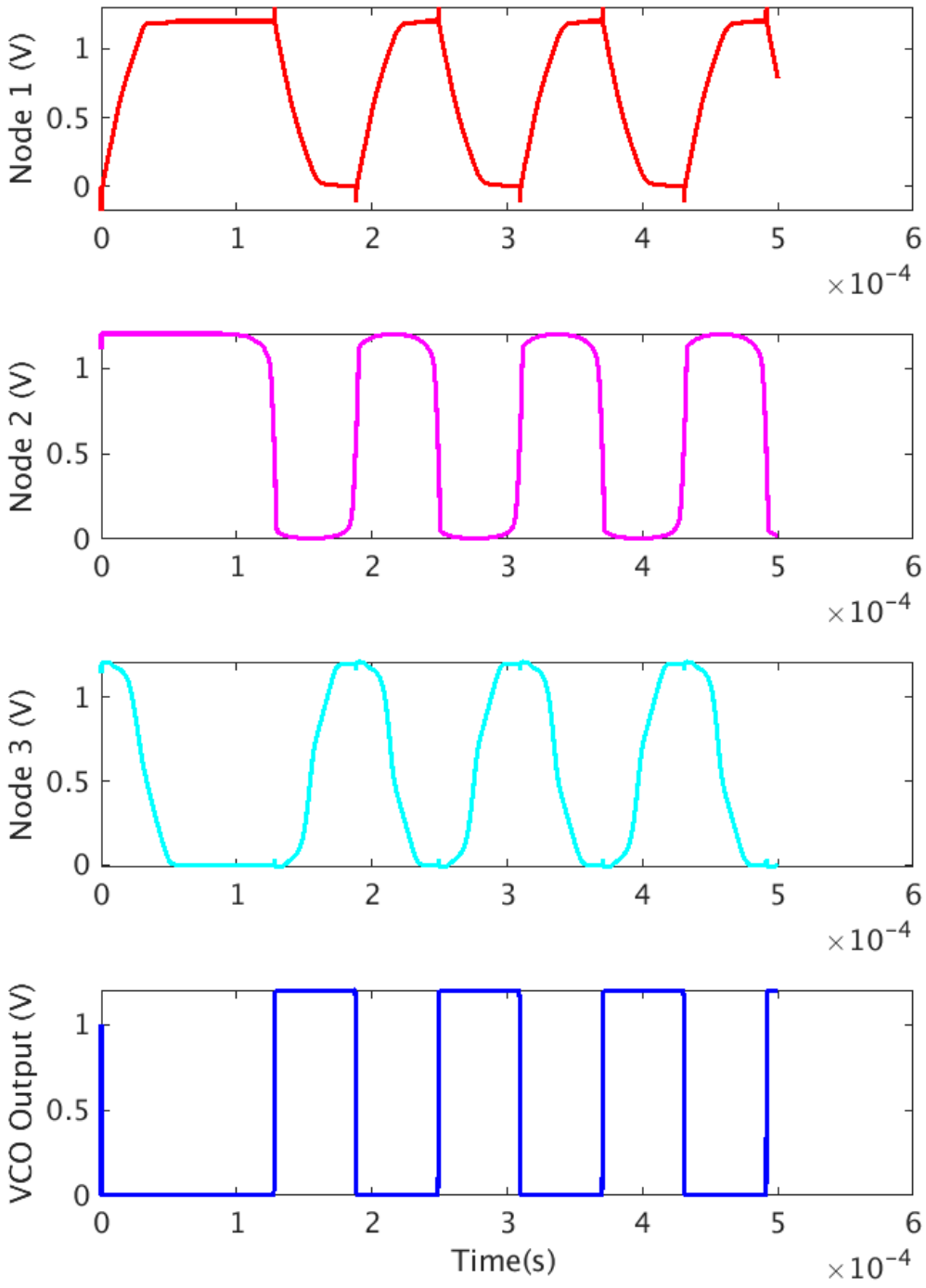

Figure 23: Simulation waveforms obtained from different nodes in the VCO

to control voltage and temperature. In Figure 25, the VCO frequency increases in a non-linear manner as the control voltage is increased. Similarly as the temperature

increases, the VCO frequency of operation also increases. In nominal case, the VCO frequency of operation is 8.254 kHz, with the control voltage at 550 mV. The voltage sensitivity of the oscillation frequency is 97 Hz/mV, which is required for proper working of the RFLO. With a constant 550 mV control voltage, the temperature dependence of the circuit is exponentially increasing such that the VCO is running at 927 Hz at -40°C and 44 kHz at 85°C as depicted in Figure 24.

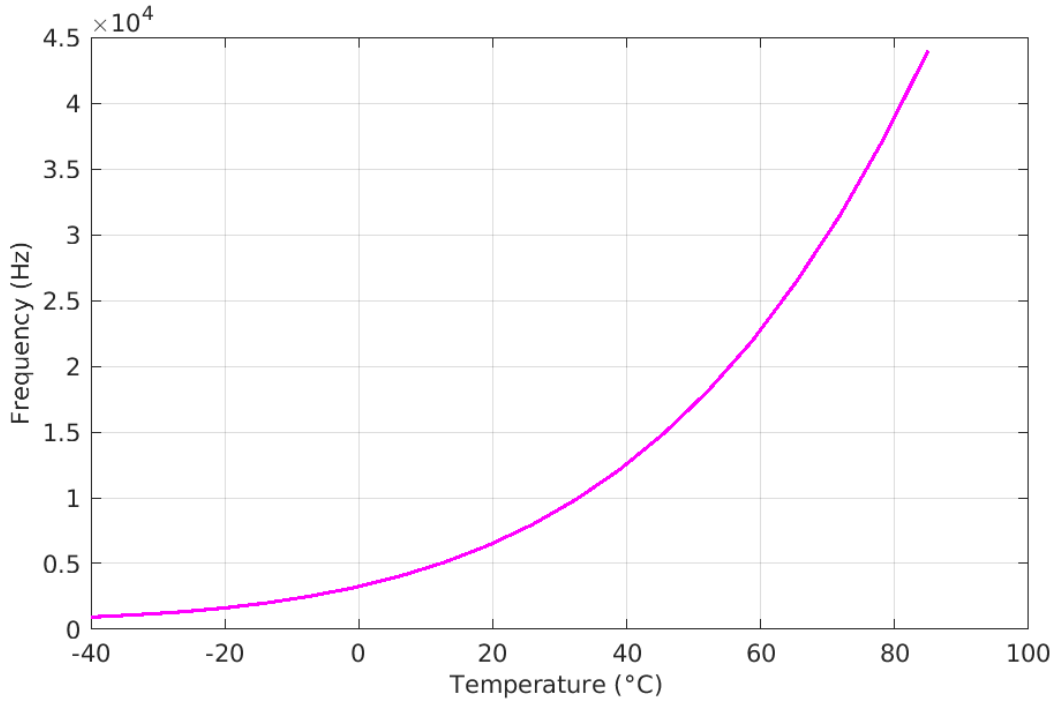

Figure 24: VCO oscillation frequency as function of temperature

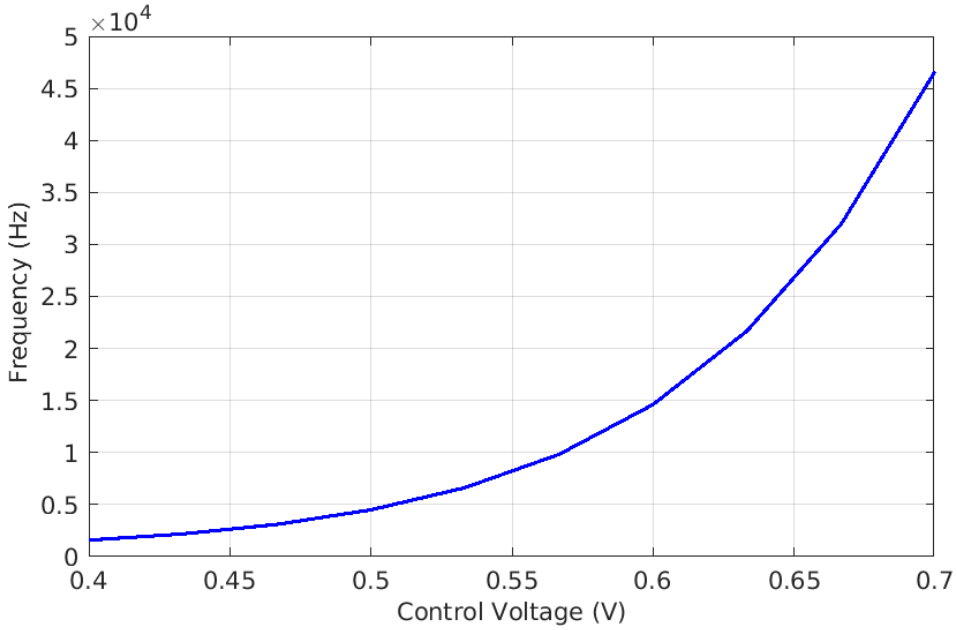

Figure 25: VCO oscillation frequency as function of control voltage

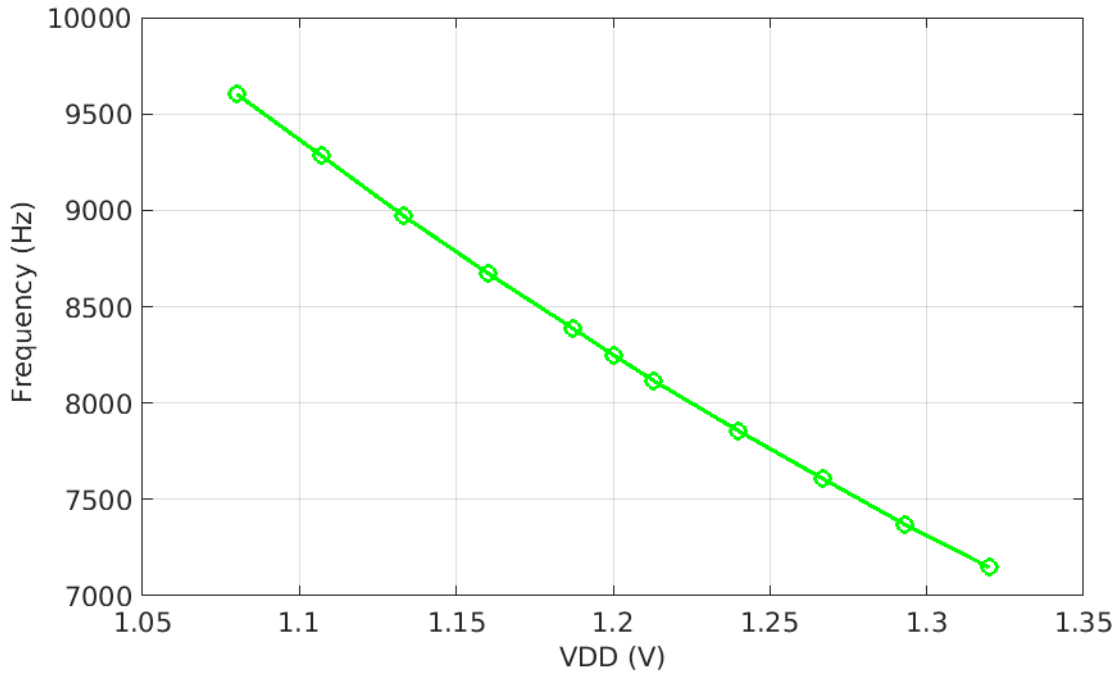

Figure 26: VCO oscillation frequency at different VDD values

The VCO oscillation frequency as fucntion of V_{DD} is shown in Figure 26. As the V_{DD} value increases, the VCO frequency decreases and vice versa. This frequency dependency on V_{DD} is due to the fact that as V_{DD} increases the threshold voltage (V_T) also increases which requires more time to reach that particular threshold. This results in the increase of the propagation delay(t_d) or reduction in frequency of operation (f_0) of VCO (see Equation 24 and 26). The oscillation frequency of the VCO is analysed with the V_{DD} variations of $\pm 10\%$ and the results are shown in Figure 26. The highest clock frequency is attained when V_{DD} is 1.08 V and it's corresponding value is 9.6 kHz. On the other hand, the lowest oscillation frequency of 7.2 kHz is obtained with VDD of 1.32 V.

5.4 Resistor-less Beta Multiplier Bias Current Generator

Figure 27 shows the circuit diagram of the constant current reference circuit is a resistor-less beta multiplier (RBM) circuit [41] that consists of only PMOS and NMOS transistors .The PMOS and NMOS transistors in RBM are mirrored to provide equal bias currents (5 nA) to both the resistor and switched-capacitor branch. The design consumes 27.51 nW of power.

The resistor-less beta multiplier bias current generator is the circuit designed based on a conventional beta multiplier with the resistor replaced with transistors. In Figure 27, transistors M8, M10, M12 and M14 form a diode-connected composite transistor that biases another set of composite transistor formed by M7, M9, M11 and M13. Transistors M7, M9, M11 and M13 operates as a resistor [41], [42]. The

PMOS transistors M0, M1 and M2 have equal W and L dimensions, thus in the all three branches, there flows an equal amount of current. The PMOS transistors M3 and M4 have equal dimensions which are ratioed with the other PMOS transistors of RBM to provide a current of 5 nA in the two branches. Hence,

$$I_{REF1} = I_{REF2} = 5\ nA \tag{28}$$

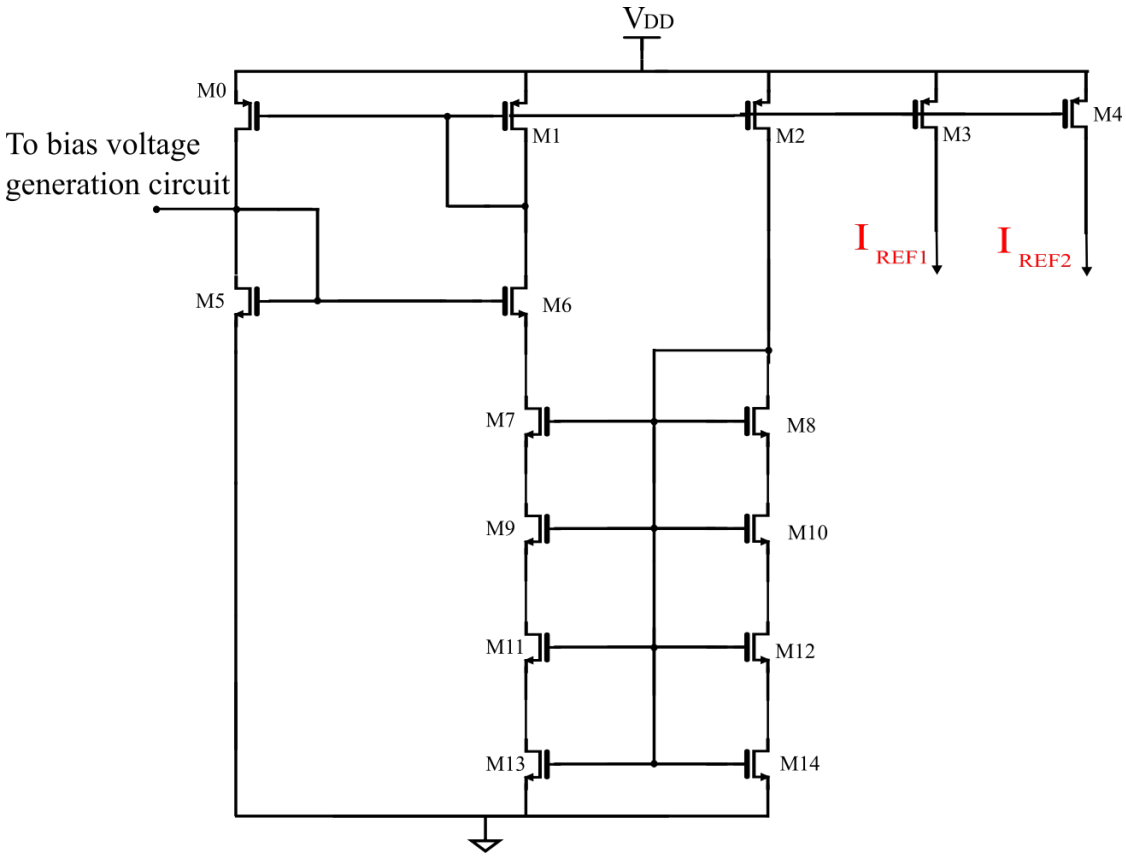

Figure 27: Schematic of constant current reference circuit

The variations in the current provided by the resistor-less beta multiplier bias current generator across temperature for different V_{DD} values are shown in the graph of Figure 28. As the V_{DD} value increases the curve drifts up which implies more current flow. Any change in V_{DD} causes changes in I_{REF1} and I_{REF2} values. However, since both the mirrored PMOS transistors M3 and M4 (Figure 27) are equally dimensioned, any process, voltage and temperature (PVT) variations will effect both PMOS transitors in the same manner. This will in turn results in the same changes I_{REF1} and I_{REF2} and thus resulting in cancelling out the effect of changes in the reference voltage reaching the input of the amplifier.

The circuit diagram with RFLO incorporating bias current generator is shown in Figure 29. The two PMOS transistors M0 and M1 are mirrored with PMOS transistors in bias current generator.

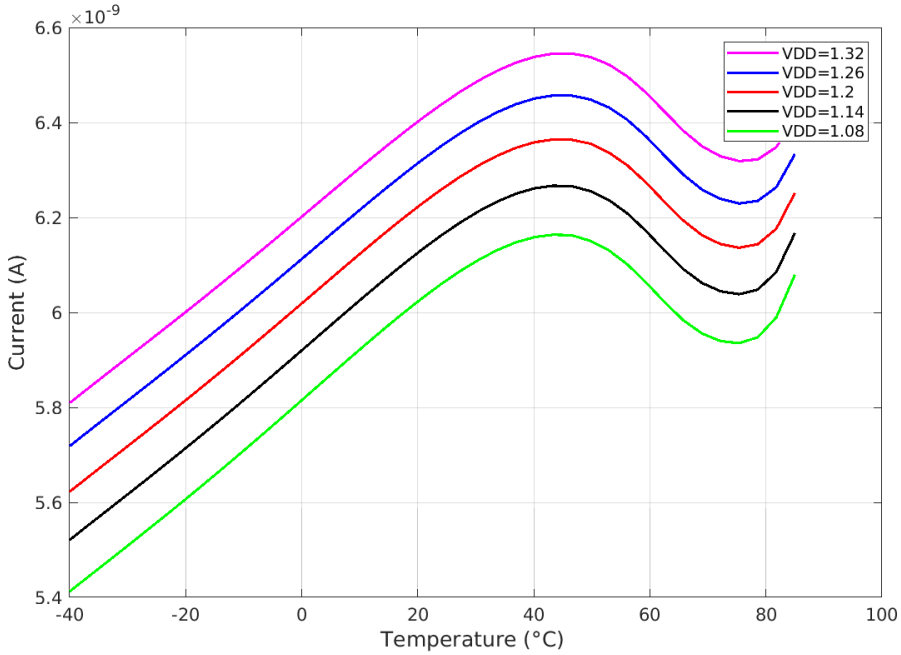

Figure 28: Current versus temperature plot of current reference for various VDD values

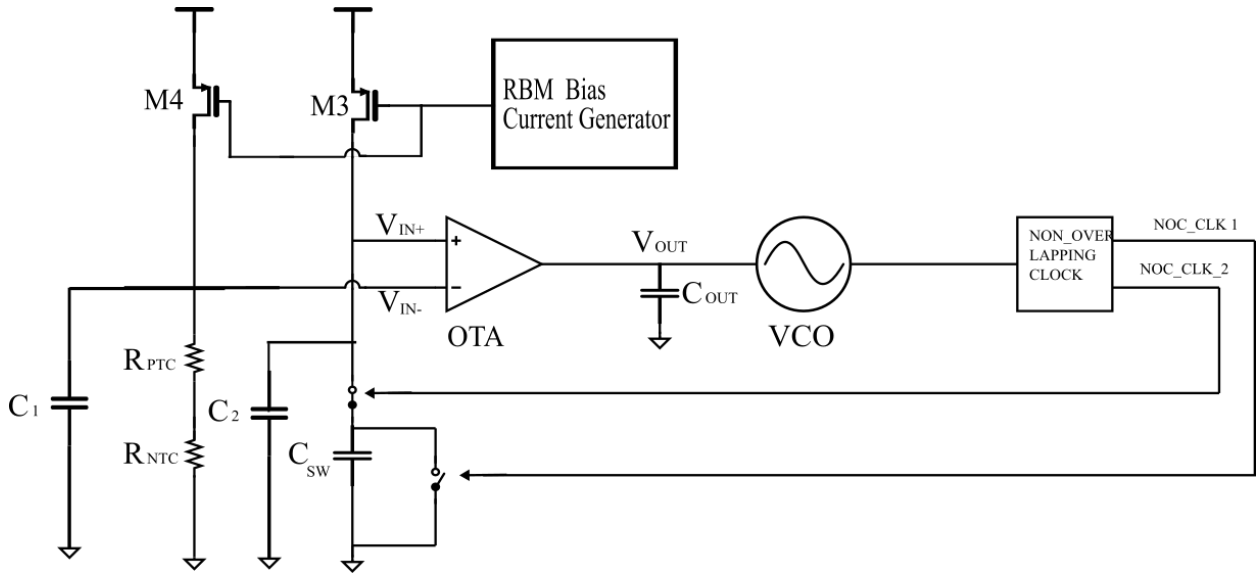

Figure 29: Schematic of RFLO incorporating RBM

5.5 Bias Voltage Generator for Ultra-low-power Amplifier

The ultra-low-power amplifier discussed in section 5.2 requires bias voltages V_{B1}, V_{B2} and V_{B3} for its operation (see Figure 20) [7]. These three bias voltages are generated by a bias voltage generator which essentially consists of only PMOS and NMOS transistors and associated current sources as shown in Figure 30. The PMOS transistors and NMOS transistors are stacked separately to develop appropriate voltage across each transistor stacking. The bias voltages are generated from bias voltage generator is applied to the gates of the transistors in the ultra-low-power amplifier (see Figure 20). V_{B1} is applied to the gate of the transistors M3, M4 and M11 and V_{B2} is applied to the gate of the transistors M5 and M6 that are used for biasing the amplifier. Similarly V_{B3} is applied to the gate of the transistors M7 and M8 of the amplifier. Since PMOS transistors of the amplifier is biased by bias voltage generated from stacking PMOS transistor (see Figure 30), any process variation which causes the change in bias voltage will have same effect on transistors of both bias voltage generator and the amplifier, hence resulting in cancellation of their effects. In other words, bias voltages required by the transistors and generated by the bias network increase or decrease simultaneously based upon the PVT variations. Same cancelling effect is present with the NMOS transistor stacking. The generated bias voltages V_{B1}, V_{B2} and V_{B3} are 900 mV, 300 mV and 400 mV respectively. The bias currents of 1 nA and 3.5 nA are provided by the current reference circuit discussed in section 5.4.

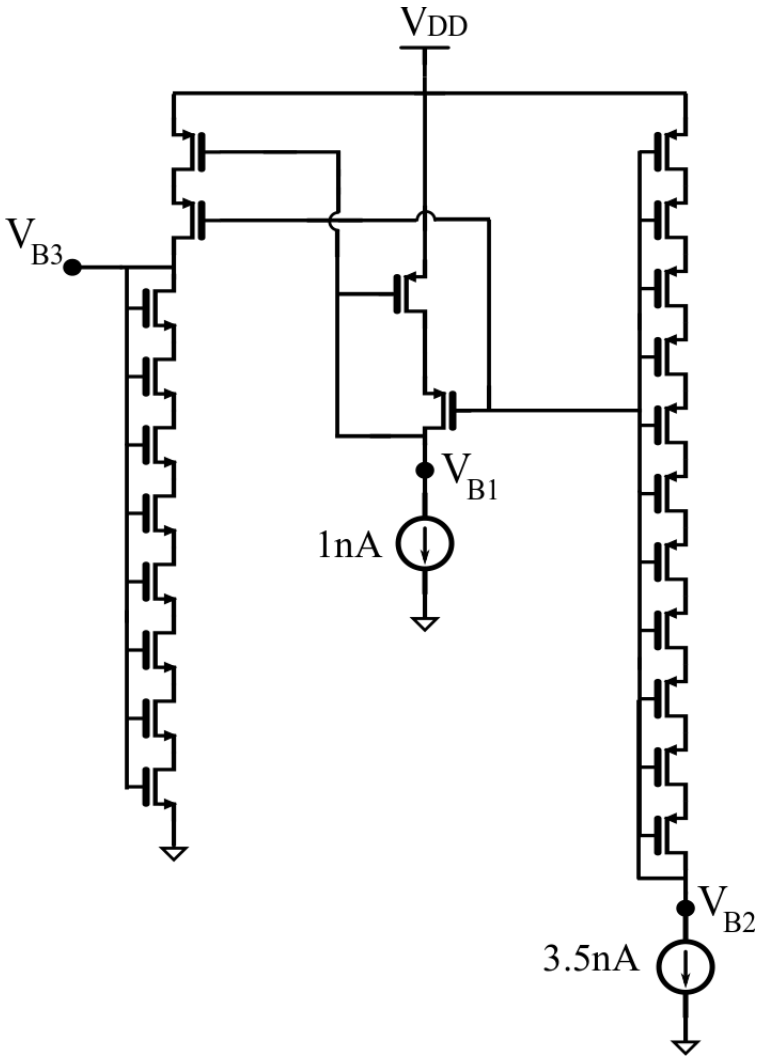

Figure 30: Bias voltage generation circuit [7]

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5.6 Simulation Results of the Wake-up Clock

Based upon the value of reference resistor and switched capacitor, the wake-up clock operates at different frequency resulting in different power consumption for each frequency of operation. For different values of operating frequency F_{OUT} , the power consumed and layout area is listed in Table 3. It is clear from the Table 3 that higher the frequency, higher the power it consumes but taking a lesser layout area. After careful consideration of F_{OUT}, power and area trade-off, the proposed design is the one with F_{OUT} of 8.254kHz, power of 70.4nW and layout area of $153318\mu m^2$

Table 3: Table showing F_{OUT}, power and area trade-off of the wake-up clock

R(MΩ)	C_{SW}**(pF)**	F_{OUT} **(kHz)**	**Power Consumption (nW)**	**Area** (μm^2)
30	4	8.254	70.4	153318
15	4	16.508	84.83	107193
15	2	33.016	112.3	83681
7.5	2	66.032	166.9	60618

One of the main performance parameter of wake-up clock is the temperature stability of the oscillation frequency which is expressed in terms of ppm/°C. Ideally this value should be zero. The temperature stability of the proposed start-up timer is 7.35 ppm/°C. The temperature coefficient of the clock is simulated in the range of -40°C to 75°C is just 7.35 ppm/°C, but the clock frequency decreases abruptly from 75°C to 85°C. This is depicted in Figure 31.

The initial unstable clock output at start-up can be seen in Figure 32 followed by a stable clock after settling time as shown in Figure 33. The settling time of the timer solely depends upon the time it takes for the amplifier output to become stable, which in turn depends upon the dominant pole of the amplifier. The amplifier which is operational transconductance amplifier have the dominant pole determined by the amplifier output impedance and the output capacitor C_{OUT} (see Figure 6). Once the clock output is stable, the only source of frequency variation is from the temperature dependency of the components; especially the reference resistor and the switched-capacitor circuit.

The proposed resistive frequency locked loop oscillator design takes around 12 ms to provide a stable clock signal, which is depicted in Figure 34. Initially the clock frequency rises as high as 80 kHz which then drops and settles to 8.254 kHz.

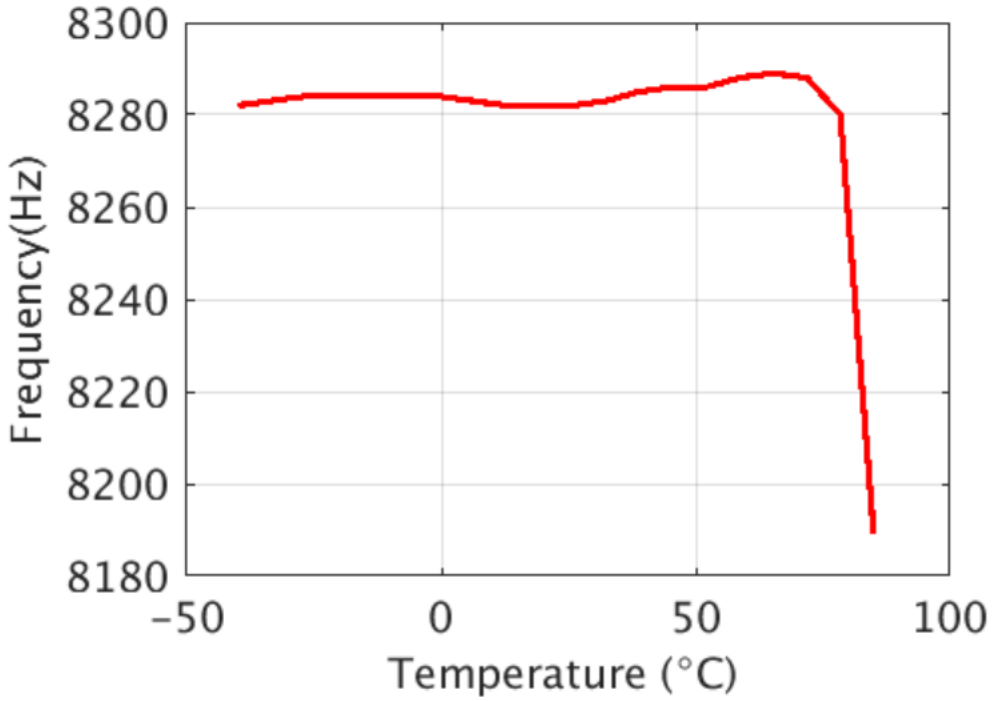

Figure 31: Temperature stability plot of wake-up clock

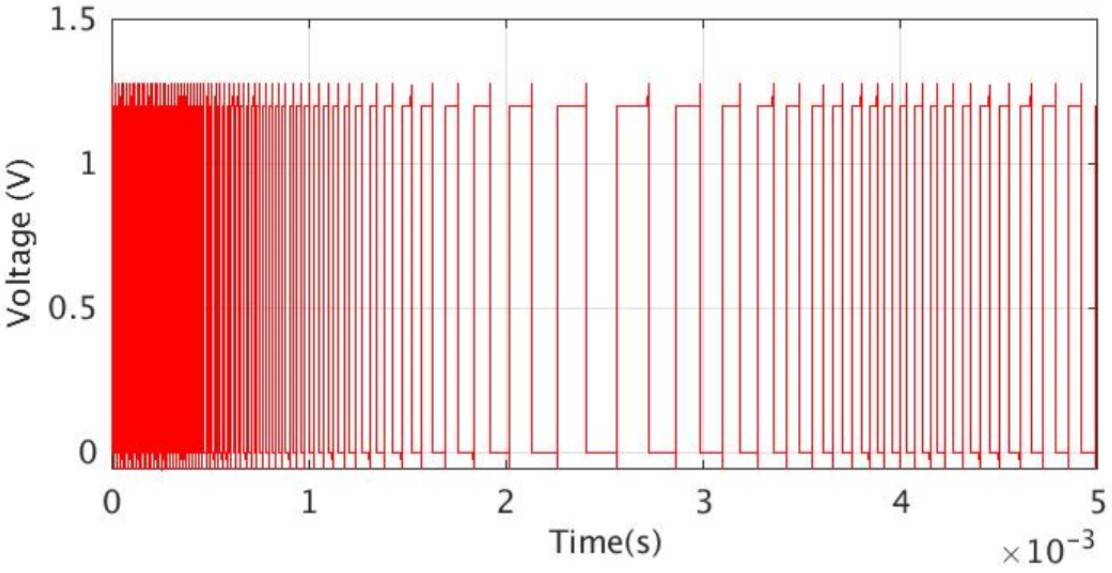

Figure 32: Clock waveform before settling time

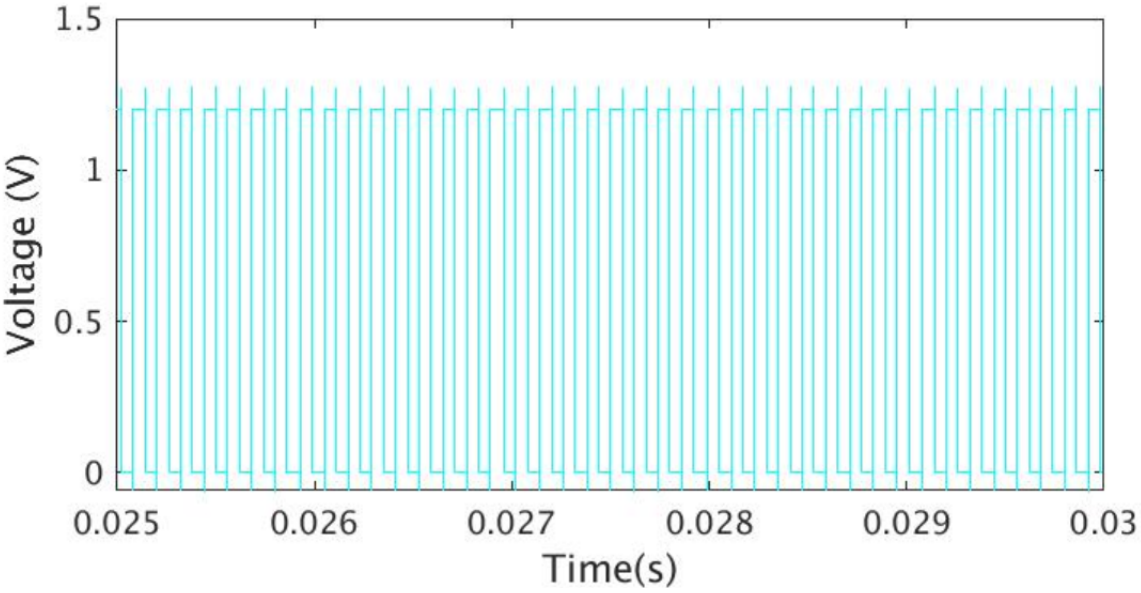

Figure 33: Stable clock signal of the proposed oscillator

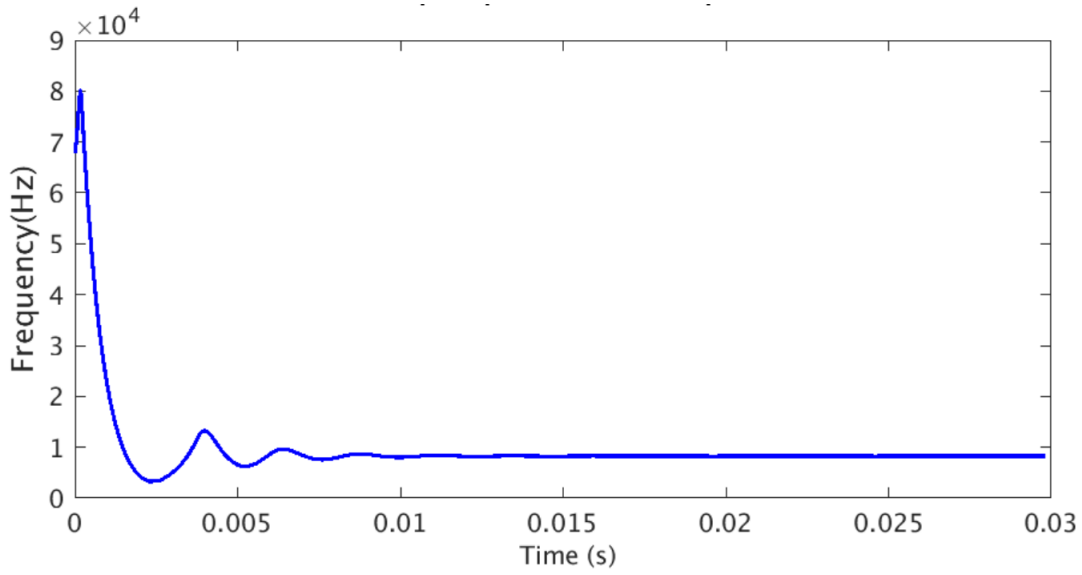

Figure 34: Start-up response of wake-up timer

Table 4: Performance characteristics of the proposed wake-up clock.

Frequency of Operation	8.254 kHz
Power Consumption	70.4 nW
Temperature Stability	7.35 ppm/°C
Temperature Range	-40°C to 75°C
Start-up Time	12.5 ms
Energy/Cycle	8.53 pJ/Cycle
Line Sensitivity	0.073 %/ΔV
Layout Area	0.153 mm^2

The simulation results of the designed ultra-low-power wake-up clock is shown in Table 4. The clock running at 8.254 kHz consumes only 70.4 nW at the room temperature. The energy per cycle E is given by

$$E = \frac{P}{F_{OUT}} \tag{29}$$

where P is the power consumed by the RFLO. The value of E for the designed RFLO is 8.53 pJ/Cycle. The layout area for the whole design is 0.153 mm^2, which will be discussed in upcoming section.

The pie-chart in Figure 35 represents the relative power consumed by each sub-block. Around 30 nW power is consumed by the resistor-less beta multiplier bias current generator and the bias voltage generation circuit. The amount of power consumed by the ultra-low-power OTA is 16.32 nW and the non-overlapping clock generator consumes 16.14 nW. The least amount of power is consumed by the VCO which is 8.01 nW. The power consumption of each circuit block is listed in Table 5.

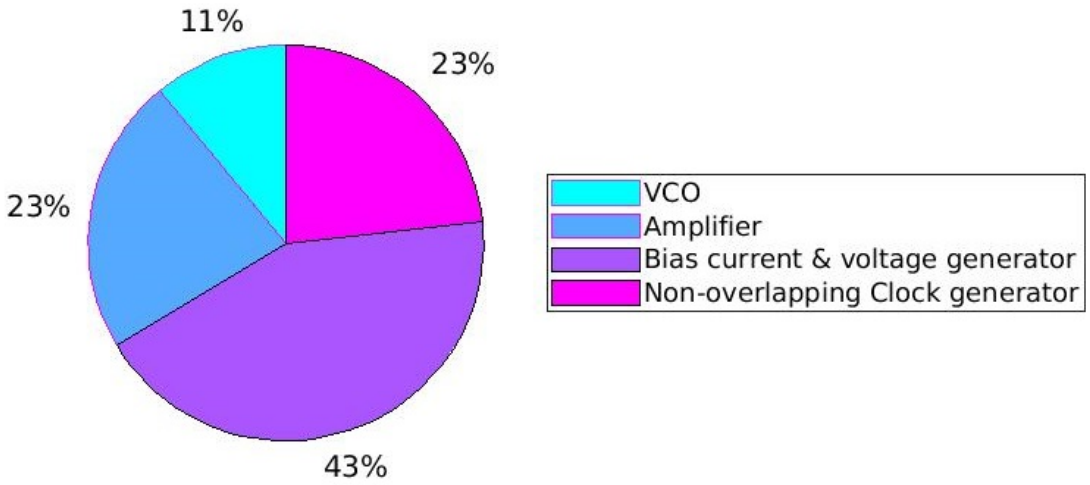

Figure 35: Relative power consumption of each circuit block

The relative deviation from the nominal output frequency for different VDD values is shown in Figure 36. The output clock frequency increases when the VDD is

Table 5: Power consumption of each circuit block of the wake-up clock

SL No.	Block Name	Power Consumption (nW)
1	VCO	8.01
2	Amplifier	16.32
3	RBM	29.93
4	NOC	16.14
5	**Total**	**70.4**

increased and vice versa. The ±10 % variation in VDD is considered here. The line sensitivity of the RFLO is given by

$$Line\ Sensitivity(\%/\Delta V) = \left(\frac{\frac{F_{OUT.MAX}-F_{OUT.MIN}}{F_{OUT}}}{\Delta V}\right) \cdot 100 \tag{30}$$

where $F_{OUT.MAX}$ is the maximum frequency of F_{OUT} and $F_{OUT.MIN}$ is the minimum frequency of F_{OUT}. Here the $F_{OUT.MAX}$ is 8.257 kHz at 10% higher V_{DD} of 1.32 V. The minimum F_{OUT} is 8.250 kHz at 10% lower V_{DD} of 1.04 V. The line sensitivity of the RFLO is 0.073 %/ ΔV.

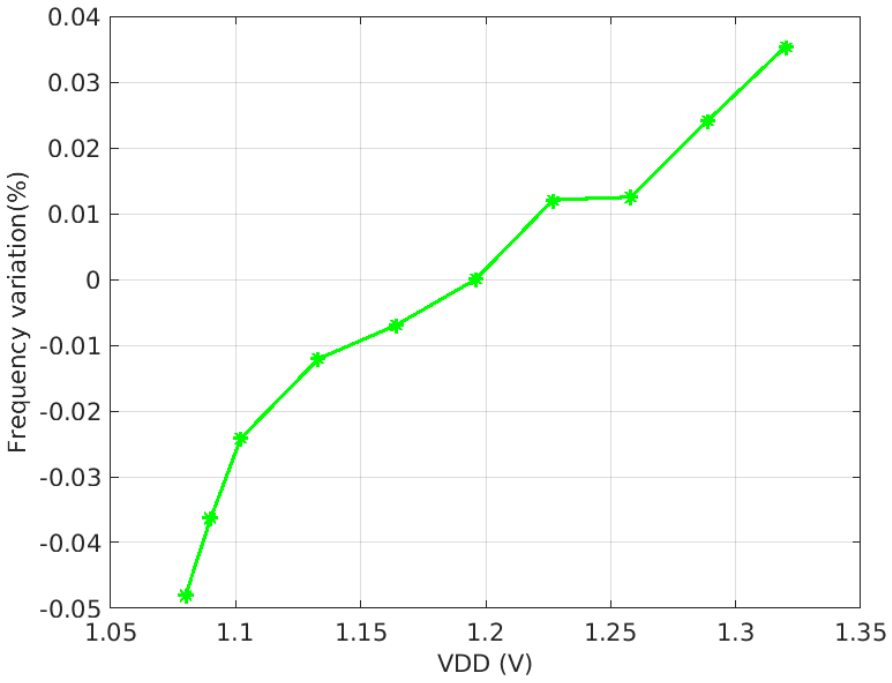

Figure 36: Percentage variation of clock frequency with respect to VDD

Figure 37 shows the power consumption of RFLO across the temperature and for the different VDD values. As can be seen from the graph, the power consumption

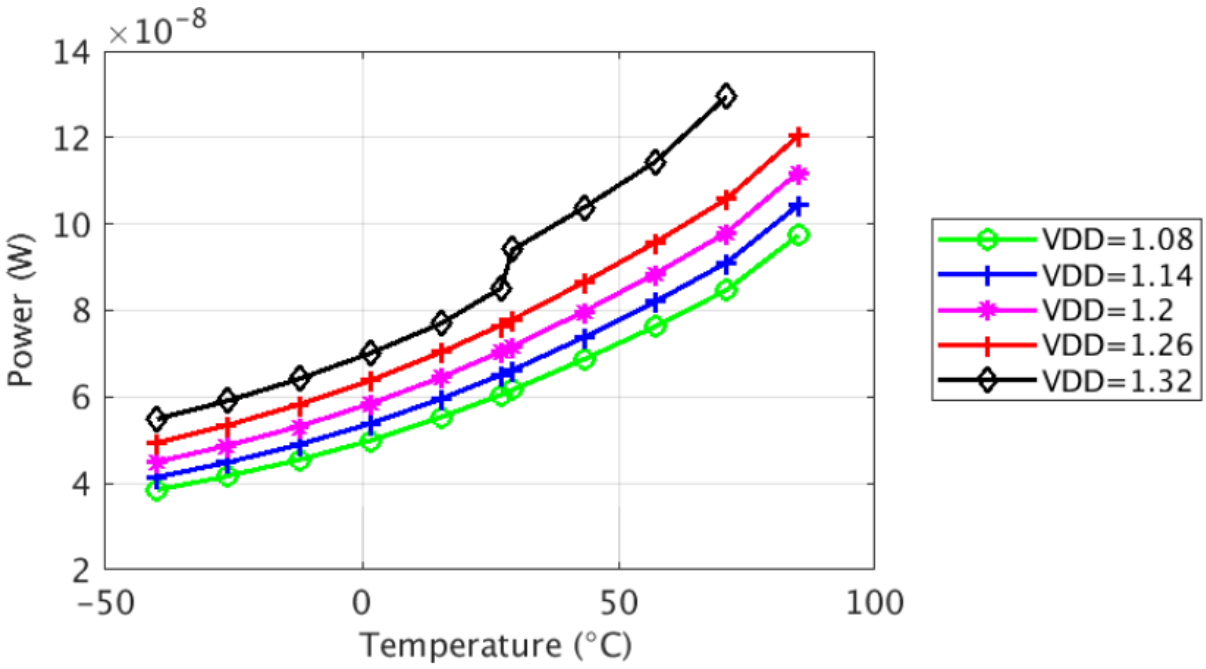

Figure 37: Power consumption of the wake-up as function of temperature

Table 6: Clock frequency at different CMOS process corner

CMOS Corner	F_{OUT} **(kHz)**
CMOS Typical Mean	8.254
CMOS Worst Speed	8.324
CMOS Worst Zero	8.256
CMOS Worst One	8.251
CMOS Worst Power	8.184
CMOS Very Slow	8.393
CMOS Very Fast	8.095

of the wake-up clock increases as the temperature rises. Similarly, increase in VDD values also increases the power consumption.

The resistive frequency locked oscillator (RFLO) has been simulated in various process corners. Table 6 shows various corners and corresponding clock frequency. At typical process corner, the clock frequency is 8.254 kHz. All previous simulations were conducted in typical mean corner. The largest frequency deviation is found in the fast NMOS and fast PMOS corner with a value of 8.095 kHz, the frequency difference of 159 Hz from the nominal value. In the fast NMOS and fast PMOS corner, both the PMOS and NMOS transistors consumes higher power than in the nominal case, and it operates with the lower temperature and the lower threshold voltage. This corner is indicated as 'CMOS Very Fast' in Table 6 and frequency of operation of the wake-up clock is 8.095kHz at this corner. The corner wherein the

operating conditions are set just opposite to the fast NMOS and fast PMOS corner is the slow NMOS and slow PMOS corner (CMOS Very Slow). This corner is found to show the second worst frequency deviation (0.139 kHz) with clock frequency of the 8.393 kHz. The proposed design is also simulated in different R and C corners and the resulting frequency of operation F_{OUT} is listed in Table 7.

Table 7: Clock frequency at different R and C process corners

R and C Corners	F_{OUT} **(kHz)**
R, C Typical Mean	8.254
C Worst Power	9.001
C Worst Speed	7.609
R Worst Power	9.57
R Worst Speed	7.337
R, C Worst Power	10.43
R, C Worst Speed	6.763

Comparison of the characteristics of the designed oscillator with those of other state-of-the-art designs provided in the reference section is given in Table 8. The proposed clock is designed with a 180 nm CMOS technology. The design proposed in the reference [12] consumes less power compared to this design at the cost of lower frequency of operation. The design presented in [11] has a layout area as low as 0.032 mm^2, but the power consumption is 120 nW which is higher compared to this design. The design [35] takes only $0.08mm^2$, but the other performance parameters such as power consumption and temperature stability are not good for the design. For the given range of the temperature, the temperature coefficient for the proposed wake-up clock is the least among all the designs provided in Table. Reference design [7] have specifications similar to the proposed design. The only performance parameters that is worse is the start-up time which is 12.5 ms in the proposed design, whereas in the other designs it is less than 2.5 ms.

5.7 Layout

The layout has been drawn and the post layout simulations for the RFLO have been performed. Figure 38, 39 and 40 show the layout of the amplifier, the bias voltage generation circuit and the voltage-controlled oscillator respectively. The overall layout of the wake-up clock is shown in Figure 41.

From the pie-chart shown in Figure 42, the largest area of the layout is taken by reference resistors which is 60% of the total layout area. The layout area covered by the ultra-low-power amplifier, the VCO and the bias circuit is only 1% each. The second largest area after the resistor is taken by the averaging capacitors(C) in the reference circuits. Large area in the layout is also taken by load capacitor of the ultra-low-power amplifier. Table 9 lists the layout area taken by each block. The area taken for routing is included as can be seen from the table. The overall circuit diagram of the proposed resistive frequency locked oscillator is shown in Figure 43.

Table 8: Comparison of the simulation results with other state-of-the-art designs

	This work	***[7]***	***[10]***	***[11]***	***[12]***	***[35]***
Process(nm)	**180**	180	90	65	180	350
Power (nW)	**70.4**	110	280	120	5.8	180000
Frequency(kHz)	**8.254**	70.4	100	18.5	0.011	30000
TC (ppm/°C)	**7.35**	34.3	13600	22	45	90
Area(mm^2)	**0.153**	0.26	0.12	0.032	0.24	0.08
Start-up Time(ms)	**12.5**	<2.5	0.01	N/A	N/A	N/A
Temperature Range (°C)	**-40/+75**	-40/+80	-40/+90	0/+90	-10/+90	-20/+100
Line Sensitivity (%/ΔV)	**0.073**	0.75	0.82	1	1	4

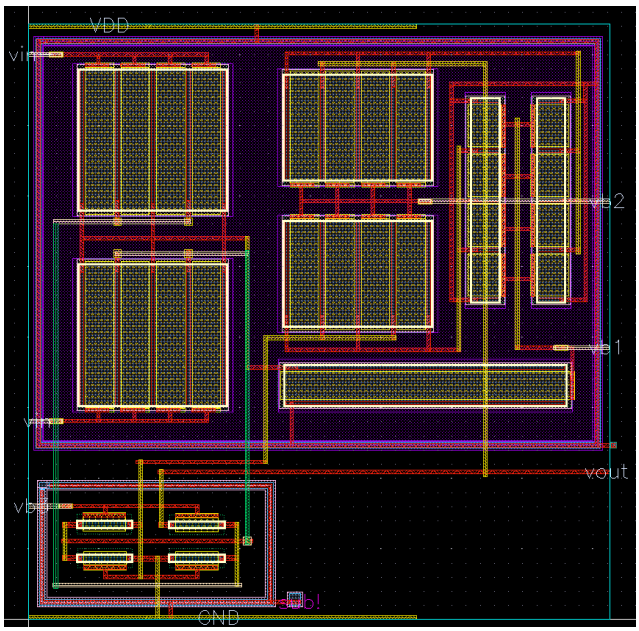

Figure 38: Layout of the amplifier

The output port from where the output clock signal of 8.254 kHz is available is indicated with a red box.

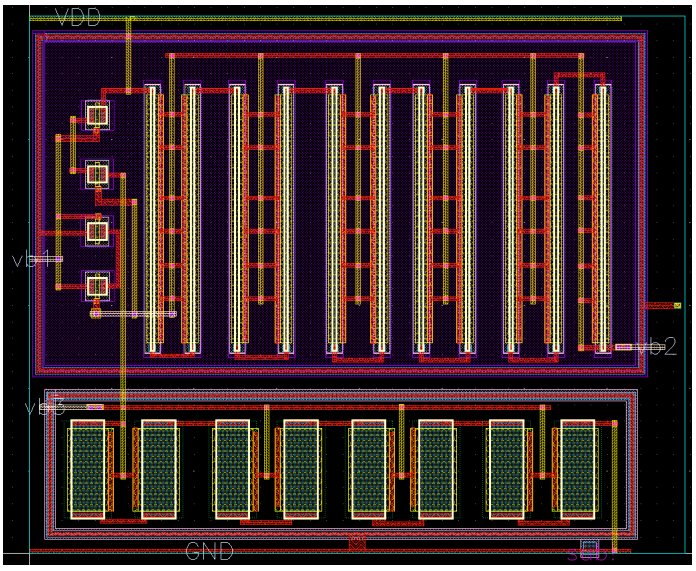

Figure 39: Layout of the bias voltage generation circuit

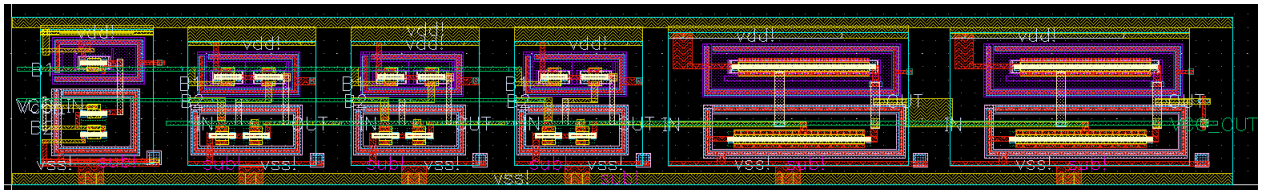

Figure 40: Layout of VCO

Table 9: Table showing layout area of each circuit block of the wake-up clock

SL No.	**Block/Component Name**	**Area (μm^2)**
1	Amplifier	1522
2	Bias	1184
3	VCO	1128
4	Current Reference	5400
5	Clock	2310
6	Capacitors	47024
7	Resistors	92250
8	Routing Overlead	1250
	Total Area	**153318**

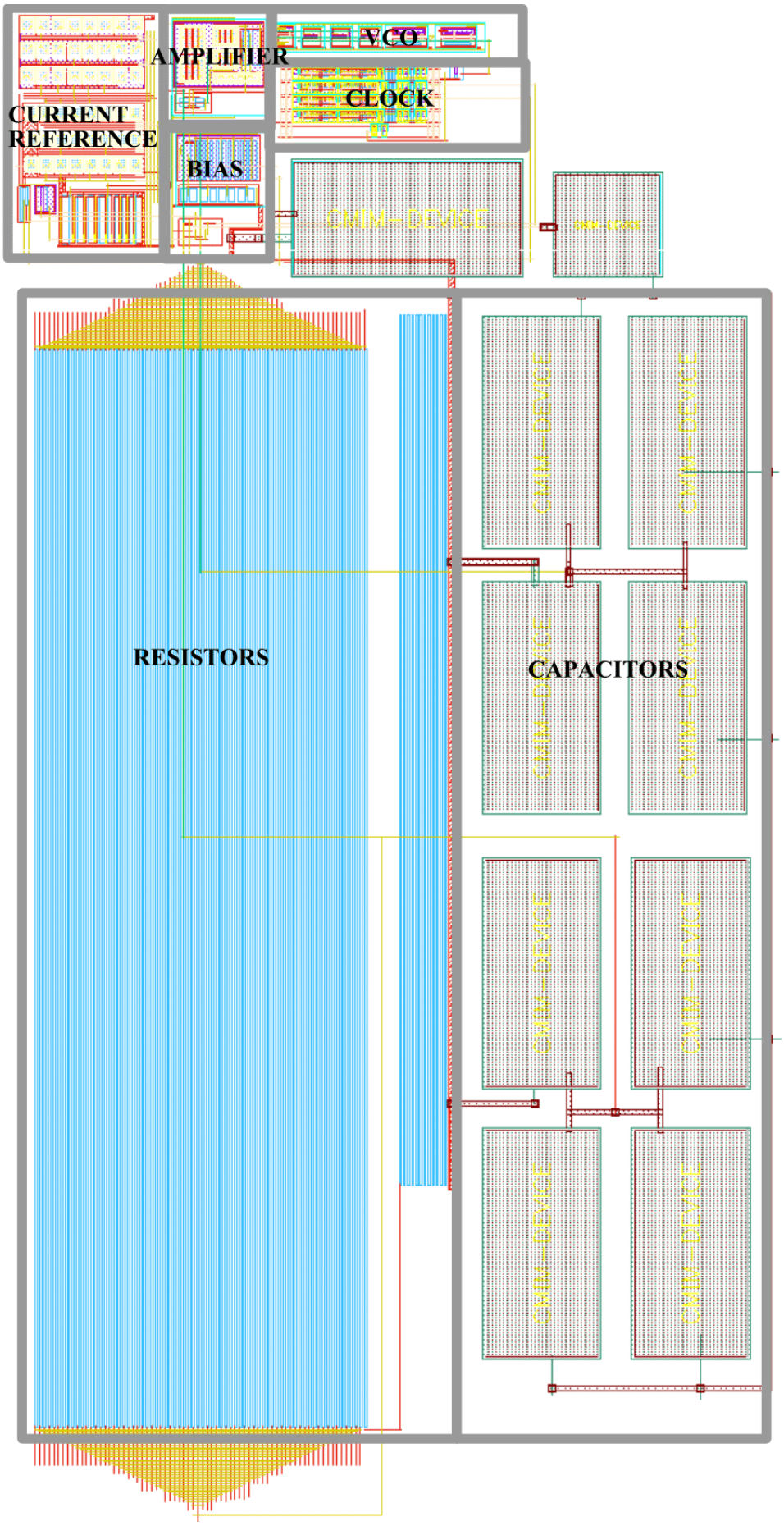

Figure 41: Layout of the wake-up clock

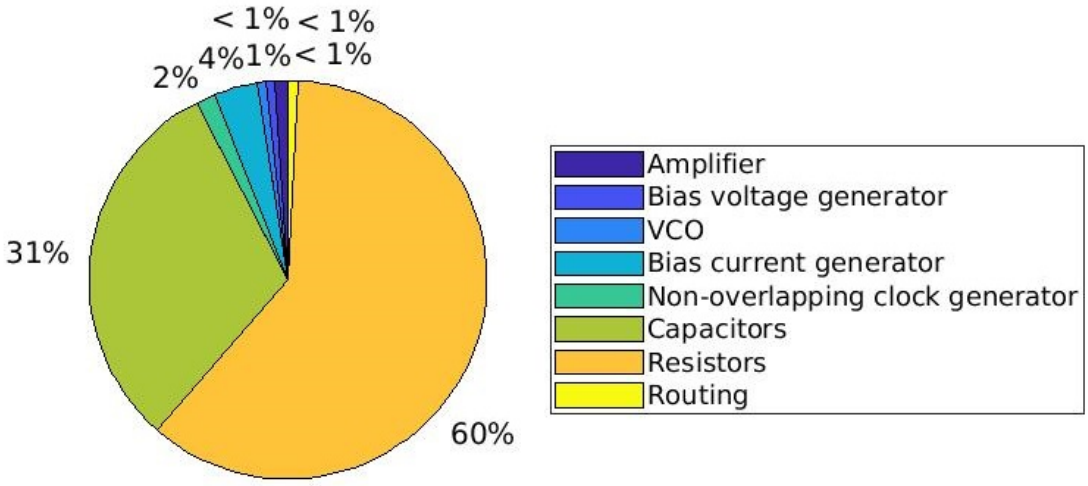

Figure 42: Chart showing relative layout area of each block

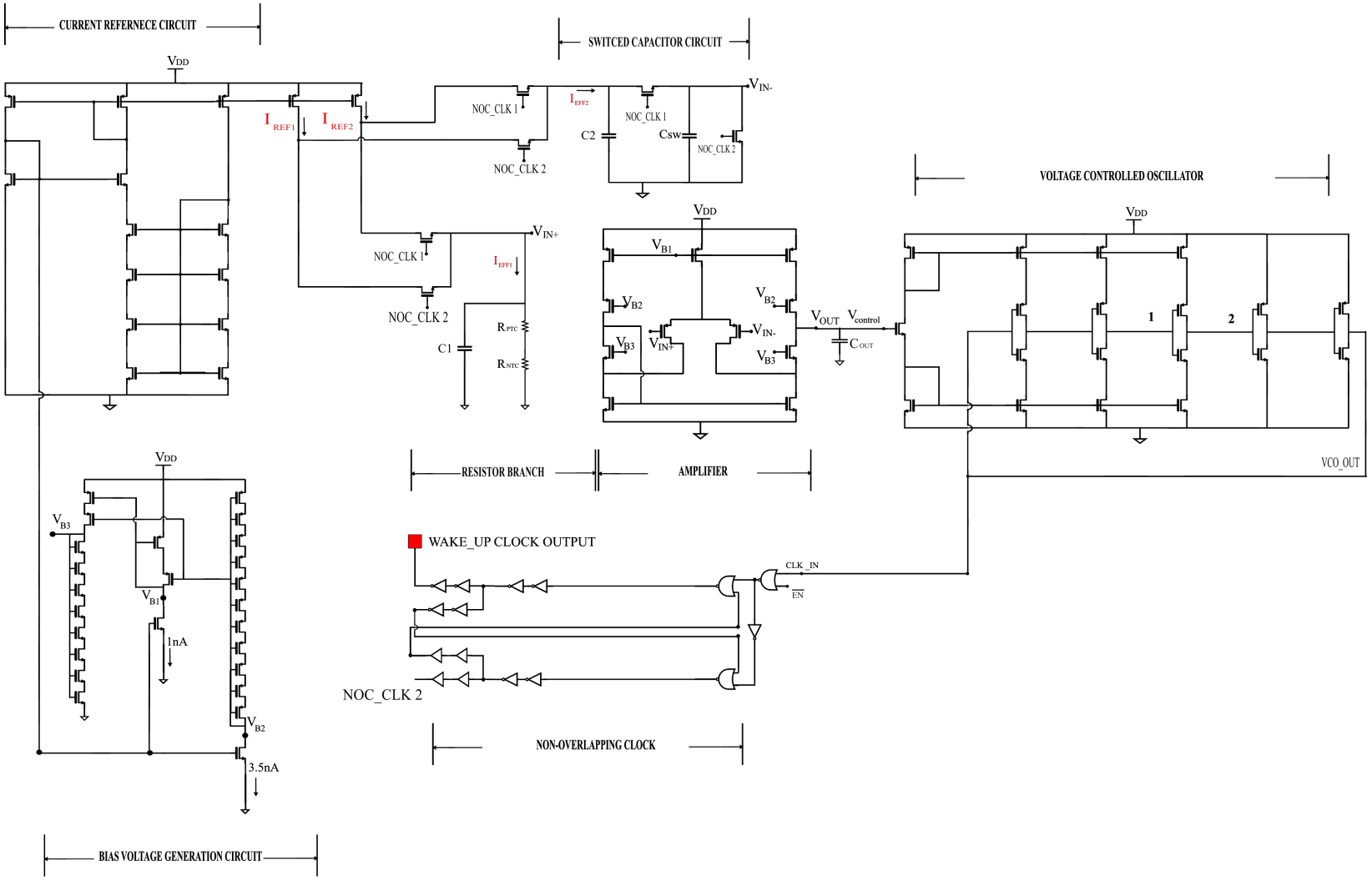

Figure 43: Circuit Diagram of Ultra-low-power Wake-up Clock

6 Conclusion

This thesis has presented the design and analysis of an ultra-low-power wake-up clock for SoC applications in a $0.18\mu m$ CMOS process. This is used to provide the low-power clock signal to the circuitry, especially when it is sleep mode. The designed ultra-low-power circuit includes an operational transconductance amplifier (OTA), a current-starved voltage controlled oscillator (VCO), a non-overlapping clock generator, a bias reference current generator and a bias voltage generation circuit. The layouts for all the sub-blocks were drawn, and the post-layout simulations were carried out.

The proposed topology replaces the power-hungry comparator in the conventional RC relaxation oscillator with an ultra-low-power amplifier. The comparator is also a main source of temperature instability in conventional designs. A combination of a positive temperature coefficient (PTC) resistor and a negative temperature coefficient (NTC) resistor are connected in series and the voltage drop across it provides the reference voltage for the wake-up clock. A p type resistor and an n type resistor are used for this purpose. The series connection of resistors have temperature stability of 0.0027 ppm/°C resulting in increasing the overall clock stability with respect to temperature. The ultra-low-power amplifier, the VCO and the non-overlapping clock generator along with the switched-capacitor circuit forms a frequency-locked feedback loop producing a temperature-compensated clock signal. The current reference generator circuit employed here is a resistor-less beta multiplier based current reference circuit. Any mismatch between the currents in the two nodes is compensated by current chopping technique employed.

The designed resistive frequency locked oscillator (RFLO) produces an 8.254 kHz clock with an average temperature coefficient of 7.35 ppm/°C in the -40 °C to 75 °C temperature range. The RFLO is shown to have a line sensitivity of 0.073 %/V with variation of ±10%. The proposed wake-up clock consumes only 70 nW power at the room temperature. The design takes the layout area of 0.153 mm^2 with the resistor covering 61% of the total layout area. This frequency locked loop (FLL) based design has a start-up time of around 12 ms. The energy per cycle for the clock is 8.53 pJ/cycle. As the design avoids external components, it is suited for fully integrated System-On-Chip (SoC) applications.

Out of many possible design improvements, two of them are very relevant. Firstly, as we discussed in the above section, the major part of the layout area is consumed by the reference resistors and hence, replacing this temperature-compensated reference with MOS based process, voltage and temperature (PVT) invariant reference circuit would reduce the layout area drastically. Another improvement on the current design is employing capacitor-trimming technique, the switched-capacitor in the input of the ultra-low-power amplifier is connected in parallel and switched to generate different clock signals. As the resultant switched-capacitor value increases, the frequency of the clock decreases and vice versa. Hence, the same clock could be used as a wake-up clock as well as a system clock. The stability is also improved by this technique when the RFLO is operated to generate higher frequency clock signal.

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