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SAN SEBASTIÁN

Low-power frequency-conversion based temperature sensor for long-range passive RFID sensor applications

A Bachelor Thesis submitted for the degree of

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Abstract

A low-power frequency-conversion based temperature sensor interface optimized for passive UHF RFID applications have been designed and implemented. The interface is based on a reference capacitor that is charged by a temperature dependent current and discharged by a hysteresis loop. The circuit has been implemented in a standard CMOS 180nm process. The post-layout simulations show that the presented architecture is able to compensate for variations on the bandgap reference and cover a wide temperature range (140°C) with minimum active area ($0.019mm^2$), reduced power consumption ($\cong 6.5\mu W$), and reduced effect of PVT variations, accomplishing the design objectives.

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Chapter 1

Introduction

Bar code systems are worldwide known for their use in object identification: a reader scans the code and extracts some information. Nowadays, they are being replaced by UHF Radio-frequency identification (RFID) systems, which can be considered as the evolution of bar codes. The main difference between these two technologies is that bar codes need a direct line-of-sight between the tag and the reader, whereas RFID readers can detect a tag between a wide distance range. Furthermore, bar codes store a fix information that cannot be changed, while with RFID tags can be programmed many times to change the sending information.

The different parts that form RFID systems are shown in the Fig. 1-1. There are also different types of tags, however the passive ones are the most attractive solutions as they do not have any power source. There are different methods to provide power to the tag, but they are mostly activated by the waves the reader is sending.

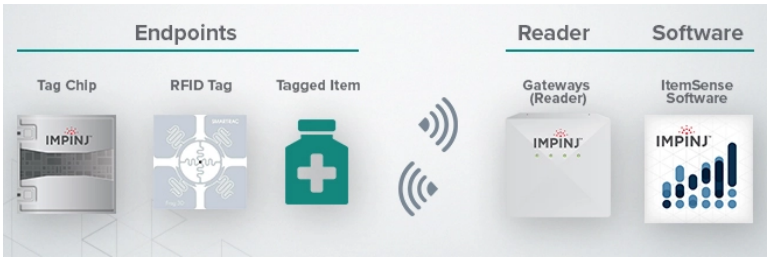

Figure 1-1: RFID systems

One of the main advantages is the multiple application areas of RFID systems. Their main application field is the Industry 4.0. They have been one of the most important factors in its evolution, as they are being used for many purposes like process monitoring or inventory management. They are also being integrated in other fields like in the aerospace or medical sectors and nowadays, there are even some projects using RFID solutions in the agricultural sector. This has lead to a great evolution and market growth in the last decade: in 2017 the

market was valued at $11.81 billion and it is expected to reach the $26.67 billion by 2024.[1] Therefore, more research concerning to RFID systems should be done, as it is clear that it will become one of the most important technologies in the near future.

However, the most attractive aspect of RFID tags is that they allow to develop remote sensing systems. It is possible to attach a sensor to the tag and then send to the reader information about the parameter they are sensing. Remote sensing with RFID tags show attractive advantages such us low cost, high flexibility, wireless communication and battery-less operation. However, it also means that the temperature sensor that is introduced in the system should fulfill some strong requirements: wide temperature range (depending the application), high precision, accuracy, ultra low consumption and low area. Among the different magnitudes to be measured, temperature has always been one of the most interesting, as nearly all systems need to control the temperature in which they are operating.

Temperature is an analog magnitude and therefore is mostly converted to an electrical analog signal by a transductor. However, RFID tags need a sensor with a digital output. The reason to this is that these small and battery-less sensors work combined with a microcontroler that processes the information and sends it to the reader. Designers therefore have to make a double conversion from temperature to analog signal and then to a digital signal; or a direct conversion to a digital signal.

Temperature sensors using thermistors and Resistance Temperature Detectors (RTDs) to transform the temperature into an electronic signal have shown great precision results. The basic idea of these transductors is to generate a temperature dependant voltage or current, generated by the commented components.

On the one hand Thermistors are made of ceramic semiconductor materials and have values that can go from some Ω to MΩ, generally with a negative temperature coefficient. The resistor is connected to a temperature independent voltage, therefore the information is given here by a current that changes with the temperature, $i_{temp} = \frac{v}{R_{temp}}$. The main advantage of this devices is their sensitivity (fast response when small temperature change) and their main drawback is that their behaviour is not linear with the temperature. On the other hand, RTDs are made of platinum or nickel and have a positive temperature coefficient. Their resistance change is linear with the temperature, therefore they are easier to use than thermistors. They are also more robust to extreme temperatures, as they can operate in a range between -200°C to 600°C. The penalty in this kind of solution is the low sensitivity, usually around $1\frac{\Omega}{^oC}$. The principle of operation with RTDs is slightly different. Instead of a constant voltage, a temperature independent current is used and therefore the information is a varying voltage.

The architecture of the sensors using those transductors is generally based on a Voltage-Domain operation principle: they create a temperature dependant voltage that is compared

with a fixed one. However it has been proved not to be the most optimal way: higher resolution can be obtained, but the complexity and chip area are increased.[2] The alternative to these sensors, are the ones working with a Time-Domain operation principle, Fig. 1-2. These architectures showed better results in the aspect of chip area and power consumption. In this type of sensors the temperature information is encoded in time parameters such as frequency or duty cycle. However, time-domain sensors lack of accuracy.[3]

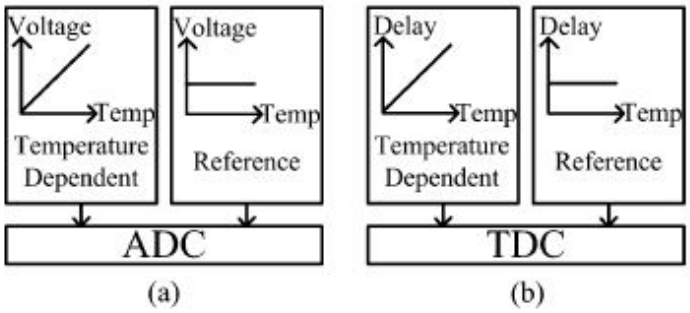

Figure 1-2: Comparison (a) Voltage-Domain and (b) Time-Domain Sensors

Electronic circuits using RTDs or Thermistors have shown great operation ranges and precision, however they have become not the optimal solution for small and battery free devices. Their large area translates to higher costs.[4] The Integrated Circuits (ICs) are the best solution to this problem. With more customizable electronic architectures, a good design and good packaging, high precision can be met while reducing the total area and costs.

Most IC sensors are fabricated in metal-oxide semiconductor (CMOS) technology due to its many advantages. First of all costs can be reduced when fabricating in high volumen while having the same satisfactory results. The sensitivity to mechanical stress is lower due to their small size. It also shows some problems concerning to the low-frequency noise component and the errors introduced by the components. However there are many ways to fight against these effects in a satisfactory way[5] .

In conclusion, IC temperature sensors based on time-domain principles are the best solution for applications that need small and cheap sensing devices, like RFID systems. For example in the medicine sector, where fast and wearable devices can be invented to check temperature of people;[4] or for Industry 4.0 sector, where machines have to operate within a temperature range. However, their main disadvantages are their low temperature operation range and their sensitivity to it. Therefore, designers have to look for the best architecture that fight against these trade-offs.

Chapter 2

State of the art

In this section an overview of the already implemented IC sensors is going to be done extracting important information from journal and conference papers. Is going to be considered as "important" all the information concerning to size, consumption, precision and operation principles. In Table 2.1, a comparison between more temperature sensors is done.

A Passive RFID Tag Embedded Temperature Sensor With Improved Process Spreads Immunity for -30°C to 60°C Sensing Range[6]

The main issue to work with RFID Tags is the low power consumption required to the sensors. In order to achieve that, this sensor uses the bandgap reference to generate the sensing signals, instead of having a particular circuit for it. However, the SNR and linearity are damaged. The system includes a low power ring oscillator clock generator which is used to extract the information of the generated temperature dependent pulse widths (using capacitors).

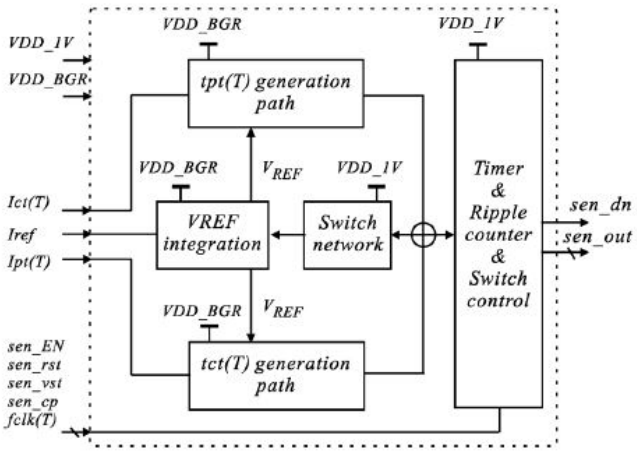

Figure 2-1: Block diagram of the proposed temperature sensor

- Technology: 0,18μm
- Active Area: 0.014mm^2
- Supply Voltage: 1V
- Power Consumption: 0.35μW
- Temperature Range: from -30°C to 60°C
- Inaccuracy: $\pm$1.5°C (3σ)
- Sensing resolution: 0.3°C
- Calibration: one point at 20°C
- Sampling rate: 68 samples per second (14.5msec)

A PWM output Temperature Sensor[7]

This paper shows a time-domain sensor based on a Pulse Width Modulation principle. A capacitor is charged and discharged by two currents, one of them dependant to the temperature. The temperature information will be storeD in the changing duty cycle of the square wave generated in the capacitor. This duty cycle should have a linear behaviour with the temperature, however in reality it shows second order components.

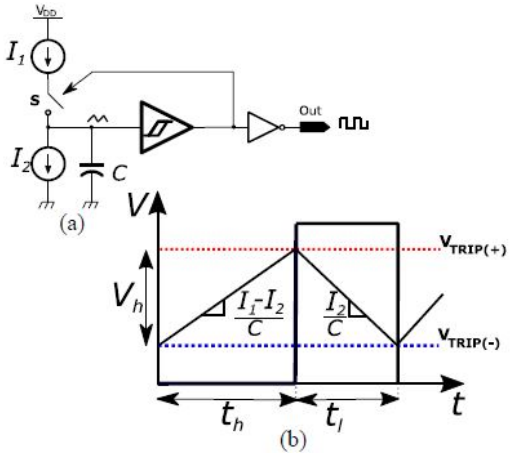

Figure 2-2: Operation principle of the sensor: basic schematic and temperature dependant wave

- Technology: 0.6μm XFAB CMOS
- Active Area: 0.371mm^2 (BG+Modulator)
- Supply Voltage: 5V
- Current Consumption: from 70μW to 125μW
- Temperature Range: from -40°C to 125°C
- Inaccuracy: no information
- Sensing resolution: no information

- Calibration: no information
- Sampling rate: no information

An Ultralow Power Time-Domain Temperature Sensor With Time-Domain Delta-Sigma TDC[8]

In this sensor the temperature information is stored in the delays formed in the clock generated by a BJT inverter chain. This clock is compared with an external temperature independent clock (a temperature compensated crystal oscillator, TXCO) and modulated by a $\Delta\Sigma$ time to digital converter. The result of this architecture is high energy management efficiency and high resolution.

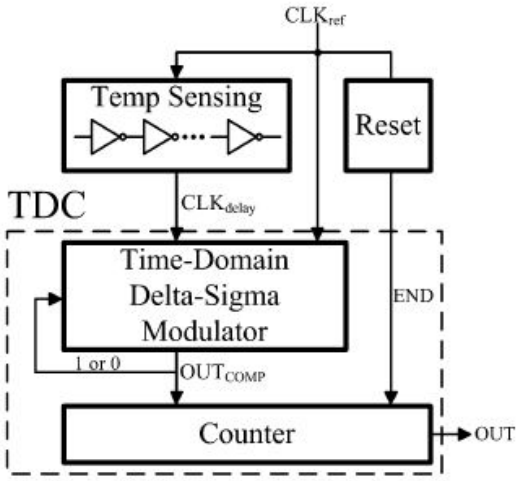

Figure 2-3: Architecture of the sensor

- Technology: 0,18μm
- Active Area: 0.089mm^2
- Supply Voltage: 1.8V
- Current Consumption: 820nW
- Temperature Range: from -20°C to 80°C
- Inaccuracy: $\pm$0.99°C (3σ)
- Sensing resolution: 0.09°C
- Calibration: two points (-20°C and 60°C), second order master curve
- Sampling rate: 1.25 samples per second

Additionally to the shown information, the paper includes a study of the sensitivity to the Vdd variation: from 1.6V to 2V it shows a maximal error of 7°C.

1.2V-0.18um CMOS Temperature Sensor With Quasi-Digital Output for Portable Systems[9]

The main difference of this work is the frequency output of the temperature sensors. The operation principle relies on a multivibrator that converts a current to a frequency: a current drives the capacitor between the limits of a comparator. The paper presents two alternative sensors, depending on the generation of the current: V_{TH}-T *sensor* and β-T *Sensor*.

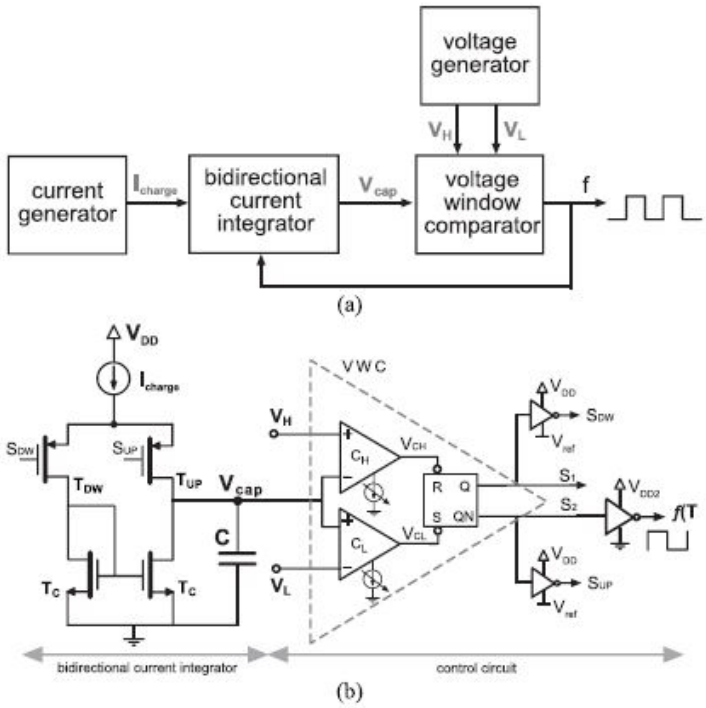

Figure 2-4: Diagram and basic schematic of the proposed temperature sensor

- Technology: 0,18μm
- Active Area: 0.024mm^2 for V_{TH}-T *sensor* and 0.019mm^2 for β-T *Sensor*
- Supply Voltage: 1.2V
- Current Consumption: 3μW for V_{TH}-T *sensor* and 1.9μW for β-T *Sensor*
- Temperature Range: from -40°C to 120°C
- Inaccuracy: $\pm$1°C
- Sensing resolution: $335\frac{Hz}{^oC}$ for V_{TH}-T *sensor* and $460\frac{Hz}{^oC}$ for β-T *Sensor*
- Calibration: one point
- Sampling rate:

Additionally to the shown information, the paper includes a study of the sensitivity to the Vdd variation: from 1.2V to 1.4V it shows an error less than 1%.

Conclusions

Temperature sensors based on a time-domain operation principle are a good solution to approach to the desired specifications of RFID tags[7 –10] . However, is not possible to accomplish all of them at the same time. This trade-off can be observed in Table 2.1, where different temperature sensors are compared. Ultra low power consumption is achievable ($< 1\mu W$) in some cases but at the expense of increasing the effect of the process and voltage variations. 2-point calibration is usually needed in order to compensate for accuracy errors and linearity deviations caused by fabrication process variations.[8] Some work such as in[11] and in[12] report excellent results in terms of temperature range, resolution and inaccuracy, but show higher power consumption ($93\mu W$ and $160\mu W$). It is clear, that a trade-of between the parameters is necessary and each design needs to be optimized for each application scenario. In this work, a temperature sensor has been designed for ultra low-cost and long temperature range RFID systems, therefore paying special attention to maximum measuring range with minimum design area and without affecting much to the rest of parameters.

Table 2.1: Comparison of different temperature sensors

Sensor	**Technology**	**Temp. Range (°C)**	**Area (mm^2)**	**Supply Voltage (V)**	**Consumption(μW)**	**Sensing Resolution**
[6]	0.18	-30 to 60	0.014	1	0.35	0.3 °C
[7]	0.6	-40 to 125	0.371	5	70 to 125	-
[8]	0.18	-20 to 80	0.089	1.8	0.820	0.09 °C
[9] (A)	0.18	-40 to 120	0.024	1.2	3	335 $\frac{Hz}{^oC}$
[9] (B)	0.18	-40 to 120	0.019	1.2	1.9	460 $\frac{Hz}{^oC}$
[11]	0.18	-20 to 120	0.118	1.8	93	0.048
[12]	0.18	0 to 100	0.0004	1.8	163 to 212	0.058
[10]	0.35	-10 to 120	0.84	2	3.9	±2 °C

Chapter 3

Objectives

The State of the Art sensors show that time-domain based operation principle show acceptable results in the requirements of RFID systems. However, it is difficult to obtain a balance between all of them. Due to this strong trade-off, optimizing one aspect of the sensor leads to a deterioration in others. For example, ultra low power consumption is achievable at the expense of increasing the effect of the process and voltage variations. Wide temperature range with great resolution and inaccuracy results can be obtained but with the penalty of having a higher power consumption.

The main objective of this project is to develop a temperature sensing interface suitable for RFID applications and showing a good balance between the most important requirements. For that, the following goals need to be achieved:

- Low power consumption, $<10\mu$W, as the chip has an autonomous power
- The operation voltage needs to be small in order to allow efficient operation of the power harvester
- Cover a wide temperature range
- High linearity in order to avoid expensive calibration procedures
- Reduced effect of process and voltage variations
- Low size

Chapter 4

Operation principle

The Block Diagram of the whole temperature sensor system is presented in Figure 4-1. A bandgap will be used in order to provide reference voltages and bias currents to other blocks. The temperature sensing interface transforms the temperature into a signal, encoding the information with a Pulse Width Modulation (PWM). The clock generator is a block from the RFID tag itself and it will be used in the Time-To-Digital block to extract the information from the generated temperature dependent signal.

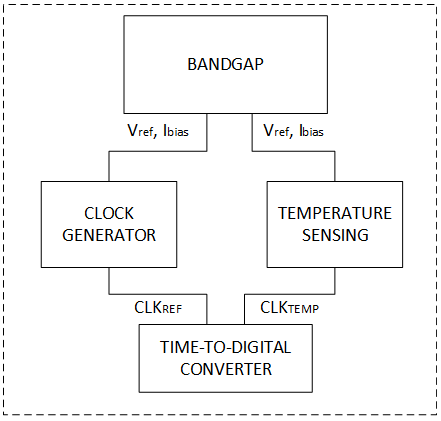

Figure 4-1: Block Diagram of the whole Temperature Sensor System

The operation principle of the temperature sensing interface, Figure 4-2, basically consists of a capacitor that is charged by a temperature dependent current, I_{charge} and discharged by a hysteresis loop. The capacitor starts completely discharged, at 0V. V_{out} then equals also to 0 and the switch is open. The top current will charge the Capacitor, until $V_{cap} = V_{ref}$, at that point the output of the comparator will be a logical high. The next two inverters create a square wave in the output with short rise and fall times. V_{out} closes the switch discharging the capacitor until $V_{cap} = 0$V. At that point, the charging phase starts again.

The resulting waveform in the capacitor, V_{cap}, is a saw-tooth signal, with a slope depending

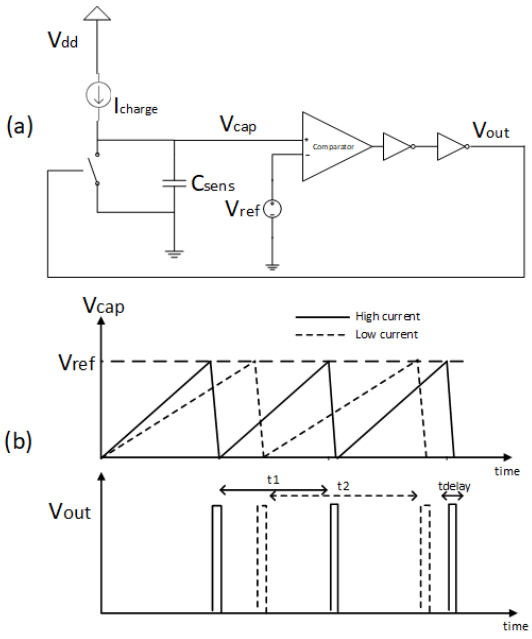

Figure 4-2: a) Simple schematic of the proposed temperature sensor, b) Resultant output and capacitor waveforms

on the charging current and to the capacitor. In the output, V_{out}, there is a pulse train wave, whose delay between pulses also depends on I_{charge}. Concretely, both depend on how fast the capacitor has been charged till V_{ref} (voltage reference of the comparator). This speed will change with I_{charge}: the higher the current, the faster the charging. Finally, this current will depend on the temperature.

With this system a signal with a temperature dependent frequency is generated: V_{out} has a variable time between pulses depending on the charging current (t_1 and t_2 in Figure 4-2), and therefore a variable clock frequency. The period of the generated pulse train signal is extracted from the basic equation of a capacitor, Eq. (4.1), and it will be the time needed to charge the capacitor plus a delay time, which is the discharging time of the capacitor and the traveling time through the comparator and inversors. This t_{delay} is also the width of the generated pulses, so it should be high enough in order to have pulses that can be detected, but also low enough to produce a negligible effect in the frequency. From Figure 4-2 it is known that the capacitor charges from 0V to V_{ref}, and that i equals I_{charge}.

$$i(t) = C\frac{dV(t)}{dt} \rightarrow \Delta t = C\frac{\Delta V}{i} + t_{delay} \approx C\frac{V_{ref}}{i_{charge}} \tag{4.1}$$

The temperature dependence of the system is introduced by a resistor, modeled by the Eq. (4.2). The circuit shown in Figure 4-3 generates the temperature variable current, I_{charge}. Long length transistors are used for the current mirror in order to minimize the voltage supply dependence and the Early effect. The fixed voltage is implemented with a Gain Boosting stage.

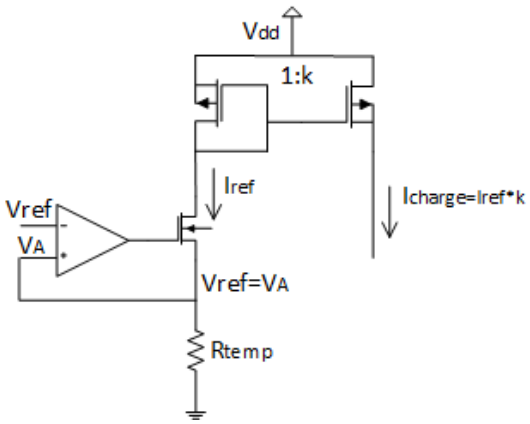

Figure 4-3: Temperature dependence generation

$$R_{temp} = R_{ref} * [1 + \alpha * (T - Tref)] \tag{4.2}$$

Therefore,

$$I_{ref} = \frac{V_A}{R_{temp}} = \frac{V_A}{R_{ref} * [1 + \alpha * (T - Tref)]} \tag{4.3}$$

Where R_{ref} is the resistance at T_{ref}, $T_{ref} = 27^{o}$C and $\alpha =$ temperature coefficient.

The charging current will be a copy of a reference current, multiplied by a factor of k.

$$I_{charge} = k * \frac{V_A}{R_{ref} * [1 + \alpha * (T - Tref)]} \tag{4.4}$$

Including the temperature effect in the Eq. (4.1), and ignoring the delay introduced by the hysteresis loop, the frequency of the pulse train is modeled by the Eq. (4.5)

$$f_{temp} = \frac{k * V_A}{C * V_{ref} * R_{ref} * [1 + \alpha * (T - Tref)]} \tag{4.5}$$

From Eq. (4.5) it can be deduced that the frequency is strongly dependent to the reference voltage of the comparator (charging threshold of comparator) and to the fixed voltage of the reference current (V_A). Then, unpredictable voltage variations from the bandgap will produce also an offset in the frequency, for example: an increase in this voltage will let the capacitor to be charged to a higher threshold and therefore the frequency will change. The problem here then is that the behaviour (frequency) will not only depend on the temperature, also to an unknown voltage that cannot be accessible.

The main solution to this problem would be to take out the effect of this voltage from the operation principle equation, Eq. (4.6). The easiest way to extract the dependency to this parameter is to make the fixed voltage of the gain boosting stage equal to the reference voltage

of the comparator, $V_A = V_{ref}$. If both values are the same, the effect of both parameters is cancelled as one is in the numerator and the other in the denominator.

$$f_{temp} = \frac{k * V_A}{C * V_{ref} * R_{ref} * [1 + \alpha * (T - Tref)]} \rightarrow \frac{k}{C * R_{ref} * [1 + \alpha * (T - Tref)]} \tag{4.6}$$

Chapter 5

Implementation

The previous section was a theoretical explanation of how the sensing interface works. In this section, the implemented architecture is going to be explained in a transistor level.

5.1 Circuit design

5.1.1 Generation of temperature dependent current

The first step is to generate a reference current that is dependent to the temperature. The implemented architecture will be the one shown in the Figure 4-3.

The current variation will come from the temperature dependency of the resistor. Therefore, the first task will be to choose the most temperature dependent resistor available in the technology. At this point, the components commented in the State of the Art, RTDs or Thermistors, could be used. However, it is decided to use smaller resistors that can be integrated in a small chip.

A study of all the available resistors is shown in Figure 5-1. The objective here is to find the one with the higher temperature coefficient in absolute values: the higher the coefficient, the higher the resistance variation.

Making the assumption that all the resistors in the technology are linearly perfect, the temperature coefficient can be easily extracted. Varying the temperature from -20°C to 100°C, the coefficient extraction is calculated in Eq. (5.1). Negative values mean that higher temperatures make the resistance values lower.

TYPE		R@-20ºC	R@27ºC	R@100ºC		Temp. Coefficient
Rnhpoly		1438,8489	1360,5442	1250		-0,001155897
Rnlplus2t		109,89011	130,03901	161,94332		0,003301909
rnlpoly		138,79251	160,51364	194,93177		0,002884834
rnplus2t		1176,4706	1257,8616	1398,6014		0,00144626
rnwell		3616,6365	4098,3607	5235,6021		0,003157456
rnwod2t		1923,0769	2277,9043	3007,5188		0,003845555
rphpoly		1510,574	1500,3751	1482,5797		-0,000152695
rphripoly		5882,3529	5555,5556	5181,3472		-0,00106936
rplplus2t		123,38063	146,73514	183,82353		0,00339702
rplpoly		148,15912	170,9694	207,25389		0,002850087
rpplus2t		2639,2188	2824,8588	3129,8905		0,00142846

Figure 5-1: Study of resistor types

$$\begin{aligned} \alpha_1 &= \frac{\Delta R}{R_{ref} * \Delta T} = \frac{R_{120} - R_{27}}{R_{27} * (120 - 27)} \\ \alpha_2 &= \frac{\Delta R}{R_{ref} * \Delta T} = \frac{R_{27} - R_{-20}}{R_{27} * (27 + 20)} \\ \alpha &= \frac{\alpha_1 + \alpha_2}{2} \end{aligned} \tag{5.1}$$

As Figure 5-1 shows, the resistor with the highest temperature coefficient is the rnwod type ($\alpha = 0.0038^{o}C^{-1}$) and it will lead us to the highest current variation in this technology.

The next step is to generate a fixed and temperature non-dependent voltage, where the resistor is going to be connected. For that, an operational amplifier in a "Gain Boosting" topology is going to be used, explained in the reference.[13] Figure 5-2 shows the schematic of this architecture.

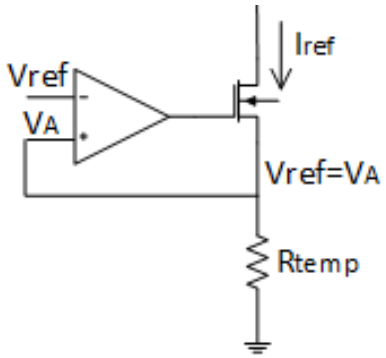

Figure 5-2: Gain Boosting topology

Gain Boosting is a technique commonly used to obtain high output impedance without the need to add cascode stages. The output of the amplifier, V_{out} is connected to the gate of a nmos transistor, whose source is connected to one of the inputs of the amplifier and to the resistor, V_A. The other input will be the external reference voltage, V_{fix}, around 0.3V in this case. It is needed to have a stable voltage in the resistor, and with this topology V_A is enforced to have the same value as V_{fix}. If the drain voltage of the transistor increases, the source voltage will also increase, and therefore the gate voltage will decrease. However, the current of the transistor will be reduced, and therefore V_A will stay constant.

Once the structure of this stage is clear, the next step is to implement it. In order to decide the correct values of the components, the following design rules has to be taken in mind.

The value of the resistor has a direct impact on three important aspects of the temperature sensor: the frequency, the size of the chip and the current consumption.

First of all, as it is shown in Eq. (5.2), the lower the value of the resistor the higher the frequency of the generated output signal. There is no strict operation frequency range threshold, but as a rule, it should not work in the MHz range.

$$f_{temp} = \frac{k * V_A}{C * V_{ref} * R_{ref} * [1 + \alpha * (T - Tref)]} \tag{5.2}$$

As it was explained in previous sections, a fixed voltage is applied to the resistor. It can be easily concluded with the Ohm law that with higher resistor, the needed current will be lower, leading to a lower power consumption. However, it would also mean higher chip area.

The size of the temperature sensing interface is a more critical design rule. The goal of this project is to design a cheap and small temperature sensor, and therefore the size of all components is a decisive factor.

To conclude, the resistor value is a trade-off between area and power consumption.

The Gain Boosting stage is made of an Operational Amplifier and an output transistor. Its goal is to obtain a stable voltage in the source of the output transistor equal to one of the operational amplifier input. An already designed amplifier is going to be used, shown in Figure 5-3, with a bias current of 150nA. The reference voltage should not be higher than 500mV. As shown in Eq. (5.2), V_A could also be a degree of freedom, however a 300mV reference voltage, V_{fix}, is chosen.

With this topology it is enforced to have $V_A = V_{fix}$, and it is also known that, $V_A = i * R$. Therefore, the output transistor must allow a current flowing through it high enough to have the needed voltage. This current is constantly adjusted and could take high values. If the output transistor has not enough gain, the result V_A will be lower than expected. This will also be decisive for the next stage, the Current Mirror.

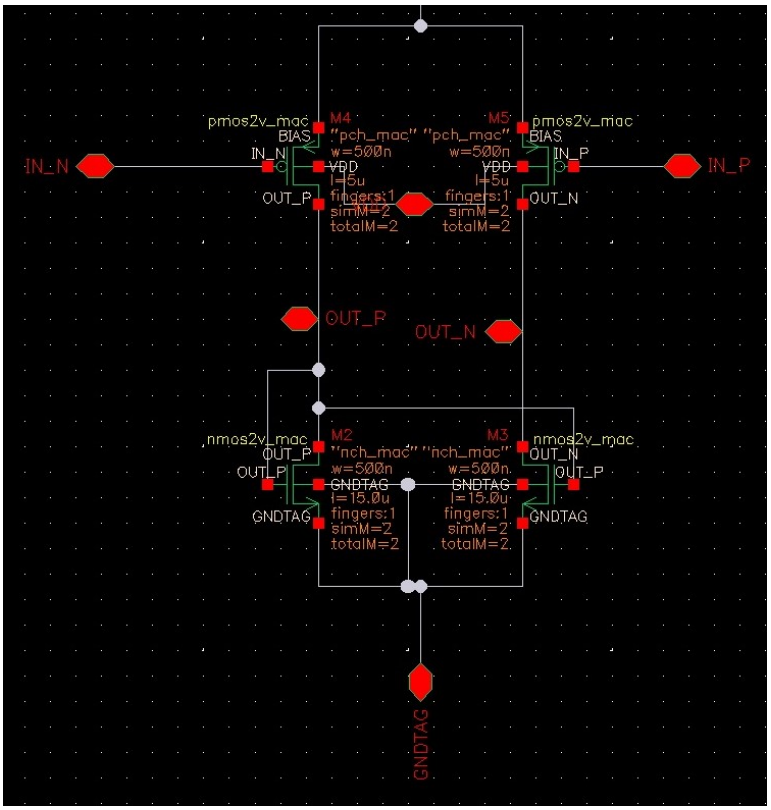

Figure 5-3: Used operational amplifier

5.1.2 Current Mirror

The next stage of the temperature sensing interface is to copy the reference current (temperature dependent) to the branch that will charge the capacitor. For that a simple current mirror architecture is going to be implemented.

The first task at designing this stage is to have a current mirror that allows to flow in the reference brunch a current high enough so that the Gain Boosting works (explained in the previous subsection). Therefore, the transistors must have the correct gain, resulting in big devices.

The next step is to decide the multiplication factor between devices. The easiest solution would be to have a 1:1 current mirror, the copied current would be exactly the same as the reference current. However, it is not a good decision for the consumption optimization.

It can be easily extracted the needed current flowing through the reference branch, because is the same as in the Gain Boosting stage. Using the Ohm law in Eq. (5.3), it is reached to a high current that cannot be modified. The next branch is used to charge the capacitor, and the needed current can be much lower than the calculated reference current.

$$V_A = i * R \rightarrow 0.3 = i * 180k\Omega \rightarrow i = 1.6\mu A \tag{5.3}$$

Therefore the optimal decision is to have a 2:1 current mirror, which decreases the power consumption by having one current lower than the other, but which still fulfills the requirements.

5.1.3 Capacitor

This component is the key of the operation principle of the system, which consists basically on charging and discharging this capacitor faster or slower, depending on the temperature.

First of all a capacitor independent to the temperature must be used. The Metal-Insulator-Metal types (MIMCAP) show good stable behaviour. One of the terminals is connected to the ground and the other to the branch where the reference current is copied: that way the capacitor is charged (special attention must be paid to this current as it has to be high enough to charge the capacitor). In order to discharge it, this terminal has to be also connected to a switch that will short circuit this point with ground. A transistor will be used for that, which will be activated once the capacitor has been fully charged to a threshold established by the next block.

The used capacitor is a degree of freedom which will be used to correct some undesirable effects on the frequency and size of the temperature sensing interface.

Deduced from the operation equation of the system, the capacitor has a direct impact on the frequency: they are inversely proportional. On the other side, the capacitor value is directly connected to its size: the bigger the value, the larger the size. This has to be taken in mind for future steps, as it is going to be one of the bigger components of the temperature sensor. Finally, the chosen capacity has also an impact on the needed charging current. If a capacitor of many pF is chosen, the charging current should be higher leading to higher consumption.

The transistor that short circuits the component to the ground for its discharging needs a high gain, as it drives a high current to execute this process.

5.1.4 Comparator and inverters

The capacitor of the previous stage has to be discharged only after it has charged to a value above a certain threshold. To meet that condition a comparator is needed, which will also put the threshold to the charging, V_{ref}.

The comparator will compare V_{ref} with the capacitor voltage. When V_{cap} is above V_{ref}, the system should discharge the capacitor and start again the cycle. For that, the output of this block will generate a logical high and it should be connected to the switch (transistor) that discharges the capacitor (by short circuiting it). So first of all, a high-speed comparator is needed, which will introduce higher consumption. The one shown in Figure 5-4 is going to be used, with a bias current of 200nA. Till now all the used transistors were the same type. In

this architecture two nmos are going to be introduced that have lower voltage threshold than the rest. The reason for that is that it can improve mismatch and fabrication errors. With this comparator we obtain a high response, reducing the delay time introduced in this stage, and also a square waveform.

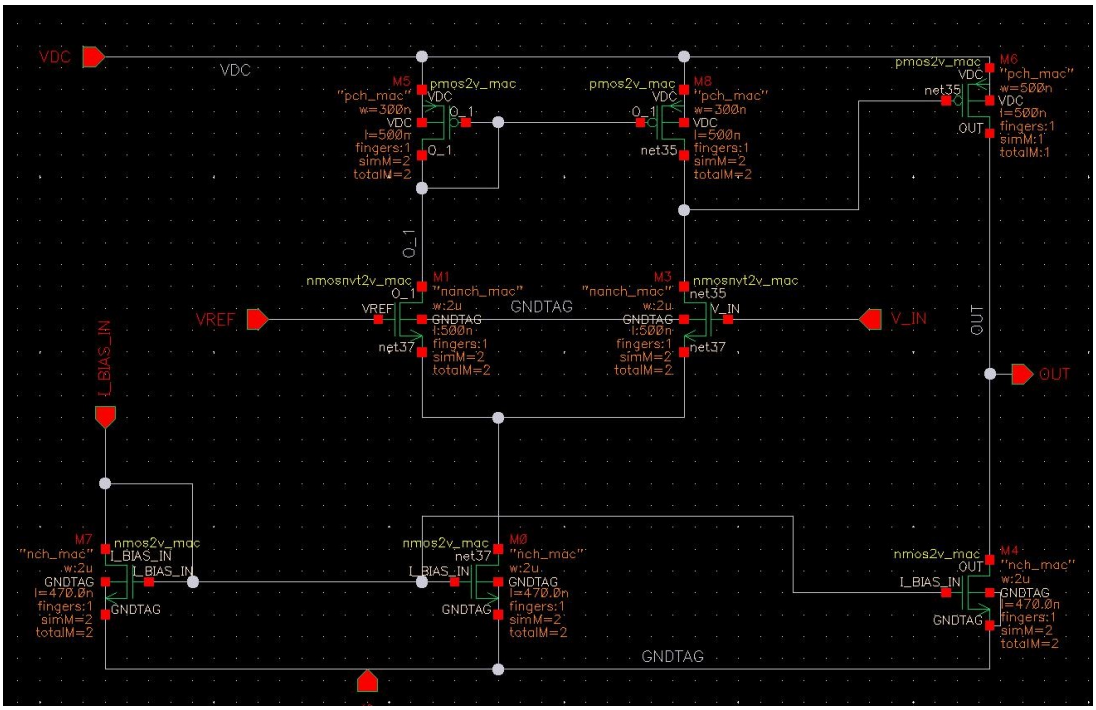

Figure 5-4: Used high speed comparator

The output of the comparator should activate the discharging transistor of the capacitor. This transistor is designed to be big, as it discharges the capacitor very fast. Therefore, the previous stage needs to have a really high drive strength in order to activate this transistor. For that, two extra inverters are added.

The used transistros here are big enough to provide the required driving stregnth. One of the problems here is that if they are too big, they also need bigger bias current. Big transistors will also introduce big parasitic capacitor that will be needed to be charged and discharged, introducing more delay to the system (which we would like to avoid). Therefore, the values of this transistors must be a trade-off between obtaining a square wave as perfect as possible, current consumption and parasitic capacitors. Figure 5-5 shows the used inverters.

Another important issue in this stage is to control the consumption of the inverters. The intermediate signals are rectangular pulses, but the transition between high and low is not perfectly sharp. This transition is result of the parasitic capacitors that are introduced, which are also being charged and discharged. This leads to both top and bottom transistors to be activated at the same time, producing a shortcircuit between voltage supply and ground.

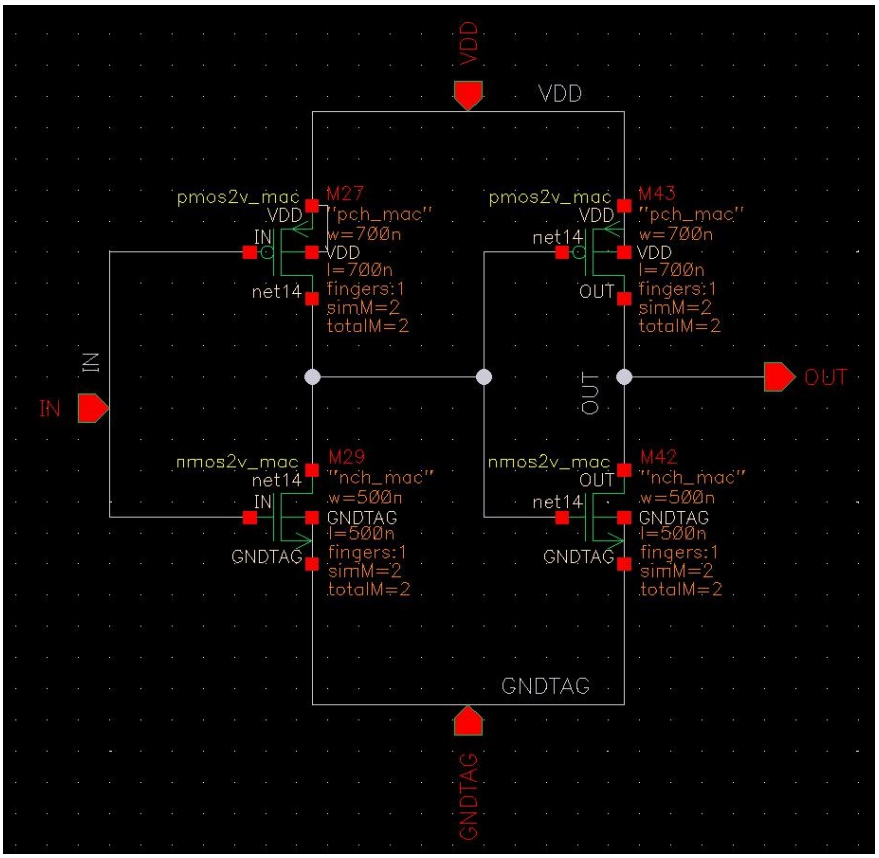

Figure 5-5: Used inverters

5.1.5 ENABLE

Sensors usually work on demand: they are only activated when they have to take samples. Theefore, an enable port must be added to the whole system, that should minimize the power consumption in the off state.

Starting with the capacitor, since the Operation Principle Chapter (4) it has been assumed that the initial state condition of the capacitor is that it starts completely discharged, at 0V. However, in the presented circuit that assumption cannot be made. Figure 5-6 shows that although the system is not activated, one of the terminals is connected to ground and the other to a net with an uncertain voltage level. Therefore the capacitor could be still charged from previous working times or there could be some voltage interference.

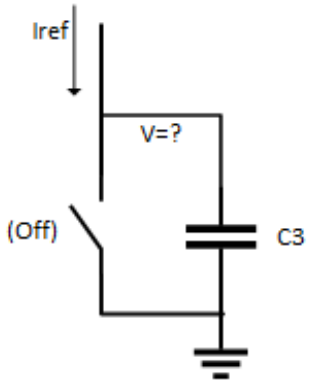

Figure 5-6: Unknown voltage in off state

In order to fix this problem, an extra pin is going to be added to the temperature sensing interface: an enable port. A high signal is used to activate the system and a low signal to settle everything to zero.

Coming back to the capacitor issue, it is easily solved connecting one of the terminals to a switch that short circuits it with the ground. When the switch is on, it has both terminals to ground and therefore it is fully discharged. That should happen when the system is not working: at a low enable signal. If an inverter is added to activate the switch the problem is solved: the low enable signal enters the inverter, which transforms it into a high signal that activates the switch and that short circuits both terminals of the capacitor to ground, obtaining a completely discharged capacitor. When the enable signal is high, the whole system is activated and the capacitor starts at the condition it was required: 0V. Figure 5-7 presents the explained solution.

The next issue comes with the power consumption. In an off state the expected current consumption of a device is expected to be zero, however, in the presented architecture, the reference branch of the current mirror is working all the time. As shown in Figure, 5-8 The solution here is to add a switch in this branch that is activated with the enable signal. When

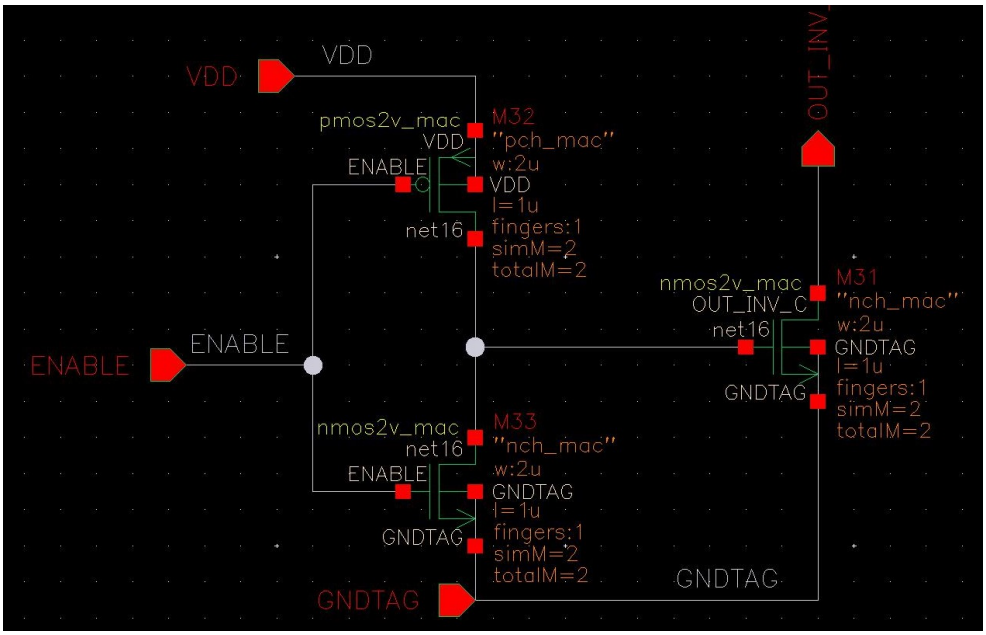

Figure 5-7: Used inverter and switch to force the 0V initial condition of the capacitor

the enable signal is high, the switch is activated and the branch is working perfectly. When the enable signal is low, the switch is opened and the branch is cut.

Finally, this enable must also control the switch that is in the output of the inverters, the one of the hysteresis loop that discharges the capacitor in each working cycle. For that an AND gate (composed of a NAND gate and an inverter) is going to be designed. The inputs of the gate will be the enable signal and the output pulse train signal of the inverters stage. This output signal will only reach the controlling switch when the system is activated. Adding the circuit shown in Figure 5-9 the explained solution is achieved.

The gain of the used transistors must be high in order to have a high-speed circuit with perfect square waveforms. Additionally, this circuits will increase the power consumption, however making the length of the transistors higher, it can be decreased.

5.1.6 Immunity to voltage supply

The current mirror of the temperature sensing interface is connected to the voltage supply, which will come from a bandgap. This block works in a nearly ideal way, however, the given voltage can suffer from variations. These variations can affect to the current mirror behaviour, causing the Early effect, and therefore to the overall temperature sensing interface. The main countermeasure to this effect is to have transistors with higher lengths.

The current mirror transistors are directly connected to the voltage supply, and therefore a change in it will also modify the voltage between drain and source. In Figure 5-10 it can be seen that the variation of Vds could lead the transistor to work on another region, changing

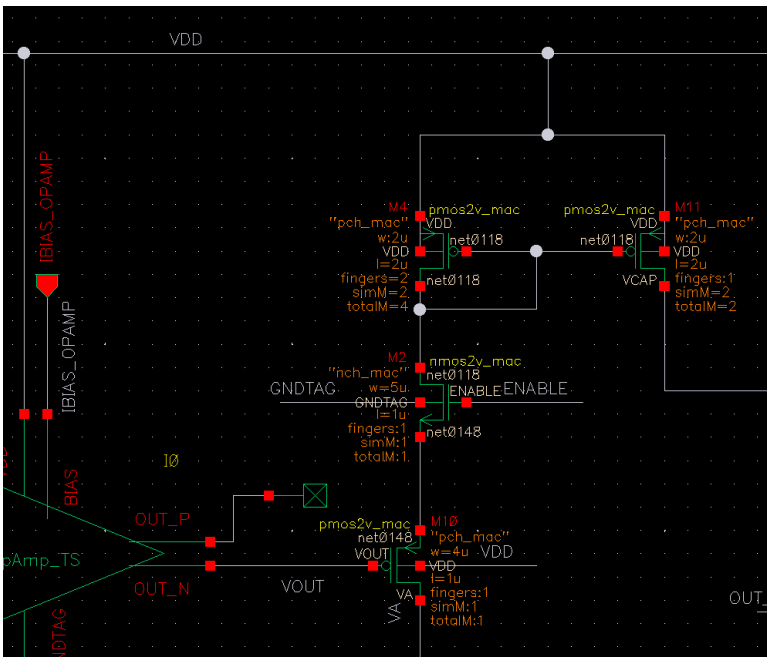

Figure 5-8: Transistor acting as a switch in the reference branch of the current mirror for consumption optimization

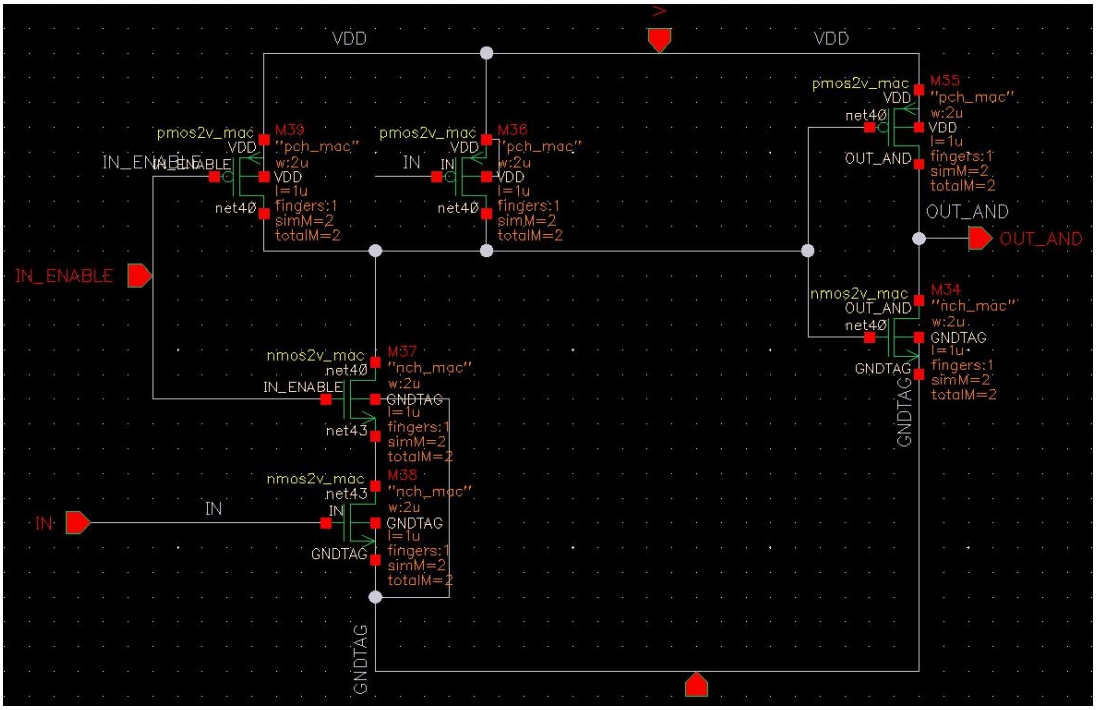

Figure 5-9: AND gate

also the provided current and therefore the operating frequency. The saturation region slope depends on the length of the transistors. Increasing this parameter the region becomes more stable, which makes the whole system more stable to the voltage supply variations.

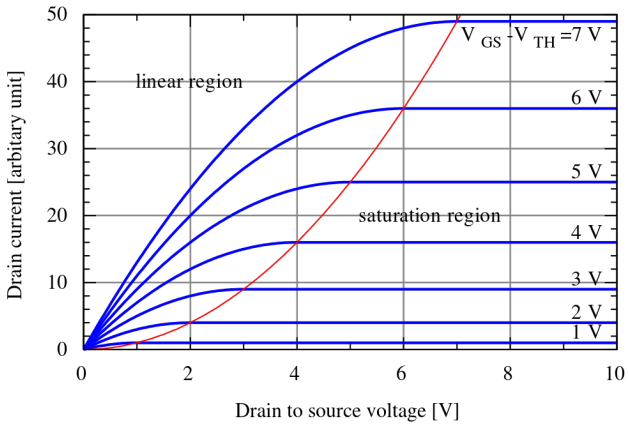

Figure 5-10: Drain current versus drain to source voltage of a MOSFET

In order to check that, some simulations are going to be done. The frequency of the output signal is going to be plotted against the voltage supply variation (from 1.7V to 1.9V), making a parameter sweep of the length of the transistor (800n, 1.4u, 2u, 2.6u, 4u). It can be deduced from the simulations that the higher the length of the transistor the more stable is the system against the supply variation: at 800nm a variation of 5.57kHz is obtained, and at 4um a variation of 0.92kHz. The length of 2u is chosen for the design with a frequency variation of 2.1kHz.

5.2 Layout

The sensor has been designed in p-substrate 0.18-μ CMOS technology and PMOS and NMOS transistors have been used in the whole architecture, with a voltage supply of 1.8V. The resistor has a value of 180kΩ and the most temperature dependent resistors available in this process have been used: n-well resistors under diffusion with a temperature coefficient of $\alpha = 0.0038$ $^{o}C^{-1}$. The Metal-Insulator-Metal (MIM) capacitor has a value of 6pF and a small temperature coefficient.

In Figure 5-11 the layout of the temperature sensing interface is shown where two extra inverters have been added to the original architecture in order to minimize the parasitic capacitance effects when connecting this module to others in the whole temperature sensor. The resultant chip has an active area of 0.019mm^2.

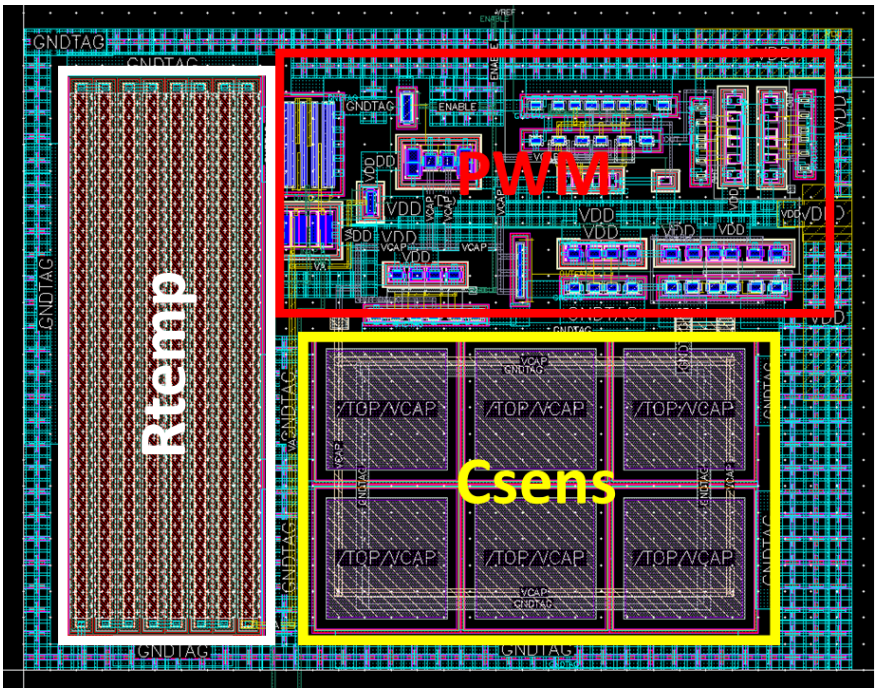

Figure 5-11: Layout of the whole temperature sensing interface, with a size of 0.019mm^2

Chapter 6

Results

6.1 Theoretical and Simulation results

Once the circuit is built, it is necessary to compare the real and the theoretical behaviours. As explained in the Operation Principle Chapter (4), the system should follow the equation (6.1)

$$f_{temp} = \frac{k * V_A}{C * V_{ref} * R_{ref} * [1 + \alpha * (T - Tref)]} \tag{6.1}$$

The relevant values used in the circuit design are shown in Table 6.1

Parameter	Value
Current mirror factor, k	0.5
V_A=V_{fix}	300mV
Capacitor	6pF
Comparator V_{ref}	300mV
Resistor, R_{ref}	180kΩ
Temperature coef., α	0.0038 $^{o}C^{-1}$

Figure 6-1 shows both the theoretical and circuit behaviour results. One of the reasons of the offset between both graphs is the t_{delay} introduced by the comparator and inverters that was ignored during the extraction of the Eq. 6.1. Although it is small, its effect can be seen in the frequency offset. In addition to it, the transistors also contribute to the offset: they introduce parasitic capacitors, and their operation also changes with the temperature. On the other hand, the circuit improves one aspect of the theoretical behaviour: second order effects are decreased leading to a better linearity. This will be explained in the Future Work Chapter (8).

Finally, Figure 6-2 shows that the capacitor and output signals are as expected in the

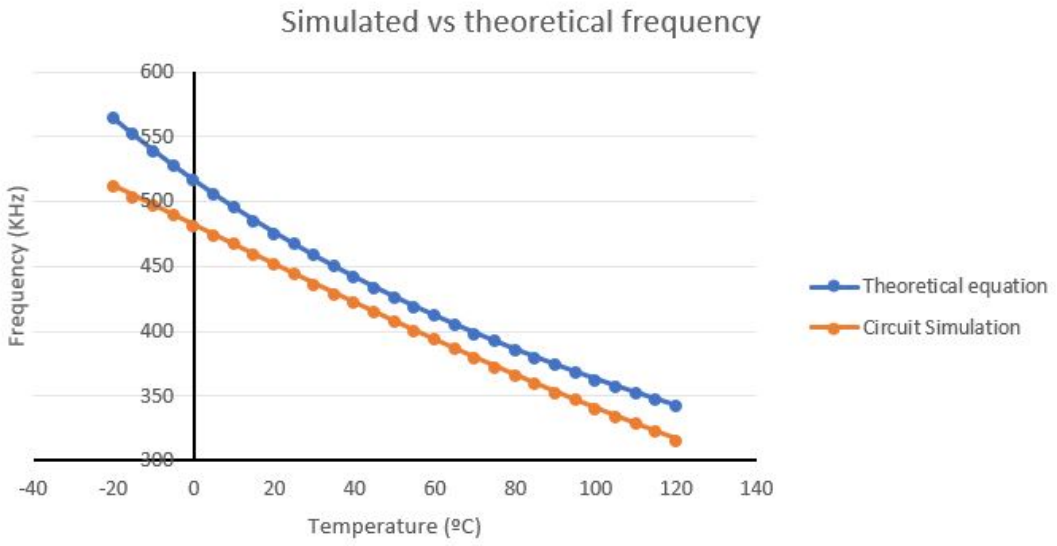

Figure 6-1: Theoretical behaviour vs Simulation

Operation Principle Chapter (4). The temperature effect is also present in the simulations.

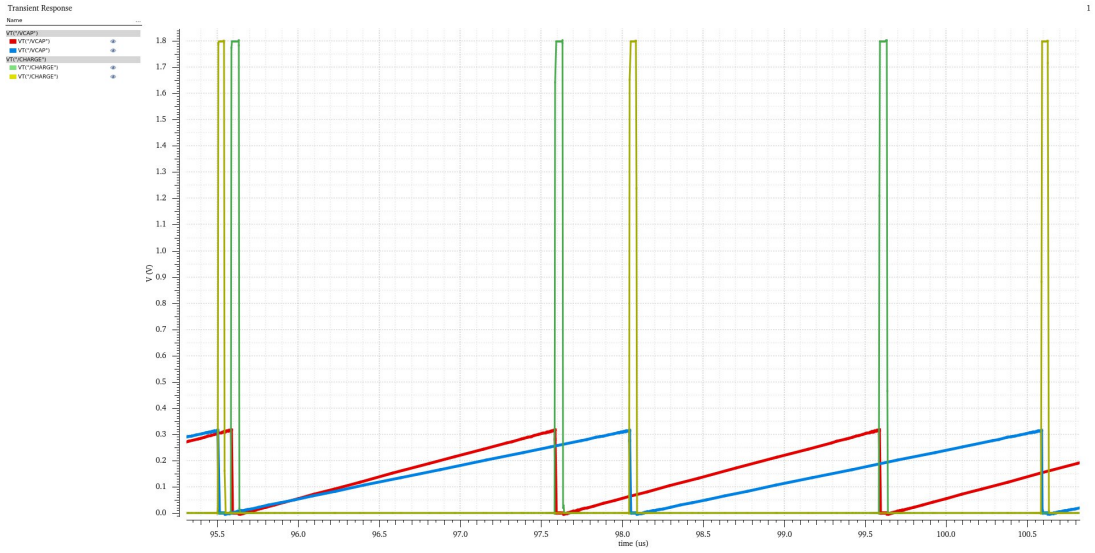

Figure 6-2: Capacitor voltage signal and output signal at -10 °C and 60°C

In the previous section, the behaviour of the circuit was explained stage by stage. The simulations made at this point could help to understand better how the temperature sensing interface works.

6.1.1 Generation of temperature dependent current

The main issue in this stage was to generate a temperature independent voltage. For that, a Gain Boosting architecture is implemented in the circuit. The result is plotted in Figure 6-3,

and it shows that the goal is achieved: for any temperature a voltage equal to a fixed one is enforced.

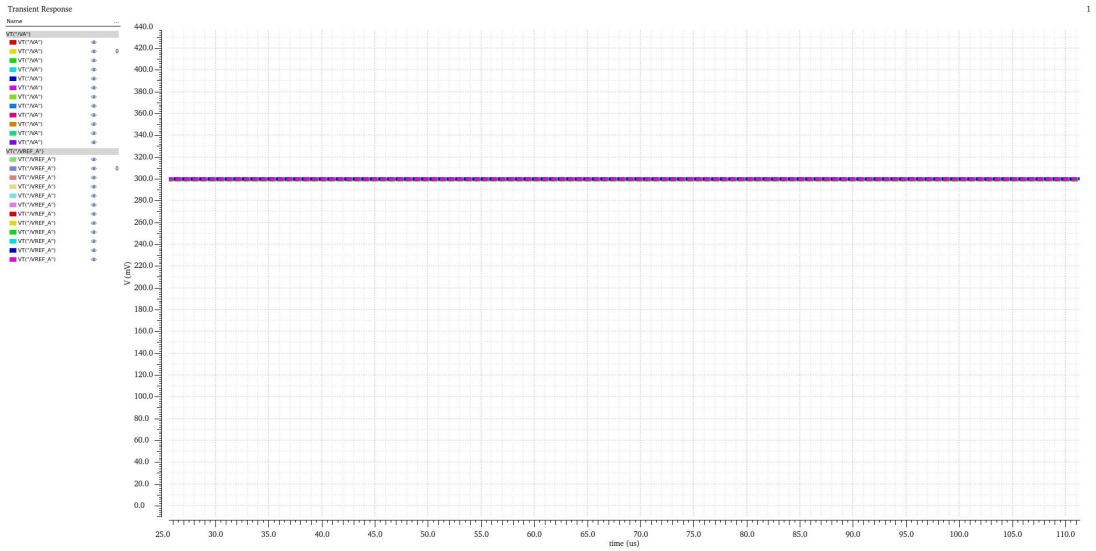

Figure 6-3: A fixed voltage of 0.3V is enforced in the net V_A for any temperature

From this block it can also be checked if the generated reference current is dependent to the temperature. As explained in previous section, this reference can be calculated from Eq. (6.2). Figure 6-4 presents that an increase in the temperature creates a lower current and that the calculations of Eq. (6.2) are correct.

$$V_A = i * R \xrightarrow{@30^oC} 0.3 = i * 180k\Omega \rightarrow i = 1.6\mu A \tag{6.2}$$

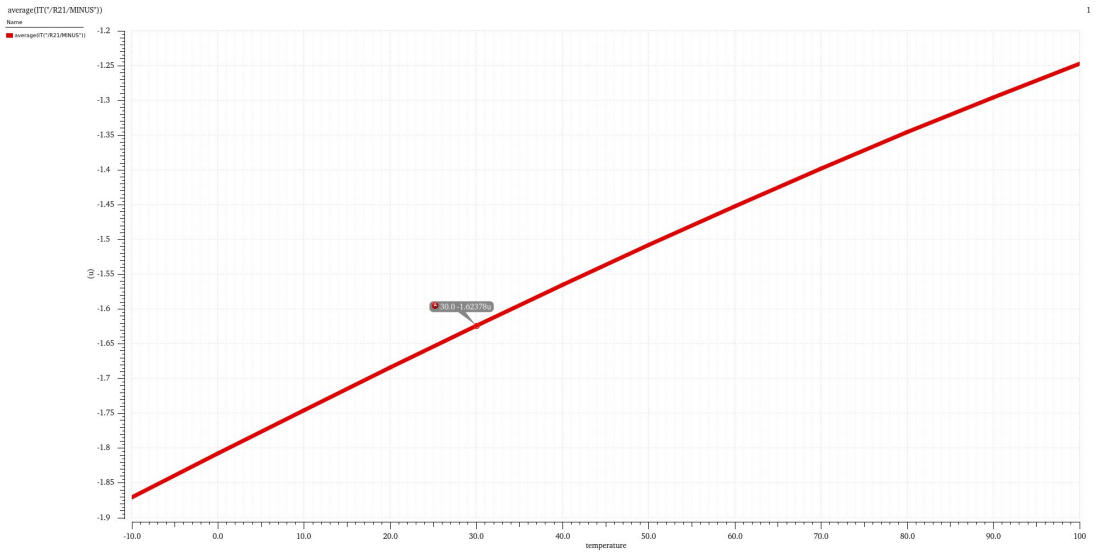

Figure 6-4: Generated reference current at different temperatures

6.1.2 Current Mirror

Remembering the decision made in the previous chapter, the copied current should be half of the reference current, as presented in Figure 6-5.

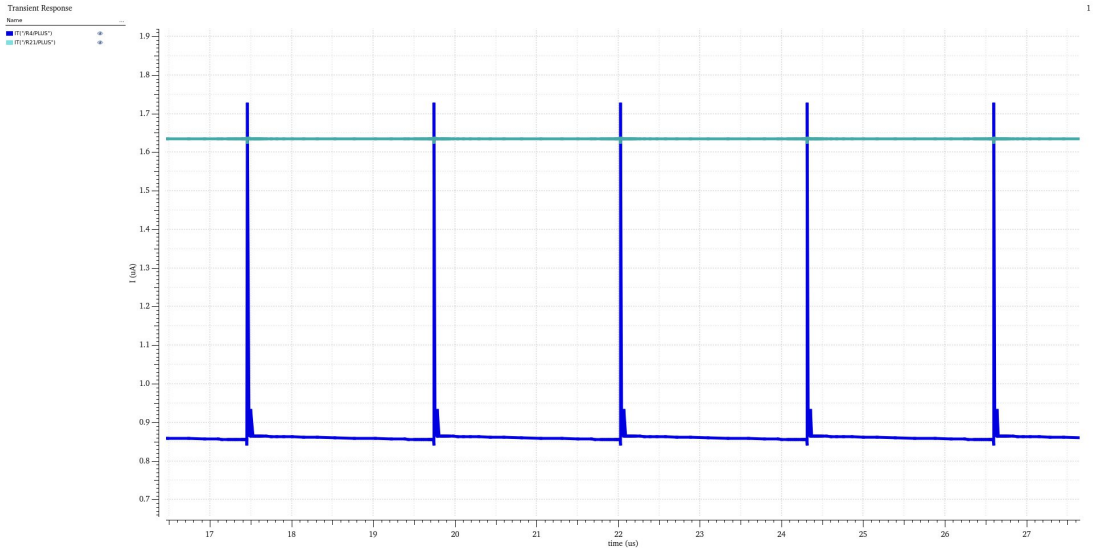

Figure 6-5: Reference and copied current at 30 °C

The graph also shows some peaks in the copied current, that occur when the capacitor is discharged as shown in Figure 6-6. The output branch of the current mirror is connected to one terminal of the capacitor. When the discharging stage happens, this terminal is short circuited to the ground. That results in a short circuit from supply to ground and generates the peaks of both figures.

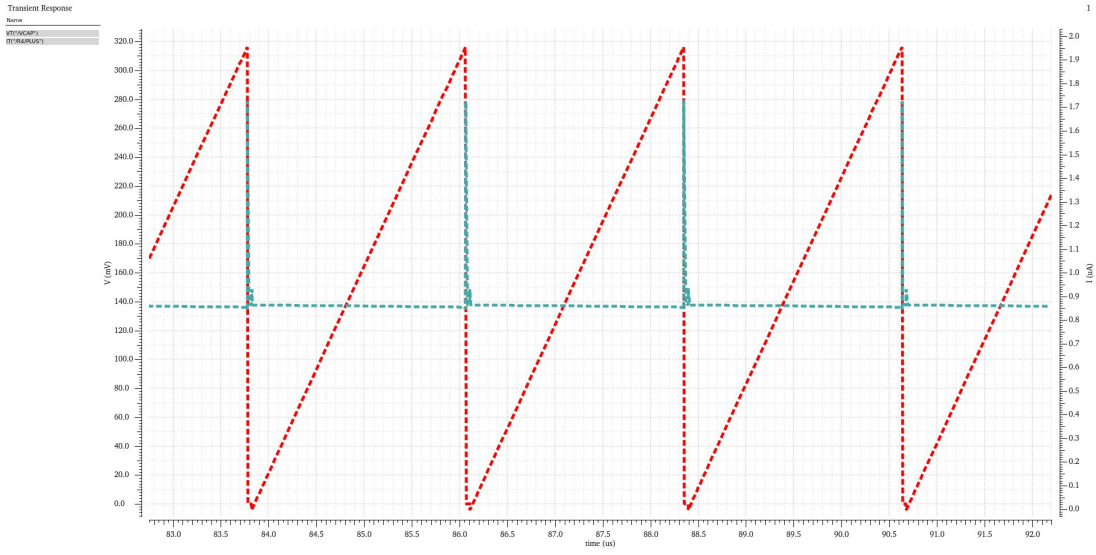

Figure 6-6: The current peaks happen at the capacitor discharging due to a short circuit of Vdd with ground

6.1.3 Capacitor

This component is the most crucial one, as the operation principle relies on its charge and discharge. Figure 6-7 shows that this is achieved: the voltage increases till it reaches a fixed value, and then a fast discharge happens.

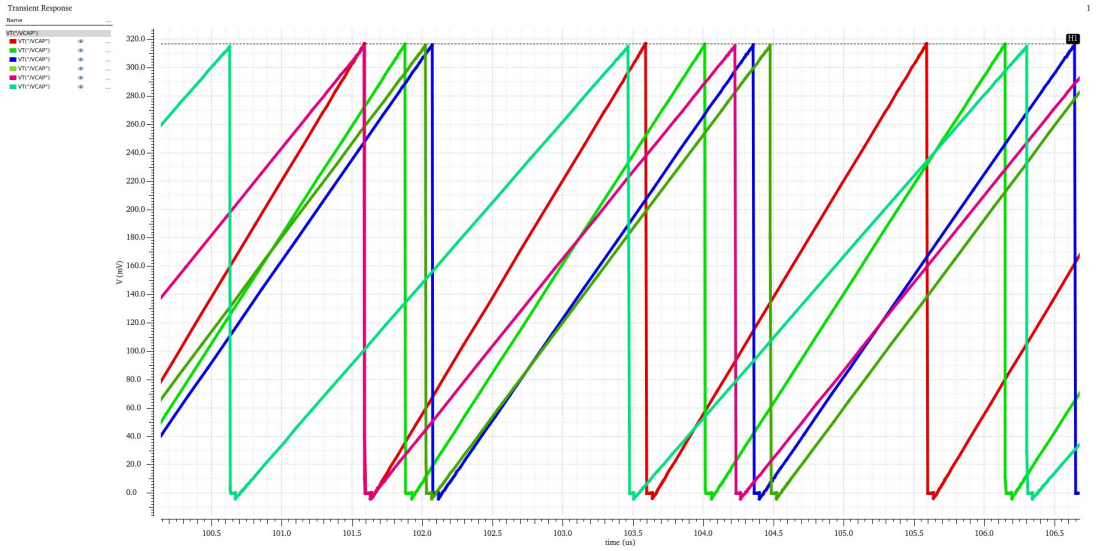

Figure 6-7: Voltage signal at the capacitor at 6 different temperatures

The temperature effect is present in the charging time. For higher temperatures, the current decreases and therefore it needs more time to charge it.

6.1.4 Comparator and inverters

One of the requirements of this stage, was to design a high-speed comparator. In Figure 6-8 this activating time can be seen: 120ns.

Additionally, Figure 6-9 presents the output signals of the comparator and of both inverters. It can be noticed that each device decreases rise and short times, resulting in more perfect square waves.

6.1.5 Power consumption

Finally, the power consumption has to be checked. In Figure 6-10 the sum of the currents of all branches is plotted.

The consumption behaviour shows periodical peaks of really high currents as explained before. Therefore, the average consumption must be checked. For 50ms of operation, the overall consumption for different temperatures is shown in Figure 6-11.

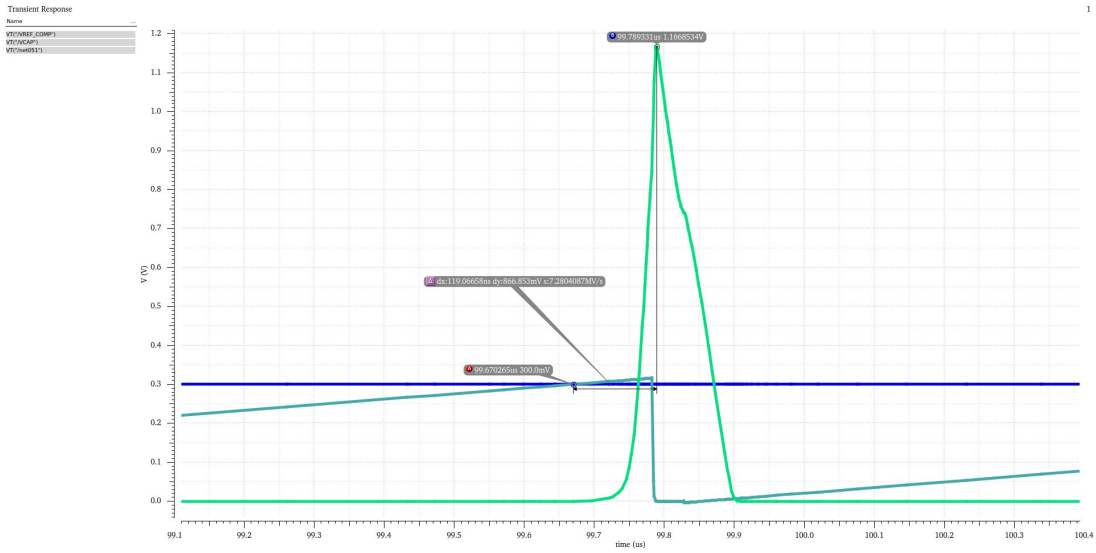

Figure 6-8: Capacitor signal, Reference signal and comparator output signal

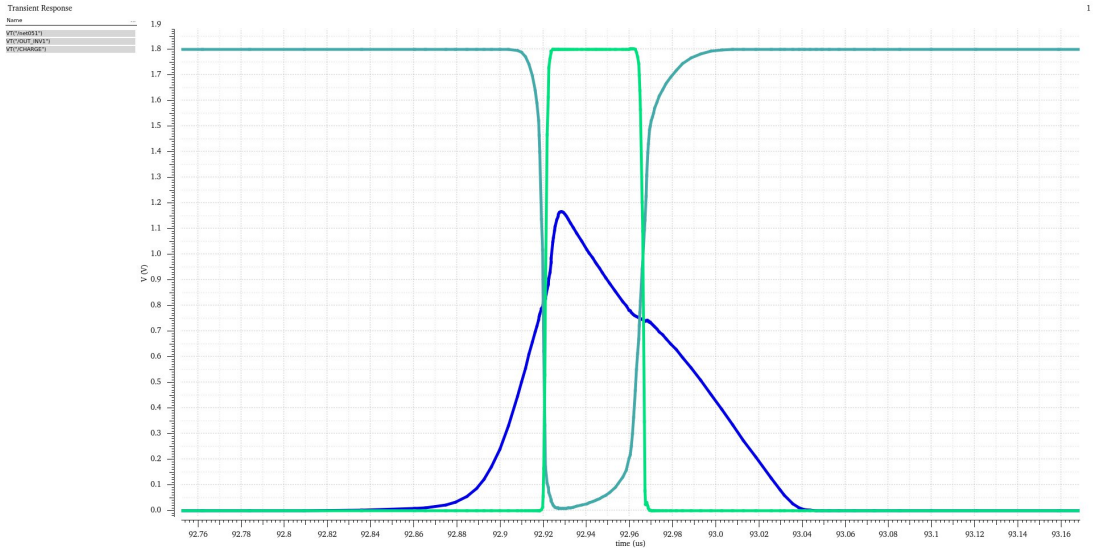

Figure 6-9: Output signals of comparator and both inverters

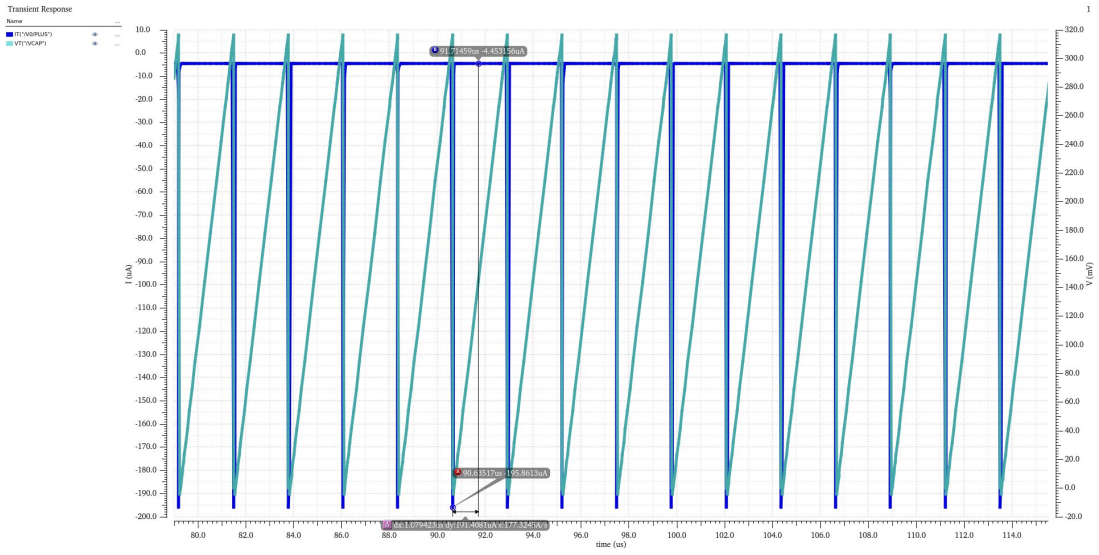

Figure 6-10: Current behaviour and capacitor voltage signal

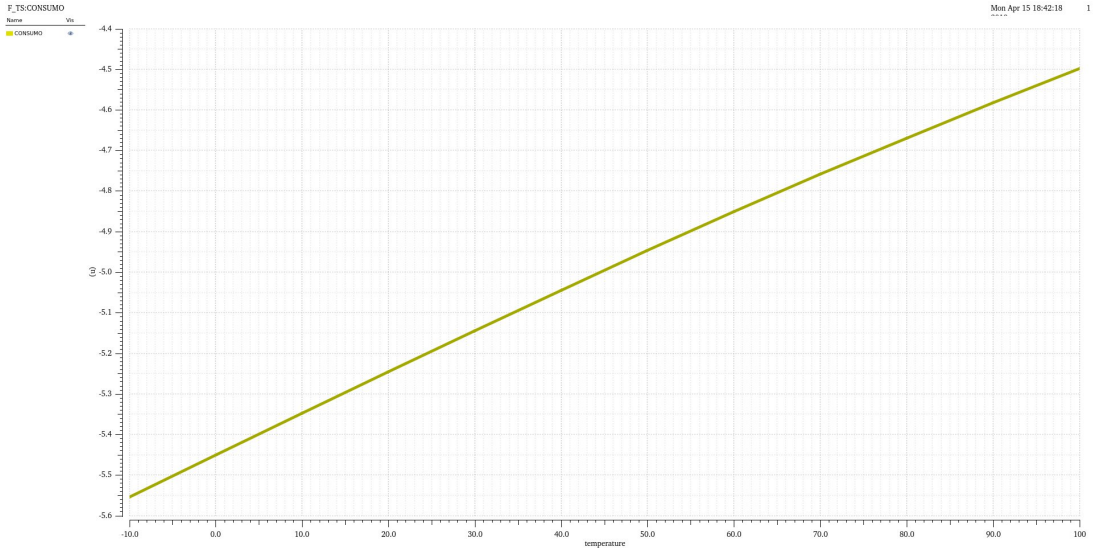

Figure 6-11: Average current consumption for different temperatures

6.2 Comparison between technologies

The Integrated Circuits for RFID systems can be implemented in different technology processes. This processes depend, for example, in the type of memory used in the tags. This will force to use transistors with some dimension differences.

In Fig. 6-12 a comparison between two technologies is done. Their main difference is the threshold of the transistors.It can be concluded that for this circuit the used technology is not so crucial, as the obtained results are similar.

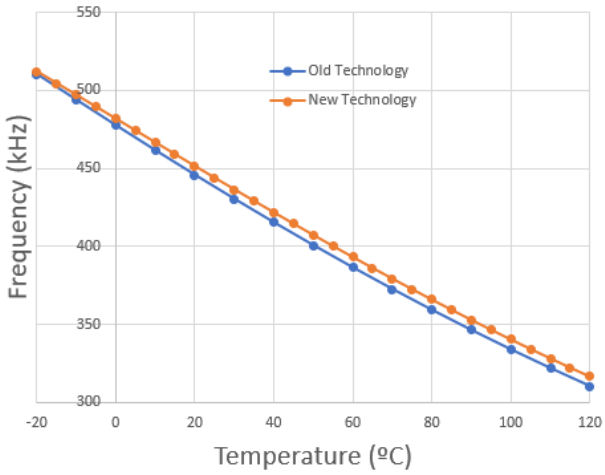

Figure 6-12: Frequency behaviour of the system developed in two different technologies

6.3 Simulation with the CLK module

The whole temperature sensor has different modules that work all of them together. As it was explained, the temperature information is encoded in the frequency of a pulse train signal. The microcontroller of the temperature sensor could extract the information from this signal, however it is not a reliable solution. In this section a more complete system is going to be studied.

The temperature dependent pulse train signal is going to be compared to a temperature independent pulse train signal, created by a clock module from the RFID Tag itself, shown in Figure 6-13. The microcontroller will count for a fixed time how many pulses are in the clock signal and in the temperature sensing interface. The clock signal count will always be the same, but the pulses count of the sensing signal will change, as its frequency changes with the temperature.

In Figure 6-13 the block used for the pulse counting is also shown. It is a Verilog block that works as an adder: each time the input signal changes from high to low it adds 1 to the

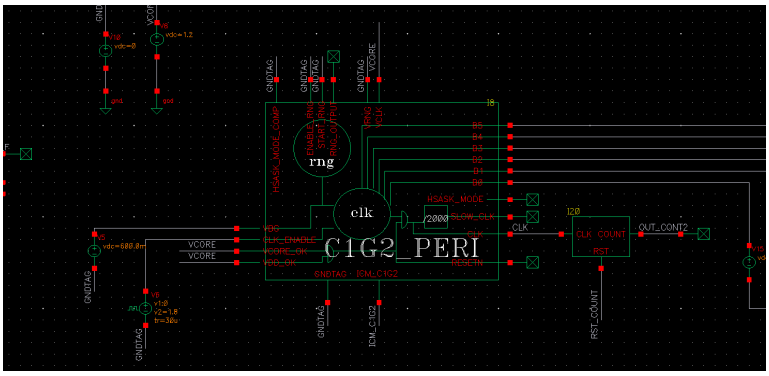

Figure 6-13: Module of the temperature independent clock signal

total sum (starting from 0). Figure 6-14 presents the implemented code.

First of all some simulations are going to be done concerning to the clock. Figure 6-15 shows both the clock signal and the sensing signal and Figure 6-16 the temperature effect on the clock signal. Apparently the clock signal has also a dependence to the temperature, however the module includes some methods to create a more stable signal (with calibration). In future steps, the temperature sensing interface can also take advantage to that temperature dependence of the clock by combining both architectures and interconnecting them.

At this point the temperature detection method explained before could be applied: compare the frequency of the clock signal and the sensing interface signal. The problem here is that this method is effective if there is a difference big enough to provide an acceptable resolution. The clock frequency is around 2MHz and the sensing signal goes from 300kHz to 480kHz. As Eq. (6.3) show, the count difference would be minimum.

$$\begin{aligned} N_{-20^oC} &= \frac{f_{clk}}{f_{-20^oC}} \approx 4 \\ N_{120^oC} &= \frac{f_{clk}}{f_{120^oC}} \approx 6 \end{aligned} \tag{6.3}$$

In future steps of the work, this issue will be resolved connecting both signals into a Time to Digital Converter (TDC), that will extract the temperature encoded information.

6.4 Post-Layout Simulation results

The layout design allows to make more precise simulations, as now all the parasitic effects can be taken into account.

Figure 6-17 shows the behaviour before the layout implementation and also the post-layout simulation including parasitic effects and real currents. The designed circuit shows good results that follow the operation expected. The delay introduced ignored in the Operation Principle

```
inout RST;
electrical RST;
inout COUNT;
electrical COUNT;
parameter integer pulse_number=10;
integer cnt;


analog begin

    @(initial_step) begin
        cnt=0;
    end

    @(cross(V(RST)-0.5,+1)) begin
        cnt = 0;
    end

    @(cross(V(CLK)-0.5,+1)) begin
        if (V(RST)<0.5)

            cnt = (cnt+1);
        else //Reset in low
            cnt = 0;
    end

    if (cnt > pulse_number )
    begin
        $strobe("***********************************************");
        $strobe("AHDL block ends simulation!!!!!!");
        $strobe("***********************************************");
        $finish;
    end
    V(COUNT)<+transition (cnt,10n,10n,10n);

end

endmodule
```

Figure 6-14: Verilog code of the pulse counter module

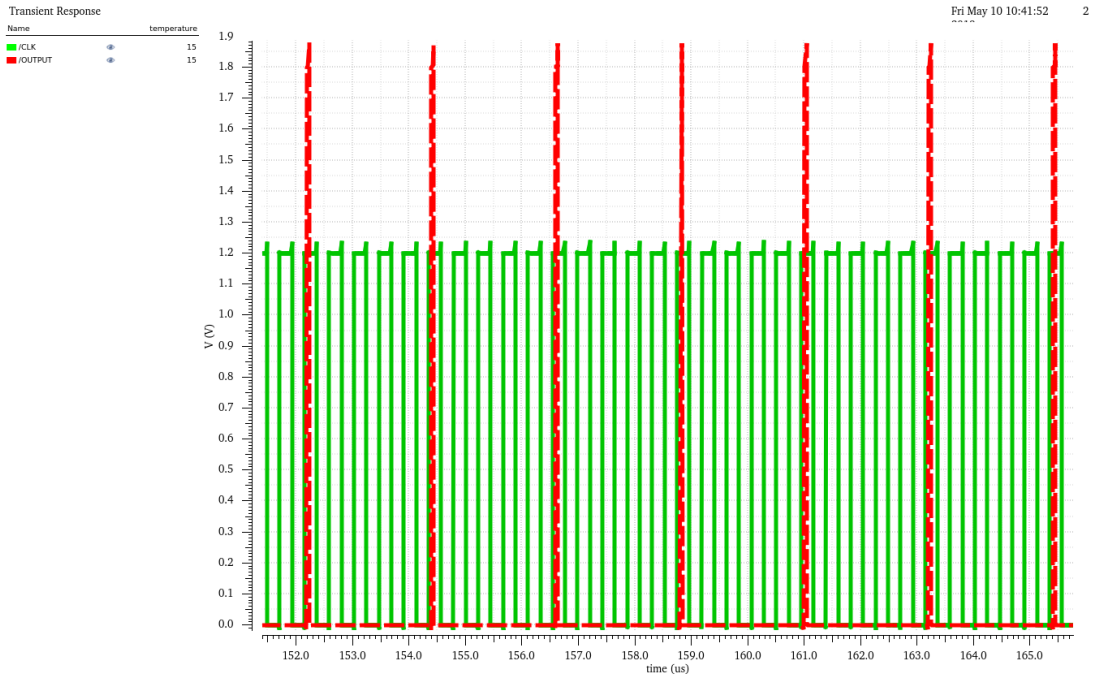

Figure 6-15: Output signals of the clock and the temperature sensing interface

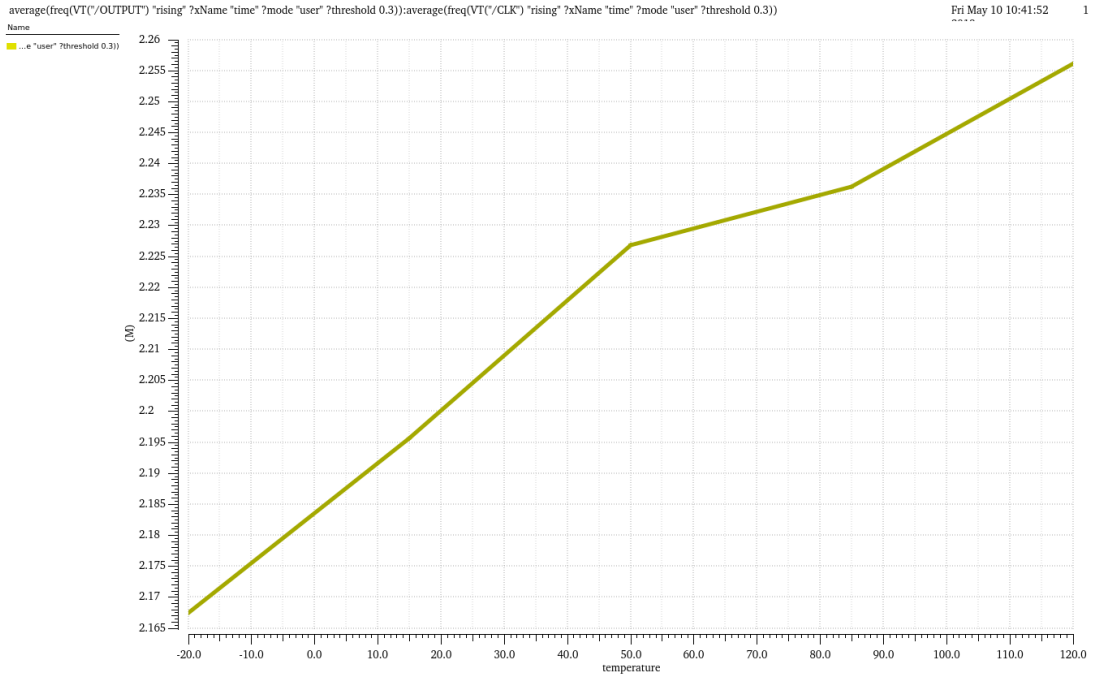

Figure 6-16: Frequency behaviour of the output signal of the clock module

and the parasitic capacitance are the cause of the frequency offset. The temperature sensor covers 140C, from -20C to 120 C, with a resolution of $1.2\frac{kHz}{}$.The power consumption goes from 5.1 μW to 7.6 μW.

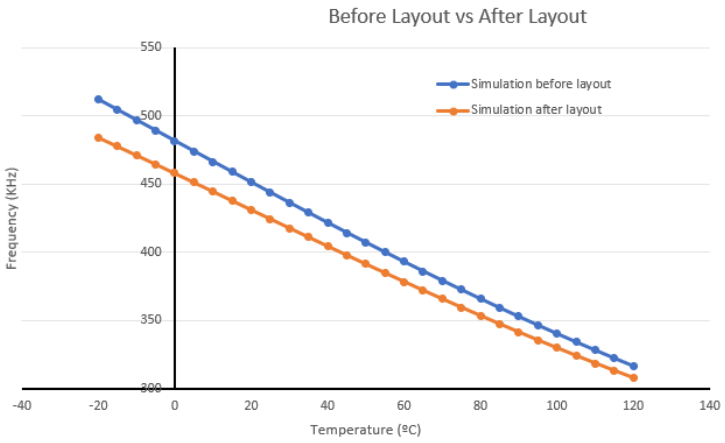

Figure 6-17: Frequency behaviour before layout vs after layout

The study of the effect of process variations is also done. The first approach is done with a Monte Carlo Sampling simulation, evaluating the system at 27°C with 120 points. The obtained result is shown in Figure 6-18.

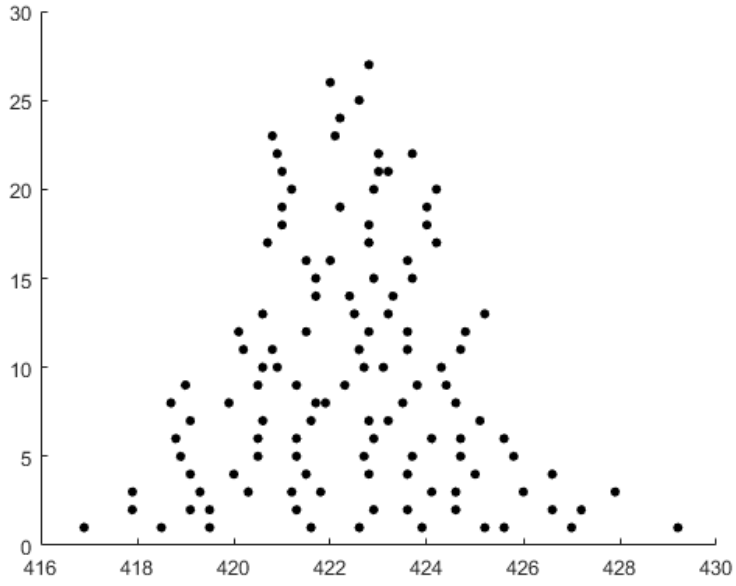

Figure 6-18: Monte Carlo Sampling Simulation after layout

Next step is to measure the system with more strict conditions. For that the sensor is going to be evaluated at different corners, introducing the effect of the process to all the components in the architecture. Figure 6-19 presents the frequency behaviour at different corners and also

an approximation of the committed error in the temperature.

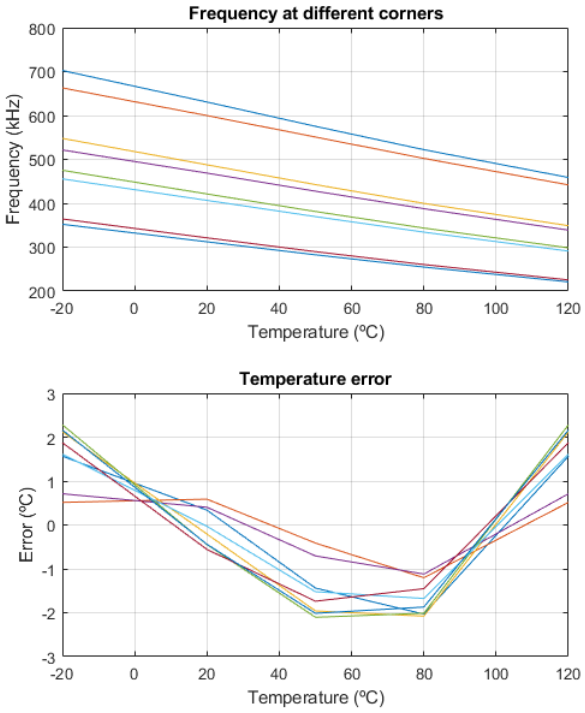

Figure 6-19: Effect of the corners to the behaviour of the system

For the error estimation a calibration process must be done. In future steps of the work, once included the TDC and the clock reference, a more precise calibration could be done. However at a first approach this method is sufficient to evaluate the performance of the temperature sensing interface. First of all, each corner curve is approximated to an ideal line, which will be extracted by taking the frequency value at -20°C and at 120°C. Then applying the steps shown in Eqs. (6.4), the errors of Figure 6-19 are obtained. Therefore, this is a 2-point calibration system.

$$\begin{aligned} offset &= f_{simulation} - f_{ideal} \\ \%meas &= 100 * \frac{offset - \mu(offset)}{\Delta f} \\ Error_{temp} &= (120 - (-20)) * \frac{\%meas}{100} \end{aligned} \tag{6.4}$$

Finally, the robustness of the sensing interface to the variations of the bandgap voltages is checked. Figure 6-20 shows the frequency error obtained at different supply voltages (variation of ±5%), presenting an acceptable voltage supply immunity. In Operation Principle Chapter (4) it was decided to make the fixed voltage, V_A, equal to the reference voltage of the

comparator, V_{ref}, as a countermeasure to voltage variations. Figure 6-21 reveals the achieved improvement: an error of 41% has been reduced to a 0.56%.

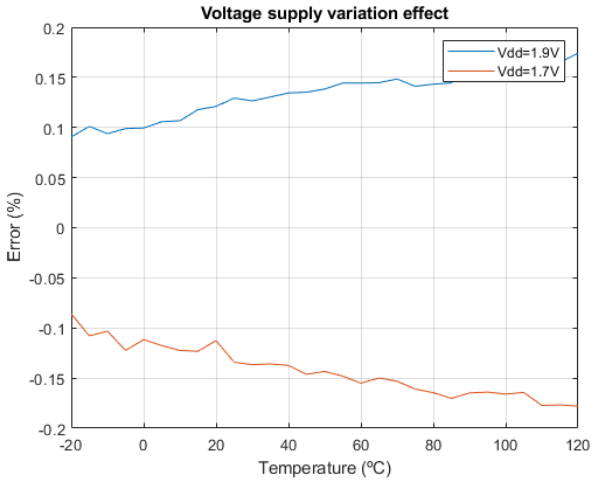

Figure 6-20: Effect of the voltage variation in the frequency

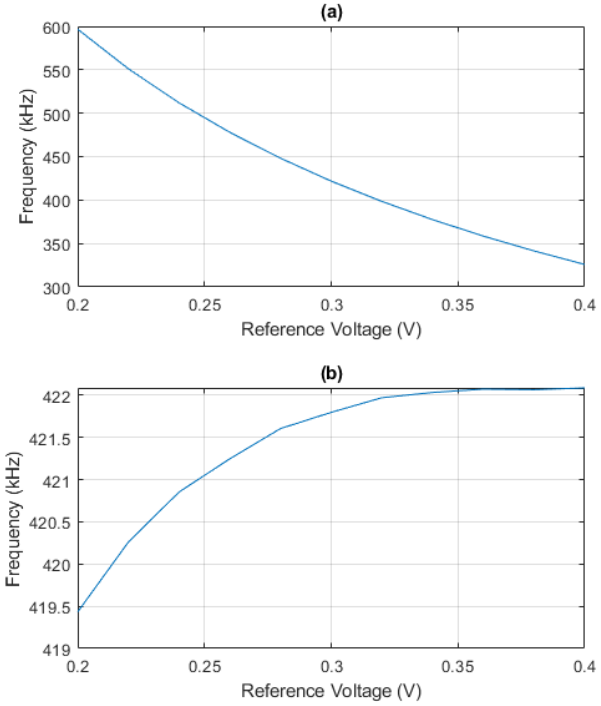

Figure 6-21: Reference voltage variation effect to the frequency at 27C (a) V_A independent to V_{ref}, (b) $V_A = V_{ref}$

Chapter 7

Project Budget

In this chapter the budget of the developed project will be detailed. It will be divided in different items:

- **Software.** For the development of the project two different software licences where needed: Cadence and Calibre.
- **Human Work.** Costs involving the human resources that took part in the development of the project.
- **Fabrication.** The designed sensor will be fabricated in the process TSMC 0.18 CMOS Logic or Mixed-Signal/RF.
- **Indirect Costs.**

In Fig. 7-1 all the costs of the project are detailed. The overall project budget is 27.230€.

		Time (months)	Intensity	Cost
SW	Cadence	3	50%	8000
	Calibre	1	50%	5000
			Total	**13000**

		Time (hours)	Cost x hour	Cost
Human Work	Junior Engineer	350	25	8750
	Supervisor	20	90	1800
			Total	**10550**

	Block Cost	Occupation	Cost
Fabrication	3140	50%	1570
		Total	**1570**

	Cost
Indirect Costs	2110
Total	**2110**

Figure 7-1: Costs of the project

Chapter 8

Conclusions and Future Work

The presented temperature sensor interface has shown acceptable results and operation. A paper (Appendices) has been one of the results of this project and it is currently being evaluated to be presented in the DCIS Conference in November of 2019.

Next step of the project is to fabricate it and make real measurements. In the future, there are also some aspects of the sensor that could be improved.

8.1 Increase the Frequency range

In the Operation Principle chapter, the behaviour of the temperature sensing interface was deduced with the Eq. (8.1)

$$f_{temp} = \frac{k * V_A}{C * V_{ref} * R_{ref} * [1 + \alpha * (T - Tref)]} \tag{8.1}$$

The frequency range is set by the temperature dependence of the resistor. Then, the frequency range would be fixed just by this parameter. If more temperature dependencies are introduced in the equation, it is obvious that the frequency range will depend on more parameters and therefore the frequency range will increase.

At this point, the chosen resistor has a positive temperature coefficient ($\alpha = 0.0038^oC^{-1}$), which means that the resistance increases with the temperature, which leads to a lower frequency (it is in the denominator). If the goal is to increase the frequency range, the new temperature coefficients cannot destruct each others behaviours. That means that in the denominator only positive coefficients can be added and in the numerator just negative ones. That way at higher temperatures, the numerator will be decreased and the denominator will be increased, following to a much lower frequency than before (and viceversa).

Going back to the Eq. (8.1) the temperature dependencies can be introduced to these

parameters: capacitor, reference voltage of the comparator (V_{ref}) and fixed voltage of the gain boosting stage ($V_A = V_{fix}$). The found solution in this project has been to work on this last parameter.

Until now this voltage has been generated by an external voltage supply or a bandgap, which have a fixed value. It is known that this exact voltage can be obtained with a resistor and a fixed current, as shown in Eq. (8.2). If a temperature independent current is obtained, then a temperature dependent resistor can be introduced in the architecture.

$$V_{fix} = V_A = i * R \rightarrow V_A = i_{fix} * R * [1 + \alpha * (T - Tref)] \tag{8.2}$$

As explained before, this resistor must decrease its valued at higher temperature in order to decrease the numerator of the operation principle equation. Therefore, the temperature coefficient has to be negative. The Eq. (8.3) is the result of introducing this effect.

$$f_{temp} = \frac{k * i_{fix} * R_{VA} * [1 + \alpha_- * (T - Tref)]}{C * V_{ref} * R_{ref} * [1 + \alpha_+ * (T - Tref)]} \tag{8.3}$$

Going back to the resistor study made in the Circuit Design Chapter (5) (Figure 5-1), the best solution is to choose the Rnhpoly type resistor for this stage, with a temperature coefficient equal to $\alpha = -0.001156°C^{-1}$. The value of the generated voltage will be chosen to be 0.26V therefore the resistor must have a value of 514.524kΩ for a fixed current of 500nA. Figure 8-1 shows the resultant schematic for this new stage.

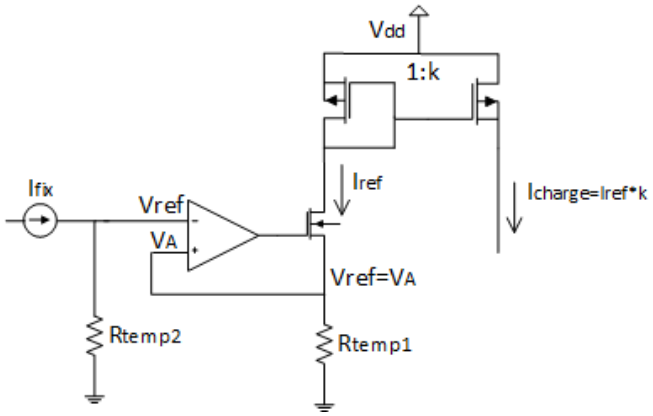

Figure 8-1: Schematic of the new architecture

In Figure 8-2 the frequency behaviour with the new branch and without it are plotted. At first, the used current is ideal. With this method the frequency range has increased from 200kHz to 230KHz (a 15% of increment). However some other aspects of the temperature sensing interface have been deteriorated.

On the one hand, the size of the chip is increased. The needed resistance value is really high which leads to a higher active area. Figure 8-3 shows the layout of the new resistors next

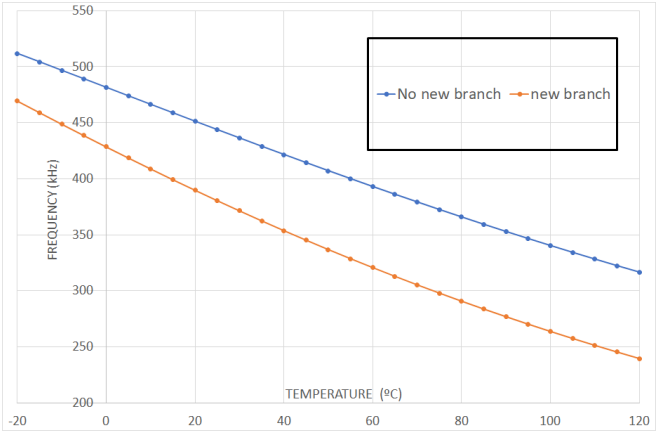

Figure 8-2: Frequency behaviour of the system with the new branch and without it

to the designed temperature sensor. The length of the resistors ($L = 100\mu m$) fits with the length of the chip, but the width ($W = 30\mu m$) has to be added to the chip. The total area would be 0.0229 mm^2 , which means an increment of 19%. This increase in the active area results in higher costs for the chip.

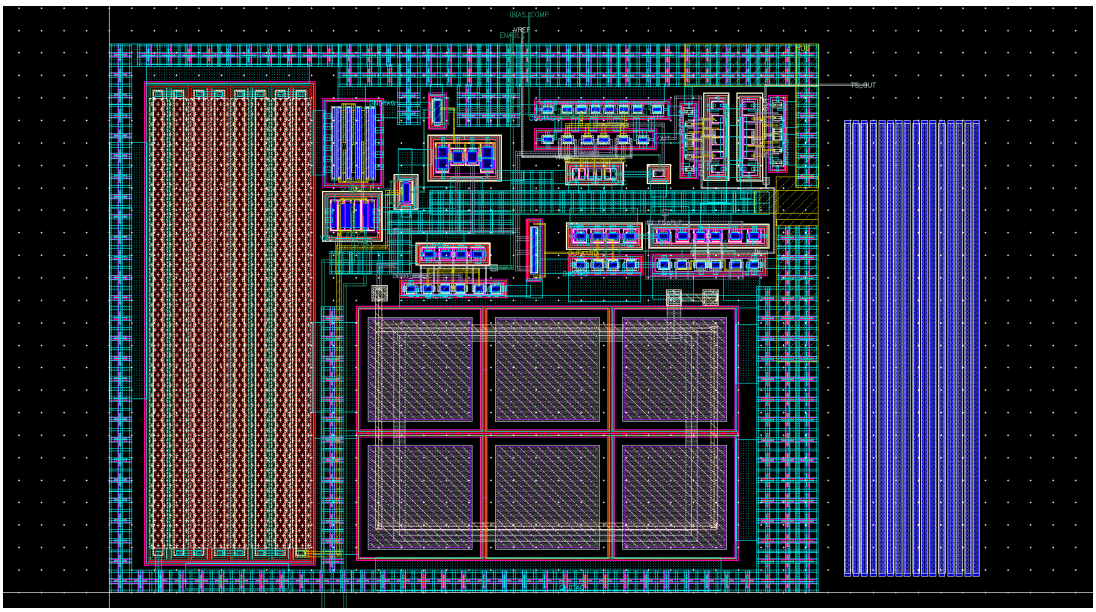

Figure 8-3: Layout of the resistors of the new branch next to the layout of the designed chip

At first, the simulations using an ideal current show a good behaviour. However, when introducing real currents, that also depend on the temperature, the second order effects have increased with this new branch. This will affect to the calibration process, making it more complicated and therefore more expensive.

With Figure 8-4 it can be concluded that this is a bad solution, the frequency range has been even decreased with this system (it covers 170kHz now).

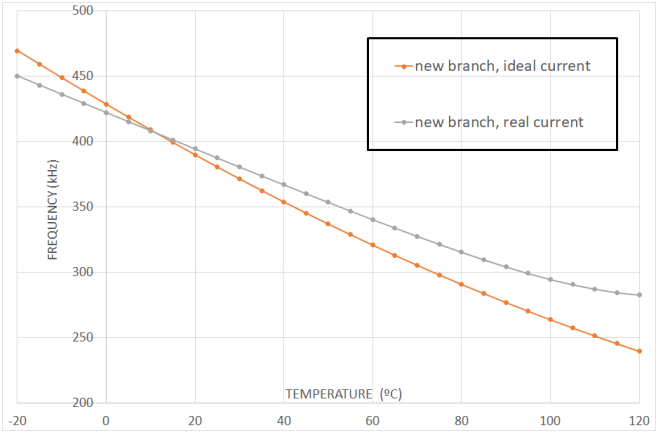

Figure 8-4: Frequency behaviour of the system with the new branch using real and ideal currents

Therefore, more time must be spent to think about new ways to increase the frequency range without deteriorating other crucial aspects of the temperature sensing interface.

8.2 Power Consumption

The implemented temperature sensor is designed for RFID applications. Therefore the power consumption is a crucial parameter of the chip. The temperature sensor interface shows an acceptable power consumption: from 5.1 μW to 7.6 μW. However, there are some better chips in the State of the Art concerning to power consumption.

One of the most important stages is the inverters chain at the end of the architecture. As it was explained in previous chapters, it must be ensured that both transistors never are activated at the same time. that would lead to a higher current consumption. For that the input square waves should be as perfect as possible. In the future, this stage could be improved in terms of current consumption.

Another important stage is the current mirror. It was explained that the output current is the half of the reference in order to minimize the total current consumption. On the one hand, this current could be decreased, however, a study should be done and check if the capacitor is optimally charged. On the other hand, the reference branch has a set value of around 1.5μA due to the Gain Boosting stage: a fixed voltage is applied to a resistance, therefore the current is also fixed. By changing the resistor value and the fixed voltage this reference current could be decreased. However, this would change the whole behaviour of the system and it should be studied from the start.

8.3 Corners and calibration

In previous sections a small study of the different corners is done, shown in Figure 8-5. A first calibration method is also explained, however it is not sufficient.

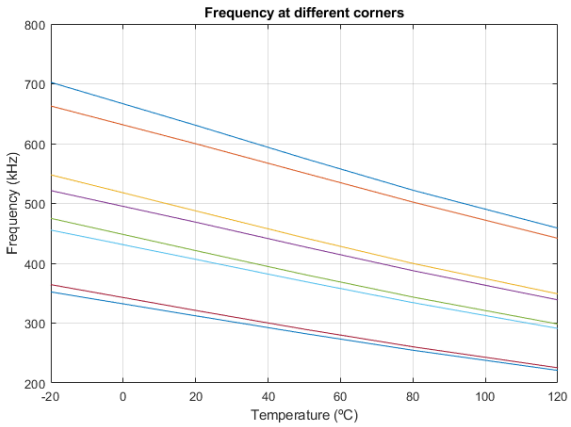

Figure 8-5: Frequency behaviour at different corners

In future steps of the work, once the TDC is selected and the whole system is working, a more precise and convenient calibration should be done.

8.4 Other temperature dependencies

Remembering the comparison between the theoretical behaviour and the simulation, Figure 8-6, it is noticed that an improve in the linearity of the frequency is achieved. This second order compensation comes from other temperature dependencies.

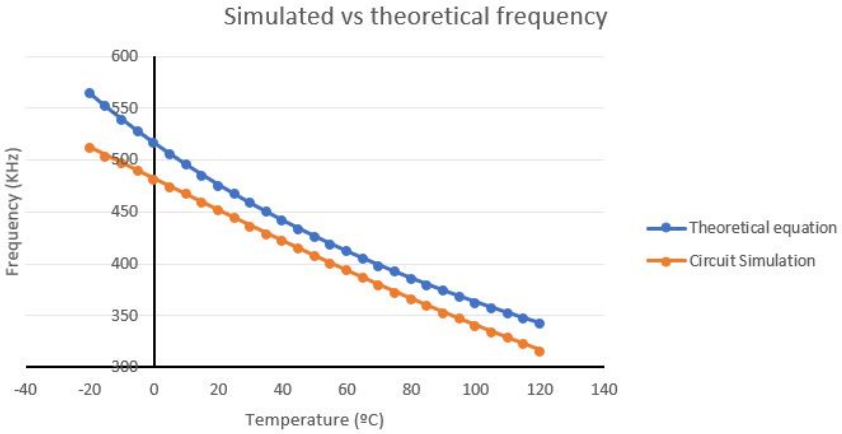

Figure 8-6: Theoretical behaviour vs Simulation

On the one hand, the capacitor should be charged till a threshold, which is the voltage reference of the comparator. This should happen independently to the temperature. However

the obtained results, Figure 8-7, indicate that the capacitor is charged to some mV higher. This voltage difference, has a direct impact on the frequency.

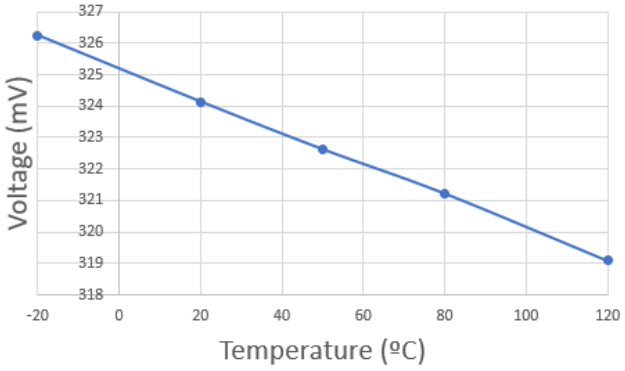

Figure 8-7: Maximum capacitor voltage charge at different temperatures

On the other hand, the comparator and the inverters introduce a delay in the signal, which is the time that the signal needs to travel through them. This delay is also dependent to the temperature (transistors temperature dependence) and has a direct effect on the frequency. Changing the resistance and the capacitor to ideal components (no temperature dependence), the effect of the inverters can be observed in Figure (8-8).

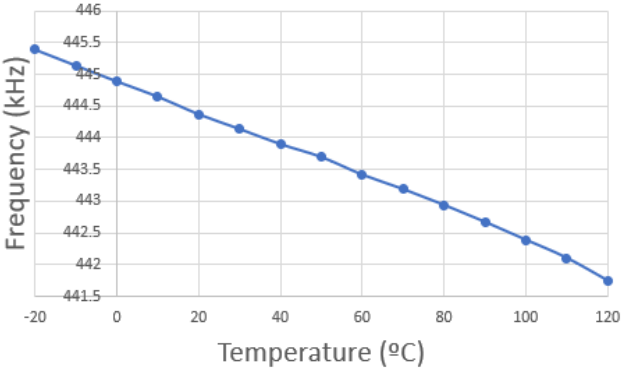

Figure 8-8: Effect of the delay time introduced by the comparator and the inverters

A more precise theoretical equation should include this effects, as seen in Eq. (8.4)

$$f_{temp} = \frac{k * V_A}{C * V_{ref} * [1 + \alpha_V * (T - Tref)] * R_{ref} * [1 + \alpha_R * (T - Tref)] + k * V_A * t_{delay}[1 + \alpha_t * (T - Tref)]} \tag{8.4}$$

8.5 Conclusion

The results obtained in the simulations are compared with State of the Art sensors in Table 8.1. It can be seen how the developed interface has a remarkable temperature range of 140°C with one of the smallest area requirements. Regarding the sensibility it also offers the highest value from the temperature to frequency alternatives with a really adjusted power consumption. It is shown that the designed sensor achieves a trade-off between the important parameters: consumption below 10μW, wide temperature range (from -20°C to 120°C), small size, acceptable frequency linearity, good resolution and good immunity to voltage variations. Measurement results will be obtained in future steps of the work, after fabricating the device. Additionally, this module will be connected to a TDC which will extract the encoded temperature information. In conclusion, the explained sensor finds a compromise between all the aspects resulting into a multipurpose solution for RFID applications and for that reason a paper has been sent to the DCIS Congress 2019, appendices (A), and is now being evaluated.

Table 8.1: Comparison of different temperature sensors

Sensor	**Technology**	**Temp. Range (°C)**	**Area (mm^2)**	**Supply Voltage (V)**	**Consumption(μW)**	**Sensing Resolution**
[6]	0.18	-30 to 60	0.014	1	0.35	0.3°C
[7]	0.6	-40 to 125	0.371	5	70 to 125	-
[8]	0.18	-20 to 80	0.089	1.8	0.820	0.09°C
[9] (A)	0.18	-40 to 120	0.024	1.2	3	335 $\frac{Hz}{^oC}$
[9] (B)	0.18	-40 to 120	0.019	1.2	1.9	460 $\frac{Hz}{^oC}$
[11]	0.18	-20 to 120	0.118	1.8	93	0.048°C
[12]	0.18	0 to 100	0.0004	1.8	163 to 212	0.058°C
[10]	0.35	-10 to 120	0.84	2	3.9	±2°C
This work	0.19	-20 to 120	0.019	1.8	5.1 to 7.6	1200$\frac{Hz}{^oC}$

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Appendices

Appendix A

DCIS 2019 Paper

Low-power frequency-conversion based temperature sensor for long-range passive RFID sensor applications

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dept. name of organization (of Aff.)
name of organization (of Aff.)
City, Country
email address

2nd Given Name Surname
dept. name of organization (of Aff.)
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City, Country
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3rd Given Name Surname
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name of organization (of Aff.)
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***Abstract*—A low-power frequency-conversion based temperature sensor interface optimized for passive UHF RFID applications have been designed and implemented. The interface is based on a reference capacitor that is charged by a temperature dependent current and discharged by a hysteresis loop. The circuit has been implemented in a standard CMOS 180nm process. The post-layout simulations show that the presented architecture is able to compensate for variations on the bandgap reference and cover a wide temperature range (140ºC) with minimum active area ($0.019mm^2$), reduced power consumption ($\cong 6.5\mu W$), and reduced effect of PVT variations, accomplishing the design objectives.**

***Index Terms*—temperature sensor, low power, RFID, PWM**

I. Introduction

UHF Radio-frequency identification (RFID) systems have experienced a great evolution and market growth in the last decade. The main characteristics of this technology are its low cost, small size, long communication-range and possibility to operate without a battery. These characteristics make the technology ideal for logistics and automatic trazability.

In addition to these applications of passive RFIDs, it is also possible to attach a sensor to the tag and use the system for remote sensing. Among the different magnitudes to be measured temperature is one of the most interesting. A temperature sensors developed for RFID passive applications needs to be designed according to specific design criteria: First, it must show good results in terms of power consumption ($< 10\mu W$), as the chip has an autonomous power. Second, the operation voltage needs to be small in order to allow efficient operation of the power harvester. Next, the sensor should cover a wide temperature range but with high linearity in order to avoid expensive calibration procedures. Last, the size should be reduced.

Temperature sensors based on a time-domain operation principle are a good solution to approach to the desired specifications of RFID tags [2] - [5]. However, is not possible to accomplish all of them at the same time. Ultra low power consumption is achievable ($< 1\mu W$) in some cases but at the expense of increasing the effect of the process and voltage variations. 2-point calibration is usually needed in order to compensate for accuracy errors and linearity deviations caused by fabrication process variations [3]. Some work such as in [6] and in [7] report excellent results in terms of temperature range, resolution and inaccuracy, but show higher power consumption ($93\mu W$ and $160\mu W$). It is clear, that a trade-of between the parameters is necessary and each design needs to be optimized for each application scenario. In this work, a temperature sensor has been designed for ultra low-cost and long temperature range RFID systems, therefore paying special attention to maximum measuring range with minimum design area and without affecting much to the rest of parameters.

This work is organized as follows: The proposed temperature sensor interface is reported in Section II. Section III presents the sensor implementation. Finally, Section IV discusses the post-layout simulation results. Last, the conclusions are presented in Section V.

II. Operation Principle

The Block Diagram of the whole temperature sensor system is presented in Fig. 1. A bandgap will be used in order to provide reference voltages and bias currents to other blocks. The temperature sensing interface transforms the temperature into a clock signal, encoding the information into its frequency . The clock generator is a block from the RFID tag itself and it will be used in the Time-To-Digital block to extract the information from the generated temperature dependent signal using the system clock as a reference.

The operation principle of the temperature sensing interface, Fig.2, basically consists of a capacitor that is charged by a temperature dependent current, I_{charge} and discharged by a hysteresis loop. The capacitor starts completely discharged, at 0V. V_{out} then equals also to 0 and the switch is open. The top current will charge the Capacitor, until $V_{cap} = V_{ref}$, at that point the output of the comparator will be a logical high. The next two inverters create a square wave in the output with short rise and fall times. V_{out} closes the switch discharging the capacitor until $V_{cap} = 0$V. At that point, the charging phase starts again.

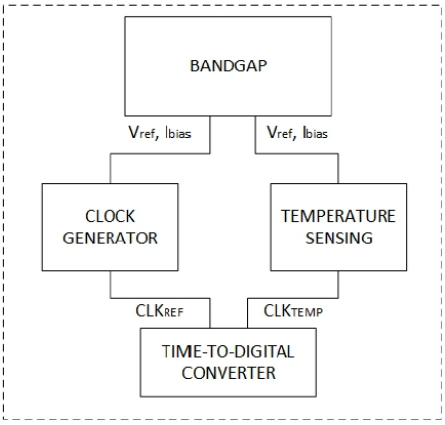

Fig. 1. Block Diagram of the whole Temperature Sensor System

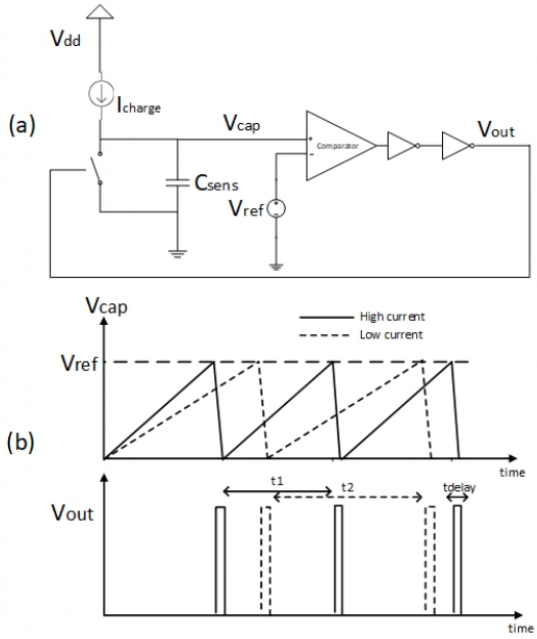

Fig. 2. a) Simple schematic of the proposed temperature sensor, b) Resultant output and capacitor waveforms

The resulting waveform in the capacitor, V_{cap}, is a saw-tooth signal, with a slope depending on the charging current. In the output, V_{out}, there is a pulse train wave, whose delay between pulses also depends on I_{charge}. Concretely, both depend on how fast the capacitor has been charged till V_{ref} (voltage reference of the comparator). This speed will change with I_{charge}: the higher the current, the faster the charging. Finally, this current will depend on the temperature.

With this system a temperature dependent signal is generated: V_{out} has a variable time between pulses depending on the charging current (t_1 and t_2 in Fig. 2), and therefore a variable clock frequency. The period of the generated pulse train signal is extracted from the basic equation of a capacitor, Eq. (1), and it will be the time needed to charge the capacitor plus a delay time, which is the discharging time of the capacitor and the traveling time through the comparator and inversors. This t_{delay} is also the width of the generated pulses, so it should be high enough in order to have pulses that can be detected, but also low enough to produce a negligible effect in the frequency. From Fig. 2 it is known that the capacitor charges from 0V to V_{ref}, and that i equals I_{charge}.

$$i(t) = C\frac{dV(t)}{dt} \rightarrow \Delta t = C\frac{\Delta V}{i} + t_{delay} \approx C\frac{V_{ref}}{i_{charge}} \quad (1)$$

The temperature dependence of the system is introduced by a resistor, modeled by the Eq. (2). The circuit shown in Fig. 3 generates the temperature variable current, I_{charge}. Long length transistors are used for the current mirror in order to minimize the voltage supply dependence and the Early effect. The fixed voltage is implemented with a Gain Boosting stage.

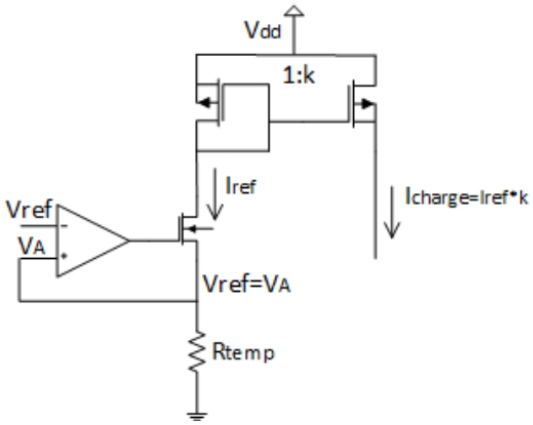

Fig. 3. Temperature dependence generation

$$R_{temp} = R_{ref} * [1 + \alpha * (T - Tref)] \quad (2)$$

Therefore,

$$I_{ref} = \frac{V_A}{R_{temp}} = \frac{V_A}{R_{ref} * [1 + \alpha * (T - Tref)]} \quad (3)$$

Where R_{ref} is the resistance at T_{ref}, T_{ref} = 27 °C and α = temperature coefficient.

The charging current will be a copy of a reference current, multiplied by a factor of k.

$$I_{charge} = k * \frac{V_A}{R_{ref} * [1 + \alpha * (T - Tref)]} \quad (4)$$

Including the temperature effect in the Eq. (1), and ignoring the delay introduced by the hysteresis loop, the frequency of the pulse train is modeled by the Eq. (5)

$$f_{temp} = \frac{k * V_A}{C * V_{ref} * R_{ref} * [1 + \alpha * (T - Tref)]} \quad (5)$$

From Eq. (5) it can be deduced that the frequency is strongly dependent to the reference voltage of the comparator (charging threshold of comparator) and to the fixed voltage of the reference current (V_A). Then, unpredictable voltage variations from the bandgap will produce also an offset in the frequency. Making $V_A = V_{ref} = 0.3$V this effect is decreased.

III. Implementation

The sensor has been designed in p-substrate 0.18-μ CMOS technology and PMOS and NMOS transistors have been used in the whole architecture, with a voltage supply of 1.8V. The resistor has a value of 180kΩ and the most temperature dependent resistors available in this process have been used: n-well resistors under diffusion with a temperature coefficient of $\alpha = 0.0038$ °C^{-1}. The Metal-Insulator-Metal (MIM) capacitor has a value of 6pF and a small temperature coefficient.

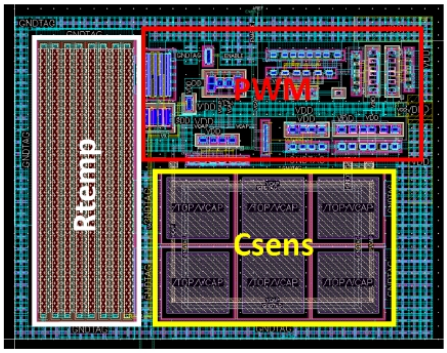

Fig. 4. Layout of the temperature sensing interface

In Fig. 4 the layout of the temperature sensing interface is shown where two extra inverters have been added to the original architecture in order to minimize the parasitic capacitance effects when connecting this module to others in the whole temperature sensor. The resultant chip has an active area of 0.019mm^2.

IV. Post-Layout Simulation Results

Fig. 5 shows the theoretical behaviour deduced in the Eq. (5) and also the post-layout simulation of the implemented architecture including parasitic effects and real currents.

The designed circuit shows good results that follow the operation expected. The delay introduced ignored in the Operation Principle and the parasitic capacitance are the cause

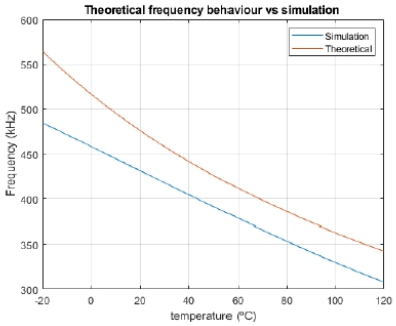

Fig. 5. Theoretical frequency behaviour vs post-layout simulation

of the frequency offset. The temperature sensor covers 140°C, from -20°C to 120 °C, with a resolution of $1.2\frac{kHz}{°C}$.The power consumption goes from 5.1 μW to 7.6 μW.

From theoretical study to simulation values the circuit improves in terms of linearity. The reason to this is that the temperature dependence is not just introduced by the resistor. On the one hand, the capacitor should be charged just to V_{ref} before the comparator detects it and the discharge starts. However, simulation results show that the comparator have a small temperature dependency that affect to the final frequency. On the other hand, the inverters after the comparator generate a delay time, t_{delay}, which also depends on the temperature. These two effects contribute to the final linearity improvement in the simulation curve.

The study of the effect of process variations is also done. Fig. 6 shows a Monte Carlo Sampling post-layout simulation at 27°C and Fig. 7 presents the frequency behavior at different corners. Fig. 7 also shows an approximation of the committed error in the temperature.

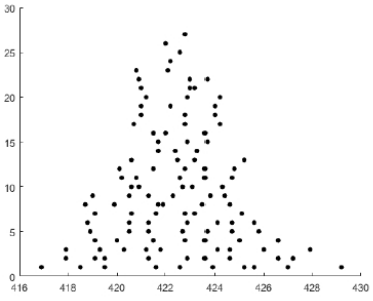

Fig. 6. Monte Carlo Sampling Simulation after layout

Finally, the robustness of the sensing interface to the variations of the bandgap voltage (VREF) is checked. Fig. 8 shows the frequency error obtained at different supply voltages (variation of $\pm 5\%$), presenting an acceptable voltage supply

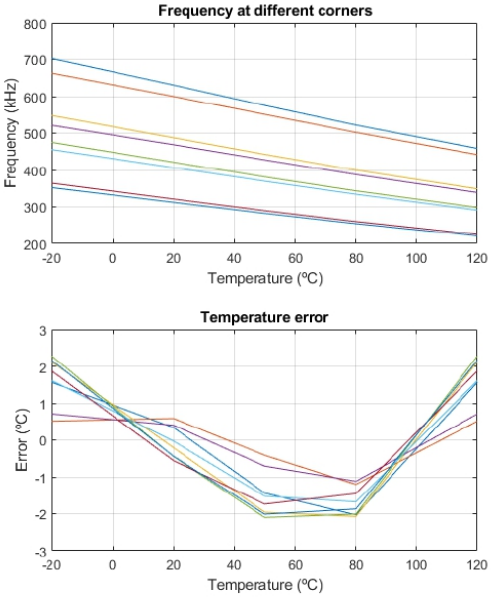

Fig. 7. Effect of the corners to the behaviour of the system

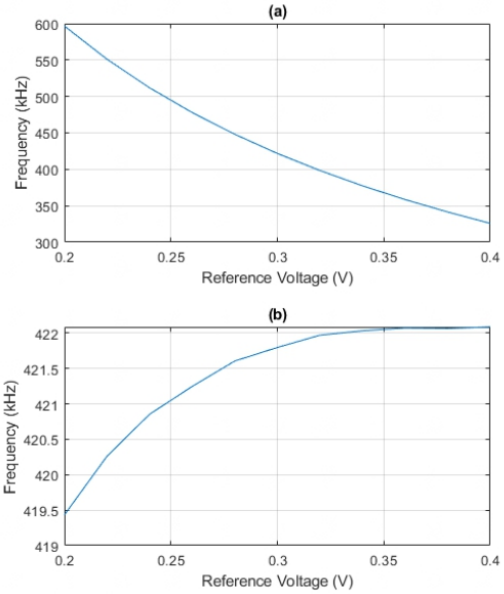

Fig. 9. Reference voltage variation effect to the frequency at 27°C (a) V_A independent to V_{ref}, (b) $V_A = V_{ref}$

immunity. In section II it was decided to make the fixed voltage, V_A, equal to the reference voltage of the comparator, V_{ref}, as a countermeasure to bangap voltage variations. Fig. 9 reveals the achieved improvement: an error of 41% has been reduced to a 0.56%.

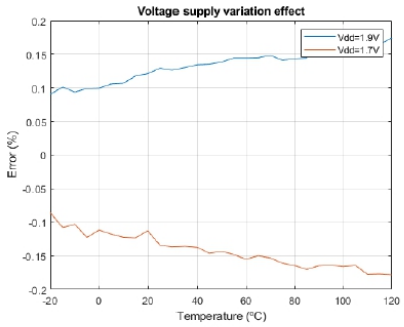

Fig. 8. Effect of the voltage variation in the frequency

The results obtained in the simulations are compared with the state of the art in Table I. It can be seen how the developed interface has a remarkable temperature range of 140ºC with one of the smallest area requirements. Regarding the sensibility it also offers the highest value from the temperature to frequency alternatives with a really adjusted power consumption.

V. Conclusion

This paper has proposed a reliable temperature sensing interface that fulfills the requirements of RFID passive tags. Table I compares the performance results of the presented temperature sensor and State of the Art sensors. It is shown that the designed sensor achieves a trade-off between the important parameters: consumption below 10μW, wide temperature range (from -20°C to 120 °C), small size, acceptable frequency linearity, good resolution and good immunity to voltage variations. Measurement results will be obtained in future steps of the work, after fabricating the device. Additionally, this module will be connected to a TDC which will extract the encoded temperature information. In conclusion, the explained sensor finds a compromise between all the aspects resulting into a multipurpose solution for RFID applications

Acknowledgment

References

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TABLE I
COMPARISON OF DIFFERENT TEMPERATURE SENSORS

Sensor	Technology	Temp. Range (°C)	Area (mm^2)	Supply Voltage (V)	Consumption(μW)	Sensing Resolution
[1]	0.18	-30 to 60	0.014	1	0.35	0.3 °C
[2]	0.6	-40 to 125	0.371	5	70 to 125	-
[3]	0.18	-20 to 80	0.089	1.8	0.820	0.09 °C
[4] (A)	0.18	-40 to 120	0.024	1.2	3	335 $\frac{Hz}{^oC}$
[4] (B)	0.18	-40 to 120	0.019	1.2	1.9	460 $\frac{Hz}{^oC}$
[6]	0.18	-20 to 120	0.118	1.8	93	0.048
[7]	0.18	0 to 100	0.0004	1.8	163 to 212	0.058
[5]	0.35	-10 to 120	0.84	2	3.9	$\pm$2 °C
This work	0.18	-20 to 120	0.019	1.8	5.1 to 7.6	1200$\frac{Hz}{^oC}$

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