Middleton, C., Dalcanale, S., Uren, M., Pomeroy, J., Uren, M. J., Chang, J., ... Kuball, M. (2019). Thermal transport in Superlattice Castellated Field Effect Transistors. *IEEE Electron Device Letters*, *40*(9), 1374-1377. https://doi.org/10.1109/LED.2019.2929424

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/LED.2019.2929424, IEEE Electron Device Letters

Thermal Transport in Superlattice Castellated Field Effect Transistors

Callum Middleton, Stefano Dalcanale, James W. Pomeroy, Michael J. Uren, *Member, IEEE*, Josephine Chang, Justin Parke, Ishan Wathuthanthri, Ken Nagamatsu, Sarat Saluru, Shalini Gupta, Robert Howell, and Martin Kuball, *Senior Member, IEEE*

***Abstract*— Heat extraction from novel GaN/AlGaN superlattice castellated field effect transistors developed as an RF switch is studied. The device thermal resistance was determined as 19.1 ± 0.7 K/(W/mm) from a combination of Raman thermography measurements, and gate resistance thermometry. Finite element simulations were used to predict the peak temperatures and show that the three-dimensional gate structure aids the extraction of heat generated in the channel. The calculated heat flux in the castellations shows that the gate metal provides a high thermal conductivity path, bypassing the lower thermal conductivity superlattice, reducing channel temperatures by as much as 23%.**

***Index Terms*—AlGaN, FET, Temperature**

I. Introduction

GaN has a wide bandgap, high breakdown field, and high carrier mobility [1]. These desirable characteristics have led to wide ranging applications of GaN-based devices, from high-frequency, high-power RF, through to efficient DC power converters [2]. Superlattice castellated field effect transistors (SLCFETs) are a new RF switch design [3]. They benefit from a reduced on-state resistance and low off-state capacitance, resulting in a cut off frequency up to eight times higher than other FET based RF switches [4]. SLCFETs can provide the low loss, broadband performance of RF MEMS as well as the speed and reliability of FETs [5]. SLCFETs have small feature sizes and heating is localized within a channel region smaller than 160 nm, making heat extraction a challenge. If heat is allowed to build up in the small features, this can cause an increase in ON-resistance, and potentially early device failure. Here we study their thermal dissipation, which must be understood because of the potential adverse effect of channel temperature on electrical device performance and reliability.

To extract the temperatures experienced in the device, micro-Raman thermography and gate resistance thermometry (GRT) are used to determine the buffer and gate temperatures respectively. Finite element simulations are used to extrapolate from the measured temperatures to the peak channel temperature and gain insight into the heat flow.

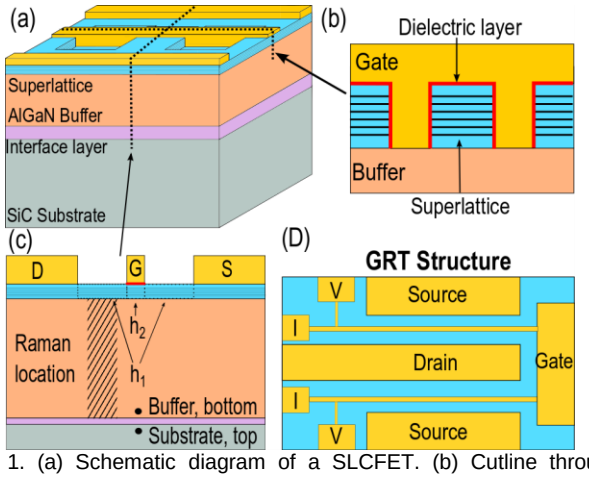

Fig. 1. (a) Schematic diagram of a SLCFET. (b) Cutline through castellation. Gate dielectric is shown in red. (c) Cutline from source to drain with the Raman measurement location and the location of the heat deposition areas h_1 and h_2 considered. (d) GRT structure, with pads labelled I are used to supply current and pads labelled V are used to measure voltage.

II. Experimental Details

The superlattice channel employed in the SLCFETs studied, (Fig. 1 a-c), uses a stack of individually confined 2DEGs to increase the number of conduction paths and reduce ON resistance. The OFF capacitance is dominated by source-drain fringing fields and hence remains relatively unaffected by the multiple channels [3], whilst the three-dimensional gate structure allows the channels to be pinched off from the sides, reducing the threshold voltage [4]. The specific devices studied have 6 channels, with epitaxy based on [6], 2×67.5 µm transistors with L_G = 250 nm and L_{GS} = L_{GD} = 1 µm. The superlattice channel sits atop an AlGaN buffer with a low aluminum concentration. The superlattice is etched away periodically to create the castellated structure, which is topped with the gate dielectric layer, and then the gate metal, with more details on the processing and detailed electrical characteristics given in [3], [4]. Example I(V) characteristics are displayed in the inset of Fig. 2. Thermal measurements were performed at V_G =0 V for V_{DS} = 1, 2 and 3 V. Micro-Raman thermography was performed using a Renishaw InVia Raman system with the 488 nm line of an Ar^+ laser focused using a 50× objective which has an N.A. of 0.60, providing a lateral spatial resolution of ≈ 0.4 µm [7]. As the laser wavelength is below the bandgap of the GaN, the measured

Manuscript received October 9, 2001. We acknowledge financial support from the Engineering and Physical Science Research Council (EPSRC) through the programme grant GaN-DaME (EP/P00945X/1).

C. Middleton (email: cm1720@bristol.ac.uk), S. Dalcanale, J. W. Pomeroy, M. J. Uren, and M. Kuball are with the Centre for Device Thermography and reliability, University of Bristol, UK.

J. Chang, J. Parke, I. Wathuthanthri, K. Nagamatsu, S. Saluru, S. Gupta, and R. Howell are from the Northrop Grumman Mission Systems, Linthecum, MD.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/LED.2019.2929424, IEEE Electron Device Letters

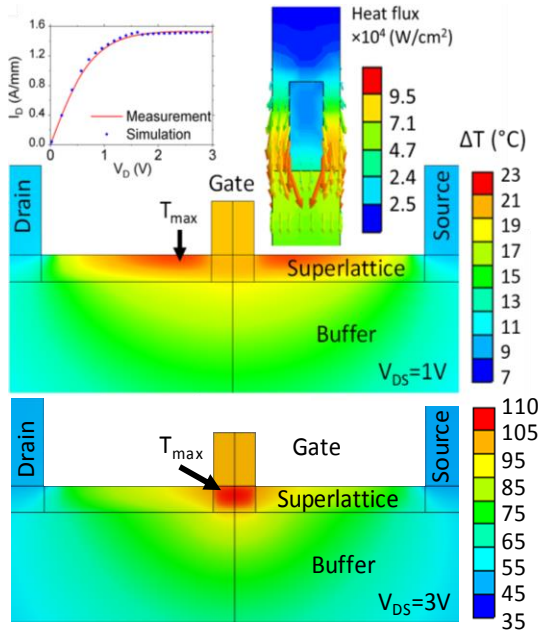

Fig. 2. SLCFET temperature distribution at V_{DS} = 1 V and power density of 1.3 W/mm from the finite element simulation (middle) and V_{DS} = 3 V and power density of 5.7 W/mm (bottom). The ΔT shown is relative to the temperature at the edge of the chip. The view is that of Fig. 1 (c). Inset top left shows a measured and simulated I(V) curve for V_G = 0 V. Inset top right is heat flux in a single castellation for V_D = 1 V, with increased flux at the base of the gate than the base of the channel apparent. The view is that shown in Fig. 1 (b).

spectra are a depth average, providing an average buffer temperature over the volume indicated in Fig. 1 (c). The temperature change is determined from the empirical equation

$$\Delta\omega = \omega_0 - \frac{A}{exp\left(B\hbar\omega/k_bT\right)-1}, \quad (1)$$

where $\Delta\omega$ is the phonon frequency change, ω_0 is the phonon frequency at T = 0 K, A and B are empirical constants, $\hbar$ is the reduced Planck's constant, k_b is the Boltzmann constant and T is the temperature[8]. More details on Raman thermography, including the empirical constants used, can be found in [9].

To determine the heat distribution in the devices 3D T-CAD simulations were performed using Silvaco Atlas. This simulation was used to create the I(V) curve reproducing the experimental data are shown in Fig. 2. This electrical simulation was used to find the electric field in the two areas h_1 and h_2 shown in Fig. 1(c). The ratio of electric field in h_1 and h_2, which varies with drain voltage, was then used to inform the heat dissipation in these areas in a 3D thermal finite element simulation. 3D finite element thermal simulations were undertaken using ANSYS® [10]. Taking advantage of the device symmetry, one quarter of the device is simulated on an aluminum sample holder. To reduce the computational complexity, several castellations were modelled at the center of the device, with the rest of the device modelled by a simple continuous gate structure, where the gate sits vertically above the superlattice only. The number of castellations was increased in the model until the peak temperature at the center of the device converged, i.e., the result was identical to having the castellation structure along the whole gate. This was found to be 20 castellations. Where possible, the relevant material properties are taken from literature [11], [12], however the buffer and interface layer thermal conductivity were adjusted

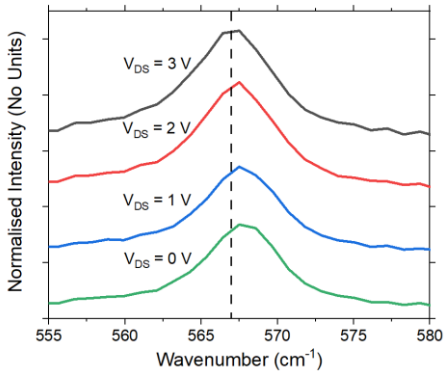

Fig. 3. Measured Raman data for drain voltages (V_{DS}) between 0 V and 3 V the device temperature was determined from the E_2 peak, as the A_1(LO) mode was broadened by phonon-plasmon coupling.

to provide the best fit to the Raman thermography results.

The GRT device structure, a schematic of which is shown in Fig. 1 (d) had 4 additional contacts connected to the end of the gate fingers. These were used to force currents of less than 10 μA through the gate metal and measure its resistance, with voltages typically being in the region of 1.5 mV [13]. This was then used to determine device temperature during its operation; the temperature dependence of the gate resistance was calibrated with the device mounted on a thermal chuck. The simulation is then used to predict the channel temperature (ΔT_C) at the power dissipations used in the experiments.

III. Results and Discussion

Fig. 3 shows the measured Raman E_2 (high) peak, which is used to calculate the temperature. Measured and simulated buffer temperatures in the devices along with the predicted temperatures are displayed in Fig. 4. All temperature increases shown are with respect to the temperature at the edge of the sample, caused by the thermal resistance between sample and its holder (R_{SH}). For Raman measurements the temperature measured experimentally corresponds to the temperature of the buffer layers in the device; the finite element simulation was fitted to this measurement and used to extract the peak channel temperature. The so determined average thermal conductivity for the buffer and interface layer in the thermal model was found to be 46.3 W/m.K. This agrees with thermal conductivity values for AlGaN and thermal boundary resistances for GaN-on-SiC devices reported in [11], [14].

The GRT measurement gives an average temperature along the entire gate finger, not just the active gate width of 135 μm. As shown in Fig. 1 (d) there is an additional 15 μm of gate finger outside the active area. Temperatures measured from gate resistance thermometry (ΔT_{GR}) will therefore be lower than the peak temperature in the gate (ΔT_{GP}). By finding the temperature profile of the gate in the simplified thermal simulation we determine

$$\Delta T_{GP} = 1.11\Delta T_{GR} - 0.11\Delta T_B \quad (2)$$

where T_B is the temperature at the end of the gate finger. As R_{SH} cannot be determined in the GRT experimental set up, this parameter was adjusted in the thermal model to fit the experimental results. The measured ΔT_{GR}, corrected ΔT_{GP} and determined channel temperature ΔT_C from these are shown,

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/LED.2019.2929424, IEEE Electron Device Letters

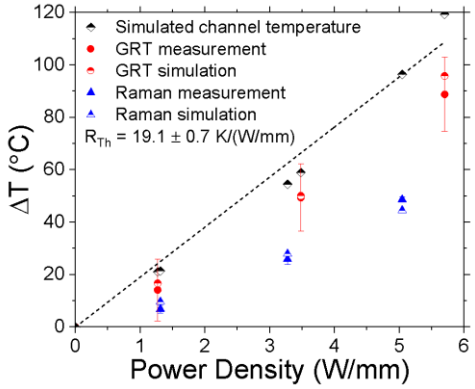

Fig. 4. Raman thermography and GRT temperature rise in with respect to chip edge, as a function of power density. The Raman temperature is the buffer temperature in the device, while the GRT temperature is a temperature average of the gate contact over the whole device, ΔT_{GR}. The dashed line is fit to the simulated peak channel temperature, ΔT_C, to determine the thermal resistance.

along with the Raman thermography results, in Fig. 4. The thermal resistance is found by fitting a linear trend line through the simulated ΔT_C data forced through the origin giving a value of 19.1 K/(W/mm). This is higher than reported results for conventional GaN-on-SiC HEMTs (14 (K/(W/mm)) [7].

This comparison shows there is only a small detrimental thermal impact from the SLCFET design despite the local power density being higher in the castellations for the same overall power density. The maximum power density, defined as the power dissipated over the entire active gate width, measured in this work was 5.7 W/mm in the saturation regime, corresponding to a V_{DS} of 3 V. The heat flux in a single castellation calculated from the thermal simulation is shown in the inset of Fig. 2 for V_{DS} = 1 V. It illustrates that there is significant heat flow through the gate contact to the buffer, with almost twice as much heat flowing through the base of the gate as through the base of the channel. Although the gate insulator adds as a resistance to heat flow from the channel to the gate contact, the gate contact clearly acts as a heat pipe avoiding the low thermal conductivity superlattice, adding efficient lateral heat spreading and mitigating the impact of the increased power density. If the gate is replaced with superlattice material, but the power dissipation area kept the same, the ΔTC increases from 116°C to 143°C. This is a 23% increase in ΔTC, highlighting the importance of the high thermal conductivity gold gate in heat spreading in SLCFETs.

From the electrical T-CAD model, at the highest V_{DS} of 3 V the electric field is 4× higher under the gate whereas for the lowest V_{DS} of 1 V (linear regime) it is only 1.5× higher. The temperature profile between for this V_D = 1 V case is shown in Fig. 3, where the peak temperatures are displaced from the gate and occur in the access region, in spite of the higher electric field under the gate. The additional vertical heat transport through the gate is enough to overcome the increased power density in this area of the channel.

Improvements in thermal resistance are desired for high power device operation and one method for achieving this is optimizing the heat pipe effect of the gate contact. This can be increased by reducing the thickness of the gate dielectric layer.

TABLE I
SIMULATED ΔT (°C) WITH RESPECT TO CHIP EDGE AT DIFFERENT POINTS ALONG THE CENTRAL AXIS IN A SLCFET FOR A POWER DISSIPATION OF 5.7 W/MM, WITH THE LOCATIONS INDICATED IN FIG. 1(C).

Device Layout	Gate (°C)	Buffer, Bottom (°C)	Substrate, Top (°C)
Current	95	41	25
GaN Buffer	72	34	24
Diamond Substrate	77	20	5

Finite element simulations suggest this layer causes the channel temperature ΔT_C to be 21°C hotter than the gate temperature ΔT_{GP} at 5.7 W/mm power dissipation. Reducing its thickness from 15 nm to 5 nm could reduce ΔT_C by 10%; heat flux through the gate foot is 3× larger than the heat flux through the channel foot for the 5 nm gate dielectric and only 2× larger for the 15 nm gate dielectric.

Currently, the devices differ from many traditional GaN based HEMTs in their use of an AlGaN buffer. Including aluminum increases the bandgap and hence the critical field of the buffer, however it also reduces the thermal conductivity. As shown in Table 1, at 5.7 W/mm of power dissipation the finite element simulations suggest a temperature increase due to the buffer of 54°C, 47% of the overall temperature rise. Replacing the AlGaN with GaN and inputting a typical GaN/SiC thermal boundary resistance of 16 m^2K/GW reduced the buffer temperature drop to 28°C, and the ΔT_C by 19% [9], [14]. If it is required to maintain the buffer specifications to preserve the electrical characteristics of the devices, then replacing the SiC substrate with a polycrystalline diamond substrate with assumed thermal conductivity of 1500 W/m.K has been shown to reduce thermal resistances by as much as 36% in GaN HEMTs. The impact is reduced in SLCFETs due to the higher thermal resistance of the buffer, for a thermal boundary resistance of 16 m^2K/GW and a diamond substrate with a constant thermal conductivity of 1500 W/m.K there was still a reduction in ΔT_C of 14% [7].

IV. CONCLUSION

SLCFETs are an exciting development for efficient, reliable RF switches, but their small feature sizes mean heating is confined to nanometer scale castellations. Their thermal resistance has been found using a combination of Raman thermography, gate resistance thermometry, and finite element analysis to be 19.1 ± 0.7 K/(W/mm). Finite element analysis shows that the three-dimensional gate structure aids thermal transport, as the gold gate has a higher thermal conductivity than surrounding material and provides a heat pipe, resulting in 23% lower temperatures. When the device is operated in the saturation regime the heat deposition is focused under the gate and twice as much heat flows through the base of the gate as flows through the base of the channel. However in the linear regime, the peak temperature occurs in the access region as the gate reduces the temperature in the vicinity of the castellation. The overall thermal resistance of the device can be further enhanced by reducing the gate dielectric thickness, removing the aluminum from the buffer or using a diamond substrate.

REFERENCES

[1] G. Meneghesso, G. Verzelli, F. Danesin, F. Rampazzo, F. Zanon, A. Tazzoli, M. Meneghini, and E. Zanoni, "Reliability of GaN High-Electio-Mobility Transistors: State of the Art and Perspectives," *Transactions on Device and Materials Reliabilities*, vol. 8, no. 2, pp. 332-343, 2008.

[2] U. K. Mishra, P. Parikh, and Y. F. Wu, "AlGaN HEMTs – an overview of device operations and applications," *Proceedings of the IEEE*, vol. 90, no. 6, pp. 1022-1031, 2002.

[3] R. S. Howell, E. J. Stewart, R. Freitag, J. Parke, B. Nechay, H. Cramer, M. King, S. Gupta, J. Hartman, M. Snook, I. Wathuthanthri, P. Ralston, K. Renaldo, H. G. Henry, R. C. Clarke, "The Super-Lattice Castellated Field Effect Transistor (SLCFET): A novel high performance Transistor topology ideal for RF switching," in *2014 IEEE International Electron Devices Meeting.* Pp. 11.5.1-11.5.4, 2014.

[4] R. S. Howell, E. J. Stewart, R. Freitag, J. Parke, B. Nechay, M. King, S. Gupta, M. Snook, I. Wathuthanthri, P. Ralston, H. G. Henry, "Advances in the Super-Lattice Castellated Field Effect Transistor (SLCFET) for wideband low loss RF switching applications," in *2016 IEEE MTT-S International Microwave Symposium (IMS)*, pp. 1-3, 2016.

[5] J. Parke, R. Freitag, M. Torpey, R. S. Howell, E. J. Stewart, M. Snook, I. Wathuthanthri, S. Gupta, B. Nechay, M. King, P. Borodulin, K. Renaldo, H. G. Henry, "High-Performance SLCFETs for Switched Filter Applications," in *2016 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, pp. 1-4, 2016.

[6] S. Helkman, S. Keller, Y. Wu, J. S. Speck, S. P. DenBaars, and U. K. Mishra, "Polarization effects in AlGaN/GaN and GaN/AlGaN/GaN heterostructures," *Journal of Applied Physics*, vol. 93, no. 12, pp. 10114–10118, 2003.

[7] J. W. Pomeroy, M. Bernardoni, D. C. Dumka, D. M. Fanning, and M. Kuball, "Low thermal resistance GaN-on-diamond transistors characterized by three-dimensional Raman thermography mapping," *Applied Physics Letters*, vol. 104, no. 8, p. 83513, 2014.

[8] J. B. Cui, K. Amtmann, J. Ristein, and L. Ley, "Noncontact temperature measurements of diamond by Raman scattering spectroscopy," *Journal of Applied Physics*, vol. 83, no. 12, pp. 7929–7933, Jun. 1998.

[9] M. Kuball and J. W. Pomeroy, "A Review of Raman Thermography for Electronic and Opto-Electronic Device Measurement With Submicron Spatial and Nanosecond Temporal Resolution," *IEEE Transactions on Device and Material Reliability*, vol. 16, no. 4, pp. 667–684, 2016.

[10] ANSYS 18.1, "Academic release." 2017.

[11] W. Liu and A. A. Balandin, "Thermal conduction in AlxGa1-xN alloys and thin films," *Journal of Applied Physics*, vol. 97, no. 7, p. 073710–1/6, 2005.

[12] E. A. Burgemeister, W. Von Muench, and E. Pettenpaul, "Thermal conductivity and electrical properties of 6H silicon carbide," *Journal of Applied Physics*, vol. 50, no. 9, pp. 5790–5794, 1979

[13] G. Pavlidis, S. Pavlidis, E. R. Heller, E. A. Moore, R. Vetury, and S. Graham, "Characterization of AlGaN/GaN HEMTs Using Gate Resistance Thermometry," *IEEE Transactions on Electron Devices*, vol. 64, no. 1, pp. 78–83, 2017.

[14] A. Manoi, J. W. Pomeroy, N. Killat, and M. Kuball, "Benchmarking of Thermal Boundary Resistance in AlGaN/GaN HEMTs on SiC Substrates: Implications of the Nucleation Layer Microstructure," *IEEE Electron Device Letters*, vol. 31, no. 12, pp. 1395–1397, Dec. 2010