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Improvement in electrical characteristics of Silicon on Insulator (SOI) transistor using graphene material

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ABSTRACT

This paper presents the electrical characteristics of a short channel Silicon on Insulator (SOI) transistor with a graphene layer. The graphene sheet is used at the bottom of the channel close to the source side and a proportionally heavily p-type retrograde doping implanted in nearly middle of the channel. To increase the gate electrostatic control over the channel we incorporated a high-K material i.e. HfO_2 as the gate oxide insulator. Due to Graphene growth and Retrograde Doping in the Channel, we called this structure "GRDC-SOI" transistor. Because graphene sheet has low band gap and high mobility, we used it to increase the on-state current. Engineered p-type retrograde doping utilized for both decreasing off-state current and increasing on-state current. These dopants cause impurity scattering in the depth of the channel and deflect electron movements and decrease off-current. On the other hand, these dopants which are located almost in the middle of the channel can play the role of base in an NPN Bipolar Junction Transistor (BJT), and turn it on and exceed the on-state current. An immense comparison among our proposed device and a device similar to GRDC-SOI but without Graphene sheet (RDC-SOI) and a conventional structure shows that our proposed device has superior electrical characteristics in terms of I_{ON}/I_{OFF} ratio, transconductance, subthreshold slope, leakage current, breakdown voltage and short channel effects like hot carriers injection and DIBL. Our analyses demonstrate that GRDC-SOI transistor can open a window for utilizing Graphene material in digital circuits and system on chip applications.

Introduction

Since last decades, for expansion of Moore's law and satisfying electronic industry requirements, shrinking of Metal Oxide Field Effect Transistors (MOSFET) have been continued [1]. Silicon on Insulator (SOI) Technology has a huge role to increase the quality of these transistors [2]. However as transistors are scaled, leakage current increases and some unwanted effects which are called Short Channel Effects (SCE), appear [3–8]. Therefore, there is a common opinion in the community that MOSFET scaling is not appropriate anymore and it is necessary to utilize new materials and device concepts to continue scaling and performance improvement [9,10].

2-D Graphene, which is made of a single layer of graphitic carbon is an interesting material for future electronics industry [11]. Although high carrier mobility and 2-D structure of graphene are desirable for device designers, but lack of bandgap in it prevents the device to be completely turned off and this is a challenge in logic devices [10,12]. RF (Radio Frequency) FETs usually are biased in active region in circuits and are standby for amplifying, therefore GFET (FET with gapless large-area graphene channel) has got attention for RF applications. On the other hand, RF circuits are not as much complex as digital integrated circuits and RF chips have more flexibility in utilizing new materials. In the meantime, variety of transistors and materials used in RF circuits including bipolar transistors, n-channel MOSFETs and High Electron Mobility Transistors (HEMTs) [13,14].To open a bandgap in graphene and making it a semiconductor, several techniques are proposed including using bilayer graphene and applying a perpendicular field [15,16], narrowing graphene sheet in one dimension to form graphene nanoribbon [16,17], and applying strain to graphene.

In this work we tried to benefit intrinsic behavior of graphene sheet i.e. high carrier mobility and low band gap, to increase on-state current. In order to control leakage current, we found the optimum place for P-type retrograde doping in the channel to decrease leakage current. This is due to the fact that electron movement is deflected by adding these dopants and the resultant impurity scattering occurs from where the gate control is low in the channel. This engineered P-type doping profile

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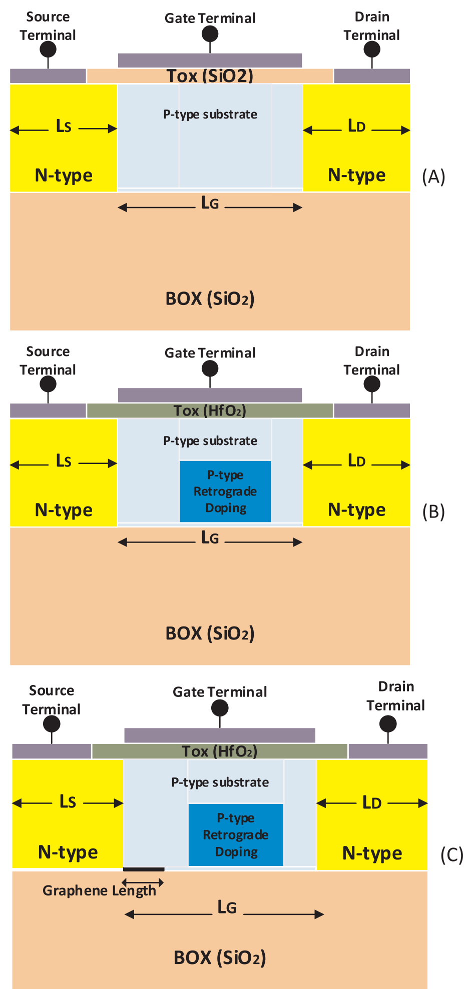

Fig. 1. Device schematic of (A) C-SOI, (B) RDC-SOI, and (C) GRDC-SOI MOSFETs.

also takes part in exceeding on-state current, by forming base junction of NPN bipolar Junction Transistor (BJT), in parallel to intrinsic n-channel SOI MOSFET where source and drain regions are also equal to "Emitter" and "Collector", respectively. Furthermore, for more electrostatic control over the channel and further increasing the on-current in the device, we used HfO_2 material with dielectric constant of $k = 16$ [18–21], as gate insulator in the proposed device instead of SiO_2 with $k = 3.9$ [22] in the C-SOI device. It should be noted that in this work the electrical characteristics of GRDC-SOI MOSFET is compared with RDC-SOI and C-SOI MOSFET counterparts where the active region including source, channel and drain regions are made from silicon material. The rest of this work consists of three sections. Section two presents a cross section view of the structures under study with related parameters. In section three, the simulated and extracted results are reported and discussed. Finally in section four, we explain comprehensive conclusion for this study.

Simulation setup and device design

Fig. 1(A–C) shows the schematic diagram of three considered structures i.e. C-SOI, RDC_SOI and GRDC-SOI MOSFETs. All parameters related to geometry and dopings of these structures are presented in Table 1. Device simulation have been carried out with 2-D Silvaco ATLAS software. We enabled FLDMOB, CONMOB, SRH, Auger, HEI, HHI, BGN, IMAPC SELB models where FLDMOB and CONMOB mobility models take into account field and concentration dependent mobility; SRH and Auger models consider recombination process in the device; HEI and HHI calculate hot electron and hole current density; BGN model applies the band gap dependency to doping density and IMAPC SELB models impact ionization generation phenomenon which mostly happens in the drain side of the channel in our simulations [22]. Although graphene material is not defined in Silvaco Software, in order to have acceptable behavior in simulations, we utilized 3C-SiC material like the work carried out in the literature [23]. The parameters of this material were modified including carrier mobility, bandgap, velocity saturation and carrier effective mass by "user. Material" in ATLAS to achieve a behavior close to graphene. Table 2 shows the basic parameters to define graphene in TCAD and Fig. 2 shows I_{DS}-V_{GS} characteristic of Graphene-FET. This confirms there is a good agreement between experimental [12], other theoretical works [24] and our simulation results.

Results and discussion

This section consists of two subsections. Part A presents comparative study of the devices shown in Fig. 1(A–C) in terms of DC and AC electrical performance. Part B considers impact of graphene nanoribbon (GNR) width on the important device electrical parameters.

DC and AC electrical performance

It is obtained from Fig. 3 that I_{ON}/I_{OFF} current ratio is about 10^6 in RDC-SOI and GRDC-SOI and OFF-current and sub-threshold slope of these devices are much less than the C-SOI which is excellent in such a short channel length. These achievements are indebted to engineered doping in the channel and incorporating HfO_2 material (with permittivity of 16) as the gate insulator for high electrostatic control over the channel. In fact, retrograde doping profile in the channel blocks electron passage due to impurity scattering, and reduces leakage current when transistor is off. On the other hand, it causes creation of easier path for electrons from top of the channel when transistor is in on-state and the channel is created. The reduced amount of off-current in GRDC-SOI with respect to RDC-SOI can be described by tendency of graphene to attract electrons passing from it.

In addition to I_{ON}/I_{OFF} current ratio, GRDC-SOI also shows improvement in transconductance (g_m), due to more drain current. Transconductance that shows how much the gate voltage controls the drain current [28], is depicted in Fig. 4. It is obvious that GRDC-SOI has more g_m value. Therefore, it can exhibit more intrinsic gain with respect to RDC-SOI and C-SOI at $V_{GS} = 0.3$–0.7 V i.e. the usual biasing range for amplification.

Fig. 5 depicts output characteristics of three structures. Based on this figure, GRDC-SOI and RDC-SOI have much more current with respect to C-SOI at higher bias voltages. This current increase in two devices can be described by parallelism of two transistors i.e. one MOSFET in top of the channel and a BJT in the place of retrograde doping. At $V_{GS} = 0.9$ V which voltage is high enough for creation of the channel in the top of silicon layer, by increasing the drain voltage, more carriers tend to pass from the channel and this cause more electron concentration and current density in it and BJT transistor drives to turn on. In such a case, N-type source, P-type retrograde doping and N-type Drain play the role of "Emitter", "Base" and "Collector" regions of assumed NPN transistor parallel to MOSFET transistor. More current of GRDC-SOI with respect to RDC-SOI is due to the presence of the graphene material at the bottom of the channel, which attracts more electrons towards itself and creates an easier path for them to flow.

Drain Induced Barrier Lowering (DIBL) is an important short channel effect which considers drain voltage effect on the lowering of the channel conduction band [29]. This problematic effect should be reduced, because it leads to leakage current and threshold voltage variation. In order to consider DIBL effect in devices, we used the following relation:

Table 1
Geometry and process parameters for RHD, DM-RHD and C-SOI structures.

Parameter	Values C-SOI	RDC-SOI	GRDC-SOI
Top oxide thickness (Tox)	1.0 nm (SiO_2)	1.0 nm (HfO_2)	1.0 nm (HfO_2)
Silicon channel thickness	10.5 nm	10.5 nm	10.5 nm
Buried oxide thickness (BOX)	80 nm	80 nm	80 nm
Channel Length (L_G)	30 nm	30 nm	30 nm
Source/Drain Extension Length (L_S , L_D)	20 nm	20 nm	20 nm
Source/Drain Electrode Length	15 nm	15 nm	15 nm
Gate Workfunction	4.5 eV	4.5 eV	4.5 eV
Channel doping (p-type)	1e12 cm^{-3}	1e12 cm^{-3}	1e12 cm^{-3}
Source/Drain doping (n-type)	9e18 cm^{-3}	9e18 cm^{-3}	9e18 cm^{-3}
P-type Retrograde doping Length	–	14 nm	14 nm
P-type Retrograde doping Height	–	7 nm	7 nm
P-type Retrograde doping in the channel	9e18 cm^{-3}	9e18 cm^{-3}	–
Graphene Length along the channel	–	–	5 nm
Graphene width	1000 nm	1000 nm	1000 nm
Graphene Bandgap	–	–	0.0 eV

Table 2
Applied parameters for simulation of graphene in TCAD simulator.

Electrical properties	Value in simulation
Bandgap (eV)	0 [12,25]
Electron and Hole Mobility ($cm^2\ V^{-1}\ S^{-1}$)	7500 in accordance to [26]
Saturation Velocity (cm/s)	1E8 > 3E7 [27]
Electron and Hole effective mass	0.0251
Electron and Hole Shockley-Read-Hall recombination lifetime (s)	1e-12

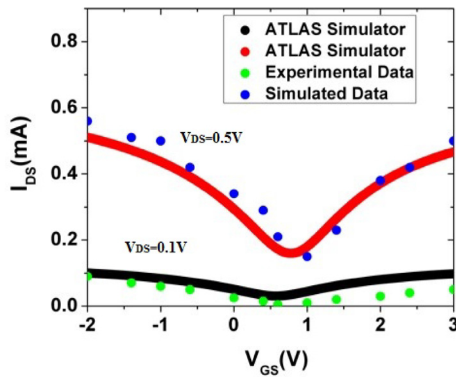

Fig. 2. Simulator results against experimental data at V_{DS} = 0.1 V [12] and theoretical data at V_{DS} = 0.5 V [24] for graphene-FET.

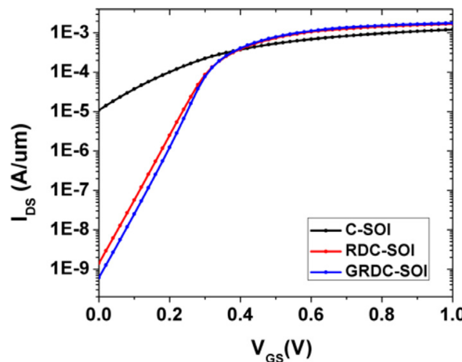

Fig. 3. Transfer characteristics of C-SOI, RDC_SOI and GRDC-SOI MOSFETs at V_{DS} = 0.9 V.

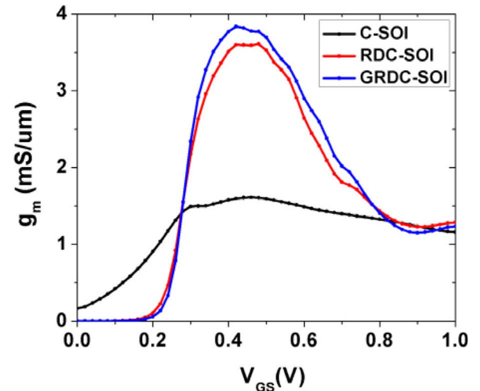

Fig. 4. G_mVariation versus V_{GS} at V_{DS} = 0.9 V.

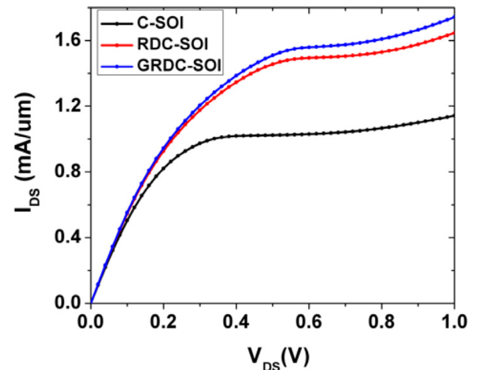

Fig. 5. Output characteristics of C-SOI, RDC_SOI and GRDC-SOI MOSFETs at V_{GS} = 0.9 V.

$$DIBL = \frac{V_{g1} - V_{g2}}{V_{DS2} - V_{DS1}} \tag{1}$$

where V_{g1} and V_{g2} are gate voltages corresponding to drain current of I_{DS} = 1E-4 A at V_{DS1} = 0.2 V and V_{DS2} = 1.2 V, respectively. It should be noted that the mentioned drain current value is quite optional and we chose it according to devices curves. From Table 3, it is clear that RDC-SOI and GRDC-SOI devices are more persistence against this short channel effect. This improvement in these devices is due to the presence of p-type retrograde doped region in their channel which is like an obstacle against drain voltage and immune the source side.

In MOSFETs, when electrons pass from the channel, they collide to

Table 3
DIBL value of three devices.

	V_{gs1} (V)	V_{gs2} (V)	DIBL (mV/V)
C-SOI	0.271	0.143	128
RDC-SOI	0.354	0.269	85
GRDC-SOI	0.343	0.255	87

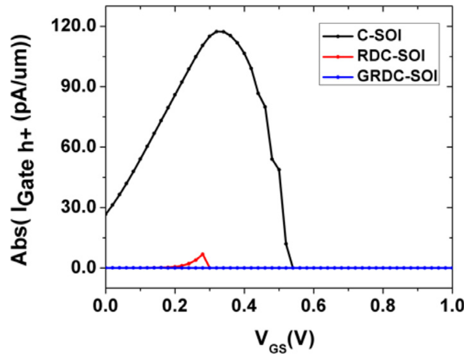

Fig. 6. Absolute value of gate hot hole current for C-SOI, RDC-SOI and GRDC-SOI at V_{DS} = 0.9 V.

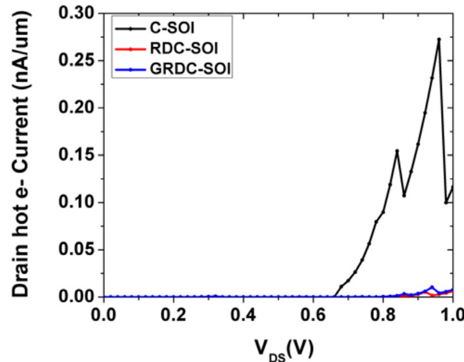

Fig. 7. Drain hot electron current for C-SOI, RDC-SOI and GRDC-SOI at V_{GS} = 0.9 V.

silicon atoms, especially close to the drain region where they have high kinetic energy. These collisions create hot electrons and holes which increase the device temperature. These hot carriers may have enough energy to pass from the gate oxide insulator barrier and then enter into gate electrode which leads to gate leakage current. Figs. 6 and 7 both indicate that gate hot hole and drain hot electron currents in RDC-SOI and GRDC-SOI is much lower in comparison to C-SOI counterpart. These emphasize both devices (particularly GRDC-SOI) reliability against this short channel effect with respect to C-SOI MOSFET. It should be noted that gate hot hole current has been stated in absolute value, because some of hot holes after creation are propelled to gate positive voltage, affected by drain higher potential.

Breakdown voltage is a good measure to consider device persistence against higher unexpected voltages. This parameter has seriously been considered in the literature [30–32]. It is mostly mentioned in high voltage and smart-power applications, where they also offer the advantage of compatibility with VLSI processes. Fig. 8 depicts breakdown voltage of three MOSFETs under study. It confirms GRDC-SOI has more than 10 times higher breakdown voltage and reliability with respect to its counterparts. This higher breakdown voltage in our proposed device origins somehow from lower collisions, less hot carriers and reduced device temperature.

Until now we considered the parameters related to DC performance of a device. In the following we are going to point to some preferences

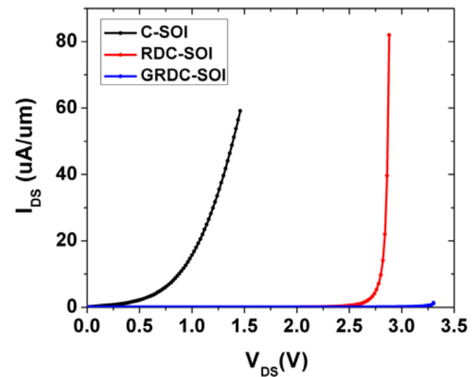

Fig. 8. Breakdown voltages of C-SOI and RDC-SOI and GRDC-SOI at V_{GS} = 0 V.

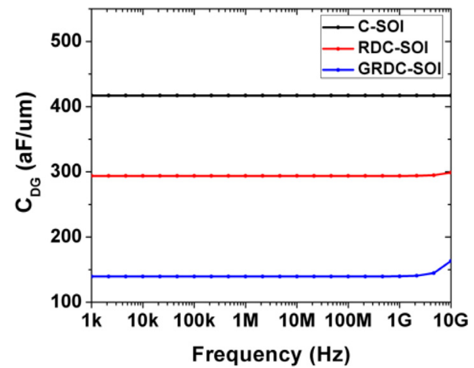

Fig. 9. Drain-Gate capacitance as a function of frequency at bias V_{GS} = V_{DS} = 0.5 V for three structures.

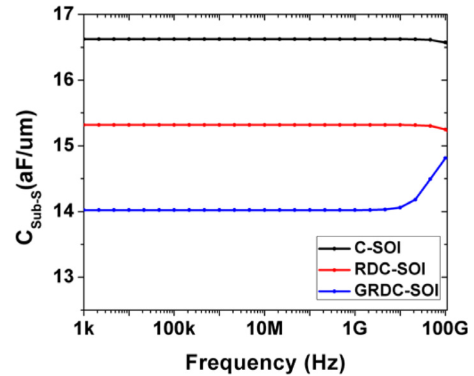

Fig. 10. Substrate-Source capacitance as a function of frequency at bias V_{GS} = V_{DS} = 0.5 V for three structures.

of our device that is a figure of merit in RF performance. To estimate the switching speed of the devices, drain-gate ($C_{Drain\text{-}Gate}$) and substrate-source ($C_{Substrate\text{-}Source}$) capacitances were simulated at bias conditions of V_{GS} = V_{DS} = 0.5 V as shown in Figs. 9 and 10, respectively. In all cases, parasitic capacitances for GRDC-SOI are lower. Actually, the presence of retrograde doping and graphene material at depth of channel have mitigated electrical coupling between drain-gate and substrate-source, which these parasitic capacitances reduced. As a result, delay time and dynamic power dissipation are improved in our proposed device.

Impact of GNR width

Graphene sheet is a gapless material and when it is confined in the width direction, it is called graphene nanoribbon (GNR) which exhibits a non-zero bandgap. In order to test GRDC-SOI MOSFET performance in

Table 4
Graphene nanoribbon parameters, incorporated in simulations.

Graphene nanoribbon (GNR) width (nm)	Eg (eV)	Electron mobility ($cm^2\ V^{-1}\ s^{-1}$) [33]
1	0.3 [34]	20
10	0.15 [34]	800
100	0.003 [17]	8000
1000	0	30,000

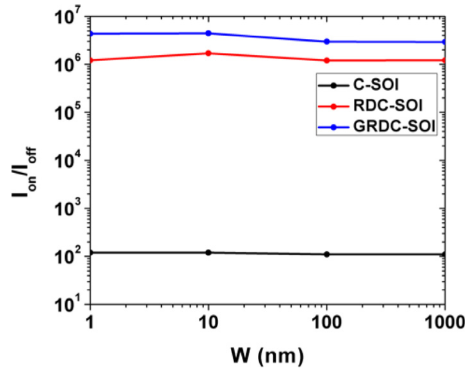

Fig. 11. ON-OFF current ratio versus graphene nanoribbon (GNR) width for three MOSFETs at V_{GS} = 1.0 V and V_{DS} = 0.9 V.

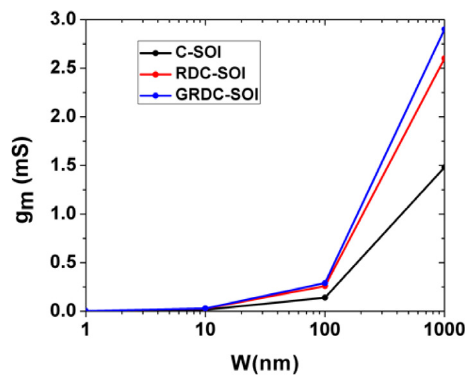

Fig. 12. Transconductance versus graphene nanoribbon (GNR) width for three MOSFETs at V_{GS} = 0.6 V and V_{DS} = 0.9 V.

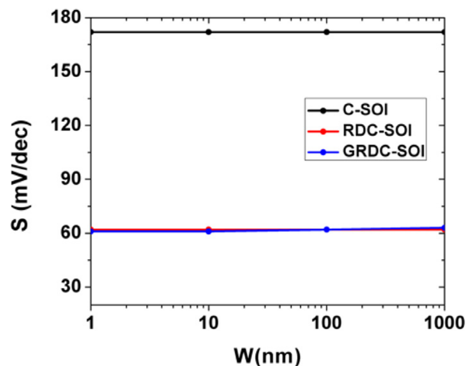

Fig. 13. Subthreshold slope versus graphene nanoribbon (GNR) width for three MOSFETs at V_{DS} = 0.9 V.

different GNR widths, we swept the device width from 1 nm to 1000 nm to consider its impact on the device performance. Due to the fact that GNR width directly affects the electronic properties like bandgap and mobility, it is necessary to incorporate correct values for this case. Table 4 shows incorporated values for GNR simulation in different widths.

According to the Fig. 11, GRDC-SOI has the highest ON-OFF current ratio with respect to other counterparts. It is clear in this figure that as device width increases, this ratio does not change too much. This is because the amount of gate electrostatic control over the channel will not be varied as a result of the graphene nanoribbon width.

Fig. 12 shows as device width increases, transconductance also increases for all devices. But this increment is more intense for GRDC-SOI. This property in GRDC-SOI is indebted to graphene material which leads to more proportional drain current increase in this device with respect to RDC-SOI.

Subthreshold slope (SS) parameter states device speed to turn on from off states and it is stated with the amount of gate voltage increment to increase the drain current one decade in subthreshold regime. It is observed from Fig. 13, that SS in RDC-SOI and GRDC-SOI MOSFETs are close to the ideal value of 60 mV/dec for all of the examined device widths. This improvement in these devices owes to retrograde doping in their channels.

Conclusion

The proposed GRDC-SOI MOSFET demonstrated superior electrical characteristics with respect to RDC-SOI and C-SOI MOSFETs. Furthermore, this engineered device can turn on the NPN bipolar transistor by retrograde doping in the depth of its channel and increase its on-state current using the advantage of graphene material. GRDC-SOI also shows excellent persistence against short channel effects like DIBL and hot carriers injection, which these confirms this device reliability. According to abovementioned benefits, GRDC-SOI can open a window for using graphene material in digital and low power integrated circuits, while scaling transistors for system on chip applications.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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