

Interactive Compact Device Modeling Using Qucs Equation Defined Devices

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Introduction



The latest Qucs[1] release marks a turning point in the development of the Qucs device and circuit modeling facilities. Release 0.0.11 introduced component values defined by equations, and for the first time allowed subcircuits with parameters. Release 0.0.12 extends these features to add device model construction using symbolic equations that are similar to model code written in the Verilog-A language. In designing the latest Qucs modeling features the Qucs team has attempted to address the need to provide the package with an interactive and easy to use modeling system that allows fast compact device and circuit macromodel construction.

The Qucs equation defined device (EDD)

- Qucs EDD [2] is a multi-terminal nonlinear component with branch currents that can be a function of the branch voltages, and stored charge that can be a function of both branch voltages and currents.
- EDD is similar, but more advanced, to the B type controlled source implemented in SPICE 3fs.
- EDD is capable of realizing the same models as the SPICE B device plus an extensive range of more complex compact device models.
- EDD is an advanced component, allowing users to construct their own models from a set of equations derived from physical device properties.
- EDD models can be combined with conventional circuit components and Qucs equation blocks to build compact device subcircuit models.

The Qucs EDD structure

An EDD model is a charge non-linear. Each branch has current I_n and voltage V_n and charge Q_n , where $1 \leq n \leq 8$. The eight branch limit can be increased if required. Branches with $I=0$ and $Q=0$, that are connected to external inputs, act as high impedance voltage probes. Fig. 1 shows an EDD model for a semiconductor diode. The diode I-V characteristics are set by subcircuit parameters identical to the SPICE diode parameters [3]. Conditional branch current and charge equations can be selected by if-then-else statements with a C like ternary operator ($?:$) syntax. Nested if statements are allowed. EDD equations may include branch variables, variables from equation blocks, subcircuit parameters, the operators defined in Verilog-A, and functions selected from an extended set of mathematical functions defined by Qucs, including $limexp$. Variables and equations may be entered in any order in the Qucs Equation block. In Fig. 1, EDD diode current I_d is the sum of branch currents I_1 to I_4 , where I_1 represents the forward bias region, I_2 the reverse bias region and I_3 plus I_4 the reverse breakdown region.

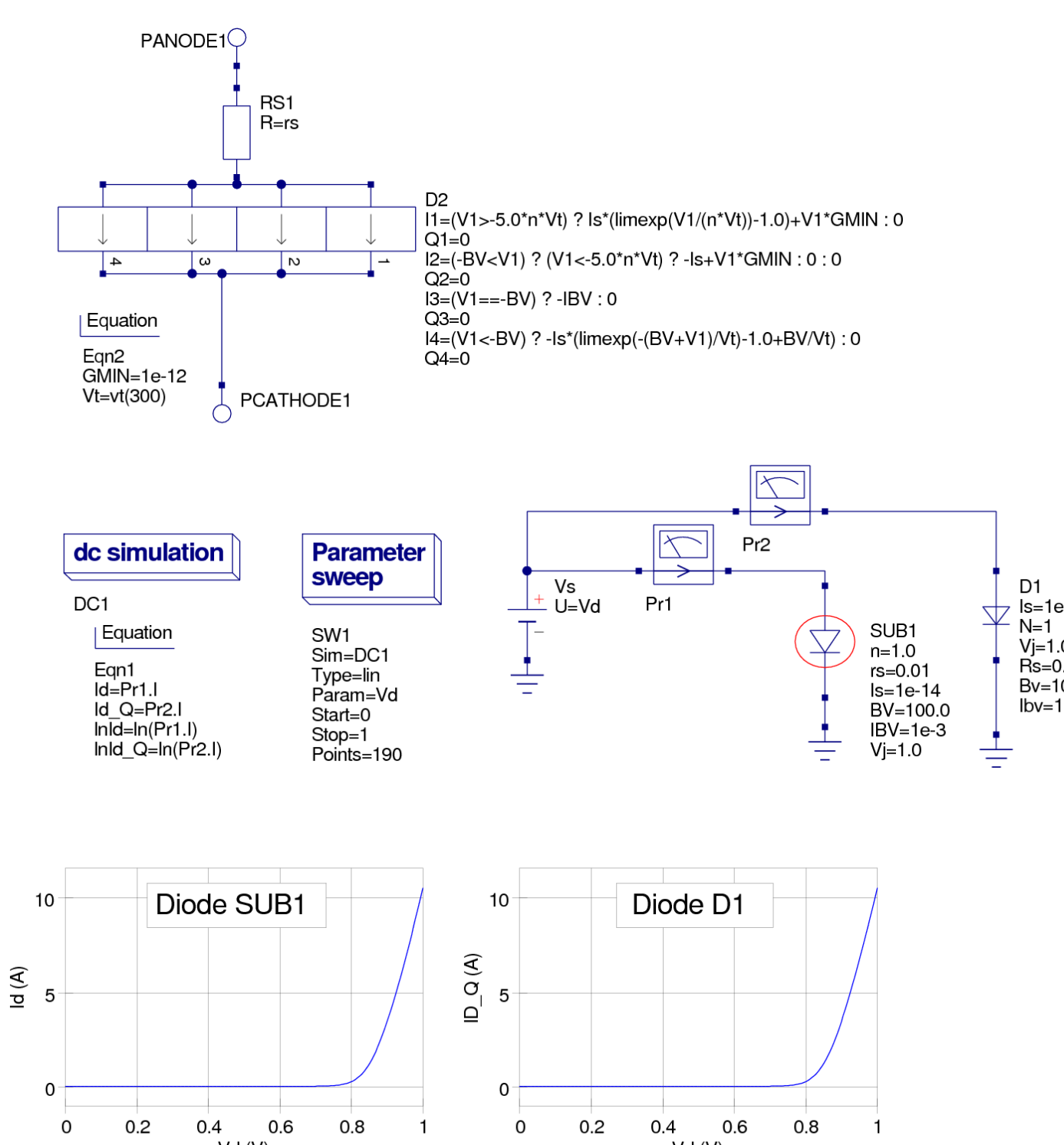


Fig. 1: DC diode model test circuit and simulation results; SUB1 is the EDD component and D1 the model built-in diode model with the same parameters as SUB1.

Diode capacitance effects

The next stage in the development of the EDD diode model illustrated in Fig. 1 is to add capacitance effects: depletion layer and diffusion capacitance for the reverse and forward bias regions of operation respectively. Fig. 2 illustrates the diode EDD model with these added via contributions to the device charge. Again the same syntax to the SPICE diode model has been employed in the derivation of the EDD charge equations. An area factor has also been added to the EDD model presented in Fig. 2.

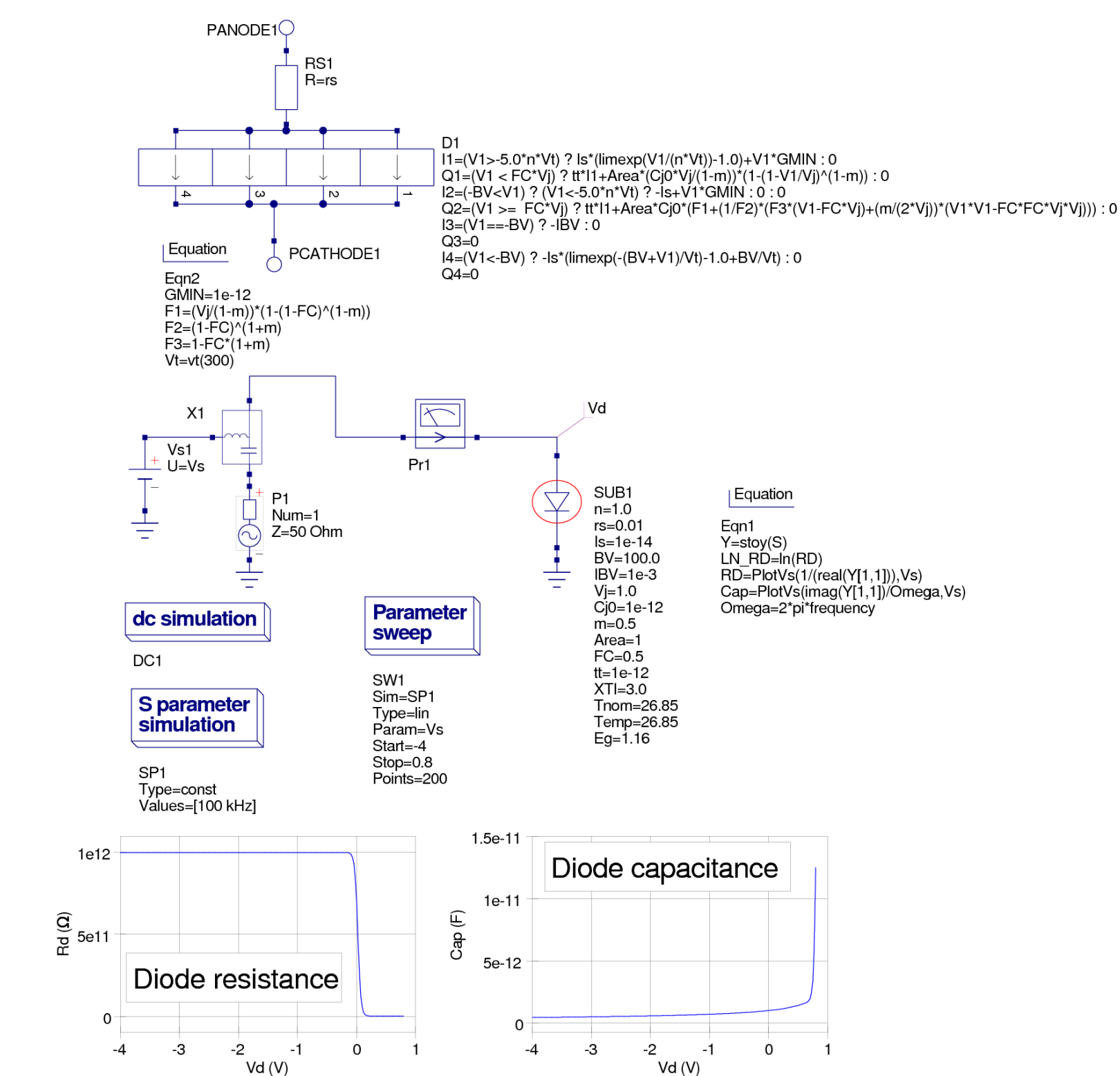


Fig. 2: EDD diode model capacitance and resistance simulation

Summary: The Qucs EDD model is an innovative nonlinear component. It allows easy construction of compact device models and circuit macromodels via the Qucs GUI, allowing fast prototyping prior to translation into Verilog-A and model implementation using ADMS. This is a major step forward for Qucs. It should be of interest to anyone designing and testing compact device and integrated circuit simulation models.

Modeling temperature effects

The EDD diode model illustrated in Fig. 3 employs SPICE temperature parameters Tnom and Temp to determine the temperature dependencies of the model parameters. In Fig. 3 EDD diode parameters I_s , V_j and C_j0 are defined as functions of temperature. Comparison between the Qucs built-in diode model and the EDD compact model given in Fig. 3 shows good agreement in the I-V d.c. characteristics over a wide temperature range. Device self-heating effects can be modeled by employing one of the EDD branches to monitor an external signal which is proportional to device power dissipation.

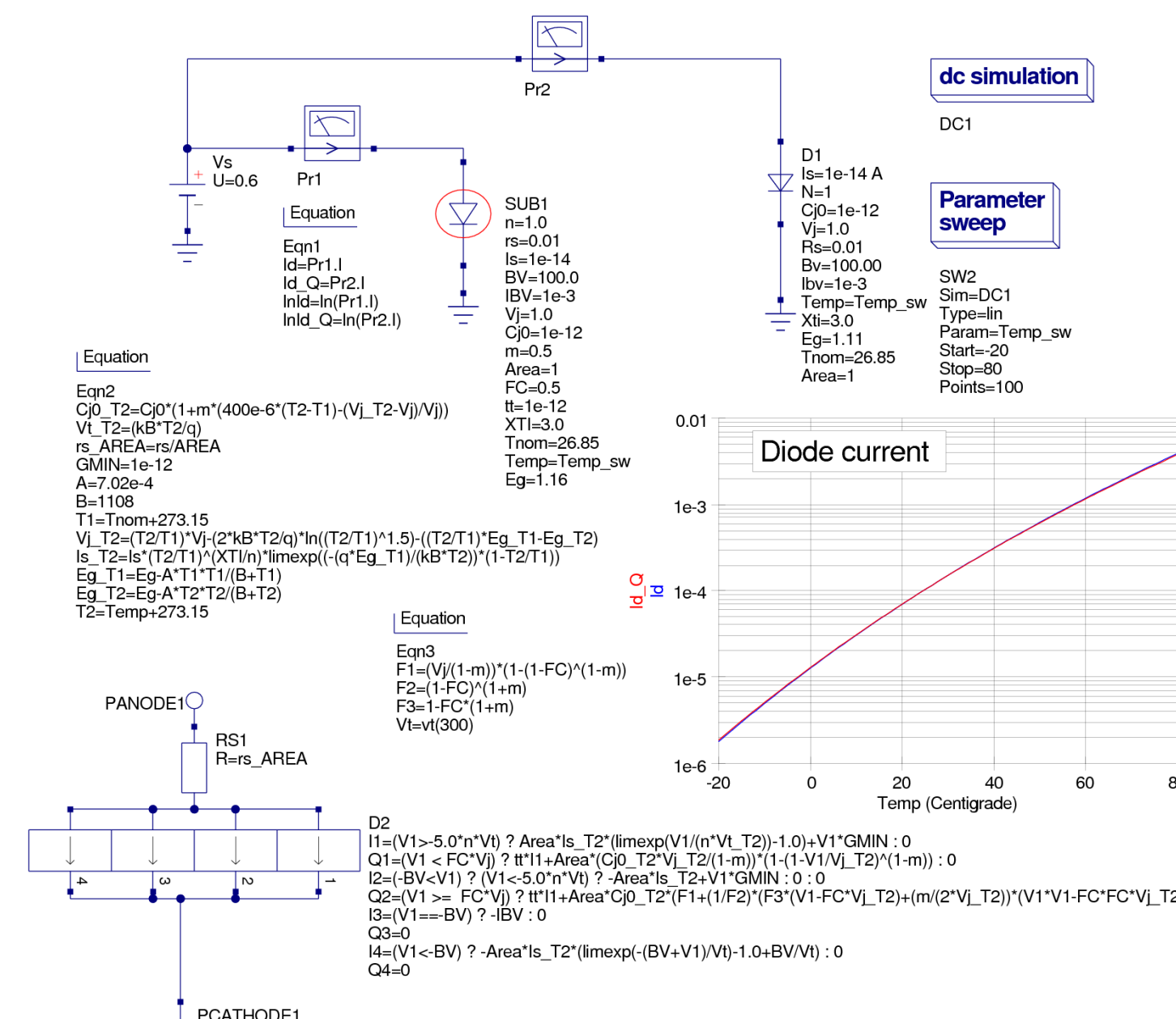


Fig. 3: The EDD diode model and temperature scan test circuit

Compact device subcircuits with package parasitic components

Fig. 4 shows a model for a p⁺n⁺ tunnel diode [4] with series resistance R_s and inductance L_s connection components plus diode capacitance modeled by parallel fixed value capacitor C_p. By adding conventional components to EDD models, compact device subcircuits can be easily constructed for testing and performance evaluation. Fig. 5 illustrates a basic monostable pulse generator derived from the EDD tunnel diode subcircuit model.

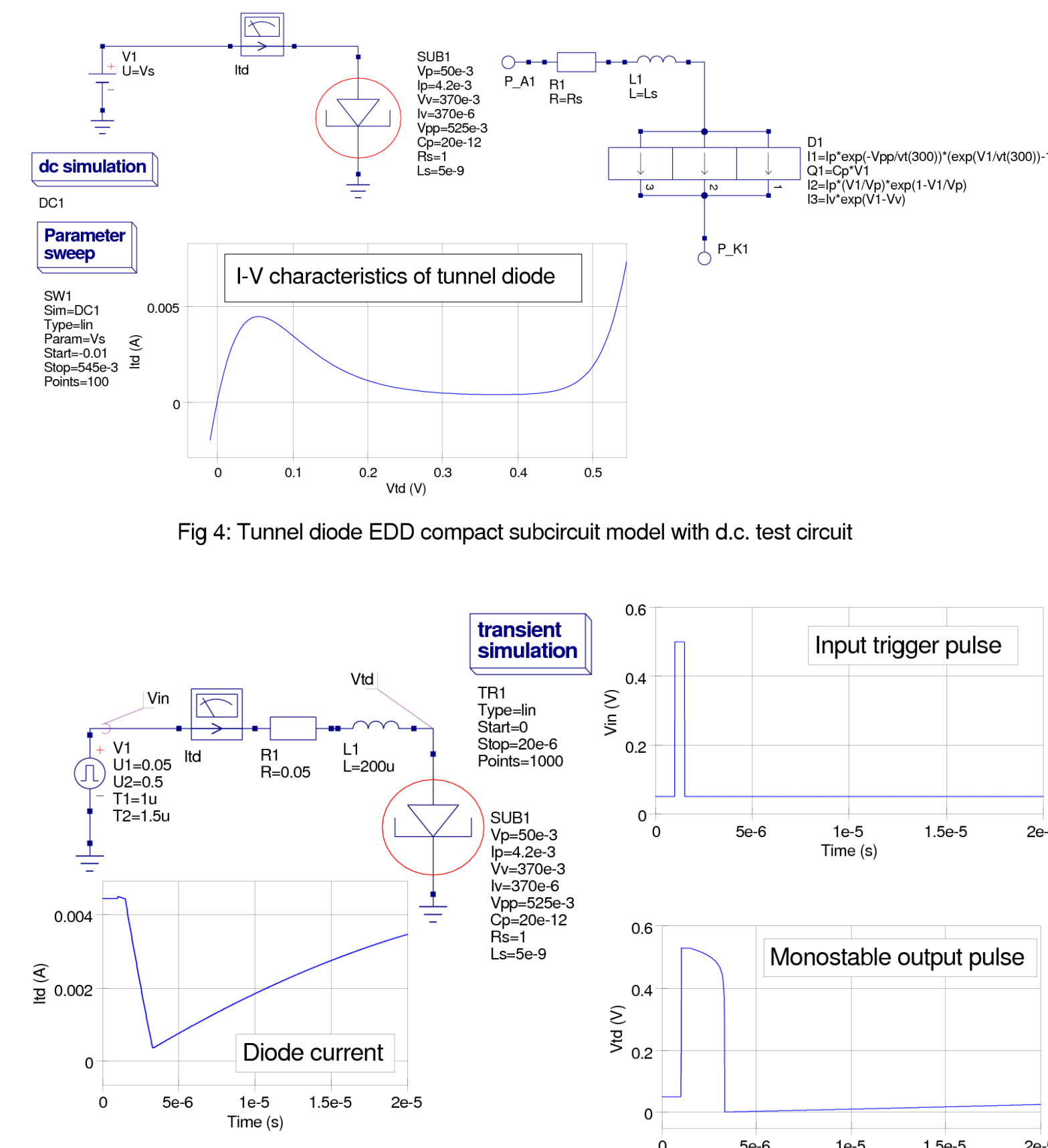


Fig. 4: Tunnel diode EDD compact subcircuit model with d.c. test circuit

Fig. 5: Tunnel diode monostable pulse generator test circuit and waveforms

Non-linear passive components

Non-linear passive components are sometimes present in compact device and circuit macromodels. The model and test circuit given in Fig. 7 indicates how the Qucs EDD device handles such situations. This example demonstrates the use of a gyrator with an EDD model to form a nonlinear inductance of the form implemented in SPICE 2g6.

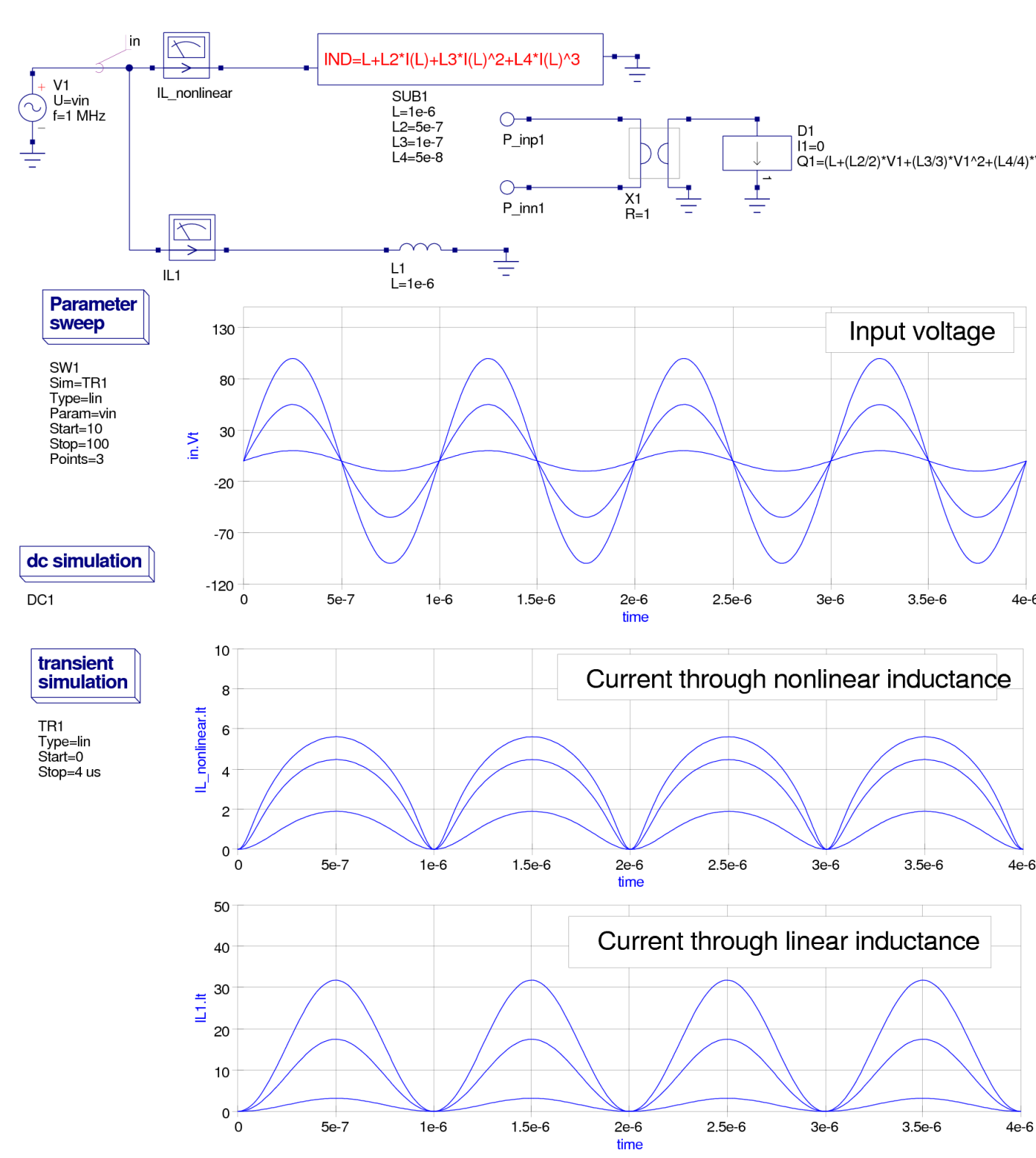


Fig. 6: SPICE 2g6 style non-linear inductance model, test circuit and waveforms: the inductance is specified by coefficients L1, L2, L3 and L4

The Curtice Level 1 MESFET model

The compact device model presented in Fig. 7 is a level 1 Curtice [5] model of a MESFET. This example illustrates how Qucs EDD models, passive components, equation blocks and subcircuit parameters can be combined to form multi-terminal compact device subcircuits. Figures 8 to 11 show MESFET test circuits and simulation results.

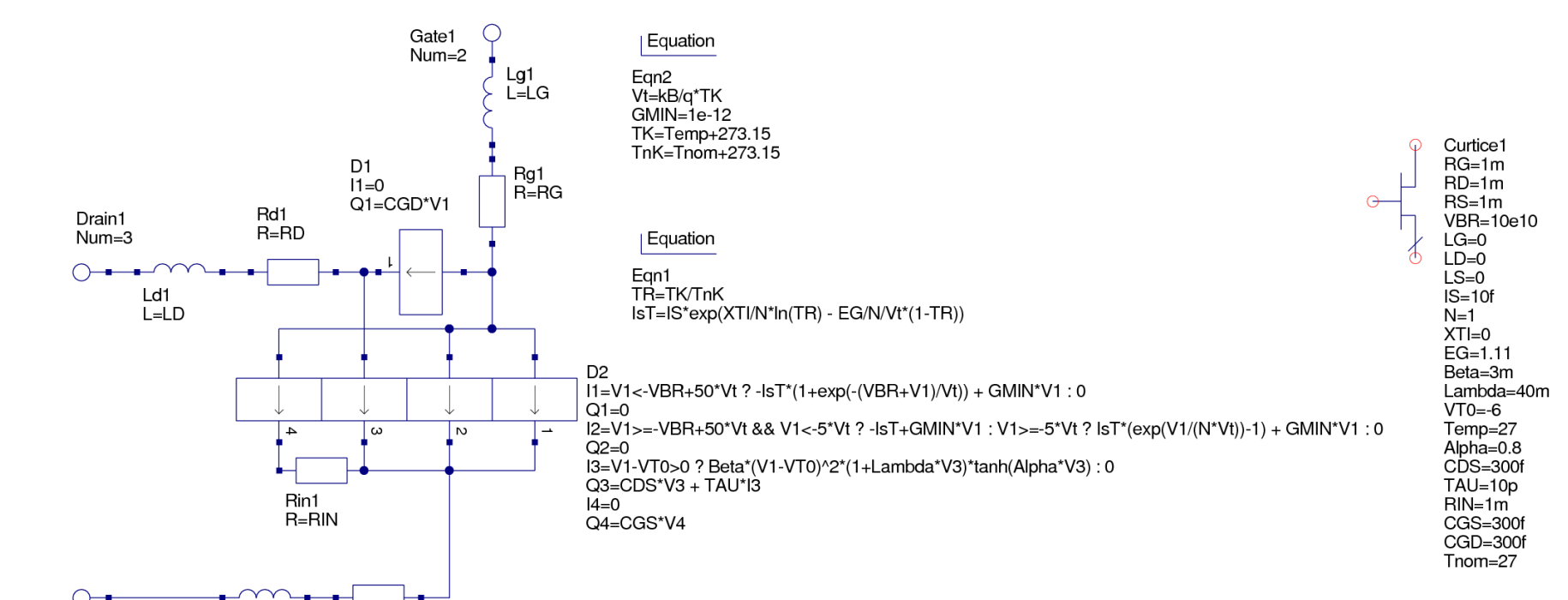


Fig. 7: The Curtice level 1 MESFET model

| Name | Symbol | Description | Unit | Default |
|--------|-----------|---|-------------|------------------|
| RG | R_G | External gate resistance | Ω | 1m |
| RD | R_D | External drain resistance | Ω | 1m |
| RS | R_S | External source resistance | Ω | 1m |
| VBR | V_{BR} | GS breakdown voltage | V | 10 ¹⁰ |
| LG | L_G | External gate lead inductance | H | 0 |
| LD | L_D | External drain lead inductance | H | 0 |
| LS | L_S | External source lead inductance | H | 0 |
| IS | I_S | Diode saturation current | A | 1 |
| N | N | Diode emission coefficient | 1 | 10 |
| XTI | X_{TI} | Diode saturation temperature coefficient | eV | 0 |
| EG | E_G | Diode energy gap | eV | 1.11 |
| TAU | τ | Internal time delay from drain to source | s | 10p |
| RIN | R_{IN} | Series resistance to CGS | Ω | 1m |
| CGS | C_{GS} | Interelectrode G-S bias-independent capacitance | F | 300f |
| CGD | C_{GD} | Interelectrode G-D bias-independent capacitance | F | 300f |
| CDS | C_{DS} | Interelectrode D-S bias-independent capacitance | F | 300f |
| Tnom | T_{NOM} | Device parameter measurement temperature | $^{\circ}C$ | 27 |
| Temp | T | Device temperature | $^{\circ}C$ | 27 |
| Alpha | α | Coefficient of V_{GS} in \ln function for quadratic model | 1/V | 0.8 |
| Beta | β | Transconductance parameter | A/V^2 | 3m |
| Lambda | λ | Channel length modulation parameter for quadratic model | 1/V | 40m |
| VTO | V_{TO} | Quadratic model gate threshold voltage | V | -6 |

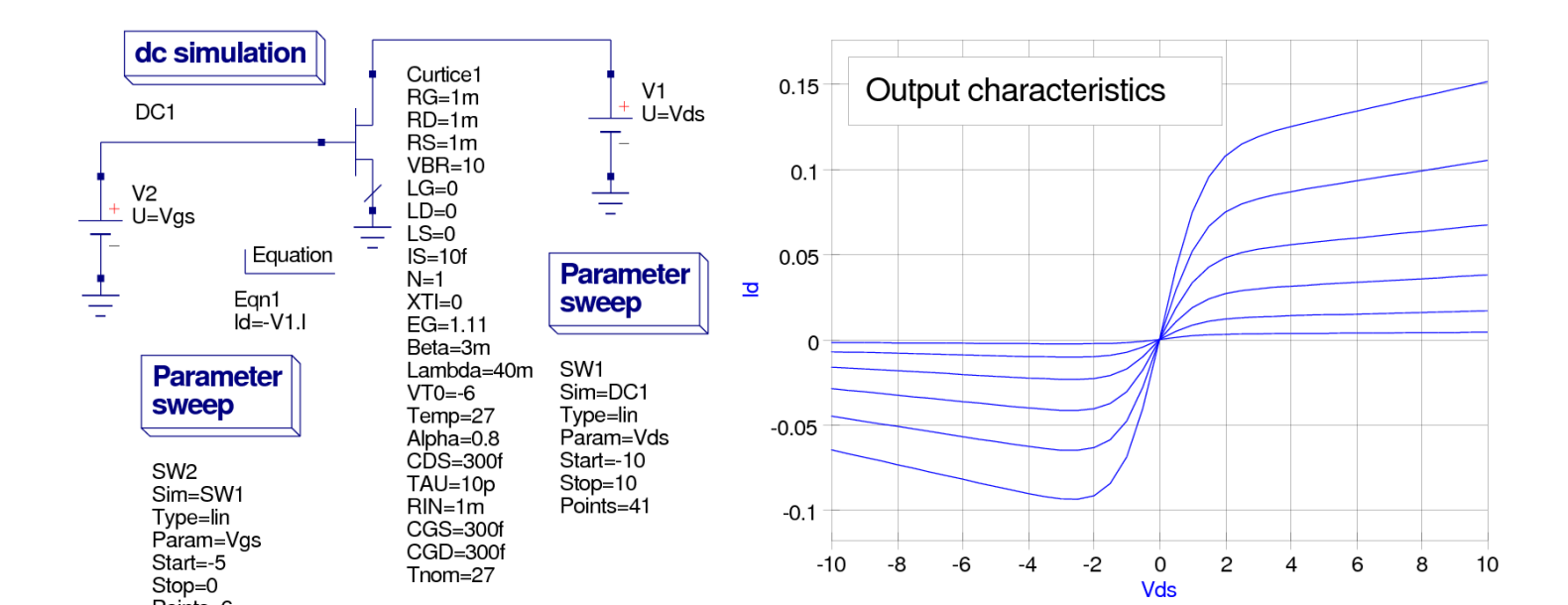


Fig. 8: MESFET I_d versus V_d test circuit and characteristics: V_{gs} is also scanned

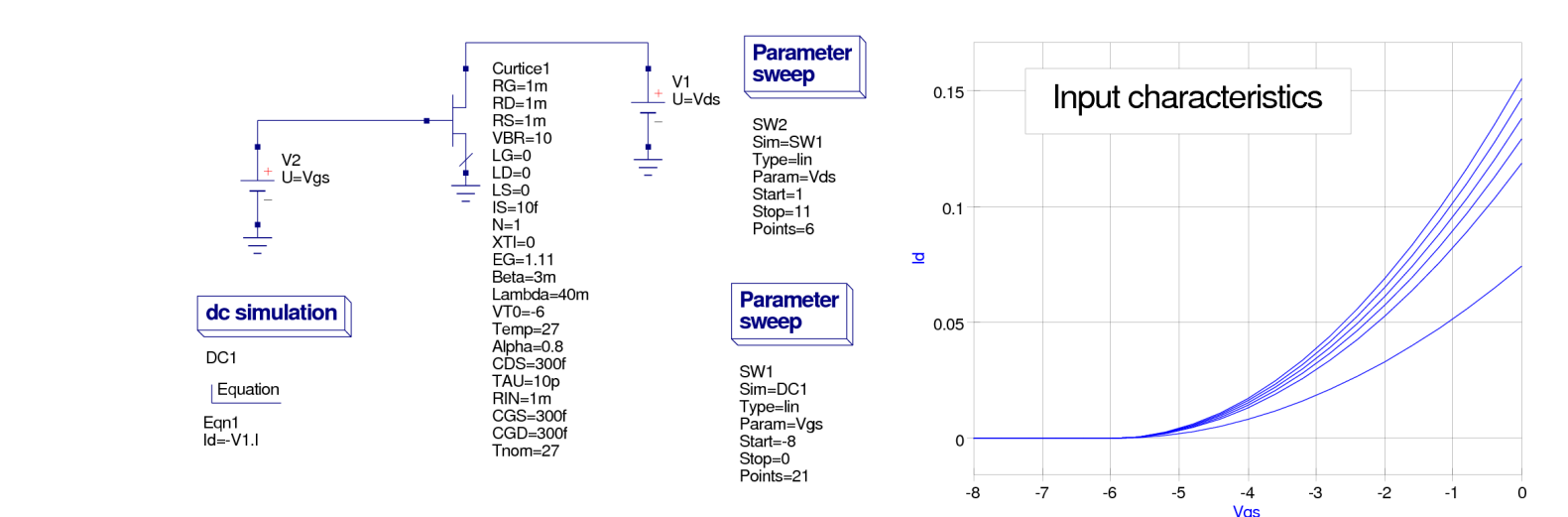


Fig. 9: MESFET I_d versus V_d test circuit and characteristics: V_d is also scanned

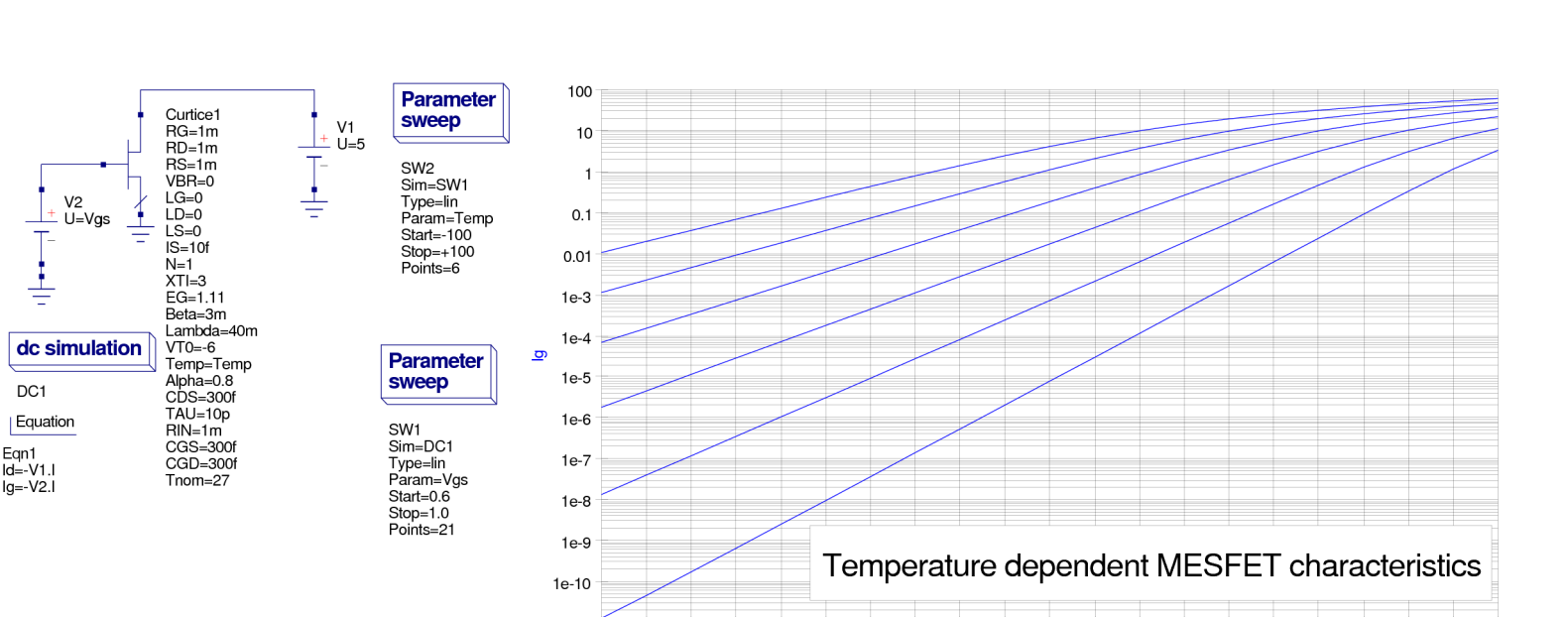


Fig. 10: MESFET I_g versus V_g test circuit and characteristics: Temp is also scanned

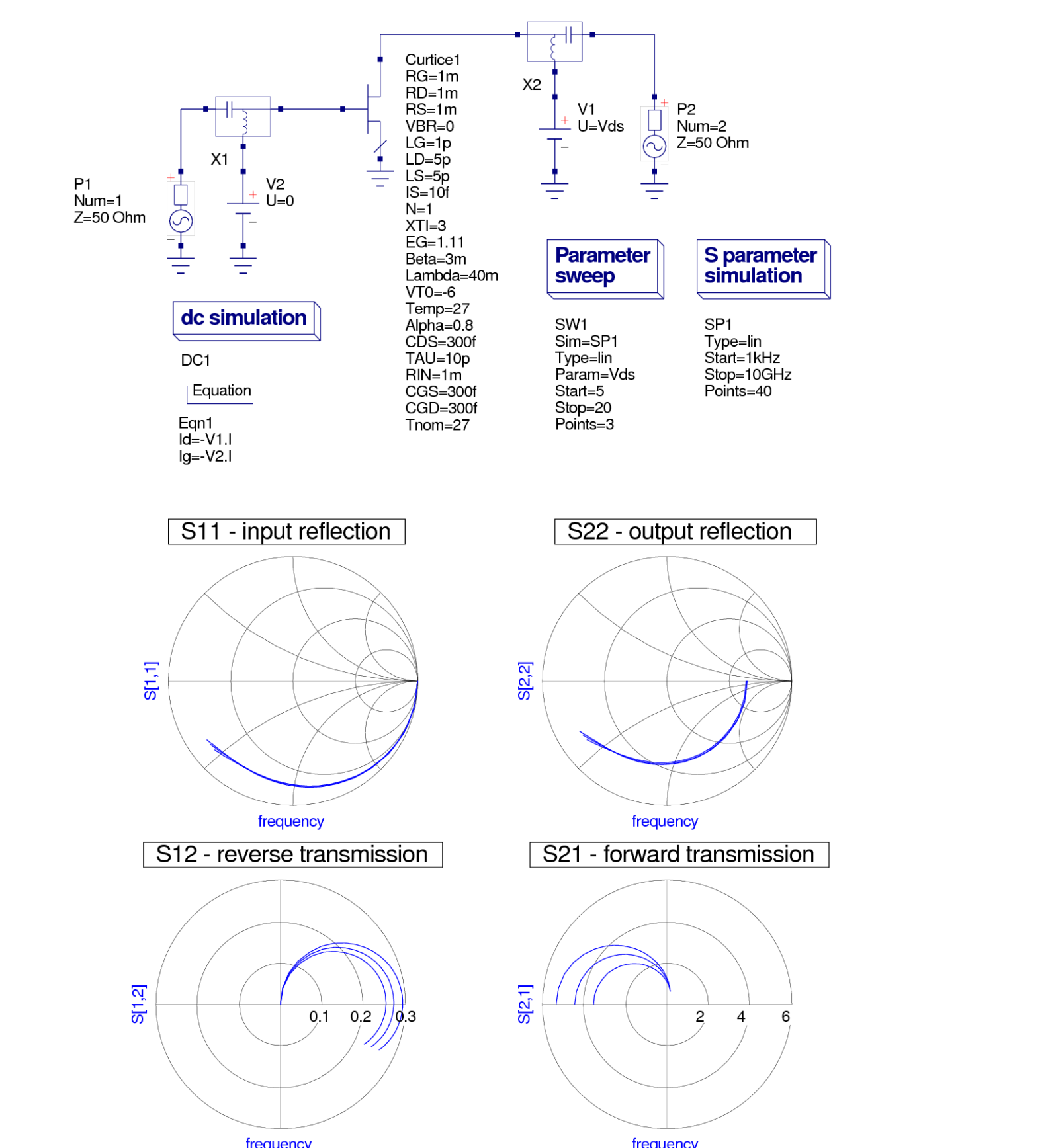


Fig. 11: MESFET S-parameter test circuit and characteristics

References: [1] Qucs: Quite Universal Circuit Simulator, <http://qucs.sourceforge.net>.

[3] Paolo Antognetti and Giuseppe Massobrio (Editors), 1998, "Semiconductor Device Modeling with SPICE", McGraw-Hill Inc, pp 1-32.

[5] W.R. Curtice, 1980, "A MESFET model for use in the design of GaAs integrated circuits", IEEE Transactions on Microwave Theory and Techniques, MTT-28, pp. 448-456.

[2] Mike Brinson, "Component and compact device and circuit modelling using symbolic equations", Qucs Tutorial, <http://qucs.sourceforge.net>.

[4] S. M. Sze, "Physics of Semiconductor devices", (2nd Edition), 1981, John Wiley & Sons Inc, pp 516-536.