

A Hybrid Verilog-A and Equation-Defined Subcircuit approach To MOS Switched Current Analog Cell Modeling and Simulation in the Transient and Large Signal AC Domains

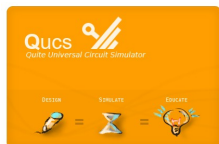
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- Background
- First and second generation current memory cells
- Computationally efficient Verilog-A code for voltage controlled switches and switched current MOS transistor models
- A macromodel for an ideal switched current memory cell
- A hybrid macromodel for a switched current first generation memory cell
- A hybrid macromodel for a switched current second generation memory cell
- A large signal AC low-pass switched current filter example
- Relative transient timings for $Z^{-1/2}$ hybrid macromodels
- Summary

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Background

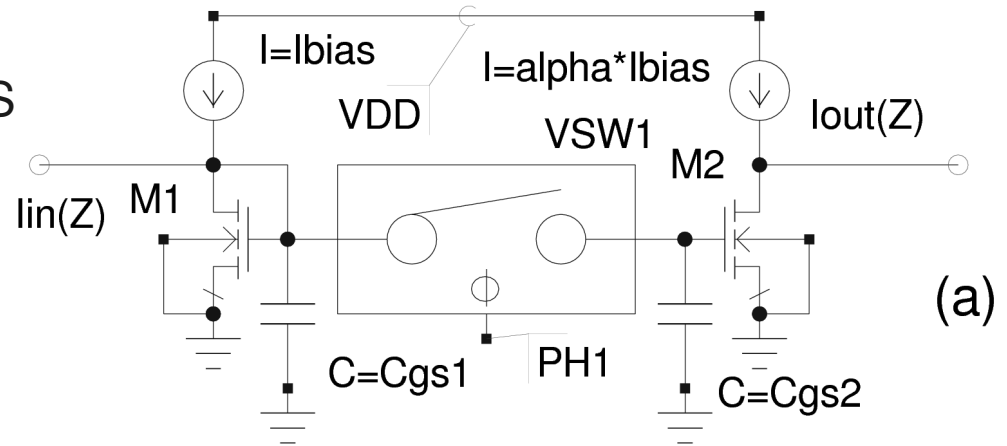
- Conventional modeling and simulation of two phase switched current MOS integrated circuits is normally undertaken at semiconductor device level, making transient analysis of complex systems particularly lengthy.
- Measurable reductions in transient simulation run times can be achieved by modeling part, or all, of a switched current design as a macromodel.
- Circuit simulators rarely include special purpose simulation engines designed to handle emerging technologies, like switched current MOS technology, at a functional level.
- This paper presents a hybrid Verilog-A/equation-defined device modeling technique based on embedded Verilog-A code for non-linear devices plus parametrized subcircuits which have been optimized for run-time simulation speed.
- The proposed hybrid modeling procedure has been tested using the “Quite universal circuit simulator” (Qucs) and applied to the design of functional switched current memory cell macromodels.



First and second generation current memory cells

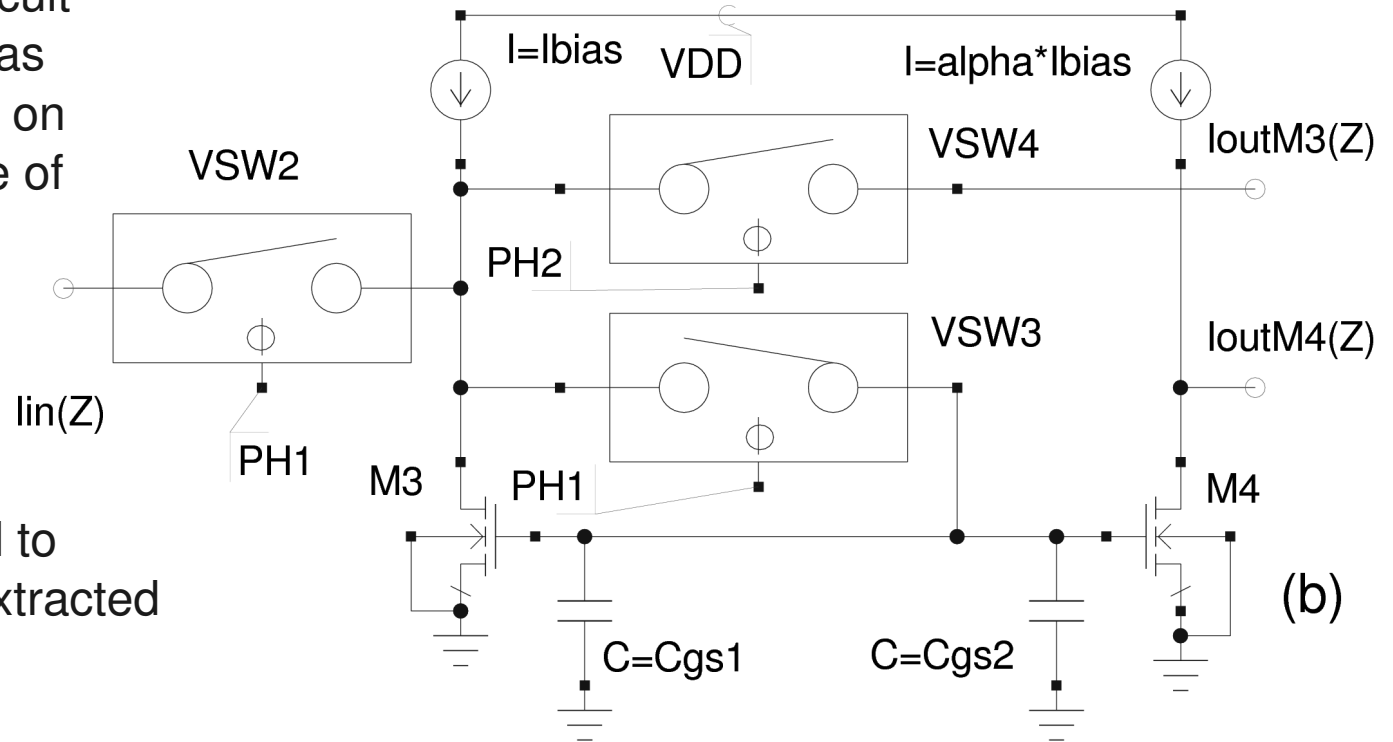
- The fundamental circuit underpinning MOS switched current technology is the current memory cell:

- (a) first generation current mirror circuit
- (b) second generation circuit with direct and mirrored output.



$$I_{out}(Z)/I_{in}(Z) = (W/L)_{M2}/(W/L)_{M1} \cdot Z^{-1/2} = \alpha \cdot Z^{-1/2}$$

- As the name implies this circuit represents an input current as an equivalent charge stored on the gate-source capacitance of an MOS transistor.



$$I_{outM3}(Z)/I_{in}(Z) = Z^{-1/2}$$

$$I_{outM4}(Z)/I_{in}(Z) = (W/L)_{M4}/(W/L)_{M3} \cdot Z^{-1/2} = \alpha \cdot Z^{-1/2}$$



Computationally efficient Verilog-A code for voltage controlled switches

```

`include "disciplines.vams"
`include "constants.vams"
//
module vswitch(swIN, swOUT, PH);
inout swIN, swOUT, PH;
electrical swIN, swOUT, PH;
`define attr(txt) (*txt*)
parameter real LEVEL = 1.0 from [1.0 : inf]
`attr(info = "Switch high level control voltage" unit="V");
parameter real Rclosed = 10.0 from [1e-9 : inf]
`attr(info = "Switch closed series resistance" unit = "Ohm");
parameter real Ropen = 1e9 from [1e-9 : inf]
`attr(info = "Switch open series resistance" unit = "Ohm");
parameter real gain = 100.0 from [1e-9 : inf]
`attr(info = "Switch gain factor");
parameter real ShapeF = 0.5 from [1e-9 : inf]
`attr(info = "Switching point scaling factor");
real Vmid;
analog begin
@(initial_model)
begin
Vmid=ShapeF*LEVEL;
end
I(swIN, swOUT) <+ V(swIN, swOUT)/(Rclosed +
Ropen/(1+limexp(gain*(V(PH)-Vmid))));
end
endmodule

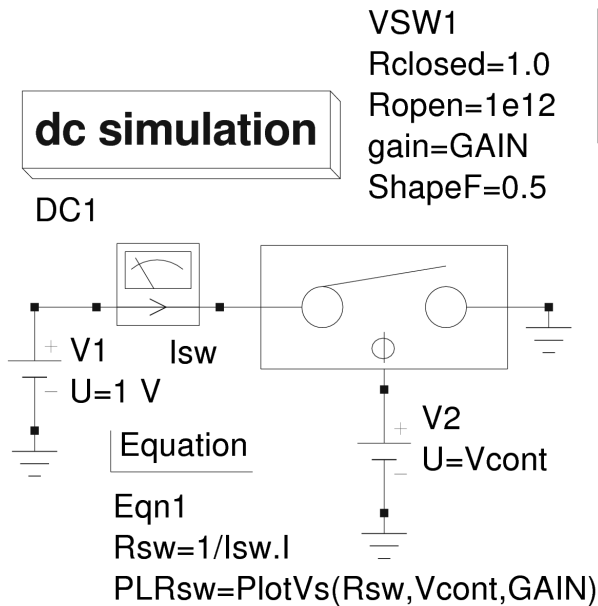
```

$$R_{sw} = R_{closed} + R_{open} * F1, \text{ or } R_{sw} = R_{closed} + R_{open} / F2$$

$$\text{Where } F1 = \frac{1 - \tanh(\text{gain} * [VPH - \text{ShapeF} * LEVEL])}{2}$$

$$F2 = 1 + \text{limexp}(\text{gain} * [VPH - \text{ShapeF} * LEVEL])$$

switches

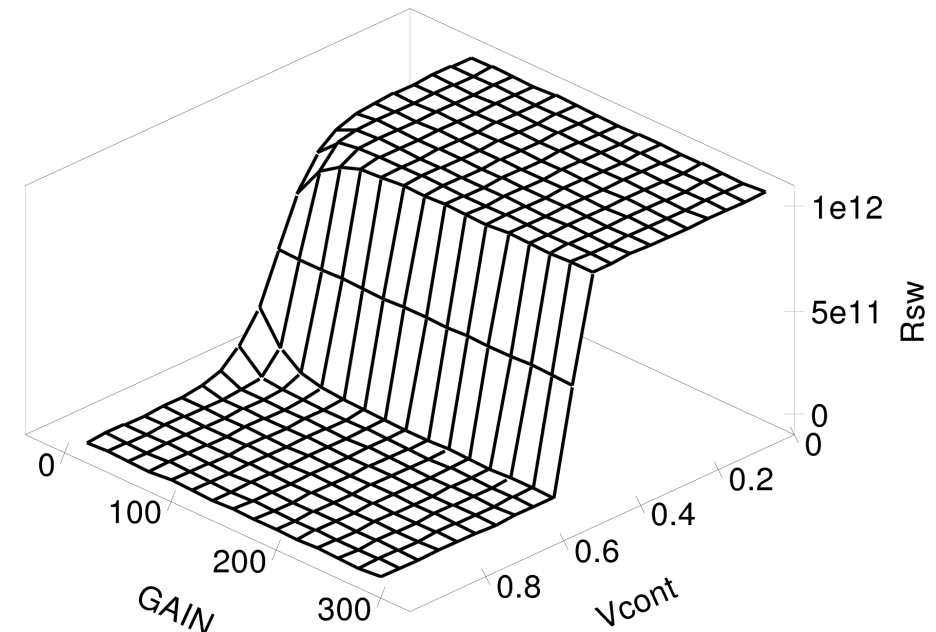


Parameter sweep

SW1
Sim=SW2
Type=lin
Param=GAIN
Start=20
Stop=300
Points=15

Parameter sweep

SW2
Sim=DC1
Type=lin
Param=Vcont
Start=0
Stop=1
Points=21



Computationally efficient Verilog-A DC code for the EPFL-EKV 2.6 long channel nMOS transistor model

- To minimize the number of numerical computations undertaken each time the code is called during simulation all numerical constants and algebraic constant expressions are grouped within a Verilog-A `@(initial_model)` block.

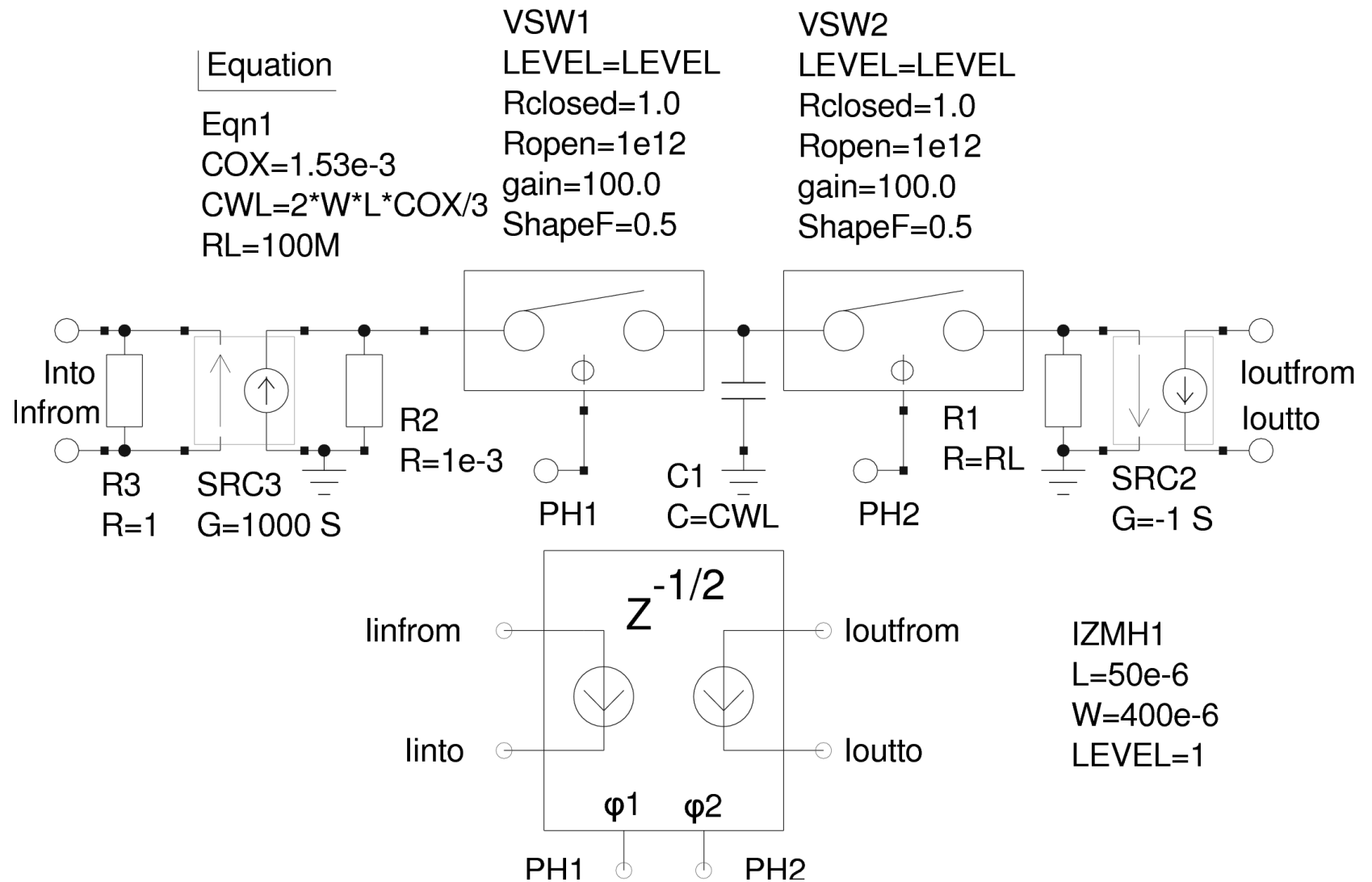
- The `@(initial_model)` block is called only once at the start of a simulation sequence (usually during the initial DC analysis).

```
`include "disciplines.vams"
`include "constants.vams"
module EKV26nMOSLDCD (Drain, Gate, Source, Bulk);
inout Drain, Gate, Source, Bulk;
electrical Drain, Gate, Source, Bulk;
`define attr(txt) (*txt*)
parameter real L = 10e-6 from [0.0 : inf]      `attr(info="length parameter" unit = "m" );
parameter real W = 10e-6 from [0.0 : inf]      `attr(info="Width parameter" unit = "m");
parameter real VTO = 0.5 from [1e-6 : 2.0]     `attr(info="long channel threshold voltage" unit="V" );
parameter real GAMMA = 0.7 from [0.0 : 2.0]    `attr(info="body effect parameter" unit="V**(1/2)");
parameter real PHI = 0.5 from [0.3 : 2.0]      `attr(info="bulk Fermi potential" unit="V");
parameter real KP = 50e-6 from [10e-6 : inf]   `attr(info="transconductance parameter" unit = "A/V**2");
parameter real THETA = 50e-3 from [0 : inf]    `attr(info="mobility reduction coefficient" unit = "1/V");
real P1, P2, P3, P4, P5, P6, P7, P8, P9;
real VGprime, VP, n, Beta, If1, Ir1, If, Ir;
analog begin
@(initial_model)
begin
    P1 = -VTO+PHI+GAMMA*sqrt(PHI); P2 = GAMMA/2; P3 = P2*P2;
    P4 = GAMMA*P2-PHI; P5 = PHI+4*$vt+1e-6; P6 = KP*W/L;
    P7 = 1/(2*$vt); P8 = 2*$vt*$vt; P9 = -PHI;

end
VGprime = V(Gate,Bulk)+P1;
if (VGprime > 0.0)
    VP = P4+VGprime-GAMMA*sqrt(VGprime+P3);
else
    VP = P9; n = 1+P2/sqrt(VP+P5); Beta = P6/(1+THETA*VP);
If1 = ln(1+limexp((VP-V(Source,Bulk))*P7)); If = If1*If1;
Ir1 = ln(1+limexp((VP-V(Drain,Bulk))*P7));
Ir = Ir1*Ir1;
I(Drain,Source) <+ P8*n*Beta*(If-Ir);
end
endmodule
```

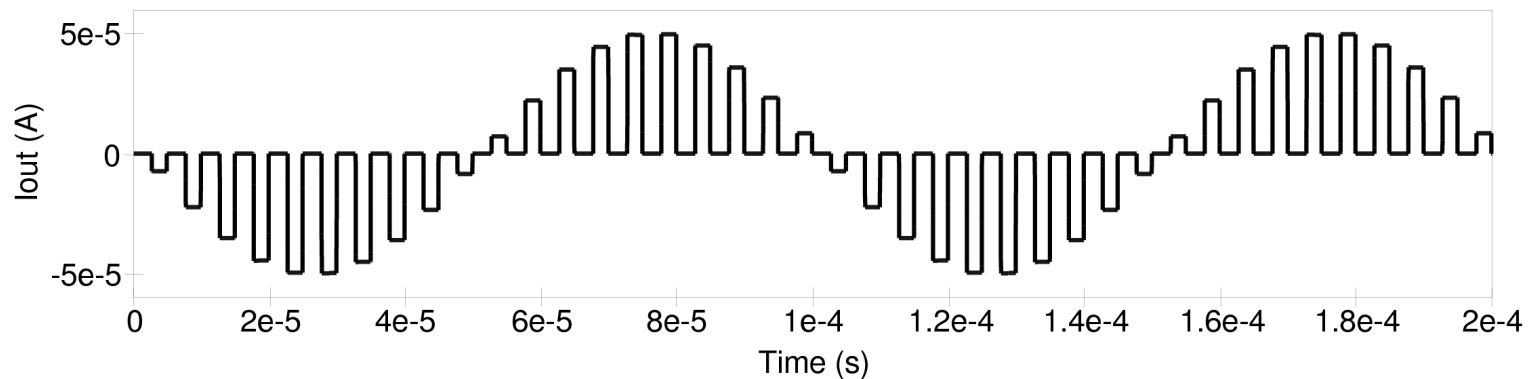
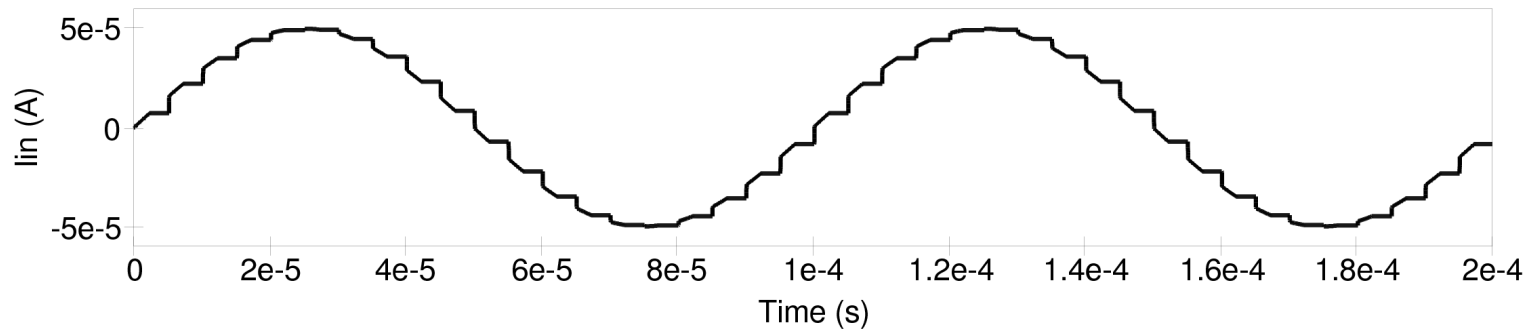
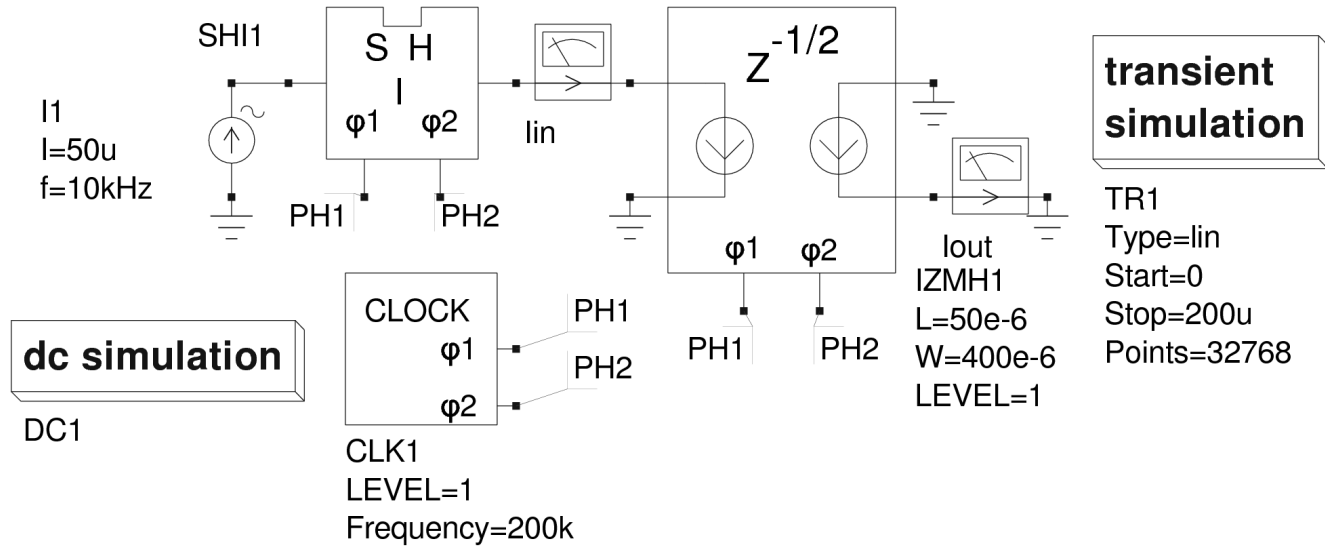


A macromodel for an ideal switched current memory cell

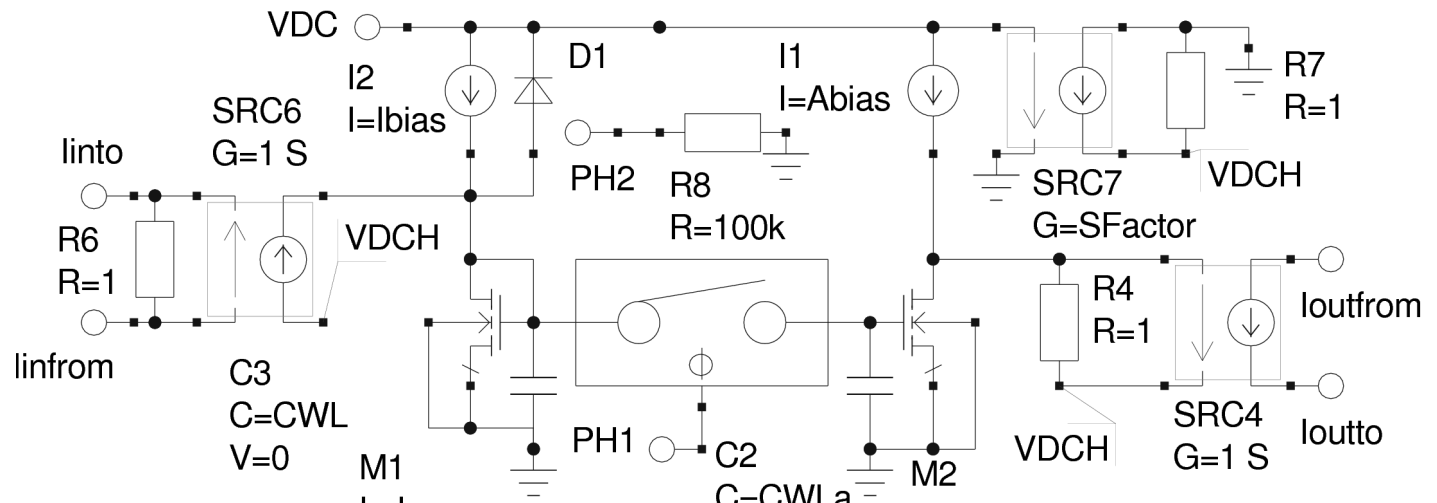


Ideal switched current memory cell macromodel test circuit and example waveforms: input signal $f=10\text{kHz}$, two phase clock sampling $f = 200\text{kHz}$

Signal frequency = 10kHz at 50 μA peak,
 $I_{\text{bias}} = 200\mu\text{A}$ DC,
 Two phase sampling frequency = 200kHz



A hybrid macromodel for a switched current first generation memory cell



$$C3 = 2 * W * L * COX / 3$$

$$C2 = \alpha * C3$$

Equation

Eqn2

$$AW = \alpha * W$$

$$Abias = \alpha * I_{bias}$$

$$L = L$$

$$W = W$$

$$VTO = 0.6$$

$$GAMMA = 0.7$$

$$PHI = 0.97$$

$$KP = 150e-6$$

$$THETA = 50e-3$$

VSW3

$$LEVEL = 1$$

$$R_{closed} = 1.0$$

$$R_{open} = 1e12$$

$$gain = 100.0$$

$$ShapeF = 0.5$$

$$L = L$$

$$W = AW$$

$$VTO = 0.6$$

$$GAMMA = 0.7$$

$$PHI = 0.97$$

$$KP = 150e-6$$

$$THETA = 50e-3$$

Equation

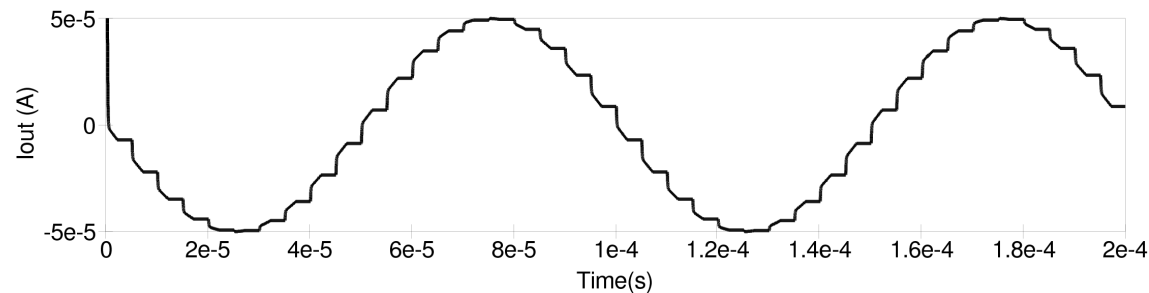
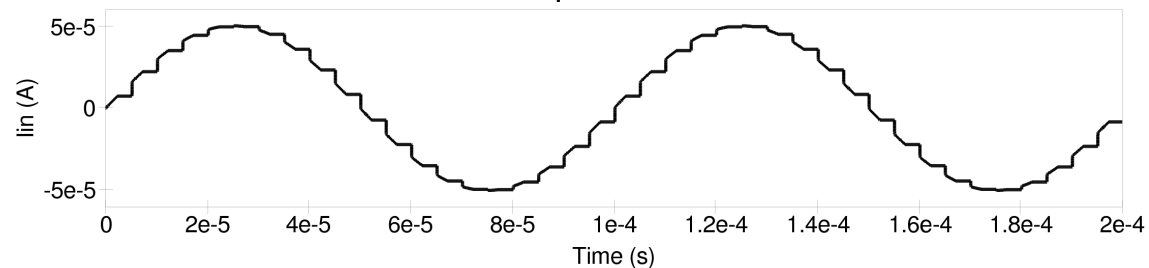
Eqn1

$$COX = 1.53e-3$$

$$CWL = 2 * W * L * COX / 3$$

$$CWL\alpha = \alpha * CWL$$

Signal frequency = 10kHz at 50μA peak,
I_{bias} = 200μA DC,
Two phase sampling frequency = 200kHz



A hybrid macromodel for a switched current first generation memory cell Verilog-A code

```

`include "discipline.vams"
`include "constants.vams"
module G1TranZMH (linfrom, linto, loutfrom, loutto, PH1, PH2, VDC);
inout linfrom, linto, loutfrom, loutto, PH1, PH2, VDC;
electrical linfrom, linto, loutfrom, loutto, PH1, PH2, VDC;
electrical n1, n2, n3, n4;
`define attr(txt) (*txt*)
parameter real L=10e-6 from [1e-20:inf] `attr(info='channel length' unit="m");
parameter real W=20e-6 from [1e-20:inf] `attr(info='channel width' unit="m");
parameter real LEVEL=1.0 from [1.0:inf] `attr(info='control voltage high' unit="V");
parameter real alpha=1.0 from [0.01:inf] `attr(info='output transistor W/L scale factor');
parameter real SFactor=0.5 from [0:inf] `attr(info='supply voltage scale factor');
parameter real Ibias=50e-6 from [1e-12:inf] `attr(info='dc bias current' unit="I");
real Rclosed, Ropen, gain, ShapeF, COX, CWL, CWLa, RL, Vmid, Abias;
real VTO, GAMMA, PHI, KP, THETA, P1, P2, P3, P4, P5, P6, P6a, P7, P8, P9;
real VGprime, VP, n, Beta, If, If1, Ir, Ir1;
real VGprimea, VPa, na, Betaa, Ifa, Ifa1, Ira, Ira1;
analog begin
@(initial_model)
begin
Rclosed=1.0; Ropen=1e12; gain=100.0; ShapeF=0.5; COX=1.5e-3;
CWL=2*W*L*COX/3; CWLa=CWL*alpha; Vmid=ShapeF*LEVEL;
VTO=0.6; GAMMA=0.7; PHI=0.97; KP=150e-6; THETA=50e-3;
P1 = -VTO+PHI+GAMMA*sqrt(PHI); P2 = GAMMA/2; P3 = P2*P2;
P4 = GAMMA*P2-PHI; P5 = PHI+4*$vt+1e-6; P6 = KP*W/L; P6a=P6*alpha;
P7 = 1/(2*$vt); P8 = 2*$vt*$vt; P9 = -PHI; Abias=alpha*Ibias;
end;

```

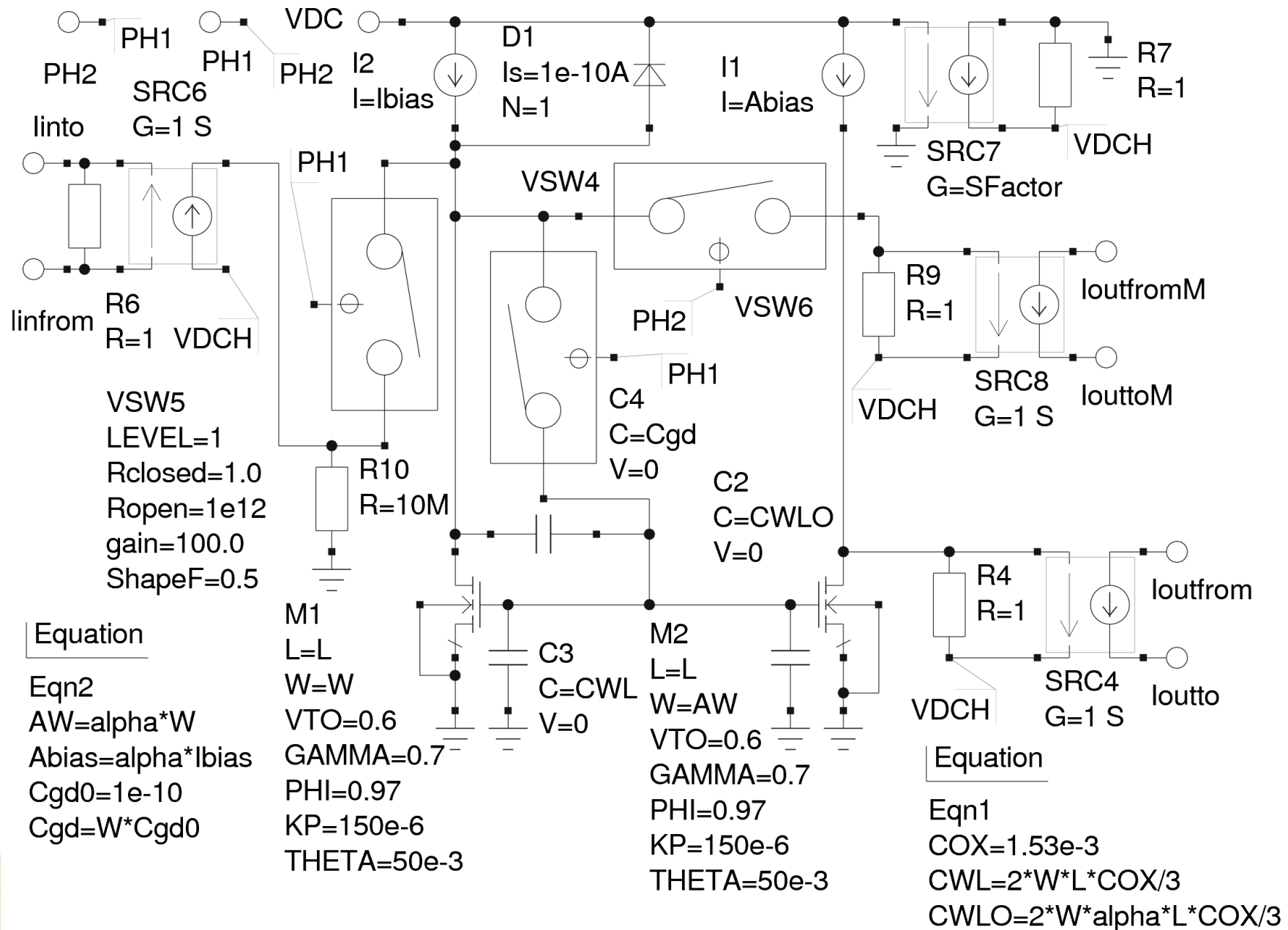
```

I(linfrom, linto) <+ V(linfrom, linto);
I(n4, n1) <+ V(linfrom, linto);
I(VDC, n1) <+ Ibias;
I(n1, VDC) <+ 1e-12*(limexp(V(n1, VDC)/$vt)-1.0)+V(n1, VDC)*1e-12;
VGprime = V(n1)+P1;
if (VGprime > 0.0)
    VP = P4+VGprime-GAMMA*sqrt(VGprime+P3);
else
    VP = P9;
n = 1+P2/sqrt(VP+P5);
Beta = P6/(1+THETA*VP);
If1 = ln(1+limexp(VP*P7)); If=If1*If1;
Ir1 = ln(1+limexp((VP-V(n1))*P7)); Ir=Ir1*Ir1;
I(n1) <+ P8*n*Beta*(If-Ir);
I(n1) <+ ddt(CWL*V(n1));
I(n1, n2) <+ V(n1, n2)/(Rclosed+Ropen/(1+limexp(gain*(V(PH1)-Vmid))));
I(n2) <+ ddt(CWLa*V(n2));
//
I(VDC, n3) <+ Abias;
VGprimea = V(n2)+P1;
if (VGprimea > 0.0)
    VPa = P4+VGprimea-GAMMA*sqrt(VGprimea+P3);
else
    VPa = P9;
na = 1+P2/sqrt(VPa+P5);
Betaa = P6a/(1+THETA*VPa);
Ifa1 = ln(1+limexp(VPa*P7)); Ifa=Ifa1*Ifa1;
Ira1 = ln(1+limexp((VP-V(n3))*P7)); Ira=Ira1*Ira1;
I(n3) <+ P8*na*Betaa*(Ifa-Ira);
I(n4, n3) <+ V(n4, n3);
I(loutfrom, loutto) <+ -V(n4, n3);
I(n4) <+ V(n4);
I(n4) <+ -SFactor*V(VDC);
end
endmodule

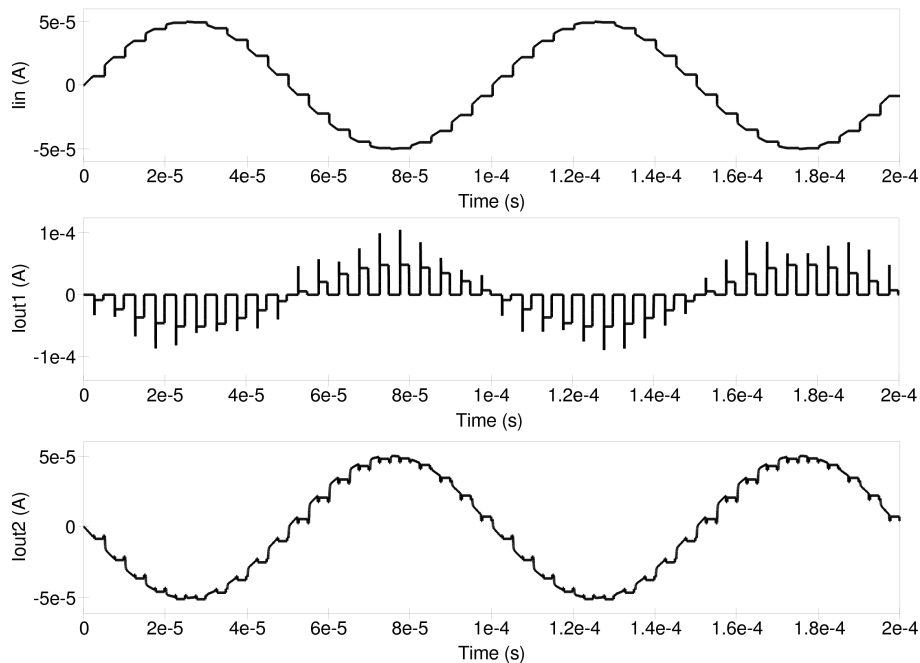
```



A hybrid macromodel for a switched current second generation memory cell: model

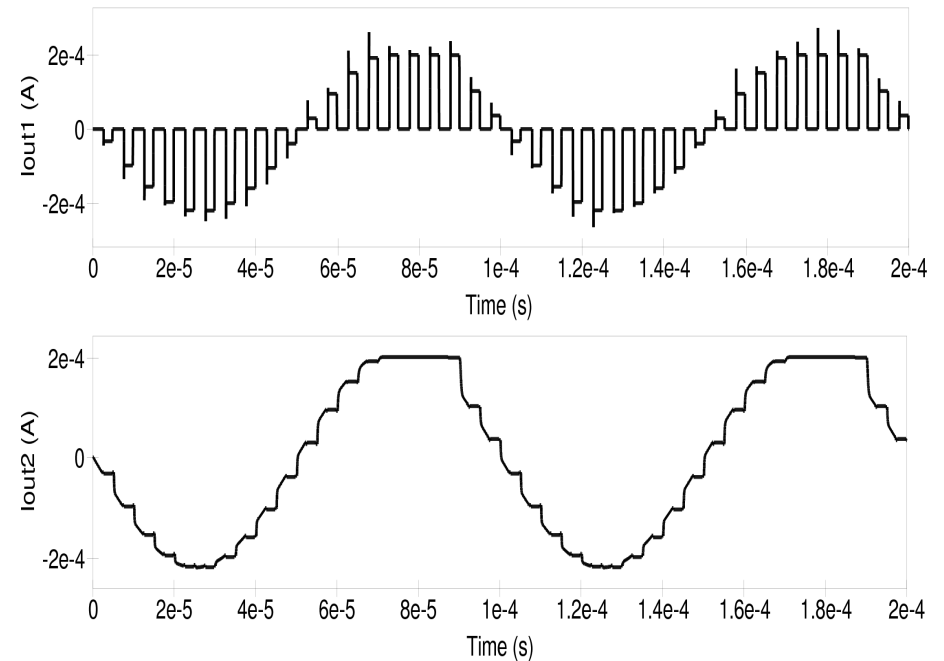


A hybrid macromodel for a switched current second generation memory cell: waveforms



Signal frequency = 10kHz at $50 \mu\text{A}$ peak,
 $I_{bias} = 200 \mu\text{A}$ DC,
Two phase sampling frequency = 200kHz
 i_{out1} equivalent to $i_{outM3}(Z)$, and
 i_{out2} to $i_{outM4}(Z)$

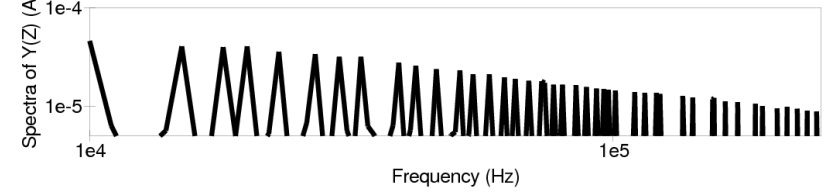
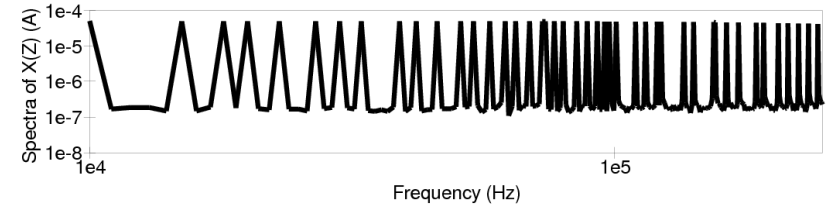
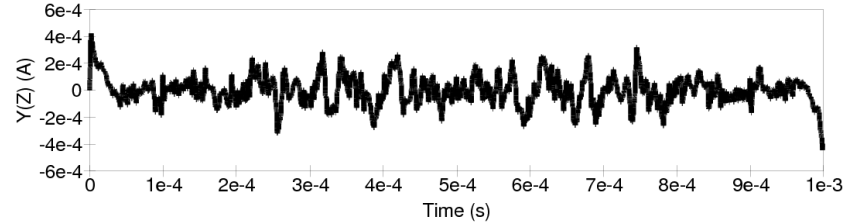
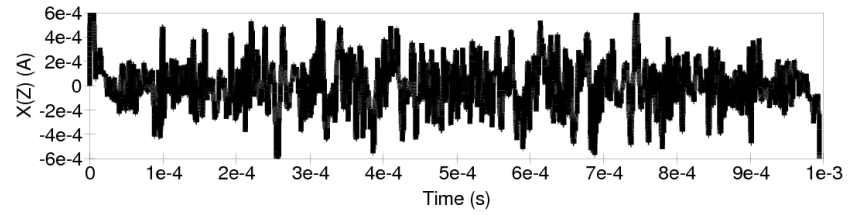
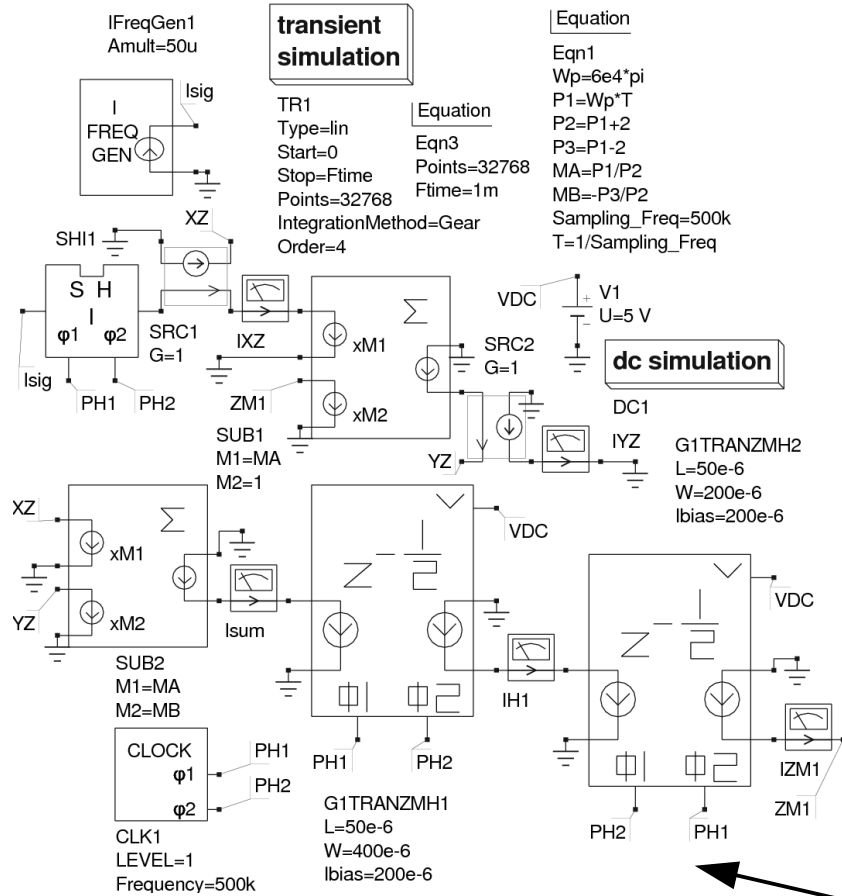
NO DISTORTION



Signal frequency = 10kHz at $210 \mu\text{A}$ peak,
 $I_{bias} = 200 \mu\text{A}$ DC,
Two phase sampling frequency = 200kHz
 i_{out1} equivalent to $i_{outM3}(Z)$, and
 i_{out2} to $i_{outM4}(Z)$

DISTORTION

A large signal AC low-pass switched current filter example



S Domain transfer function

$$T(S) = \frac{1}{1 + \frac{S}{\omega_p}}$$

Bilinear S to Z transform

$$S = \frac{2}{T} \frac{1 - Z^{-1}}{1 + Z^{-1}}$$

$$Y(Z) = [MA * X(Z) - MB * Y(Z)] * Z^{-1} + MA * X(Z)$$

Where $T(Z) = \frac{Y(Z)}{X(Z)}$, $MA = \frac{\omega_p * T}{\omega_p * T + 2}$ and $MB = \frac{\omega_p * T - 2}{\omega_p * T + 2}$

T is the period of the two phase sampling clock

$$\omega_p = 2 * \pi * f_p \text{ and } f_p = 20\text{kHz}$$



Relative transient timings for $Z^{-1/2}$ hybrid macromodels

Memory cell model	Number of nodes	Number of linear components	Number of non-linear components	Explicit Trap. integration	Implicit Gear integration (order 4)
Ideal	7	6	2	1	1.1
Gen. 1	11	11	4	5.1	5.5
Gen. 2	14	14	6	10.5	11.2

- The Table given above clearly indicates that the relative simulation time for the three hybrid switched current memory cell models increases as the number of nodes and non-linear components increases.
- This observation accounts for the fact that semiconductor device level models of switched current circuits are significantly slower than hybrid macromodels.

Summary

- **Transient simulation of two phase switched current integrated circuits is often undertaken at semiconductor device level, resulting in long simulation times even when analysing the performance of moderate size circuits.**
- **This paper introduces a hybrid Verilog-A/subcircuit modeling technique for the construction of functional behavioral macromodels which have improved transient simulation run times when compared to device level simulation.**
- **Hybrid switched current integrated circuit macromodels are particularly suitable for the simulation for of mixed-mode electronic systems which include both established analog and digital components plus emerging technology devices modeled at both functional and semiconductor hierarchical levels.**

