Fabrication et caractérisation de transistor réalisée à basse température pour l'intégration 3D séquentielle

Jessy Micout

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THÈSE

Pour obtenir le grade de

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Présentée par

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Thèse dirigée par **Gérard GHIBAUDO, HDR, CNRS Alpes**

préparée au sein des **Laboratoires CEA-LETI et IMEP-LAHC**
dans **l'École Doctorale Electronique, Electrotechnique, Automation et Traitement du Signal**

Fabrication et caractérisation de transistors réalisés à basse température pour l'intégration 3D séquentielle

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CONTENTS

Acknowledgments 1

Contents i

List of figures iv

List of tables x

1. Technological context 1

1.1 3D integration 2

1.2 MOSFET transistor 5

1.3 Challenge for the junction formation 8

1.3.1 Profile influence on electrical performance 8

1.3.2 Extension Last/Gate First Integration process at high temperature 10

1.3.3 Gate First/Gate Last and Xlast/Xfirst integration schemes 12

1.4 Goal of this work 14

2. Low-Temperature Extension-Last FDSOI integration 15

2.1 Background 16

2.1.1 Control of the amorphization thickness 20

2.1.2 SPER rate dependency 21

2.1.3 EOR-defects influence on electrical performance 27

2.2 Analysis on Extension Last integration 34

2.2.1 Review of previous electrical results 34

2.2.2 R_{access} improvement 38

2.2.3 DIBL optimization 52

3. Low-Temperature Extension-First FDSOI integration 61

3.1 Results and conclusion of previous studies 62

3.1.1 Process Of Reference process flow of a 14 nm FDSOI ... 62
3.1.2 Electricals results ... 66
3.1.3 R_{access} optimizations ... 68
3.2 Extension First without liner ... 75
3.2.1 Advantage to implant through bare silicon ... 75
3.2.2 Integration proposition ... 79
3.3 EOT improvement ... 83
3.3.1 Electrical measurements ... 83
4. Low-Temperature FinFET integration ... 95
4.1 FinFET introduction ... 97
4.2 Finfet junction schemes ... 98
4.2.1 Defect-crystalline integrity ... 99
4.2.2 Angle restriction and conformal doping ... 101
4.2.3 Bending Fin ... 103
4.2.4 Embedded *In situ* doped raised source drain epitaxy ... 104
4.2.5 Description of the FinFET process flow ... 107
4.3 Proposition for Low Temperature devices ... 109
4.3.1 Horizontal Seed configuration ... 111
4.3.2 Central Seed configuration ... 112
4.3.3 Lateral seed configuration ... 113
4.3.4 The Double SPER configuration ... 114
4.4 Fabrication and Electrical characterization ... 122
4.4.1 Process flow modification ... 122
4.4.2 Electrical results ... 126
4.4.3 Non-recrystallization default ... 132
4.4.4 Straggle and EOR density diminution ... 134
4.4.5 Strain effect ... 139

4.5 Perspective on potential integration schemes ... 141
4.5.1 Summary of integration schemes ... 152
5. Conclusion ... 157
Bibliography ... 161
Résumé en Français ... 173

LIST OF FIGURES

Figure 1.1: Transistor cost and lithography tool cost versus years, from [2] ... 2

Figure 1.2: Bulk, FDSOI and FinFET architectures ... 3

Figure 1.3: Description of 3D integration process flow, in parallel integration (a) or sequential integration (b) ... 4

Figure 1.4: Illustration of the trade-off for the 3D sequential integration ... 5

Figure 1.5: nMOS transistor scheme in on state and I_d-V_g characteristics ... 6

Figure 1.6: Illustration of the different components of the total resistance ... 8

Figure 1.7: Schematic illustration of the junction profile influence on the I_d-V_g characteristics ... 9

Figure 1.8: Standard process flow for 28 nm FDSOI technology with gate first/Extension Last integration 11

Figure 1.9: Main differences between Gate First/Gate Last and Extension First/Extension Last integration scheme ... 13

Figure 1.10: Transistor performance versus transistor cost according to the considered integrations schemes and the architectures used in this thesis ... 13

Figure 2.1: Ion implantation and consequences on lattice crystal ... 16

Figure 2.2: Illustration of the SPER process ... 17

Figure 2.3: TEM cross section picture of an as-implanted boron-doped sample and the electrical doping concentration measured by ECV, after a SPER activation at 600 °C/2 min (from [9]) ... 18

Figure 2.4: KMC simulations of the amorphous thickness as a function of the dose rate ... 21

Figure 2.5: Atomistic configurations for (100), (011) and (111) crystalline plane, from [18] ... 22

Figure 2.6: Schematic representation of normal and twin configuration from [31], and TEM cross section picture evidencing stacking fault ... 23

Figure 2.7: Schematic illustration of crystalline orientations for <110> and <100> -oriented channel ... 24

Figure 2.8: SPER rate as a function of the temperature and the crystalline orientation [30], and the temperature and doping specie for the <100> crystalline orientation [24] ... 26

Figure 2.9: Illustration of the EOR defects formation ... 28

Figure 2.10: Illustration of the influence of the EOR defects on the junction properties ... 28

Figure 2.11: Summary of the expected degradation on I_d-V_g curves due to EOR effects 30

Figure 2.12: Illustration of the cut-off and sinking effect, from [37] 31

Figure 2.13: Sheet resistance measurements as a function of the annealing duration, with different location of the EOR, from [37] 32

Figure 2.14: Recommendation for carbon profile to limit both the TED effect and the BIC formation 33

Figure 2.15: Process flow for HT and LT devices 35

Figure 2.16: I_{on}-I_{off} and R_{on} -DIBL trade-off for p&n MOS devices. 37

Figure 2.17: I_d-V_g and electrical schemes of 500 °C- and 600 °C- activated devices, with an analytical fitting. 38

Figure 2.18: a) TEM observation of a 500 °C-activated device, b) I_{on}-I_{off} performance of the observed device 39

Figure 2.19: Electrical simulation by taking into account the precise dose rate of the amorphization profile in .a) and the time-annealing evolution at 500 °C in .b), and TEM cross section picture in c). 40

Figure 2.20: I_{on}-I_{off} trade-off before and after a post back end supplementary annealing (500 °C/10 min) 41

Figure 2.21: 3D view of the recrystallization mechanism with amorphization profile shown in Figure 2.19.a) 42

Figure 2.22: TEM cross section picture of 600 °C-activated nMOS (.a), 500 °C-activated pMOS (.b) and 500 °C-activated nMOS (.c).. 43

Figure 2.23: Time-annealing evolution of 600 °C-activated nMOS (.a), 500 °C-activated pMOS (.b) and 500 °C-activated nMOS (.c).. 44

Figure 2.24: Expected recrystallization mechanism for two seed configurations....................................... 45

Figure 2.25: 28 nm electrical simulation for nMOS splits, evidencing the negligible influence of the Silicide/c-Si interface length ($L_{contact}$) above 30 nm 46

Figure 2.26: KMC simulations of the a/c front with <110>-and <100> oriented channel, for 600C°C-activated nMOS. 48

Figure 2.27: I_{on} I_{off} and I_d-V_g curve with 600 °C/tilt 0° split 49

Figure 2.28: time annealing evolution for 600 °C activated nMOS devices, with or without tilt 49

Figure 2.29: KMC simulation of oxygen and nitrogen recoil... 51

Figure 2.30: DIBL as function of L_g for HT and LT split.. 53

Figure 2.31: Process simulations of the boron chemical-concentration profile, a) as implanted and b) after a 630 °C/2 h annealing. 54

Figure 2.32: Boron solubility as a function of the temperature from [54] 56

Figure 2.33: Process simulations as implanted of the boron chemical-concentration profile, with a reduction of the boron concentration in the channel 57

Figure 3.1: Process flow of HT POR devices for a 14 nm technology 63

Figure 3.2: Diverging steps in the process flow of High-Temperature and Low-Temperature devices 65

Figure 3.3: I_{on}-I_{off} trade-off from [57] 67

Figure 3.4: R_{access} for low temperature splits from [57] 68

Figure 3.5: Illustration of the morphological result, and the interpretation for electrical device 69

Figure 3.6: (a) Measured R_{sheet} and (b) calculated R_{sheet} as a function of the activation level for low temperature splits from [1] 70

Figure 3.7: EDX and TEM of No PAI sample on full sheet after 600 °C/ 2 min annealing 71

Figure 3.8: SIMS of the as-implanted n-type samples 71

Figure 3.9: (a) LT and HT device configuration and (b) R_{spa} as a function of the offset spacer thickness . 73

Figure 3.10: I_{on} versus the doping concentration into the RSD 74

Figure 3.11: Structures used for to study the nitrogen and oxygen recoil into dopant deactivation 76

Figure 3.12: Dopant profiles and TEM cross section pictures after implantation (through bare silicon splits) 77

Figure 3.13: R_{sheet} results of p and n type, though nitride, oxide and bare silicon 78

Figure 3.14: Main step modification into the Extension First integration scheme to implant without nitrogen recoil 79

Figure 3.15: T_{si} consumption according the etching recipe 80

Figure 3.16: CD measurements during the process flow 81

Figure 3.17: Main steps of the X^{1st}/Gate Last integration scheme 82

Figure 3.18: C-V measurements and extracted EOT for LT and HT devices 84

Figure 3.19: I_g-V_g for LT splits according to three gate lengths 85

Figure 3.20: Normalized $I_{g,lin}$ vs L_g for both methods 88

Figure 3.21: Comparison between simulated and experimental gate current for short and long gate lengths 90

Figure 3.22: ΔEOT variation as function of the gate length 91

Figure 3.23: Illustration of the oxygen-ingress phenomenon 92

Figure 4.1: Planar and Fin FETs on SOI architecture. 97

Figure 4.2: Implantation-angle definition for this work 99

Figure 4.3: TEM picture from [5]. Due to the surface proximity, new recrystallization fronts appear, and can cause defect formation. 100

Figure 4.4: Angle restriction for tilted implantation for a) unipolar and b) N|P transition region (SRAM configuration) 101

Figure 4.5: Illustration of the single-sided implantation 102

Figure 4.6: Hard Mask utilization to improve the angle restriction 103

Figure 4.7: Main steps of a FinFET flow with embedded *in situ* doped raised source drain epitaxy 104

Figure 4.8: Main steps of e-RSD with for thermal-budget devices 105

Figure 4.9: TEM cross section pictures of HT e-RSD FinFET with or without oxidation/desoxidation cycles 106

Figure 4.10: R_{access} and hole mobility with and without oxidation/desoxidation cycles 107

Figure 4.11: Mains steps of the FinFET process flow 108

Figure 4.12: Structure used for simulations 110

Figure 4.13: TEM pictures of the fin-width cross section after two amorphizing implantations 111

Figure 4.14: R_{on}-DIBL trade-off for the horizontal-seed configuration, for different seed thicknesses...... 112

Figure 4.15: R_{on}-DIBL trade-off for the central-seed configuration, for different amorphization thicknesses 113

Figure 4.16: R_{on}-DIBL trade-off for the lateral-seed configuration, for different seed thicknesses 114

Figure 4.17: Illustration of the DSPER process 115

Figure 4.18: Zoom of the cross section of the fin width after the first amorphizing implantation 116

Figure 4.19: TEM picture of the fin-width cross section of a 35 nm-thick fin after the DSPER process ... 117

Figure 4.20: TEM picture of the fin-width cross section of a 16 nm-thick fin after the DSPER process ... 118

Figure 4.21: Variation of the measured fin width after the HF clean 118

Figure 4.22: Illustration of the etch-stop layer consumption, after the gate patterning, and its consequence on the process flow 119

Figure 4.23: R_{on}-DIBL trade-off for non-doped zone surrounding the fin, for different seed thicknesses. 120

Figure 4.24: Relative R_{on}-DIBL trade-off for different non-recrystallized thicknesses at the top fin 122

Figure 4.25: Process flow of High-Temperature and Low-Temperature devices 123

Figure 4.26: Diagram of the a/c interface depth for different implantation conditions 124

Figure 4.27: Tilted SEM pictures of FinFET devices with or without implantation prior to the epitaxy 125

Figure 4.28: TEM pictures at the length and width cross section of Low temperature FinFETs 126

Figure 4.29: I_{on}-I_{off} trade-off of HT and LT FinFET 127

Figure 4.30: Simulated and experimental amorphization depth for ‘T_{amo} = 6 nm’ splits 128

Figure 4.31: I_{on} and I_{off} values plotted as a function of the fin widths 129

Figure 4.32: I_d-V_g curves, $V_{t,sat}$, DIBL and SS vs L_g at for the ‘T_{amo} = 6 nm’ split. 130

Figure 4.33: I_{on} I_{off} performance benchmark of FinFET devices, built on silicon channel with embedded *in situ* doped raised source drain. 131

Figure 4.34: Illustration of two possible recrystallization defaults 133

Figure 4.35: R_{on}-W for LT ‘T_{amo} = 6 nm’ split and HT POR 134

Figure 4.36: R_{on}-DIBL for ‘T_{amo} = 6 nm’ and ‘T_{amo} = 12 nm’ LT splits 135

Figure 4.37: Dopant profile simulation for ‘T_{amo} = 12’ and ‘T_{amo} = 6’ nm splits, as implanted the final profile after an 630 °C/2 h annealing 136

Figure 4.38: $I_{d,min}$ vs L_g for L_g=60 nm and for low temperature splits 137

Figure 4.39: Evolution of the TED and straggle effects with scaling 138

Figure 4.40: Process flow differentiation for low temperature devices with or without recess, and ellipsometry measurements 139

Figure 4.41: Relative mobility for HT POR, LT split with or without recess 140

Figure 4.42: Main steps of the process modification to use the S-SPER 142

Figure 4.43: R_{on} comparison between a fully activated fin and the S-SPER process 143

Figure 4.44: Cross sections following the fin width and gate length direction of FinFET after gate formation, with the channel etching step 144

Figure 4.45: Cross sections following the fin width direction of FinFET after the gate formation, with the targeted channel etching, and with an over etching case 145

Figure 4.46: Process flow to form a Hard Mask at the top fin 146

Figure 4.47: Illustration of the consequence of changing the channel orientation on the recrystallization mechanism 148

Figure 4.48: Illustration of a twisted and non-twisted implantation........ 149

Figure 4.49: Main steps of the non-twisted SPER........ 150

Figure 4.50: Fin-width cross section after the recess........ 151

Figure 4.51: Main steps of the NTP process........ 152

LIST OF TABLES

Table 1: First-order extrapolation of the SPER rate (nm/min) as function of temperature, dopant concentration and crystalline orientation 26

Table 2: Split table details for low temperature splits 36

Table 3: Temperature/annealing couple and the estimated $L_{contact}$ 47

Table 4: Split details for p and n MOS devices 66

Table 4.1: Implantation split description 124

Table 4.2: Minimal SiN thickness according two implantations and node configurations 147

Table 4.3: Summary of integration optimizations 153

1. TECHNOLOGICAL CONTEXT

Contents

1. Technological context ... 1

1.1 3D integration ... 2

1.2 MOSFET transistor ... 5

1.3 Challenge for the junction formation ... 8

1.3.1 Profile influence on electrical performance ... 8

1.3.2 Extension Last/Gate First Integration process at high temperature ... 10

1.3.3 Gate First/Gate Last and Xlast/Xfirst integration schemes ... 12

1.4 Goal of this work ... 14

1.1 3D INTEGRATION

For 50 years, the semiconductor market has followed the Moore law, which consists in doubling the transistor density every 18 months. Since then, industries and laboratories have followed this empirical law, as well-described by Intel in [1]: “Performance […] and cost are two key drivers of technological development. As more transistors fit into smaller spaces, processing power increased and energy efficiency improved, all at a lower cost for the end user. This development not only enhanced existing industries and increased productivity, but it has spawned whole new industries empowered by cheap and powerful computing”. Such an evolution has the consequence that, today, microelectronic is everywhere: from computer to internet of things, from automobile to spacecraft.

Manufacturing Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) has thus been required in the past decades to reduce its physical dimensions in order to increase the device performance and simultaneously reduce its cost. Device dimensions are however approaching the physical limits of miniaturization, while tool cost are increasing, as underlined in Figure 1.1, which describes transistor and lithography tool costs as a function of the years.

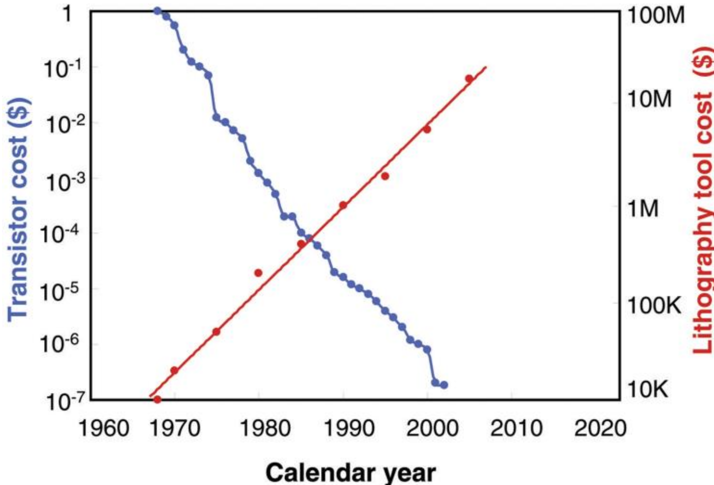


Figure 1.1: Transistor cost and lithography tool cost versus years, from [2]

Merely reducing the transistor dimensions becomes more and more challenging. Besides, the scaling has also led to increase the parasitic phenomena, such as short channel effects (SCE). These effects are due to the loss of the electrostatic control by the gate on the channel. One way to overcome this issue is to reduce the active zone width, while its thickness is simultaneously increased in order to maximize the drive current of such devices. The active zone is hence called fin in reference to its shape. Another alternative is to reduce the space-charge zone by introducing a Buried Oxide (BOX), allowing to fully deplete the region. Devices built in the first (respectively second) configuration are called FinFETs (FDSOIs). The geometry difference between bulk, FDSOI and FinFET architectures is shown in Figure 1.2 (the spacers and epitaxial regrowth are not represented for the sake of understanding).

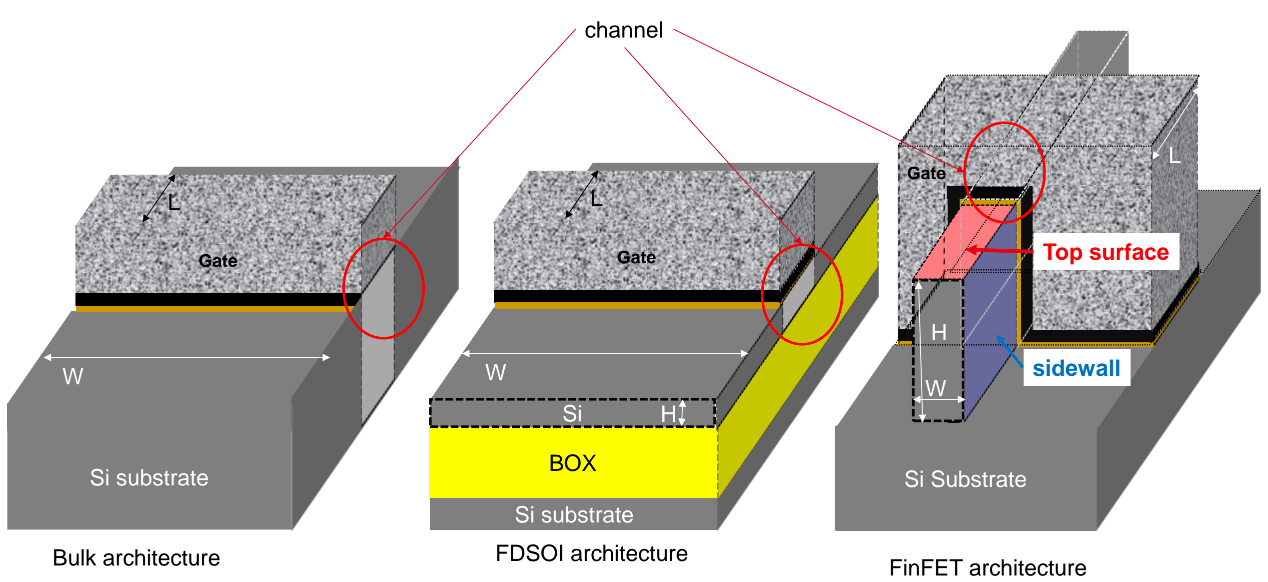


Figure 1.2: Bulk, FDSOI and FinFET architectures

It can be seen that contrary to FDSOI devices, FinFETs are inherently 3D, with the gate surrounding the channel, while the gate is only 2D in a FDSOI device. Thanks to an active zone both narrower and thicker, the charge in the channel for FinFET is controlled by the gate at the top and at the side, which maintains a suitable electrostatic coupling. Better electrostatic control is achieved thanks to the BOX for FDSOI. In this thesis, transistors will be manufactured for digital

applications, according to the FDSOI architecture in chapter 2 and 3, and to the FinFET on SOI architecture in chapter 4.

In order to keep increasing density of integrated circuit, an alternative that is additionally compatible with these architectures is offered by the 3D integration scheme. This technique consists in stacking different transistor levels, one on the top of the other [3]. Two integration types might be distinguished. The first one is the parallel integration, where different chips are processed independently, then stacked vertically and connected afterward. The second one is the sequential integration, where transistor layers are processed sequentially and the stacked layers can be connected at the transistor scale. These two types of 3D integration are illustrated in Figure 1.3.

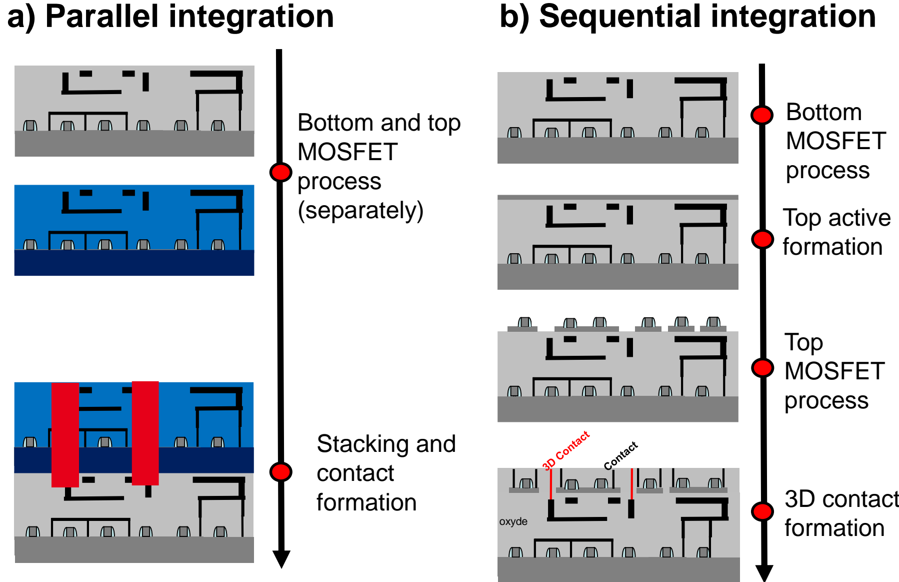


Figure 1.3: Description of 3D integration process flow, in parallel integration (a) or sequential integration (b)

While the manufacturing process with the parallel integration is relatively simpler, a much higher alignment accuracy is reached with the sequential one [4],[5]. This integration is an active field in the CEA-LETI. One of the main challenge of such an integration is to be able to process a high performance transistor at the top tier with a low thermal budget in order to preserve the transistor at the bottom from any degradation. As illustrated in Figure 1.4, the standard thermal budget to manufacture a transistor is indeed superior to 1000 °C, while the thermal stability of a

manufacturing MOSFET is insured at 400 °C, which corresponds to the standard thermal budget of the Back End Of Line.

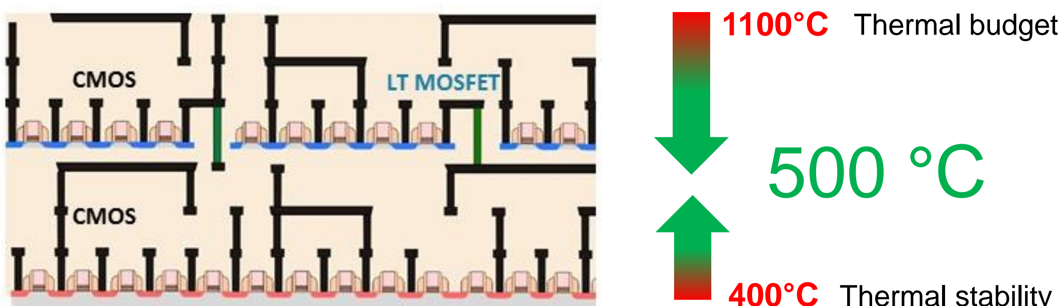


Figure 1.4: Illustration of the trade-off for the 3D sequential integration

To preserve the bottom transistor, the top one should hence be manufactured at low thermal budget, below 500 °C. One of the main challenge consists in changing the dopant activation methodology that is commonly performed with a high thermal budget (>1000 °C). The technological option chosen at CEA-LETI and for this work is to form the junction of top transistors by Solid Phase Epitaxial Regrowth (SPER), allowing to reduce the activation anneal at temperatures that are compatible with 3D sequential integration. This work mainly focuses on the dopant activation with such a process in order to manufacture low temperature transistor. The SPER process will be explained in section 2.1.

1.2 MOSFET TRANSISTOR

In this section, a brief presentation of the structure and the basic principles of a MOSFET transistor are presented. For more details, the reader can refers to [6], [7].

The MOSFET is a transistor used for switching electronic signals and is usually composed of three layers. At first, a semiconductor substrate, which enables the current to flow between two regions, called source and drain (S&D). The current can flow thanks to a field effect via the polarization of a layer formed by a metal (gate) through a thin layer of dielectric material (gate

oxide). The region below the gate is named channel. If the source and drain regions are doped with n-type impurities (phosphorus for this thesis), electrons are the majority charge carriers and the device is thus called nMOS. The device is called pMOS in the case of p-type impurities (boron in this thesis), where holes are the majority charge carriers. Figure 1.5.a) illustrates the nMOS transistor scheme in on state, with the region previously mentioned.

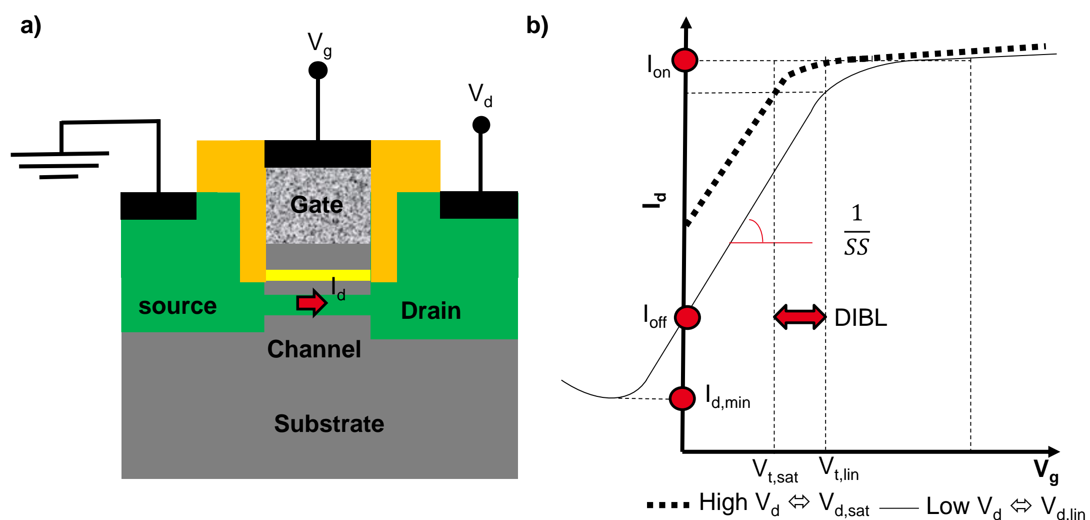


Figure 1.5: nMOS transistor scheme in on state and I_d-V_g characteristics

When the gate voltage (V_g) is positive and above a specific voltage called threshold voltage (V_t), device is in strong inversion mode. An electron layer is formed below the gate stack, allowing the conduction between the source and the drain. The drain current characteristic (I_d) as a function of V_g is illustrated in Figure 1.5.b). For $V_g<V_t$, the transistor is not conductive (off state) since the inversion channel is not formed. Parasitic effects can however lead to a conduction. For $0<V_g<V_t$ (weak inversion mode), the flowing current is defined as sub threshold current. In Figure 1.5.b) two different curves are shown, that depends on the drain voltage (V_d) values. At low V_d, transistors are in the linear mode, while at high V_d they are in saturation mode. Some figures of merits used during this thesis are also shown such as the on-state current (I_{on}), off-state current (I_{off}), the minimum drain current ($I_{d,\ min}$). The linear threshold voltage $V_{t,\ lin}$ and saturation one $V_{t,\ sat}$ are not equal in Figure 1.5.b). This is due to the Drain Induced Barrier Lowering (DIBL), which is one of

the SCE component. Besides, the sub threshold Swing (SS), which should be close to 60 mV/decade, might also be degraded.

In Figure 1.5.a) the source and drain are additionally considered as perfectly conducting. As the current flows through the contact lines and the source to the drain, the voltage can however drop due to the material resistivity (the silicon and metal contact). This supplementary and parasitic resistance is called access resistance. In a long channel device, the access resistances are negligible compared to the channel one. In a short channel device, these two resistances become however comparable [2]. The total transistor resistance R_{on} (also referred as R_{tot}) is then defined as:

$$R_{on} = \frac{V_{d,lin}}{I_{d,lin}} = R_{channel} + R_{access} \tag{1}$$

In this work, the access resistances will be decomposed as the sum of three components:

$$R_{access} = R_{co} + R_{epi} + R_{spa} \tag{2}$$

Each component of the access resistance correspond to a specific area at the source and drain regions. R_{co} corresponds to the contact resistance between the contacts and the doped region, R_{epi} to the doped region and R_{spa} is the resistance corresponding to the zone below the offset spacer. The different contributions to the total resistance R_{on} are illustrated in Figure 1.6.

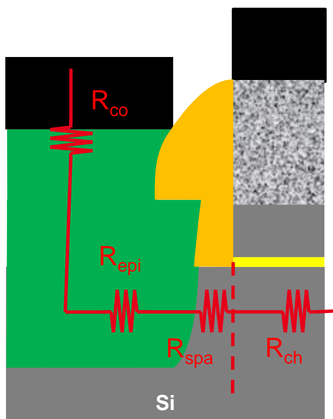


Figure 1.6: Illustration of the different components of the total resistance

In the past decades the device performance (I_{on}/I_{off} ratio) was mainly limited by the mobility, which describes the ability of the carrier charge (hole or electron) to move through a solid according to a specific electric field. Mobility boosters, such as strain effects, were thus the main lever to improve performance. Today, the significant current degradation is due to too-high access resistance [8]. This thesis will be thus focused on this parameter, plus the non-conventional dopant activation in order to manufacture low-temperature transistor.

1.3 CHALLENGE FOR THE JUNCTION FORMATION

The influence of the concentration profile of the charge carriers on electrical performance will be at first described, to underline the importance to position the junction profile. The standard junction formation will be secondly explained because manufacturing low-temperature transistor directly inherits from the high-temperature process flow. Four integration schemes (Extension First/Extension Last, Gate First First/Gate Last) involved in this thesis will be then described. The benefits and drawbacks related to each option will be finally presented.

1.3.1 Profile influence on electrical performance

Junctions that were originally defined in microelectronics corresponds to the interface between p-type and n-type regions. In this work, junctions represents the limit between the source (or the drain) and the channel, which is undoped in FDSOI and FinFET devices. Positioning junctions is generally defined by using the iso-concentration profile position of charge carriers. While a high doping concentration (above 1×10^{20} at/cm^3) in the Source and Drain is compulsory to lower the access resistance, the dopant concentration in the channel should be below 1×10^{19} at/cm^3 to avoid DIBL degradation [9]. While an ideal junction for digital application is sketched in Figure 1.7.a), in Figure 1.7.b) is represented an underlapped with a small abruptness one. Figure 1.7.c) drafts the corresponding I_d-V_g curves.

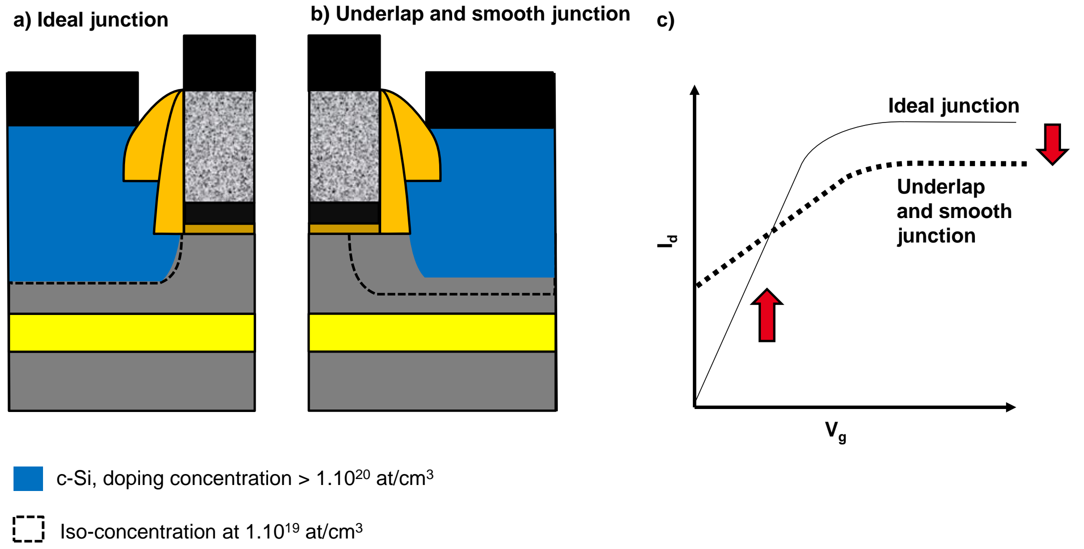


Figure 1.7: Schematic illustration of the junction profile influence on the I_d-V_g characteristics

In Figure 1.7.a), dopants are perfectly placed under the first spacer, with a high activation level, above 1×10^{20} at/cm^3. The junction is additionally abrupt, as highlighted by the iso-concentration at 1×10^{19} at/cm^3 very close to the high activation area. On the contrary, in Figure 1.7.b), the high activation level is located at the edge of the first spacer while the iso-concentration at 1×10^{19} at/cm^3 is situated in the channel, which highlights a smooth junction profile in the doping concentration profile. Figure 1.7.c) summarizes the influence of the junction formation on the electrical performance of the device. In the second case, the drive-in current decreases due to a too

small activation level under the spacer. But, at the same time, because dopants with concentration above 1×10^{19} at/cm^3 are located under the channel, the electrostatic control is not maintained, and the off-state current, the DIBL and the sub threshold swing (SS) increase. Positioning the junction is thus a key challenge to address high performances.

1.3.2 Extension Last/Gate First Integration process at high temperature

The main steps of the High Temperature Process Of Reference (HT POR) are described in Figure 1.8 with a Gate First/Extension Last integration scheme. In that case, a 28 nm FDSOI architecture is used.

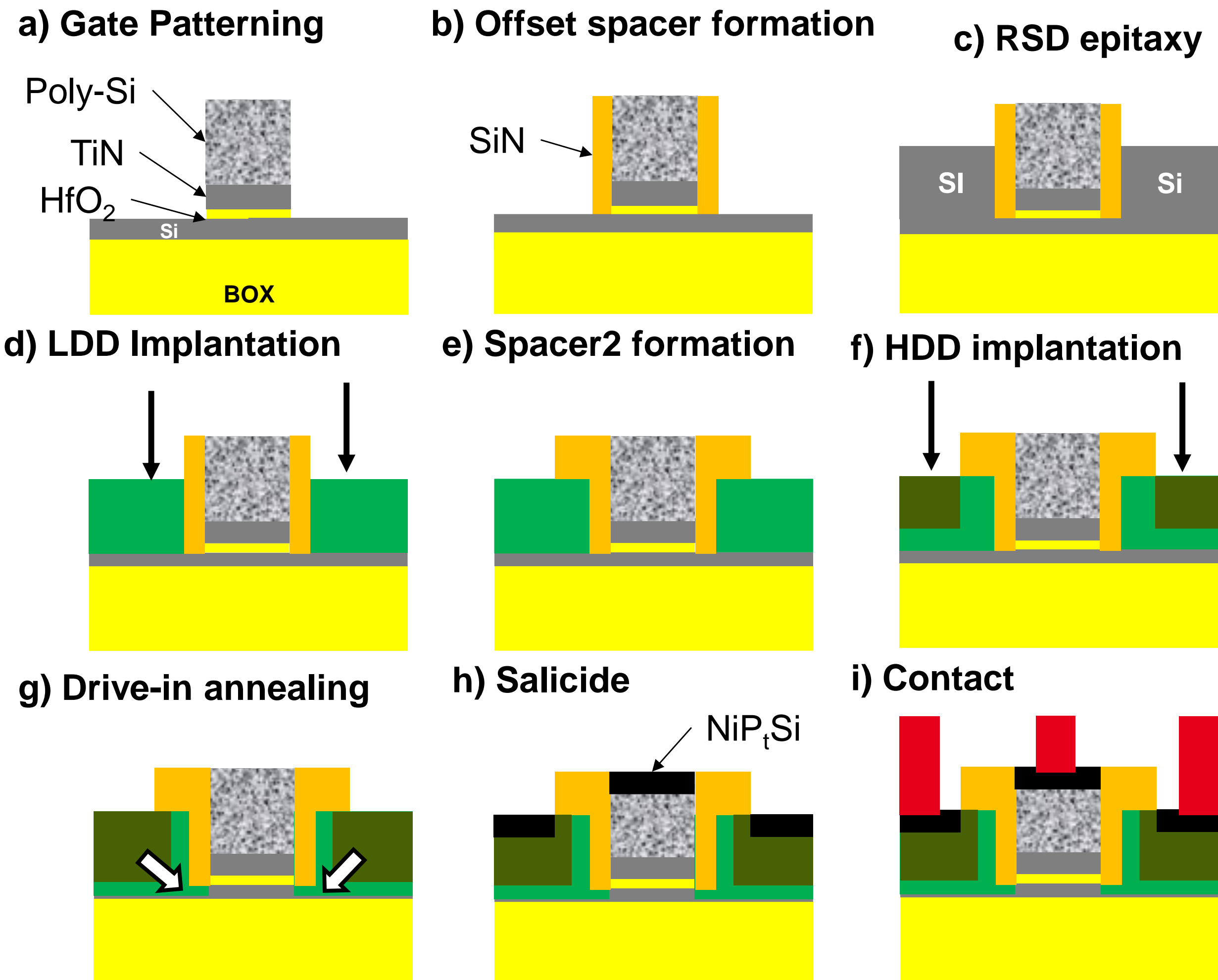


Figure 1.8: Standard process flow for 28 nm FDSOI technology with gate first/Extension Last integration

FDSOI devices are fabricated on a 7 nm-thick Si channel on a 25 nm Buried Oxide. The gate stack is at first deposited then etched (Gate First integration), and is composed of an HfO_2, a TiN, and a Poly Si stack (Figure 1.8.a). SiN is then deposited and etched in order to form the offset spacer (Figure 1.8.b). Raised Source Drain (RSD) epitaxy is performed (Figure 1.8.c). A Lightly Doped Source/Drain (LDD) implantation is carried out (Figure 1.8.d) after the offset spacer formation to form junctions, followed by the second spacer formation (Figure 1.8.e) and a Heavily Doped source/Drain (HDD) implantation (Figure 1.8.f). Because the implantations are carried out after the epitaxy, this integration scheme is called Extension Last. A drive-in annealing is then performed in order to activate dopants and to place them below the offset spacer by diffusion

(Figure 1.8.g). NiPtSi salicidation process is performed in order to lower the contact resistance (Figure 1.8.h). Depending on the application, several metal levels can be built in order to connect the transistors with each other and to create the electrical circuits (Figure 1.8.i).

In order to manufacture low-temperature transistor, the drive-in annealing at 1050 °C should thus be suppressed. The first consequence is that no dopant will be placed under the offset spacer, which will hence degrade the access resistances. Also, the dopant activation at 500 °C will lead to a low level activation, which will increase the access resistance. Different integration schemes are therefore proposed in order to form the junctions, which will be investigated during this thesis.

1.3.3 Gate First/Gate Last and Xlast/Xfirst integration schemes

In the previous process flow, the implantations have been performed after the epitaxy. Without the annealing, no diffusion should occur, which results in a degradation of the access resistance. Implantation condition might be tuned to place dopant below the offset spacer. But a higher dose and energy might lead to place dopant below the gate. Besides, the junction shape depends on the epitaxy thickness and shape variation. To overcome these issues, implantations might be performed before the epitaxy, and such an integration scheme is called Extension First. This will allow to dope under the offset spacer. However, when the gate is deposited and patterned before the junction formation, an offset spacer is still compulsory to avoid a gate stack degradation. For low temperature fabrication, the junction might still be misaligned with the gate stack. An additional solution is thus to deposit the gate stack after the S&D formation. For low-temperature fabrication, this might enable a better junction alignment, but at a higher device cost. The main differences in the process between the Gate Last/Gate First and Extension Last/Extension First integration schemes are summarized in Figure 1.9.

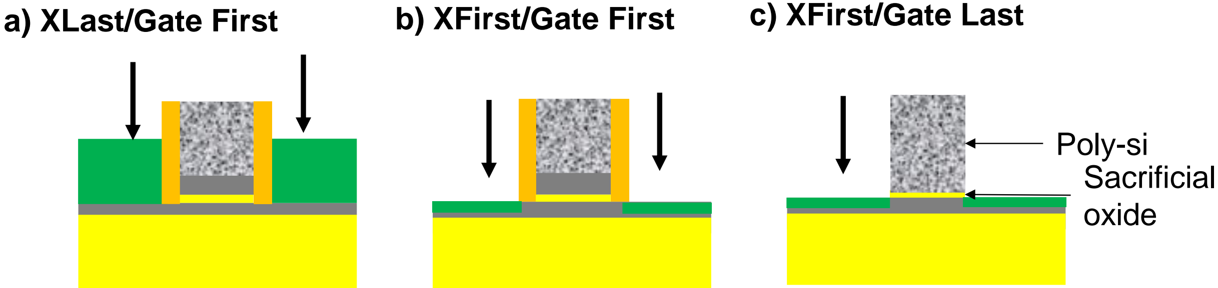


Figure 1.9: Main differences between Gate First/Gate Last and Extension First/Extension Last integration scheme

Through these process flows, it can be concluded that a Gate Last/Extension First integration scheme would result in an increase of both the device performance and the device cost due to additional steps, in comparison to a Gate First/Extension Last one. In this thesis, three integrations will be investigated, and summarized in Figure 1.10, which illustrates the transistor performance versus the transistor cost according to the considered integration schemes.

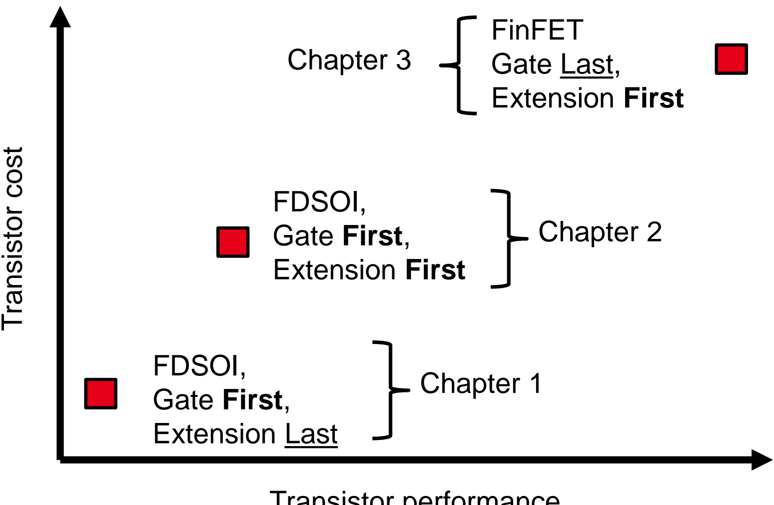


Figure 1.10: Transistor performance versus transistor cost according to the considered integrations schemes and the architectures used in this thesis

1.4 GOAL OF THIS WORK

The aim of this thesis is to manufacture and to characterize transistors with low-temperature dopant activation, in order to reach the same performance as devices manufactured with standard thermal budget. The work is organized around the SPER process, which will be described in details in chapter 2. This work is hence divided in three chapters, according to each considered integration scheme and architecture used.

In a previous thesis [9], low-temperature FDSOI devices with a 600 °C and 500 °C-activation anneal had been fabricated according to the Gate First/Extension Last integration schemes. In chapter 2 we will focus on the development of a new and stable 500 °C SPER activation process for both N and P FETs, assisted by relevant simulations and electrical characterizations.

The Extension First integration scheme has also been proposed in the former study to optimize low-temperature device. In chapter 3, different solutions will be given and evidenced by morphological results in order to optimize such an integration for the 3D sequential integration.

Finally, in chapter 4, low-temperature FinFETs with Gate Last/Extension First integration will be manufactured and characterized in order to reach higher performances.

2. LOW-TEMPERATURE EXTENSION-LAST FDSOI INTEGRATION

In order to achieve 3D sequential integration with metal lines between two stacked tiers, the thermal budget of the top transistor has to be reduced down to 500 °C [10]. The main challenge in the thermal budget reduction deals with thermal dopant activation, which is usually obtained by thermal activation at temperatures around 1050 °C. To decrease the thermal budget, SPER, which consists in activating dopants by recrystallizing an amorphous layer, can be used as it enables high dopant activation at temperatures below 600 °C. Here we focus on the development of a 500 °C SPER activation process for both N and P FETs. Extension-Last-integration devices activated with SPER at 500 °C or 600 °C and with High Temperature (HT) anneal at 1050 °C were previously fabricated [11]. In this chapter, through performance and simulation analysis, it will be at first demonstrated that it is possible to recrystallize at 500 °C, enabling high I_{on} value. A solution will be secondly proposed to reduce short channel effects, allowing a further increase of the I_{on}/I_{off} ratio.

Contents

2. Low-Temperature Extension-Last FDSOI integration 15

2.1 Background 16

2.1.1 Control of the amorphization thickness 20

2.1.2 SPER rate dependency 21

2.1.3 EOR-defects influence on electrical performance 27

2.2 Analysis on Extension Last integration 34

2.2.1 Review of previous electrical results 34

2.2.2 R_{access} improvement 38

2.2.3 DIBL optimization 52

2.1 BACKGROUND

This section will introduce several key concepts that will be used throughout this work. At first, and in order to manufacture low temperature device, dopants have to be activated with a small thermal budget. Solid Phase Epitaxy Regrowth (SPER) process has been proposed as a good candidate to suppress the standard thermal activation. To efficiently use this process, several parameters, such as the minimal crystalline seed or the maximum dopant concentration, should be taken into account. The importance of controlling the amorphized thickness will be also underlined. The End-Of-Range defects formation will be also explained and their impacts on the device electrical characteristics will be described. The SPER-rate dependencies will finally be studied.

IMPLANTATION DEFECTS

Dopants are usually incorporated into the crystalline lattice via beam line implantation. When an implanted ion knocks on the lattice, several configurations are possible on the place of this impurity with respect to the silicon atoms, as shown in Figure 2.1.

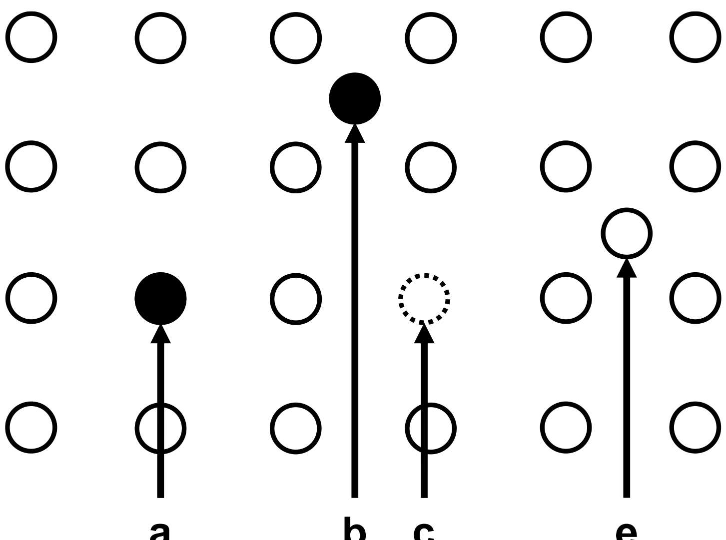


Figure 2.1: Ion implantation and consequences on lattice crystal

In the first configuration (a), implanted specie (black circle) replace a silicon atom (white circle) in a substitutional site. Thanks to this substitution, the supplementary charge carrier (hole or electron) of each doping atom can participate in the operation of the MOSFET. The doping atom is hence considered as electrically active. In the second configuration (b), the doping atom is in the interstitial site, and is thus electrically inactive. Finally, due to the impact of the implanted specie on the crystalline lattice, some silicon atoms might be displaced into interstitial site (e), forming a vacancy (hollow circle) (c). Besides, contaminant impurities like oxygen or nitrogen, can also take the place of doping ones, leading thus to non-activated dopants.

SPER PROCESS

To replace thermal activation for low-temperature devices, Solid Phase Epitaxy Regrowth (SPER) process is proposed and might be view as one of the key technological modules to achieve high performance with the 3D sequential integration [11]. It is a solid-solid transition between the amorphous and crystalline phases of the semiconductor material, as shown in Figure 2.2.

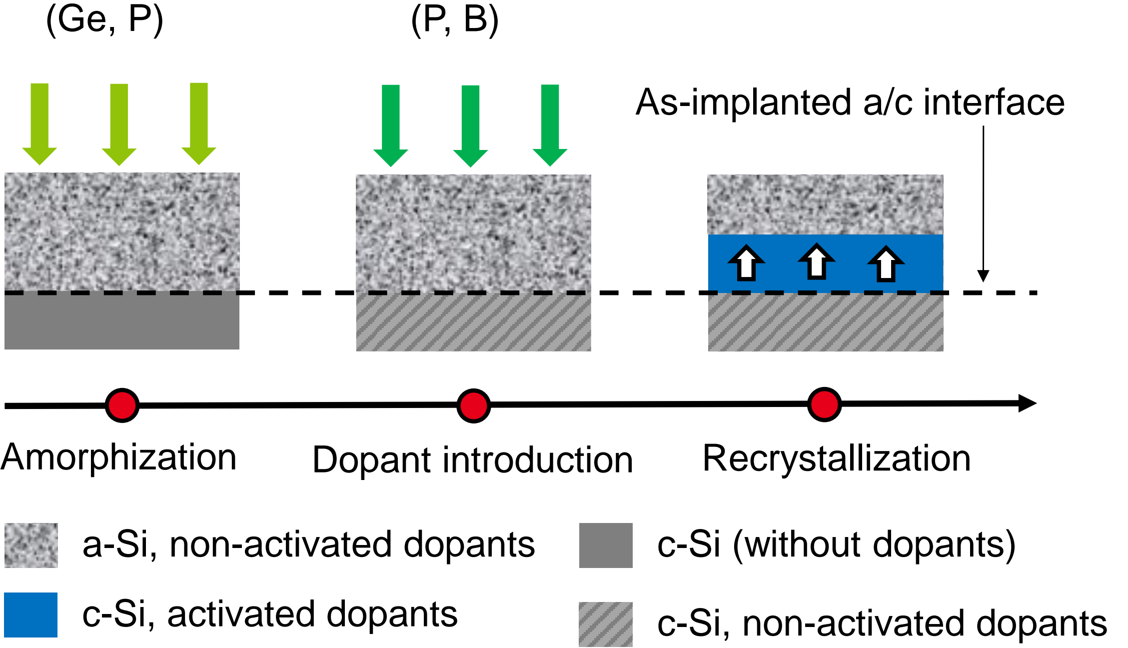


Figure 2.2: Illustration of the SPER process

Starting from a crystalline template, implantations are performed in order to amorphize a chosen quantity of this crystalline layer. The recrystallization is then carried out thanks to a small thermal annealing, which might be performed below 600 °C. The silicon layers remaining crystalline after the implantation acts thus as a seed to recrystallize the amorphized layer. The recrystallization hence starts from the amorphous/crystalline interface.

The amorphization of the layer is caused by the impact of the implanted ions with lattice atoms. It can be done either by the doping specie (if implantation conditions and the specie itself allow to damage the crystal lattice), or by a neutral specie, like germanium for example. In addition, only dopant located into the previously amorphous layers might be efficiently activated ($>1\times10^{20}$ at/cm^3) if the thermal budget is in the 600 °C range and below. Indeed, dopants can go into substitutional sites during the recrystallization process, as evidenced by L. Pasini in [9]. A TEM cross section picture of an as-implanted, boron-doped and 7 nm-thick SiGeOI with a 3 nm-thick SiN capping is shown in Figure 2.3.a), which are extracted from this study. After a 600 °C/2 min annealing, the doping concentration has been extracted by Electrochemical Capacitance-Voltage (ECV) techniques, to measure the active boron concentration profiles [12]. In Figure 2.3.b) is plotted the resulting doping concentration as a function of the depth, which is also compared with the chemical one obtained by KMC simulation.

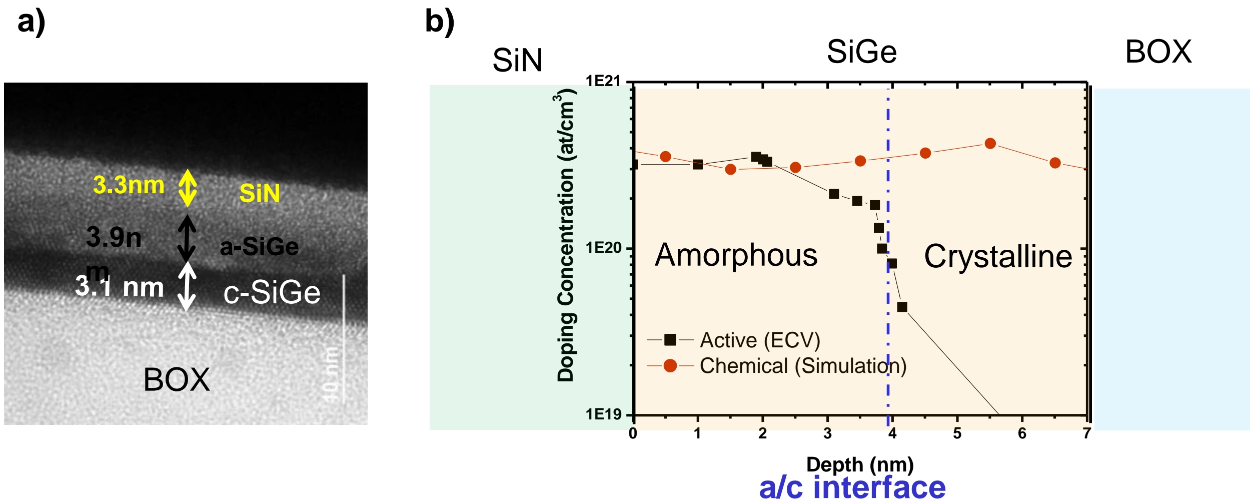


Figure 2.3: TEM cross section picture of an as-implanted boron-doped sample and the electrical doping concentration measured by ECV, after a SPER activation at 600 °C/2 min (from [9]).

It has been observed that below the former amorphous/crystalline interface, the electrical dopant concentration quickly drops and only 2 nm of the non-amorphized area was activated beyond 1×10^{19} at/cm^3.

Besides, recrystallization might also occur via Random Nucleation and Growth (RNG), which consists in a random nucleation into the amorphous region, forming recrystallized pocket. This cluster might expand into crystallite, resulting to polycrystalline-silicon formation. This is an undesired result for our study, as doped polycrystalline silicon is more resistive than doped single-crystal one, and will thus lead to lower MOSFET performances. This mechanism usually occurs after the SPER process, due to its high activation energy [15].

MAXIMUM ACTIVE CONCENTRATION

At the thermodynamic equilibrium, the maximum dopant before the creation of a different phase is called solid solubility limit. Activating dopants via the SPER process enables however to reach higher activation levels, because this process occurs out-of-equilibrium [13], [14]. The maximum dopant concentration that should not be exceeded for the SPER process has been fixed using the clustering limit, which represents the concentration before the formation of inactive cluster, which will also deactivate dopant and reduce the carrier mobility [9]. The clustering limit for phosphorous (respectively boron) is estimated at 6×10^{20} at/cm^3 in [9] (respectively 3×10^{20} at/cm^3 in [15]) at 600 °C.

MINIMAL CRYSTALLINE SEED

In order to use the SPER process, a minimal crystalline-seed thickness is mandatory, which depends on the implanted specie, as well as the dose and energy used during implantation. It has been estimated by KMC simulation in [16] that a 3 nm-thick seed is at least required for Phosphorous implantation at 1 keV. It has been calculated by ellipsometry measurements in [17] that, according to the implantation dose, between 3 nm and 5 nm of the crystalline seed thickness is mandatory for Arsenic implantation at 1 keV. For the future electrical simulations, 3 nm has been chosen to be the minimal targeted thickness in our study, regardless of the specie, the dose and the energy used.

2.1.1 Control of the amorphization thickness

As the dopant activation is efficient only in the amorphized layer, its thickness control is of utmost importance. It can be estimated *a priori* by process simulations or *a posteriori* by TEM observations. In this work, to form this amorphous layer, the initially crystalline silicon is damaged by beam line implantations. Thereby, the depth of this layer is linked to the implanted species, the energies, the concentrations [18], [19], as well as the temperature during implantation, and the tilt [20]. The dose rate is usually not mentioned in publications, possibly due to its dependency with the implantation tools and energy used. The amorphous thickness is however strongly dependent of these parameters, especially for thin amorphous layers.

The implantation current I (A) is linearly linked to the dose rate D (at/cm^2/s) by $D = \frac{(I/q)\times t}{S}$, where q is the electron charge, t is the implantation duration and S is the ion beam scanning area. The implantation current – or the dose rate – also depends on the considered specie. For example, in LETI and for low energy (less than 20 keV), the current might be tuned at 500 µA for Ge implantation, and at 5 mA for P and B implantation.

An example of the amorphous layer thickness modification as a function of the dose rate is given by KMC simulation in Figure 2.4. The different dose rates correspond to the two different tools used in this work, Tool#1 and Tool#2, which are typical values for low-energy implantations (< 20 keV). Here, the active zone is 24 nm-thick, with a 7 nm-thick Si channel.

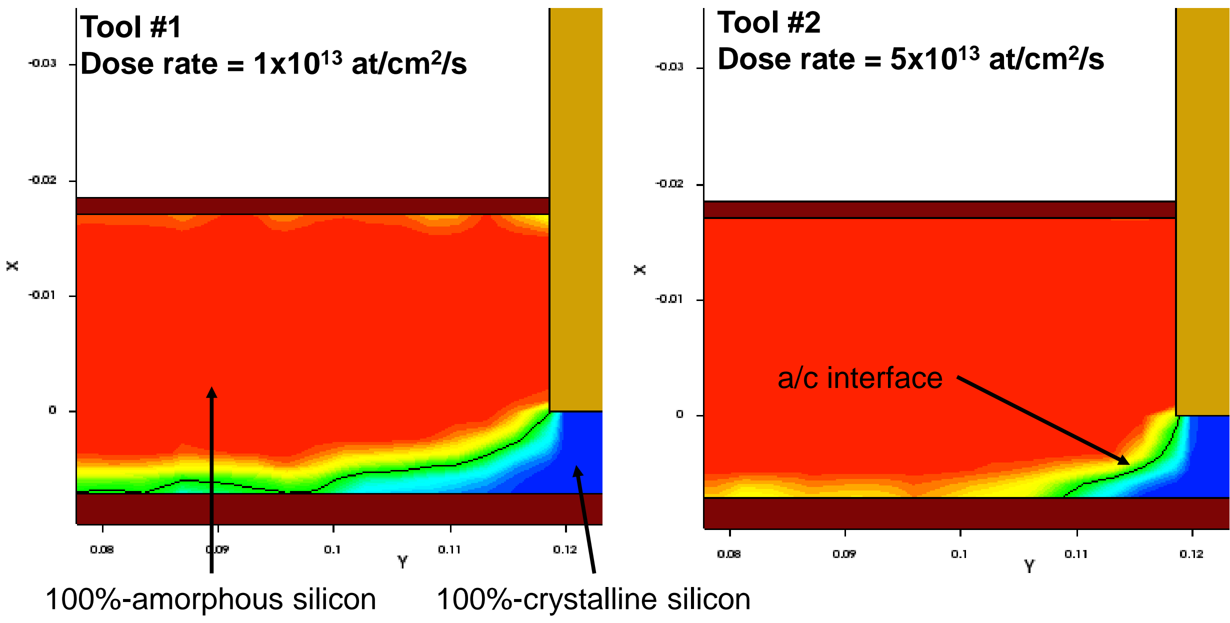


Figure 2.4: KMC simulations of the amorphous thickness as a function of the dose rate

It can be seen in Figure 2.4.a) that the amorphous/crystalline (a/c) interface leaves a horizontal seed, while in Figure 2.4.b), the seed can only come from the channel. With this simple observation, crystalline regrowth mechanisms between this two configurations will not follow the same crystalline orientation and might thus be very different.

2.1.2 SPER rate dependency

In the previous work [16], it has been demonstrated that with a 600 °C/2 min activation, high performance is achievable for low-temperature devices. In this work, we will investigated if such performances are achievable with an even lower annealing (500 °C). A first estimation of the annealing time will be given with such a temperature. If the recrystallization annealing is indeed higher than one hour, SPER cannot be considered as a viable option in an industrial-oriented point of view. To estimate the annealing duration, the SPER rate, which is the velocity of the recrystallization, will be evaluated for our devices. It depends on various parameters, such as the temperature [22], the crystalline orientation, the impurities concentration [23]–[25], the mechanical

pressure [26], [27] or the strain [28], [29]. In this section, a brief review of the SPER rate dependence with the temperature, the crystalline orientation and dopants concentration as well as other impurity concentration such as nitrogen or oxygen, will be presented, by considering these parameters as the most important ones.

CRYSTALLINE ORIENTATION DEPENDENCY

A structure is defined as crystalline when atoms are arranged periodically. According to the phenomenological model developed in [30], a free atom becomes crystalline when it forms at least two undistorted bond to already-crystalline atoms. This recrystallization mechanism depends on the crystalline plane used as a seed. The three main ones (the other being equivalent) are shown in Figure 2.5. The recrystallization mechanism according to the crystalline plane is also added.

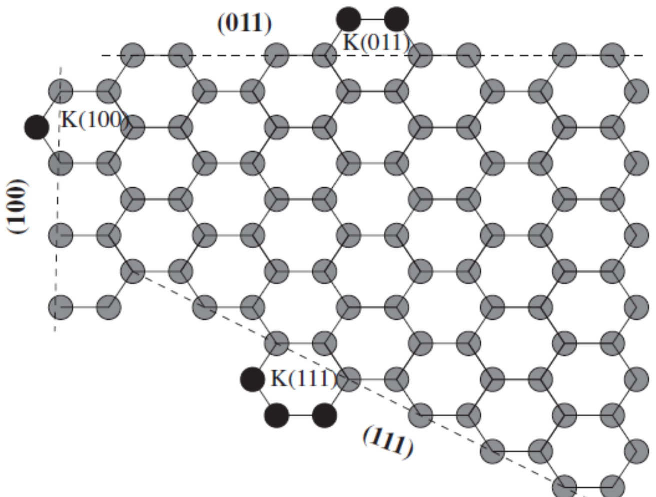


Figure 2.5: Atomistic configurations for (100), (011) and (111) crystalline plane, from [18]

The dependency is hence due to the compulsory number of atoms to form the crystalline structure. In the (100) crystalline plane, one atom of the amorphized layer is enough to form two undistorted bond with the crystalline structure, while for the (110) crystalline orientation, two atoms have to be involved to form a cluster. In this configuration each atom will be able to form 2 undistorted bond with the crystalline layer. Because of this necessary clusterization, the regrowth will be slower than for the (100) case. For the (111), a 3-atom cluster is mandatory. The

recrystallization velocity is thus highly anisotropic and varies within a range of 20:10:1 for the (100), (110), and (111) crystalline plane, respectively [30].

In addition, the <111> crystalline plane presents another specificity. During a recrystallization which follows this orientation, the atoms can be arranged by following the crystalline structure, or by mirroring this one. The second atomistic arrangement is called twinning effect. The intersection between a 'normal' crystalline structure and a 'twin' one will lead to the apparition of stacking faults. The difference between 'normal' and 'twin' configuration is shown in Figure 2.6, as well as a TEM cross section picture showing such defects. At this stage, it is unknown if these twin defects will lead to a resistivity degradation [15].

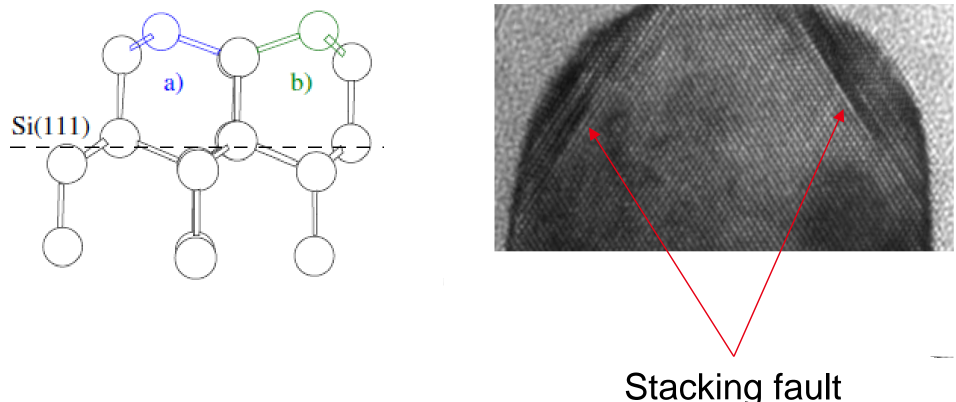
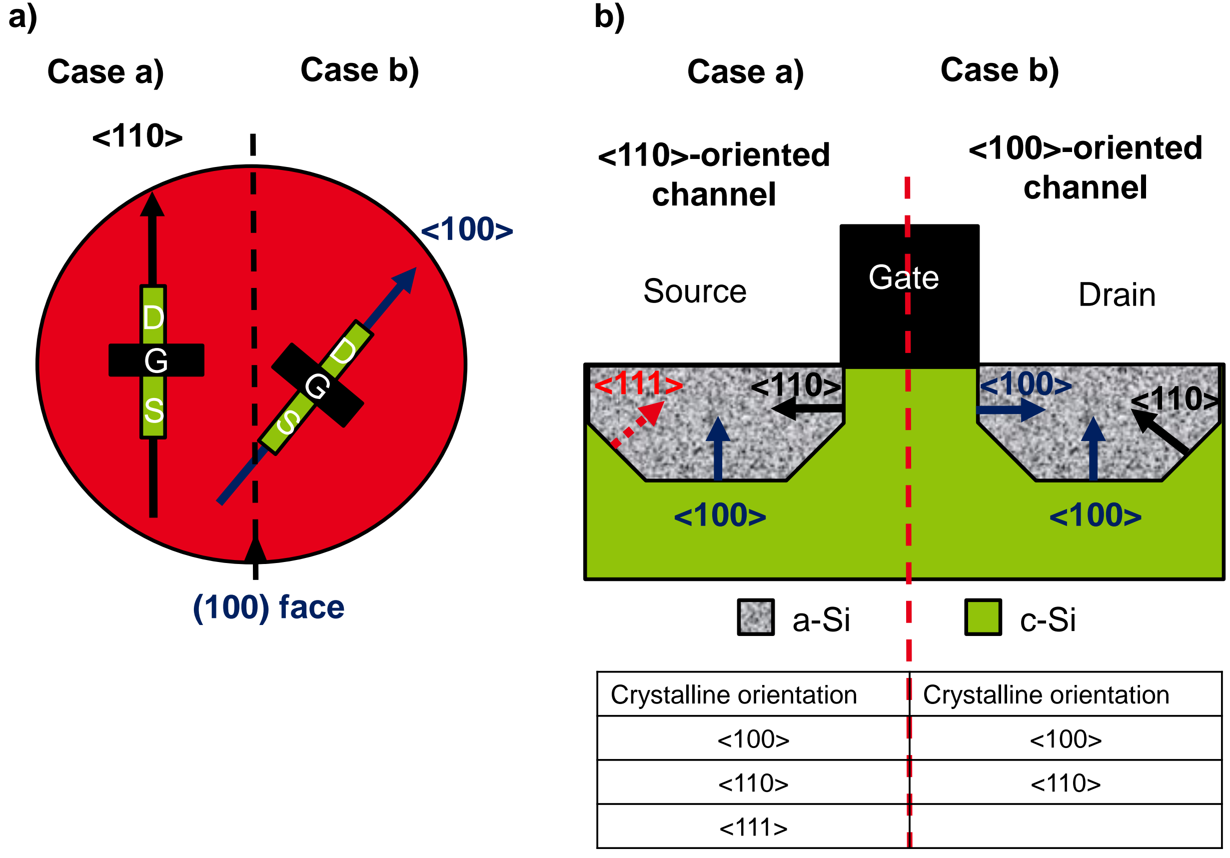


Figure 2.6: Schematic representation of normal and twin configuration from [31], and TEM cross section picture evidencing stacking fault

The crystalline orientation(s) that will be involved during recrystallization process depends on the wafer and device manufacturing. Usually, the top surface of wafers follows the (100) crystalline surface orientation. Device channels are patterned in order to have a current flow along the <110> or the <100> crystalline orientation. <110> is generally the standard one used in microelectronic. Analyzed devices in this chapter have however a <100> channel orientation. Figure 2.7.a) represents the top view of a wafer with a (100) surface orientation with a notch oriented according to the <110> crystalline orientation. The active zone (AZ) and the gate of two

devices are illustrated, one with a <110>-oriented channel (case a)), the second with a <100>-oriented one (case b)). A cross section of such devices is reported in Figure 2.7.b), with an example of amorphized areas, where the three crystalline orientations are represented.



Crystalline orientation	Crystalline orientation
<100>	<100>
<110>	<110>
<111>	

Figure 2.7: Schematic illustration of crystalline orientations for <110> and <100> -oriented channel

For both cases, the regrowth will hence be multidirectional, leading to complex recrystallization mechanism. While in the first configuration (case a)), the three crystalline planes might be involved, with suspected stacking fault formation due to the (111) crystalline plane, for the second configuration, no (111) crystalline planes should be involved during the SPER process. These hypothesis have been confirmed experimentally and by simulation in [15] and [9]. As a conclusion, the recrystallization mechanism highly depends on the wafer and device orientations, and on the amorphous layer shape.

TEMPERATURE DEPENDENCY

The SPER rate increases exponentially with the annealing temperature, following an Arrhenius-type behavior $v = v_0 \times \exp(-{E_a}/{k_b T})$, where v is the SPER rate, E_a the activation energy, k_b Boltzmann's constant, and T the temperature. It had been evidenced that the prefactor v_0 is temperature-independent but crystalline-orientation dependent [15]. Therefore, it is worth noticing that the crystalline orientation and the temperature influence the SPER rate independently.

DEPENDENCY WITH IMPURITIES

It had been previously described that doping concentration should not exceed a critical concentration to avoid clustering effect. In addition to this phenomenon, it has also been demonstrated by experience and by simulation that doping species, such as P or B, enhance the regrowth velocity until a critical doping concentration C_c, which is temperature-dependent [9], [13], [22], [24], [32]. This critical concentration might be view as the best trade-off between clustering effect (which slows down the SPER rate) and dopant effect (which speeds it up).

In [24], it had been demonstrated that doping species (P, As, B) with concentration up to 3×10^{20} at/cm^3 enhance the SPER rate in the 460–660 °C range, which has also been confirmed in the previous study [9]. It can be summarized that for phosphorous and boron species, for our temperatures of interest (450 °C-600 °C) and for doping concentration up to 8×10^{20} at/cm^3, the SPER rate will increase: doping specie will be assumed to not degrade this velocity.

In addition, the presence of non–dopant impurities, such as nitrogen or oxygen, has been reported to delay the SPER rate [23], [33]–[35], which opposes the impact of the doping impurities. As mentioned by P. Rudolph in [33], this suggest that “[…] the SPER rate is sensitive to shifts in the Fermi level” in the semiconductor material. In [15], it had been supposed that neutral impurities lower the free-energy and thereby slower the SPER rate.

CONCLUSION ON THE SPER RATE

As a conclusion, the SPER rate dependency with the temperature, the crystalline orientation and the doping specie is shown in Figure 2.8. These results are extracted from Drosd et al. in [30] and Johnson et al. in [24].

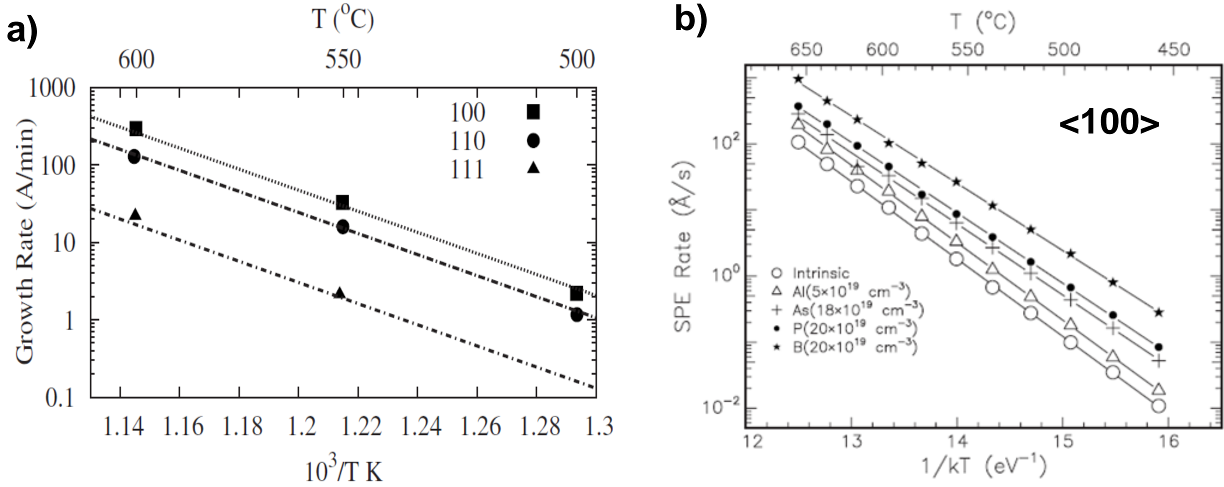


Figure 2.8: SPER rate as a function of the temperature and the crystalline orientation [30], and the temperature and doping specie for the <100> crystalline orientation [24]

To our knowledge, no studies have been conducted that take into account all these three parameters, simultaneously. It had thus been chosen to apply the ratio of [30] on the SPER rates in [24], in order to give at first an estimation of the SPER rate according to these three parameters, which are reported in Table 1.

Deduced values		SPER rate (nm/min) for dopant		
Annealing	Crystalline Orientation	Intrinsic	P @ 2^e20 at/cm³	B @ 2^e20 at/cm³
600°C	<100>	≈ 30	x10 ≈ 300	x3 ≈ 900
	<110>	≈ 15	≈ 150	≈ 450
	<111>	≈ 1.5	≈ 15	≈ 45
500°C	<100>	≈ 0.2	x20 ≈ 4	x3 ≈ 12
	<110>	≈ 0.1	≈ 2	≈ 6
	<111>	≈ 0.01	≈ 0.2	≈ 0.6

Table 1: First-order extrapolation of the SPER rate (nm/min) as function of temperature, dopant concentration and crystalline orientation

By taking into account these three parameters, an estimation of the SPER rate is hence possible. For example, the SPER rate for nMOS devices with P implantation at 500 °C following the <110> crystalline orientation is estimated at 2 nm/min, while for pMOS devices with B implantation, the SPER rate is estimated at 6 nm/min. Therefore, recrystallizing 30 nm with such conditions will required an annealing duration of 15 min (respectively 5 min) for phosphorus (respectively boron) implants. The deduced values in Table 1 will be used in this way in section 2.2.2.

However, these data come from full-sheet experiments and measurements. The recrystallization mechanism involved is therefore one-dimensional. In patterned devices, amorphous/crystalline interfaces are however curved and two or three of the crystalline orientations might be involved during the recrystallization process. A more complex mechanism might be involved, which could result in supplementary differences between the SPER rate values.

2.1.3 EOR-defects influence on electrical performance

When an amorphizing implantation is carried out on a silicon substrate, the crystalline lattice is damaged. In other words, a certain amount of substitutional silicon atoms are displaced into interstitial sites, resulting in a production of vacancies and interstitials. At the as-implanted amorphous/crystalline interface, the amount of interstitial silicon Si_i have been found to exceed the amount of the vacancy [36]. During the recrystallization process, the interstitial supersaturation agglomerates into larger extended defects, which are located just below the former a/c interface, in the "end of range" region of the amorphizing implantation. These defects are called End Of Range (EOR) defects. This phenomenon is illustrated in Figure 2.9.

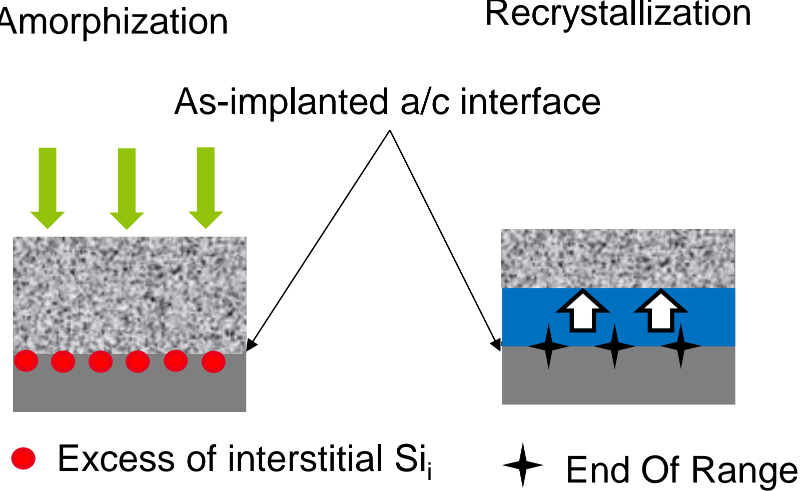


Figure 2.9: Illustration of the EOR defects formation

These defects can have detrimental effects on the device performances. Three major degradations might indeed occur due to these defects according to the interaction with dopants, as studied in [37]. As illustrated in the case of boron junction in Figure 2.10, the defects can alter the junction shape (Figure 2.10.a)), the junction activation level (Figure 2.10.b)) and the junction leakage (Figure 2.10.c)).

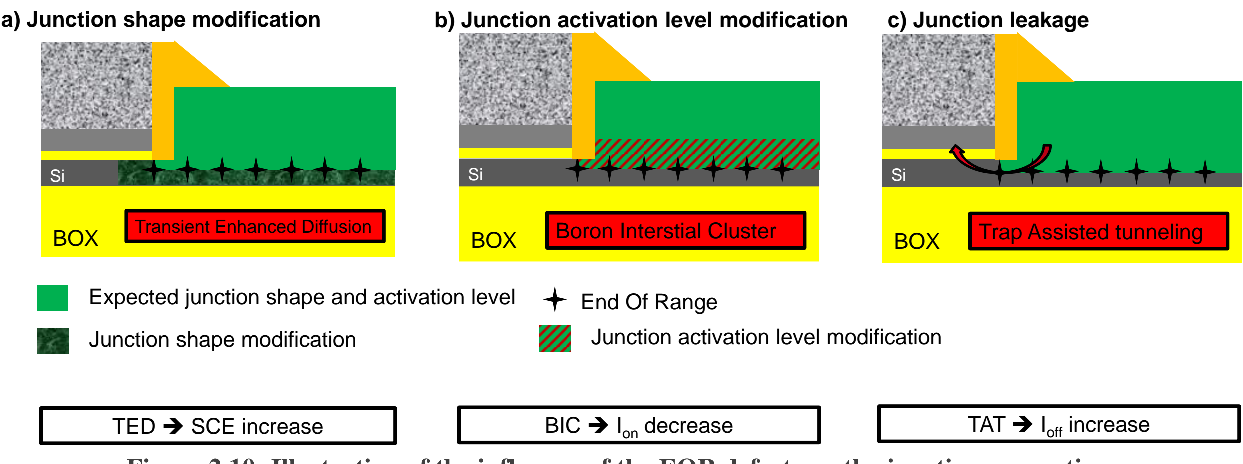


Figure 2.10: Illustration of the influence of the EOR defects on the junction properties

Figure 2.10.a) illustrates that the junction is closer to the gate than expected, and electrical parameters such as the DIBL and the SS might thus increase. This 'anomalous' diffusion is called the Transient-Enhanced Diffusion (TED), and can occur, even at low temperature. This phenomenon is due to the formation of a highly mobile pairs from Si_i and B_s that enhances boron diffusion [36]. Boron should indeed migrate less than 1 nm with a thermal budget of 600 °C/10 s [38]. It has however been observed in [39] that, for this thermal budget and with a pre-amorphization performed by germanium implantation, boron atoms have migrated up to 24 nm, which has been attributed to the excess of interstitial silicon induced by ion implantations. Thereby, this migration especially depends on the concentration of the interstitial silicon [36].

In Figure 2.10.b) is sketched that, close to the former amorphous/crystalline interface, Boron-Interstitial Clusters (BICs) are formed. Here, Si_i ejects boron atoms from substitutional site B_s to interstitial one B_i. Boron atoms are thus electrically inactive, resulting in an access resistance degradation, and thus to a decreased I_{on}.

In addition, BIC and TED can also influence each other: while BIC might be viewed as a reservoir of interstitials, which can contribute to the TED effect (DIBL degradation), the TED can lead to a boron clusterization due to an excessive concentration of boron at a specific location (R_{on} degradation) [38].

In Figure 2.10.c), the EOR defects are shown to induce higher junction leakage through the Trap Assisted Tunneling (TAT). This could lead, for example, to an I_{off} increase [37], [40], due to the increase of the minimum drain current value (due to the Gate Induced Drain Leakage (GIDL), or the strong Shockley-Read-Hall (SRH) leakage in the junction).

The expected degradations on the I_d-V_g curves due to these effects are summarized in Figure 2.11.

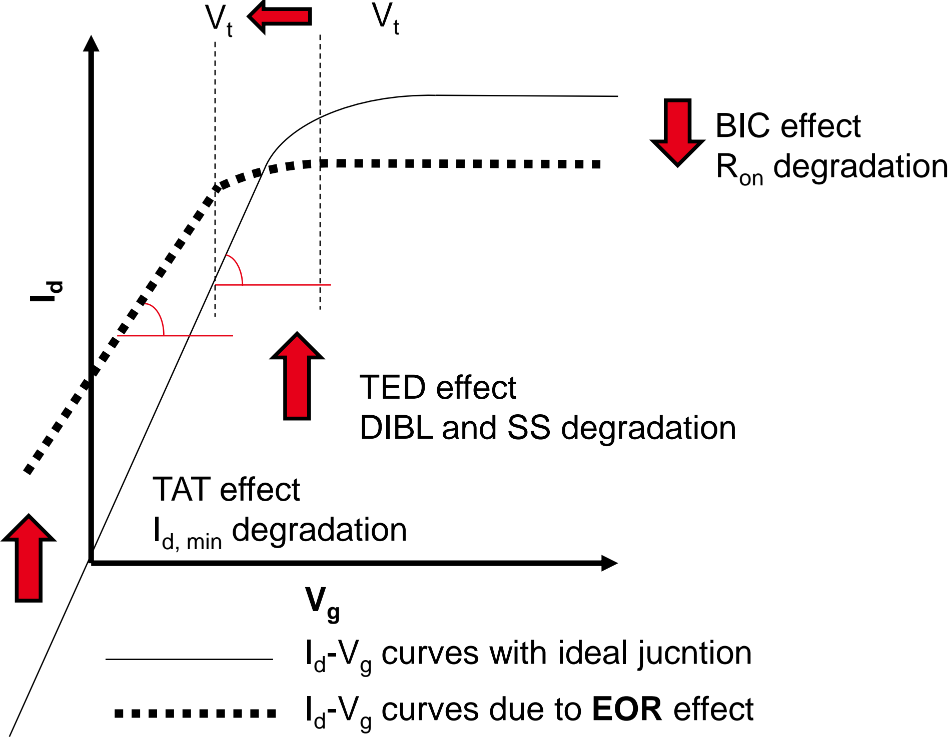


Figure 2.11: Summary of the expected degradation on I_d-V_g curves due to EOR effects

These effects are only observed for devices fabricated at low temperature, as high temperatures are known to generally dissolve the EOR defects [41]. When a high temperature process is indeed involved, such as a Rapid Thermal Annealing (RTA) at 1000 °C during 10 s, such defects are not observed. However, with a furnace annealing with temperature between 700 °C and 900 °C, a sheet resistance degradation has been observed, interpreted in [41], [42], as a boron deactivation.

DISSOLUTION DEFECT BY SOI

It has been demonstrated in [37],[43], that, by using a SOI wafer with thin thickness, the EOR concentration can be minimized, even at low temperature. Figure 2.12 summarizes the main result from [37]. In Figure 2.12.a) is sketched the influence of the SOI to cut-off the Si_i concentration, while in Figure 2.12.b) defects are sunk into the BOX.

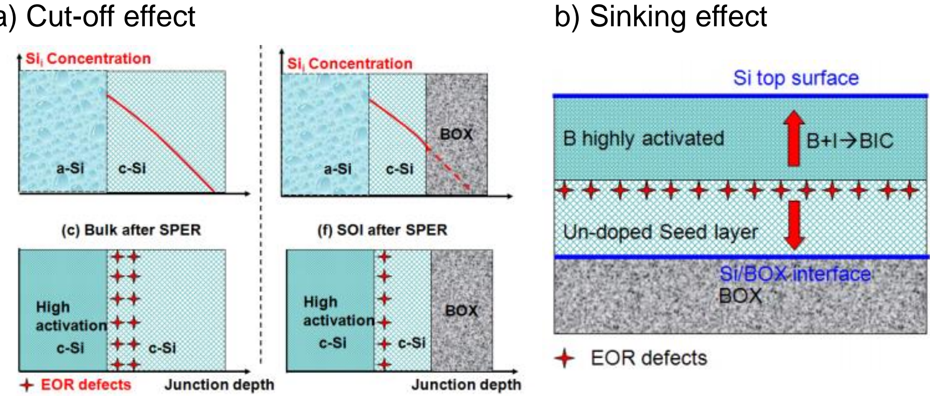
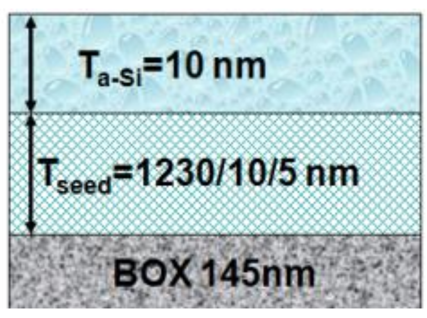


Figure 2.12: Illustration of the cut-off and sinking effect, from [37]

Compared to bulk sample, the BOX of the SOI one can cut off the Si_i profile. The consequent reduction leads to a more-stable electrical activation and less-enhanced diffusion.

Besides, the Si_i tends to move toward free surfaces. While on bulk sample, the Si top surface acts as the only defect sink, on SOI samples, the BOX can act as an additional one. By locating the EOR as close as possible from the BOX, the Si_i flux flowing to the Si/BOX interface can be increased.

The optimized position has been experimentally investigated in [37]. For the same amorphizing implantation, three different samples have been used, with a channel thickness equal to 1240 nm, 20 nm and 15 nm, as shown in Figure 2.13.a). This leads to place the EOR defects at different location with respect to the BOX. The resulting sheet resistance measurements after a recrystallization process performed at 500 °C is shown in Figure 2.13.b). The annealing duration has been varied from 2 min to 10h.



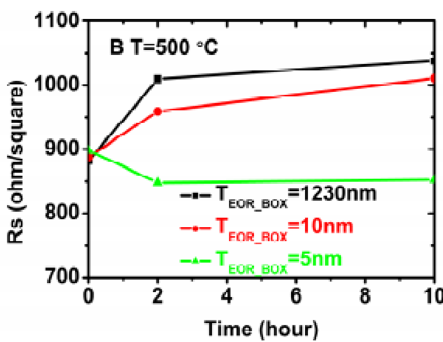


Figure 2.13: Sheet resistance measurements as a function of the annealing duration, with different location of the EOR, from [37]

An increase of the sheet resistance has been observed during the first 2 hours of the post anneal when the EOR defects are located relatively far from the BOX (T_{EOR_BOX} =1230 nm and 10 nm). When EOR defects are 5 nm close to the BOX, a decrease of the sheet resistance is observed, confirming the EOR defect density reduction. In our case, the annealing duration has been set below 1h for industrial interest. Even if in the previous study no sample has been measured after a 30 min annealing, the trend will be assumed to be the same. The amorphous/crystalline interface must be thus located as closest as possible from the BOX.

CARBON CO-IMPLANTATION

To limit the influence of these supplementary interstitials on the boron diffusion, one option is to co-implant neutral impurities, such as nitrogen, fluorine or carbon. However, neutral impurities will delay the SPER rate [33]–[35]. The SPER Rate has been measured to be 100 time slower than expected due to the presence of fluorine [22]. In this work, a deeper investigation of the use of carbon co-implantation has been performed, as carbon has indeed the ability to capture interstitial [44] [45] and/or to slow down BICs dissolution [46]. In this process, two carbon atoms have to be involved in order to capture one interstitial silicon atom [44], [47]. The interstitial profile created by the germanium and boron implantation conditions need thus to be estimated in order to choose the accurate carbon one.

Besides, a boron deactivation due to the interaction between boron and carbon atoms had been evidenced in [48], [49]. This deactivation has been shown to be dependent of the annealing temperature as well as the boron and carbon concentration. This might be viewed as a competition

for carbon atoms to either capture Si_i, to interact with Si_i-B_v complexes, or to form a pair with B_s. It has been concluded that carbon concentration should thus be at least ten times superior to the boron one to avoid electrical deactivations, for annealing in the range of 450 °C up to 750 °C.

It has been found in addition in [50], [51], [52] that carbon atoms might migrate even at low temperature. It had thus been concluded that a pre amorphized layer is essential to retrain the high carbon concentration in the desired region.

As a conclusion, to effectively limit the TED effect, carbon atoms should be located in the Si_i-rich area, with a concentration at least twice higher than the excess interstitial. To avoid boron deactivation, carbon concentration should at least be ten time above the boron one. Amorphized areas, in addition, avoid carbon migration. Figure 2.14 illustrates the recommendation for carbon implantation to limit the TED effect and the BIC formation.

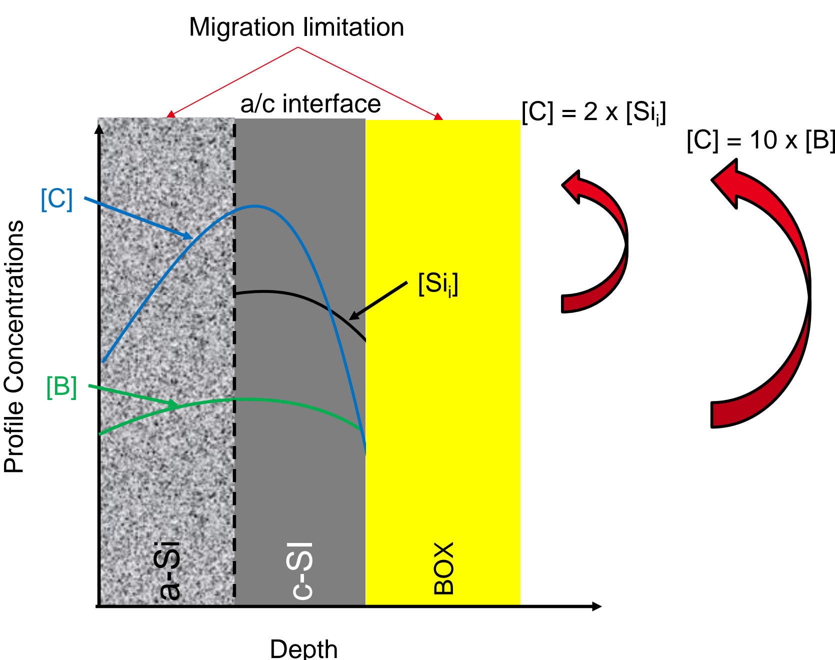


Figure 2.14: Recommendation for carbon profile to limit both the TED effect and the BIC formation

In a FDSOI device with the SPER process, two areas are already in an amorphous state (the amorphous silicon and the BOX), limiting thus the carbon migration. For a boron concentration

equal to 3×10^{20} at/cm^3, it is thus advised to reach carbon concentration above 3×10^{21} at/cm^3. It is worth noticing that such concentrations might additionally influence the amorphized depth.

As a conclusion of this section, the SPER process and its dependencies has been explained, which will allow to better understand the device degradation in section 2.2

2.2 ANALYSIS ON EXTENSION LAST INTEGRATION

In this section, optimizations for Extension Last integration scheme has been based on a 28 nm FDSOI-technology lot, already studied in [9]. The device fabrication is at first explained, which is representative of a 28 nm FDSOI technology. A review of the results shown in [9] is then proposed, in order to analyze afterward device degradations.

2.2.1 Review of previous electrical results

FDSOI devices were fabricated on 7 nm-thick <100>-oriented Si channels with a 25 nm Buried Oxide, followed by HfSiON/TiN/Poly-Si gate stack. After offset spacer formation, 18 nm-thick Raised Source Drain epitaxy was carried out. Modifications between splits appears afterwards. Figure 2.15 shows the difference between the High Temperature (HT) and the Low Temperature (LT) process flow

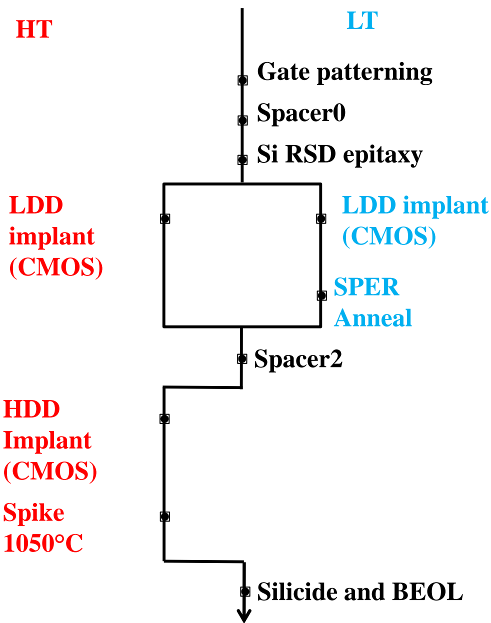


Figure 2.15: Process flow for HT and LT devices

For High Temperature devices, a Lightly Doped source/Drain (LDD) implantation have been performed after the epitaxy, followed by the second spacer formation and a Heavily Doped source/Drain (HDD) implantation. For Low Temperature devices, only one implantation was carried out, after the offset spacer formation, in order to avoid the clustering effect. In addition, while for HT devices a spike annealing was performed to activate dopants, for LT ones, in order to reduce the thermal budget, only a small annealing was carried out after the implantation to use the SPER process. It is worth noticing that after implantations, the thermal budget to manufacture devices is inferior to 500 °C. The efficient activation at 500 °C can be thus reliably evaluated. After these modifications, standard silicide and BEOL with a thermal budget inferior to 400 °C was carried out. The detail of low-temperature splits is given in Table 2.

Type	Implantation condition	Split name	Annealing
nMOS	Phosphorus only	600°C	**600°C/1min**
		500°C	**500°C/10min**
pMOS	germanium and double boron implantation	600°C	**600°C/1min**
		500°C	**500°C/10min**

Table 2: Split table details for low temperature splits

The implantations conditions for p and n MOS devices had been chosen by KMC simulations to amorphize 22 nm of the 25 nm-thick source and drain regions. High and constant doping profiles (above 1×10^{20} at/cm^3) had also been targeted. While for nFETs, one phosphorous implantation is enough to obtain such conditions, for pFETs, a pre amorphization implantation and two boron implantations are needed. In this study, splits had furthermore been defined according to two annealing temperatures for the SPER process, set at 600 °C or 500 °C. The first temperature had been chosen as well-working devices with this thermal budget had already been successfully fabricated in [9]. The second one is the targeted thermal budget for 3D sequential integration. From these conditions, it was expected to leave a horizontal seed. The recrystallization process should thus follow the <100> crystalline orientation. According to Table 1, while at 600 °C, the regrowth should be complete in less than 10 s, at 500 °C, the full recrystallization for both boron and phosphorous accesses should be complete in 5 min. The thermal budget thus appears to be adapted.

Characterized devices are 210 nm-wide, with gate lengths from 120 nm down to 30 nm, and at $V_d = 1$ V. Figure 2.16.a) shows the resulting I_{on}-I_{off} trade-off. The R_{on}-DIBL trade-off is also added in Figure 2.16.b). It has been noticed in [9] that the POR is not at the state to the art, due to a thicker spacer (12 nm instead of 8 nm).

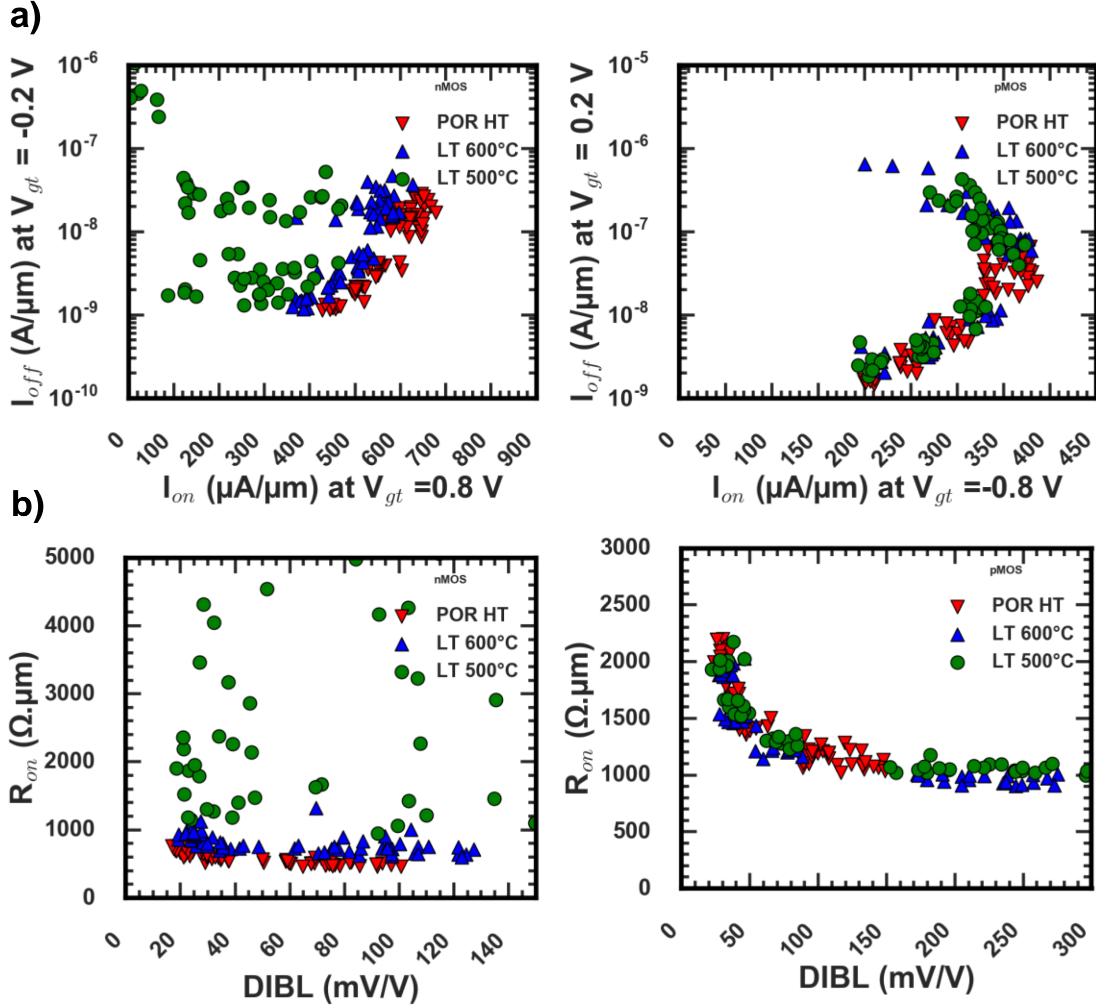


Figure 2.16: I_{on}-I_{off} and R_{on} -DIBL trade-off for p&n MOS devices.

For LT nMOS devices, while devices with a 600 °C activation exhibit performances closes to the HT POR, the 500 °C-activated ones show an I_{on} degradation without I_{off} modification. This observation is correlated with the R_{on} degradation observed in Figure 2.16.b). A deeper investigation has been made to understand this point, and is explained in the next subsection.

For LT pMOS devices, devices activated at 600 °C and 500 °C achieve performances close to the reference ones, as observed in Figure 2.16.a). This observation highlights the feasibility to achieve high performance devices with low temperature activation [11]. The LT devices with the shortest gate lengths however show an I_{off} increase with an I_{on} decrease. A DIBL degradation is

also observed in Figure 2.16.b). The understanding of such results will be described in the sub section 2.2.3.

2.2.2 R_{access} improvement

In this sub section, the origin of the I_{on} and R_{on} degradation of the low-temperature nMOS devices is investigated. It has been more specifically suspected that the R_{on} degradation is due to a higher access resistance (R_{access}) for 500 °C-activated devices in comparison to the 600 °C-activated ones. To confirm this hypothesis, I_d -V_g curves extracted at V_d = 50 mV of both splits are plotted in Figure 2.17.a), for 30 nm-long device. From these curves, a R_{access} value can be analytically extracted for both splits. By adding a supplementary 650 Ω.µm on the R_{access} value of the 600 °C-activated device, the global I_d-V_g curve shape of the 500 °C-activated one is reproduced. This supplementary access resistance is electrically schematized in Figure 2.17.b).

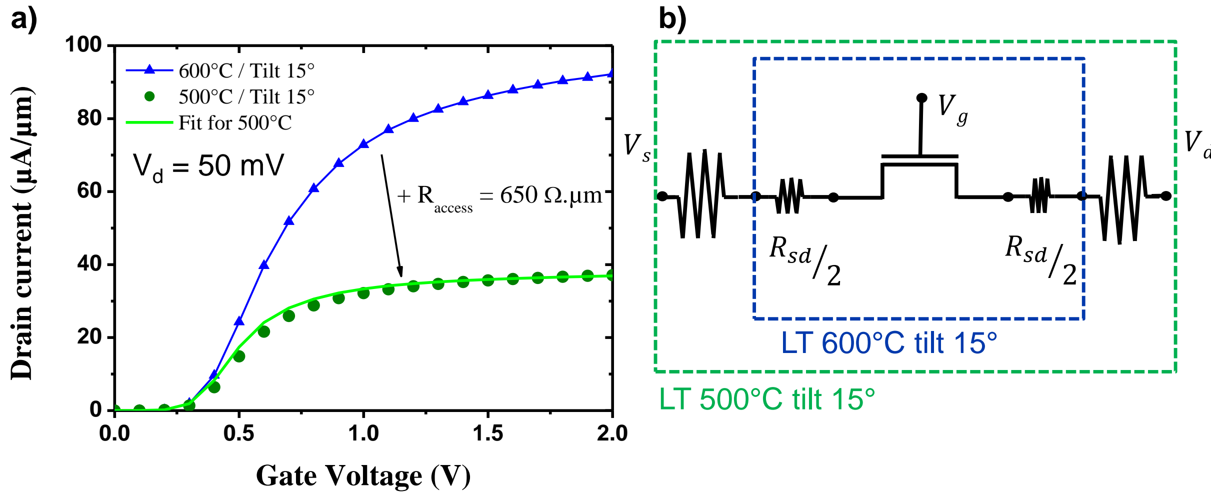


Figure 2.17: I_d-V_g and electrical schemes of 500 °C- and 600 °C- activated devices, with an analytical fitting.

This degradation for low temperature devices could be explained by a partial recrystallization. To confirm this hypothesis, a TEM cross-section picture of 34 nm-long and

210 nm-wide device with I_{on}-I_{off} value show in Figure 2.18.b) has been carried out and displayed in Figure 2.18.a).

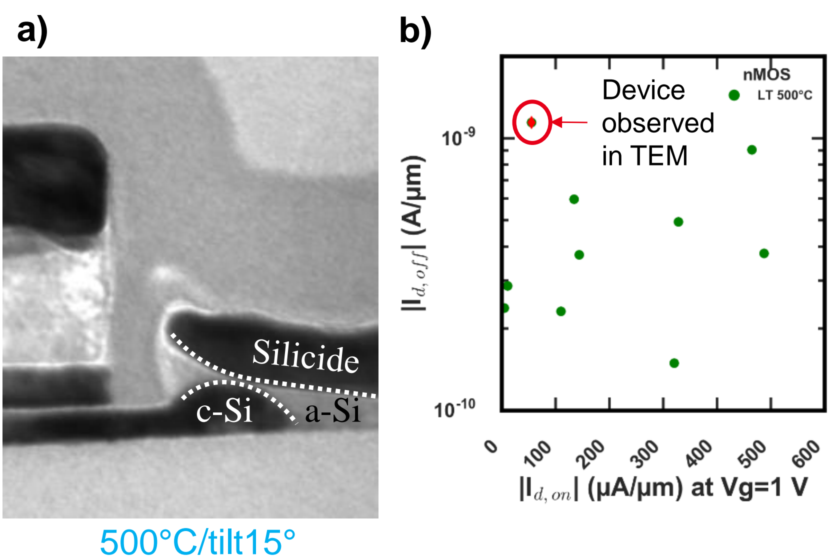


Figure 2.18: a) TEM observation of a 500 °C-activated device, b) I_{on}-I_{off} performance of the observed device

The TEM cross-section is a picture of the gate and the active zone (source or drain) of a device after the manufacturing. While the active zone was expected to be composed of crystalline silicon and silicide, amorphous silicon is clearly visible between these two elements. The very poor I_{on} value is thus explained by a partial recrystallization. The pure R_{access} degradation might indeed be attributed to the amorphous layer, highly resistive. In addition, it is worth noticing that, in the TEM picture, the recrystallized part is not in contact with the silicide, which degrades the contact resistance.

In the TEM picture, no crystalline seed for recrystallization at the bottom of the S&D areas is observed, except at the very edge of the channel. Recrystallization thus proceeds from the channel edge, which are in this case acting as a seed. This full amorphization is unexpected, because a 3 nm-thick horizontal seed has been targeted by KMC simulation in the previous study. These simulations are thus inexact and a deeper investigation has been made to identify the origin of this error.

In the previous study, electrical simulations have been performed with a dose rate equal to 1×10^{13} at/cm²/s, which is the typical value for tool #1. However, implantations have been carried out via tool#2, where the dose rate is equal to 5×10^{13} at/cm²/s. As previously seen, this dose rate modification might totally change the amorphous layer depth, leading to a different amorphous/crystalline interface shape, and thus to different recrystallization orientations, as observed in the TEM picture in Figure 2.18.a).

To validate this point, qualitative observations through KMC simulations have been performed including this time the impact of the dose rate. Figure 2.19.a) shows the amorphous/crystalline interface profile with the precise dose rate used during implantations. Figure 2.19.b) shows the time-annealing evolution of the amorphous/crystalline front at 500 °C, taking into account the SPER rates as a function of crystalline orientation and temperature, and starting with the amorphous/crystalline interface previously simulated and shown in Figure 2.19.a). The TEM cross section picture shown in Figure 2.18.a) is also added in Figure 2.19.c).

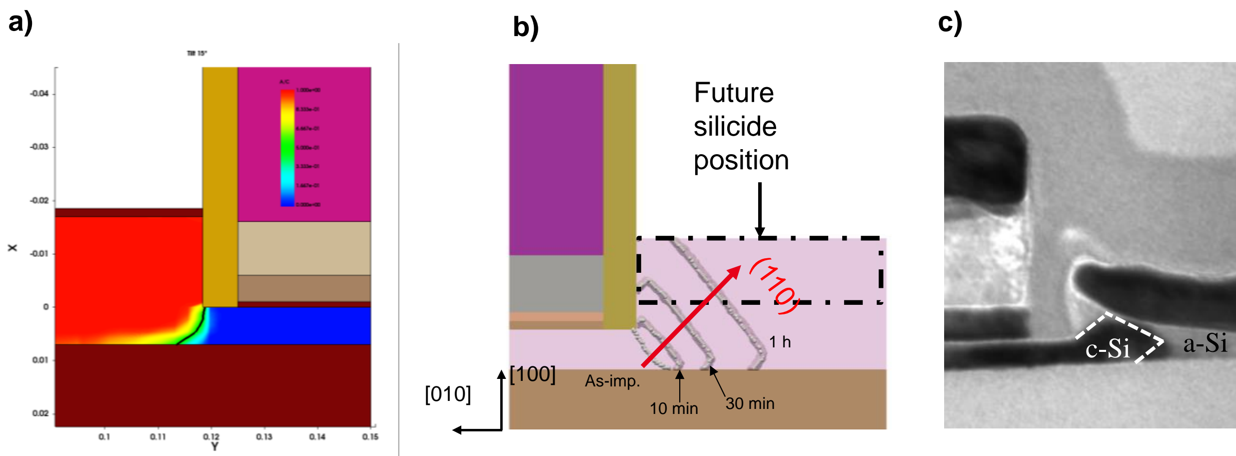


Figure 2.19: Electrical simulation by taking into account the precise dose rate of the amorphization profile in .a) and the time-annealing evolution at 500 °C in .b), and TEM cross section picture in c).

In Figure 2.19.a), the amorphous/crystalline interface shows a full amorphization. The resulting amorphous/crystalline interface shape in Figure 2.19.b) matches this time the experimental one, observed in TEM-cross section picture in Figure 2.19.c). Thereby, precise dose rate must be taken into account into simulations to predict the shape of the amorphization.

The recrystallization is thus partial and limited by the SPER rate along <110> fronts. A 500 °C/10 min annealing is indeed not enough to allow the recrystallization up to the future silicide position. This simulation does not however take into account dopant-enhanced regrowth rate effects, but simulated and experimental observations matches relatively-well. To our knowledge, no calibrated simulations taking into account the effect of dopant concentration on the SPER rate with the considered thermal budget and crystalline orientation are available. Nevertheless, these simulations give a valuable insight into the regrowth mechanisms, enabling to understand the partial recrystallization and the amorphous/crystalline interface shape in the TEM picture in Figure 2.19.c), which thus lead to the I_{on} degradation observed in Figure 2.16.

Because of the seed shape, which leads to recrystallize via the <110> crystalline orientation, the duration of the annealing has to be modified. Indeed, SPER along <110> fronts is twice lower than along <100> ones, as explained in section 2.1.2. To validate this point, a 10 min supplementary annealing after the Back End Of Line process (BEOL) was applied for 500 °C-activated devices, and the resulting I_{on}-I_{off} trade-off is plotted in Figure 2.20, for two gate length, 30 nm and 60 nm.

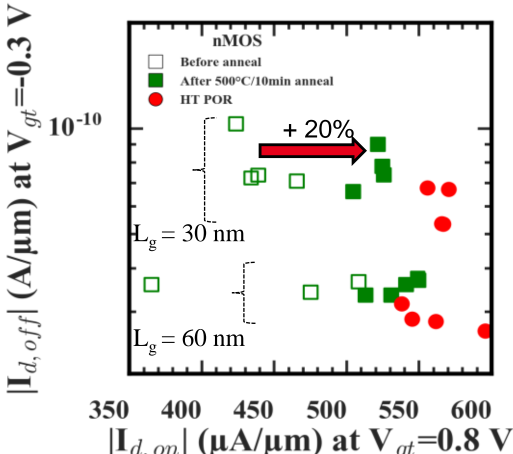


Figure 2.20: I_{on}-I_{off} trade-off before and after a post back end supplementary annealing (500 °C/10 min)

After the supplementary 500 °C/10 min annealing, I_{on} values are increased by 20 % without I_{off} modification for the shortest gate length. This might thus be interpreted as a complementary

recrystallization of the SD area, confirming our analysis. Activating devices at 500 °C is thus possible, also for nMOS ones, when the annealing time is adapted to the considered orientation used during the recrystallization.

Via this study, it has been shown that the dose rate influence the depth of the amorphous layer. For these implantations conditions, full access amorphization has been observed. It is additionally noticed that using the channel as a seed is feasible as long as the annealing duration is tuned to take into account the change of the crystalline orientation used for the recrystallization process.

RECRYSTALLIZATION OPTIMIZATION

In comparison to a horizontal seed, using the channel as a seed will involve more complex recrystallization mechanisms, which might thus influence the annealing duration. Figure 2.21 shows a simulation with a 3D view of the recrystallization mechanism after a 600 °C/100 s annealing of devices with the same geometry than the fabricated one.

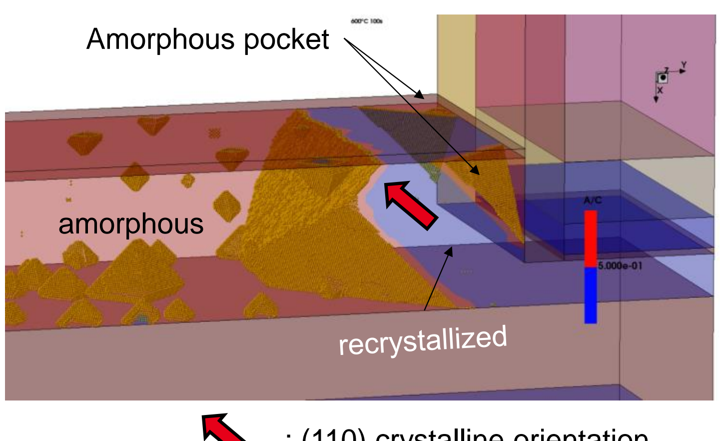
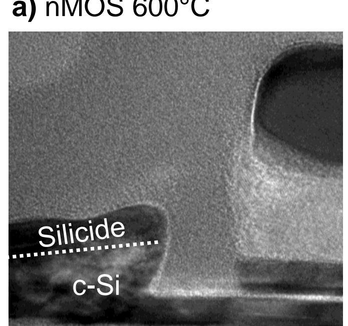


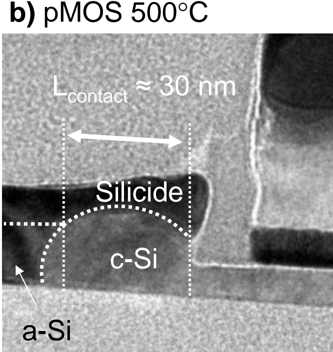
Figure 2.21: 3D view of the recrystallization mechanism with amorphization profile shown in Figure 2.19.a)

It can be observed that even if the main crystalline front is along <110> crystalline orientation, other orientations will still be involved into recrystallization process, forming for example amorphous pocket at the corner of the SD area. This change of the crystalline orientation and the impact on device performance will be investigated via morphological and electrical results,

and thanks to the qualitative calculus of the SPER rate, explained in 2.1.2 and summarized in Table 1. For both n&p type, dopant concentration in the junction has been estimated at 2×10^{20} at/cm^3.

Concerning the I_{on}-I_{off} trade-off in Figure 2.16.a), for all 600 °C-activated devices, electrical performances are close to the HT POR, for both p&n MOS. Same result is also found for pMOS devices activated at 500 °C. To explain these good results, TEM cross section pictures of such devices for 600 °C-activated nMOS and 500 °C-activated pMOS are compared in Figure 2.22.a) and .b). In Figure 2.22.c), the TEM cross section picture of Figure 2.18.a), for 500 °C-activated nMOS is also added for comparison.





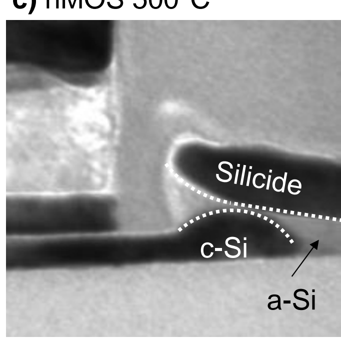


Figure 2.22: TEM cross section picture of 600 °C-activated nMOS (.a), 500 °C-activated pMOS (.b) and 500 °C-activated nMOS (.c)

In Figure 2.22.a), in the SD area, no partial recrystallization is observed. This is due to a relatively high SPER rate at 600 °C. This velocity is indeed equal to 120 nm/min according to the values estimated in Table 1, following the <110> crystalline orientation at 600 °C with phosphorous specie enhancement. Thus, contact between silicide and recrystallized silicon is large enough to achieve high I_{on} value. For pMOS devices, at 500 °C, the SPER rate is lower and equal to 9 nm/min along <110> fronts. However, with a 10 min annealing, a large area has been recrystallized, and it is observed in Figure 2.22.b) that 30 nm of the SD is recrystallized and in contact with the silicide. This minimum contact length $L_{contact}$ might thus be sufficient to conserve a lower silicide/silicon contact resistance as no significant performance degradation has been observed.

In Figure 2.22.c), no contact between silicon and silicide is indeed observed, which might thus explains the poor I_{on} value. The strong I_{on} variation and dispersion of the 500 °C-activated nMOS devices (from 550 µA/µm down to 30 µA/µm) observed in Figure 2.16.a) might additionally be explained by this minimum contact length. The amorphized part between the silicide and the recrystallized area is indeed very thin (smaller than 1 nm). A small fluctuation during device fabrication, such as the depth of the silicide, the thickness of the epitaxy or the depth of the amorphous layer, might thus lead to form the contact between the silicide and the recrystallized area. Still, the highest performances reached 84 % of 600 °C-activated devices one. Thereby, the contact length $L_{contact}$ between the silicide and the doped area is not long enough. It might thus be assumed that the minimal contact length should be at least equal to 30 nm.

To confirm this hypothesis, and by taking into account the precise dose rate for each implantation conditions, as well as the SPER dependency with the crystalline orientation and the temperature, KMC simulations have been carried for Low Temperature splits, for both p&n MOS. The time annealing evolution of the amorphous/crystalline interface shape is shown in Figure 2.23, with devices activated at 600 °C and 500 °C.

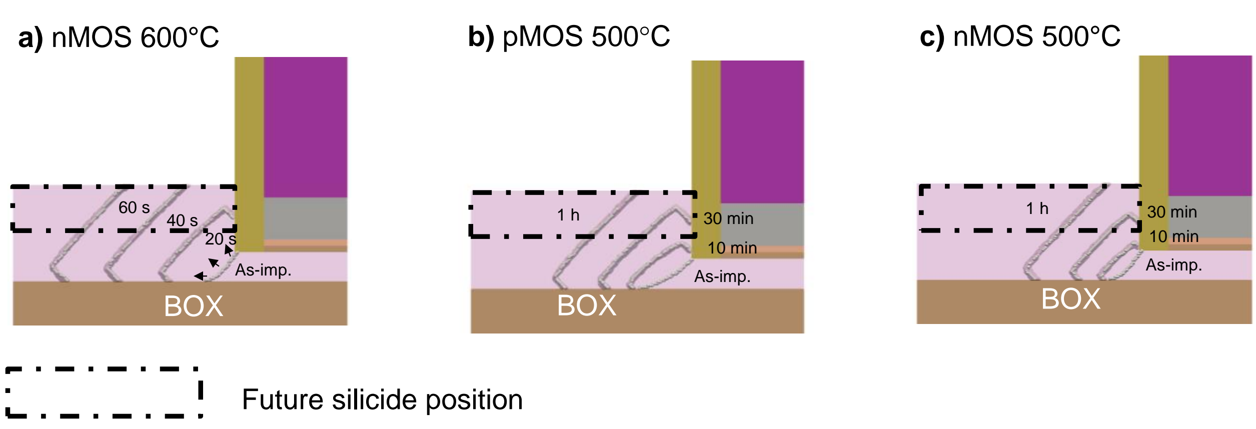


Figure 2.23: Time-annealing evolution of 600 °C-activated nMOS (.a), 500 °C-activated pMOS (.b) and 500 °C-activated nMOS (.c)

The SPER of 600 °C-activated devices rate is high enough to recrystallize a large part of the SD area (Figure 2.23.a). The amorphization shape for pFETs is slightly different from nFET and leave a crystalline seed extending far away from the channel. At 500 °C for both n and p type,

a 10 min annealing is not enough to form a contact, which is consistent with the TEM picture of nMOS devices, but does not correspond to the TEM picture previously observed for pMOS devices. These simulations however do not take into account dopant-enhanced regrowth rate effects. It could hence constitute the first hypothesis about the difference between n and p MOS devices. Indeed, as shown in Table 1 in section 2.1.2, the SPER rate is three time larger with boron incorporation than with phosphorous one.

Figure 2.24 depicts two devices, with different crystalline seed, and thus two different a/c interfaces. The first one (Figure 2.24.a) represents a horizontal seed, which was at first expected, and the second one (Figure 2.24.b) with a seed coming from the channel, which has been observed in this study. In these schemes are also added the expected evolution of the a/c interface after an arbitrary partial recrystallization. The future silicide position is added, in order to highlight the contact area between the doped SD and the silicide.

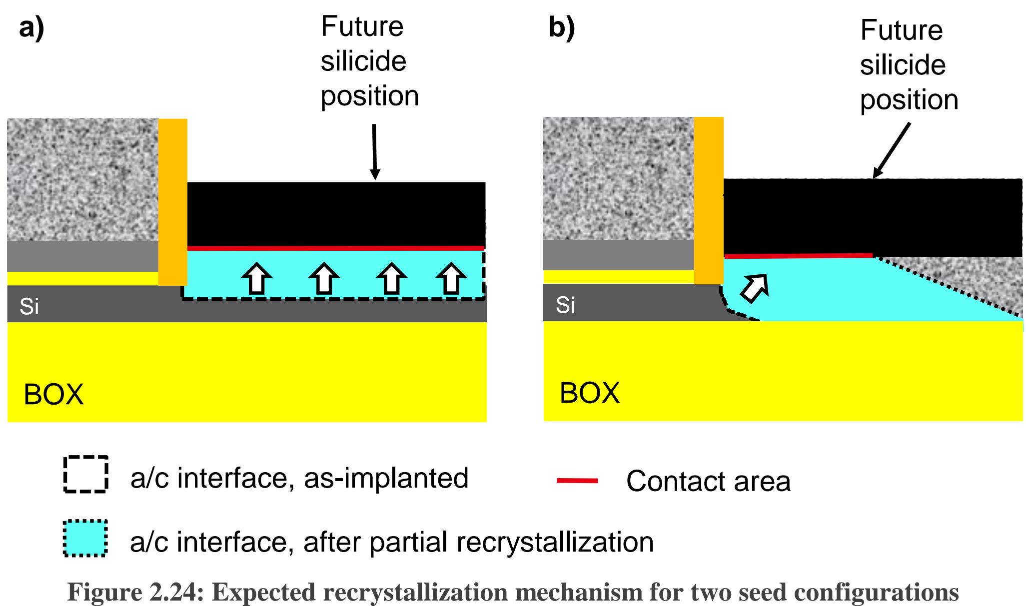


Figure 2.24: Expected recrystallization mechanism for two seed configurations

Figure 2.24.a) thus represents what it is commonly expected, and the contact area corresponds approximately to the silicide surface. With a horizontal seed, in order to form a contact

with the silicidation, all the SD should be recrystallized. In Figure 2.24.b), the contact area is reduced due to the different recrystallization mechanism when the channel act as a seed.

In order to estimate the minimum length of the silicide/recrystallized regions ($L_{contact}$) needed to reach the POR performance, electrical simulations using SDEVICE have been carried out. At first order, the recrystallized part has been considered uniformly doped at 2×10^{20} at/cm^3, as described in Figure 2.25.a). The amorphous layer has been however considered to be totally non-activated. The resulting I_{on} as a function of the contact length is shown in Figure 2.25.b).

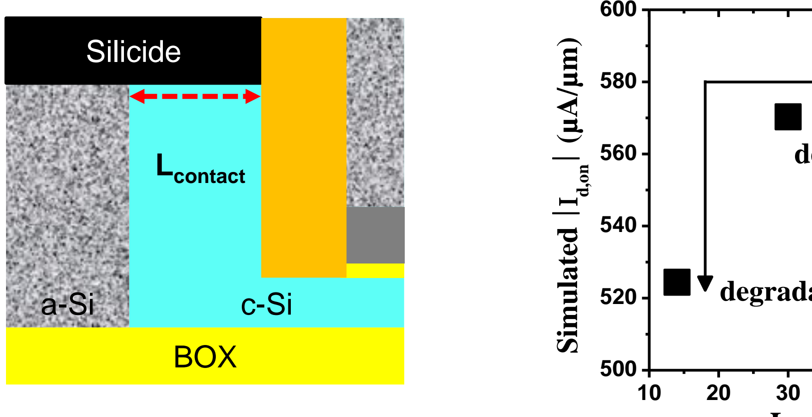


Figure 2.25: 28 nm electrical simulation for nMOS splits, evidencing the negligible influence of the Silicide/c-Si interface length ($L_{contact}$) above 30 nm

In Figure 2.25.b), a contact length equal to 60 nm represents the most ideal case, with a value equivalent to our electrical results. The I_{on} value is slightly degraded (-2 %) for $L_{contact}$ = 30 nm. However, decreasing this contact length down to 15 nm lead to a 10 % I_{on} degradation, and is thus considered as insufficient. A contact length equal to 30 nm is also consistent with the TEM cross section pictures (Figure 2.22). It thereby appears to be a reasonable target for the recrystallization length when full amorphization occurred.

Finally, by taking value from Table 1 for nMOS devices, a 15 min annealing should be at least applied for nMOS –and thus CMOS- devices to recrystallize the SD. Because this value is an estimation of the SPER rate, for future study, it is however advised to also double this annealing duration. The recrystallized areas are indeed shorter in the TEM cross section pictures for 500 °C-

activated devices for n and p type than what could be expected from values given in Table 1. It could be explained by the fact that the recrystallization mechanism involved to estimate the SPER rate in Table 1 is one-dimensional. Through morphological and through simulations, it had been observed that the amorphous/crystalline interfaces are however curved and that two or three of the crystalline orientations might be involved during the recrystallization process. A more complex mechanism might thus be involved, and could result in an additional difference of the SPER rate values of Table 1 and the one taking place in our process.

For further studies, an example of such temperature/annealing time couple is given in Table 3, together with the estimated contact length.

	annealing		
	600°C/2min	500°C/20min	500°C/30min
Lcontact	240 nm	52 nm	78 nm

Table 3: Temperature/annealing couple and the estimated $L_{contact}$

CHANNEL ORIENTATION

It is worth noticing that using the channel as a seed in only possible when the channel is <100>-oriented. Indeed, for a <110>-oriented channel, <111> crystalline orientation should be present, slowing significantly down the SPER rate, and possibly forming {111} twin defects. To highlight this point, Figure 2.26 shows, for the 600 °C-activated nMOS devices, the time annealing evolution of the a/c front, for a <110>-oriented channel (Figure 2.26.a) and for a <100>-oriented one (Figure 2.26.b).

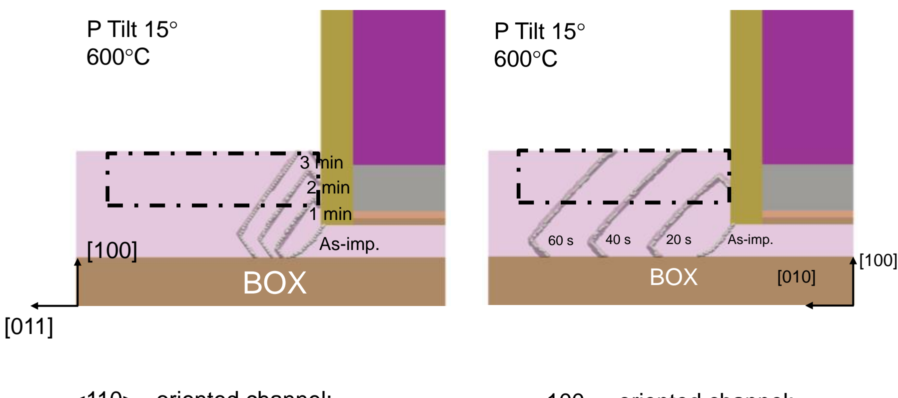


Figure 2.26: KMC simulations of the a/c front with <110>-and <100> oriented channel, for 600C°C-activated nMOS.

As expected, it is observed in Figure 2.26.a) that after a 1 min annealing, only a slight volume is recrystallized. In [9], [36], [37], [38], it has also been observed by TEM picture that a full amorphization stops the recrystallization process. Full recrystallization with this orientation is not sustainable to manufacture low-temperature transistors with high performance. Finally, channel strain relaxation has been observed in [16] for a <110>-oriented channel, but to our knowledge, no study has been carried out for a <100> oriented one for low temperature devices. An interesting study could thus be performed on this point.

NON-TILTED IMPLANTATION

Finally, a last split has been analyzed in the previous study, for 600 °C-activated nMOS devices, with non-tilted implantation. Figure 2.27.a) shows the I_{on} I_{off} trade-off and Figure 2.27.b) represents the I_d-V_g curve with this supplementary split.

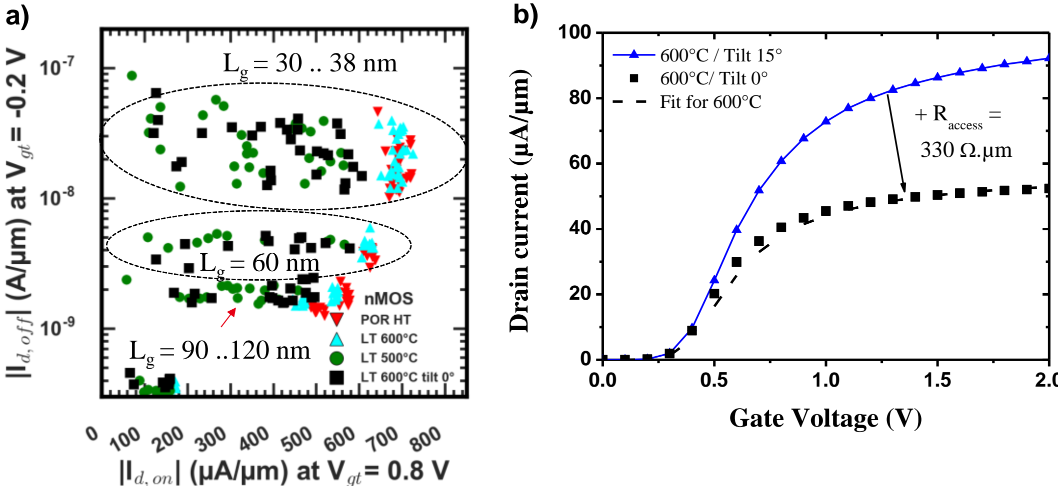


Figure 2.27: I_{on} I_{off} and I_d-V_g curve with 600 °C/tilt 0° split

It can be observed in Figure 2.27.a) that for the 600 °C/tilt 0° split, I_{on} degradation without I_{off} modification is observed. In addition, the same signature for this degradation can be observed between this split and the 500 °C-activated one. As for the former split, a R_{on} degradation is suspected, and confirms in Figure 2.27.b), where the global shape of the curve is fitting by adding an additional 330 Ω.µm on the R_{access}, similar to the 500 °C split. This degradation is as well interpreted as a partial recrystallization. Profile amorphization has been estimated by KMC simulation with the precise dose rate, and Figure 2.28 shows the resulting time-annealing evolution for 600 °C-activated devices, with and without tilted implantations.

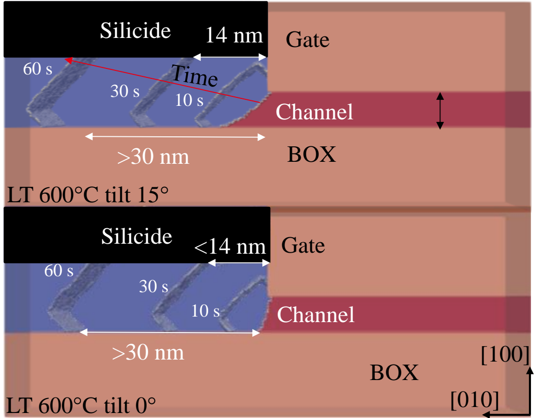
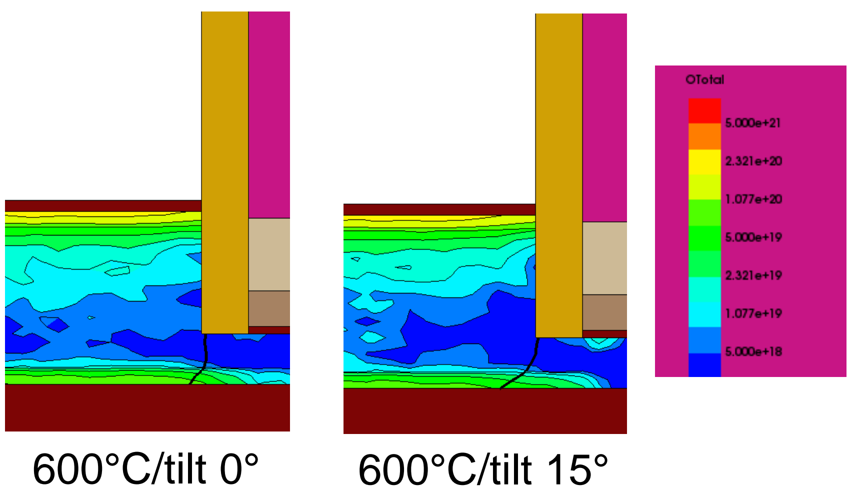


Figure 2.28: time annealing evolution for 600 °C activated nMOS devices, with or without tilt

It can be observed that the slight difference of the amorphization profile should not significantly influence the recrystallization length. In 60 seconds, recrystallization should thus have extended over 30 nm from the channel edge. Additionally, the dopant enhancement on the SPER rate should increase $L_{contact}$ up to 120 nm, according Table 1. The I_{on} degradation for non-tilted implantations is thus in this case not merely explained by the orientation and doping conditions.

Oxygen or nitrogen incorporation by implantation recoil in the access could be a possible explanation of the SPER rate reduction. KMC simulations have been performed to qualitatively evaluate the oxygen (Figure 2.29.a)) and nitrogen recoil (Figure 2.29.b)) for both LT split at 600 °C

a) Oxygen concentration



b) Nitrogen concentration

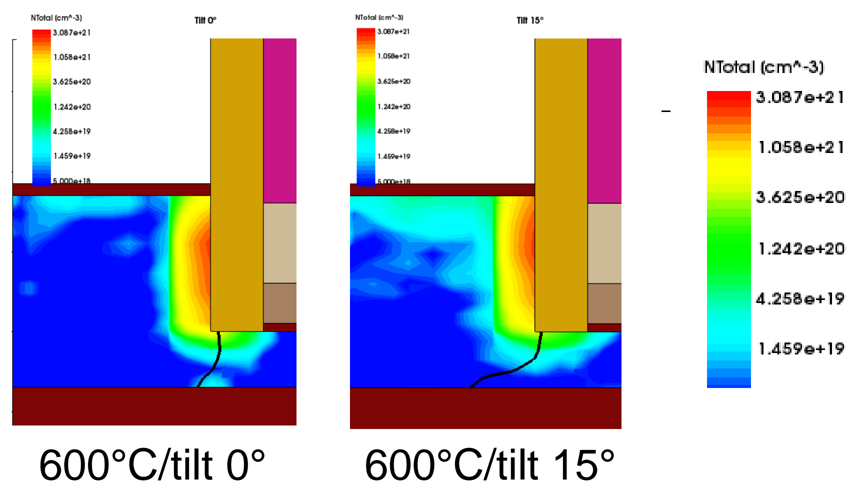


Figure 2.29: KMC simulation of oxygen and nitrogen recoil

No significant profile differences could be observed between the two implantations in Figure 2.29.a) and .b), and nitrogen or oxygen incorporation hence does not seem responsible of the SPER rate reduction.

The anchoring point between the a/c interface and the BOX may in this case plays a significant role. The effect of a wet clean before implantation should be studied when full amorphization is involved, in order to suppress the possible oxygen recoil due to the implantations.

Finally, it had been demonstrated that using the channel as a crystalline seed is feasible for the SPER process. Precise implantation conditions for Extension Last integration scheme is thus not compulsory. In such a scheme, the amorphization especially depends on the variation of the epitaxy thickness. While targeting a partial amorphization requires precise implantations conditions in order to leave a crystalline seed, for a full amorphization, such a precision is in fact not compulsory. It has however been experimentally observed that the shape of the a/c interface is critical and that an almost vertical front must be avoided to be able to lower the thermal budget down to 500 °C.

2.2.3 DIBL optimization

In the introduction of this section, a significant DIBL degradation has been observed for low-temperature pMOS devices compared to the High Temperature Process of Reference, regardless the activation temperature. As a reminder, the DIBL as a function of the gate length is plotted in Figure 2.30, for HT and LT devices previously described.

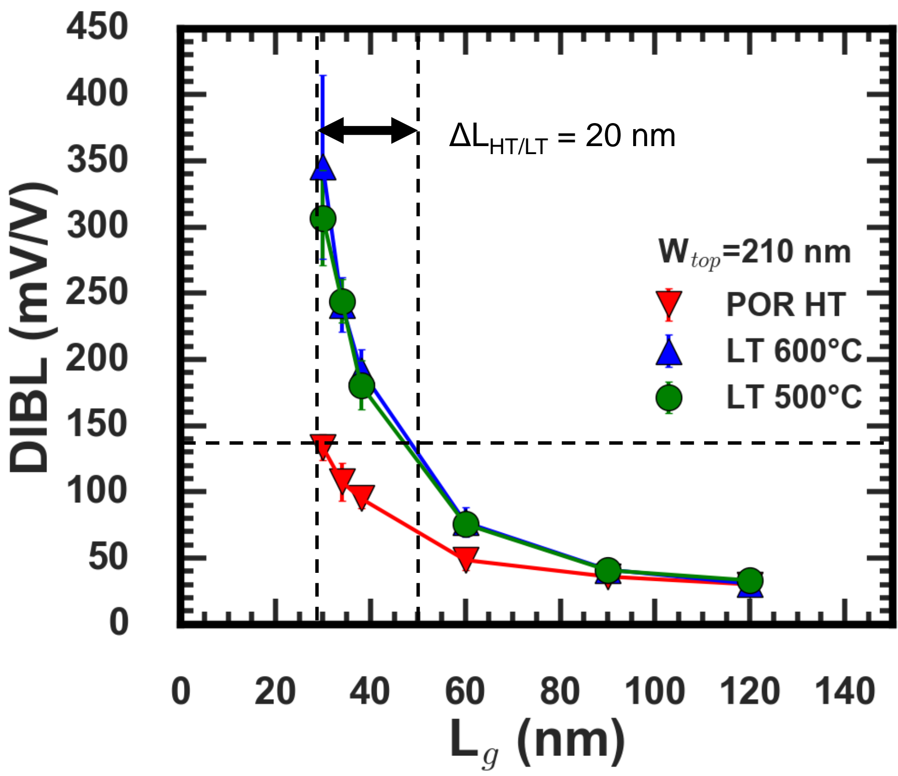


Figure 2.30: DIBL as function of L_g for HT and LT split

For the shortest gate length (30 nm), DIBL value of all low-temperature devices is higher than 350 mV/V, largely exceeding the POR value, which is equal to 150 mV/V. The DIBL degradation can be either due to non-optimized implantation conditions or by TED effect. In this sub section, the origin of the DIBL degradation for pMOS devices compared to the HT POR is investigated in details.

ANALYSIS

KMC simulations have then been performed with the precise dose rate, for a 7 nm-thick channel, 20 nm-thick RSD, 10 nm-thick offset spacer and 50 nm-long device. Figure 2.31 shows the resulting simulation right after the implantation (Figure 2.31.a)), and after a 630 °C/2 h annealing (Figure 2.31.b)). The color gradient represents the boron chemical concentration. It is worth noticing that such simulations take into account the impact of the TED effect. The amorphous/crystalline interface has also been added to the figure.

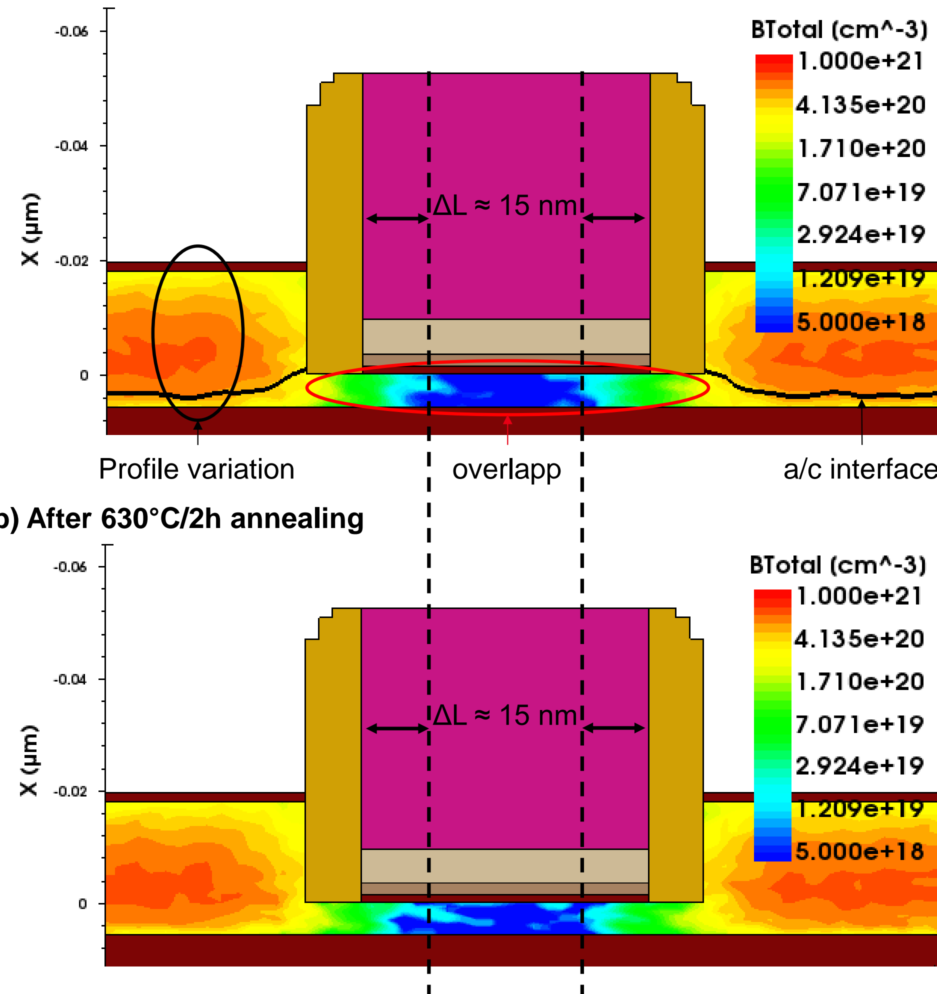


Figure 2.31: Process simulations of the boron chemical-concentration profile, a) as implanted and b) after a 630 °C/2 h annealing.

Implantation conditions of the simulation have been set to reach a high doping concentration in the SD area (above 1×10^{20} at/cm^3). A relatively-high chemical concentration (above 1×10^{19} at/cm^3) is however observed in the channel region, which might lead to an overlapped junction. This simulation shows that, between the gate edge and the iso-concentration of 1×10^{19} at/cm^3, 15 nm of the channel is doped (about 7.5 nm at each side of the gate). A difference in the electrical length between low and high temperature devices might thus explain the DIBL

degradation. Based on the simulation results and taking into account that the 1×10^{19} at/cm^3 iso-concentration of the HT POR devices is at the gate edge (simulations not shown here), it can be concluded that the electrical length difference between LT and HT devices ($\Delta L_{HT/LT}$) is equal to 15 nm.

The difference of the electrical gate length between the LT and HT split might also be experimentally extracted at the first order using Figure 2.30. By fixing an arbitrary value on the DIBL of 140 mV/V for L_g = 30 nm, the electrical-length difference between high-temperature device and low-temperature ($\Delta L_{HT/LT}$) is estimated to 20 nm. This value is close to the one estimated by simulation. In that case, this electrical-length difference leads to a DIBL degradation of +200 mV/V. Besides, the same methodology has also been applied in the previous thesis [4], and an electrical-length difference of 8 nm has led to a DIBL degradation of +100 mV/V. The DIBL degradation could hence be explained by an overlapped junction.

No difference in the junction profile has however been observed before and after a 630 °C/2 h annealing, which might indicate that the DIBL degradation may not be caused by TED effect. The DIBL degradation suggests that the dopants located into the channel are electrically active up to 1×10^{19} at/cm^3, while these dopants were not situated in the previously-amorphized region. As evidenced in a former study, and shown in Figure 2.3, only the dopants located into the previously amorphized layers or very close to the as-implanted amorphous/crystalline interface (below 2 nm) are indeed activated with electrical concentration beyond 1×10^{19} at/cm^3.

Through the simulation in Figure 2.31, the amorphous/crystalline interface is at least 10 nm away from the channel zone. Low activation level was expected for dopants in the non-amorphized region. It can hence be suspected that the thermal-activation level in these devices is higher than the one observed in the former experiences, and is discussed in the following sub section.

In the literature, various values are given for the electrical solubility of boron, as described by P. Pichler in [55]. The boron solubility limit plotted as a function of the temperature extracted from this study is shown in Figure 2.32.

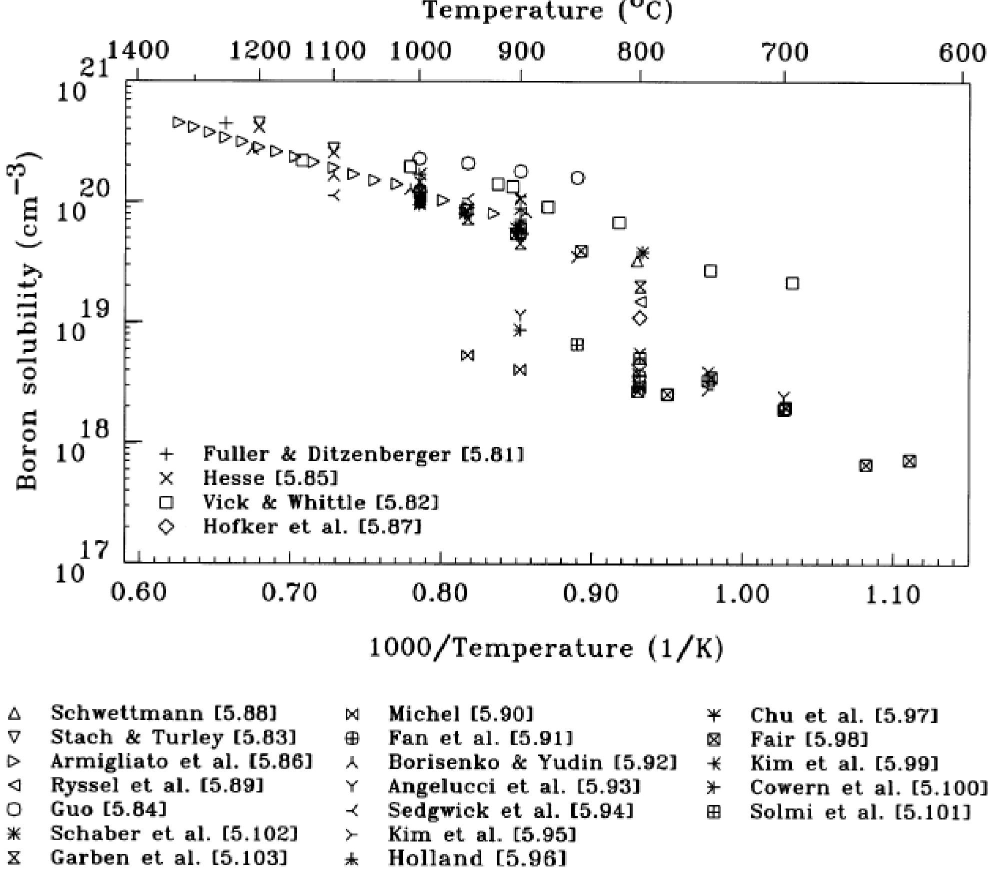


Figure 2.32: Boron solubility as a function of the temperature from [54]

As seen in Figure 2.32, the activation level varies from 2×10^{18} at/cm^3 to 2×10^{19} at/cm^3 at 700 °C. This might be explained by the fact that the electrical solubility of a dopant depends on the dopant cluster formation. If the implantations has generated a lots of point defects, the inactive cluster formation can increase, reducing the electrical solubility. It is also worth noticing that the ideal electrical solubility limit corresponds to the thermodynamic equilibrium, i.e. with an infinite annealing duration and in a perfect crystal (without point defects). One particular reference (S.F. Guo in [56]) gives a very high value, above 2×10^{20} at/cm^3 at 830 °C, which is far beyond the other references. This might be due to the fact that this experimental value has been obtained by Boron-Nitride layer diffusion, which enable to incorporate boron atoms without implantation. The absence of point defects created by implantation could hence be the origin of this very high activation level. Values above 1×10^{19} at/cm^3 might be obtained by extrapolating the electrical solubility at 500 °C.

In our device, it has to be noticed that the silicon-interstitial concentration in the region below the spacer can be particularly low. This region is indeed relatively far from the implanted region and two interstitial sinks (channel-BOX and channel-spacer/gate interface) are very close to each other (below 10 nm). This could hence explain the very high activation level observed at 500 °C in the non-amorphized region situated below the spacer and the gate.

As a conclusion, it is suspected that the relatively high activation level (above 1×10^{19} at/cm^3 at 500 °C) of boron can be obtained for dopants located below the offset spacer and below the gate, even if this region has not been amorphized. To reduce the DIBL of our devices, the boron concentration in the channel should thus be reduced. SProcess simulation in Figure 2.33 shows that such implantation conditions might be found.

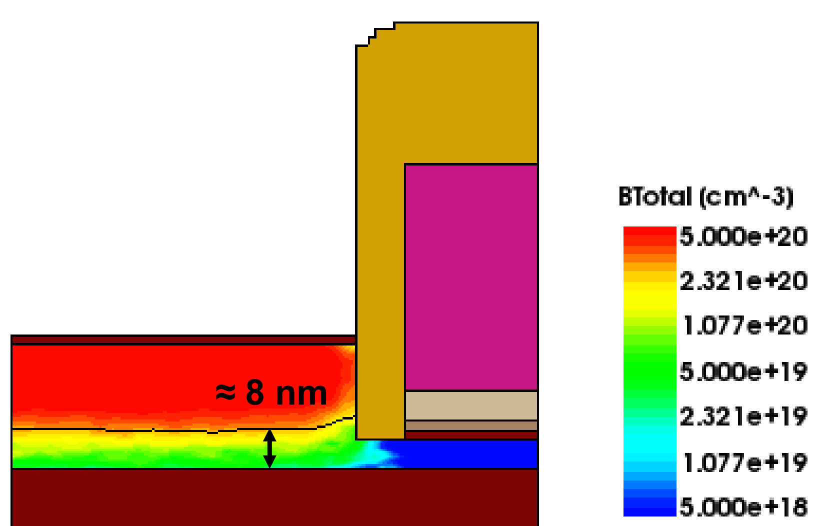


Figure 2.33: Process simulations as implanted of the boron chemical-concentration profile, with a reduction of the boron concentration in the channel

In this case, we observe that the 1×10^{19} at/cm^3 iso concentration is below the offset spacer and not in the channel. The DIBL could thus be better controlled.

To remember

- Solid Phase Epitaxy Regrowth will be the main mechanism involved during this thesis to manufacture low-temperature devices.
- Implantation current plays also a key role to control the seed thickness.
- The SPER rate mainly depends on three parameters:
    - the temperature,
    - the crystalline orientation,
    - the type of impurities and their concentrations.
- Due to the excess of interstitial at the amorphous/crystalline interface, several electrical degradations might occurred:
    - I_{on} decrease due to Boron-Interstitial Cluster (BIC),
    - DIBL increase due to Transient-Enhanced Diffusion (TED),
    - $I_{d,\ min}$ increase due to Trap-Assisted Tunneling (TAT).
- TED effect might be reduced thank to carbon co-implantation.

I_{on} degradation for nMOS devices

- It has been shown that 500 °C activated device can reach performance comparable with devices activated with high-temperature annealing.
- The origin of the poor performance of nMOS devices at 500 °C has been analyzed and is attributed to a too small duration of the SPER anneal.
- These data show that a full access amorphization can allow the recrystallization at 500 °C. The amorphous/crystalline interface must however not be fully vertical and the channel orientation must be in the <100> crystalline direction. In these conditions, the annealing duration should be in the 30 minutes range.

- Recrystallizing a fully amorphized S&D is only possible with a <100>-oriented channel. In a <110>-oriented channel, the apparition of twin defects stops the recrystallization after few nanometers of crystal regrowth.

DIBL degradation for pMOS devices

- The degraded DIBL of our p-type devices is attributed to a non-optimized boron concentration in the channel.
- A high electrical solubility of boron is observed in the region below the spacer and in the channel, up to 1×10^{19} at/cm^3 at 500 °C. This high value might be explained by the small interstitial concentration in that region where two interstitial sinks are present at a distance of 6 nm.
- To optimize the DIBL in future devices, it is thus advised to reduce the boron concentration at the channel entrance, below 1×10^{19} at/cm^3.

3. LOW-TEMPERATURE EXTENSION-FIRST FDSOI INTEGRATION

This chapter focuses on Extension First (X^{1st}) integration scheme. In a previous study [57], low temperature device performances have respectively reached 90 % and 95 % of the High Temperature Process Of Reference devices for n and p MOS. In this work, two levers of performance improvement are evidenced: the first one concerns access resistance and the second one deals with the suppression of the EOT regrowth at the gate edge. Thanks to these optimizations guidelines, low temperature performance (I_{on}-I_{off} trade-off) are expected to be improved with respect to the previous study.

Contents

3. Low-Temperature Extension-First FDSOI integration 61

3.1 Results and conclusion of previous studies 62

3.1.1 Process Of Reference process flow of a 14 nm FDSOI 62

3.1.2 Electricals results 66

3.1.3 R_{access} optimizations 68

3.2 Extension First without liner 75

3.2.1 Advantage to implant through bare silicon 75

3.2.2 Integration proposition 79

3.3 EOT improvement 83

3.3.1 Electrical measurements 83

3.1 RESULTS AND CONCLUSION OF PREVIOUS STUDIES

In [16] it had been evidenced that the region below the offset spacer was highly critical to reduce the global access resistance. To lower the resistance of the region situated below the offset spacer (R_{spa}), a new integration scheme had been proposed, called Extension First (X^{1st}) integration scheme, detailed in [9]. In the introduction of this section, the device fabrication of low-temperature Extension First devices is described, detailing the main process difference with high-temperature device process flow. The main result and conclusion of this integration scheme will also be described. This will allow to better understand the optimizations, which are intrinsically linked to the previous study, and proposed in sections 3.2 and 3.3.

3.1.1 Process Of Reference process flow of a 14 nm FDSOI

A reference of devices manufactured at high temperature is compulsory in order to compare the electrical characteristic of low-temperature ones. In this section, the Process Of Reference performed at High Temperature (HT POR) is thus at first described.

The 14 nm FDSOI technology proposed by STMicroelectronics presents some significant differences in the Front End Of Line transistor process flow compared to the 28 nm technology discussed in the chapter 2. Raised Source Drain epitaxies have been performed with the use of SiGe 35 % and SiC epitaxies for pMOS and nMOS respectively. The junction doping steps is obtained by *in situ* doped epitaxy instead of using beam line implantations. Besides, only for pMOS devices, a SiGe channel with 25 % Ge content has been introduced. It enables to lower the threshold voltage and to boost the hole mobility [58]. The process flow of High Temperature Process Of Reference (HT POR) devices in a CMOS integration is illustrated in Figure 3.1.

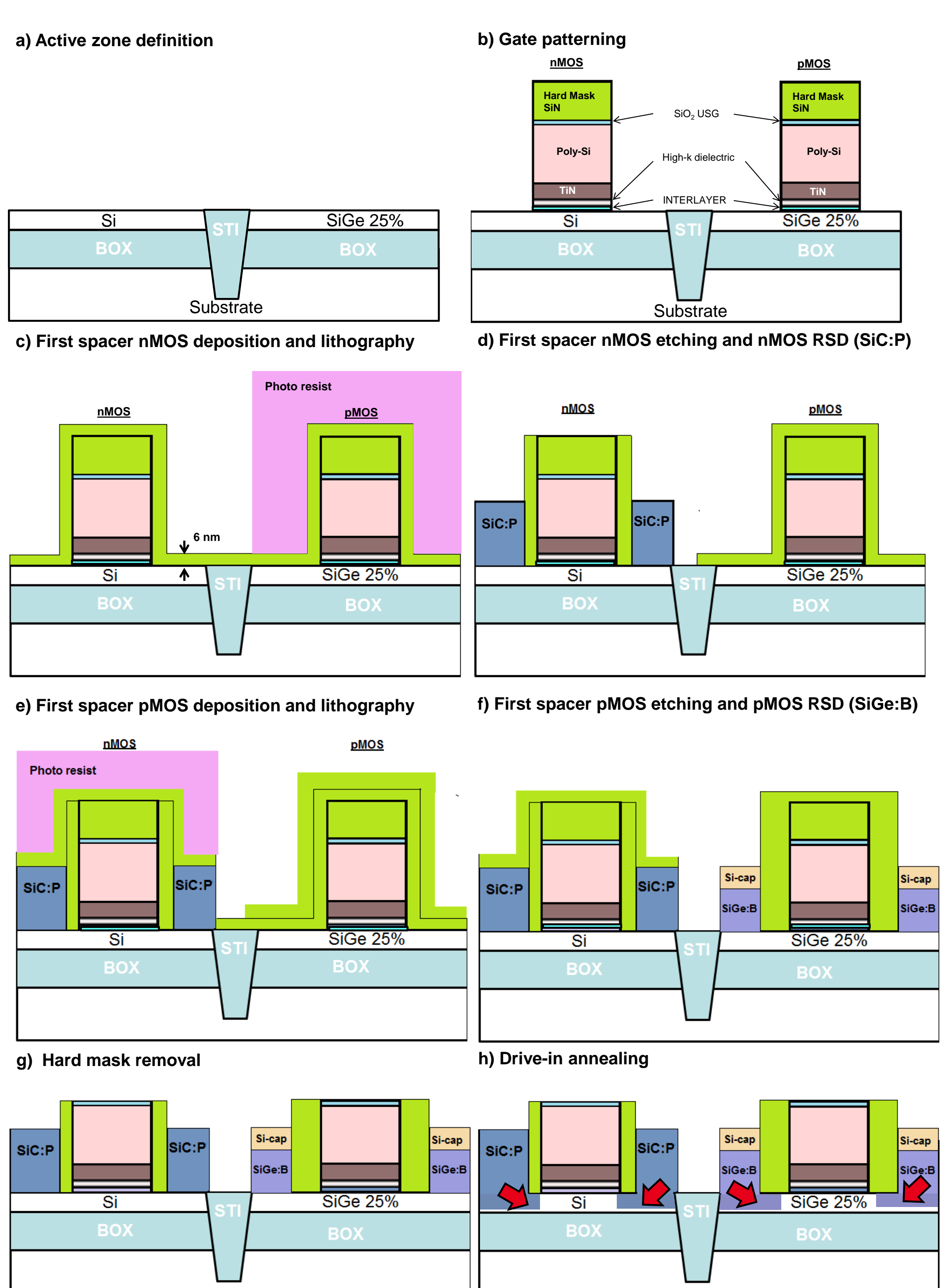


Figure 3.1: Process flow of HT POR devices for a 14 nm technology

FDSOI devices were fabricated on 6 nm-thick <110>-oriented Si (respectively SiGe) channels for nMOS (respectively pMOS) devices, with a 20 nm Buried Oxide (Figure 3.1.a). The gate stack is composed of a 1 nm-thick HfO_2, a 4 nm-thick TiN, a 24 nm-thick Poly Si, 6 nm SiO_2 and a 30 nm SiN Hard-Mask (Figure 3.1.b). A 6 nm-thick SiN is deposited on both pMOS and nMOS devices. pMOS zone are protected by photo resistive material, and the nitride on the nMOS zone is selectively etched from silicon film in order to form the 6 nm-thick nMOS offset spacer (Figure 3.1.c). The photo resistive material is then stripped, and SiC:P Raised Source Drain (RSD) epitaxy is performed on nMOS zone (Figure 3.1.d). pMOS zones are protected from this epitaxy thanks to the remaining SiN liner. A 3 nm-thick SiN is deposited on both pMOS and nMOS devices, and the latter are then protected by photo resistive material (Figure 3.1.e). The nitride on the pMOS zone is selectively etched from SiGe film in order to form the 9 nm-thick nMOS offset spacer. The photoresist material is stripped, and SiGe:B RSD epitaxy is then carried out on pMOS zone (Figure 3.1.f). nMOS zones are protected from this epitaxy thanks to the remaining SiN liner. The nitride liner from nMOS zones is then etched and the Hard Mask is removed (Figure 3.1.g). Afterwards, a drive-in anneal, which consist in a spike (1000 °C/1 s) and a dynamic surface annealing laser (1050 °C, 30 ns), is performed to activate dopants and to drive dopants under the offset spacer by diffusion (Figure 3.1.h).

For low-temperature devices, annealing have to be suppressed to reduce the thermal budget. The absence of dopant below the offset spacer results in a dramatic R_{access} degradation [16]. An implantation step has thus been carried out before the *in situ* doped raised source drain epitaxy, in order to place dopants at the gate edge. This integration scheme is hence called Extension First (X^{1st}). The modifications between Low-Temperature and High-Temperature splits are illustrated in Figure 3.2. During device fabrication, all mandatory steps in a CMOS integration, such as photoresist depositions and stripping, have been carried out, but not shown in Figure 3.2.

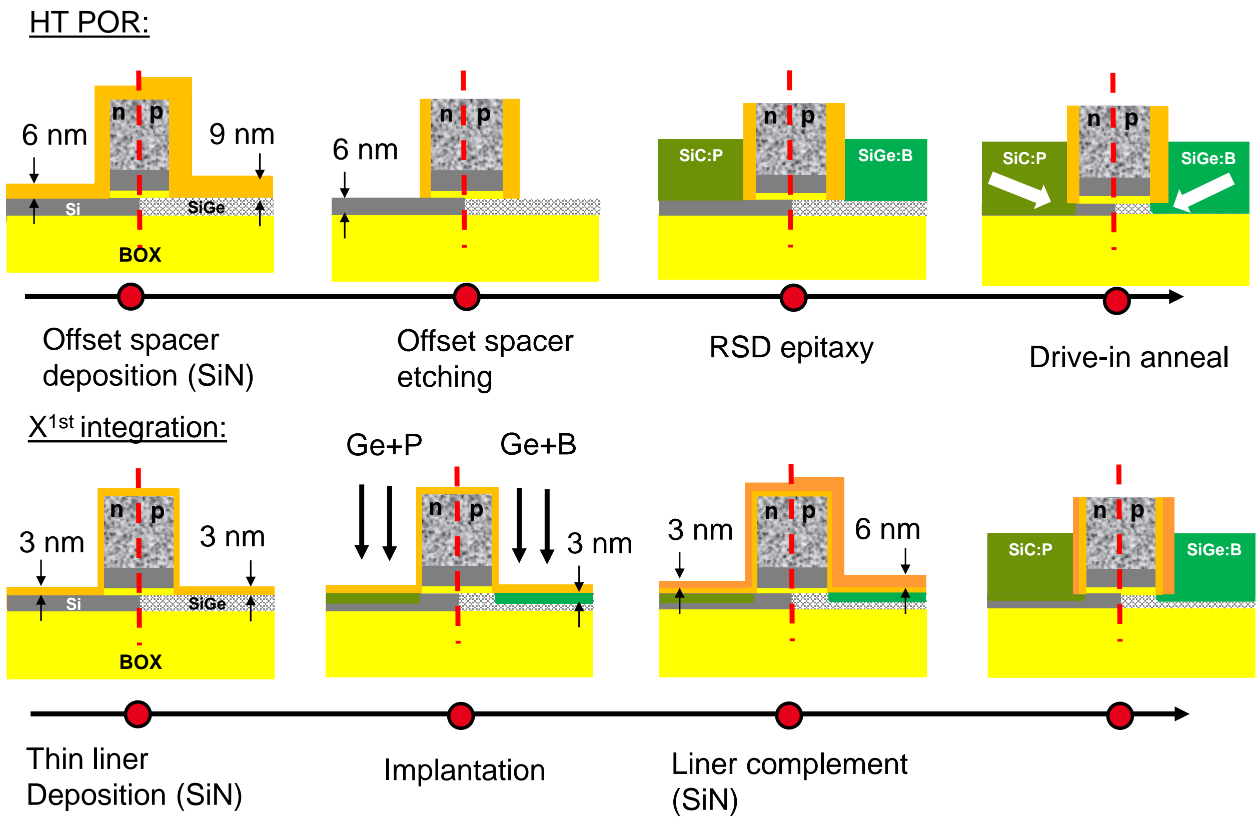


Figure 3.2: Diverging steps in the process flow of High-Temperature and Low-Temperature devices

For the Low-Temperature devices, a first 3 nm-thin nitride liner is deposited. A partial amorphization of the 6 nm-thick film is targeted by an implantation through the liner. For n-type (respectively p-type) devices, germanium and phosphorous (germanium and boron) have been implanted in order to dope the region below the offset spacer. A liner is then deposited to obtain the same offset spacer thickness than the HT POR. This liner is called ‘complement liner’, and is 3 nm-thick (6 nm –thick) for n-type (p-type) devices. SiC:P (SiGe:B) *in situ* doped raised source drain epitaxy is then performed, with a reduction of the thermal budget at 630 °C (respectively 640 °C).

Implantation splits used in this work (but defined in [57]) are described in Table 4.

Split Name	nMOS devices		
	Ge implantation	P implantation	Annealing
HT POR	None	None	1050°C
No Implant	None	None	None
No PAI	None	Yes	None
PAI	Yes	Yes	None

Split Name	pMOS devices		
	Ge implantation	B implantation	Annealing
HT POR	None	None	1050°C
No Implant	None	None	None
PAI	Yes	Yes	None

Table 4: Split details for p and n MOS devices

A split without implantation has been defined (for p and n MOS devices) in order to confirm the importance to dope below the offset spacer. It has been considered that for such low energy (< 2 keV) and dose (< 5×10^{14} at/cm^2), implanting phosphorous or boron only does not amorphize the crystalline silicon. A Pre-Amorphization Implantation (PAI) is then mandatory. For nMOS devices, a split without PAI has additionally been defined. The activation level for both p and n type is expected to be superior to 1×10^{20} at/cm^3.

By implanting through the thin liner and without dopant diffusion, the junction alignment with the gate is only defined by the thin liner thickness, while in the HT POR flow, the junction alignment depends on the spacer deposition thickness, the spacer etching process and the dopant diffusion. Contrary to the Extension Last integration scheme, the junction shape does not depends on the epitaxy thickness and shape variation, but only on the first liner thickness variation. In [16] it has also been evidenced that the thin liner only vary of 1 angstrom on a 300 mm wafer. In addition to allowing a smaller thermal budget, using Extension First integration scheme has been proven to induce a smaller variation on the electrical performance [57].

3.1.2 Electricals results

The resulting I_{on}-I_{off} trade-off for n and p type, and for High and Low temperature devices are shown in Figure 3.3.

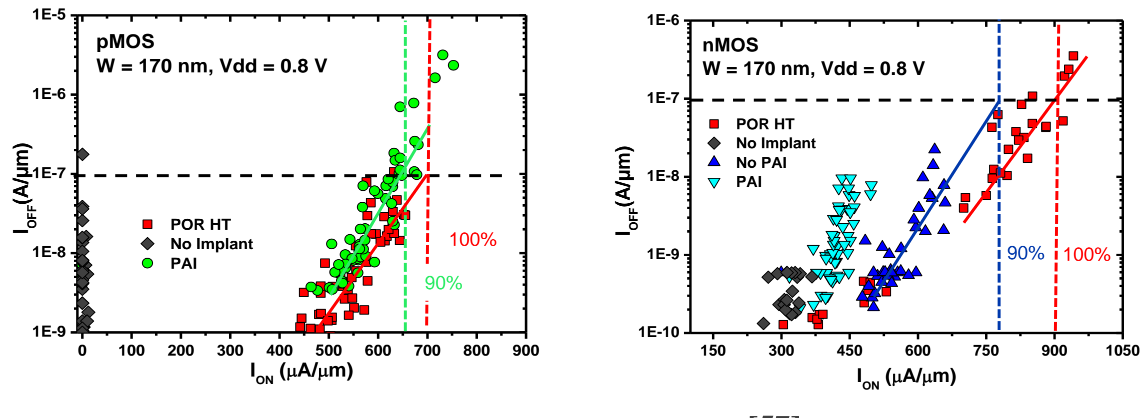


Figure 3.3: I_{on}-I_{off} trade-off from [57]

The 'No implant' split shows very poor value, below 100 µA/µm for pMOS, and inferior to 400 µA/µm for nMOS. Best implanted low-temperature split performances have reached 90 % and 95 % of the High Temperature Process Of Reference devices for n and p MOS, respectively. Doping below the offset spacer is thus compulsory to achieve high performance for low temperature devices.

EXTENSION LAST AND EXTENSION FIRST COMPARISON

The interest of Extension First integration scheme with respect of Extension Last one is discussed in this sub-section. Amorphizing and doping implantation right at the channel entrance should indeed enable to obtain high activation level in the most critical region for access resistance (R_{access}) minimizations [16]. Access resistances of low temperature and high temperature devices have been extracted using Y function methodology [59], and are shown in Figure 3.4. The Extension Last access resistances of electrical lot discussed in the previous chapter are also added.

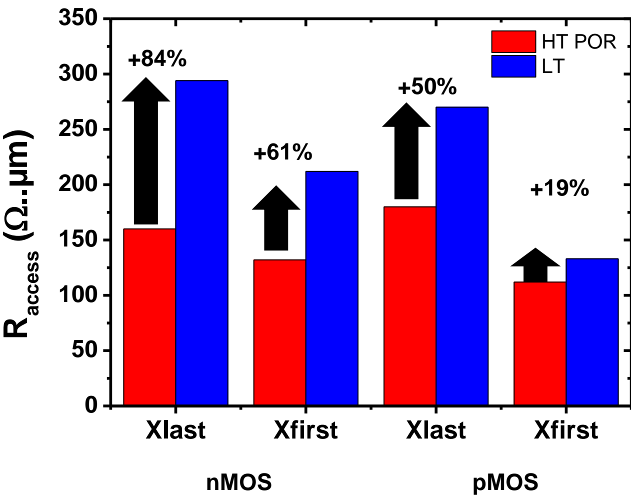


Figure 3.4: R_{access} for low temperature splits from [57]

While for a fair interpretation, the two integrations should be compared on the same lot and with the same spacer thickness, this first observation enables to underline that, with Extension First integration scheme, access resistances for both n and p type are closer to their respective references in comparison to the Extension Last integration scheme, especially for p-type.

3.1.3 R_{access} optimizations

As explained in chapter 1, the access resistance might be decomposed as the sum of three resistances ($R_{access} = R_{co} + R_{epi} + R_{spa}$). In the following paragraphs, conclusion on the R_{access} improvement are given, especially for the R_{spa}, which has been identified in the previous work as the main lever to improve device performances. This will enable to give some optimizations, which will be explained in section 3.2 and 3.3.

R_{SPA} LIMITATION/IMPROVEMENT

As shown in Figure 3.4, while for pMOS devices the R_{access} values of low temperature devices are 19 % higher than the HT ones, for nMOS devices, a 60 % degradation is observed. In [57], it had been attributed to a higher R_{spa}. To understand the origin of these strong degradations, implantations on a morphological lot of a 7 nm-thick film have been carried out for low temperature

splits with implantation only (without *in situ* doped raised source drain epitaxy and salicidation). This is thus a representation of the activation level achieved below the offset spacer, as sketched in Figure 3.5

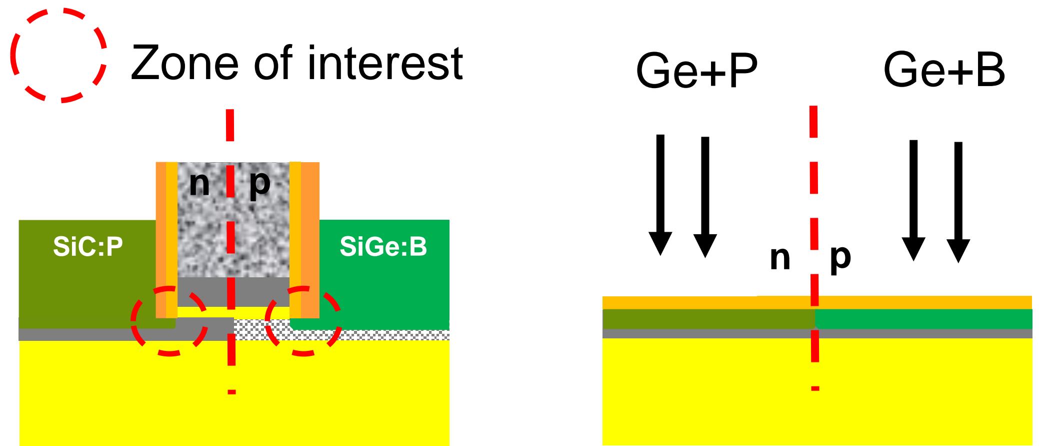


Figure 3.5: Illustration of the morphological result, and the interpretation for electrical device

Sheet resistances of such implantations are shown in Figure 3.6.a). The expected sheet resistance has also been calculated, by assuming a constant activation level in the amorphized depth. The mobility has been extracted from Masetti in [60], which allows to estimate at first order the activation level according to the measured sheet resistance and the amorphized depth. In Figure 3.6.b) and c) are plotted the resulting calculated sheet resistance as a function of the activation level and the amorphization thickness, for both doping species.

a) b)

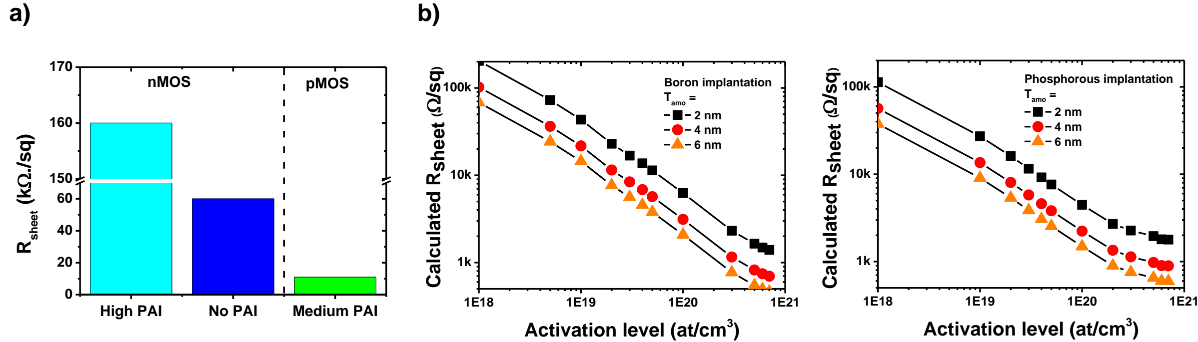


Figure 3.6: (a) Measured R_{sheet} and (b) calculated R_{sheet} as a function of the activation level for low temperature splits from [1]

For boron implantation, the measured sheet resistance is equal to 10 kΩ/sq. The amorphization depth has been estimated in [9] at 4 nm, which corresponds to a low activation level equal to 2×10^{19} at/cm3, one decade lower to what had been expected. For the No-PAI phosphorous implantation, the film should not be amorphized, due to the low energy and dose involved during the implantation. Dopant activation is thus performed without the SPER process, and the maximum activation level should thus be equal to the solid solubility limit, *i.e.* equal to 5×10^{19} at/cm^3 at 600 °C [9]. For the PAI split, a minimum of 2 nm of the film should be amorphized and recrystallized. SPER should enable high activation level, above 1×10^{20} at/cm^3, which should thus correspond to a sheet resistance below 10 kΩ/sq. On the contrary, a high value, equal to 160 kΩ/sq, has been measured. This value corresponds to a lower activation level, below 1×10^{18} at/cm^3. This dopant deactivation is hence attributed to the presence of impurities such as oxygen or nitrogen. In this work, this hypothesis has been verified by TEM measurements of n-type No PAI sample with Energy-Dispersive X-ray (EDX) spectroscopy, and shown in Figure 3.7. This morphological characterization confirms that implanting through a SiN liner and a native oxide can indeed incorporate nitrogen and/or oxygen into the film.

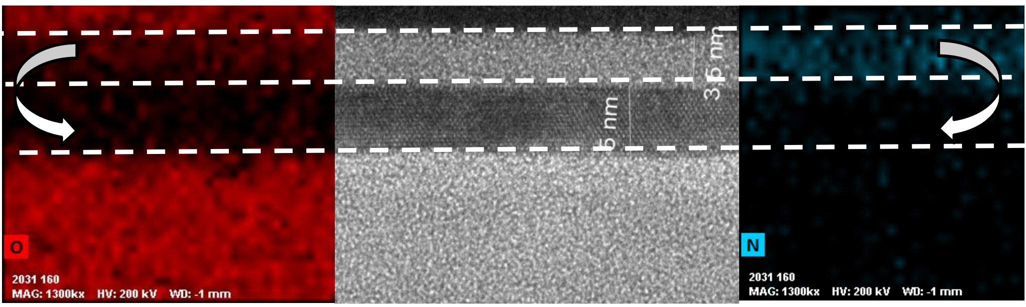


Figure 3.7: EDX and TEM of No PAI sample on full sheet after 600 °C/ 2 min annealing

As specified in [34], [35], neutral impurities might delay SPER rate and deactivate dopants. Phosphorous deactivation has been additionally observed in [61] when implantation is performed through a SiN liner, and might thus explained the R_{sheet} degradation observed in the morphological lot (Figure 3.6). Boron deactivation due to nitrogen recoil has also been observed in [62]. Secondary Ion Mass Spectrometry (SIMs) has been performed for n-type samples in order to confirm this result. The chemical concentration of phosphorous and nitrogen specie is plotted in Figure 3.8 as a function of the film depth.

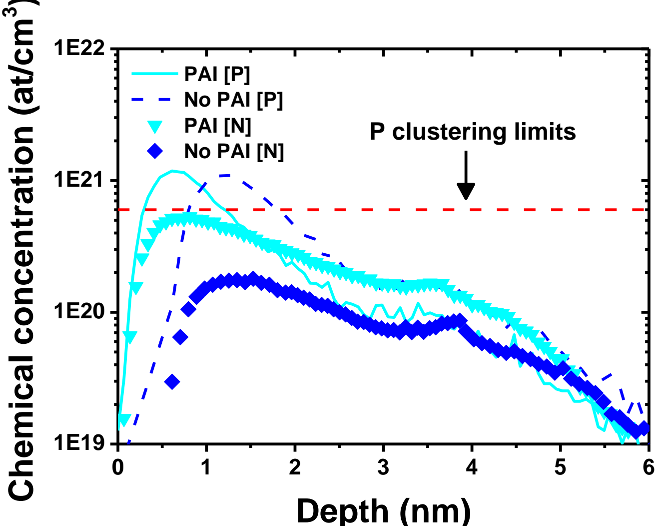


Figure 3.8: SIMS of the as-implanted n-type samples

Nitrogen recoil in the silicon film is evidenced for both samples, with a higher concentration when a Pre-Amorphization Implantation is carried out. It has thus been demonstrated that nitrogen has been incorporated during implantations. Besides, sheet resistances might be additionally degraded due to chemical phosphorous concentrations way above the clustering limit. Higher on state current might thus be expected if nitrogen/oxygen incorporation is avoided, and with a more sustainable doping concentration. Lowering R_{spa} appears thus to be one of the main lever to reach higher electrical performance.

R_{SPA} SPECIFICATION

As previously explained, the sheet resistance measurements are an indication of the activation level of dopant located below the spacer. In order to estimate the maximum sheet resistance values that should be achievable, SDEVICE simulations have been carried out by taking into account the activation level in this area for n-type devices. At first, sheet resistance has been simulated in order to obtain a more precise activation level according to each measured samples. This activation level has then been reported into electrical simulation for dopant located into the film.

For the High Temperature device, the junction has been simulated by taking the hypothesis of a slightly underlapped configuration (-2 nm). For the Low Temperature devices, the junction is considered ideal (fully aligned with the gate edge) but the activated region is 3 nm thick, in order to be consistent with a 3 nm seed configuration. Activation level for high-temperature (respectively low-temperature) device is equal to 6×10^{20} at/cm^3 (respectively 2×10^{20} at/cm^3) into the epitaxy, which is in agreement with the previous work [57]. The geometries used for these simulations are shown in Figure 3.9.a), without the silicide and the gate stack illustration for the sake of clarity. The resulting sheet resistance is plotted in Figure 3.9.b), for the HT and LT devices.

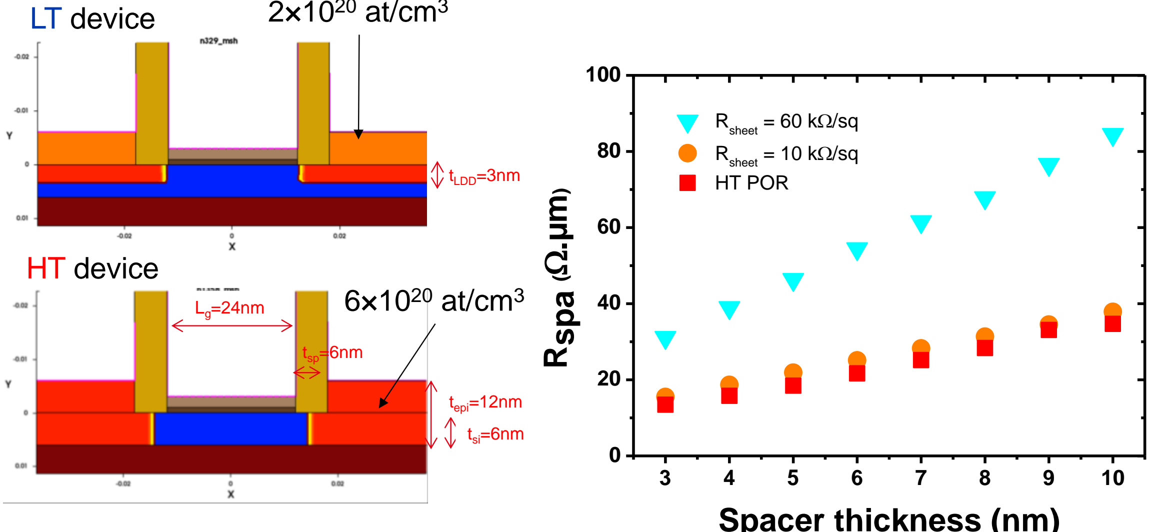


Figure 3.9: (a) LT and HT device configuration and (b) R_{spa} as a function of the offset spacer thickness

For a 6 nm-thick spacer, which corresponds to the spacer thickness of the characterized devices, the ideal sheet resistance of the area located below the offset spacer will be around 10 kΩ/sq to achieve the same R_{spa} than for High Temperature devices. As a conclusion, on future development for sheet resistance reduction of the R_{spa}, this value will be taken as a target. Same result has also been assumed for pMOS devices.

It is worth noticing that this X^{1st} architecture offers great opportunity in term of dynamic performance. Indeed, because the junction is implanted close to the gate, it does not rely on an annealing to locate dopant at the right position. It enables an increase of the spacer thickness which will be beneficial for dynamic performance. For HT devices however, annealing drive the dopants up to the channel entrance, and might lead to junction abruptness degradation.

PERSPECTIVE: R_{CO} AND R_{EPI} DEGRADATION

In [57], a lower activation level of Low-Temperature device (2×10^{20} at/cm^3) with respect to HT POR (6×10^{20} at/cm^3) has been measured. This degradation has been attributed to the lower thermal budget required to perform *in situ* Doped Raised Source Drain epitaxy. Achieving a higher activation level might thus be very challenging for devices manufactured at low thermal budget.

The impact of the activation level into the RSD area on electrical performance has been simulated for Low-temperature devices, and has been compared with the HT POR. The structure used is the same as the one involved for the R_{spa} improvement (see Figure 3.9.a)). Figure 3.10 shows the I_{on} as a function of the doping concentration into the epitaxy. It had been assumed that R_{spa} will be optimized for LT devices, and a high activation level for dopant located below the offset spacer (above 1×10^{20} at/cm^3) is thus assumed.

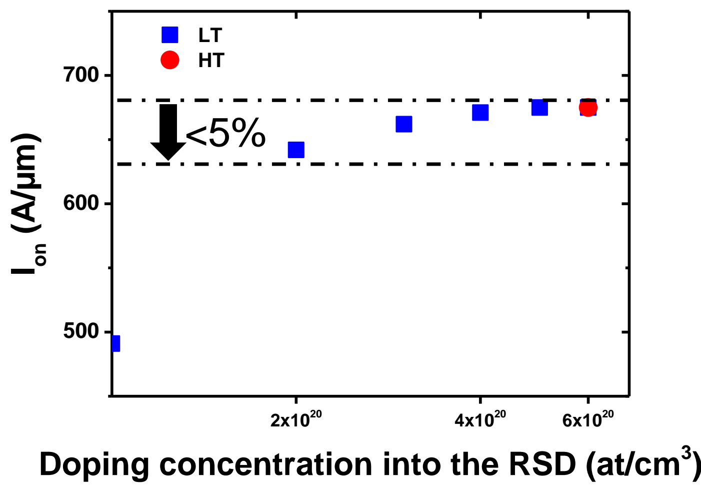


Figure 3.10: I_{on} versus the doping concentration into the RSD

The main difference on the I_{on} value is located in the transition of the activation level from 1×10^{20} at/cm^3 up to 2×10^{20} at/cm^3. When the activation level into the epitaxy is thus above 2×10^{20} at/cm^3, R_{epi} will be considered as satisfying in order to achieve high I_{on}. R_{epi} improvement has hence not been investigated in this work.

A degradation of the contact resistance by a factor 5 has been estimated by simulation for nMOS devices, due a different activation level in SiC:P epitaxy, with or without HT annealing. To overcome this issue without increasing the activation level, a shallow amorphizing implantation before salicidation might be done. It has been shown in [63] that using Ge amorphization before Ti silicidation lead to very low contact resistivity. More recently in [64], it has been demonstrated that using SPER before salicidation improves the R_{on} value by 23 % (respectively 30 %) for p FinFET

(respectively n FinFET), enhancing device performance by 17 % (respect. 13 %). SPER before salicidation can thus be viewed as a promising candidate to lower contact resistivity. This study might be considered as the next step after the reduction of the R_{spa},

As a conclusion, the previous study has shown promising results on low-temperature device performance thanks to the Extension First integration scheme. Especially for nMOS devices, dopants located below the offset spacer have not been activated via SPER process, and a fraction of dopants might additionally be deactivated due to nitrogen recoil. An optimization of Extension First integration scheme to overcome these issues on this specific area will be proposed in the following sections.

3.2 EXTENSION FIRST WITHOUT LINER

In order to improve the electrical performance (higher I_{on}/I_{off} ratio), it has been demonstrated in the previous section that R_{spa} should be minimized. Nitrogen and/or oxygen recoil during implantation steps should be indeed avoided. In this work, the advantage of implanting through bare silicon has been studied. It will be then proposed to integrate this technological solution into device fabrication.

3.2.1 Advantage to implant through bare silicon

Three morphological splits have been defined to evaluate the influence of a nitride capping and/or oxide liner in the silicon film. Implantations have been carried out through structures sketched in Figure 3.11. The first one, called ‘through nitride’ will be considered as the reference split, and corresponds to the LT split of the previous study, *i.e.* with the presence of 3 nm-thick SiN/0.8 nm-thick native oxide. The second aims at analyzing the influence of the oxygen recoil into dopant activation. In the last split, the goal is to implant into the silicon without any layer or contaminant that could deactivate dopants. A HF clean has been performed before implantation to suppress any native oxide, with a queue time inferior to one hour. Finally, the SiN liner of the first split has been measured by ellipsometry and is equal to 3.1 nm.

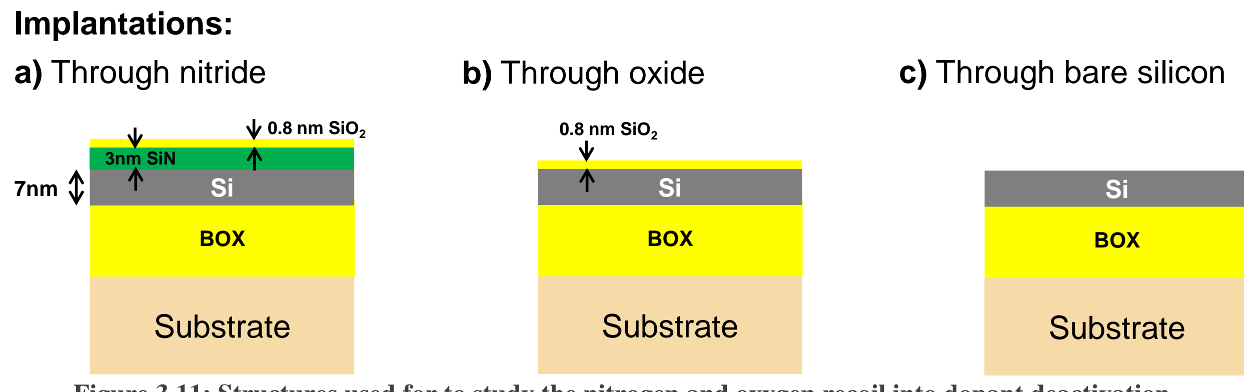


Figure 3.11: Structures used for to study the nitrogen and oxygen recoil into dopant deactivation

Implantations involved for the first structure corresponds to the No PAI and PAI splits of the previous study, respectively for n and p type. For the second and third splits, the implantation conditions have been defined via KMC simulations. An equivalent amorphization thickness and the same doping concentration have been defined between these two splits for a fair comparison of the experimental results. The clustering limits, defined at 6×10^{20} at/cm^3 for phosphorous and at 3×10^{20} at/cm^3 for boron in the previous work [9], have also been targeted as the maximum concentrations in order to avoid dopant deactivation. It is worth noticing that precise dose rate has also been taken into account simulation in order to better control the amorphization thickness (see the sub section 2.1.1 in chapter 2 for more details). TEM cross section pictures of n and p-type samples are shown in Figure 3.12, which correspond to implantations through bare silicon without annealing. The theoretical dopant profiles extracted by CTRIM simulations have also been superposed on the pictures.

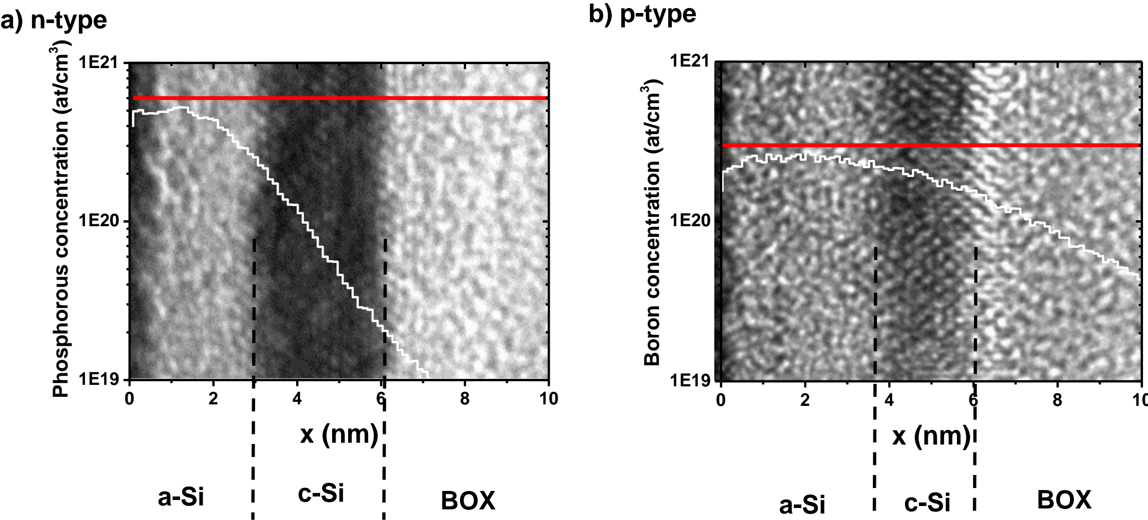


Figure 3.12: Dopant profiles and TEM cross section pictures after implantation (through bare silicon splits)

It can be seen from Figure 3.12 that between 2 nm and 3 nm of the silicon are left in a crystalline state, which is consistent with the simulations. The maximum dopant concentration does not exceed the clustering effect limit. For these conditions, the calculated sheet resistances should be around 1-2 kΩ/sq for n and p MOS devices (cf Figure 3.6.b)).

RESULT

Figure 3.13 shows the measured sheet resistances. This result is shown for both p and n type, after a recrystallization annealing of 600 °C/2 min.

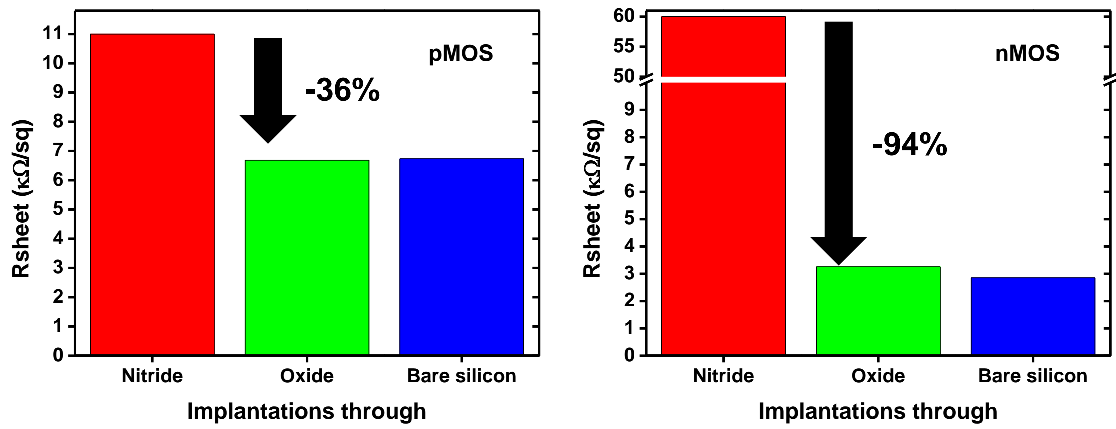


Figure 3.13: R_{sheet} results of p and n type, though nitride, oxide and bare silicon

Clear R_{sheet} improvement is observed for both n and p samples when implantations are performed without the thin liner. This improvement is thus interpreted as a higher activation level due to the suppression of the nitrogen recoil. No modification of sheet resistance is however observed for implantation trough a native oxide. The HF clean used to remove the native oxide is thus considered as not required.

The impact of nitrogen implantation on phosphorous (respectively boron) junction has been studied in [61] (respectively [62]), and the result will be compared with our study. Nitrogen-free implantations result in an improvement of the R_{sheet} of 200 % (respectively from 20 % up to 40 %) with a 600 °C/60 s (respectively 650 °C/60 s)-activation and for nitrogen concentration above 1×10^{20} at/cm^3. This suggests that P-N or B-N complexes had been produced. Our result for n (respectively p)-type sample with a 96 % (respectively 36 %) improvement is thus consistent with these studies. It is however worth noticing that our result shows higher sheet resistances in comparison to the expectation. Nevertheless, by using Figure 3.9, these values are below the maximum sheet resistance (10 kΩ/sq) and implanting through oxide or bare silicon is thus expected to improve access resistances of devices.

Additionally, the influence of native oxide on activation level through sheet resistance measurements has been performed in [25] on a 22 nm-thick Si film. A slight difference has been measured for both n and p type and after a 600 °C/2 min annealing. Our result is thus consistent

with this previous study, indicating that surface preparation does not seem to play a role in the SPER process for a 600 °C/2 min annealing.

3.2.2 Integration proposition

Implanting without the thin liner and before the epitaxy is hence compulsory to lower access resistances. A solution is thus to etch the first liner before performing implantation. The main step modification into the Extension First integration scheme is sketched in Figure 3.14.

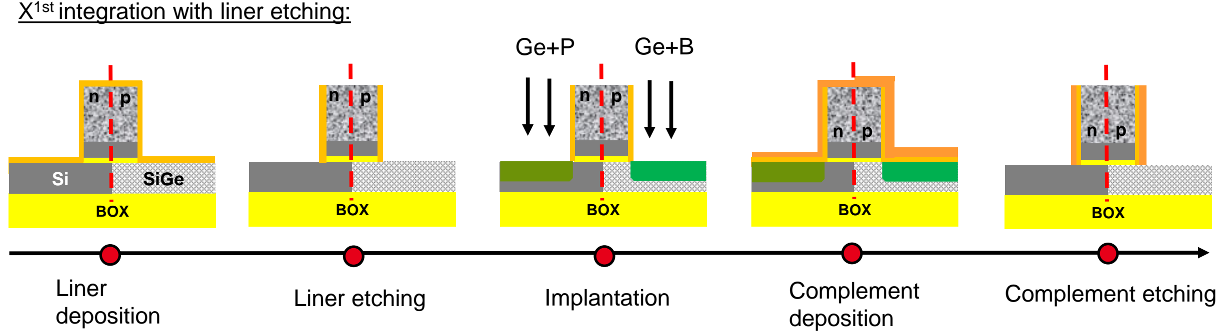


Figure 3.14: Main step modification into the Extension First integration scheme to implant without nitrogen recoil

It can be seen that, using this process, the liner is expected to be removed from the S/D, while remaining on the gate edge. Implantations are then performed through bare silicon, avoiding the nitrogen recoil. The complement liner is deposited then etched. Its thickness differs from p-type to n-type to allow a fair comparison with the HT POR. Compared to the original X^{1st} process flow, this integration scheme hence leads to an additional etch. As a consequence, a supplementary silicon consumption might be expected. This might lead to a thinner silicon film due to the supplementary etching. It has thus to be ensured that a minimum crystalline template remains after the offset spacer formation to be able to use the SPER process and to perform the epitaxy regrowth. Etching the thin liner should thus be optimized in order to lower the silicon consumption. Ellipsometry measurements have been performed before and after the thin etching for two etching recipes, and the silicon thickness (T_{si}) consumption due to these etching is plotted in Figure 3.15.

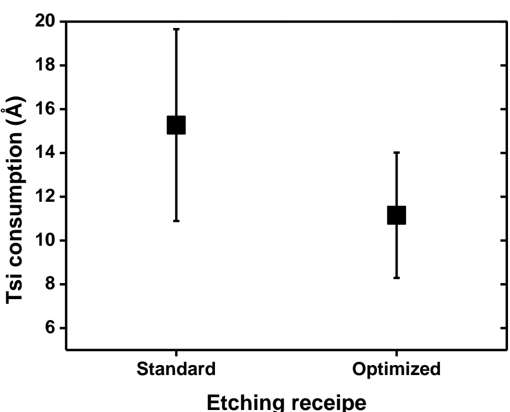
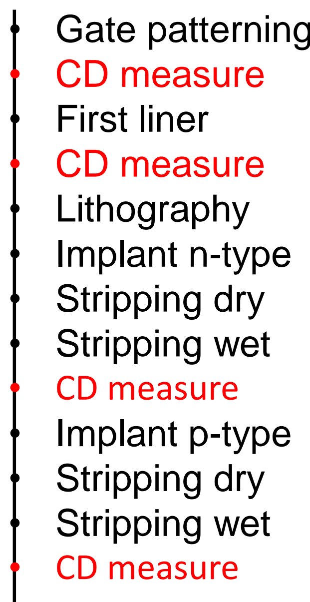


Figure 3.15: T_{si} consumption according the etching recipe

Thanks to an optimized recipe, the silicon thickness consumption as well as the standard deviation are reduced, allowing to efficiently reduce the influence of the supplementary etching on the device performance.

INTEGRATION LIMITATION FOR CMOS INTEGRATION

The first liner is 3 nm-thin and is unintentionally damaged during implantations. It might be hence consumed during the implant lithography stripping steps that occur for each MOS type. From the previous work with the original X^{1st} process flow [9], the consumption of the liner has been measured using a Scanning Electronic Microscope (SEM) measurement. The Critical Dimension (CD) of the gate has thus been measured at different steps (after the gate patterning, after the first liner deposition, after the n-type and p-type strippings). The different steps and are detailed in Figure 3.16.a), and the results of the monitoring are reported in Figure 3.16.b).



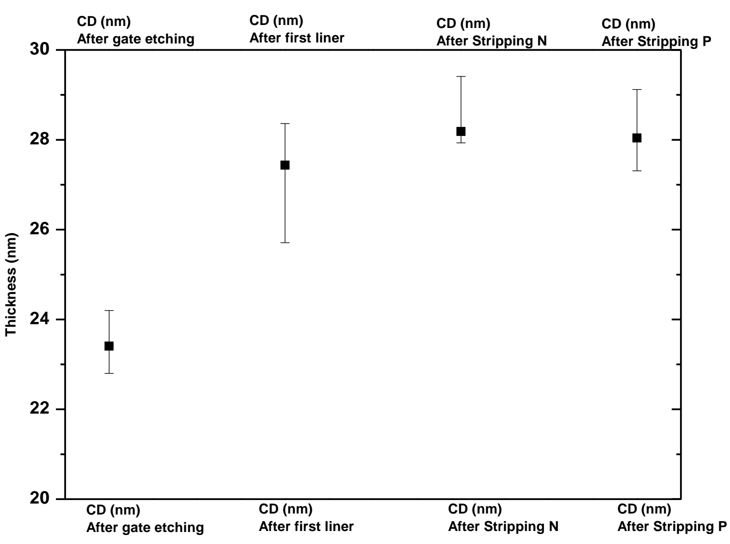


Figure 3.16: CD measurements during the process flow

According to the three last measurements, no consumption of the first liner has been observed. Processing devices with the original Extension First integration scheme is thus CMOS-compatible. However, the consequence of the additional etching, performed before the stripping steps, on the thin liner consumption has not be evaluated. A risk of consuming the metal gate is still possible, and for industrial interests, should be investigated.

X^{1ST}/GATE LAST

Another proposition that does not involved a supplementary etching is to implant before the offset spacer deposition without tilted angle. But without offset spacer, the metal gate will be exposed to implantations. The gate stack might be thus degraded, and implantation tools might also be contaminated, which is obviously undesired. In that case, using gate last integration scheme could be a solution. The main steps of the proposed process flow with Extension First/Gate Last integration scheme are sketched in Figure 3.17.

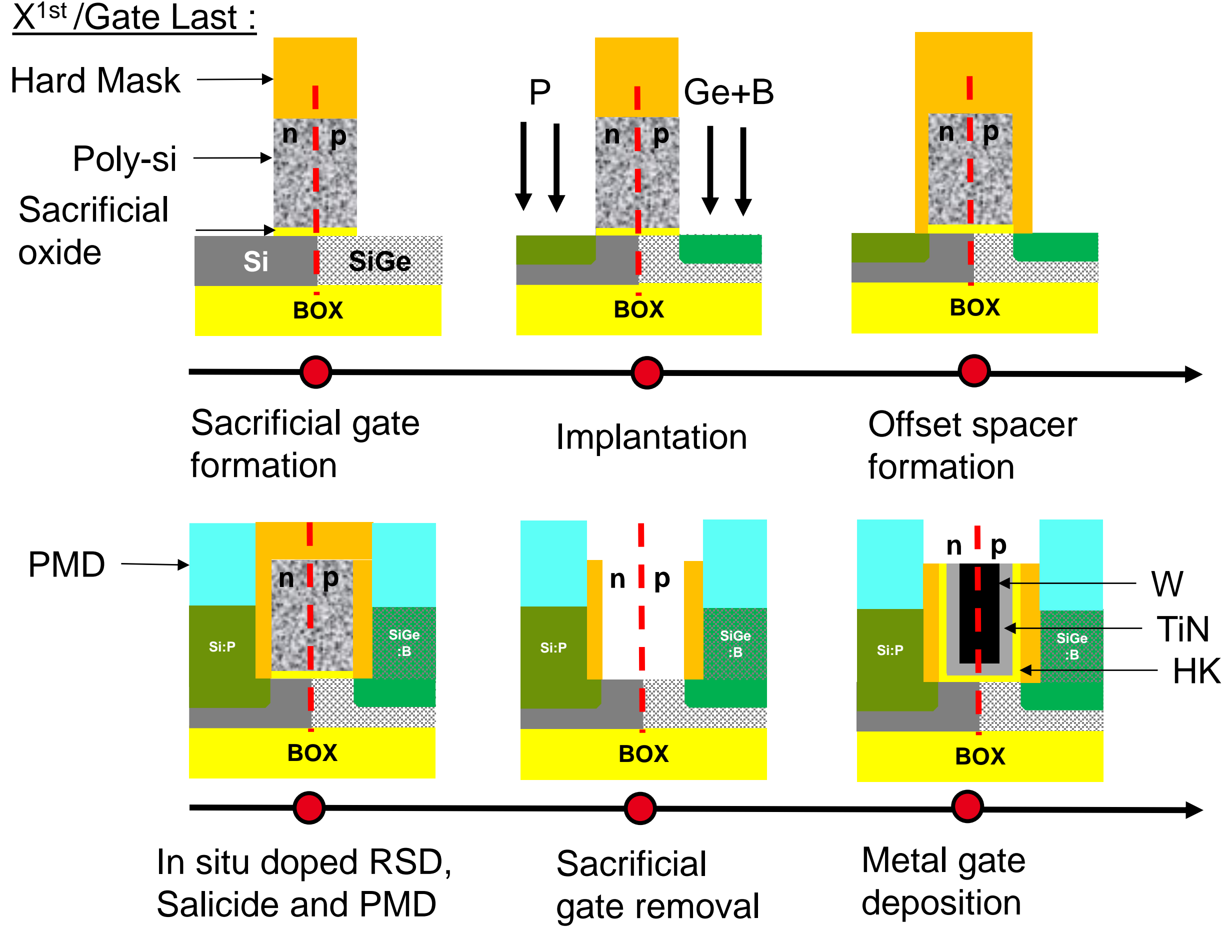


Figure 3.17: Main steps of the X^{1st}/Gate Last integration scheme

The sacrificial gate stack is composed of a sacrificial oxide, a polycrystalline silicon and a hard mask, which are then patterned to form the sacrificial gate. The oxide is used as an etch-stop layer when the sacrificial gate will be removed. The implantation steps are then performed. Junction with high activation level and aligned at the gate edge might thus be expected in that configuration. The offset spacer is then formed. On the access zone, an *in situ* doped raised source drain epitaxy is carried out. After the second spacer and the silicide formation (not shown here), PMD is deposited and planarized, using the nitride hard mask as a selective stop layer. The sacrificial gate is then removed, replaced by a High-K/metal gate stack, and is then planarized. This solution is expected to be CMOS-compatible, but at higher device cost.

As a conclusion, this section has evidenced the significant advantage to implant through bare silicon. This technological solution might be integrated into device fabrication, but to be CMOS-compatible, Extension First/Gate Last integration scheme seems to be more suitable, but at a higher device cost. Nevertheless, with this integration scheme, junctions should be perfectly aligned at the gate edge.

3.3 EOT IMPROVEMENT

In the section 3.1, the performance degradation between HT and LT had been attributed to access resistance degradation. It has been assumed that the EOT was constant with scaled gate lengths.

An EOT regrowth for the shortest length devices could however occur and this increase might be different for the high temperature and low temperature process. The original conclusions obtained on the performance degradation of LT process are hence reinvestigated in this section, accounting for this potential EOT regrowth.

3.3.1 Electrical measurements

In this in-depth investigation, the eventual EOT regrowth has been evaluated using, this time, both CV and IV measurements.

C-V MEASUREMENTS

CV measurements have been carried out at 90 kHz and shown on Figure 3.18. The EOT absolute value is obtained by fitting the curve between the measured capacitance and the simulated one, using [65]. The fits are shown on the same figure. The differentiation of CV values at fixed V_g for two close gate lengths enable to remove any parasitic capacitance and the gate length uncertainties compared to the mask dimension. Moreover, a 50-interdigitated transistor structure enables to measure the capacitance even for the shortest gate lengths. Figure 3.18 shows the C-V

measurements and the absolute EOT which is deduced for both n&p MOS. The differentiation has been carried out for the following couples of gate lengths:

ΔL_1 = 150 nm – 60 nm, and ΔL_2 = 26 nm – 24 nm.

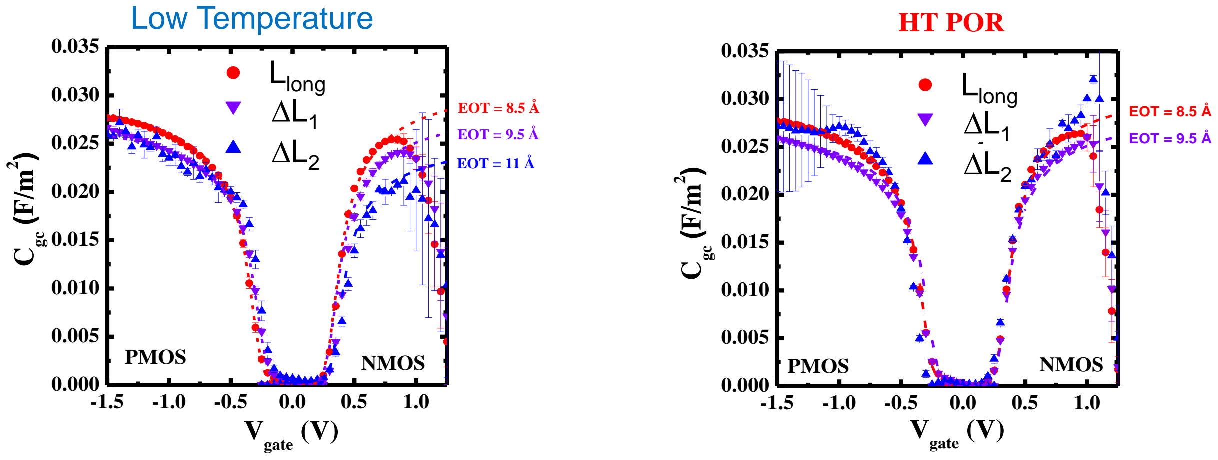


Figure 3.18: C-V measurements and extracted EOT for LT and HT devices

While for long channel the dispersion of the set of data is suitable for a correct extraction of EOT, the dispersion is too large for short channels, as shown by the large standard deviation. For the nMOS HT POR split, ΔEOT = 1 Å ± 1 Å, and for the nMOS LT No implant split, ΔEOT = 2 Å ± 1 Å. A conclusion about an EOT variation is therefore impossible using only CV measurement. In addition, for pMOS HT POR, the fit for the shortest gate length is impossible due to the large dispersion.

The problem of the large dispersion could be explained by the linear dependency of the oxide capacitance with the EOT and by a too large gate leakage. This variation is thus not satisfying to fully conclude about a potential EOT regrowth due to the LT process flow, and another method is proposed in this work.

I-V MEASUREMENTS

In the simple direct Fowler-Nordheim model, the gate current is linked to the EOT following equation (3):

$$I_g = W.L.A.e^{\left(-\frac{EOT}{B}\right)} \quad (3)$$

where A and B are constants depending on material parameters, but independent of the gate length L and the width W. Because of the exponential dependency, the measured gate current is expected to lead to a larger signal in case of EOT regrowth. It is however assumed here that any variation of the material parameters (like gate dielectric constant or effective masses) is interpreted as an EOT variation. The impact of such material variation will however be the same at the performance level.

To ensure an unbiased extraction, outlier data are at first removed by using Grubbs-Smirnov's statistical test [66]. Then, to avoid the impact of short channel effects, the gate current is measured at low drain voltage (V_d = 25 mV). In addition, to eliminate trap-assisted current leakage contribution, the gate current is taken at high V_g. Finally, as no gate resistance can distort the measurements as I_g^{max}<100 µA, the highest value of available gate voltage is taken, which is about 1.7 V. Figure 3.19 shows the average gate current density I_g^{lin} versus the gate voltage V_g measurements, for LT splits and for three gate lengths.

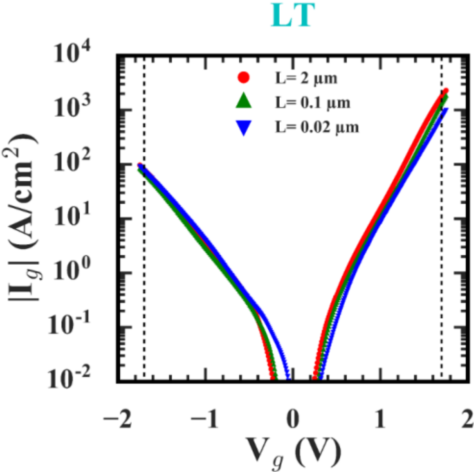


Figure 3.19: I_g-V_g for LT splits according to three gate lengths

The comparison of the averaged I_g^{lin} as a function of the gate length allows to identify if any degradation has occurred. This degradation could be explained by:

1) an EOT variation,
2) a difference between the mask and the effective channel length,
3) a difference of the potential between the overlap and the channel, which will impact the gate current in the same manner as 2).

These three hypotheses will be studied in the following paragraphs. At first, it has to be noted that with a lithography precision estimated around ±2 nm in the worst case scenario, the hypothesis 2) would lead at maximum to a 20 % degradation of I_g^{lin} for the shortest gate length. Then, assuming that there is no EOT regrowth and using the very simple direct tunneling model, 2) and 3) would influence the gate current according to equation (4):

$$I_g(L) = W.(L + \Delta L).A.e^{\left(-\frac{EOT}{B}\right)} + I_{g,overlap} \quad (4)$$

Using a differential method with respect to the gate length, would lead to equation (5), which becomes independent of the gate length:

$$I_g^{new}\left(\frac{L_2 + L_1}{2}\right) = \frac{\partial I_g}{\partial L} = \frac{I_g(L_2) - I_g(L_1)}{L_2 - L_1} = W.A.e^{\left(-\frac{EOT}{B}\right)} \quad (5)$$

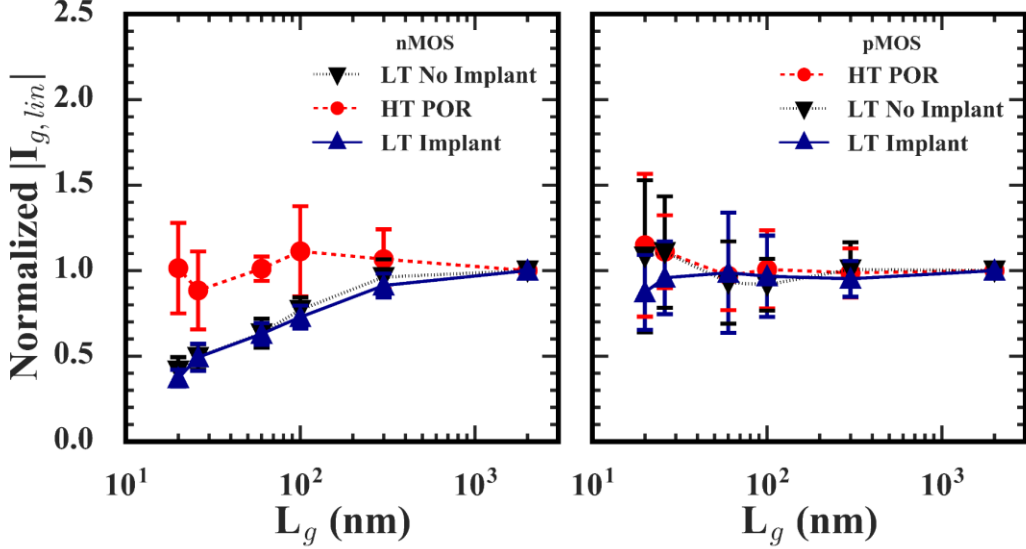
Therefore, if a monotonic gate current variation is caused by an extra gate length ΔL, applying the differential method would give an I_g^{new} parameters independent of L. On the contrary, if the gate current variation is caused by an EOT variation with L, the differential method would give I_g^{new} values still varying with L, according to:

$$I_g^{new}\left(\frac{L_2 + L_1}{2}\right) = W.A.e^{\left(-\frac{EOT(L)}{B}\right)}\left(1 - \frac{L + \Delta L}{B}\frac{\partial EOT(L)}{\partial L}\right) \quad (6)$$

In that situation, EOT(L) could be extracted simpler from the logarithm of I_g per unit area, if a value of B is known.

Figure 3.20.a) plots the I_g^{lin} per unit area, normalized with respect to the I_g^{lin} per unit area of the longest gate length, as a function of the gate length, for nMOS and pMOS devices of the HT POR and the LT processes. Figure 3.20.b) plots the result of the differential method described by equation (5) and (6) and is therefore based on gate current values but not divided by the gate length. The results of the differential methods are then normalized with respect to the value obtained for the longest gate length. The use of the differential method shown in Figure 3.20.b) is then used to clarify the origin of the previous results.

a) Classical method



b) Differential method

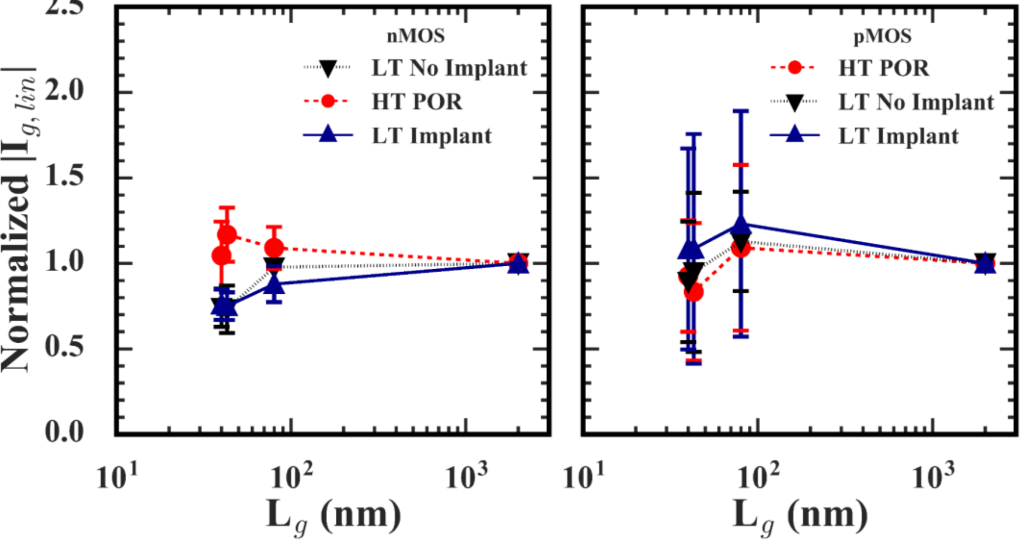


Figure 3.20: Normalized $I_{g,lin}$ vs L_g for both methods

For nMOS, the normalized I_g^{lin} of the HT POR is relatively constant, which clearly indicates a stable EOT or a very limited ΔL. A significant degradation however occurs starting from 300 nm for the LT splits, and larger than a factor 2 for the shorter gate length of 20 nm. For pMOS, the variation of the normalized I_g^{lin} is far less significant, and the variability in the value of I_g^{lin} is much

larger than in the nMOS case, as indicated by the errors bars (standard deviation of I_g^{lin} around its average).

As expected, the differential of I_g^{lin} for nMOS devices of HT POR is relatively constant, which clearly indicates a stable EOT and very limited ΔL. For the LT splits however, the differential is not constant, which indicates a degradation of the EOT, and not an impact of the ΔL.

The weakly varying values for pMOS confirm a weaker regrowth of the EOT. It can be noted that the presence of a source of variability strongly impacts the gate current with this method.

These results therefore suggest that it is possible to extract a value of ΔEOT from the logarithm of the gate current per unit area, if a value of B is known:

$$\ln(I_g(L_{Long})) - \ln(I_g(L)) = \frac{\Delta EOT(L)}{B} \tag{7}$$

COMPARISON

The value of B in equation (1) is highly dependent on the model of gate tunneling current considered. The simple FN tunneling model is convenient to separate the different contribution of the variation of I_g^{lin}, as highlighted in the previous section, but it suffers from too strong assumptions to be applied to the complex SiO_2/HfO_2 gate stack of the devices considered here. To obtain a better estimation of the B parameter, a more complete modeling of the tunneling gate current has hence been carried out using the scattering matrix formalism, assuming a 3D electron gas in the semiconductor [67][68]. The SiO_2 thickness has been varied from 2 Å to 4 Å and the HfO_2 one from 19 Å to 21 Å. The value of the SiO_2 effective mass has been set to 0.5 m_0, while the one of HfO_2 has been fixed at 0.165 m_0. The tunneling currents obtained with this approach are shown in Figure 3.21.

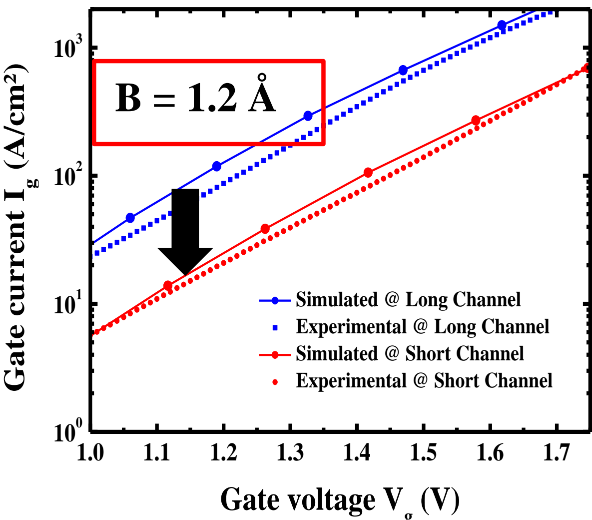


Figure 3.21: Comparison between simulated and experimental gate current for short and long gate lengths

A value of 1.2 Å has been extracted from these calculations for the B parameter. It will be used in the next section to deduce the resulting ΔEOT observed in LT nMOS devices.

ANALYSIS

The ΔEOT value, plotted in Figure 3.22, is hence deduced from equation (1). The value of B is obtained using the scattering matrix formalism.

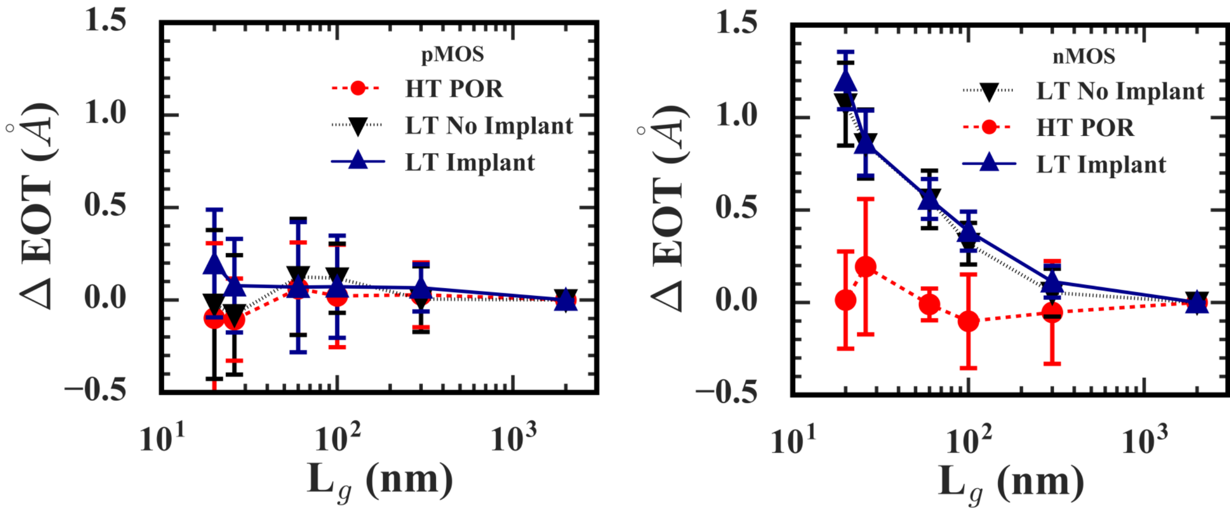


Figure 3.22: ΔEOT variation as function of the gate length

In the case of pMOS, no EOT regrowth has been found for HT POR and LT with a high precision of 0.4 Å. For nMOS, HT POR shows also no EOT regrowth, while for LT, a clear degradation of 1.2 Å ± 0.2 Å between short and long channel is observed. This degradation corresponds to a variation of 10 % of the EOT and could thus lead to 10 % I_{on} degradation, as I_{on} is inversely proportional to EOT.

The same gate stack has however been performed for both types of MOSFETs and could not thus justify the EOT regrowth. It could thus be attributed to an oxygen ingress coming from an oxidation of the thin liner. This ingress is expected to occur during the spacer complement deposition, which is made at 630 °C during 2 hours. Figure 3.23 sketches thus the mains step involved during this phenomenon.

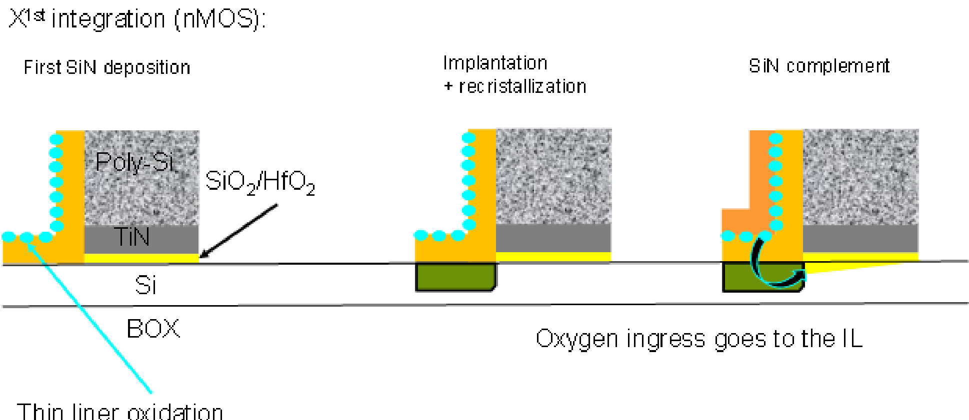


Figure 3.23: Illustration of the oxygen-ingress phenomenon

The thin liner oxidation is hence not linked to the implantation as the EOT regrowth is strictly the same of the LT splits, with or without implantation. The difference in EOT regrowth between n and p MOS LT splits can be explained by the fact that the latter is built on $SiGe_{27\ \%}$ channel and the oxidation kinetics in SiGe is lower than for Si [69]. To resolve this problem, a small reducing treatment could be applied before spacer complement deposition. This solution will be implemented in a further study.

To remember

From the previous study:

- Extension First integration scheme corresponds to an implantation performed before the epitaxy, at the gate edge.
- It enables to reach high performance for low temperature devices (95 % for pMOS, 90 % for nMOS) with respect to the HT POR.
- The doping of the region below the offset spacer has been identified as the main critical limitation for LT devices. Implanting through a nitride liner lead to nitrogen recoil in the amorphous region, and must be avoided.

In this work:

R_{spa} improvement

- A maximum R_{sheet} of 10 kΩ/sq must be obtained in order to reach the same R_{spa} than the HT POR.
- Avoiding the nitrogen recoil enables to improve R_{sheet} by a 94 % (respectively 36 %) for n-type (respectively p type) samples. All R_{sheet} values are below 10 kΩ/sq at 600 °C.
- To be CMOS-compatible, Extension First/Gate Last integration scheme seems to be more suitable, but will be more expensive to be manufactured. Nevertheless, junctions will be perfectly aligned at the gate edge

EOT improvement

- A method to extract EOT variation has been proposed, based on gate current measurement. This enables a more precise extraction of the EOT variation between long and short channel.
- To ensure unbiased extraction, it is advised:
    - to remove outlier data,
    - to measure the gate current at low drain voltage and high gate voltage,
    - to ensure that no gate resistance can distort the measurements.

- An EOT regrowth had been evidenced for nFETs, attributed to an oxygen ingress.
- To overcome this issue, a small treatment by HF cleaning before the spacer complement deposition might be applied.

4. LOW-TEMPERATURE FINFET INTEGRATION

It has been demonstrated in our previous study that low temperature devices are compatible to achieve high performance for FDSOI devices thanks to Extension First integration. In the previous chapter, deeper investigations have been carried out in order to improve these performances, by especially reducing the R_{on} value and the EOT regrowth via optimizations of the Extension First integration. It has thus be shown that the electrical performance of transistors are directly linked to the junction formation. In addition, in this chapter is proposed to increase even more the performances by fabricating FinFET devices with low thermal budget. To lower access resistances, embedded *in situ* doped raised source drain epitaxy (e-RSD) has been chosen today as the mainstream options to form junctions with dopant activated at high temperature. This process is however incompatible with 3D sequential integration, and a process flow with implanted junctions have been chosen. Different implantation configurations have been studied and analyzed in section 1.2 to dope the entire accesses, and a new scheme has been proposed, called Double SPER (DSPER), which consists in using twice the SPER process, one for each side of the accesses. Finally, devices have been fabricated with a thermal budget of 650 °C, as shown in section 1.3, by using, notably, e-RSD and DSPER. Further optimization have additionally given to achieve higher performances in section 1.4.

Contents

4. Low-Temperature FinFET integration 95

4.1 FinFET introduction 97

4.2 Finfet junction schemes 98

4.2.1 Defect-crystalline integrity 99

4.2.2 Angle restriction and conformal doping 101

4.2.3 Bending Fin 103

4.2.4 Embedded *In situ* doped raised source drain epitaxy 104

4.2.5 Description of the FinFET process flow 107

4.3 Proposition for Low Temperature devices 109

4.3.1 Horizontal Seed configuration 111

4.3.2 Central Seed configuration 112

4.3.3 Lateral seed configuration 113

4.3.4 The Double SPER configuration 114

4.4 Fabrication and Electrical characterization 122

4.4.1 Process flow modification 122

4.4.2 Electrical results 126

4.4.3 Non-recrystallization default 132

4.4.4 Straggle and EOR density diminution 134

4.4.5 Strain effect 139

4.5 Perspective on potential integration schemes 141

4.5.1 Summary of integration schemes 152

4.1 FINFET INTRODUCTION

As especially observed in the chapter 2, the device performance for scaled gate lengths is degraded by the short channel effects. These effects are due to the loss of the electrostatic control by the gate on the channel. One way to overcome this issue is to reduce the active zone width, and its thickness is simultaneously increased in order to maximize the drive current of such devices. The active zone is hence called fin in reference to its shape, and devices built in this configuration are called FinFETs. The geometry difference between planar and Fin FETs on SOI is shown in Figure 4.1 (the spacers and epitaxial regrowth are not represented for the sake of understanding).

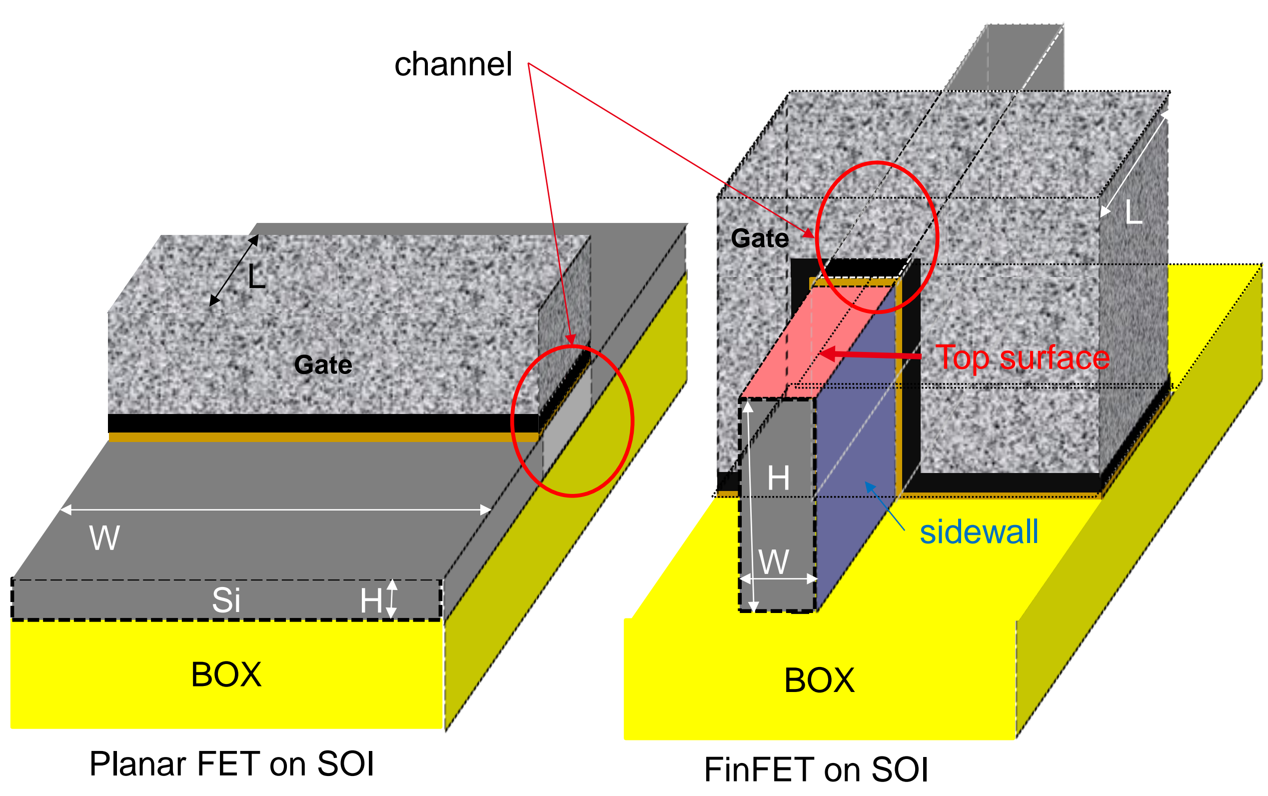


Figure 4.1: Planar and Fin FETs on SOI architecture.

It can be seen on Figure 4.1 that contrary to FDSOI devices, FinFETs are inherently 3D, with the gate surrounding the channel, while the gate is only 2D in a FDSOI device. Thanks to an

active zone both narrower and thicker, the charge in the channel for Fin FET is controlled by the gate at the top and at the side, which maintains a suitable electrostatic coupling.

The electrical characteristics of transistors are furthermore directly linked to the junction formation [70], and the access zones will be thus deeply investigated in this chapter. In the early steps of the FinFET development, well-established and conventional ion implantation beam line and furnace annealing have been used to dope and activate source and drain. Doping implantation and activation have however been challenging to achieve high performance for FinFET devices [71], [72], as exposed in section 4.2.

4.2 FINFET JUNCTION SCHEMES

The entire access of the fin should be indeed doped [70], [71], [73]. To fully activate the access zones of FinFETs, many strategies have been used by varying the angles of the ion implantation beam line. The beam line may be indeed oriented according two angles, which are conventionally called tilt θ and twist α. The tilt is the angle between the beam line and the normal to the surface of the wafer, while the twist is the angle between the projection of the beam line on the wafer and the line passing through the notch and the center of the wafer. Two beam line configurations with two different tilt (0, 45°) for the same twist (90°) are represented in Figure 4.2.a) and.b), respectively. The sectional view from above of the wafer and devices used in this study is also shown in Figure 4.2.c). This work is carried out in the standard orientation, i.e. the substrate is oriented according the (100) crystalline plane, while the gate is oriented according the (110) crystalline plane, as shown in Figure 4.2.c).

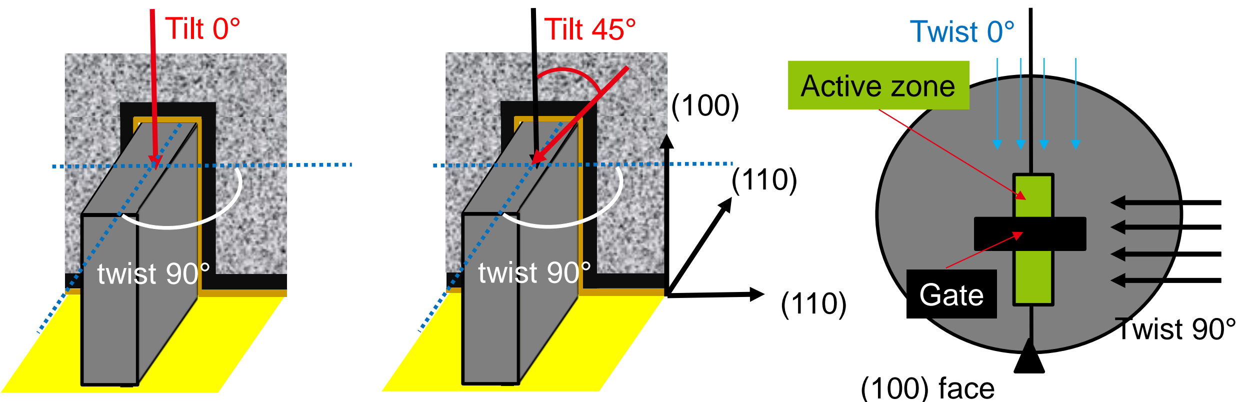


Figure 4.2: Implantation-angle definition for this work

In the following work, two configurations will be regularly considered, called tilted and non-tilted implantations. These configurations are represented in Figure 4.2 , without (Figure 4.2.a) or with (Figure 4.2.b) tilted implantation, with a fixed twist at 90° and 270° when two implantations is mandatory.

The following section will first highlight three challenges to dope the entire fin by implantation.

4.2.1 Defect-crystalline integrity

The first issue concerns the crystalline integrity of the fin, which has been underlined for non-tilted implantations. In this configuration, the implantation energy has indeed to be high enough in order to dope the entire fin height, leading to an undesired amorphization through the fin. For example, Figure 4.3.a) depicts a TEM picture of the width cross section of a fin from [74]. In Figure 4.3.b), a rapid thermal annealing at 1050 °C has been performed, and polycrystalline silicon is observed at the top of the fin. This configuration is thus known to lead to defective recrystallization.

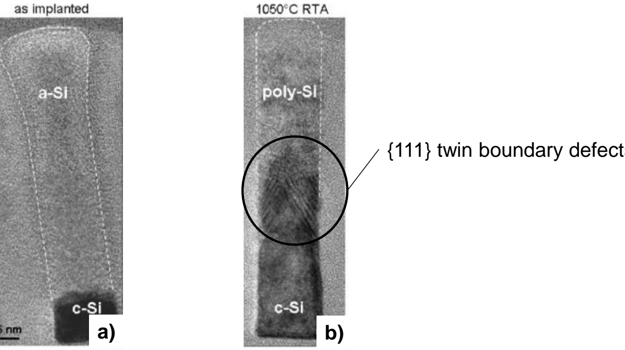


Figure 4.3: TEM picture from [5]. Due to the surface proximity, new recrystallization fronts appear, and can cause defect formation.

Due to the 3D structure of the fin and the surface proximity, solid-solid transition is delayed [74] and Random Nucleation and Growth (RNG) may thus occurred, leading to the polycrystalline silicon formation observed in Figure 4.3.b) and also shown in [74]–[77]. It has been additionally observed in [74] that, in this configuration and with respect to the conventional crystalline orientation, only 25 nm of the amorphous layer can be recrystallized before RNG occurred.

Besides, the amorphized zone is thicker as the doping specie is heavier. This amorphization issue is thus more critical for nMOS devices, which are usually doped with phosphorous or arsenic atoms, than for pMOS ones, doped with boron atoms. In other words, access resistances for n-type devices are expected to be more degraded than for p-type ones [72].

In addition, due to the fin width and to the crystalline orientation, {111} twin boundary defects are visible in the regrown region, as observed in Figure 4.3.b). They originate from both right and left side surfaces, at the Si-SiO_2 interface [74].

As a consequence, it appears that doping the entire fin might be very challenging with this approach, especially for nFET devices.

To overcome the undesired amorphization, instead of implanting at room temperature, several study has shown the interest to heat the wafer during implantation. The dynamic annealing is indeed enhanced by increasing the wafer temperature, leading to increase the mandatory dose to amorphized the silicon. In other words, TEM cross section pictures and electrical characterization in [78], [79], [11] highlight crystalline silicon without twin boundary defect remains thanks to such

an implantation technic, improving I_{on} value. However, hot implantation will create more defects, leading to degrade carrier mobility, especially for pMOS devices [9]. For low temperature devices, SPER will be used, and amorphization is thus compulsory. By using hot implantation, a post amorphization implant is hence mandatory, leading to the same default as previously described. This option has thus been discarded for low-temperature FinFETs in this work.

4.2.2 Angle restriction and conformal doping

Non-tilted implantation is hence not sufficient enough to activate dopants without defect formation. Tilted implantation can be used to implant dopants in the sidewalls, using thus lower energies and thereby smaller amorphized thickness. Another issue occurred however for this configuration. All angles are indeed not suitable to achieve high performance by lowering the access resistances, due to simple geometrical considerations. This is illustrated in Figure 4.4, with the dimensions of the 14 nm FinFET technological node of the reference in [80]. Figure 4.4.a) represents FinFETs on the same doping type, while Figure 4.4.b) sketches FinFETs of CMOS types in a SRAM configuration.

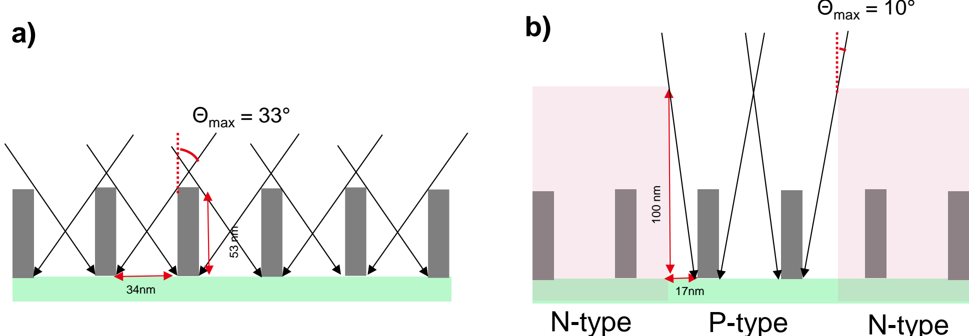


Figure 4.4: Angle restriction for tilted implantation for a) unipolar and b) N|P transition region (SRAM configuration)

In this example, the maximum allowed angle able to implant the entire fin is 33°. This angle restriction is due to the tight pitch between devices and the fin geometry. In this configuration, the fin bottom is not implanted beyond this maximum angle, and access resistance would be thus

degraded. For CMOS devices in a SRAM cell, as depicted in Figure 4.4.b), this maximum angle is even reduced to 10°, due to the photoresist thickness [71]. Besides, dopants might be backscattered at low energy [81], [82] because of this angle restriction. For example, only 10 % of the total active dopant concentration is retained at the sidewall with 10°-tilted angle in [81]. It is also worth noting that using twice tilted implantation would lead to dope more the top fin than its bottom. Data of reference [83] and [84] enable to have the measure of the impact of this angle restriction: the I_{on} value of devices without conformal doping might be lower by around 25 % and a 20 % drive-in current degradation has been observed for boron implantation when going from 45° to 10° tilt.

To overcome this issue, Figure 4.5 represents an alternative to the angle restriction, by implanting only one side on each fin.

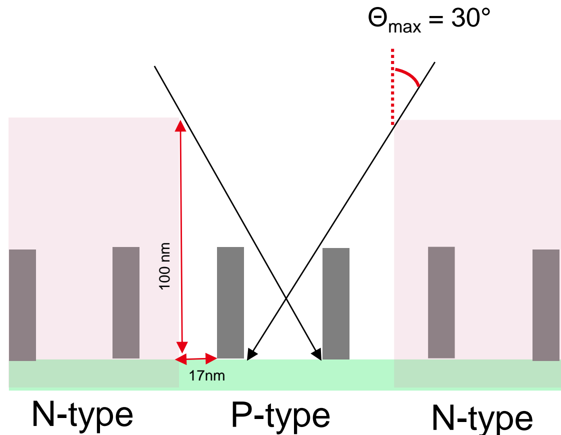


Figure 4.5: Illustration of the single-sided implantation

While the maximum allowed angle is expanded from 10° to 30°, the fin is however still not fully doped, and lower drive-in current has then been observed in [73] in comparison to the double-sided implantation.

Another solution might be to use a Hard Mask instead of a photoresist. By selecting the proper material, it might be foreseen that the mandatory thickness could be drastically decreased. Figure 4.6 shows the consequence of choosing a 60 nm-thick Hard Mask instead of a photoresist.

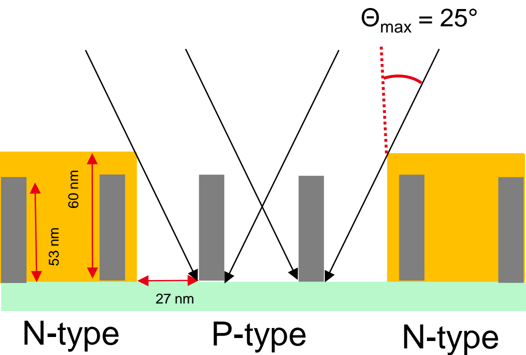


Figure 4.6: Hard Mask utilization to improve the angle restriction

By reducing the thickness of the photoresist, the maximum achievable angle will be improved to 25°, but it will be at the detriment of the fabrication cost. A hard mask is indeed more expensive to use than a photoresist.

ALTERNATIVE IMPLANTATIONS

Due to these issues, alternative implantations have been studied, such as doped-silicate glass doping [71], [72], molecular monolayer doping or vapor phase doping [3]. But a high temperature process is intrinsically mandatory for all these alternatives, to activate and/or to diffuse dopant, which is hence not compatible with 3D sequential integration.

An interesting alternative that does not required a thermal activation or diffusion and avoid the shadowing effect is the plasma implantation, which enables a 3D doping activation and enhances conformal doping [85]. In [84], 15 % gain on the I_{on} value has been found with a standard activation (thermal annealing), thank especially to a lower access resistance. This technics is furthermore compatible with low thermal activation.

4.2.3 Bending Fin

The third issue is caused by the structure of the fin. Indeed, to achieve high performance, i.e. to reduce short channel effects and to increase the drive current, the fins are becoming narrower and higher. This high aspect ratio weakens the fin integrity, when stress effect is applied during process fabrication. For example, fin bending might be induced during STI formation [86], or by

depositing a capping layer on multiple fin with a tight pitch [87]. It is worth noticing that few data has been found on this subject, while it might considered as one of the most critical issue for the most advanced nodes.

4.2.4 Embedded *In situ* doped raised source drain epitaxy

In order to have a conformal doping in the access zone and to avoid damage due to implantations, the integration of embedded *in situ* raised source drain (e-RSD) has been proposed [88] and might be view as the standard option to lower access resistances. Figure 4.7 sketches the main steps of a FinFET process flow with this integration.

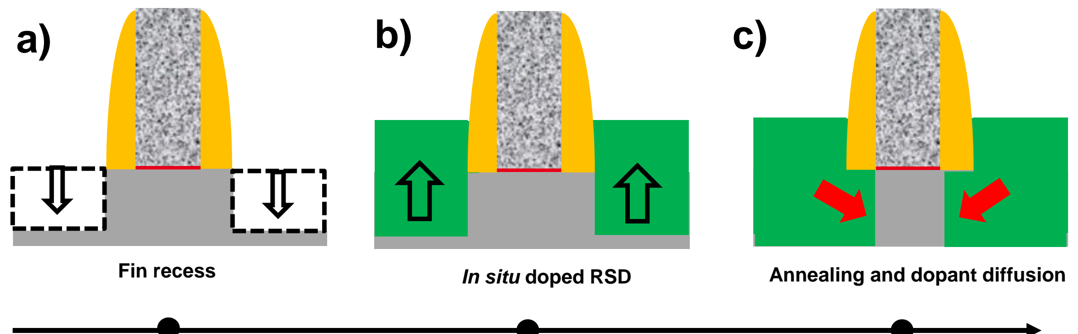


Figure 4.7: Main steps of a FinFET flow with embedded *in situ* doped raised source drain epitaxy

After the offset spacer formation, the access zones of the fin are recessed (Figure 4.7.a) and *in situ* doped raised source drain epitaxy is performed (Figure 4.7.b). A rapid thermal annealing (Figure 4.7.c) is then carried out to drive dopants under the offset spacer in order to lower the access resistances. An additional source of interest for embedded *in situ* doped raised source drain epitaxy comes from their ability to improve mobility thanks to strain like SiGe for p-type or SiC for n-type [71],[89]. For p-type devices and on bulk substrate, strain effect with fin recess has been investigated by lattice kinetic Monte Carlo and TCAD simulation [90]–[92]. I_{on} improvement of 13 % [93] up to 25 % [88] has been observed in comparison to splits without stressors and non-embedded raised source drain. This improvement is linked to the conjoint effects of a R_{access}

reduction (more effective source drain doping) and a mobility increase (strain effect). Using embedded *in situ* doped raised source drain epitaxy might be thus a good option to lower access resistance for high temperature devices, as well as for low temperature one. The activation of dopants can be indeed obtained below 500 °C contrary to other implant techniques previously discussed. J. Aubin *et al* in [95] have shown for example the feasibility of a selective SiGe:B regrowth at 450 °C.

E-RSD FOR LOW TEMPERATURE FINFETS

At low temperature, no or few doping diffusion is expected, and the region below the offset spacer would not be doped with only a vertical recess followed by an *in situ* doped epitaxy. Since it has been concluded that doping this region is compulsory to obtain low R_{access} values [57], using only epitaxy to lower access resistances of low-temperature devices requires to add another step to consume the region below the offset spacer. For example, the cavity can be obtained with silicon oxidation/desoxidation cycles, as described in Figure 4.8.

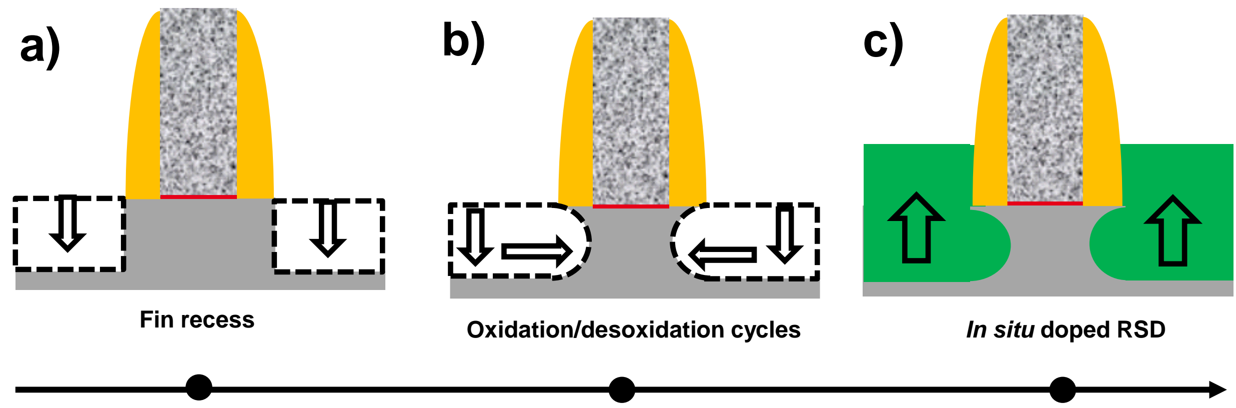


Figure 4.8: Main steps of e-RSD with for thermal-budget devices

pMOS FinFETs with this additional lateral recess have been fabricated. More specifically, with the process flow described in the next sub section, splits have been defined with or without oxidation/desoxidation cycles, after the fin recess, but still before the *in situ* doped epitaxy. It is worth noticing that these devices have been submitted to a spike annealing. These cycles have been tuned to etch 8 nm of crystalline silicon, in order to keep a sufficient crystalline silicon seed for the

epitaxy. Figure 4.9 shows two TEM pictures in the gate-length direction of such devices, without (Figure 4.9.a) or with (Figure 4.9.b) the oxidation/desoxidation cycles.

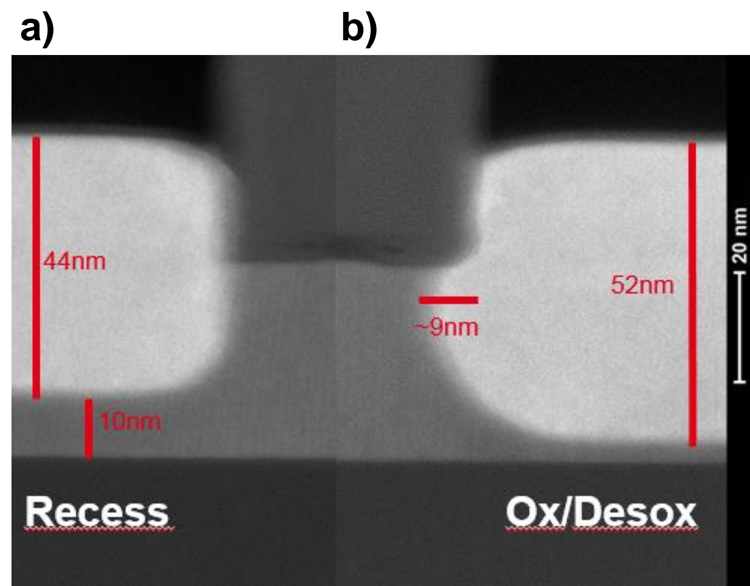


Figure 4.9: TEM cross section pictures of HT e-RSD FinFET with or without oxidation/desoxidation cycles

The oxidation/desoxidation cycles enable to etch right under the offset spacer. It is worth noticing that for the split with oxidation/desoxidation cycles, the doped epitaxy is deeper in comparison to the only-recessed one. This will thus lead to an additional gain in the access resistances.

The hole mobility and access resistances have been extracted for these two splits via the Y-function method [96] on 80 nm-wide isolated devices, for gate lengths from 80 nm to 10 µm, and is plotted in Figure 4.10.

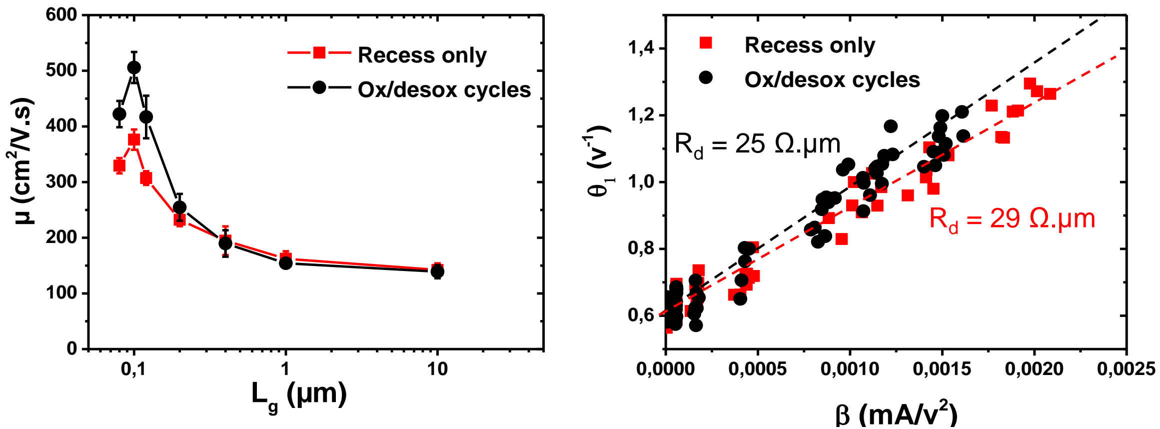


Figure 4.10: R_{access} and hole mobility with and without oxidation/desoxidation cycles

The access resistance of devices with oxidation/desoxidation cycles is 14 % smaller in comparison to the recessed-only ones, and is attributed to a deeper doped epitaxy. In addition, a better stress effect is observed with the oxidation/desoxidation cycles.

As a conclusion, using e-RSD with oxidation/desoxidation cycles should be possible to manufacture low temperature FinFETs, but will not be investigated in the following sections.

4.2.5 Description of the FinFET process flow

For this study, high temperature devices have been fabricated. The main steps of the process flow are described in Figure 4.11. It includes gate last module, embedded *in situ* doped raised source drain epitaxy and self-aligned contact.

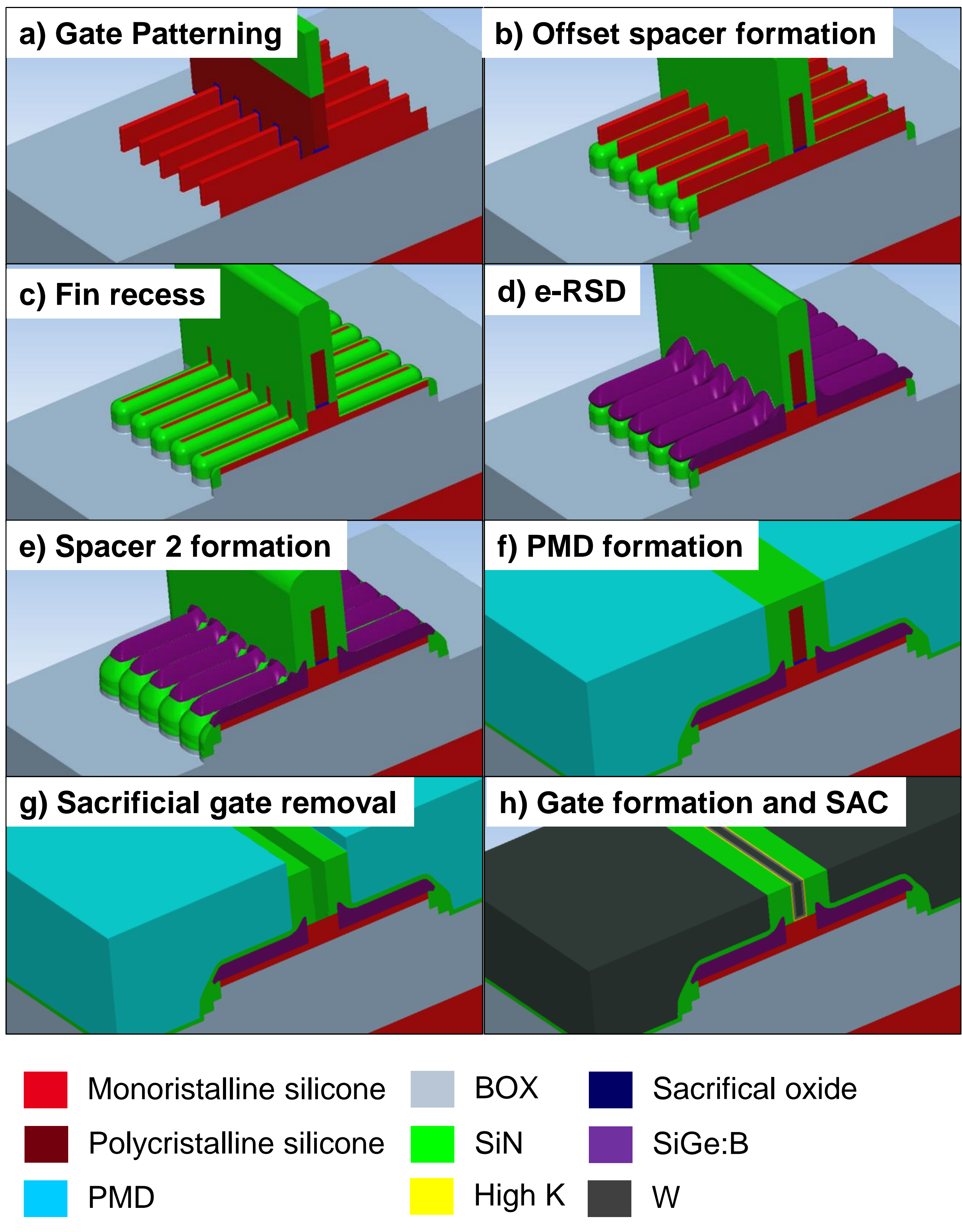


Figure 4.11: Mains steps of the FinFET process flow

The active zone is patterned in SOI wafers with (100) surface orientation, with a 33 nm-thick Silicon on 145 nm-thick Buried Oxide. The sacrificial gate stack is composed of a 4 nm-thick oxide, a 70 nm-thick polycrystalline silicon and a 90 nm-thick Hard-Mask SiN, which are then patterned to form the sacrificial gate (Figure 4.11.a). The oxide is used as an etch-stop layer when the sacrificial gate will be removed. A 10 nm-thick Si_3N_4 is then deposited and etched (Figure 4.11.b) to form an offset spacer. On the access zone, a 23 nm-thick recess is carried out by dry etching (Figure 4.11.c), followed by a 35 nm-thick epitaxy of SiGe:B, with a maximal thermal budget of 650 °C (Figure 4.11.d). A spike annealing at 950 °C is then used to activate and diffuse dopants below the offset spacer. A 15 m-thick Si_3N_4 spacer is formed (Figure 4.11e) and a 6 nm-thick CESL is deposited, followed by a PMD deposition and planarization, using the nitride hard mask as an etch-stop layer (Figure 4.11.f). The sacrificial gate is removed, replaced by a HfO_2/TiN/W stack, and is then planarized (Figure 4.11.g). Then, the PMD and CESL are removed from the active zone in order to silicide the accesses. 5 nm-thick NiPt is deposited. Then W is deposited on the active zone (Figure 4.11.h) followed by a standard Back End Of Line. In this gate last integration, the thermal budget endured by the gate stack after its formation is inferior to 500 °C.

4.3 PROPOSITION FOR LOW TEMPERATURE DEVICES

As shown in the previous chapters, SPER has been found to be a good candidate to activate dopants for low temperature integration. In order to use the solid-phase epitaxy regrowth of an amorphous layer, a crystalline seed is required to be able to recrystallize the amorphous layer. Contrary to the high temperature schemes, here an amorphization is desired and three seed configurations have been studied in this thesis. In order to choose the most appropriate configuration to lower the access resistances, these configurations have been simulated, using the commercial tool Sentaurus SDEVICE, and compared via the R_{on}-DIBL figure of merit. A FinFET following the gate length direction is depicted in Figure 4.12.a) and the width cross section of a

FinFET in the access zones with the different seed schemes is sketched in Figure 4.12.b). The simulations consider a fully activated junction at the gate edge with the doping concentration at 2×10^{20} at/cm^3 in the access, and is added in Figure 4.12.a). The geometries used for these simulations are also represented in Figure 4.12. The simulated FinFET is 7 nm-wide, 35 nm-tall and 20 nm-long, which represents devices of 14 nm node.

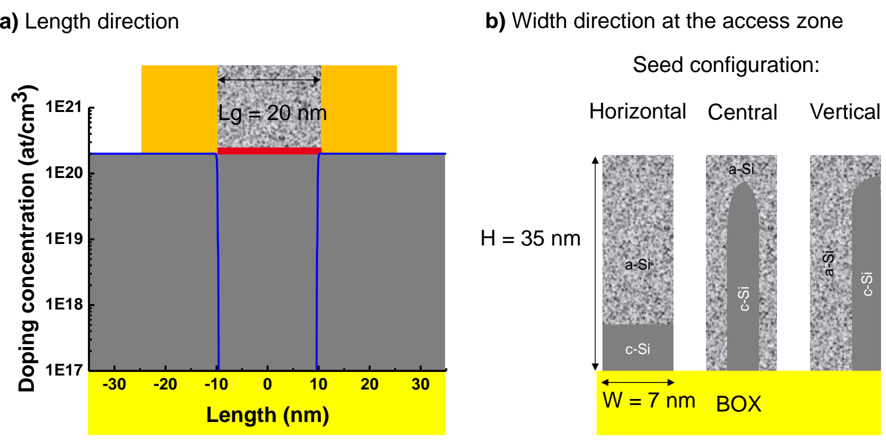


Figure 4.12: Structure used for simulations

Following the length direction (Figure 4.12.a), the doping-concentration profile represents the ideal case of a junction doping. The doping-concentration profile is thus constant until the gate edge and abruptly fall. No overlap or underlap configuration is thus taken into account here. Following the width direction, the profile has been defined constant, equal to the maximum concentration. At low temperature, beyond a critical doping concentration, clustering effect might appeared, which limits the dopant activation or reduce the carrier mobility. For example, this effect has been observed for boron concentration beyond 3×10^{20} at/cm^3 [96]. To avoid this effect, the maximum concentration has thus been targeted at 2×10^{20} at/cm^3. In Figure 4.12.b) is shown the 3 investigated seed configurations, respectively called horizontal, central, and lateral seed. As described in chapter 2, at least 3 nm of the access should remain crystalline, in order to use this one as the seed. In these simulation, no difference between a higher activation due to SPER activation in comparison to a thermal activation has been taken into account, to be able to rely about the interest of each configuration.

For the central and the vertical seed configurations, geometrical variation such as the line width roughness and amorphous/crystalline interface roughness should be taken into account in order to give the maximum value of the to-be-targeted amorphized depth. The process window of the resulting interface roughness might be estimated to null, because these configurations will involve low-dose, low-energy implantation, and because ionic implantation is a well-known, well-controlled technique. This is highlighted in Figure 4.13, which is the focus of two TEM pictures of the fin-width cross section where two amorphization conditions are led to amorphize 6 or 2 nm of the fin. In both cases, the amorphous/crystalline interface might be considered as without roughness.

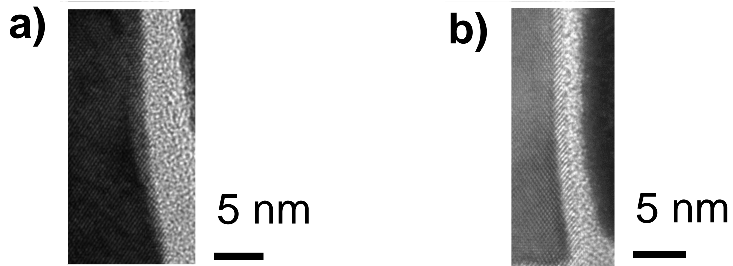


Figure 4.13: TEM pictures of the fin-width cross section after two amorphizing implantations

In [97], it has finally been concluded that the line width roughness is inferior to 1 nm, which will be thus our target concerning fin variation.

4.3.1 Horizontal Seed configuration

Using a non-tilted amorphizing implantation has been at first investigated and the bottom of the fin acts thus as the horizontal crystalline seed. Figure 4.14 shows the TCAD electrical simulation and the relevant parameters used for the simulations. The fin before and after the crystalline regrowth with vertical implant is sketched in Figure 4.14.a). In addition, the thickness T_{seed} of the crystalline seed is depicted in this figure and this zone of the fin has been considered non-doped, being thus representative of the fin thickness where the doping will not be activated

after the recrystallization. The resulting simulated R_{on}-DIBL trade-off with different crystalline seed thicknesses is displayed in Figure 4.14.b).

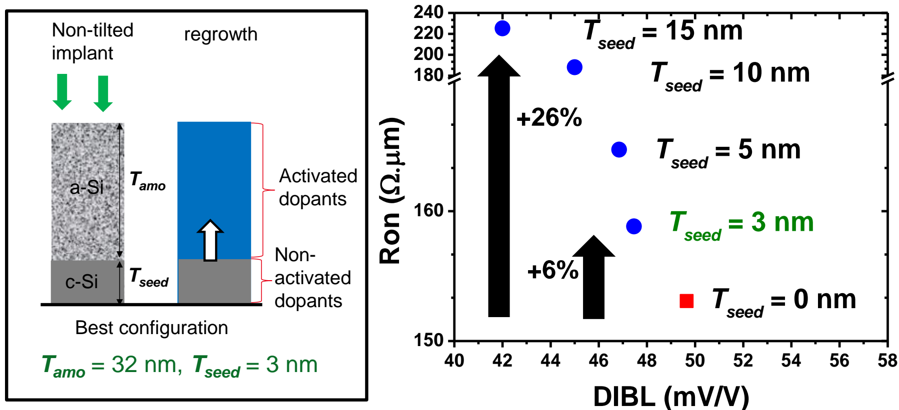


Figure 4.14: R_{on}-DIBL trade-off for the horizontal-seed configuration, for different seed thicknesses

In Figure 4.14.b), while only a slight decrease on the DIBL value is observed, the best R_{on} value is yielded by the thinnest seed. For example, a 6 % increase on the R_{on} value is induced when using a 3 nm-thick seed, compared to a full activation (T_{seed} = 0 nm). To lower the access resistances, this configuration might thus be considered as a good option, but it has been shown in [74] that at low temperature, twin crystal defects will also be present and lead to a partial recrystallization. A higher degradation is thus expected by using this scheme and is thus not adapted to achieve high-performance FinFETs.

4.3.2 Central Seed configuration

Using a double-sided tilted amorphizing implantation has then been investigated. The core of the fin has been aimed to act as the crystalline seed. The edges of the fin are thus amorphized and then recrystallized, enabling to activate the doping in the previously amorphized zone. Figure 4.15.a) summarizes this configuration, before and after the crystalline regrowth. For a 7 nm-wide fin, to be able to recrystallize the amorphous layer, a 2 nm-thick amorphization for each fin side is

defined as the best configuration, leaving thus a 3 nm-thick crystalline seed at the fin core. In this simulation, the influence of the amorphization thickness T_{amo} has been studied. Figure 4.15.b) is the resulting R_{on}-DIBL trade-off, with different amorphization thicknesses.

It is worth noticing that, for this scheme, beam line implantation is not exclusive, and using plasma implantation might be a good candidate to amorphize and to conformally dope the surrounding of the fin

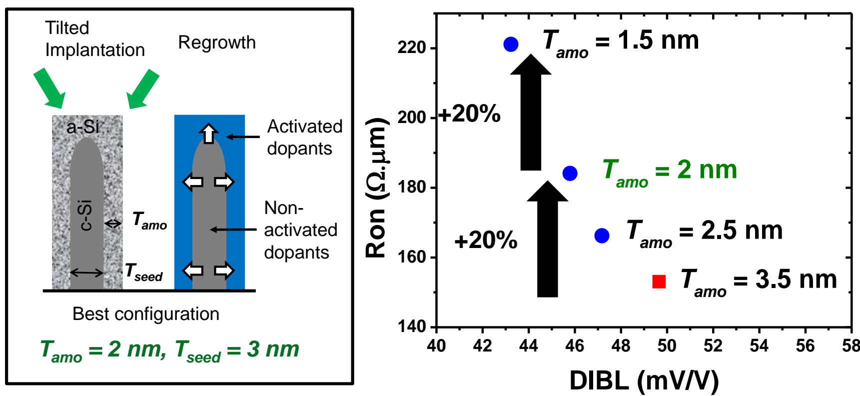


Figure 4.15: R_{on}-DIBL trade-off for the central-seed configuration, for different amorphization thicknesses

It can been noticed that a small decrease of the amorphization thickness of 5 Å results in a significant increase of the R_{on} value of 20 %. In order to use this scheme, the fin width, the line width roughness and amorphous/crystalline interface roughness should thus be precisely controlled to obtain an acceptable variation into the R_{on} value, according to our simulations. In addition, even the best configuration (T_{amo} = 2 nm) leads to a 20 % R_{on} degradation compared to a full activation case. This scheme hence suffers from unsuitable process variability and R_{on} degradation and cannot be considered as an option to achieve high performance for low temperature.

4.3.3 Lateral seed configuration

To overcome the issues of the two first seed schemes, another scenario is studied, which consist in using a single-sided tilted amorphizing implantation. Only one side of the fin is thus

amorphized and then recrystallized, leaving the other side in a crystalline state in order to act as the seed. The regrowth will therefore be lateral from one side to the other, as illustrated in Figure 4.16.a). The lateral-seed thickness T_{seed} has been varied in the simulations from 3 nm down to 1.5 nm. The electrical simulations have thus been carried out with this scheme, and Figure 4.16.b) shows the resulting R_{on}-DIBL trade-off.

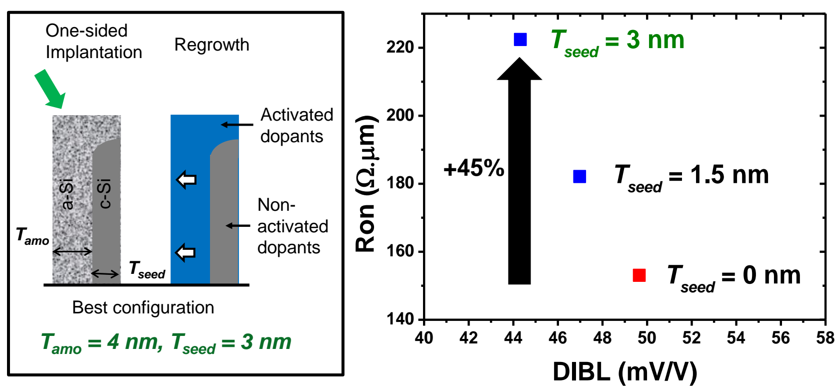


Figure 4.16: R_{on}-DIBL trade-off for the lateral-seed configuration, for different seed thicknesses

It can observed than the minimal crystalline seed thickness leads already to a 45 % R_{on} degradation compared to a full activation (T_{seed} = 0 nm), because in that configuration the fin is only half-doped. In addition, even a thinner seed (T_{seed} = 1.5 nm) yields to 20 % R_{on} degradation, compared to full activation. For the same reason than in the previous sections, this configuration is thus not suitable to aim at a low R_{on} value, i.e. to achieve high performance.

4.3.4 The Double SPER configuration

As seen in the last section, the lateral SPER with single-sided implantation is not sufficient to dope the entire fin in order to lower the R_{on} value. By using twice this scheme, one for each side of the fin, the accesses will be hence entirely doped, if the amorphization thickness is superior to the half to the fin width. It is hence more tolerant to process variabilities, such as fin width variation, line width roughness or amorphous/crystalline interface roughness, than the other configurations

and provides the lowest R_{on} value. This new process scheme is named Dual SPER (DSPER) and is described in Figure 4.17 via width cross-sections of the top of the fin.

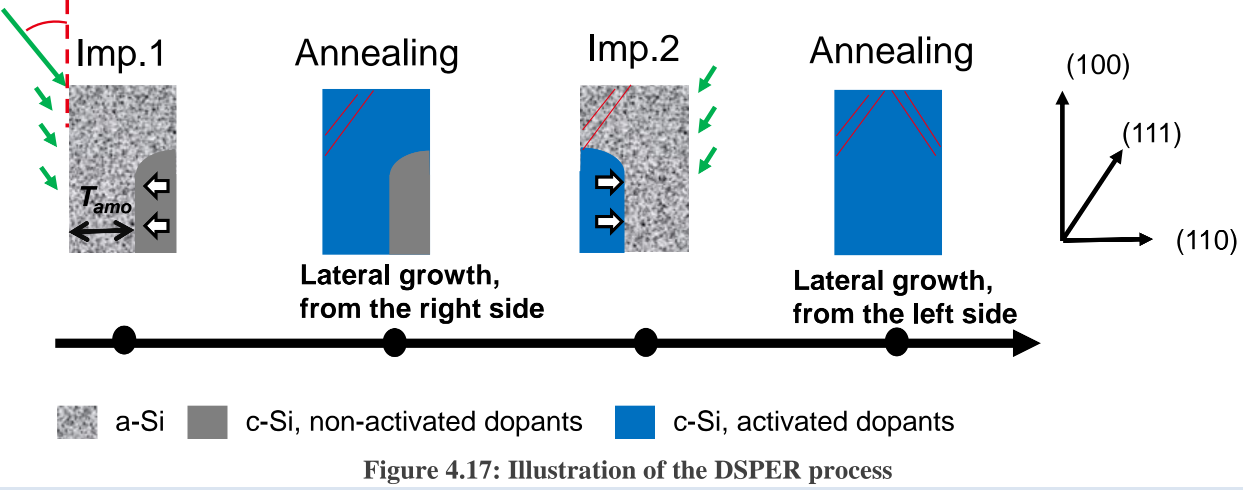


Figure 4.17: Illustration of the DSPER process

In this new proposed seed scheme, one side of the fin is at first implanted, leaving the other side in a crystalline state in order to act as the seed, like the lateral seed configuration. Once the recrystallization is fully carried out, a new implantation is performed, this time at the other side of the fin. The previously crystalline seed is thus amorphized. An already doped and activated zone of the fin is therefore used as a new crystalline seed, and another recrystallization is carried out. Consequently, at the end of the process, the entire fin is doped and activated. This configuration might thus be considered as optimal to lower access resistances, and a deeper investigation is carried out about the recrystallization mechanism.

TIME ANNEALING CONSIDERATION

Understanding the recrystallization mechanism in such a configuration might be challenging, and is highlighted in Figure 4.18, which sketches a zoom of the fin with the DSPER process after the first implantation. It represents thus the seed template involved in this process.

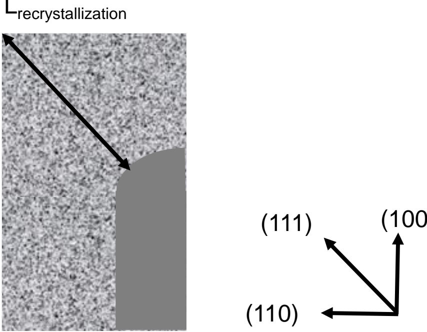


Figure 4.18: Zoom of the cross section of the fin width after the first amorphizing implantation

It is worth noticing that in this work the implantation tilt has been defined at 45°. The fin top is thus as amorphized as the sidewall. After a tilted amorphizing implantation, the amorphous layer will be laterally and vertically bounded by the crystalline seed template. Due to this configuration and in a conventional orientation, added in Figure 4.18, the three crystalline orientations will be involved to recrystallize the amorphous layer. Regrowth will thus be limited by {111} planes, and the annealing duration should thus take into account this 2D shape. This is possible by geometrical consideration, by first defining the recrystallization length, which is the minimal length from the seed to the fin corner. For a 7 nm-thick with, about 6 nm of the amorphous layer should recrystallize in the <111> crystalline orientation. According to Table 1 in the chapter 2, at 600 °C, for <111> crystalline orientation, and for boron (respectively phosphorous) implantation, the SPER rate is equal to 50 nm/min (respectively 17 nm/min). Thus, for a 1 min annealing, the access should be fully recrystallized. At 500 °C, for phosphorous implantation, the annealing time should be at least equal to 20 min, due to the exponential-dependency of the SPER rate with the temperature, while 10 min should be enough for boron implantation. This value also depends with the amorphization thickness (and thus, the targeted fin with) as well as the tilt of the implantation. Besides, it had been concluded in [98] that the SPER rate will be significantly affected by the round shape. While at 600 °C, for a 12 nm-thick fin, and with a 45°-tilted implantation, fin might be easily recrystallized, at 500 °C it is advised to take these considerations into account to avoid partial recrystallization, which might thus lead to higher access resistances.

FACET FORMATION AND OXYGEN RECOIL

By involving {111} planes for the regrowth, facet formation might also be expected in this configuration, as represented in Figure 4.17 by the red line at the fin corner. To confirm this hypothesis, morphological study, i.e. with only the active zone patterning, has been carried. 45°-tilted implantation by germanium has been performed to amorphize 12 nm of a 35 nm-thick fin, and is sketched in Figure 4.19.a). After the amorphizing implantation, boron doping has been tuned to obtain a flat profile in the width direction. The recrystallization annealing has been carried at 600 °C during 1 min, which is thus sufficient to recrystallize the amorphous layer. A TEM picture of a 35 nm-thick-fin access, after the resulting DSPER process is displayed in Figure 4.19.b), and Figure 4.19.c) sketches the resulting TEM picture. In Figure 4.19.b) is shown the as-implanted fin, with the targeted amorphized thickness. It is worth noticing that geometrical dimensions drawn in Figure 4.19.a) and Figure 4.19.c) correspond accurately to ones observed in the TEM picture in Figure 4.19.b).

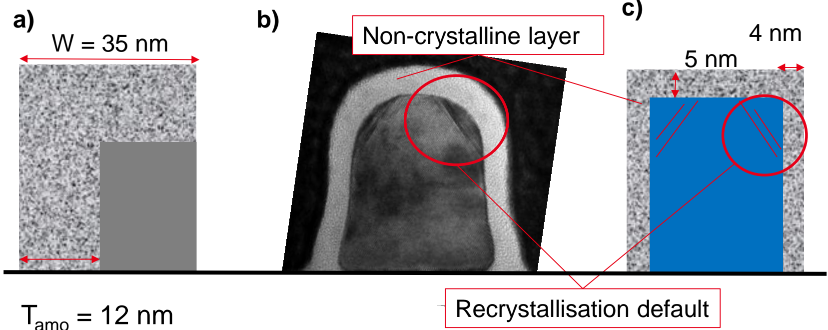


Figure 4.19: TEM picture of the fin-width cross section of a 35 nm-thick fin after the DSPER process

Two phenomena are observed in the TEM picture. At first, the {111} facet formation at the fin corner, which is directly linked to the 2D shape. However, it is not so obvious that for narrower fin, these facets will appear, because it might depend on the to-be-recrystallized depth, as well as the recrystallization mechanisms that are involved for a 2D a/c interface shape. Same morphological study has been performed to amorphize 6 nm of a 16 nm–thick fin, and is represented in Figure 4.20, with the same representation pattern that in Figure 4.19.

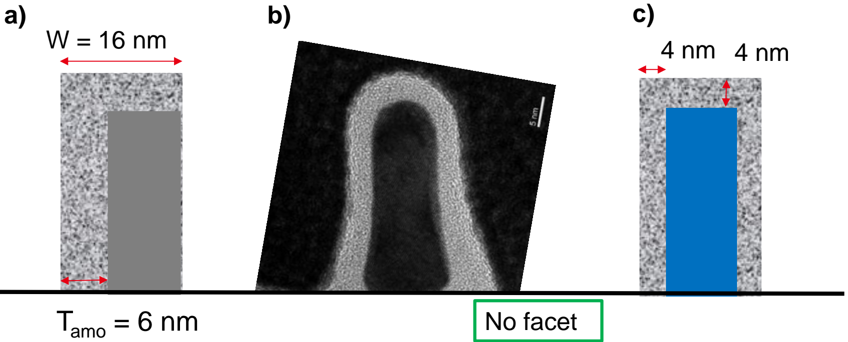


Figure 4.20: TEM picture of the fin-width cross section of a 16 nm-thick fin after the DSPER process

For a narrower fin, no facet has been observed, and at least two reasons might explained this result. At first and as supposed, it might be due a smaller amorphized thickness than in the previous study, which might thus let to avoid facet formation. The second reason might be due to the second phenomenon, observed for both TEM pictures of Figure 4.19 and Figure 4.20. As highlighted in Figure 4.19.c) and Figure 4.20.c), an unexpected 4 nm-thick non-crystalline layer is clearly visible at the fin edge at each side and does not depend on the amorphized thickness. In order to conclude if this layer is composed of an amorphous silicon due to a partial recrystallization or to an unexpected thick oxide formation, an HF clean has been carried out on isolated devices. Figure 4.21 represents the variation ΔW of the measured fin width, plotted according to the different targeted width W_{target}, starting from 30 nm down to 10 nm.

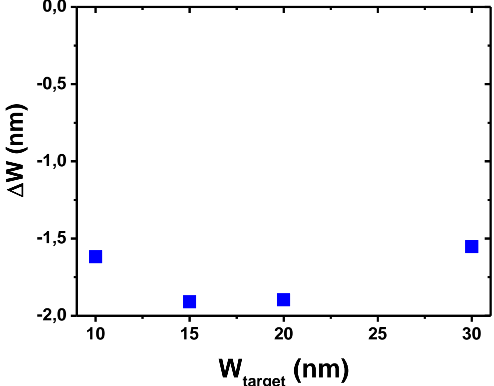


Figure 4.21: Variation of the measured fin width after the HF clean

If the non-crystalline layer is a native thick oxide, a difference of 8 nm should be observed for all fin. For all devices, the total fin width is reduced by less than 2 nm, which corresponds to a standard native-oxide thickness. The non-crystalline layer is thus probably due to a partial recrystallization. The SPER rate is indeed influenced by the surface proximity and more specifically, it has been shown in [74], [34], [99] that the presence of oxygen suppresses the SPER rate, resulting in the formation an amorphous/crystalline facet. Recently, it has been concluded in [25] that the oxygen recoil leads to a 3 nm-thick non-recrystallized layer near to the free surfaces, which is also observed in our study.

This partial recrystallization might be thus explained by the fact that no facet has been formed for a narrower fin. To conclude about this hypothesis, deeper investigation has to be made, with the introduction of an HF clean right before implantation. According to [25], no native oxide has been indeed observed in their sample when implantation is realized one hour after the clean. It is thus advised to hold one step after the other in this period, or to perform a deeper investigation to estimate more precisely the minimal mandatory duration between the clean and the implantation before the native-oxide growth will influence the device performances.

Besides, this HF clean might also consume the etch-stop sacrificial oxide in a gate last configuration. In Figure 4.22 is represented the gate-length cross section of a FinFET. The etch-stop oxide consumption is shown in Figure 4.22.a) before implantations, and in Figure 4.22.b) is represented the FinFET after the gate stack formation.

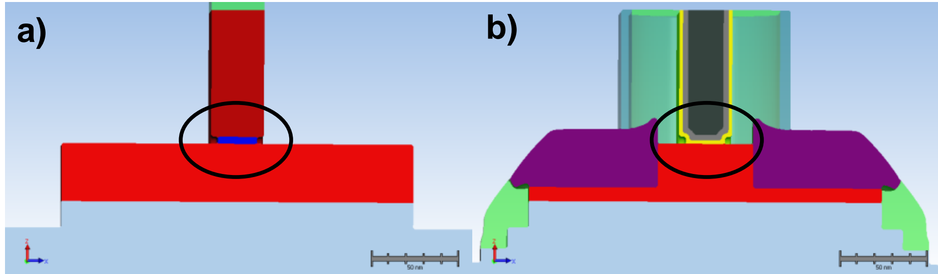


Figure 4.22: Illustration of the etch-stop layer consumption, after the gate patterning, and its consequence on the process flow

This might thus induce an additional parasitic capacitance, and for further study, it might be useful to deposit a thin liner, as seen in the chapter 3. This deposition might however lead to a fin collapse, as observed in [87]. Besides, at low-thermal budget, the junction might be misaligned with respect to the gate. This might thus lead to an increase of the access resistances.

Thereby, facet formation might still be present in this configuration, even for narrower fin.

CONSEQUENCE OF AN AMORPHOUS LAYER SURROUNDING THE FIN

To understand the influence of the amorphous layer surrounding the fin on device performance, electrical simulations have been performed. Figure 4.23.a) sketches the simulated FinFET structure after the regrowth, and the resulting R_{on} versus DIBL for two different amorphization thicknesses that surround the fin is plotted in Figure 4.23.b) for a 7 nm-thick fin. These thicknesses are equal to 1.5 nm and 3 nm and are considered as non-doped in the simulations.

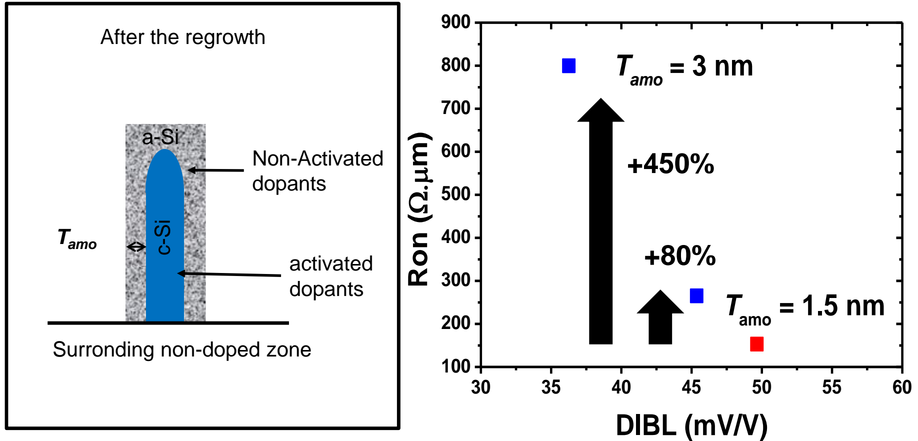


Figure 4.23: R_{on}-DIBL trade-off for non-doped zone surrounding the fin, for different seed thicknesses

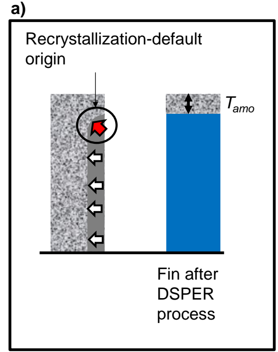
For a 7 nm-thick fin, while a 3 nm-thick non-doped layer surrounding the fin lead obviously to an enormous 450 % degradation of the R_{on} value, even a 1.5 nm-thick amorphous layer degrade the R_{on} value by 80 %, which highlight the importance to get rid of the oxygen recoil for advanced low temperature FinFET scaling. A solution to avoid it will be proposed in section 4.5. It is worth noticing that, in this thesis, the fin will be at minimum 13 nm-wide, and this degradation will thus be reduced.

Besides, recrystallization default at the top fin might also appear, but not visible in the TEM pictures due to this surrounding amorphous thickness.

RECRYSTALLIZATION DEFAULT AT THE TOP FIN

In [74], it has been indeed observed that for a sub-20 nm wide fin in the horizontal seed configuration, the distance over which the solid-solid transition can occurred prior RNG taking over is about 25 nm. Beyond this value, polycrystalline silicon might thus appear. For a 45°-tilted implantation and for a 7 nm-thick fin, to be in the ideal configuration in the DSPER process, amorphizing 4 nm of the sidewall of the fin is required. By geometrical considerations, this will force to also amorphize 4 nm at the top of the fin. Through this example, which is representative of this work, observing the formation of polycrystalline silicon is therefore unlikely. However, to avoid the shadowing effect as in a SRAM configuration with the use of the photoresist mask, 10°-tilted implantation is mandatory. Amorphizing 23 nm of the top of the fin will thus be involved due the DSPER process with such an angle. The polycrystalline silicon might therefore be present, leading to an increase of the access resistances. Electrical simulations have been performed to quantify this possible degradation.

Figure 4.24 sketches the same simulated FinFET structure showed in Figure 4.23.a), with different non-recrystallized layer T_{amo}, at the top of the fin, which is therefore representative of the fin thickness without doping activation. Figure 4.24.b) is the resulting R_{on}-DIBL trade-off. For a better understanding, the R_{on} values are normalized with respect to the R_{on} value of a fully-activated fin, thereby without an amorphous layer at the top of the fin.



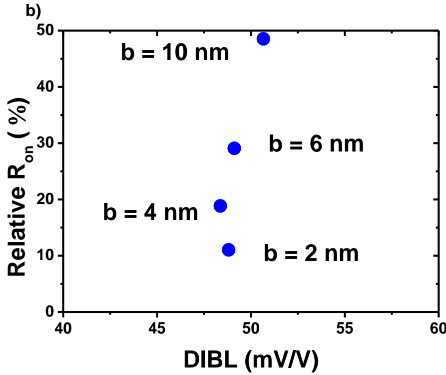


Figure 4.24: Relative R_{on}-DIBL trade-off for different non-recrystallized thicknesses at the top fin

According to these simulations, even a thin amorphous layer will degrade the R_{on} value. For a 2 nm-thick top-fin amorphous layer, a 10 % R_{on} degradation might indeed be expected.

As conclusion, while using DSPER process to dope the entire fin access might be considered as the best option in comparison to other seed schemes, some challenges have been highlighted and should be taken into account for advanced low-temperature FinFET scaling.

4.4 FABRICATION AND ELECTRICAL CHARACTERIZATION

The DSPER process has been used into the fabrication of low-temperature FinFETS devices, and this part summarizes the process flow used and the electrical results obtained. In this study, only p-type devices have been fabricated.

4.4.1 Process flow modification

The process flow for the process of reference, with thermal activation, has been described in the sub section 4.2.5. It has however to be modified for low temperature devices, especially to form junctions. As seen in the chapter 2, at low temperature, diffusion is too weak to drive dopants below the offset spacer. Implantation under the first spacer is thus mandatory for the most advanced nodes in order to reduce the access resistances [25]. Besides, thanks to the gate last process, implantations can be carried out before the first spacer formation. Indeed, as the first gate formation is sacrificial, and does not contain metal, CMOS stripping for LDD can be made without risking to degrade the gate stack. Figure 4.25.a) represents the process modification of implantation steps for low temperature devices. Figure 4.25.b) shows the beam line angular orientation used for the implantations.

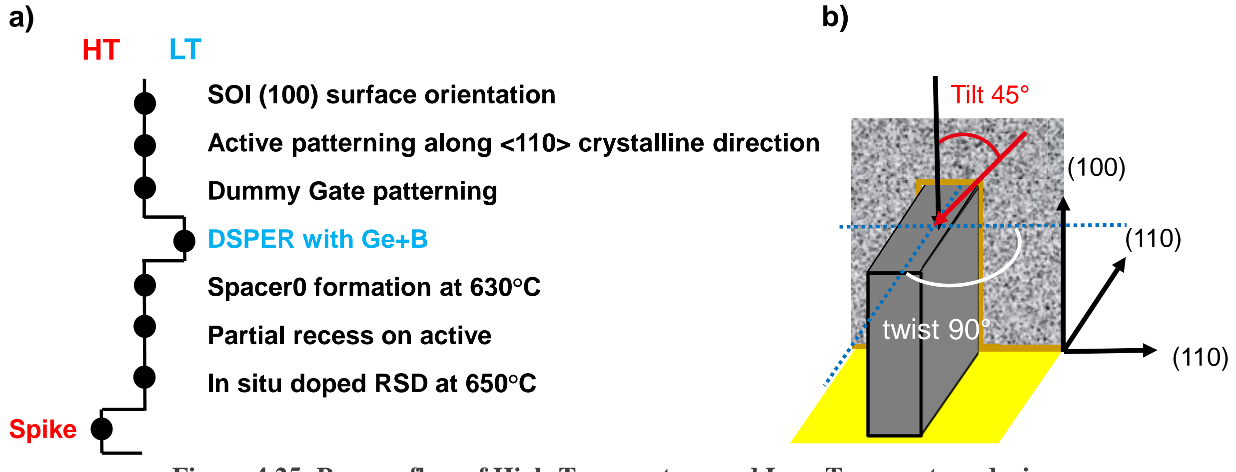


Figure 4.25: Process flow of High-Temperature and Low-Temperature devices

It can be seen in Figure 4.25.a) that the main modification for low-temperature devices is to add two implantation and annealing steps before the offset spacer definition, and to remove the spike annealing. The tilted implantation has been chosen at 45°, as shown in Figure 4.25.b), to avoid backscattering effects. The entire thermal budget of this process flow has been reduced from 950 °C down to 650 °C. To further lower the thermal budget to reach the 500 °C target needed for the 3D sequential integration, Si_3N_4 spacer might be replaced by SiCo at 400 °C [100]. The raised source drain epitaxy, done here at 650 °C, might be reduced at 500 °C, thanks to adequate precursors [101] and by the modification of the SiGe growth etch rate [102], for example.

A) SPLIT CONDITIONS

For low temperature integration with the DSPER process, the implantation conditions are directly linked to the fin width to dope the entire fin. The mask set used allows to manufacture devices with different fin widths and gate lengths. Two different fin widths (W_{top} = 12 nm and 25 nm) have been targeted with DSPER process. Two boron concentrations have also been tested, below and beyond the clustering effect, estimated in [96] at 3×10^{20} at/cm^3. The different split conditions concerning implants are summarized in Table 4.1.

Split name		LDD doping		Post Epi anneal
		T_{amo} (nm)	[B] at/cm^{3}	
HT POR		-	-	950° spike
SPER LT	T_{amo} = 6 nm	6 nm	2e20 at/cm^{3}	-
	T_{amo} = 6 nm, [B]x2	6 nm	4e20 at/cm^{3}	-
	T_{amo} = 12 nm	12 nm	2e20 at/cm^{3}	-
	T_{amo} = 12 nm, [B]x2	12 nm	4e20 at/cm^{3}	-
No Implant		-	-	-

Table 4.1: Implantation split description

In Table 4.1 is reported these 4 splits for low temperature devices, which have been named in reference to the targeted amorphization thickness as well as the boron concentrations. To dope a 25 nm-wide (respectively 12 nm-wide) FinFET, germanium implantations should amorphize more than 12.5 nm (respectively 6 nm). To ensure the full activation of the fin access, the amorphization thickness is slightly superior to the half to fin width. Indeed, the amorphous/crystalline interface present a certain roughness that is estimated to 1 nm. Thus, the targeted amorphizations are in reality 7.5 nm and 13.5 nm, as shown in Figure 4.26, which is a diagram of the a/c interface depth with different amorphizing implantation energies and doses.

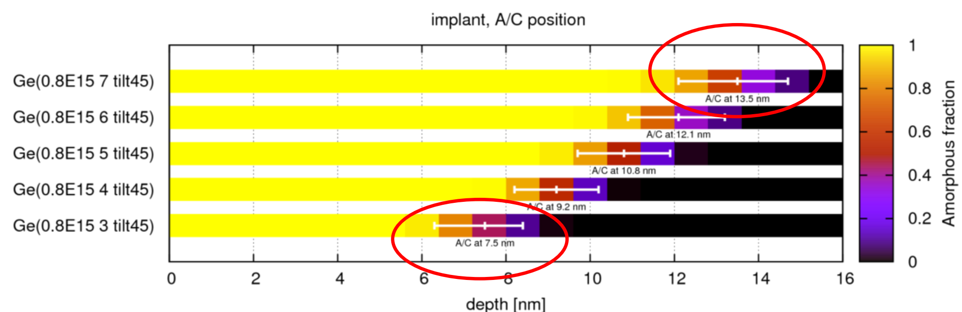


Figure 4.26: Diagram of the a/c interface depth for different implantation conditions

Besides, a split without implantation has also been defined in order to underline the importance to dope under the offset spacer. Finally, a high temperature process of reference split with a 950 °C spike annealing has also been fabricated.

B) E-RSD ON IMPLANTED FIN

A challenging step to manufacture low-temperature devices is the epitaxy regrowth, which is very sensitive to the crystalline quality of the substrate and can be defective on implanted accesses. A particular precaution into the surface preparation has thus been taken to be able to obtain a selective epitaxy regrowth without roughness. Figure 4.27 represents tilted Scanning Electronic Microscope (SEM) pictures of FinFET devices right after the epitaxial regrowth on recessed fin, without (Figure 4.27.a)) or with (Figure 4.27.b)) implantations.

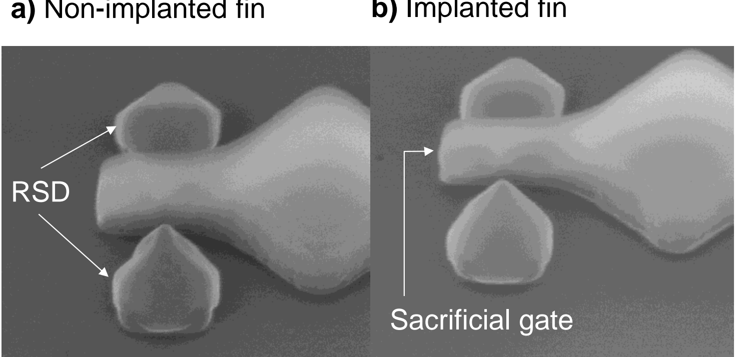


Figure 4.27: Tilted SEM pictures of FinFET devices with or without implantation prior to the epitaxy

In the tilted SEM picture of Figure 4.27.a), the epitaxy regrowth on the active zone is uniform and selective. This is a good first indication that raised source drain epitaxy on a recessed fin is feasible with a maximum thermal budget of 650 °C. In addition, epitaxy on implanted fin (Figure 4.27.b) does not change its quality. This similarity of the epitaxy quality on implanted or not implanted fin might be attributed to the etching used for the recess, which improve the surface preparation before the epitaxy.

C) TEM OBSERVATIONS

To complete these observations, two TEM cross section pictures of recessed-and-implanted-fin devices are shown in Figure 4.28, following the length direction in Figure 4.28.a) and the width direction in Figure 4.28.b). It is worth noticing that the device shown by the TEM picture in Figure 4.28.a) is not implanted (due to the absence of adapted structures for TEM observations in that direction).

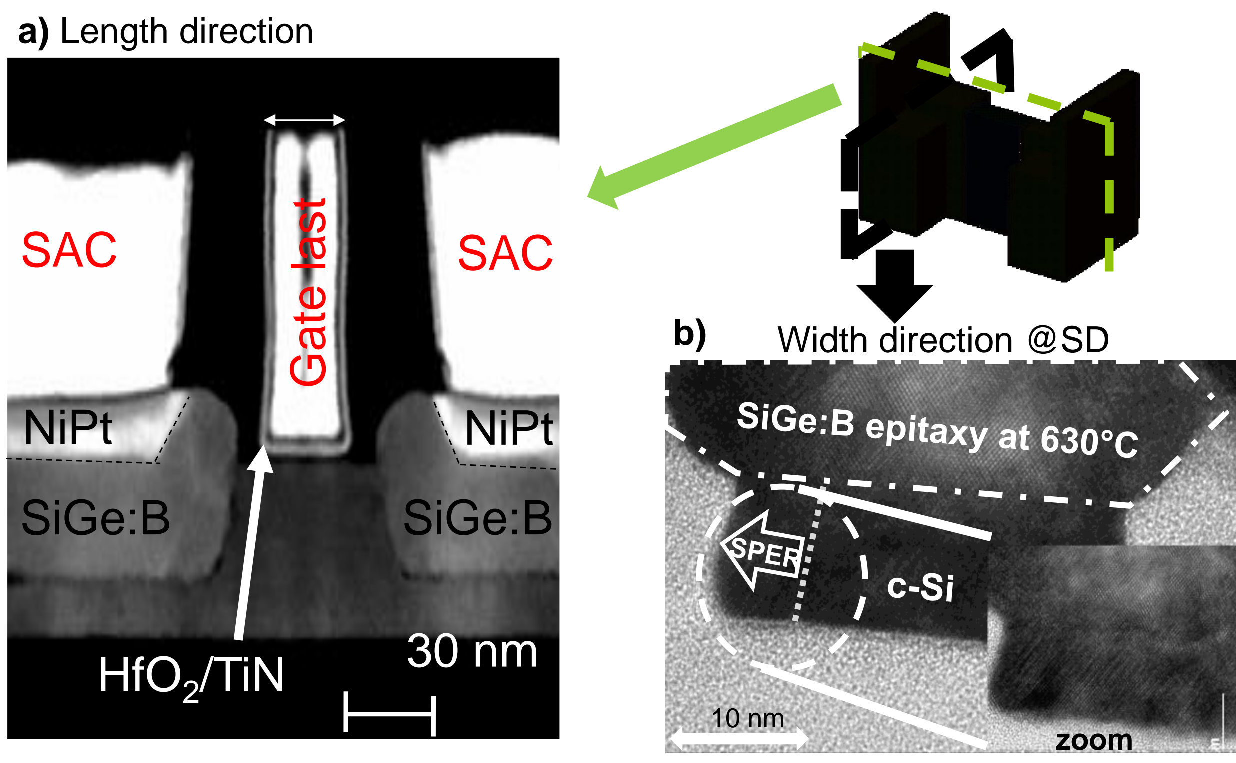


Figure 4.28: TEM pictures at the length and width cross section of Low temperature FinFETs

In both TEM pictures, the embedded *in situ* doped raised source drain epitaxy is crystalline. In addition, classical diamond-shape of the epitaxy regrowth is observed in Figure 4.28.b). Finally, in this figure, all the active zone is crystalline, at the top with the embedded raised source drain epitaxy, and at the bottom with the DPSER process. In Figure 4.28.a) is also reported the different elements included in the gate stack (HfO_2/TiN/W). Self-Aligned Contact process and salicidation might also be observed.

4.4.2 Electrical results

The electrical characterization of FinFETs is shown and analyzed in this section. Both high temperature and low temperature devices with channel lengths ranging from 30 nm to 100 nm have been characterized. The MOSFETs have been tested in saturation regime at V_{dd} = -0.7 V and in

linear regime at V_{dd} =-0.05 V. The I_{off}-I_{on} trade-off comparison between the process of reference activated at high temperature and low temperature with different doping conditions and for two fin width (W_{top} = 12 nm and 25 nm) are shown in Figure 4.29.

These results are normalized by the effective width, which corresponds to the fin width plus twice the fin height. For the fin width measurements, an error of 2 nm has been estimated. This variation might come from the measurement technic (Scanning Electronic Microscope) or by process fluctuation itself. The fin height has been measured by ellipsometry, and is considered accurate to within ±5Å. For the smallest width (W_{top} = 12 nm), this measurement error can lead to a 3 % error on the performance of devices.

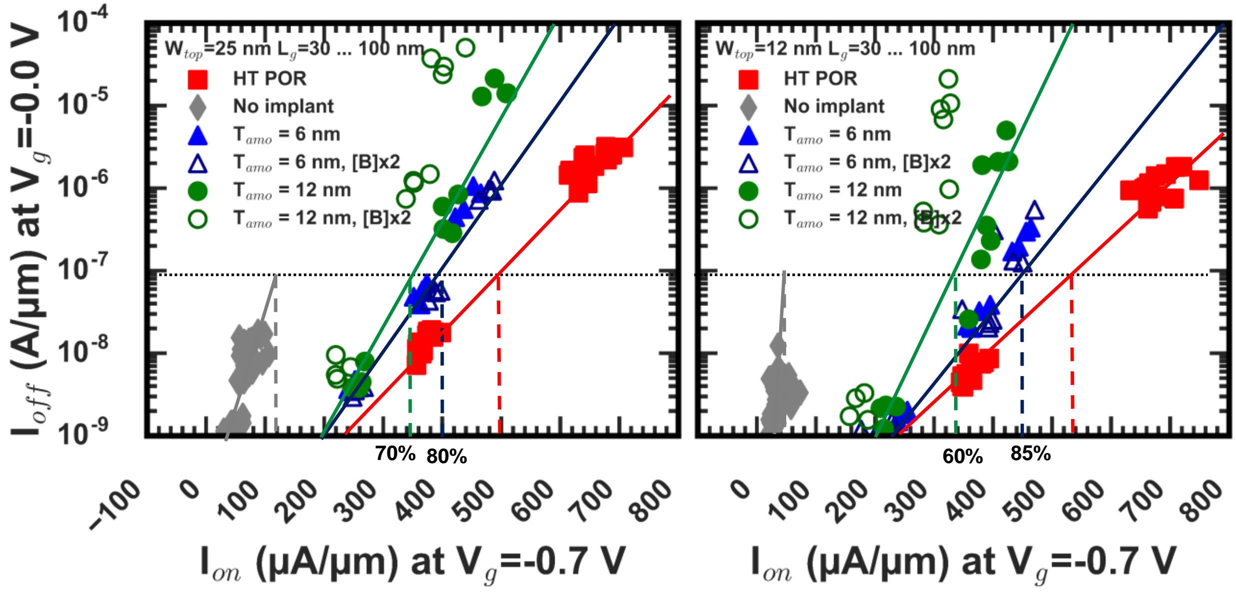


Figure 4.29: I_{on}-I_{off} trade-off of HT and LT FinFET

Functional devices are demonstrated for all implanted split at low temperature for both fin widths, underlining the importance of doping under the first spacer. While the split without implantation shows indeed very poor I_{on} value (inferior to 100 µA/µm), splits with DSPER process show higher ion value (superior to 300 µA/µm at I_{off} = 1e-7 A/µm), indicating a high activation level under the first spacer. For both fin widths, while no relevant benefit is observed by increasing the activation level from 2×10^{20} at/cm^3 up to 4×10^{20} at/cm^3 for the 'T_{amo} = 6 nm' splits, for the

'T_{amo} = 12 nm' ones, an I_{off} increase and I_{on} decrease is observed, and will be further investigated in the sub sections 4.4.3 and 4.4.4. This observation has also to be correlated with the fact that, for the wider fin (W_{top} = 24 nm), while 'T_{amo} = 12 nm' split reaches 70 % of the I_{on} performance of the HT POR, the best value (80 %) is found for the 'T_{amo} = 6 nm' ones.

A) FOCUS ON W = 12 NM

For the thinner fin (W_{top} = 12 nm), the best LT split, i.e. 'Tamo = 6 nm', reaches 90 % of the I_{on} performance of the HT POR, indicating that high activation at low temperature is possible. Besides, unexpected functional devices are found for the thinner width and 'T_{amo} = 12 nm' splits. While the fin width has been measured by Scanning Electron Microscope (SEM) and equal to 12 nm with an incertitude of 2 nm, the amorphization depth for this split should be equal to 13.5 nm with an implantation roughness estimated at 1 nm. In addition, for the simulated amorphization depth, the dose rate of implantation current for these simulation is representative of the experimental dose rate values. Figure 4.30 compares the as-implanted fins calculated by simulation (Figure 4.30.a)) or measured by TEM picture (Figure 4.30.b)), with implantation conditions corresponding to 'T_{amo} = 6 nm' split.

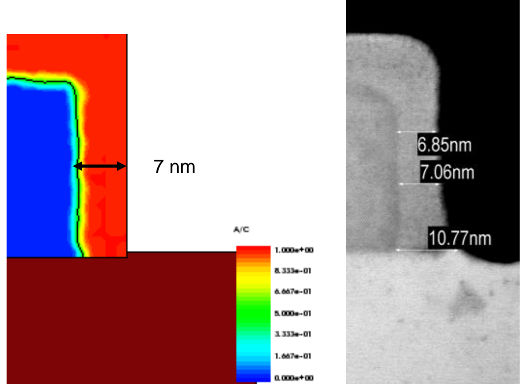


Figure 4.30: Simulated and experimental amorphization depth for 'T_{amo} = 6 nm' splits

For a fair interpretation, additional simulations for 'T_{amo} = 12 nm' split are mandatory. A good correlation between this simulation and the experimental result is nevertheless observed, with a discordance inferior to 5 Å. It is thus unlikely that a vertical recrystallization occurred for the

'T_{amo} = 12 nm' splits with the narrower fin (W = 12 nm), and low I_{on} value had been expected. It can be assumed that contrary to our previous expectation, the channel can indeed act as a seed which allows to recrystallize the amorphous zone under the first spacer.

Relatively-large I_{off} values are also found for every splits in Figure 4.29, and might thus indicate that short channel effects are not well controlled. Figure 4.31 reports the I_{on}, the I_{off} and the DIBL as a function of the fin width, for devices with gate length equal to 60 nm, and for fin width from 40 nm down to 12 nm.

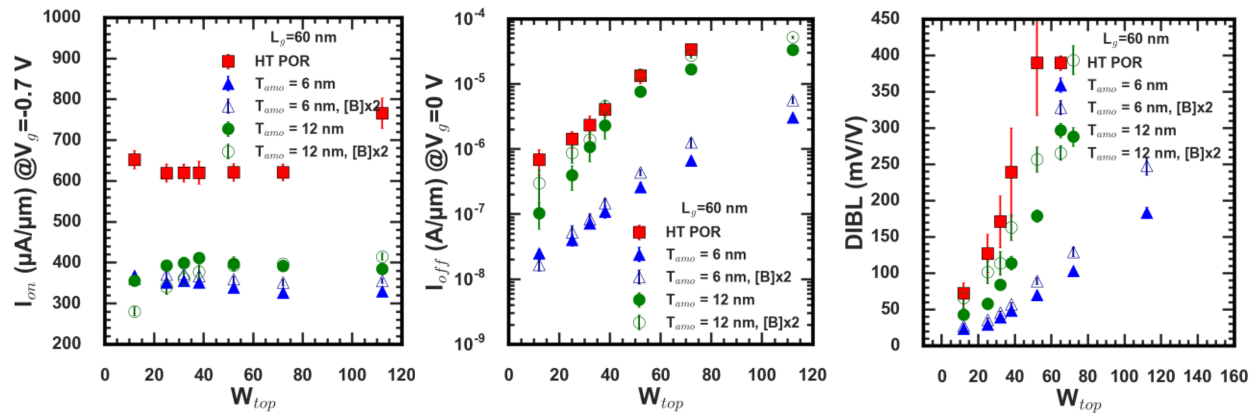


Figure 4.31: I_{on} and I_{off} values plotted as a function of the fin widths

For HT devices, large I_{off} and I_{on} values (above 1×10^{-6} A/µm and 600 µA/µm) are observed for any fin width. In addition, high DIBL values have also been observed. The HT POR is thus considered as overlapped, i.e. with a junction profile that goes under the gate, and might be due to a too big thermal budget.

For LT devices, while for 'T_{amo} = 6 nm' splits, the I_{on} value does not depend on the fin width; for 'T_{amo} = 12 nm' one, a degradation of 12 % is observed at W_{top} = 12 nm. This highlights that lateral seed for this implantation condition and this fin width is not thick enough to be used as a template for the recrystallization process. Implantations have thus to be tuned according the targeted fin width. Despite this degradation, the I_{on} value is still above 300 µA/µm. As previously mentioned, it might be possible that a fraction of the fin below the offset spacer might be

recrystallized, thanks to the channel acting a crystalline seed (as illustrated in Figure 2.23 in the chapter 2 for example).

Despites reducing the fin width for all LT splits, relatively large I_{off} value is observed. To investigate this issue, I_d-V_g curves for the 'T_{amo} = 6 nm' splits is plotted in Figure 4.32.a). Besides, the threshold voltage V_t, evaluated at constant current in saturated regime has been extracted from I_d-V_g curves, for gate lengths starting from 100 nm down to 15 nm for the 'T_{amo} = 6 nm' splits, and is plotted in Figure 4.32.b). Figure 4.32.c) and Figure 4.32.d) show the DIBL and the Substhreshold Swing (SS) plotted as a function of the gate length for the LT split.

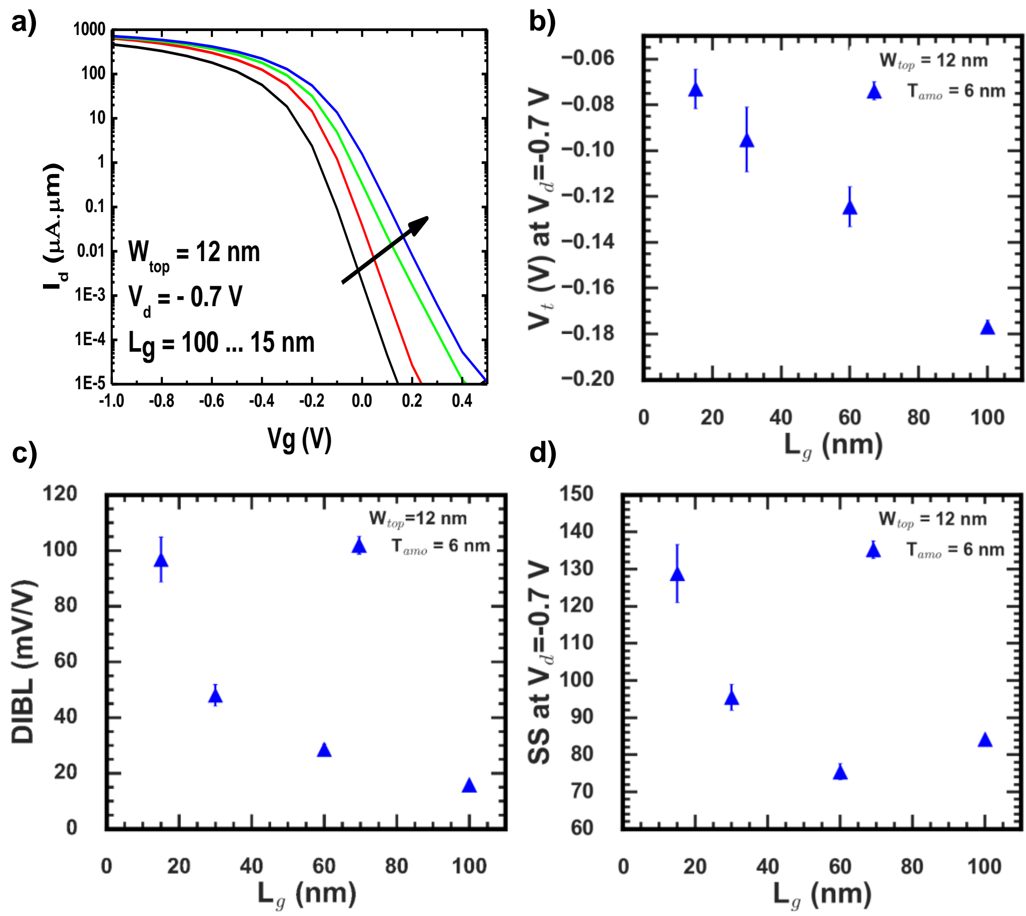


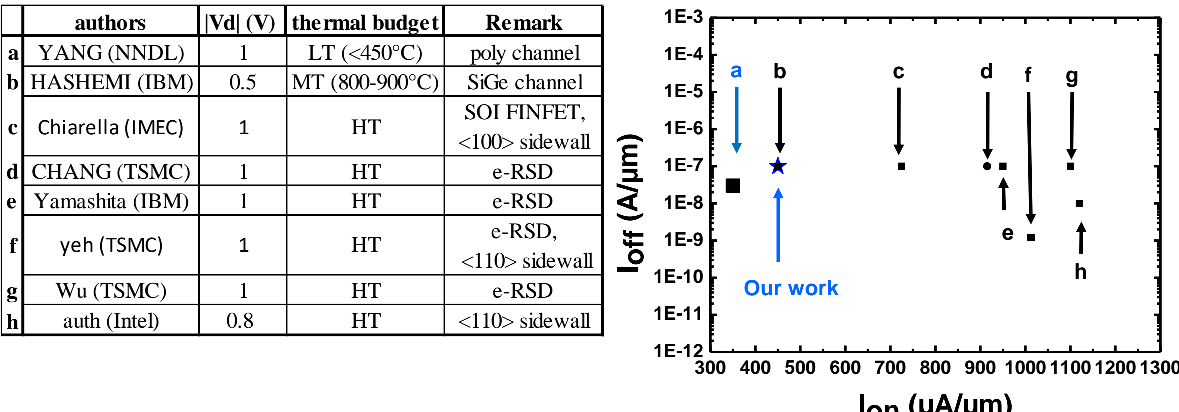
Figure 4.32: I_d-V_g curves, $V_{t,sat}$, DIBL and SS vs L_g at for the 'T_{amo} = 6 nm' split.

In Figure 4.32.a), even the longest gate length (L_g = 100 nm) shows a shift in the drain current. In Figure 4.32.b), between a long device (L_g = 100 nm) and a short one (L_g = 15 nm), the

threshold voltage is only increased by 150 mV, indicating that the V_t roll off is well controlled. It is also observed that the threshold voltage is relatively high even for the longest gate length (-200 mV). DIBL shows low value for L_g=30 nm (50 mV/V) as well as the SS (inferior to 100 mV/dec). As a conclusion, short channel effects are relatively well controlled for the best split. The large I_{off} values result thus from a non-optimized gate stack work function, yielding to too low threshold voltages, and has thus to be optimized in further studies.

B) I_{ON}-I_{OFF} PERFORMANCE BENCHMARK

Figure 4.33 finally shows I_{on}-I_{off} performance benchmark of p-type FinFETs built on silicon channel and with embedded raise source drain. For a fair benchmark, supply voltages are indicated, as well as the thermal budget for all references.



	authors	|Vd| (V)	thermal budget	Remark
a	YANG (NNDL)	1	LT (<450°C)	poly channel
b	HASHEMI (IBM)	0.5	MT (800-900°C)	SiGe channel
c	Chiarella (IMEC)	1	HT	SOI FINFET, <100> sidewall
d	CHANG (TSMC)	1	HT	e-RSD
e	Yamashita (IBM)	1	HT	e-RSD
f	yeh (TSMC)	1	HT	e-RSD, <110> sidewall
g	Wu (TSMC)	1	HT	e-RSD
h	auth (Intel)	0.8	HT	<110> sidewall

Figure 4.33: I_{on} I_{off} performance benchmark of FinFET devices, built on silicon channel with embedded *in situ* doped raised source drain.

To our knowledge, only [103] has studied a low temperature FinFET fabrication. The channel is however in polycrystalline silicon, and the comparison has thus be done with care. It is worth noticing that publication showing p-type FinFET fabrication with silicon channel and embedded raised source drain epitaxy has been difficult to found. For a fair comparison, only 3 publications, including two from TSMC, has been found and shown here. Indeed, most publications show some boosters to improve performance using stress effect, as for Hashemi *et al.* in [89] for

SiGe channel with thermal budget inferior to 900 °C, or Auth *et al.* (Intel) [93] for wrapped RSD with <110> sidewalls. As a conclusion, different boosters are used and it appears quite irrelevant to only compare our result with devices fabricated on Si channel with e-RSD. The drain current values are also widely normalized by -and indicated as- the 'effective width', but the definition proposed above might be different among the different authors. For example, Intel's authors have normalized drain current value by the pitch area.

Nevertheless, it is shown in Figure 4.33 that for low temperature integration, the proposed process flow gives the best known result, with an I_{on} increase of 30 % (100 µA/µm) in comparison with [103]. Some efforts have still to be done in order to reach the state of the art of HT devices, and further optimizations with the DSPER process are thus proposed in the next section.

4.4.3 Non-recrystallization default

In the sub section 4.3.4, it has been evidenced that a R_{on} degradation might be expected, either due to a top-fin non-recrystallization default or due to an amorphous layer which might surround the fin. These two hypothesis are summarized in Figure 4.34.

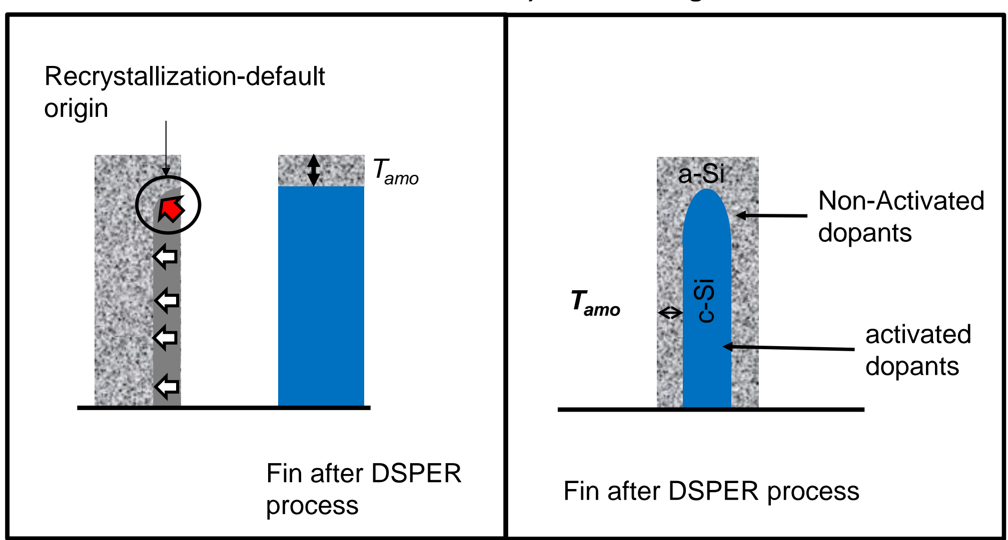


Figure 4.34: Illustration of two possible recrystallization defaults

The following sub section proposes an electrical evidence of such non-recrystallization default.

The R_{on} has been plotted as a function of the fin width in Figure 4.35 for the 'T_{amo} = 6 nm' split for low temperature devices, and for the HT POR split.

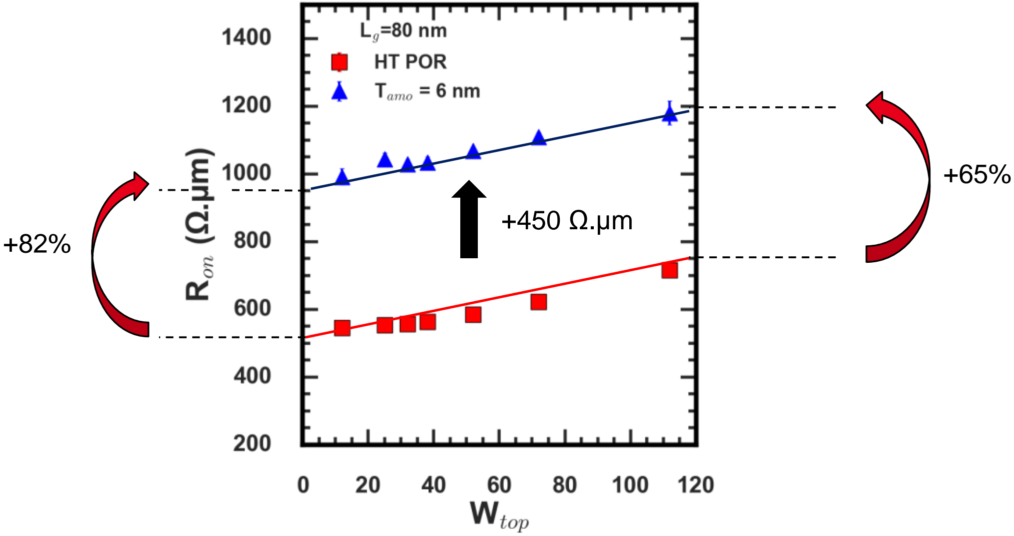


Figure 4.35: R_{on}-W for LT 'T_{amo} = 6 nm' split and HT POR

It can be seen in Figure 1.34 that the LT split shows a R_{on} decrease as the fin width is reduced. The hypothesis of an amorphous layer that surrounds the fin is, in that case, unlikely. Indeed, if an amorphous layer surrounds the fin, then the R_{on} should be more degraded for narrower fins in comparison to wider ones.

In comparison to the HT POR, the LT split shows a constant degradation of 450 Ω.µm. This degradation represents an 82 % (respectively 65 %) increase of the R_{on} between the HT POR and the LT split for the narrower (respectively wider) fin. This degradation might thus be an indication of a recrystallization default for LT split under the first spacer at the top fin. Besides, this recrystallization default might also explained that, in Figure 4.29.a), for the wider fin (W_{top} = 25 nm), while 'T_{amo} = 12 nm' split reaches 70 % of the I_{on} performance the best value is found for the 'T_{amo} = 6 nm' ones.

4.4.4 Straggle and EOR density diminution

In this sub section, a particular attention has been put on the DIBL values and variation of low temperature splits. In Figure 4.36 is plotted the R_{on} as a function of the DIBL for the 'T_{amo} = 6 nm' and 'T_{amo} = 12 nm' splits, for 25 nm-wide device.

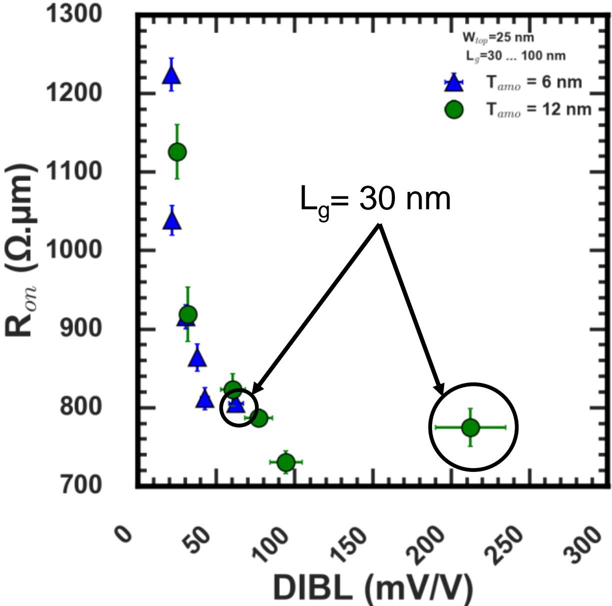


Figure 4.36: R_{on}-DIBL for 'T_{amo} = 6 nm' and 'T_{amo} = 12 nm' LT splits

A clear DIBL degradation above 100 mV/V is observed between LT splits for the same gate length (L_g=30 nm). While the 'T_{amo} = 12 nm' split should be the most optimized one in term of R_{access} for a 25 nm-thick width, both the DIBL value and its standard deviation are higher in comparison with 'T_{amo} = 6 nm' split. The main difference between theses splits is the energy and dose used to implant dopants, as the implantation energy must be increased to achieve a constant concentration for large width.

In order to understand this phenomena, simulations of the concentration profiles of these two splits have been performed for 30 nm-long devices, and plotted in Figure 4.37. The concentration profile along the gate-length cross section is shown in Figure 4.37.a), while the concentration profile along the fin-width cross section is plotted in Figure 4.37.b). These simulations have been performed after the first implantation of the DPSER process and after the most aggressive thermal annealing, which occurs during the first spacer deposition (deposition at 630 °C during 2 h).

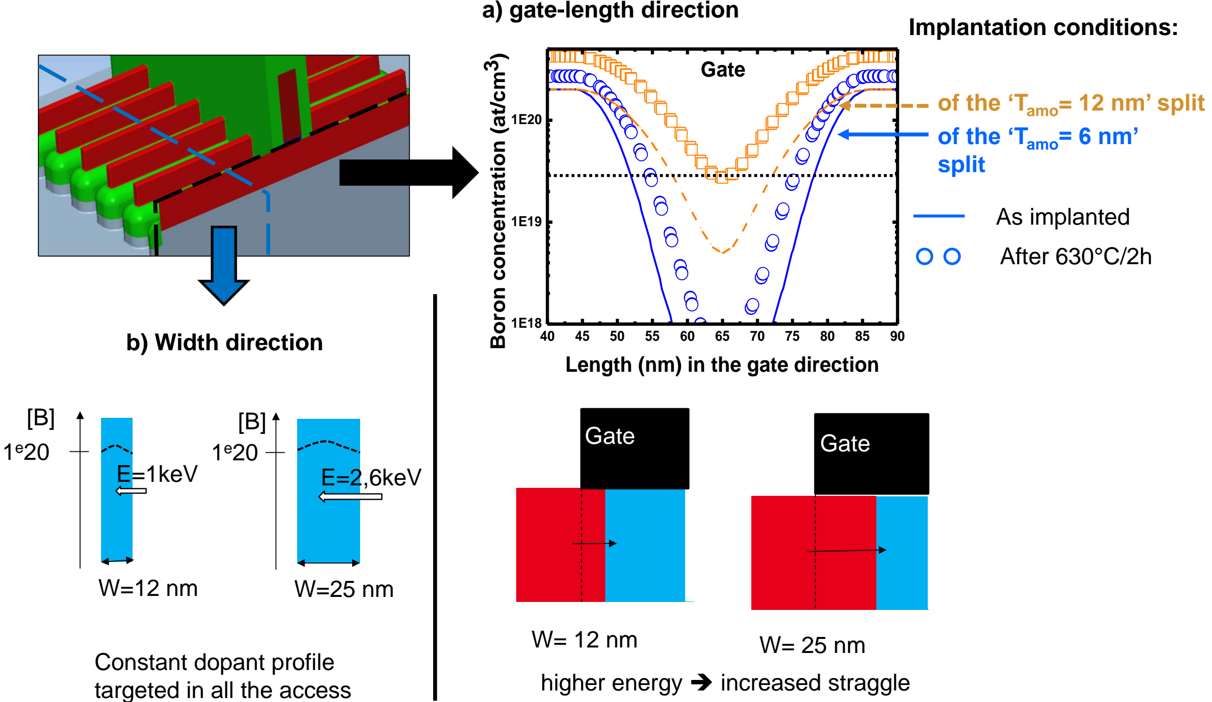


Figure 4.37: Dopant profile simulation for 'T_{amo} = 12' and 'T_{amo} = 6' nm splits, as implanted the final profile after an 630 °C/2 h annealing

Targeting a constant concentration along the width direction leads to degrade the junction abruptness in the length direction. After the first implantation, a difference of 10 nm on the electrical length is found between these two splits for a boron concentration equal to 3×10^{19} at.cm^{3}. By increasing the energy, the junction overlap is increased, due to a higher straggle.

In addition, a higher doping diffusion is also observed for the 'T_{amo} = 12 nm' split compared to the 'T_{amo} = 6 nm' one. This might also be attributed to a higher Transient Enhanced Diffusion due to a higher implantation energy and dose for the 'T_{amo} = 12 nm' split. After an amorphizing implantation, a high interstitial concentration might indeed be located at the amorphous/crystalline interface, and during the thermal annealing, these interstitials can lead to TED effect or Boron-Interstitial Clusters, resulting in a DIBL and a R_{on} degradation [45]. EOR defects might thus be present. However, these defects cannot be evidenced through a R_{on} (respectively DIBL) degradation, due to additional effects, such as the recrystallization default (respectively straggle

effect). Another to evidence such defects is to characterize the junction leakage, which should result in a higher minimal drain current ($I_{d,min}$).

This parameter is plotted in Figure 4.38.a) which represents I_d-V_g for low-temperature 60 nm-long, 12 nm-wide devices. To avoid short channel effect, the drain current should be in the linear regime with a relative high L_g. In Figure 4.38.b) is plotted the minimum linear drain current as a function of the fin width for L_g = 60 nm and for all low temperature splits.

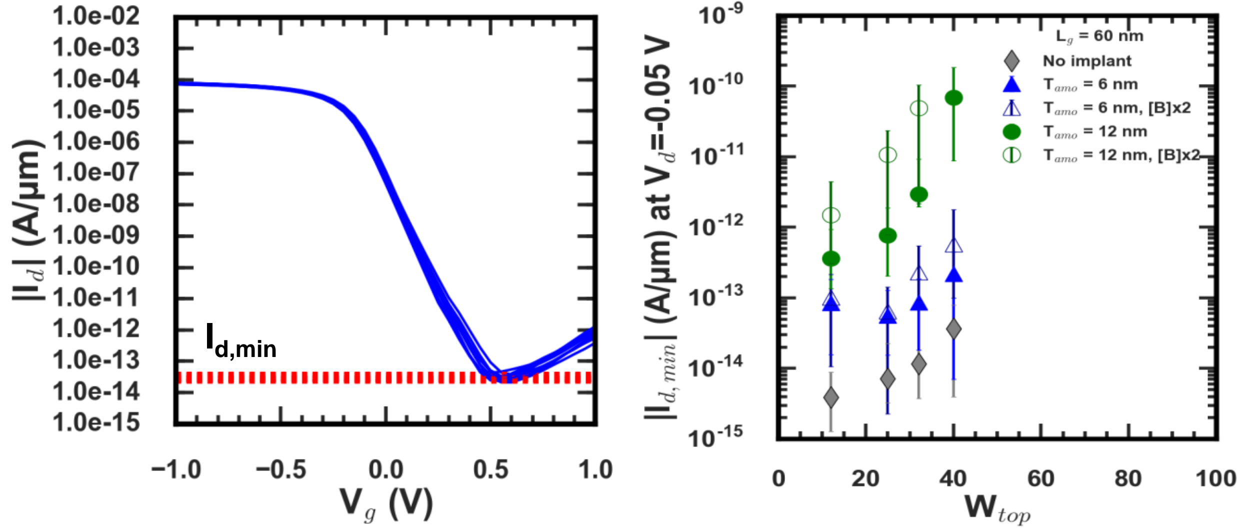


Figure 4.38: $I_{d,min}$ vs L_g for L_g=60 nm and for low temperature splits

For the 'T_{amo} = 12 nm' split, when the fin width is reduced, the $I_{d,min}$ value is also reduced. This might be an indication that EOR might are dissolved because the free surfaces are closer to the EORs, acting thus as a defect sinking effect.

For the 'T_{amo} = 6 nm' split, a relatively-stable $I_{d,min}$ with the fin width is nevertheless observed, which might thus be interpreted as fewer EORs in comparison to the 'T_{amo} = 12 nm' splits, due a lower implantation doses and energies.

The electrical gate length (extracted by TCAD simulations for the dopant concentration at 3×10^{19} at/cm^3) plotted as a function of the fin width, after the first implantation and after the spacer

formation, deposited at 630 °C/2 h is shown in Figure 4.39. An extrapolation is also added in this figure for W = 7 nm and with negligible TED thanks to the replacement of the SiN offset spacer by a SiCO one.

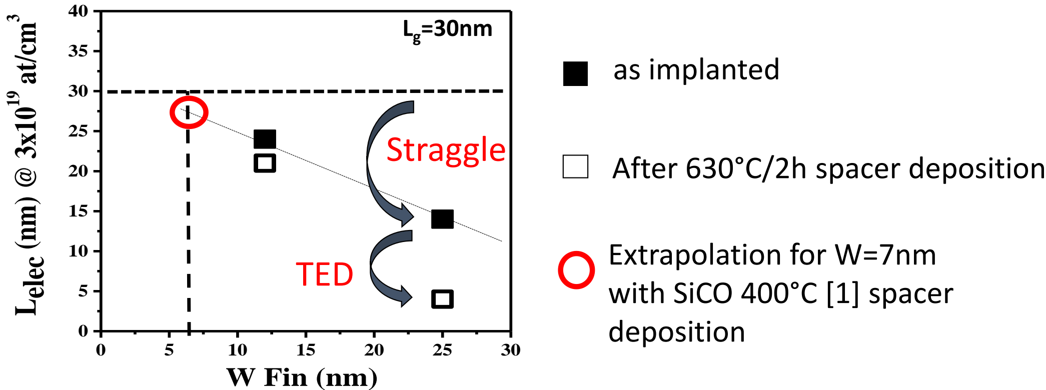


Figure 4.39: Evolution of the TED and straggle effects with scaling

A lower electrical length is extracted for the wider fin, due to the straggle effect. The implantation energy is however reduced for a more aggressive fin width, which reduce thereby the straggle effect. Furthermore, the spacer deposition anneal (630 °C, 2 h) leads to non-negligible diffusion, as shown by the simulation in Figure 4.37. This can be improved by replacing the ALD nitride spacers by SiCO deposited at 400 °C [100]. Thus, for a most advanced node (i.e. thinner width), this effect should be reduced. Thereby, both the value and the variation of the DIBL should reduced, as also observed in Figure 4.36. Another alternative to reduce this effect could be to use cryogenic implantation. As explained in the chapter 2, an amorphous thickness due to implantations will be increased at low temperature (-100 °C), compared to room temperature (25°C) for the same energy. Thus, to obtain the same room-tempered amorphous layer at low temperature, a lower energy can be used. In addition, cryogenic implantation is expected to reduce the EOR. This could thus lead to a weaker straggle and TED effect.

4.4.5 Strain effect

To our knowledge, few studies have been performed about strain effect with low thermal budget. The strain effect is brought by the e-RSD. Here, an investigation is performed for low-temperature devices manufactured with embedded or wrapped RSD, i.e with or without the fin recess. It will be focused on best implantation conditions, i.e. for the 'T_{amo} = 6 nm' split.

The main difference in the process flow for low temperature device, with and without recess, is shown in Figure 4.40.a), and Figure 4.40.b). In order to achieve the same active zone thickness (which include the fin, recessed or not, and the *in situ* doped raised source drain epitaxy), the epitaxy thickness is smaller for the 'without recess' split. In Figure 4.40.c) is shown the ellipsometry measurements of HT POR and the LT split with and without recess, after the sacrificial gate etching, the offset-spacer etching, and the epitaxy regrowth.

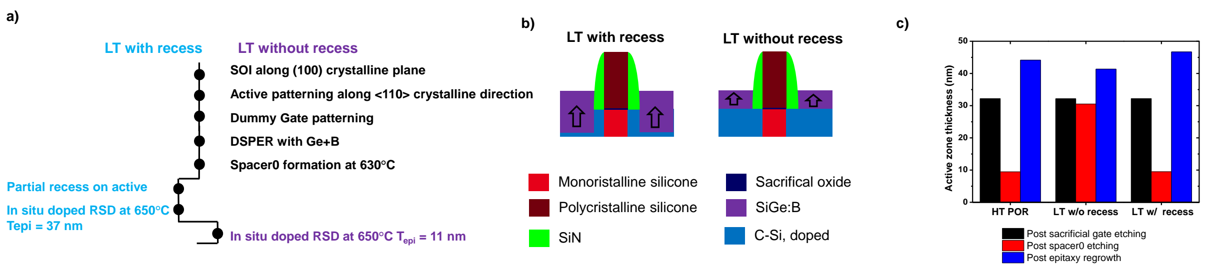


Figure 4.40: Process flow differentiation for low temperature devices with or without recess, and ellipsometry measurements

In Figure 4.40.c), a difference of 5 nm of the active zone thickness is found between low temperature splits. A difference on the access resistance might thus be suspected. The hole mobility and access resistances have been extracted for these two splits using the Y-function [96], on 30 nm-wide isolated devices, for gate lengths from 50 nm to 10 µm, and are plotted in Figure 4.41.a) and Figure 4.41.b), respectively. For a better understanding, the mobility has been normalized by the one at the highest gate length, here at 10 µm.

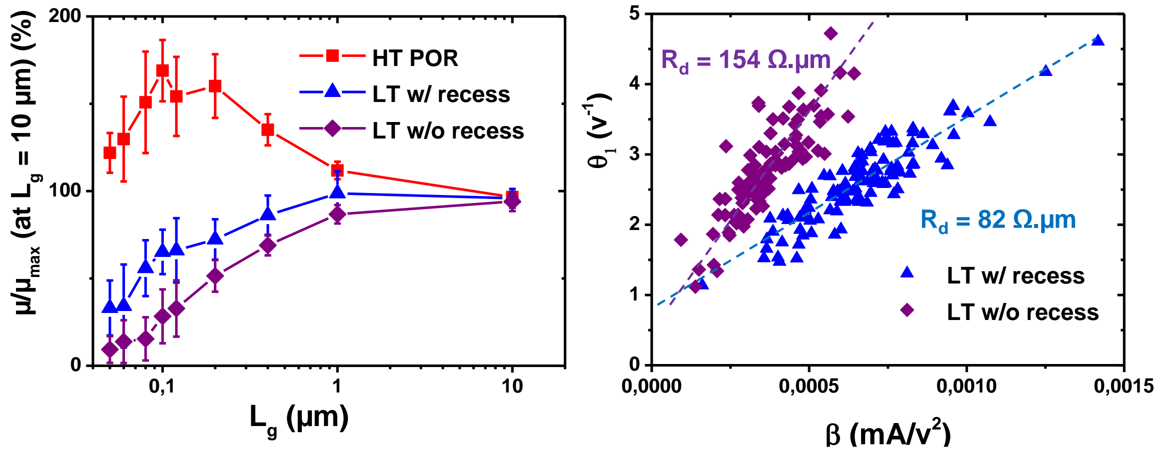


Figure 4.41: Relative mobility for HT POR, LT split with or without recess

In Figure 4.41.a), a clear effect of the strain is found for the HT POR split. An increase of the hole mobility is indeed observed, with a maximum value for L_g =100 nm. The mobility decreases however for the shortest gate length. For low temperature devices and for both splits the mobility decrease when the gate length is reduced. However, a higher mobility for low temperature split with recess is observed (for example, at L_g = 100 nm, the mobility for the recessed split is twice higher than the one without recess). These two observations (between HT and LT and between LT with or without recess) might indicate that the strain effect depends on the thermal budget.

It might however be worth noticing that the mobility degradation is observed for relatively-long gate length, up to 500 nm, where the access contributions into the carrier transport into the channel should be negligible. In the previous thesis [9], such a phenomena has also been observed, due to too high access resistances, as also observed here in Figure 4.41.b). The extraction methodology might thus be inappropriate in this case.

Besides, the hole mobility has been extracted by assuming its dependency with the gate length. A R_{access} degradation, as observed in Figure 4.41.b), should also lead to a mobility degradation, as studied by J-B. Henry in [8]. The R_{access} degradation might be explained by a suspected 3 nm-thick amorphous layer that surrounds the fin, as discussed in the sub section 4.3.4 and 4.4.3. While for the split with the recess (i.e. with e-RSD), only the area below the offset spacer

will be degraded, for the split without recess (i.e. with wrapped RSD), the access resistances will be worsen. For this split, a more important area might then be degraded. These two reasons might thus explain a R_{on} degradation.

It should be thus advised to decouple the R_{access} from the mobility. However, specific structure are compulsory [8] and not available on the mask set. For further study, splits should be performed with significant R_{access} improvement, and observing the influence on the mobility. Indeed, if the mobility is still degraded, then the stress effect is lost with low thermal budget. Otherwise, access resistance might still be the main challenging contribution.

4.5 PERSPECTIVE ON POTENTIAL INTEGRATION SCHEMES

In this section, some integration optimizations for low-temperature FinFETs are proposed and explained through process emulation thanks to the SEMulator3D software [104].

A) DSPER WITH SIN HARD MASK

The DSPER process might be viewed as a good option to dope the entire accesses. However, photoresist mask does not support a 500 °C annealing. Besides, in a CMOS integration with the utilization a photoresist mask, two lithographies are compulsory for dopant implantation, one for each MOSFET type. By using the DSPER process, four lithographies will be thus compulsory because of the mandatory small annealing to activate dopants, which will lead to a cost increase of the device fabrication. A first option to lower the fabrication cost and to simplify the process is to use only a single-sided implantation and thereby activation. This solution will however lead to a performance penalty. Another solution might be to use a Hard Mask, as SiN for example, which withstand such a temperature. By increasing the complexity of the device manufacturing, especially due to the Hard Mask formation then removal, only 2 lithographies will be mandatory.

B) SINGLE-SPER WITH SACRIFICIAL CHANNEL

Another option proposed here relies on the need to leave a 3 nm-thick crystalline area at one side of the fin to act as a lateral seed. To overcome the access resistance degradation due to

this crystalline and thus non-doped area, one solution is to start with a wider and higher fin than the targeted one, and to etch the channel right after the sacrificial gate removal. This process is called Single SPER (S-SPER), and is described in Figure 4.42, which are eyesights of devices, after the sacrificial gate patterning (Figure 4.42.a)) and after the sacrificial gate removal (Figure 4.42.b)). A wet-etching is proposed to recess the channel. For this example, geometrical considerations follow the 14 nm node design rule, i.e. the fin is 53 nm-tall and 7 nm-wide. A view from abode is also added in Figure 4.42.c), after the sacrificial gate removal, but the offset spacer is only represented for the sake of understanding.

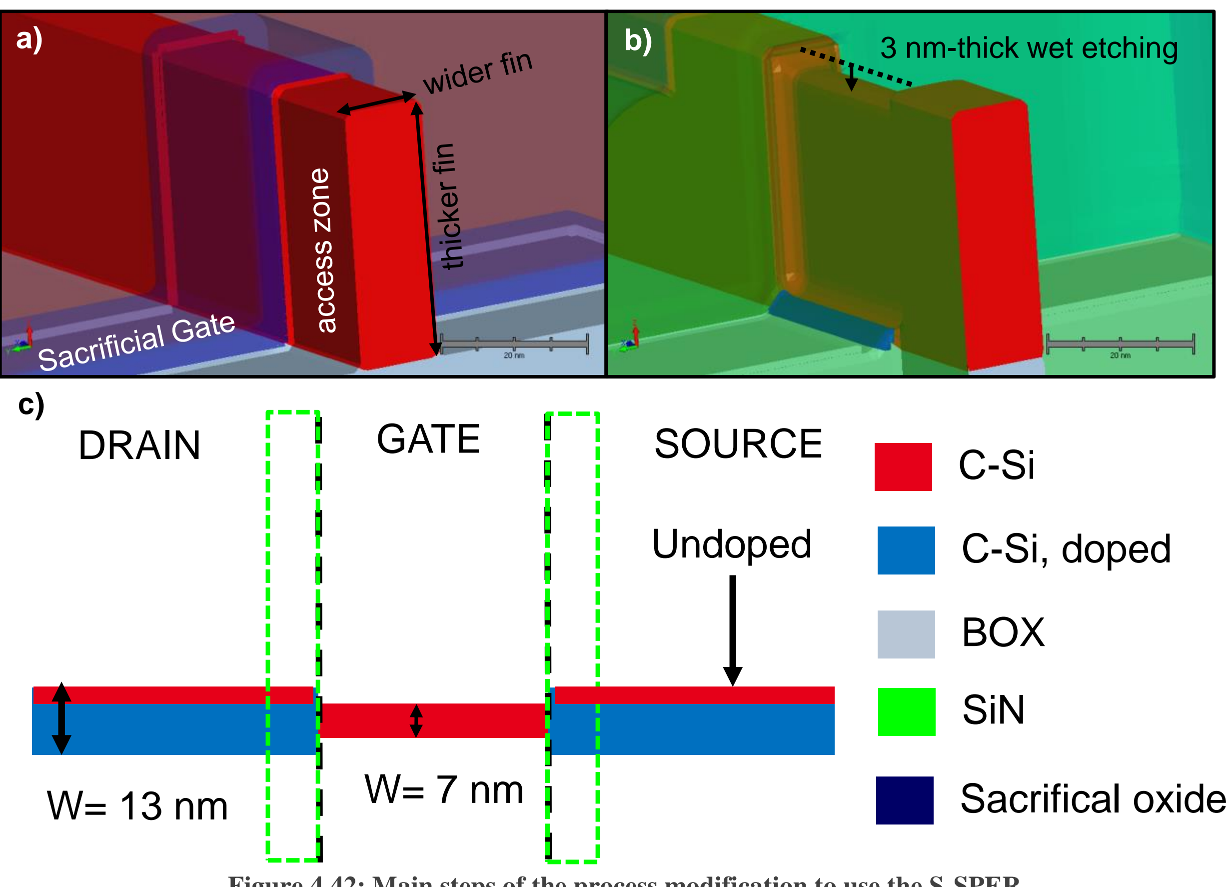


Figure 4.42: Main steps of the process modification to use the S-SPER

In comparison to the targeted-fin dimensions, the fin used in this configuration will be 6 nm-wider and 3 nm-higher than the original one in this example. Before the offset spacer deposition, a single-sided implantation is tuned to amorphize and to dope 10 nm of the fin on one side, leaving

3 nm at the other side of the fin non-doped but crystalline. A lateral SPER process is then performed to activate dopant in the previously amorphized layer (not shown here). After the sacrificial gate removal, a 3 nm-thick etching of the channel is carried out. The channel dimensions being equal to the targeted-fin ones, the electrostatic control is maintained into the channel, as was originally described by Chao *et al.* in [105].

Electrical simulations have been performed to evaluate this integration and are shown in Figure 4.43.b), between a fully-activated, 7 nm-wide, 35 nm-tall device, and with the S-SPER process, with a 13 nm-wide, 38 nm-tall fin perimeter. A view from above is added in Figure 4.43.a) for these two devices.

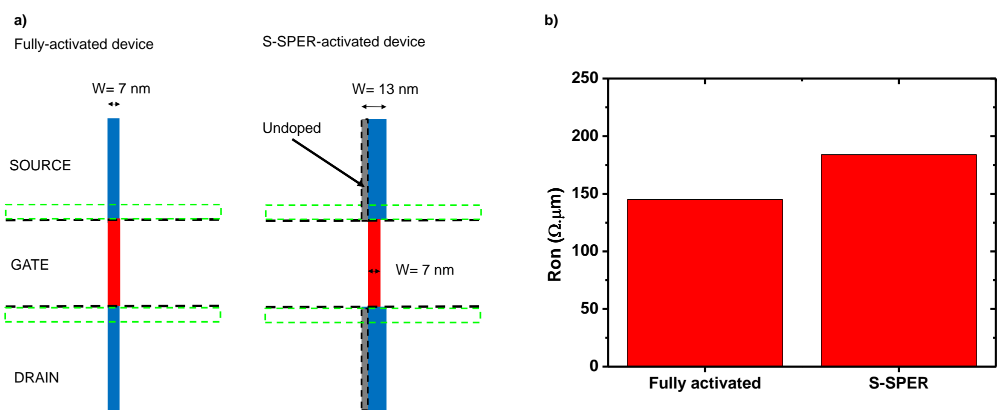


Figure 4.43: R_{on} comparison between a fully activated fin and the S-SPER process

The on-state resistance of the device with the S-SPER process is relatively close to a fully-activated one, with a 25 % degradation. It is however worth noticing that, in these simulations, an e-RSD epitaxy has not been take into account, which should result in lowering the R_{on} value, especially for the S-SPER process. This integration scheme might be thus considered as very interesting to manufacture low-temperature FinFETs.

Etching into the channel might will lead to supplementary parasitic capacitances. To illustrate the origin of these capacitances, Figure 4.44 represents the cross sections of the FinFET following the gate length (Figure 4.44.b)) and the fin width (Figure 4.44.c)) direction after gate formation. A view from above is added in Figure 4.44.a), to underline that the cut performed in Figure 4.44.c) is done at the gate edge.

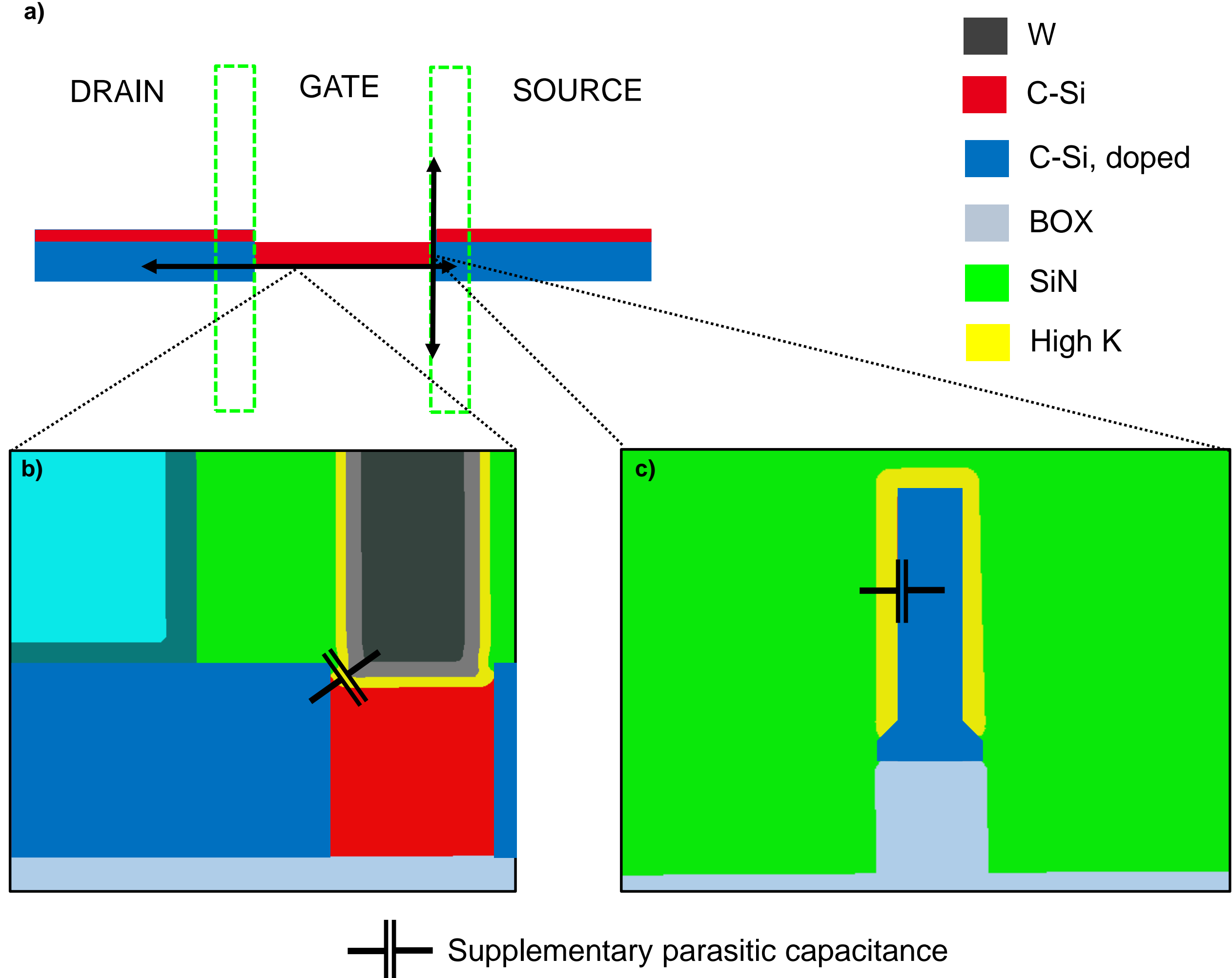


Figure 4.44: Cross sections following the fin width and gate length direction of FinFET after gate formation, with the channel etching step

Indeed, because of the supplementary anisotropic etching, the accesses are raised by 3 nm compared to the channel in Figure 4.44.b). In this region, the high-k is directly in contact with the accesses. Besides, high-k might also be present between the fin (with activated dopants) and the offset spacer, as shown in Figure 4.44.c).

In addition, the channel etching is performed without an etch-stop layer, which prevents a precise control of the etching depth. Figure 4.45 show the same pattern than in Figure 4.44.c), with an over etching.

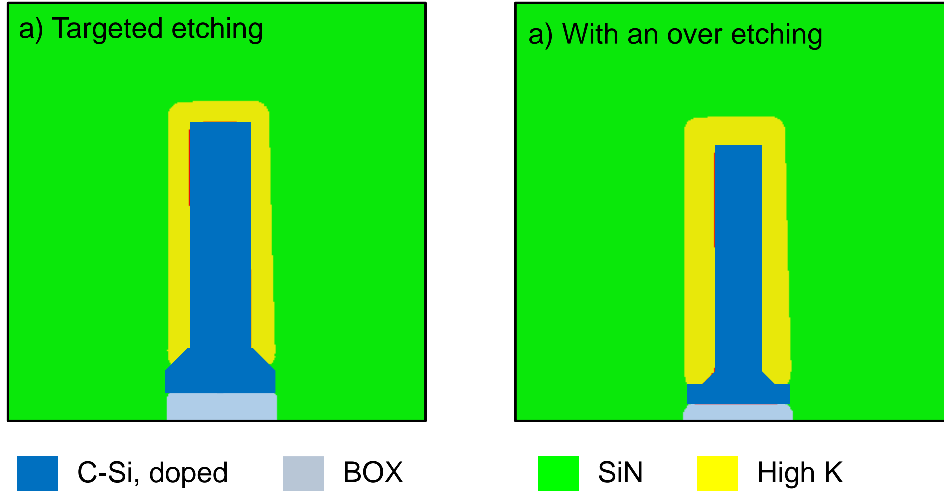


Figure 4.45: Cross sections following the fin width direction of FinFET after the gate formation, with the targeted channel etching, and with an over etching case

In an over etching configuration, the supplementary capacitance contribution will worsen. A simple solution to this issue might be to leave an amorphous layer in the access zone, which is will not be etched. In addition, due to the thicker fin, the fin space will be reduced, leading to also reduce the implantation angle. Further study is still mandatory to evaluate the interest of this alternative process flow.

C) NON-CONFORMAL HARD MASK

In this sub section, an integration optimization has been evaluated to overcome the possible recrystallization default at the top fin accesses. A technological solution is to form a capping layer at the top fin before implantation. The main steps are sketched in Figure 4.46 for a 7 nm-wide, 53 nm-tall fin. SiN has been defined as the cap layer in this example. The DSPER process is not shown for the sake of clarity.

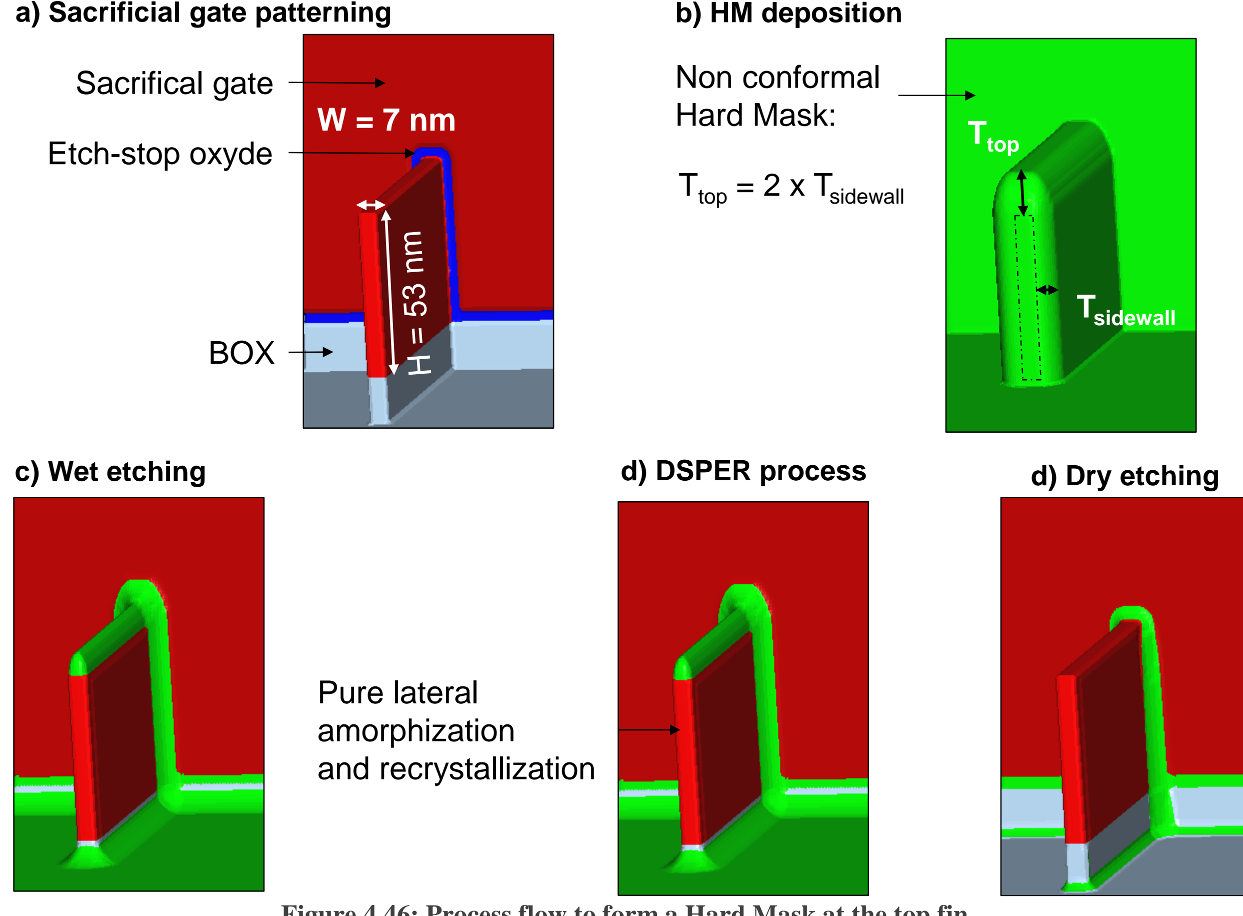
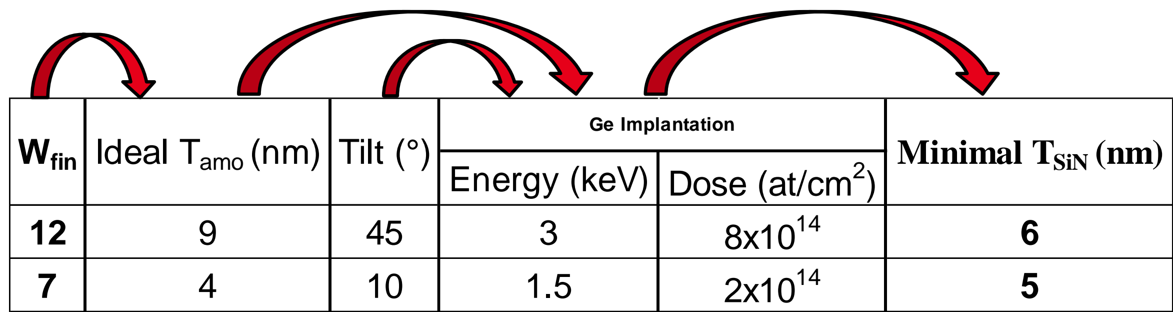


Figure 4.46: Process flow to form a Hard Mask at the top fin

Right after the sacrificial gate patterning, a non-conformal Hard Mask, i.e. with a top thickness superior to the sidewall one, is deposited. In this example, 10 nm-thick SiN has been deposited, with a lateral ratio defined at 50 %. A 5 nm-depth isotropic etching is then applied to consume the lateral thickness, leaving a 5 nm-thick cap layer on the fin accesses. A pure lateral amorphization might thus be obtained, with fully doped accesses thanks to the DSPER process. Because free surfaces are relatively far away from the recrystallization front in comparison to the recrystallization length, using this technological proposition, a unidirectional front should be involved in the recrystallization process, which will avoid recrystallization defects. If necessary, a dry etching might be applied after dopant activation to consume the capping layer.

According to the density of the material used as the Hard Mask, its thickness has to be tuned in order to avoid the amorphization of the top of the fin accesses. For specific implantation

conditions, the minimal thickness might be estimated as soon as the targeted amorphized thickness and the implantation tilt is defined. Table 4.2 shows two configurations, the first one being used in this work, and the second one being defined for a 14 nm node and with an implantation tilted defined at 10° to avoid shadowing effect. The minimal thickness has been calculated thanks to CTRIM simulation, by defining the SiN as the capping layer.



W_{fin}	Ideal T_{amo} (nm)	Tilt (°)	Ge Implantation		**Minimal T_{SiN} (nm)**
			Energy (keV)	Dose (at/cm^2)	
12	9	45	3	$8x10^{14}$	**6**
7	4	10	1.5	$2x10^{14}$	**5**

Table 4.2: Minimal SiN thickness according two implantations and node configurations

Thus, for a fin width of 12 nm, the ideal amorphized thickness configuration is equal to 9 nm, in order to leave 3 nm of the fin in a crystalline state. By defining the tilted implantation at 45° to avoid back scattering effect, the energy and dose of the amorphizing implantation has been chosen, which leads to estimate that 6 nm-thick SiN Hard Mask is mandatory to avoid amorphization of the top of the fin accesses, which is relatively thin. This thickness is about the same (5 nm) when the fin width and the tilt is reduced at respectively 7 nm and 10°. For further study, it is advised to estimate the compulsory thickness according the selected material, the fin width and implantation conditions.

D) CHANGING THE CHANNEL ORIENTATION

Another alternative may be to use another crystalline orientation to avoid recrystallization with <111> crystalline orientation. By patterning the active and gate zone along the <100> crystalline orientation, or changing the substrate orientation, no recrystallization default should occur, as observed by simulation in [106] for boron implantation. An illustration of the consequence of changing the channel orientation on the recrystallization mechanism is given in

Figure 4.47, which sketches the cross-section of a fin at the width direction, with a channel oriented either at the <110>-direction (Figure 4.47.a)), or at the <100>-direction (Figure 4.47.b)).

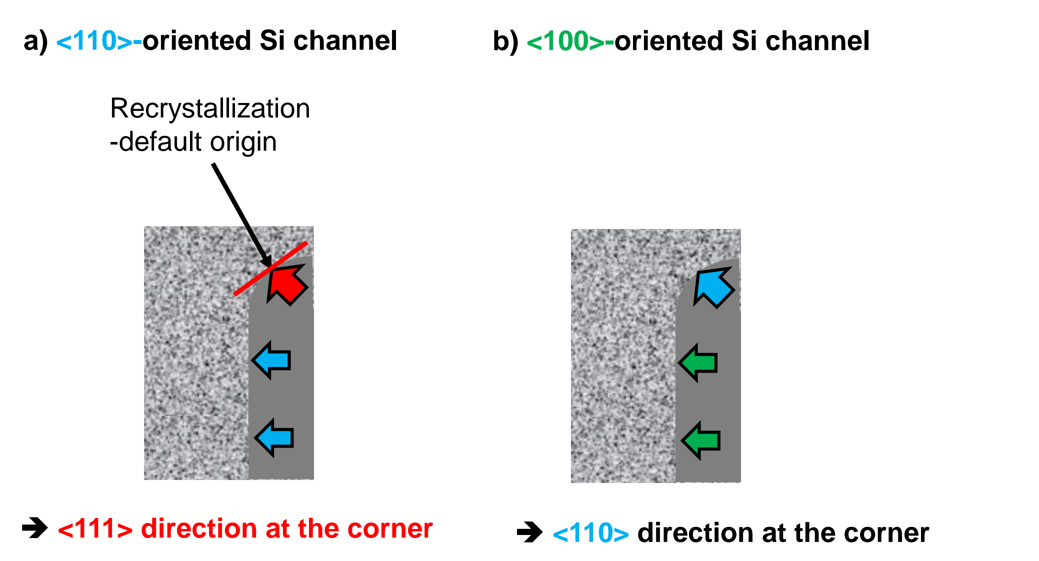


Figure 4.47: Illustration of the consequence of changing the channel orientation on the recrystallization mechanism

Thereby, a non-tilted implantation should be possible, even if the surface proximity might influence the recrystallization process, and this integration is called Orientation change and Non-Tilted (ONT) process. On planar MOSFETs, changing the orientation modifies the effective mass of the carrier, and therefore improve or degrade the channel mobility, according to the type of the FinFET. Changing from <100> to <110> channel orientation will improve hole mobility and degrade electron one. It has however been demonstrated in [107] and [108] that electron mobility is not impaired for FinFET on SOI, thus using a <110>-oriented channel appears to be an interesting solution. A full study for both p&n MOS has thus to be done, in order to give the best tradeoff between the recrystallization default and the crystalline orientation, with DSPER process and without tilted implantation.

E) <u>SPER BY PLASMA IMPLANTATION</u>

One solution to avoid angle restrictions (see sub section 4.2.2) is to implant at twist 0°. With such an orientation, the maximum achievable angle is released. Twisted and non-twisted implantations are illustrated in Figure 4.48, for the same tilt.

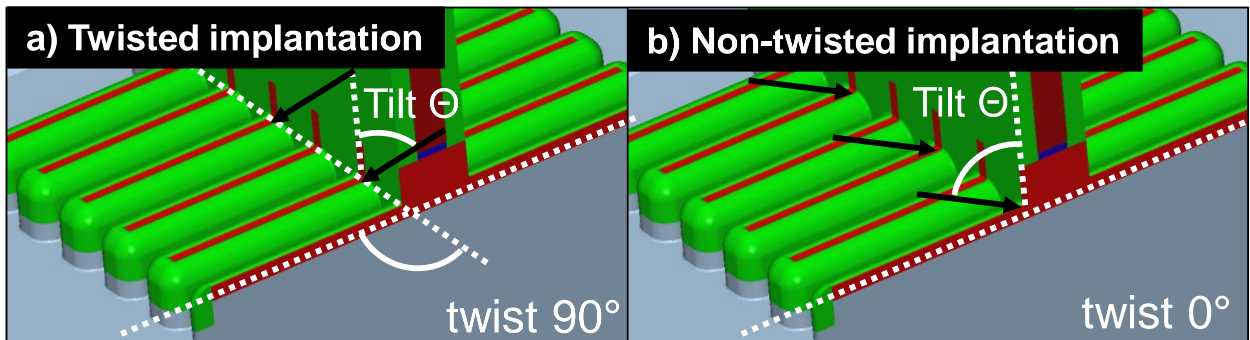


Figure 4.48: Illustration of a twisted and non-twisted implantation

Contrary to the twisted implantations, here implantations angle are not restricted, because the tight pitch between fins or the photo resist mask will not have an influence on the implantation below the offset spacer. Shadowing effects are thus overcome. An integration optimization with non-twisted implantation is evaluated here. It relies on recessing the fin after the first spacer formation, on doping the fin through implantation at twist 0°, and on using *in situ* raised source drain epitaxy. Such a process flow is represented in Figure 4.49 for a 7 nm-wide, 53 nm-high FinFETs. The new proposed process is called non-twisted SPER. In this example, the offset spacer will be 10 nm-thick.

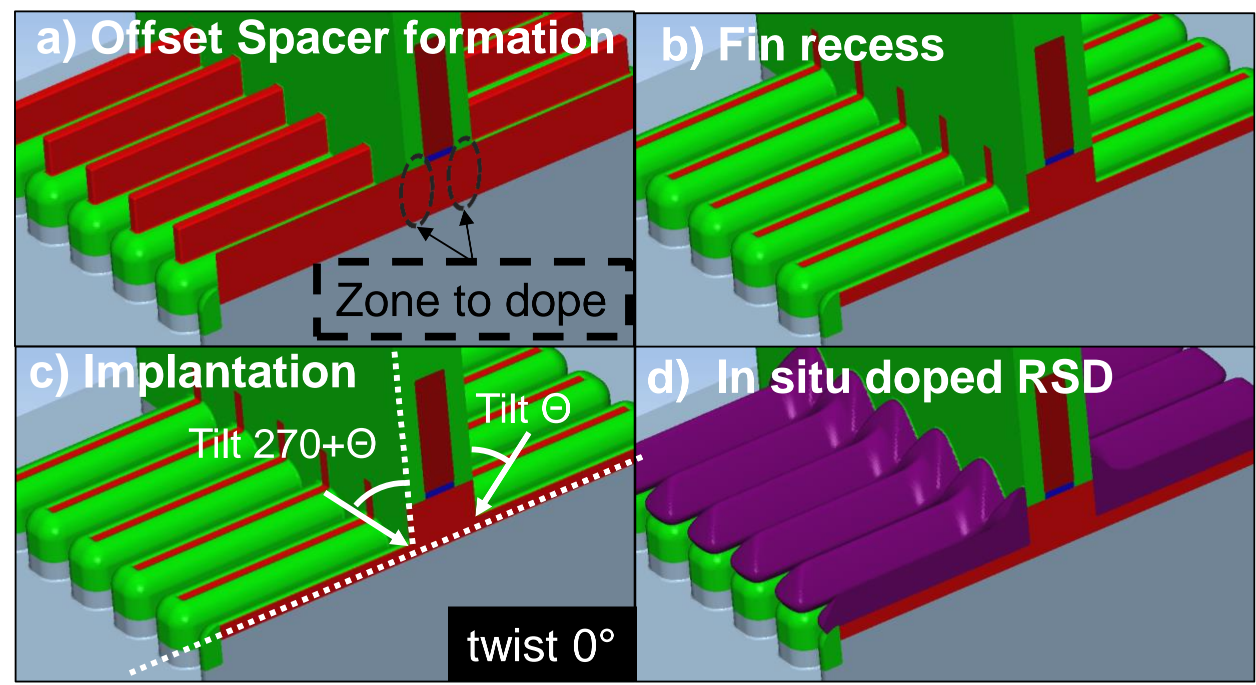


Figure 4.49: Main steps of the non-twisted SPER

After the offset spacer formation, a recess is performed. Implantations are then carried out at twist 0° as illustrated in Figure 4.49.c), with a certain tilt Θ to dope below the offset spacer, as highlighted in Figure 4.49.a). These implantations has to be done twice, one for each side of the gate. The twist here is unchanged, and only the tilt has been varied (Θ° and 270°+Θ°), but it is possible to keep the tilt, and to twist twice the wafer (0° and 180° in this example). A small annealing is then carried out to activate dopants (not shown here), followed by *in situ* doped raised source drain epitaxy to lower access resistances. In this configuration, even if implantations are carried out twice, one for each side of the gate, recrystallization will be only performed once, decreasing the wafer cost in comparison to the DSPER process. Several limitations might be viewed with such a process flow.

The recrystallization mechanism involved in this configuration is to use the channel as a seed. With a channel oriented among the <110> crystalline orientation, twin defects will be expected, as evidenced in the chapter 2. Changing the channel orientation might be compulsory to avoid recrystallization default. Besides, the targeted tilt has to be equal to 90° in order to fully dope the area under the first spacer. By using beam line implantations, this angle is not physically

achievable, and plasma implantation might be viewed as a good alternative. However, plasma implantation will lead to a very high dopant activation of at the fin surface (above 1×10^{21} at/cm^3) [85], and the epitaxy regrowth on such a surface could be an issue [109], [110]. Besides, as shown in the TEM picture in Figure 4.19.b) and Figure 4.20.b), the SPER rate drops near to the free surfaces. A defective layer due to the over doping or to the oxygen recoil might thus be expected. A thin etching to consume this defective layer after the implantation should be carried out. A more important issue is highlighted in Figure 4.50, which represents the fin-width cross-section of a FinFET after the recess. In this example, the offset spacer is 10 nm-thick, while the remaining seed is 8 nm-thick.

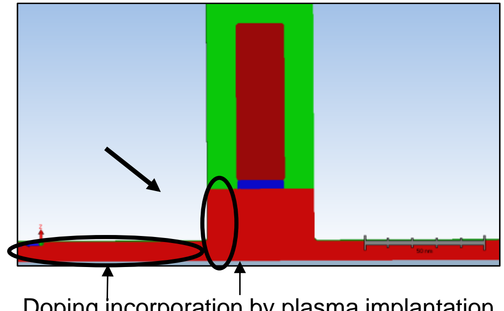


Figure 4.50: Fin-width cross section after the recess

By incorporating dopants after the recess, and in order to dope under the first spacer, the bottom of the fin will also be doped. Because the only crystalline seed is relatively far from this zone, and because the free surfaces are very close, no recrystallization is expected, which is an issue for the epitaxy process. A trade-off between the offset spacer thickness and the bottom fin one after the recess is needed. A variation of the offset spacer will lead to a variation of the offset capacitance, and is thus not advised. Another solution is to keep the targeted spacer thickness, to recess the fin in order to keep a relatively-thick fin bottom, to perform implantations and then to etch the film. An illustration of such a process flow is shown in Figure 4.51, which represents the fin-width cross-section of a FinFET.

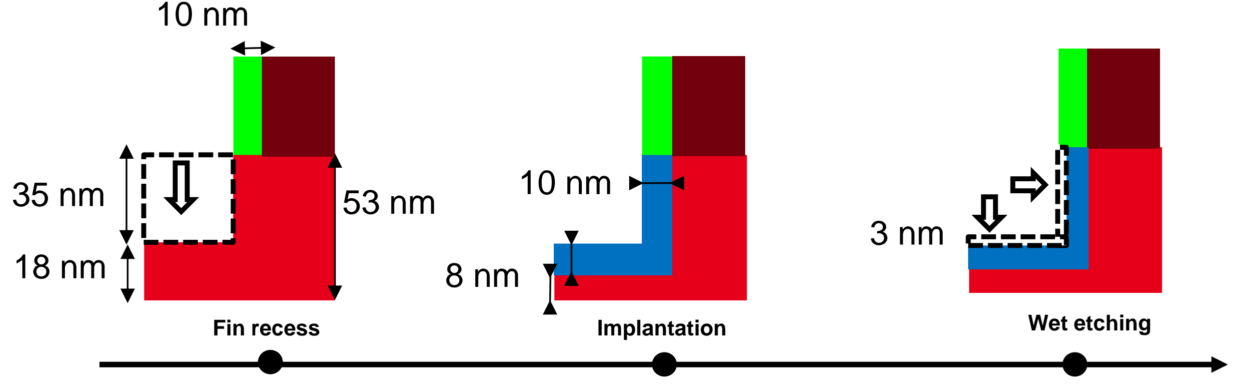


Figure 4.51: Main steps of the NTP process

For a 14 nm design rule, the fin height is equal to 53 nm, while the offset spacer might be 10 nm-large. After the offset spacer formation, a 35 nm-thick recess is carried out, followed by the non-twisted plasma implantation. Implantation conditions have to be tuned to amorphize 10 nm below the offset spacer. A wet etching is then carried out in order to consume the first nanometer, over doped or possibly amorphous. In this new configuration, the fin bottom will not be amorphized, enabling to perform the *in situ* doped raised source drain epitaxy (not shown here). However, at the bottom of the fin, a zone will not be doped. This zone being far from the spacer, it does not necessarily mean that the R_{on} value will be degraded.

The recrystallization should however be defect-free because all the fin will be implanted, but for further investigation is mandatory to evaluate the performances with such a process flow.

4.5.1 Summary of integration schemes

As seen in the previous section, many paths might be investigated to fully dope the accesses of FinFET device with low thermal budget. Table 4.3 summarizes the advantages and drawbacks of these integration-scheme propositions.

		Will the proposed integration influence …			
		DSPER	S-SPER	Plasma	Orientation
… the static performance?	R_{on}	--	-	TBQ	TBQ
	mobility	++	++	TBQ	TBQ
… the dynamic performance?	parasitic capacitance	++	--	++	++
… the device structure?		(1) (2)	(2) (3)		

TBQ: To Be Quantified

(1) For DSPER, a HM is mandatory to be CMOS compatible
(2) Risk of fin bending/fin collapse due to the non conformal Hard Mask
(3) The fin space will be reduced due to the wider fin

Table 4.3: Summary of integration optimizations

To be CMOS compatible, using the DSPER process requires to change the photoresist mask by a Hard Mask. With such a modification, the angle tilt for beam implantation is only improved up to 25°, and this will influence the access resistances (and thus, the R_{on}). Besides, a non-conformal hard mask appears to be mandatory in order to avoid recrystallization defaults, which might result to a fin collapse or a fin bending.

It has been evidenced, for the S-SPER with an etching of the channel, that a R_{on} degradation is expected, as well as a supplementary parasitic capacitance. The need to use the non-conformal hard mask to avoid recrystallization default might also degrade the fin integrity.

Plasma implantation followed by a wet etching seems to be an interesting option in order to fully dope the area below the offset spacer. It might however be mandatory to change the channel orientation to avoid recrystallization default due to the presence of the <111>-crystalline orientation during the recrystallization mechanism.

Finally, changing only the channel orientation and using a non-tilted implantation should avoid the issues shown for the DSPER and the S-SPER process. This integration scheme appears thus to be the most interesting option to manufacture low-temperature FinFETs, but the influence on the static performances should be quantified.

To remember

FinFET junction schemes

- Doping implantation and activation have been challenging to achieve high performance for FinFET devices, especially due to:
  - the defect-crystalline integrity,
  - the angle restriction,
  - the conformal doping,
  - the fin bending.
- For these reason, embedded *in situ* doped raised source and drain epitaxy (e-RSD) might be viewed as the standard option to lower access resistances for high-temperature devices.
- Using e-RSD for low-temperature devices is feasible with silicon oxidation/desoxidation cycles. In addition, such a technique should enhanced the strain effect.

Proposition for low-temperature devices

- For low-temperature devices with implantation steps, several seed configurations have been investigated in order to lower the access resistance. Among them, the DSPER process, which consist in using twice the SPER process, one for each side of the fin, might be considered as the most pertinent configuration.

Fabrication and electrical characterization

- The DSPER process has been integrated into the fabrication of low-temperature FinFETS devices.
- It enables to reach high performance for low temperature devices (85 % for pMOS) with respect to the HT POR.
- Straggle effect and EORs have been observed, but should be reduced for a more aggressive fin width, due to the reduction of the implantation doses and energies.

Perspective:

- An amorphous layer that surrounds the fin is however expected with DSPER process, and several optimizations have been proposed in order to overcome this issue while maintaining the CMOS-compatibility. Among these integrations, changing the channel orientation might be considered as the most pertinent solution for manufacturing low-temperature FinFETs.

5. CONCLUSION

In order to keep increasing the density of integrated circuit, an alternative to the most advanced architectures, such as FDSOI or FinFET, which is additionally compatible with them, is offered by the 3D sequential integration scheme. It is also an active field in the CEA-LETI. One of the main challenge of such an integration is to be able to process a high performance transistor at the top tier with a low thermal budget (below 500 °C) in order to preserve the transistor at the bottom from any degradation. It has been shown in this thesis that one of the critical step consist in changing the dopant activation methodology, which is commonly performed with a high thermal budget (>1000 °C). The technological option chosen at CEA-LETI and for this work is to form the junction of top transistors with Solid Phase Epitaxial Regrowth (SPER) process, allowing to reduce the activation anneal at temperatures that are compatible with 3D sequential integration. Solid Phase Epitaxy Regrowth has thus been the main mechanism involved during this thesis to manufacture low-temperature devices. Besides, three different integration schemes (Gate First/Extension Last, Gate First/Extension First and Gate Last/Extension First) have been be investigated on two different architectures (FDSOI, FinFET) during this thesis in order to form the junctions for low-temperature devices.

A summary of the SPER process and its dependency has been explained in the chapter 2. The SPER rate mainly depends on three parameters (the temperature, the crystalline orientation, and the type of impurities and their concentrations). It has also been evidenced that implantation current plays a key role to control the seed thickness. Besides, due to the excess of interstitial at the amorphous/crystalline interface that occurs during implantations, several electrical degradations might occurred, such as a decrease of the I_{on} due to Boron-Interstitial Cluster (BIC), an increase of the DIBL due to Transient-Enhanced Diffusion (TED), or an increase of the $I_{d,min}$

due to Trap-Assisted Tunneling (TAT). It has been underlined that the TED effect might be reduced thank to carbon co-implantation.

In the chapter 2, a focus on the development of a 500 °C SPER activation process for both N and P FETs has been performed, using simulations and electrical characterizations. The origin of the poor performance of nMOS devices at 500 °C is attributed to a too small duration of the SPER anneal. At 500 °C, for a <100>-oriented channel and for phosphorous or boron dopants, the annealing time should not exceed 30 min. These data also show that a full access amorphization can allow the recrystallization at 500 °C. The amorphous/crystalline interface must however not be fully vertical. Besides, recrystallizing a fully amorphized S&D is only possible with a <100>-oriented channel. In a <110>-oriented channel, the apparition of twin defects will indeed stop the recrystallization. For pMOS devices, the degraded DIBL is attributed to a non-optimized boron concentration in the channel. A high electrical solubility of boron is furthermore observed in the region below the spacer and in the channel, up to 1×10^{19} at/cm^3 at 500 °C. This high value might be explained by the small interstitial concentration in that region where two interstitial sinks are present at a distance of 6 nm, or by the absence of point defects due to implantations. To optimize the DIBL in future devices, it is thus advised to reduce the boron concentration at the channel entrance, below 1×10^{19} at/cm^3.

In the chapter 3, different solutions have been given in order to optimize the Extension First integration scheme, which consists in implanting before the epitaxy, at the gate edge. It enables to reach high performance for low temperature devices (95 % for pMOS, 90 % for nMOS) with respect to the HT POR, as studied in the previous thesis. The doping of the region below the offset spacer has been identified as the main critical limitation for LT devices. Implanting through a nitride liner lead to nitrogen recoil in the amorphous region, and must be avoided. A maximum R_{sheet} of 10 kΩ/sq must indeed be obtained in order to reach the same R_{spa} than the HT POR. It has

been demonstrated that avoiding the nitrogen recoil enables to improve R_{sheet} by a 94 % (respectively 36 %) for n-type (respectively p type) samples. All R_{sheet} values are additionally below 10 kΩ/sq at 600 °C. To be CMOS-compatible, Extension First/Gate Last integration scheme seems to be more suitable, but will be more expensive to be manufactured. Nevertheless, junctions will be perfectly aligned at the gate edge. Besides, a method to extract EOT variation has been proposed, based on gate current measurement. This enables a more precise extraction of the EOT variation between long and short channel. To ensure unbiased extraction, it has been advised to remove outlier data, to measure the gate current at low drain voltage and high gate voltage, and to ensure that no gate resistance can distort the measurements. An EOT regrowth had been evidenced by advanced electrical characterization for nFETs, attributed to an oxygen ingress. To overcome this issue, a small treatment by HF cleaning before the spacer complement deposition might be applied.

Finally, in the chapter 4, manufacturing low-temperature FinFETs has been investigated. Doping implantation and activation have been challenging to achieve high performance for FinFET devices (even with high thermal budget), especially due to the defect-crystalline integrity, the angle restriction, the conformal doping and the fin bending. For these reasons, embedded *in situ* doped raised source and drain epitaxy (e-RSD) might be viewed as the standard option to lower access resistances for high-temperature devices. Using e-RSD for low-temperature devices is feasible with oxidation/desoxidation cycles. In addition, such a technique should enhanced the strain effect. For low-temperature devices with implantation steps, several seed configurations have been investigated in order to lower the access resistance. Among them, the DSPER process, which consist in using twice the SPER process, one for each side of the fin, might be considered as the most pertinent configuration. An amorphous layer that surrounds the fin is however expected, and several optimizations have been proposed in order to overcome this issue while maintaining the CMOS-compatibility. Among these optimization integration, Non-Twisted Plasma (NTP)

implantations or changing the fin orientation might be considered as the most relevant solutions for further investigation. The DSPER process has been integrated into the fabrication of low-temperature FinFETS devices. It enables to reach high performance for low temperature devices (85 % for pMOS) with respect to the HT POR. Straggle effect and EORs have been observed, but should be reduced for a more aggressive fin width, due to the reduction of the implantation doses and energies.

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RESUME EN FRANÇAIS

Contexte technologique

La réduction des dimensions des dispositifs MOSFET devient de plus en plus complexe à réaliser, et les nouvelles technologies MOSFET se confrontent à de fortes difficultés. Pour surmonter ce problème, une nouvelle technique, appelée intégration 3D VLSI, est étudiée : remplacer la structure plane conventionnelle par un empilement vertical de transistors. Cette technique permet d'obtenir une meilleure performance comparée à des transistors de même dimension.

En particulier, l'intégration 3D séquentielle ou CoolCube™ au CEA-Leti permet de profiter pleinement de la troisième dimension en fabriquant séquentiellement les transistors. La réalisation d'une telle intégration apporte une nouvelle contrainte, celle de fabriquer le transistor du dessus avec un budget thermique faible (inférieur à 500 °C), afin de préserver les performances du transistor d'en dessous. Puisque ce budget thermique est principalement influencé par l'activation des dopants (>1000 °C), plusieurs techniques innovatrices sont actuellement investiguées au CEA-LETI, afin de fabriquer le drain et la source.

Dans ce manuscrit, nous utiliserons la recristallisation en phase solide comme mécanisme pour activer les dopants (inférieures à 600 °C). L'objectif de cette thèse est donc de fabriquer et de caractériser des transistors dont l'activation des dopants est réalisée grâce à ce mécanisme, afin d'atteindre des performances similaires à des transistors réalisés avec un budget thermique standard. Ce travail est organisé autour de l'activation des dopants, et en trois chapitres, où chaque chapitre est spécifique à une intégration (« Extension Last »/ « Extension First », « Gate Last »/ « Gate First ») et à une architecture (FDSOI, FINFET) considérée.

Les principales différences entre les schémas d'intégrations utilisés dans cette thèse sont présentées à la Fig. A.

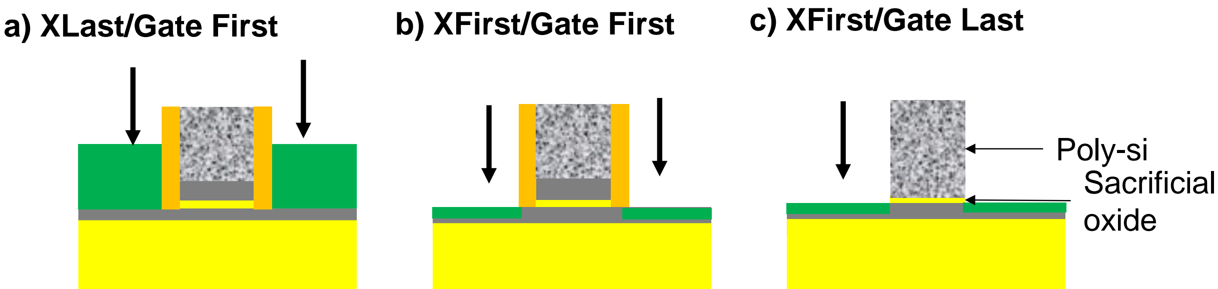

Fig. A: Principales différences entre les schémas d'intégration dits "Extension First/Extension Last" et "Gate First/Gate Last"

Le schéma d'intégration dit « Extension Last » consiste à utiliser le procédé dit SPER après l'épitaxie des sources et drains, tandis que le schéma d'intégration dit « Extension Last » consiste à implanter avant l'épitaxie des sources et drains, ce qui permet de positionner les jonctions à l'aplomb de la grille. Le schéma d'intégration dit « Gate Last » permet d'implanter à l'aplomb de la grille, alors que le schéma « Gate First » nous oblige à déposer puis graver un espaceur, afin de protéger la grilles des implantations, et d'éviter la contamination des machines par le métal de la grille.

Chapitre 1

Etude de l'intégration dite « Extension Last » sur des transistors de type FDSOI, fabriquée à faible budget thermique

Dans ce premier chapitre, le mécanisme de recristallisation par épitaxie en phase solide (« Solid Phase Epitaxy Regrowth, dit SPER en anglais) est en premier lieu expliqué. Cette technique repose sur la recristallisation d'un silicium amorphisé des dopants à partir d'une couche monocristalline, comme montré dans la Fig. B.

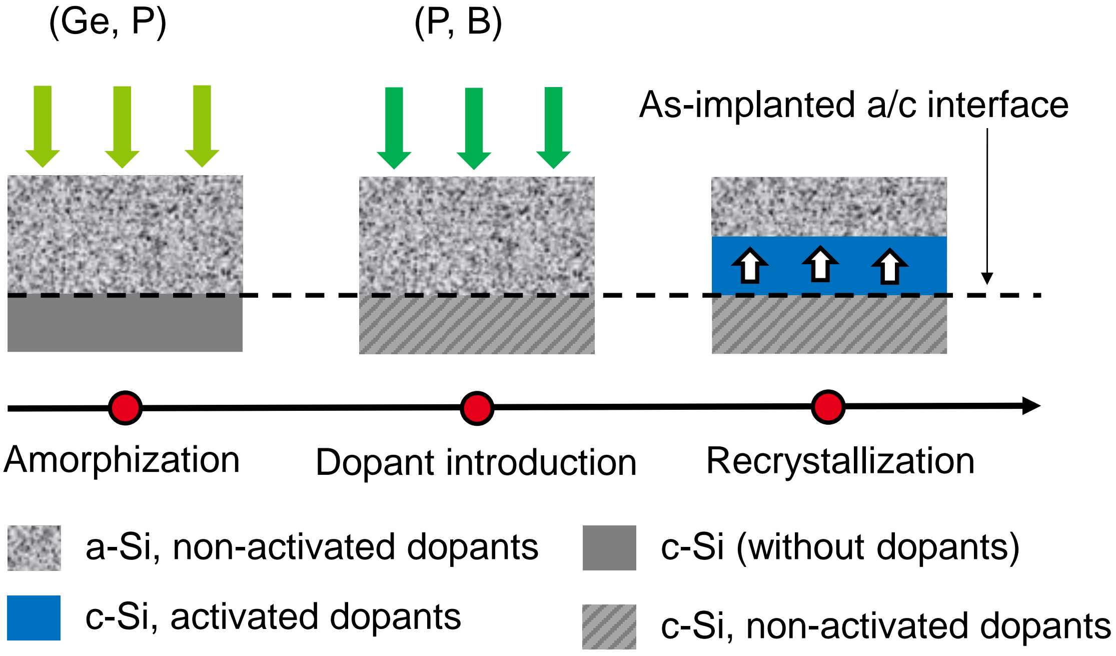

Fig. B: Illustration du procédé dit SPER

L'amorphisation du substrat monocristallin et l'incorporation des dopants sont réalisés dans cette thèse par implantation ionique, tandis que la couche amorphisée est recristallisée grâce à un recuit thermique. Ce recuit est compatible avec l'intégration 3D séquentielle, puisqu'il est possible d'utiliser des températures de recuit inférieurs à 600 °C.

Ensuite, l'influence de différents paramètres sur ce procédé est expliquée, telles que l'orientation cristalline du substrat, le type d'impuretés incorporées (volontairement ou non), leurs concentrations dans le substrat, ou la température de recuit. Ceci a permis d'estimer et de résumer la vitesse de recristallisation selon ces paramètres. Dans cette thèse, il a aussi été démontré l'importance du courant d'implantation sur la profondeur d'amorphisation.

De plus, les implantations conduisent à générer un excès de silicium en position interstitielle (Si_i) à l'interface de la zone amorphe et de la zone cristalline. Cet excès peut entrainer la formation de défauts dits EOR, conduisant à des effets indésirables dans notre cas, telle qu'une formation d'agglomérat, de diffusion transitoire accélérée, ou d'effets tunnel assisté par piège. Ceci peut amener plusieurs dégradations électriques, telles qu'un abaissement du I_{on} ou du R_{on}, une augmentation du DIBL ou du $I_{d,min}$, comme illustrées à la Fig. C.

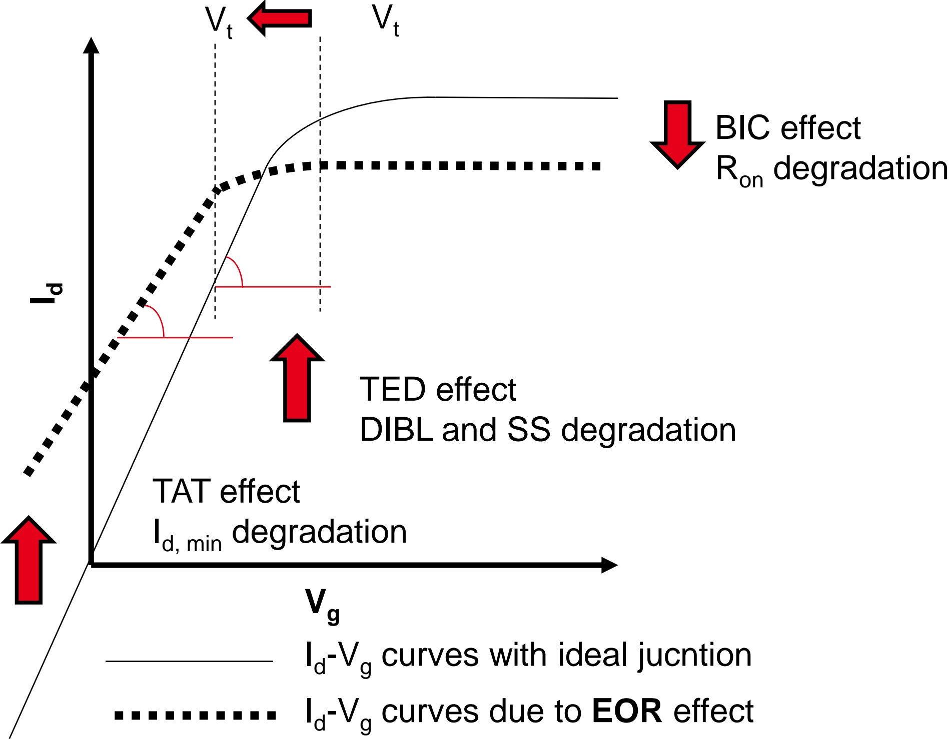

Fig. C: Résumé des dégradations sur les courbes Id-Vg que l'on peut s'attendre dues aux défauts dit EOR

Ces phénomènes peuvent être endigués lorsque qu'une couche amorphe se situe relativement près de l'interface entre la couche amorphe et la couche cristalline. Il a aussi été souligné qu'une utilisation d'une co-implantation d'espèce neutre, tel que le carbone, permet de réduire l'effet de diffusion.

Par la suite, nous nous sommes penchés sur le développement de ce procédé avec un recuit à 500 °C, à la fois pour les nMOS et pour les pMOS, pour des dispositifs qui ont été fabriqué à partir du schéma d'intégration dit « Extension Last », pour l'architecture FDSOI. En effet, à partir de résultats électriques, il a été observé des dégradations électriques, différentes selon le type de transistor (dégradation et résultat dispersé du I_{on} et du R_{on} pour le nMOS, dégradation résultat dispersé du DIBL pour le pMOS), comme indiqué à la Fig. D.

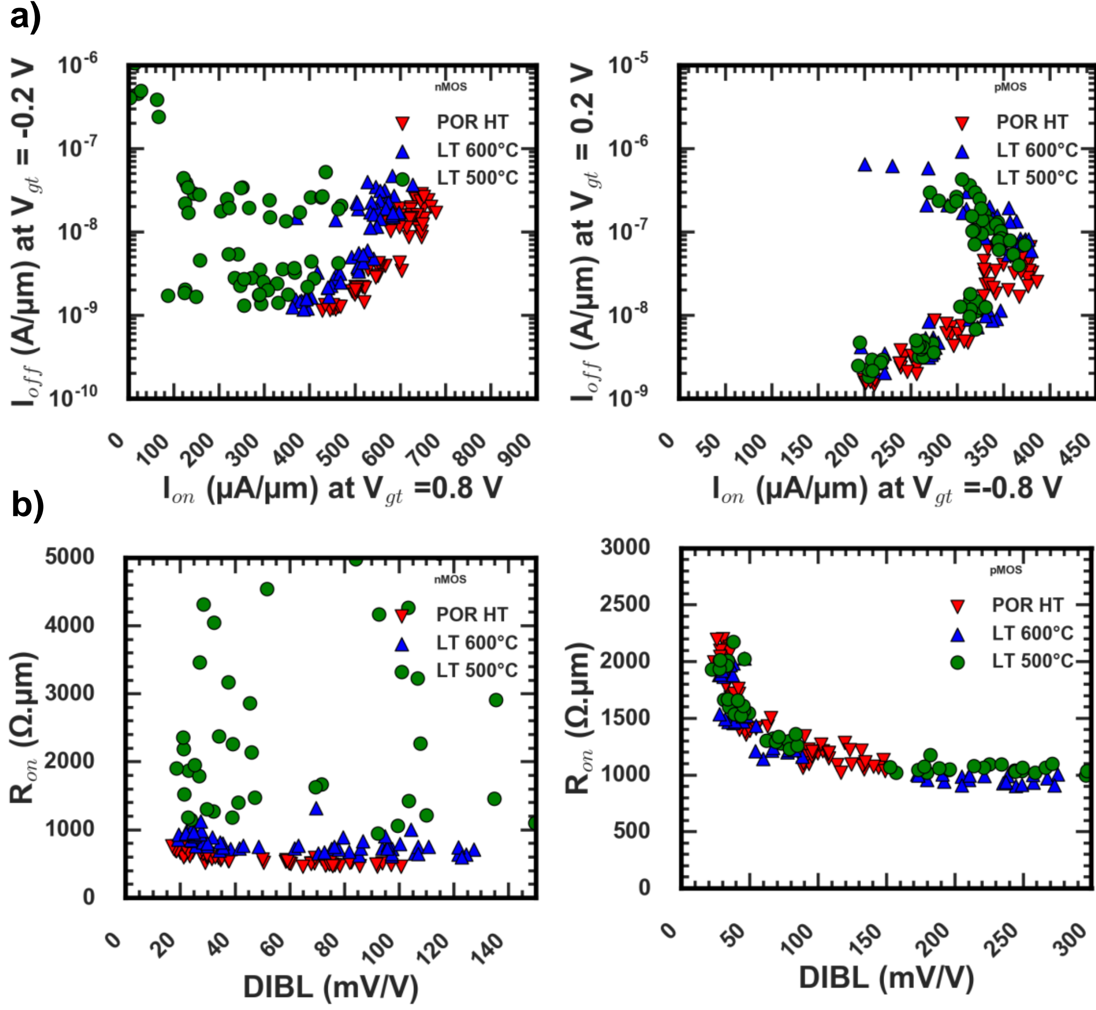

Fig. D : Ion-Ioff et Ron -DIBL pour les nMOS et les pMOS

L'origine de la faible performance des dispositifs nMOS avec un budget thermique de 500 °C est attribuée à une durée de recuit de recristallisation trop faible, ce qui a conduit à une recristallisation partielle des dispositifs, comme montré à la Fig. E.

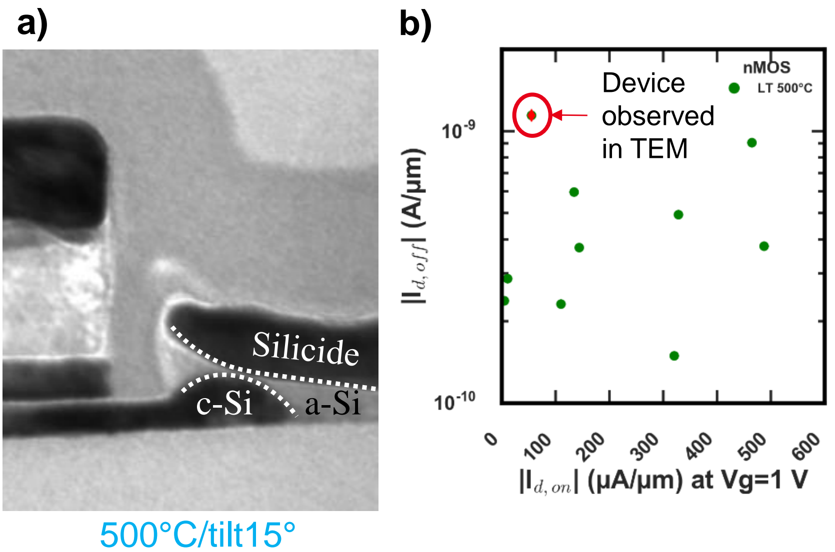

Fig. E : a) Observation TEM d'un dispositif active à 500 °C et b) performance du dispositif observé

Il a aussi été conclu que, sauf certaines conditions, recristalliser des sources et drains qui ont été totalement amorphisé est aussi possible.

L'origine de la faible performance des dispositifs pMOS est, quant à elle, attribuée à une concentration non négligeable de bore actif dans le canal. Ceci peut être corrélé à une solubilité électrique du bore relativement élevé, qui peut être expliqué par une faible concentration d'interstitielle ou une absence de points défectueux dans cette région. Il a donc été conseillé de réduire la concentration de bore dans le canal.

Chapitre 2

Etude de l’intégration dite « Extension First » sur des transistors de type FDSOI, fabriquée à faible budget thermique

Dans ce second chapitre, différentes solutions sont données afin d’améliorer l’utilisation du schéma d’intégration dit ‘Extension First’ pour l’architecture FDSOI et pour des transistors réalisés à basse température.

Ce schéma d’intégration consiste à implanter avant l’épitaxie des sources et drains, ce qui permet de positionner les jonctions à l’aplomb de la grille. Ce schéma d’intégration a permis d’atteindre des performances similaires à des transistors réalisés avec un budget thermique standard, et a été montré dans une thèse ultérieure [ref luca].

Il a été montré que les principales limitations des transistors réalisés à basse température par ce schéma d’intégration est dû à l’implantation à travers une couche de nitrure. Cette implantation fait en effet déplacer les atomes de nitrure vers la couche amorphisée, ce qui a pour conséquence de réduire la concentration des dopants actifs. Il a en effet été démontré par des résultats morphologiques, qu’éviter un tel phénomène permet de réduire les résistances d’accès, comme le montre la Fig. F.

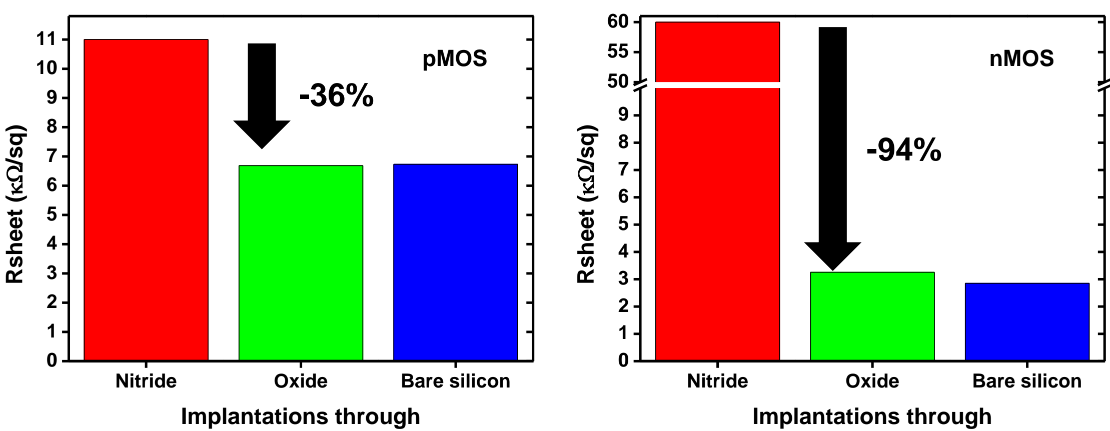

Fig. F: Résultat Rsheet des implantations de type n et p, dont le substrat est surmonté d'une couche de nitrure, d'une couche d'oxyde, ou est à nue.

Enfin, pour que cette intégration soit compatible CMOS, il a été suggéré d'utiliser l'intégration dit 'Extension Last/Gate Last', même si cela entraîne une augmentation du coût des dispositifs.

En outre, une méthode d'extraction plus précise de la variation de l'EOT pour les faibles longueurs de grilles a été proposée. Cette nouvelle méthode permet de mettre en évidence une recroissance de l'EOT pour les faibles longueurs de grille et pour les nMOS, comme indiqué à la Fig. G.

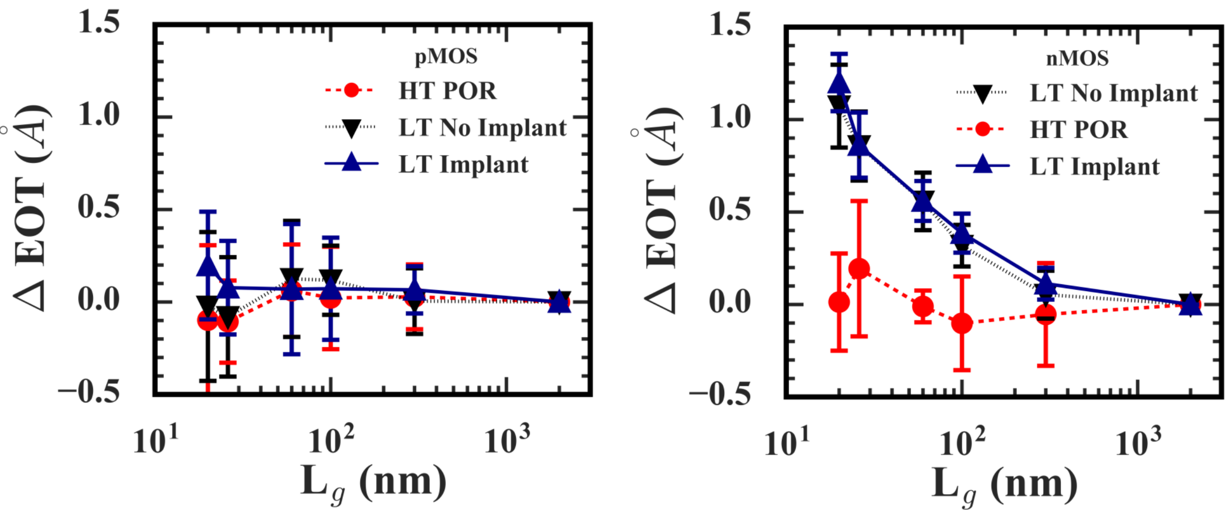

Fig. G: Variation ΔEOT en fonction de la longueur de grille

Cette augmentation de l'EOT amène donc une limitation des performances, notamment sur le I_{on}. L'origine de cette recroissance a été attribuée à l'entrée de l'oxygène dans la grille, due à l'intégration utilisée, mais aussi à cause du substrat, qui contribue à la vitesse d'oxydation. Un nettoyage HF adéquat devrait cependant permettre de résoudre cette limitation.

<u>Chapitre 3</u>

Etude de l'intégration dite « Extension First » sur des transistors de type FINFET, fabriquée à faible budget thermique

Enfin, dans le dernier chapitre, la fabrication à basse température de transistor utilisant l'architecture dit FinFET et le schéma d'intégration dit « Extension First » a été investigué. En premier lieu, un éclaircissement des différents défis liés à l'implantation ionique et l'activation de dopants (même avec un budget thermique standard) dans cette architecture a été réalisé. Il a notamment été mis en évidence que l'intégrité du « fin », la restriction de l'angle d'implantation, la difficulté d'obtenir un dopage conforme dans les accès, et la possibilité que le « fin » puisse se pencher ou s'effondrer, sont des phénomènes qui limitent la performance de ces dispositifs. Pour ces raisons (entre autre), l'utilisation de la recroissance par épitaxie dopé *in situ* et enterré a été préférée chez les industriels, et peut donc être vu comme l'option standard pour réaliser des transistors avec un budget thermique standard.

Avec un faible budget thermique, il a été montré qu'il serait aussi possible d'utiliser cette méthode (donc sans implantations), grâce à des cycles d'oxydation et de désoxydations du silicium dans les accès.

La fabrication de transistor en utilisant les implantations ioniques a tout de même été investigué, et différents schémas de recristallisation ont été comparés. Il a été conclu qu'utiliser le procédé dit DSPER (Double SPER), proposé dans cette thèse, peut être vu comme l'option la plus

pertinente parmi les différents schémas. Ce procédé consiste à utiliser deux fois le procédé SPER, un pour chaque côté du fin, comme illustré à la Fig. H.

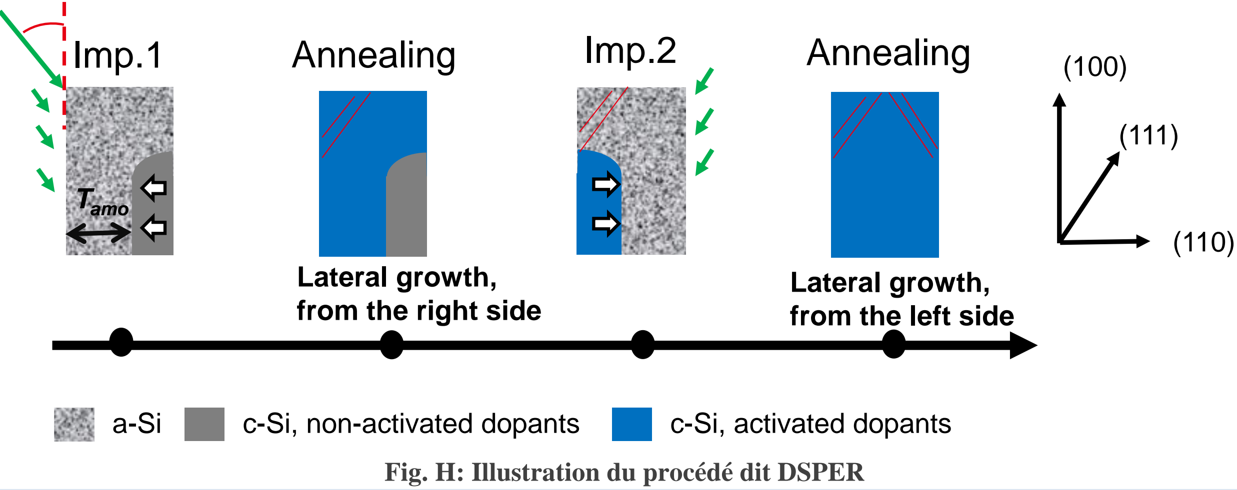

Fig. H: Illustration du procédé dit DSPER

Ce procédé a été utilisé dans la fabrication de dispositifs pMOS réalisés à basse température, et permet d'atteindre des performances proches des transistors réalisés avec un budget thermique standard. Plusieurs effets indésirables ont été montrés, comme l'effet d'extension des dopants durant l'implantation (« straggle effect » en anglais), ou la diffusion transitoire accélérée. Leurs impacts sur les performances des dispositifs devraient être cependant réduits pour des nœuds plus avancés, car nécessitent des doses et des énergies d'implantations moindres.

Il a enfin été mis en évidence que le procédé DSPER n'est pas compatible CMOS, dû notamment à la nécessité de recuire deux fois les dispositifs, et que la résistance des accès pouvait encore être réduit, en évitant notamment les défauts de recristallisation. Différentes intégrations ont alors été proposées comme perspective de fabriquer des transistors de type FinFET avec un

faible budget thermique, afin de s'affranchir de ces problèmes. Parmi elles, l'utilisation d'un canal orienté différemment peut être considérée comme le plus pertinente, comme illustré à la Fig. I.

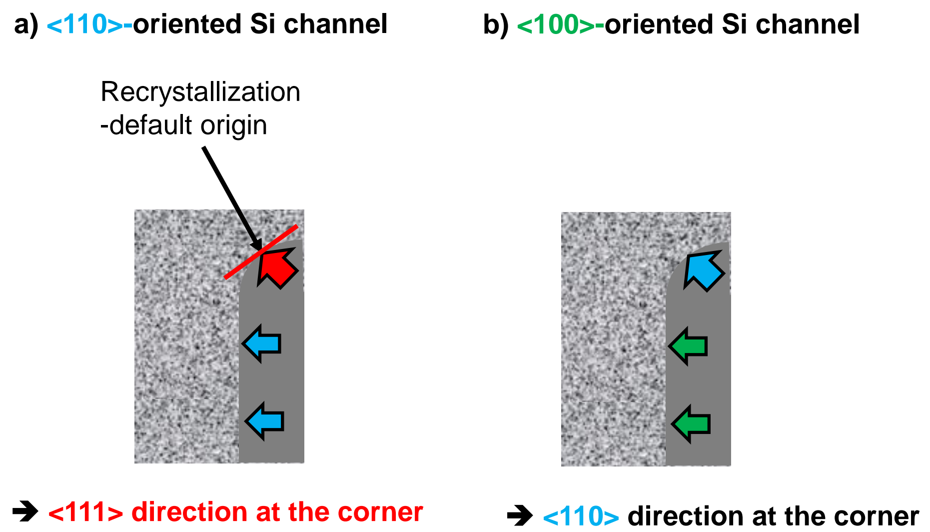

Fig. I: Illustration de la conséquence de changer l'orientation du canal sur le mécanisme de recristallisation

Résumé

La réduction des dimensions des dispositifs MOSFET devient de plus en plus complexe à réaliser, et les nouvelles technologies MOSFET se confrontent à de fortes difficultés. Pour surmonter ce problème, une nouvelle technique, appelée intégration 3D VLSI, est étudiée : remplacer la structure plane conventionnelle par un empilement vertical de transistors. Cette technique permet d'obtenir une meilleure performance comparée à des transistors de même dimension. En particulier, l'intégration 3D séquentielle ou CoolCube™ au CEA-Leti permet de profiter pleinement de la troisième dimension en fabriquant séquentiellement les transistors. La réalisation d'une telle intégration apporte une nouvelle contrainte, celle de fabriquer le transistor du dessus avec un budget thermique faible (inférieur à 500 °C), afin de préserver les performances du transistor d'en dessous. Puisque ce budget thermique est principalement influencé par l'activation des dopants, plusieurs techniques innovatrices sont actuellement investiguées au CEA-LETI, afin de fabriquer le drain et la source. Dans ce manuscrit, nous utiliserons la recristallisation en phase solide comme mécanisme pour activer les dopants (inférieures à 600 °C). L'objectif de cette thèse est donc de fabriquer et de caractériser des transistors dont l'activation des dopants est réalisée grâce à ce mécanisme, afin d'atteindre des performances similaires à des transistors réalisés avec un budget thermique standard. Dans le **premier chapitre**, nous nous sommes penchés sur le développement de ce procédé avec un recuit à 500 °C. L'origine de la faible performance des dispositifs nMOS avec un budget thermique de 500 °C est attribuée à une durée de recuit de recristallisation trop faible, ce qui a conduit à une recristallisation partielle des dispositifs. Il a aussi été conclu que, sous certaines conditions, recristalliser des sources et drains qui ont été totalement amorphisé est aussi possible. L'origine de la faible performance des dispositifs pMOS est, quant à elle, attribuée à une concentration non négligeable de bore actif dans le canal. Ceci peut être corrélé à une solubilité électrique du bore relativement élevé, qui peut être expliqué par une faible concentration d'interstitielle ou une absence de points défectueux dans cette région. Dans le **second chapitre**, il est montré que les principales limitations des transistors réalisés à basse température est dû à l'implantation à travers une couche de nitrure. Cette implantation fait en effet déplacer les atomes de nitrure vers la couche amorphisée, ce qui a pour conséquence de réduire la concentration des dopants actifs. Il est en effet démontré par des résultats morphologiques, qu'éviter un tel phénomène permet de réduire les résistances des accès. En outre, une méthode d'extraction plus précise de la variation de l'EOT pour les faibles longueurs de grilles est proposée. Cette nouvelle méthode permet de mettre en évidence une recroissance de l'EOT pour les faibles longueurs de grille et pour les nMOS. L'origine de cette recroissance est attribuée à l'entrée de l'oxygène dans la grille. Un nettoyage HF adéquat devrait cependant permettre de résoudre cette limitation. Enfin, dans le **dernier chapitre**, la fabrication à basse température de transistor utilisant l'architecture dit FinFET est investigué, et différents schémas de recristallisation sont comparés. Il est conclu qu'utiliser le procédé dit DSPER (Double SPER), proposé dans cette thèse, peut être vu comme l'option la plus pertinente parmi les différents schémas. Ce procédé a été utilisé dans la fabrication de dispositifs pMOS réalisés à basse température, et permet d'atteindre des performances proches des transistors réalisés avec un budget thermique standard. Afin de réduire encore plus les résistances des accès, en évitant notamment les défauts de recristallisation, différentes intégrations sont proposées comme perspective de fabriquer des transistors avec un faible budget thermique.

Abstract

The down scaling of MOSFET device is becoming harder and the development of future generation of MOSFET technology is facing some strong difficulties. To overcome these issues, the vertical stacking of MOSFET in replacement of the conventional planar structure is currently investigated. This technique, called 3D VLSI integration, attracts a lot of attention, in research and in the industry. Stacking transistors enables indeed to gain in density and performance without reducing transistors dimensions. More specifically, 3D sequential integration or CoolCube™ at CEA-Leti enables to fully benefit of the third dimension by sequentially manufacturing transistors. Implementing such an integration provides the new constraint of manufacturing top transistor with low thermal budget (below 500 °C) in order to preserve bottom-transistor performances. As most of the thermal budget is due to the dopant activation, several innovative techniques are currently investigated at CEA-LETI. In this work, solid phase epitaxy regrowth will be used as the mechanism to activate dopants below 600 °C. The aim of this thesis is thus to manufacture and to characterize transistors with low-temperature dopant activation, in order to reach the same performance as devices manufactured with standard thermal budget. In the **first chapter**, we will focus on the development of a new and stable 500 °C SPER activation process, assisted by relevant simulations and electrical characterizations. The origin of the poor performance of nMOS devices at 500 °C is attributed to a too small duration of the SPER anneal. These data also show that a full access amorphization can allow the recrystallization at 500 °C. For pMOS devices, the degraded DIBL is attributed to a non-optimized boron concentration in the channel, which might be due to a high electrical solubility of boron, observed in the region below the spacer and in the channel. This high value might be explained by the small interstitial concentration in that region, or by the absence of point defects due to implantations. In the **second chapter**, the doping of the region below the offset spacer has been identified as the main critical limitation for LT devices. Implanting through a nitride liner lead indeed to nitrogen recoil in the amorphous region, and must be avoided. Besides, a method to extract EOT variation has been proposed, based on gate current measurements. This enables a more precise extraction of the EOT variation between long and short channel. An EOT regrowth had been evidenced and attributed to an oxygen ingress. To overcome this issue, a small treatment by HF cleaning before the spacer complement deposition might be applied. In the **third chapter**, manufacturing low-temperature FinFETs has been investigated. The DSPER process, which consist in using twice the SPER process, one for each side of the fin, might be considered as the most pertinent configuration in order to lower the access resistance. This configuration process has been integrated into the fabrication of low-temperature FinFET devices. It enables to reach high performance for low temperature devices with respect to the HT POR. Straggle effect and EORs have however been observed, but should be reduced for a more aggressive fin width, due to the reduction of the implantation doses and energies.