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(54) **COMBINED BRANCH TARGET AND PREDICATE PREDICTION FOR INSTRUCTION BLOCKS**

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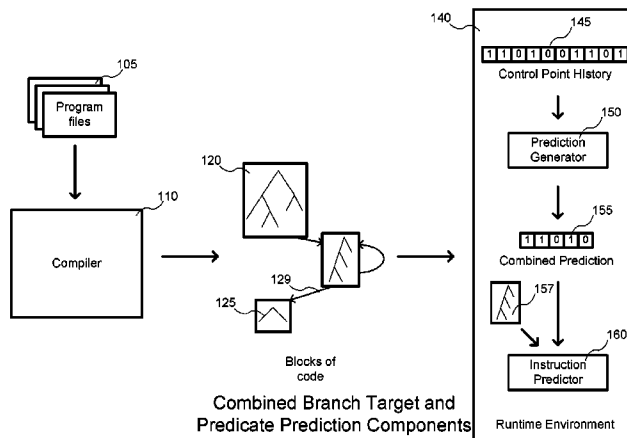
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(57) **ABSTRACT**

Embodiments provide methods, apparatus, systems, and computer readable media associated with predicting predicates and branch targets during execution of programs using combined branch target and predicate predictions. The predictions may be made using one or more prediction control flow graphs which represent predicates in instruction blocks and branches between blocks in a program. The prediction control flow graphs may be structured as trees such that each node in the graphs is associated with a predicate instruction, and each leaf associated with a branch target which jumps to another block. During execution of a block, a prediction generator may take a control point history and generate a prediction. Following the path suggested by the prediction through the tree, both predicate values and branch targets may be predicted. Other embodiments may be described and claimed.

24 Claims, 10 Drawing Sheets



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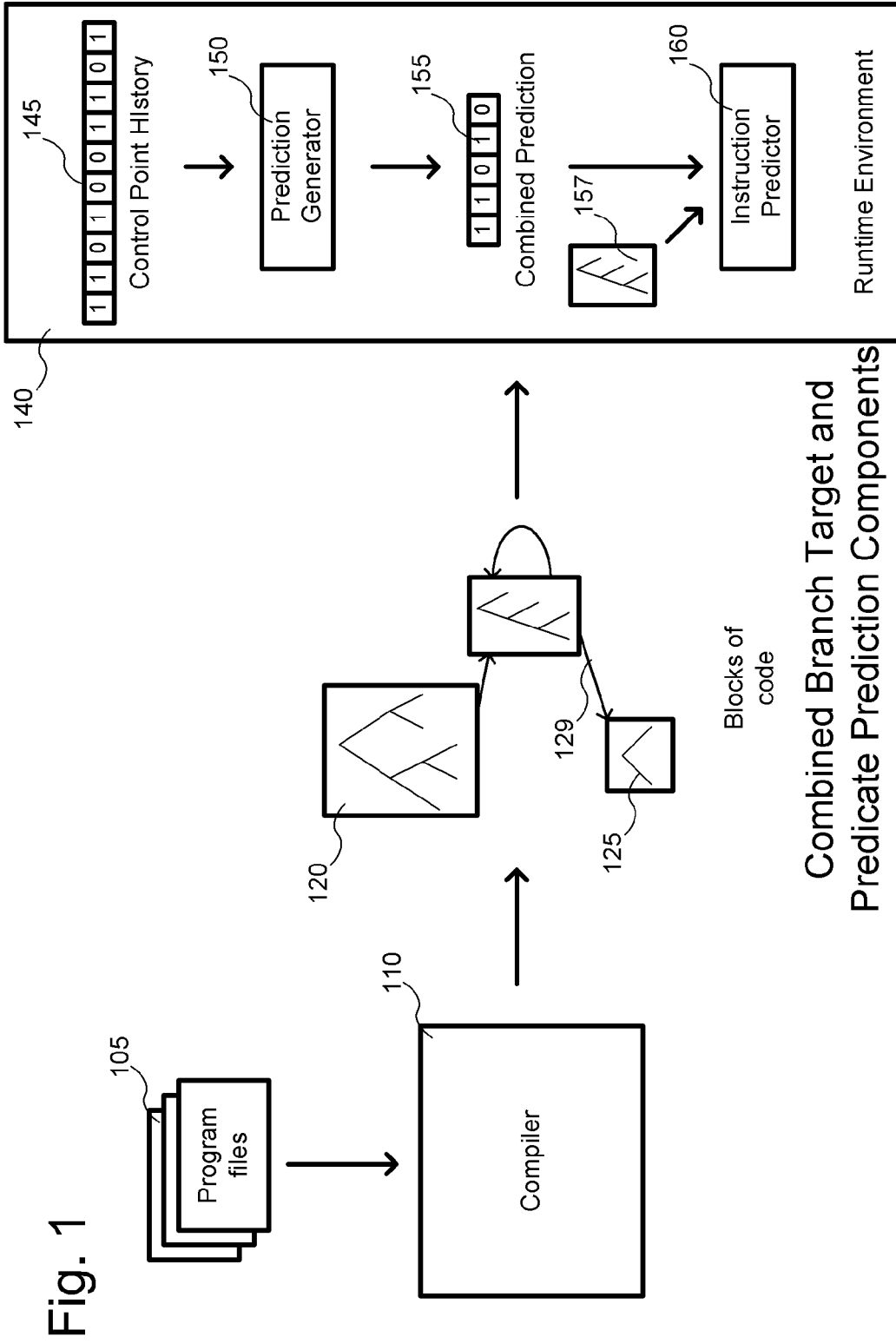
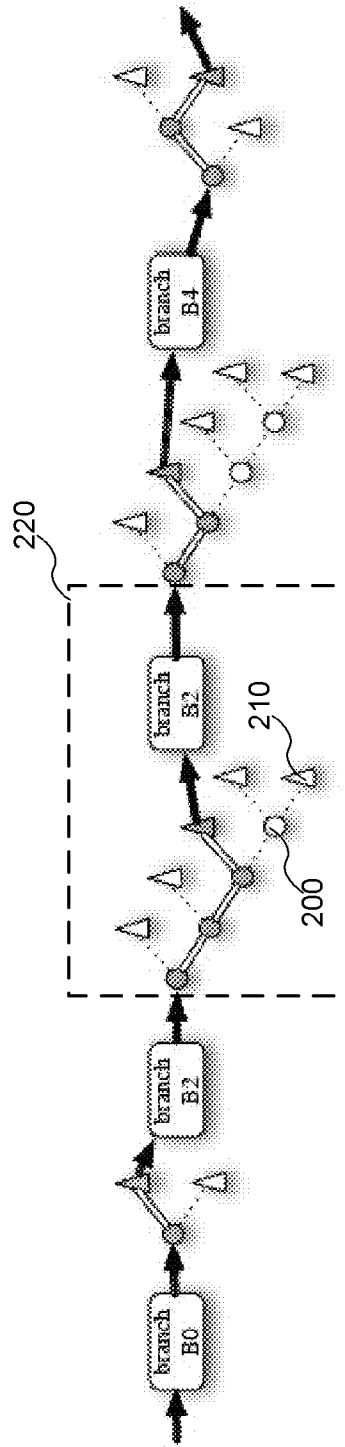
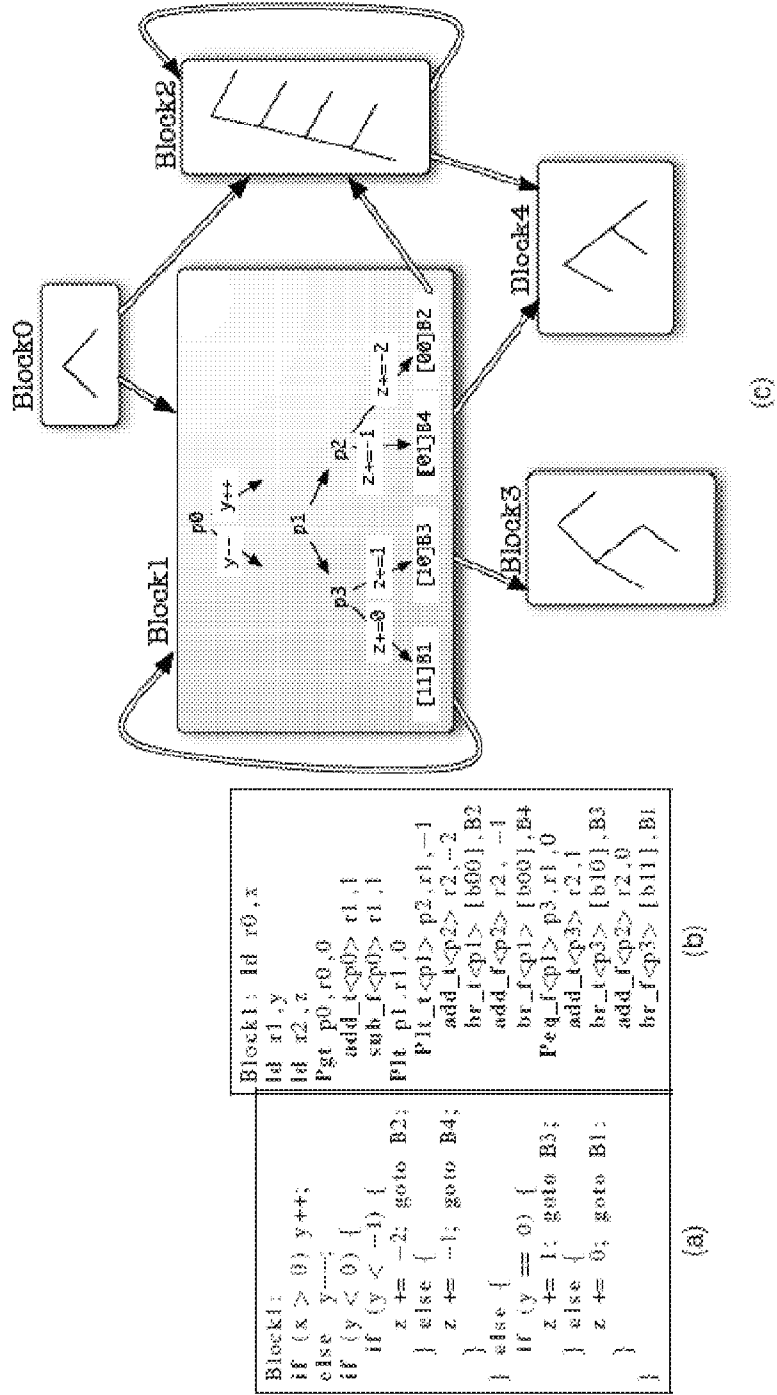


Fig. 2



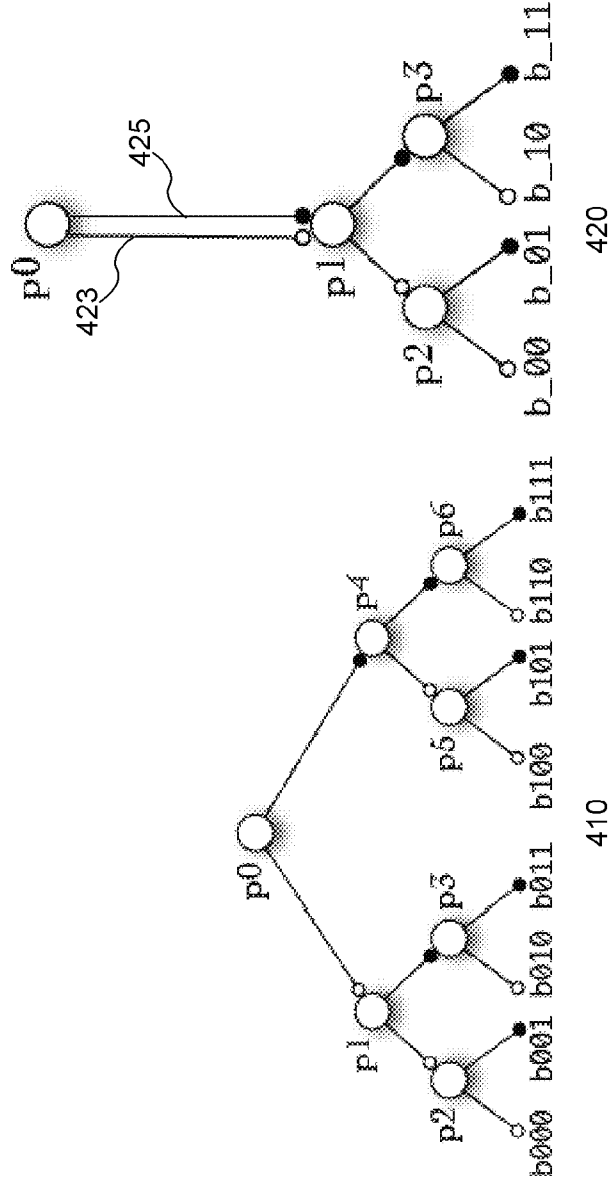
Prediction of Predicate Values
and Branch Targets

Fig. 3



Generation of Blocks of Instructions

Fig. 4



Prediction Control-flow Graphs

Fig. 5

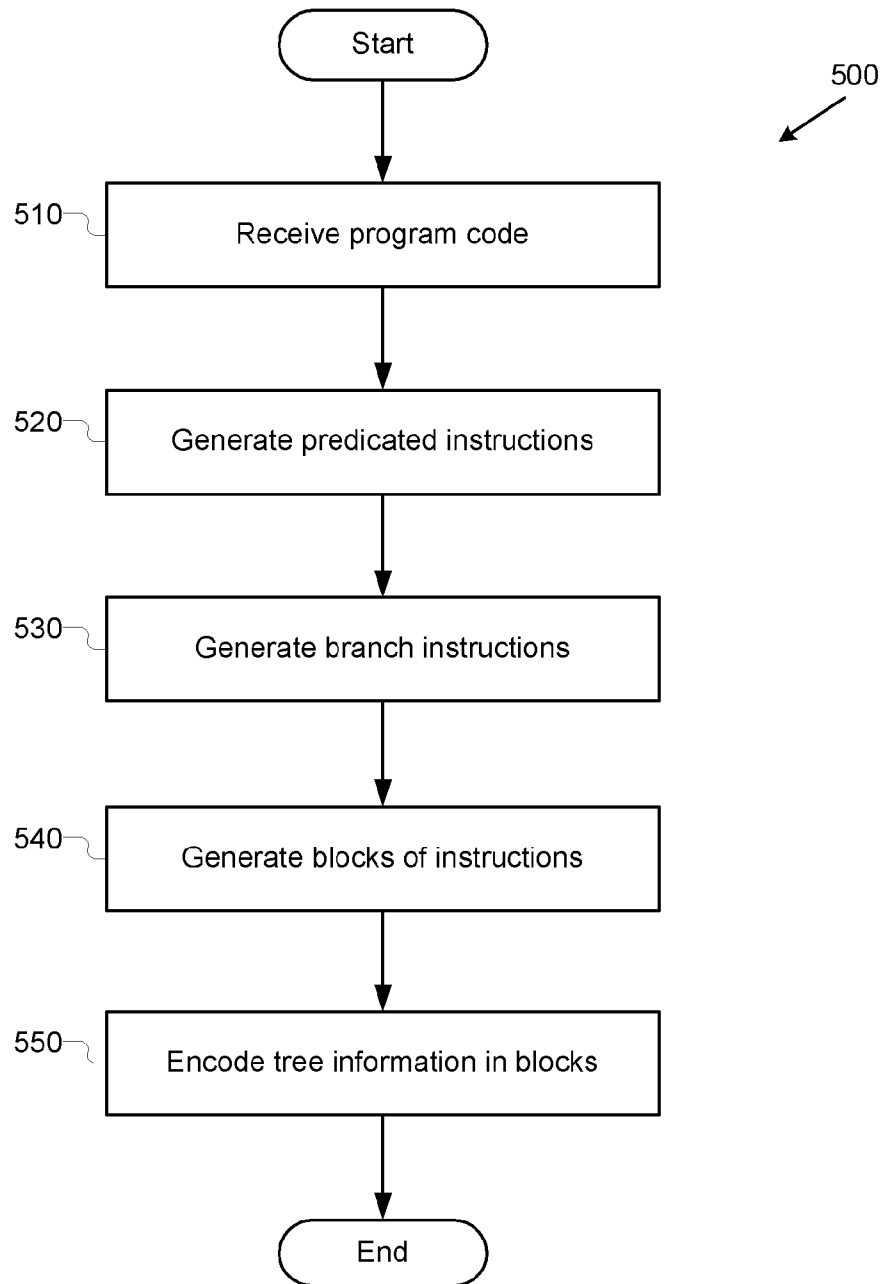
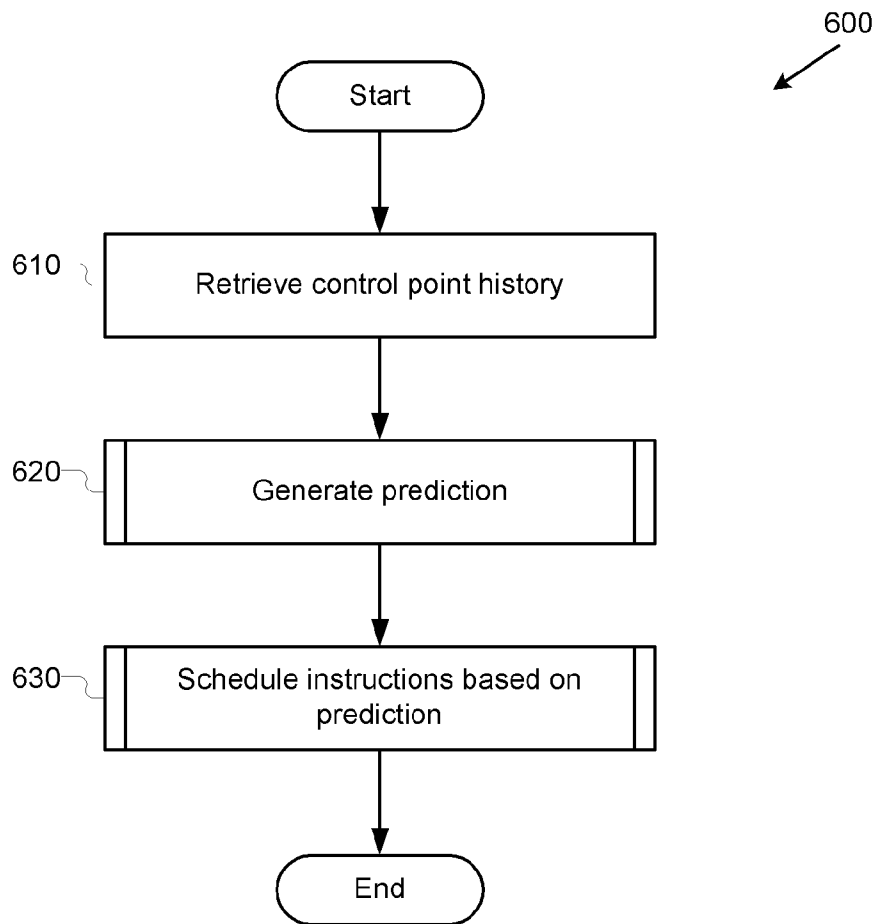
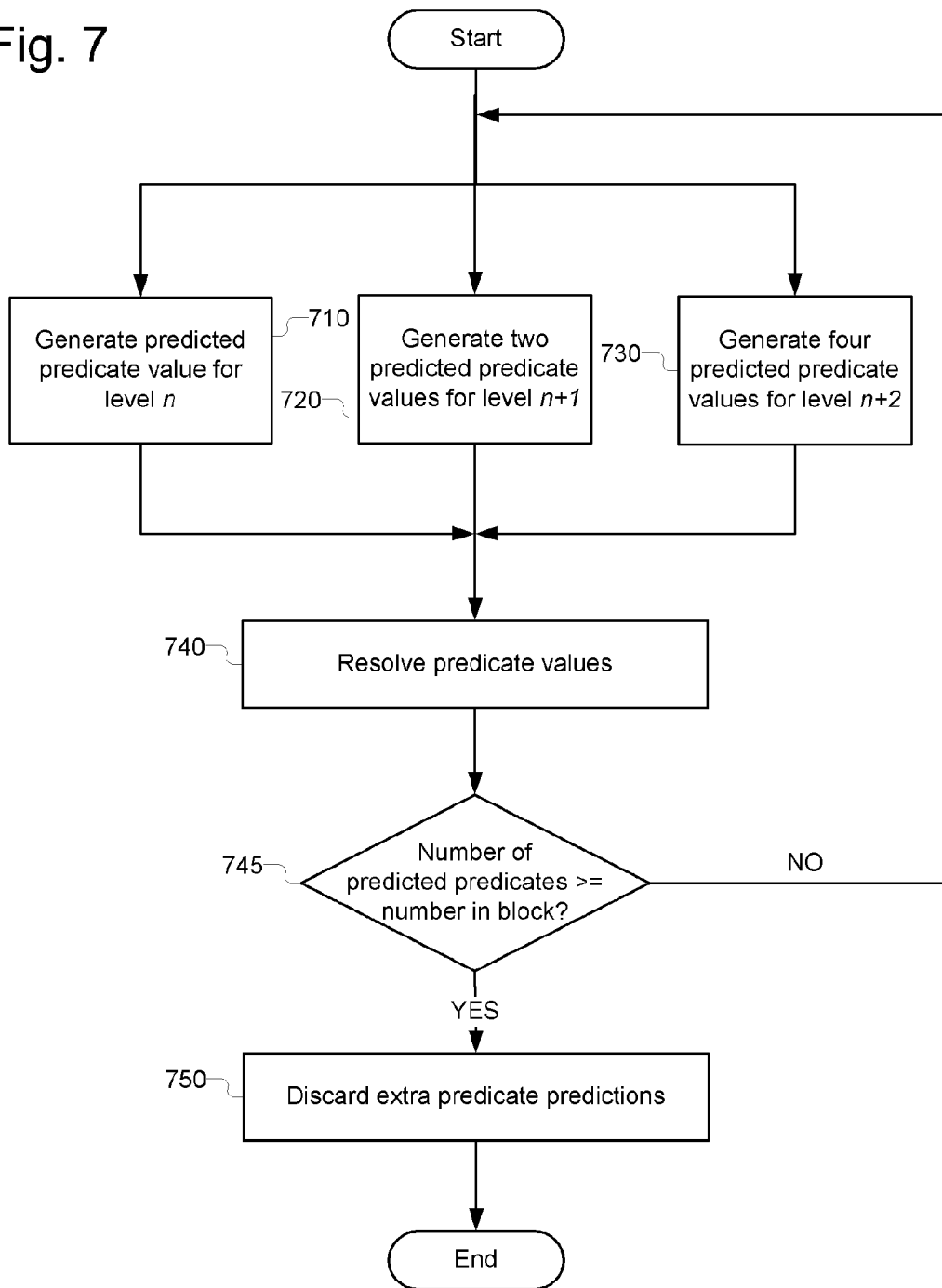


Fig. 6



700

Fig. 7



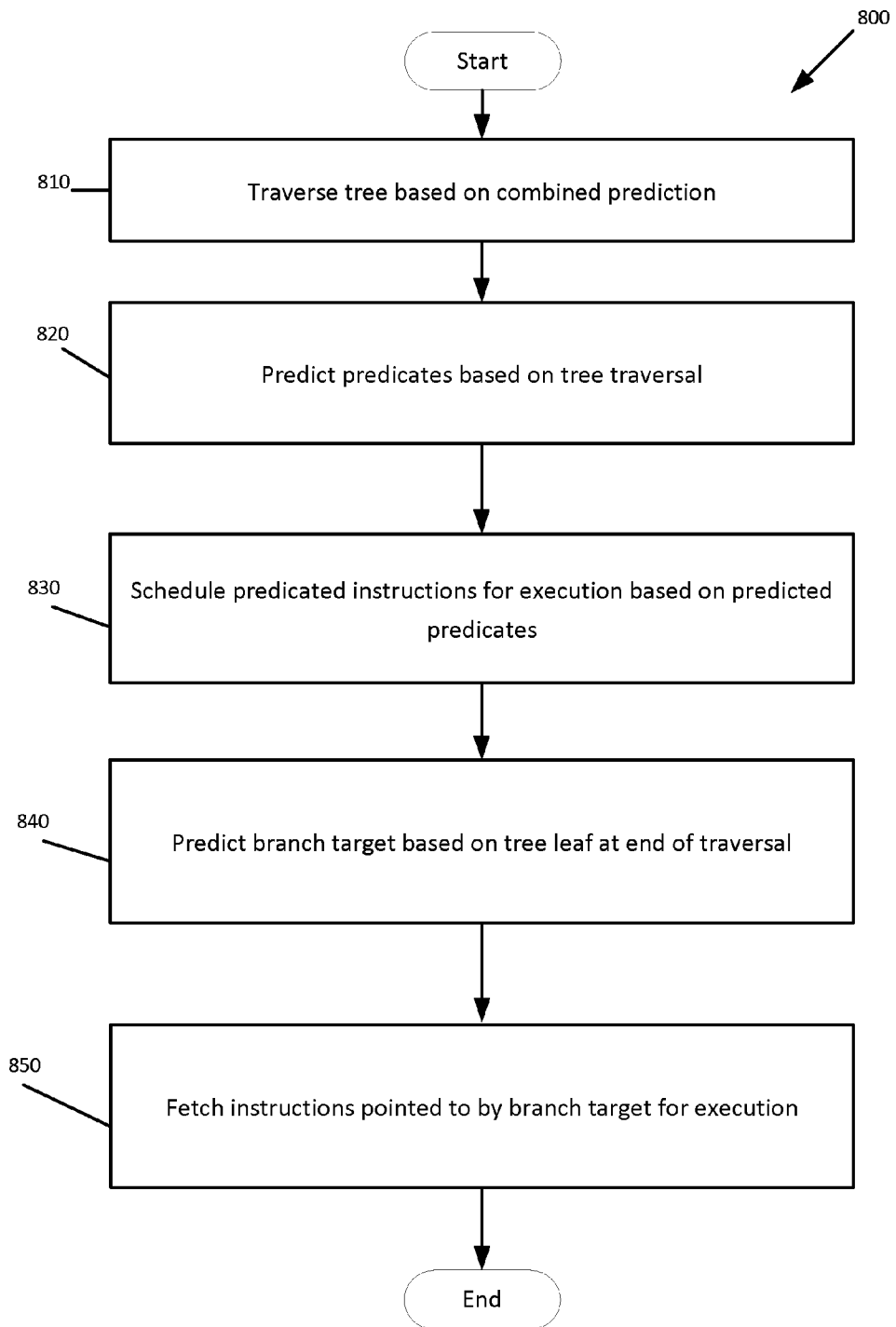
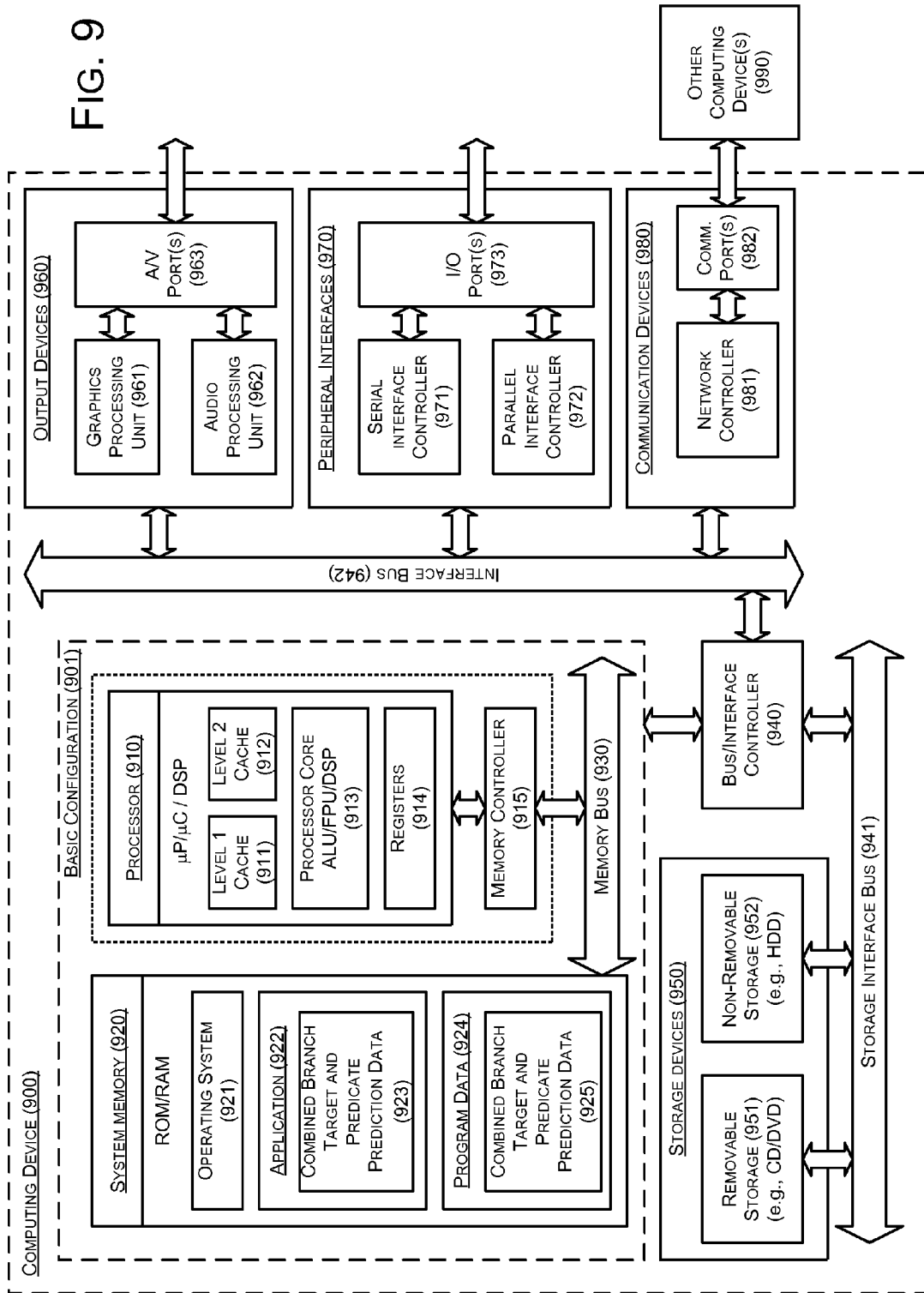


Fig. 8

FIG. 9



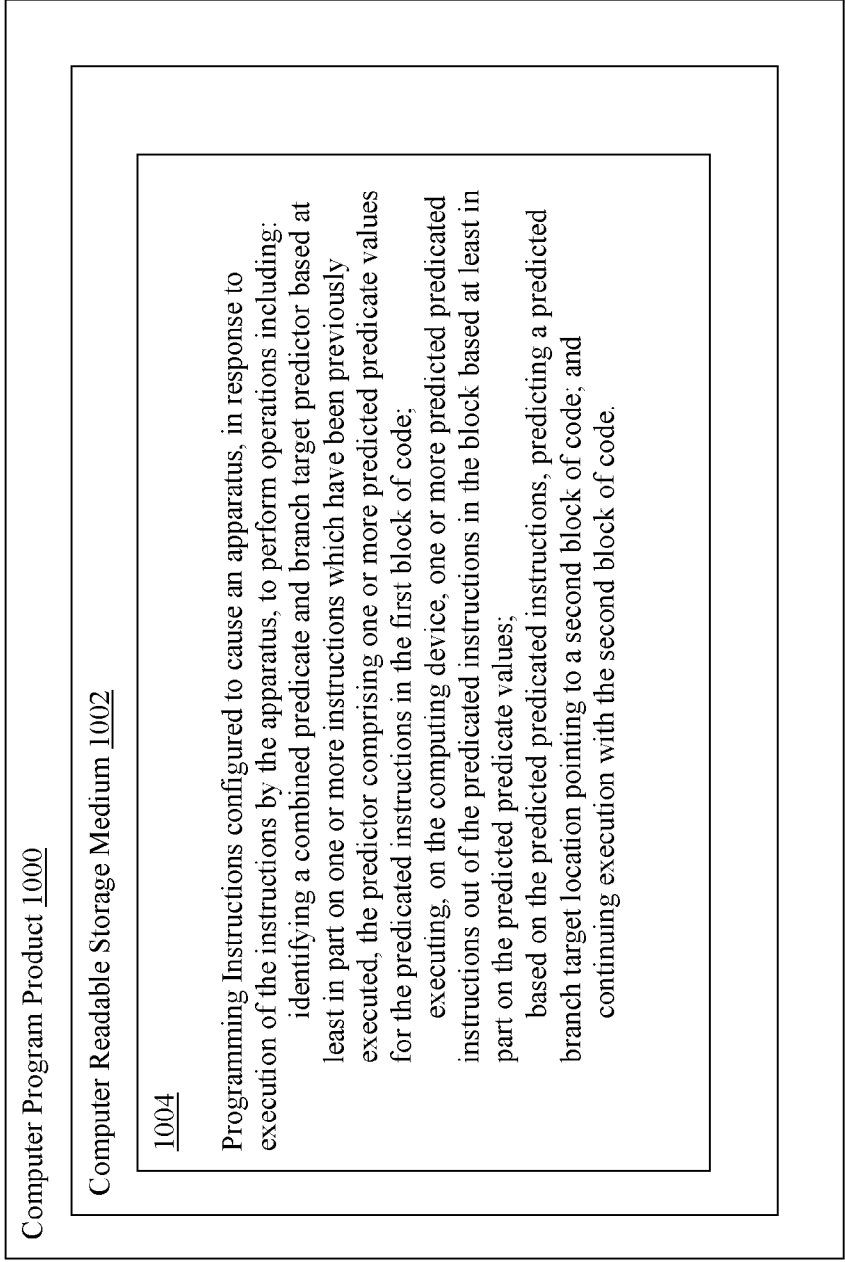


FIG. 10

COMBINED BRANCH TARGET AND PREDICATE PREDICTION FOR INSTRUCTION BLOCKS

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a national stage filing under 35 U.S.C. §371 of PCT Application No. PCT/US2010/39162, filed on Jun. 18, 2010.

BACKGROUND

Various techniques are available to improve dynamic prediction of conditional computer instructions during execution. Prediction of conditional instructions is often used to better select future instructions whose execution may be dependent on the outcome of the conditional instructions, or to accelerate execution of those future instructions. Among prediction techniques, branch prediction and predication are sometimes used. Branch prediction is often used when conditional instructions in a program are compiled to lead to two possible branching locations (or “targets”). Branch target prediction, used in branch predictors, may also be used to identify a nonconditional jump target. In this technique, a history of branch choices taken before execution of the current conditional instruction may be examined to predict that one branch or the other should be scheduled for execution.

In predication, sets of instructions associated with a conditional instruction are compiled to be associated with a predicate value, such as a Boolean value, and this predicate is typically evaluated separately. In this technique, two sets of instructions (based on the value of the conditional) are separately evaluated and results from those instructions whose associated predicate value was not the result after evaluation may be thrown away or discarded. Predicate values may themselves be predicted, such as by operating a prediction technique using a history of predicate values as input.

Current systems which use these techniques, and in particular systems which organize instructions into instruction blocks, suffer from difficulties, however. The use of branch prediction alone, both when predicting either results of branches or jump targets, fails to provide a facility for contemporaneous prediction of control instructions within blocks of instructions, which often takes the form of predication. Predication, conversely, is not suited to jumps across block boundaries. Existing predication techniques, which may serialize predicate predications, suffer from additional overhead as instructions with later predicates are forced to wait for earlier-occurring predicates. In systems which attempt to combine the techniques, the use of branch prediction and predicate prediction requires multiple data structures and introduces substantial execution overhead. Furthermore, in current systems, branches are predicted between blocks without knowledge of intervening predicates; these branches, which are predicted with a more sparse instruction history, can suffer from poor prediction accuracy.

SUMMARY

In one embodiment, a computer-implemented method for execution-time prediction of computer instructions may include generating, on a computing device, a combined predicate and branch target prediction based at least in part on a control point history; executing, on the computing device, one or more predicted predicated instructions based at least in part on the combined predicate and branch target prediction.

The method may further include proceeding with execution on the computing device at a predicted branch target location based at least in part on the combined predicate and branch target prediction.

In another embodiment, a system for predictive runtime execution of computer instructions may include one or more computer processors, and a combined prediction generator which is configured to accept a history of predicates and/or branches as input and to generate a combined predicate and branch target prediction based on the accepted history, in response to operation by the one or more processors. The system may also include an instruction fetch and execution control configured to control the one or more processors, in response to operation by the one or more processors, to execute one or more predicated instructions based on predicted predicate values obtained from the combined predicate and branch target prediction, and to proceed with execution of fetched instructions at a predicted branch target location. The predicted branch target location may be based at least in part on the predicted predicate values.

In another embodiment, an article of manufacture may include a tangible computer-readable medium and a plurality of computer-executable instructions which are stored on the tangible computer-readable medium. The computer-executable instructions, in response to execution by an apparatus, may cause the apparatus to perform operations for scheduling instructions to execute for a first block of code having predicated instructions and one or more branch targets. The operations may include identifying a combined predicate and branch target prediction based at least in part on one or more instructions which have been previously executed. The prediction may include one or more predicted predicate values for the predicated instructions in the first block of code. The operations may also include executing, on the computing device, one or more predicted predicated instructions out of the predicated instructions in the block based at least in part on the predicted predicate values. The operations may also include predicting a predicted branch target location pointing to a second block of code, based on the predicted predicated instructions, and continuing execution with the second block of code.

The foregoing summary is illustrative only and is not intended to be in any way limiting. In addition to the illustrative aspects, embodiments, and features described above, further aspects, embodiments, and features will become apparent by reference to the drawings and the following detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a block diagram of selected components of a combined branch target and predicate prediction system,

FIG. 2 illustrates a block diagram of instruction prediction based on combined branch target and predicate prediction,

FIG. 3 illustrates a block diagram of successive levels of generation of blocks of instructions from program code,

FIG. 4 illustrates a block diagram of prediction control flow graphs for code blocks,

FIG. 5 illustrates a process for generating programs which utilize the combined branch target and predicate prediction,

FIG. 6 illustrates a process for predicting branch targets and predicates using combined branch target and predicate prediction,

FIG. 7 illustrates a process for generating a combined branch target and predicate prediction,

FIG. 8 illustrates a process for scheduling instructions based on combined branch target and predicate prediction,

FIG. 9 illustrates an example computing device configured to practice various aspects of the earlier described methods,

FIG. 10 illustrates an example article of manufacture having instructions configured to enable an apparatus to practice various aspects of the earlier described methods, all ranged in accordance with various embodiments of the present disclosure.

DETAILED DESCRIPTION

In the following detailed description, reference is made to the accompanying drawings, which form a part hereof. In the drawings, similar symbols typically identify similar components, unless context dictates otherwise. The illustrative embodiments described in the detailed description, drawings, and claims are not meant to be limiting. Other embodiments may be utilized, and other changes may be made, without departing from the spirit or scope of the subject matter presented herein. It will be readily understood that the aspects of the present disclosure, as generally described herein, and illustrated in the Figures, can be arranged, substituted, combined, separated, and designed in a wide variety of different configurations, all of which are explicitly contemplated herein.

The disclosure is drawn, inter alia, to methods, apparatus, systems, and computer readable media related to prediction of predicates and branch targets using combined branch target and predicate prediction.

Described embodiments include techniques, methods, apparatus, and articles of manufacture which may be associated with using a combined structure for both branch target and predicate predictions to expedite execution of a program by a computing device. In various embodiments, these predictions may be made in block-atomic architectures, or in other architectures which divide programs into predicated basic blocks of instructions. In other embodiments, the techniques described herein may be utilized in other architectures that mix branches and predicates. In various embodiments, the predictions may be made using one or more control flow graphs which represent predicates in instruction blocks and branches between blocks. During compilation, the program may be divided into blocks and the one or more prediction control flow graphs created to be associated with each block. The prediction control flow graphs may be structured as trees such that each node in the graphs is associated with a predicate, each edge with a predicated instruction, and each leaf associated with a control instruction which jumps to another block. Then, during execution of a block, a prediction generator may take a control point history, such as a history of the last *n* predicates, and generate a prediction. The prediction may, in various embodiments, be generated as a set of predicate values for various levels of the control flow graph—as such, the prediction may include predictions for the block's predicate instructions.

An instruction fetch and execution control, by using these predicted predicate values, may predict and schedule predicated instructions for execution according to a traversal of the tree to determine to which predicates the predictions apply. Described embodiments may also utilize the control flow graph such that traversal of the graph along the predicted predicate values leads to a leaf, and therefore a branch target. In various embodiments, branch targets may refer to conditional and/or unconditional branches which generate target instruction addresses. By performing this traversal, the instruction fetch and execution control may predict the branch target, and therefore the next code block to be executed. As such, embodiments described herein may com-

bine prediction of predicates and branch targets through the use of a generation of a single, merged prediction. This may provide lower power and/or higher prediction accuracy compared with prior art systems and techniques.

In various embodiments, prediction generation may be made more efficient through use of parallel prediction generation techniques. The parallel prediction generation may be performed by generating a predicate value for a first predicate level based on a control point history, while also contemporaneously generating possible values for lower levels. After a suitable number of levels have been operated on, values from higher levels may be used to narrow down the possible values for lower-levels.

As an example, assume the prediction generator has a 10 predicate control point history length and is tasked with predicting three levels of predicates for a block. The prediction generator, in various embodiments, may do a lookup using a 10-bit history for the first prediction. Simultaneously, the prediction generator may perform two lookups using the most recent 9 bit history, along with the two possibilities for the result of the first lookup, to get a second level predicate value. Similarly, the prediction generator may perform four lookups for the third value. After this contemporaneous generation, the prediction generator may then select particular lower-level results based on the higher-level results and discard the rest. While this technique may require more lookups of prediction values than a sequentialized generation system, in scenarios where generation of individual predicate values has a long latency, this parallelized technique may provide for speed increases.

FIG. 1 illustrates a block diagram of selected components of a combined branch target and predicate prediction system in accordance with various embodiments. In the illustration of FIG. 1, a compiler 110 may receive one or more program files 105 for compilation into one or more executable programs. In various embodiments, the compiler 110 may operate to produce one or more blocks of executable code (hereinafter, also referred to simply as “code”), such as a block 120, which may have associated with them control flow graphs that represent predicated instructions, such as a prediction control flow graph 125, as well as branches which connect the graphs, such as a branch 129. In various embodiments, these blocks may be atomic blocks.

These blocks of code may then be executed in a runtime environment 140, which may be configured to perform predictions of predicate values and branch targets using the combined branch target and predicate predictions, to be described in more detail below. As illustrated, a prediction generator 150, to be executed as part of the runtime environment 140 may be configured to operate on control point histories, such as a control point history 145, to generate the combined branch target and predicate predictions, such as a combined prediction 155. In various embodiments, these instruction histories may include combinations of past predicate values, past branch target values, or both. In various embodiments, the prediction generator 150 may be implemented, in whole or in part, as a lookup table, which looks up one or more prediction values based on a control point history. Additionally, the prediction generator 150 may perform one or more parallelized lookups (or other predicate value generation techniques) in order to improve performance of prediction generation.

The generated combined prediction 155 may then be used by an instruction fetch and execution control 160, along with information about a block of instructions 157, to mark predicated instructions for execution as well as to predict branch targets to schedule execution of branched blocks of code. In

various embodiments, the instruction fetch and execution control **160** may comprise an instruction scheduler for scheduling predicated instructions based on the combined prediction **155**. In various embodiments, the instruction fetch and execution control **160** may comprise fetch control logic to predict a target based on the combined prediction **155** and to fetch an instruction for execution based on that target. Specific examples of this prediction generation and instruction prediction will be further described below. In various embodiments, the runtime environment **140** may be provided by a runtime manager or other appropriate software, which itself may be generated by the compiler **110**.

FIG. **2** illustrates a block diagram of instruction prediction based on combined branch target and predicate predictions in accordance with various embodiments. As shown, for the illustrated embodiments, execution of a program may take the form of execution of one or more predicated instructions such as a predicated instruction **200**, which leads to branch targets such as a branch target **210**. These branch targets then indicate a next block of instructions that should be executed, along with the associated predicated instructions. In various embodiments, the combined branch target and predicate predictions utilized herein are, for a block of instructions, able to predict values for an entire block's worth of predicate values as well as a branch target out of the block. This set of predictions is illustrated by the example instructions and targets within the area bounded by the dotted line **220**. The example instructions and targets include three predicted predicate values (the three shaded circles), followed by a branch target (the shaded triangle). Particular techniques for performing these predictions are described below.

FIG. **3** illustrates a block diagram of successive levels of generation of blocks of instructions from program code in accordance with various embodiments. Portion (a) of FIG. **3** illustrates an example C-style code snippet. The snippet contains conditionals, such as "if (x>0)" that leads to two possibilities, instructions: 1) "y++" and 2) "y--". The code also contains explicit branching instructions, such as "goto B2." These branching instructions indicate that a branch should be taken, if that branching instruction is executed.

Portion (b) of FIG. **3**, illustrates intermediate representation of the code after compilation. In particular, portion 3(b) illustrates how the conditional statements in the block have been represented as predicated instructions. Thus, in the illustrated example, the result of the "if (x>0)" conditional discussed above has been represented as a predicate **p0** at the line "Pgt **p0**, **r0**, **0**" In this line, the value in register **r0** is compared to see if the value is greater than 0, and the true-or-false result of that comparison is held as the value of predicate **p0**.

Next, are two possible instructions that depend on this predicate. The first is the "add_t<**p0**>**r1**, **1**" instruction, which is an add operation that is predicated on the value of **p0** and is executed if **p0** is "true." Similarly, "sub_f<**p0**>**r1**, **1**" subtracts 1 from the **r1** register if the **p0** predicate takes a value of false. In other words, the techniques and systems described herein provide predicted values for predicates like **p0**, which allow one of the predicated instructions to be scheduled before the actual value of the predicate is known, thereby potentially speeding up execution of the block.

Portion (c) of FIG. **3** illustrates an example set of blocks of instructions which may be generated by a compiler, such as the compiler **110**, from the intermediate representation of portion (b). As illustrated, in particular by Block**1**, each block may contain a branched set of predicated instructions that leads to the branches; which, in turn, instruct the execution to jump to another block. Thus, when Block**1** is executed, one more predicated instructions are performed, and then a

branch to another block is taken. If branch **B3** is taken, execution jumps to Block**3**. In various embodiments, branches may cause a block to be executed again, e.g., branch **B1**, which begins execution of Block**1** anew. As described herein, in various embodiments, the blocks of instructions have associated with them prediction control flow graphs. The prediction control flow graphs allow an instruction fetch and execution control to predict not only which predicated instructions should be predicted and scheduled for execution within a block, but also which branches are likely to be taken and therefore with which blocks execution should proceed upon exit of a currently-executing block.

FIG. **4** illustrates a block diagram of prediction control flow graphs for code blocks in accordance with various embodiments. As discussed, in various embodiments, the compiler may be configured to generate, for a block, a prediction control flow graph which indicates predicated instructions as well as branch targets for the particular block of instructions. As illustrated, the prediction control flow graph may be implemented as a tree which represents predicates by nodes, such as nodes **p0**, **p1**, and **p5** of graph **410**, and which represents branch targets as leaves, such as branch targets **b100**, **b101**, and **b110**. Additionally, the edges in the tree may represent predicted instructions—thus, if the value of predicate **p0** is "True" the instruction represented by the edge from **p0**→**p4** may be executed. As discussed herein, techniques described herein utilize these prediction control-flow graphs to predict both predicate values and branch targets by generating a combined branch target and predicate prediction which identifies a set of prediction values. By following the values through the graph, the runtime environment **140**, and in particular the instruction fetch and execution control **160**, can identify a) which predicated instructions are likely to be needed for execution, and b) what their values are. Additionally, by following the path, the instruction fetch and execution control **160** can identify a branch target for scheduling of a next block of instructions. A given control flow graph may contain paths of different lengths depending on the internal structure of a block. Thus, in various embodiments, the instruction fetch and execution control **160** may follow the path to its end at a leaf node, while in some embodiments, the instruction fetch and execution control **160** may predict a branch target based on a non-terminated following of the path, or a following of the path past its actual end.

In various embodiments, the prediction control flow graph may contain different paths for every predicate value, such as in graph **410**, which branches at every predicate. In some scenarios, however, a block may not branch on a particular predicate, such as in graph **420**, where, regardless of the value of **p0**, control for the block represented by the graph will next depend on the value of **p1**. This does not, however, mean that the same instruction will be executed in the block, as there are different edges **423** and **425** in the tree. Each of the different edges **423** and **425** may represent a different predicated instruction. Additionally, while the value of **p0** may not be completely determinative of future instructions, in various embodiments, the value may still correlate with particular future predicate or branch target values. Thus, the value of **p0** may still be maintained in a control point history for prediction generation. An example of this can be seen in the code discussed above with respect to FIG. **3**, where execution in Block**1** proceeded to predicate **p1** regardless of which value predicate **p0** took. Also, in various embodiments the prediction control flow graphs may have associated with them information about the shape of the graph, such as the number of levels in the graph or a degree of branching. This shape

information may be useful in performing prediction generation, and in particular parallelized prediction generation.

FIG. 5 illustrates a process 500 for generating programs which utilize the combined branch target and predicate prediction in accordance with various embodiments. As illustrated, process 500 may start at operation(s) 510 (“Receive program code”). At operation(s) 510, program code to compile may be received, such as by the compiler 110. As discussed above, in various embodiments, the program code may include one or more code files, and may be implemented in a variety of known computing languages. Additionally, in various embodiments, the program code may have one or more instructions or information that aid the compiler in generating code which utilizes the prediction techniques described herein. While, for the sake of ease of description, the activities of process 500 are described with reference to a single compiler, such as compiler 110, in alternative embodiments, one or more compilers or other code analysis modules may be utilized to perform these activities.

From operation(s) 510, process 500 may proceed to operation(s) 520 (“Generate predicated instructions”). At operation(s) 520, the compiler may generate predicated instructions, such as, for example, the instructions discussed above with respect to FIG. 3. As discussed above, these predicated instructions may be generated at least in part through the compiler 110 identifying conditional statements and generating predicates based on these statements. From operation(s) 520, process 500 may proceed to operation(s) 530 (“Generate branch instructions”). At operation(s) 530, the compiler 110 may generate branch instructions, for example, the instructions discussed above with respect to FIG. 3. From operation(s) 530, process 500 may proceed to operation(s) 540 (“Generate block instructions”). At operation(s) 540, the compiler 110 may generate blocks of instructions for purposes of prediction. In various embodiments, the compiler may generate branch instructions and/or generate blocks on the basis of explicit jump calls, like those illustrated above. In other embodiments, the compiler may identify blocks present in the original program code and generate branches between these identified blocks even where no jump was originally coded. The blocks may be explicitly identified, such as in the example shown in FIG. 3, or may be recognized by the compiler as set of instructions which are likely to be executed as a unit.

From operation(s) 540, process 500 may proceed to operation(s) 550 (“Encode tree information in blocks”). At operation(s) 550, the compiler may encode tree information (or approximate tree information) for the prediction control flow graphs in the respective headers of the block of instructions associated with those prediction control flow graphs. For example, as mentioned above, the tree may represent the number of predicates on various paths between the root and various unconditional jumps as leaves. In such a tree, predicates would be used in the block as nodes, predicate results/values as edges, and branch targets as leaves. In other embodiments, the compiler may encode information related to tree depth or the shape of a tree, so that, during prediction generation, the prediction generator 150 may more easily generate a proper-length prediction.

FIG. 6 illustrates a process 600 for predicting branch targets and predicates using combined branch target and predicate predictions in accordance with various embodiments. For the illustrated embodiments, the process 600 may be performed on a per-block basis, even though the illustrated example shows predictions for only a single block. In alternate embodiments, prediction may be performed on multiple blocks as needed during execution.

Accordingly, for the embodiments, process 600 may start with operation(s) 610 (“Retrieve control point history”). At operation(s) 610, the runtime environment 140, in particular, the prediction generator 150, may retrieve a control point history. In various embodiments, the control point history may include a history of predicate values which have been evaluated in the past; the history may take the form of a binary string and/or have a pre-defined length. An example may be the control point history 145 illustrated in FIG. 1. In various embodiments, the control point history may also include one or more records of branch targets taken.

From operation(s) 610, the process 600 may proceed to operation(s) 620 (“Generate prediction”). At operation(s) 620, the prediction generator 150 may use the control point history 145 to generate a prediction, such as the combined prediction 155, for use in scheduling instructions. Particular embodiments of this activity are described below with reference to FIG. 7. From operation(s) 620, process 600 may proceed to operation(s) 630. At operation(s) 630, the instruction fetch and execution control 160, using the combined prediction 155 and the block information 157, may schedule instructions for execution. Particular embodiments of this activity are described below with reference to FIG. 8.

FIG. 7 illustrates a process 700 for generating a combined branch target and predicate prediction in accordance with various embodiments. Similar to the discussion above with respect to FIG. 6, process 700 may be performed on a per-block basis; the illustrated example thus shows predictions for a single block. The illustrated example shows a parallelized technique for efficiently generating combined predictions. In various embodiments, not illustrated, however the prediction generator 150 may generate a prediction one value at a time by inputting the control point history, such as into a lookup table, receiving a predicate value. The prediction generator 150 may then proceed with a second lookup using all but the oldest value in the control point history, along with the freshly-generated predicate value to look up the next predicate value, and so on. The lookup may continue until enough values have been found that a combined branch target and predicate prediction for the block is generated.

As illustrated, process 700 may start at operation(s) 710 (“Generate predicted predicated value for level n”). At operation(s) 710, the prediction generator 150 may generate a predicted predicate value for a level n. As discussed above, this may be performed using various generation methods, including a lookup table. From operation(s) 710, process 700 may proceed to operation(s) 720 (“Generate two predicted predicated values for level n+1”). At operation(s) 720, the prediction generator 150 may generate two predicted predicate values for level n+1, using both possible predicate values for level n in the control point history. As illustrated, the action of this block may be performed in parallel with the action of operation(s) 710, as it does not immediately rely on the result of operation(s) 710. From operation(s) 720, process 700 may proceed to operation(s) 730 (“Generate four predicted predicated values for level n+2”). At operation(s) 720, a similar action may be performed, where the prediction generator generates four predicted predicate values for level n+2. The four predicted predicate values for level n+2 may be generated using all of the possible values for the results of operation(s) 710 and 720.

Following is an example for generating a combined branch target and predicate prediction in accordance with the described embodiments. If the prediction generator is operating on instruction histories of length 5, with a current control point history of 11011, at the operation(s) 710, the prediction generator 150 may look up a predicted value for level

n using the history **11011**. Simultaneously (or at least contemporaneously) with that operation, the prediction generator **150** may also perform look ups for level n+1 using instruction histories **10110** and **10111**. The instruction histories may represent the four most-recent history values in the history. Additionally, the instruction histories may be associated with two possible outcomes from the generation operation(s) at operation(s) **710**. Similarly, at operation(s) **730**, lookups may be performed using histories **01100**, **01101**, **01110**, and **01111**.

From operation(s) **710**, **720** or **730**, process **700** may proceed to operation(s) **740** (“Resolve predicate values”). At operation(s) **740**, after the results of operation(s) **710**, **720**, and **730** are known, the predicate values may be resolved. Thus, if the value from operation(s) **710** was determined to be 0, then the result from operation(s) **720** which used **10110** as input may be maintained. Other result from operation(s) **720** may be discarded. Similarly, one result may be taken from operation(s) **730**. It should be recognized that, while the illustrated example utilizes three levels of parallel predicate prediction, in alternative embodiments, different numbers of levels may be used.

From operation(s) **740**, process **700** may proceed to operation(s) **745** (“Number of predicted predicates greater than or equal to the number of blocks”). At operation(s) **745**, the prediction generator **150** may determine if a prediction has been made for at least every predicate in the current block of instructions. If not, process **700** may return to operations **710**, **720**, and **730**, and proceeds with $n=n+3$. If predictions have been made for every predicate in the block, then at operation(s) **750** (“Discard extra predicate predictions”). At operation(s) **750**, the extra predictions may be discarded. For example, using the three-level parallelized prediction discussed above, if there are five levels of predicates in the block, the process may perform two iterations of the loop, and generate six predicted predicate values. The sixth value may then be discarded. Additionally, in some embodiments, if blocks contain unbalanced trees (or other complex tree shapes) in their prediction control flow graph, the prediction generator **150** may be configured to generate enough predicted predicate values to fill the longest path in a given tree. As a result, the prediction generator **150** may avoid or reduce spending computational resources looking at potentially-complex tree descriptors. This may also result in the discarding of predicate predictions at operation(s) **750**.

FIG. 8 illustrates a process **800** for scheduling instructions based on combined branch target and predicate predictions in accordance with various embodiments. For the embodiments, process **800** may start at operation(s) **810** (“Traverse tree based on combined prediction”). At operation(s) **810**, the instruction fetch and execution control **160** may traverse the tree of the prediction control flow graph based on the combined prediction **155**. From operation(s) **810**, process **800** may proceed to operation(s) **820** (“Predict predicates based on tree traversal”). At operation(s) **820**, the instruction fetch and execution control may predict which predicates will be evaluated based on the path through the tree. From operation(s) **820**, process **800** may proceed to operation(s) **830** (“Schedule predicated instructions for execution based on predicted predicates”). From operation(s) **830**, the instruction fetch and execution control **160** may schedule predicated instructions based on these predictions for execution. From operation(s) **830**, process **800** may proceed to operation(s) **840** (“Predict branch target based on tree leaf at end of traversal”). From operation(s) **840**, the instruction fetch and execution control may predict a branch target based on the tree traversal. In various embodiments, the instruction fetch

and execution control may predict the branch target based on a tree leaf located at the end of the tree traversal, if the traversal leads to a leaf node; in other embodiments, the prediction may be based on a non-terminating traversal. From operation(s) **840**, process **800** may proceed to operation(s) **850** (“Schedule code block pointed to by branch target for execution”). From operation(s) **850**, the instruction fetch and execution control **160** may fetch one or more instructions pointed to by this branch target for next execution after the current code block. As discussed above, under process **800**, a single combined prediction, such as combined prediction **155**, may provide sufficient information to schedule both predicated instructions and branch targets for a block of instructions. The fetched instructions may be subsequently executed.

FIG. 9 is a block diagram illustrating an example computing device configured in accordance with the present disclosure. In a basic configuration **901**, computing device **900** typically includes one or more processors **910** and system memory **920**. A memory bus **930** may be used for communicating between the processor **910** and the system memory **920**.

Depending on the desired configuration, processor **910** may be of any type including but not limited to a microprocessor (μ P), a microcontroller (μ C), a digital signal processor (DSP), or any combination thereof. Processor **910** may include one or more levels of caching, such as a level one cache **911** and a level two cache **912**, a processor core **913**, and registers **914**. An example processor core **913** may include an arithmetic logic unit (ALU), a floating point unit (FPU), a digital signal processing core (DSP Core), or any combination thereof. An example memory controller **915** may also be used with the processor **910**, or in some implementations the memory controller **915** may be an internal part of the processor **910**.

Depending on the desired configuration, the system memory **920** may be of any type including but not limited to volatile memory (such as RAM), non-volatile memory (such as ROM, flash memory, etc.) or any combination thereof. System memory **920** may include an operating system **921**, one or more applications **922**, and program data **924**. Application **922** may include programming instructions providing logic **923** to implement the above-described combined branch target and predicate prediction generation and instruction prediction. Program Data **924** may include data **925** such as combined branch target and predicate predictions, control point history, and code block information.

Computing device **900** may have additional features or functionality, and additional interfaces to facilitate communications between the basic configuration **901** and any required devices and interfaces. For example, a bus/interface controller **940** may be used to facilitate communications between the basic configuration **901** and one or more data storage devices **950** via a storage interface bus **941**. The data storage devices **950** may be removable storage devices **951**, non-removable storage devices **952**, or a combination thereof. Examples of removable storage and non-removable storage devices include magnetic disk devices such as flexible disk drives and hard-disk drives (HDD), optical disc drives such as compact disc (CD) drives or digital versatile disc (DVD) drives, solid state drives (SSD), and tape drives to name a few. Example computer storage media may include volatile and nonvolatile, removable and non-removable media implemented in any method or technology for storage of information, such as computer readable instructions, data structures, program modules, or other data.

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System memory **920**, removable storage **951** and non-removable storage **952** are all examples of computer storage media. Computer storage media includes, but is not limited to, RAM, ROM, EEPROM, flash memory or other memory technology, CD-ROM, digital versatile disks (DVD) or other optical storage, magnetic cassettes, magnetic tape, magnetic disk storage or other magnetic storage devices, or any other medium which may be used to store the desired information and which may be accessed by computing device **900**. Any such computer storage media may be part of device **900**.

Computing device **900** may also include an interface bus **942** for facilitating communication from various interface devices (e.g., output interfaces, peripheral interfaces, and communication interfaces) to the basic configuration **901** via the bus/interface controller **940**. Example output devices **960** include a graphics processing unit **961** and an audio processing unit **962**, which may be configured to communicate to various external devices such as a display or speakers via one or more A/V ports **963**. Example peripheral interfaces **970** include a serial interface controller **971** or a parallel interface controller **972**, which may be configured to communicate with external devices such as input devices (e.g., keyboard, mouse, pen, voice input device, touch input device, etc.) or other peripheral devices (e.g., printer, scanner, etc.) via one or more I/O ports **973**. An example communication device **980** includes a network controller **981**, which may be arranged to facilitate communications with one or more other computing devices **990** over a network communication link via one or more communication ports **982**.

The network communication link may be one example of a communication media. Communication media may typically be embodied by computer readable instructions, data structures, program modules, or other data in a modulated data signal, such as a carrier wave or other transport mechanism, and may include any information delivery media. A “modulated data signal” may be a signal that has one or more of its characteristics set or changed in such a manner as to encode information in the signal. By way of example, and not limitation, communication media may include wired media such as a wired network or direct-wired connection, and wireless media such as acoustic, radio frequency (RF), microwave, infrared (IR) and other wireless media. The term computer readable media as used herein may include both tangible storage media and communication media.

Computing device **900** may be implemented as a portion of a small-form factor portable (or mobile) electronic device such as a cell phone, a personal data assistant (PDA), a personal media player device, a wireless web-watch device, a personal headset device, an application specific device, or a hybrid device that include any of the above functions. Computing device **900** may also be implemented as a personal computer including both laptop computer and non-laptop computer configurations.

Articles of manufacture and/or systems may be employed to perform one or more methods as disclosed herein. FIG. **10** illustrates a block diagram of an example article of manufacture having a computer program product **1000** for metering usage of components of an integrated circuit, in accordance with various embodiments of the present disclosure. The computer program product **1000** may include non-transitory computer-readable storage medium **1002** and plurality of programming instructions **1004** stored in the computer-readable storage medium **1002**.

In various ones of these embodiments, programming instructions **1004** may be configured to enable an apparatus, in response to execution by the apparatus, to perform operations including:

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identifying a combined predicate and branch target prediction based at least in part on one or more instructions which have been previously executed, the prediction comprising one or more predicted predicate values for the predicated instructions in the first block of code;

executing, on the computing device, one or more predicted predicated instructions out of the predicated instructions in the block based at least in part on the predicted predicate values;

based on the predicted predicated instructions, predicting a predicted branch target location pointing to a second block of code; and

continuing execution with the second block of code.

Computer-readable storage medium **1002** may take a variety of forms including, but not limited to, non-volatile and persistent memory, such as, but not limited to, compact disc read-only memory (CDROM) and flash memory.

The herein described subject matter sometimes illustrates different components or elements contained within, or connected with, different other components or elements. It is to be understood that such depicted architectures are merely examples, and that in fact many other architectures may be implemented which achieve the same functionality. In a conceptual sense, any arrangement of components to achieve the same functionality is effectively “associated” such that the desired functionality is achieved. Hence, any two components herein combined to achieve a particular functionality may be seen as “associated with” each other such that the desired functionality is achieved, irrespective of architectures or intermedial components. Likewise, any two components so associated may also be viewed as being “operably connected”, or “operably coupled”, to each other to achieve the desired functionality, and any two components capable of being so associated may also be viewed as being “operably couplable”, to each other to achieve the desired functionality. Specific examples of operably couplable include but are not limited to physically mateable and/or physically interacting components and/or wirelessly interactable and/or wirelessly interacting components and/or logically interacting and/or logically interactable components.

Various aspects of the subject matter described herein are described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it should be apparent to those skilled in the art that alternate implementations may be practiced with only some of the described aspects. For purposes of explanation, specific numbers, materials, and configurations are set forth in order to provide a thorough understanding of the illustrative examples. However, it should be apparent to one skilled in the art that alternate embodiments may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative embodiments.

With respect to the use of substantially any plural and/or singular terms herein, those having skill in the art may translate from the plural to the singular and/or from the singular to the plural as is appropriate to the context and/or application. The various singular/plural permutations may be expressly set forth herein for sake of clarity.

It will be understood by those within the art that, in general, terms used herein, and especially in the appended claims (e.g., bodies of the appended claims) are generally intended as “open” terms (e.g., the term “including” should be interpreted as “including but not limited to,” the term “having” should be interpreted as “having at least,” the term “includes” should be interpreted as “includes but is not limited to,” etc.).

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It will be further understood by those within the art that if a specific number of an introduced claim recitation is intended, such an intent will be explicitly recited in the claim, and in the absence of such recitation no such intent is present. For example, as an aid to understanding, the following appended claims may contain usage of the introductory phrases “at least one” and “one or more” to introduce claim recitations. However, the use of such phrases should not be construed to imply that the introduction of a claim recitation by the indefinite articles “a” or “an” limits any particular claim containing such introduced claim recitation to inventions containing only one such recitation, even when the same claim includes the introductory phrases “one or more” or “at least one” and indefinite articles such as “a” or “an” (e.g., “a” and/or “an” should typically be interpreted to mean “at least one” or “one or more”); the same holds true for the use of definite articles used to introduce claim recitations. In addition, even if a specific number of an introduced claim recitation is explicitly recited, those skilled in the art will recognize that such recitation should typically be interpreted to mean at least the recited number (e.g., the bare recitation of “two recitations,” without other modifiers, typically means at least two recitations, or two or more recitations). Furthermore, in those instances where a convention analogous to “at least one of A, B, and e, etc.” is used, in general such a construction is intended in the sense one having skill in the art would understand the convention (e.g., “a system having at least one of A, B, and C” would include but not be limited to systems that have A alone, B alone, C alone, A and B together, A and e together, B and e together, and/or A, B, and C together, etc.). In those instances where a convention analogous to “at least one of A, B, or C, etc.” is used, in general such a construction is intended in the sense one having skill in the art would understand the convention (e.g., “a system having at least one of A, B, or C” would include but not be limited to systems that have A alone, B alone, C alone, A and B together, A and C together, B and C together, and/or A, B, and C together, etc.). It will be further understood by those within the art that virtually any disjunctive word and/or phrase presenting two or more alternative terms, whether in the description, claims, or drawings, should be understood to contemplate the possibilities of including one of the terms, either of the terms, or both terms. For example, the phrase “A or B” will be understood to include the possibilities of “A” or “B” or “A and B.”

Various operations may be described as multiple discrete operations in turn, in a manner that may be helpful in understanding embodiments; however, the order of description should not be construed to imply that these operations are order dependent. Also, embodiments may have fewer operations than described. A description of multiple discrete operations should not be construed to imply that all operations are necessary. Also, embodiments may have fewer operations than described. A description of multiple discrete operations should not be construed to imply that all operations are necessary.

Although certain embodiments have been illustrated and described herein for purposes of description of the preferred embodiment, it will be appreciated by those of ordinary skill in the art that a wide variety of alternate and/or equivalent embodiments or implementations calculated to achieve the same purposes may be substituted for the embodiments shown and described without departing from the scope of the disclosure. Those with skill in the art will readily appreciate that embodiments of the disclosure may be implemented in a very wide variety of ways. This disclosure is intended to cover any adaptations or variations of the embodiments discussed

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herein. Therefore, it is manifestly intended that embodiments of the disclosure be limited only by the claims and the equivalents thereof.

What is claimed is:

1. A computer-implemented method for execution-time prediction of computer instructions, the method comprising: generating, on a computing device, a combined prediction based at least in part on a control point history wherein the combined prediction comprises one or more predictions for predicated instructions and one or more branch target predictions for branch target instructions, wherein the combined prediction relates to one or more blocks of instructions, wherein the control point history was generated at a first time and the combined prediction is generated at a second time, wherein the control point history includes one or more past predicate values evaluated for past predicated instructions and/or past branch targets evaluated for past branch target instructions, and wherein the first time is before the second time;
- fetching block instructions for the one or more blocks based at least in part on the combined prediction;
- executing, on the computing device, the one or more predicted predicated instructions based at least in part on the combined prediction; and
- proceeding with execution on the computing device at a predicted branch target location based at least in part on the one or more branch target predictions.
2. The method of claim 1, wherein generating the combined prediction comprises:
 - generating one or more predicted predicate values based on the control point history; and
 - wherein the block instructions, which correspond to the one or more predicted predicated instructions, are generated based on the one or more predicted predicate values.
3. The method of claim 2, wherein proceeding with execution comprises predicting the branch target location based on the one or more predicted predicate values.
4. The method of claim 3, wherein predicting the branch target location based on the one or more predicted predicate values comprises following a path through a prediction control flow graph based at least in part on the one or more predicted predicate values.
5. The method of claim 4, wherein the computer instructions are in a block atomic architecture, the method further comprising:
 - generating, by the computing device, the prediction control flow graph for a first block of the one or more blocks of instructions; and
 - wherein:
 - predicates in the first block of instructions are represented as nodes in the prediction control flow graph; and
 - branch targets are represented as leaves in the prediction control flow graph.
6. The method of claim 4, wherein following the path through the prediction control flow graph comprises following edges between predicates based at least in part on the one or more predicted predicate values.
7. The method of claim 2, wherein generating the one or more predicted predicate values comprises generating multiple levels of the one or more predicted predicate values in parallel.
8. The method of claim 7, wherein generating multiple levels of the one or more predicted predicate values in parallel comprises, for a level n and the control point history comprising a predicate history of length k:

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generating a predicted predicate value for level n based on a last k predicates;
 generating two predicted predicate values for level n+1 based on a last k-1 predicates and two possible predicates for level n; and
 resolving which of the two predicted predicate values for level n+1 should be used based on the predicted predicate for level n.

9. The method of claim 7, wherein generating multiple levels of the one or more predicted predicate values in parallel comprises generating predicted predicate values for up-to a particular number of levels j in a block of instructions.

10. The method of claim 9, wherein, after predicted predicate values are generated for a block of instructions comprising a number of predicate levels in the block that is greater than j, generating multiple levels of the one or more predicted predicate values in parallel comprises:

repeatedly generating predicted predicate values in multiples of j until the number of predicate levels in the block is exceeded; and

discarding predicted predicate values beyond the number of predicate levels in the block.

11. The method of claim 10, wherein generating multiple levels of the one or more predicted predicate values in parallel further comprises accessing a stored value associated with the block of instructions and representing the number of predicate levels in the block.

12. The method of claim 2, wherein:

generating the one or more predicted predicate values comprises performing a lookup of a particular predicted predicate value based on use of the control point history as an index.

13. The method of claim 1, wherein the control point history further comprises one or more past predicated instructions which were previously executed during an ongoing execution by a program.

14. A system for predictive runtime execution of computer instructions, the system comprising:

one or more computer processors;

a combined prediction generator configured to accept a history of past predicate values and/or past branch target predictions as input and to generate a combined prediction, based on the accepted history, in response to operation by the one or more processors, wherein the combined prediction comprises one or more predictions for predicate values and one or more branch target predictions for branch instructions, wherein the combined prediction relates to one or more blocks of instructions;

an instruction fetch and execution control configured to control the one or more processors, in response to operation by the one or more processors, to:

fetch block instructions for the one or more blocks of instructions, wherein the block instructions are based at least in part on the combined prediction;

execute one or more predicted predicated instructions based on the predicted predicate values obtained from the combined prediction; and

proceed with execution of fetched instructions at a predicted branch target location, wherein the predicted branch target location is based at least in part on the combined prediction.

15. The system of claim 14, wherein the instruction fetch and execution control is further configured to predict the branch target location based at least in part on the one or more predicted predicate values, in response to operation by the one or more processors.

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16. The system of claim 15, further comprising:

a storage medium, coupled to the one or more computer processors; and

one or more prediction control flow graphs stored on the storage medium, wherein respective prediction control flow graphs are configured, for respective blocks of code, to represent predicates in the blocks of code as internal nodes and branches to other blocks of code as leaves.

17. The system of claim 16, wherein the instruction fetch and execution control is configured to predict the branch target location by:

traversal of a path through the prediction control flow graph according to the one or more predicted predicate values; and

after a leaf is reached by traversal of the path, predict a location of a code block branched to at the leaf as the predicted branch target location.

18. The system of claim 14, wherein the combined prediction generator is configured to generate the combined prediction by use of a history of past predicate values as a lookup index to identify the one or more predicted predicate values, in response to operation by the one or more processors.

19. The system of claim 18, wherein the combined prediction generator is configured to generate the combined prediction by performance of multiple lookups in parallel, in response to operation by the one or more processors.

20. An article of manufacture, comprising:

a tangible computer-readable medium; and

a plurality of computer-executable instructions stored on the tangible computer-readable medium, wherein the computer-executable instructions, in response to execution by an apparatus, cause the apparatus to perform operations to schedule instructions to execute a first block of code that includes predicated instructions and one or more branch targets, the operations including:

identifying a combined prediction based at least in part on one or more past predicate values, the combined prediction comprising one or more predictions for predicate values for the predicated instructions in the first block of code, and a branch target prediction for the first block of code, wherein past predicated instructions corresponding to the past predicate values were executed at a first time and the combined prediction is identified at a second time, and wherein the first time is before the second time;

fetching one or more branch instructions based on the branch target prediction of the combined prediction; executing one or more predicted predicated instructions out of the predicated instructions in the first block based at least in part on the one or more predicted predicate values;

based at least in part on the branch target prediction or the one or more branch instructions, predicting a branch target location that points to a second block of code; and

continuing execution with the second block of code.

21. The article of claim 20, wherein predicting the branch target location comprises following a path through a prediction control flow graph for the first block of code to identify the branch target location.

22. The article of claim 21, wherein the operations further comprise generating, for respective blocks of code in a computer program, respective prediction control flow graphs.

23. The article of claim 20, wherein identifying the combined prediction comprises performing a lookup of the one or more predicted predicate values based on a history of past predicate values.

24. The article of claim 23, wherein performing the lookup of the one or more predicted predicate values comprises:
performing multiple lookups of potential predicate values in parallel; and
for potential predicate values at a level n, resolving the potential predicate values using a particular predicate value at a level n-1.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 9,021,241 B2
APPLICATION NO. : 13/321807
DATED : April 28, 2015
INVENTOR(S) : Burger et al.

Page 1 of 2

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page,

On Page 2, item (56), under "OTHER PUBLICATIONS", in Column 2,
Line 1, delete "downloaded" and insert -- downloaded --, therefor.

On Page 2, item (56), under "OTHER PUBLICATIONS", in Column 2,
Line 4, delete "Mcdonalg" and insert -- Mcdonald --, therefor.

On Page 2, item (56), under "OTHER PUBLICATIONS", in Column 2,
Line 5, delete "downloaded" and insert -- downloaded --, therefor.

On Page 2, item (56), under "OTHER PUBLICATIONS", in Column 2,
Line 6, delete "24 page." and insert -- 24 pages. --, therefor.

In the drawings,

In the drawing sheets, consisting of Fig. 7, should be deleted to be replaced with the drawing sheet,
consisting of Fig. 7, as shown on the attached page.

In the specification,

In Column 1, Lines 8-9, delete "35 U.S.C. §371" and insert -- 35 U.S.C. § 371 --, therefor.

Signed and Sealed this
Twenty-seventh Day of October, 2015



Michelle K. Lee
Director of the United States Patent and Trademark Office

