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Flexible Antenna Arrays and Transistor Devices Fabricated Using Inkjet Printing Techniques

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Flexible Antenna Arrays and Transistor Devices Fabricated Using Inkjet Printing Techniques

by

Peter Mack Grubb

Dissertation

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

Doctor of Philosophy

The University of Texas at Austin

May, 2019

Dedication

This dissertation is dedicated to everyone whose flexibility and willingness to see the opportunities made it possible:

My wife and her continual support.

My mentors at Sandia National Laboratories, the University of Texas, and Texas A&M who set me up for success.

And of course my family, for all their love, support, and encouragement through the entire process from the day I decided to apply, through today and beyond.

Acknowledgements

Portions of this dissertation were previously published in Nature Scientific Reports [1], Materials Research Express [2], the MDPI Journal of Manufacturing and Materials Processing [3], in the conference proceedings for SPIE Photonics West [4]–[6], as well as annual reports for grant contract HQ0147-14-C-6003 [7], [8]. All portions included were primarily prepared and researched by Peter Mack Grubb.

Thank you to Dr. Daniele Frisbie and Fazel Zare Bidoky for their expertise in testing and evaluating ion gel based materials for dielectrics.

Additional thanks to Novacentrix and Electroninks Inc. for their support and assistance in developing and testing the various inks and materials used in producing these devices.

Finally, a special thank you to Sandia National Laboratories for supporting the latter portion of my research as part of my continuing employment there.

Abstract

Flexible Antenna Arrays and Transistor Devices Fabricated Using Inkjet Printing Techniques

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The University of Texas at Austin, 2019

Supervisor: Ray Chen

This dissertation reports several improvements to the current state of the art in inkjet printed electronics, including new material formulations and new techniques which allow for smaller negative dimensions than had previously been reported. These new techniques and materials are used to produce several different types of devices on flexible substrates, including a new type of printed array antenna called the frequency scanning array as well as both high performance and high throughput producible transistors. The experiences of building these devices are then used to synthesize potential approaches to integrating the unique advantages of printed electronics into conventional IC manufacturing processes. This arc from material development, to device development, and finally process improvement represents a complete holistic approach to the production of flexible printed electronics devices.

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Chapter 1: Introduction

In recent years one of the major growth industries for electronics has been the ever increasing integration of measurement, quantification, and recording to daily life. These technologies have many names, including wearables, flexible electronics, or the so called "internet of things." Together these technologies are projected to generate $6 trillion in sales in the next five years [9], yet many of the unique challenges presented by this high level of device/lifestyle interaction remain unsolved. Particularly, the requirement for highly flexible and environmentally tolerant devices remains a great difficulty. One fabrication technique which is being used in order to try and meet the unique environmental challenges of the "internet of things" is printed electronics style packaging. As a result, the printed electronics industry is growing rapidly, from $35 billion this year to a projected $50 billion in the next three years [10]. This expansion is due to the unique capabilities provided by printed electronics technology. In particular, the ability for high variability without increasing costs makes the suite of techniques developed for printed electronics of particular interest for "internet of things" devices.

Despite the great promise of this field, it remains a poorly defined discipline. Processes are ill defined, with many projects taking an ad-hoc rapid prototyping approach. This makes communicating evolutions of the field difficult, as it is often hard to integrate a new technique into an existing workflow.

Advancements in the field can be generally split into three categories: materials, techniques, and processes. Materials include the formulation of new inks in order to allow them to be processed by printed electronics apparatuses. This allows new materials such as carbon nanotubes to be used in the printed fabrication of devices. Examples of technique advancements include new types of printing methods which allow for smaller dimensions

compared to existing technologies. Processes encompass the efforts to provide a common language across the discipline in order to maximize impact.

In this dissertation, I will present examples of each type of advancement. For materials, both a new CNT ink and a new hybrid organic/inorganic dielectric ink will be demonstrated. The properties of these inks will be fully characterized and various devices produced to show the potential impacts of them on future fabrication efforts.

In terms of techniques, a new micro gapping technique is presented. One of the more difficult challenges in printed electronics is feature size, which is currently limited to ~30 microns using traditional inkjet methods [11]. Several different methodologies have been developed for working around these limitations, such as imprinting [12] or flexographic printing [13]. While these methodologies allow for micron order feature sizes[14], they require static lithographically defined patterns, minimizing the unique flexibility that inkjet printing allows.

The group's previous work in printing transistors [15]–[17] is extended in order to demonstrate a 100% inkjet printed transistor with a very short channel. By using inks with differing chemical compositions for the source and drain, transistor channel lengths between 300 nanometers and 2 microns were achieved, which represents one of the smallest negative feature sizes to date achieved using purely inkjet methodologies. With these short channels, transistor devices were developed and tested. An On/Off ratio of 10^6 and a high operating frequency with an f_t of 18.21 GHz is demonstrated on a transistor with a channel length of 1 micron. The semiconducting layer of this transistor consists of a CNT thin film formed by printing semiconducting single walled carbon nanotubes in a proprietary non-aqueous solution directly onto a Kapton polyimide substrate. This is the first printed short channel transistor to achieve such extraordinary performance metrics.

In the process field, this dissertation will take experiences from fabricating a wide variety of devices including the high performance transistors, mass producible transistors, and frequency scanning arrays, and use these experiences as a basis for creating a methodology for integrating the advantages of printed electronics into conventional IC assembly. As a part of this effort, current common production workflows will be described and characterized, including the role of modeling in these workflows. Then, a new hybrid methodology will be presented, along with examples of devices that could be or have been produced using this hybrid work flow.

Chapter 2: Overview of Inkjet Printing Techniques and Requirements [1]

ADVANTAGES OF INKJET PRINTING ELECTRONICS

Printed electronics technology has been rapidly growing in step with the emergence of additive manufacturing technologies since the late 1980's [18]. Additive manufacturing, or 3D printing as it is better known, leveraged many different common paper printing techniques in order to extrude three dimensional objects made of plastic. In the same way, printed electronics exploits the heavily developed paper printing technologies in order to deposit alternative materials which allow the creation of conductive, semiconducting, and insulating thin films.

Inkjet printing provides several unique capabilities to the circuit designer's toolbox which are worth investigating in detail. The first and most obvious is that inkjet printing of electronics is a maskless process [19]. Rather than using spincoat methods to cover an entire substrate in a material and then removing the unwanted material via some sort of developer process, inkjet printing strictly deposits the materials needed on a substrate. This offers several advantages over a mask based workflow. Without a mask, design changes are trivial, requiring nothing more than a simple update of the digital pattern file. Furthermore, expensive exotic materials are much more accessible to inkjet printing methodologies since the only portion used it was is printed on the substrate. Both of these advantages ultimately lead to significant cost reductions, as variability no longer implies cost and materials are conserved.

Another unique capability relates to the total area inkjet printing can cover. PCB production methods typically top out in terms of area covered around 10" x 16" [20], while CMOS methods are typically smaller, with wafer sizes maxing out at 450mm [21]. While

[1] Several Figures from this chapter are pulled from [4] and [7]. Any material included from these sources was prepared directly by Peter Mack Grubb.

small scale printing systems don't max out until around 10.5" x 18" similar to PCB manufacturing, large scale roll to roll systems can print design on areas that are 18" wide and many meters long [22]. This capability to produce long continuous designs lends printed electronics some unique capabilities when used for applications such as antennas and transmission lines.

Finally, inkjet printing methodologies are uniquely suited to flexible applications. Many CMOS methods are incompatible with flexible substrates due to their very high temperatures [23]. In contrast, most inkjet technology is centered around lower temperature processes. This allows for a wider variety of potential substrates, including flexible ones such as PET and Kapton. Additionally, the high throughput methods developed for printed electronics are ultimately all based off of high throughput paper printing presses, necessitating the use of some sort of flexible substrate [24]. This means that most development in the field has focused its efforts on low temperature processes which are compatible with these types of systems, rather than the high temperature paradigm found in most CMOS foundries.

TYPES OF INKJET PRINTING

The most widely used printed electronics technology is the piezo-electric or drop on demand model of printing. This technology works similarly to the technology found in common office desktop printers. A membranes shape is controlled by an electric charge, allowing a small drop of the material contained in the "ink" cartridge to form at the exit of the nozzle [25]. Because this general mechanism has been widely used in inkjet printers, it is very well developed and cheap to produce. However, like its 3D printing cousins, the biggest problem with drop on demand systems is scaling. A typical 8.5" x 11" design on a Dimatix drop on demand system (Such as the one shown in Figure 2.1) will take 4-6 hours

to print each layer[25]. Thus, further printing technologies have been needed in order to reach large scale deployment.

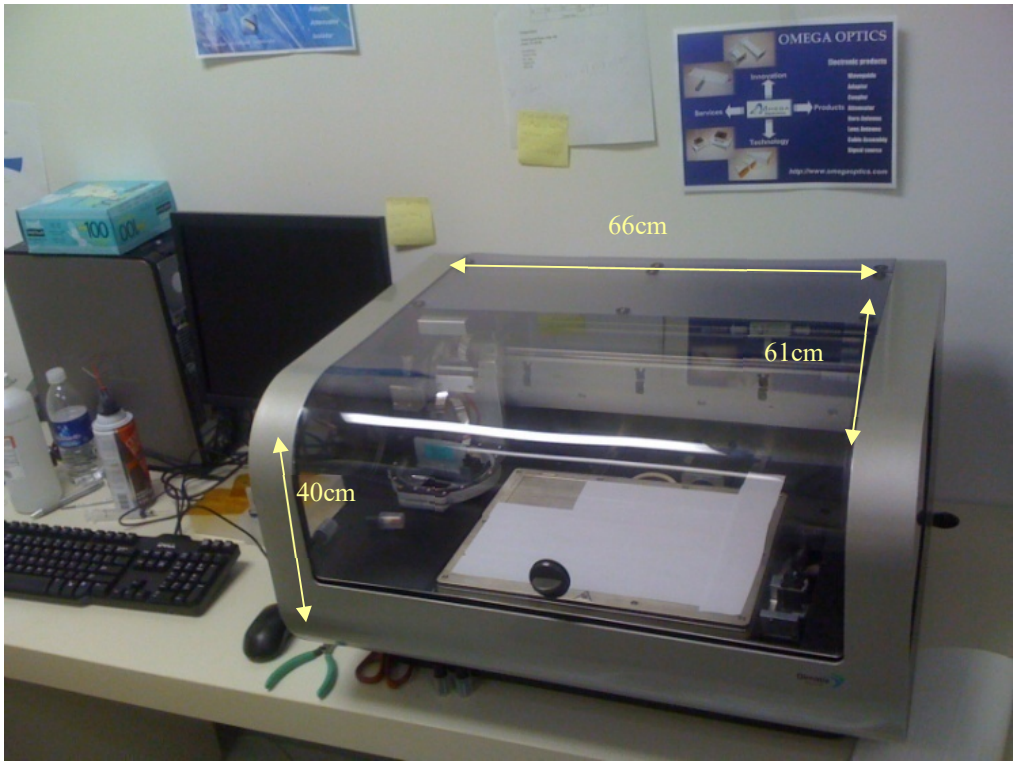

Figure 2.1: A small scale Fujifilm Dimatix Materials Printer.

Another popular printed electronics model is known as aerosol or aerojet printing. Rather than using piezo-electric membranes, these printing systems use pressure to control drop formation and application. The most well-known system is built by Optomec [26], and is technically capable of higher resolutions and better layer control than the Dimatix system. However, the aerosol based systems tend to have much more narrow requirements for printable materials. Some nanoparticle solutions can cause problems with these systems due to their particulate nature. In particular, the liquid can behave unpredictably depending on the solid/liquid ratio being ejected from the aerosol print head. Due to our group's

interest in depositing CNT films, the aerosol systems were seen to be not as good a fit for our particular fabrication requirements.

The most popular technique for large scale printed electronics production is known as roll to roll printing. This technique uses a hybrid of the drop on demand system in conjunction with printing techniques developed for mass production of written word, such as in books or newspapers [22]. In roll to roll printing, a large roll of flexible substrate is placed on one end of a printing tensioner system, such as the one shown in Figure 2.2. Several drop on demand print beds are then placed along the tensioner along with the proper curing systems. With these systems in place, the printer can create printed electronics substrate at a rate of up to 1 meter per minute [27]. The ideal combination of these two technologies would be the development of a print on demand and roll to roll system which was one to one compatible, that is a design on one was completely reproducible on the other. This would allow for a rapid prototyping and production cycle unlike anything which is possible for traditional lithographic production methods.

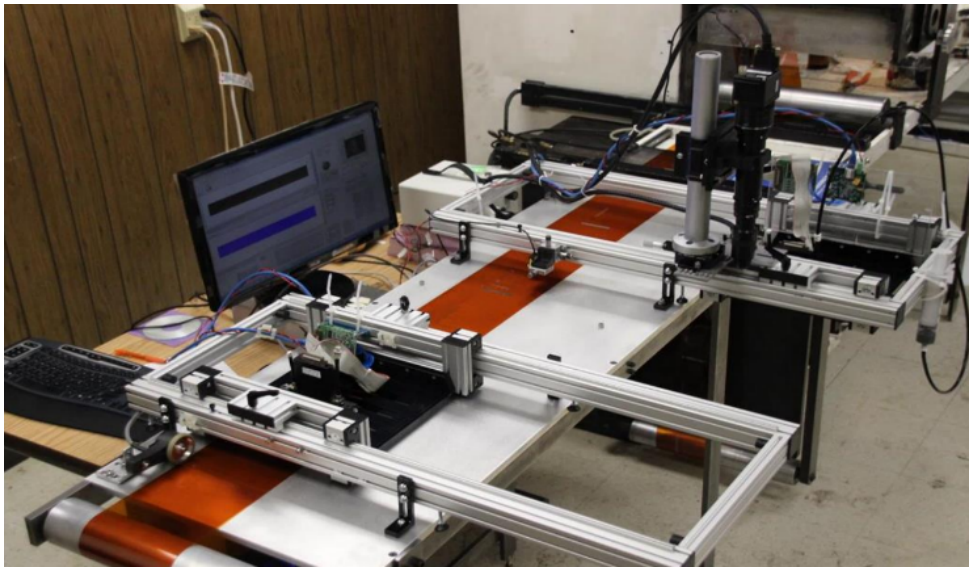

Figure 2.2: A two stage roll to roll printing system with multi-layer alignment.

These high speed roll to roll printing techniques are what make printing so interesting in the context of "internet of things" packaging. Roll to roll printing could allow for the maskless production of flexible electronics without the use of a clean room[22]. This greatly reduces the cost of device production for items which are easily integrateable into daily life. However, getting to this point requires overcoming several materials based challenges.

SUBSTRATES FOR PRINTED ELECTRONICS

The most common material used for printed electronics is Polyethylene terephthalate (PET) and its close cousin Polyethylene naphthalate (PEN). While the two materials are significantly different from a materials science standpoint [28], their similarities are more interesting relative to flexible electronics. Both materials form non-conductive highly flexible substrates which can easily be made in such a way that it is optically transparent. Technically, PEN has better thermal deformation properties than PET due to its chemical structure, as illustrated in Figure 2.3, with the difference of PET vs PEN and PET treated with a heat shrinkage minimizing coating. Given the problems associated with low temperature substrates and flexible electronics, it would seem that PEN would be the more common substrate. However, the chemical changes that make PEN better at high temperatures than PET also increase its cost somewhat [29], [30]. For the most part, the improvements in high temperature performance on PET vs PEN are not worth the cost increases. Some research groups continue to use PEN due to specific surface effects that they are exploiting, but outside these special cases, PET dominates flexible electronics

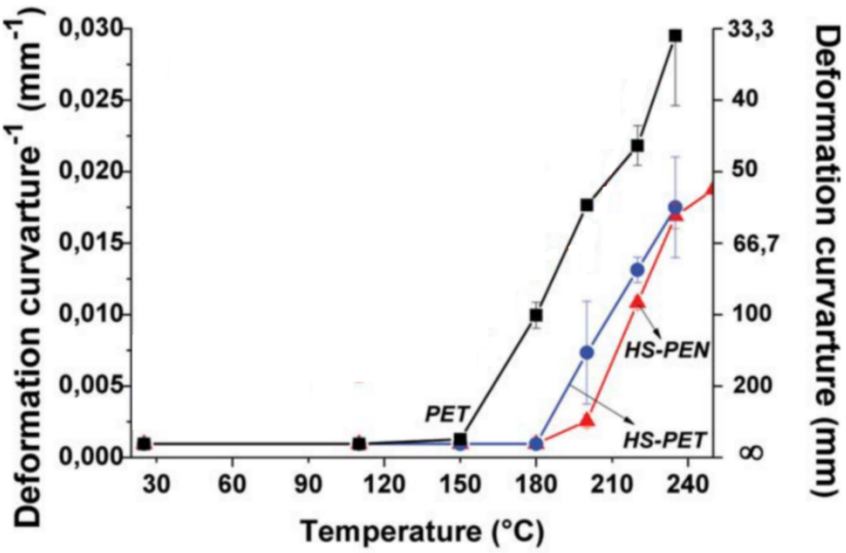

Figure 2.3: Deformation properties for PET, PEN and its derivatives. [28]

The primary competitor to PET in terms of flexible electronics adoption is Kapton. This material is a proprietary film produced by DuPont with a characteristic orange appearance as shown in Figure 2.4. Compared to PET, the temperature tolerance of Kapton is markedly higher, with most variants citing a melting deformation temperature of over 500 Celsius [31]. This temperature difference opens up whole new classes of materials which can be used on a Kapton substrate but are functionally incompatible with PET or PEN. However, Kapton is also much more expensive than PET, with most quantities cost approximately 10 times as much as the PET alternatives [32]. This increase in cost makes Kapton unusable for many common flexible projects. Despite this, it is the substrate of choice for research and development. When other variables are under investigation, it is helpful to minimize the potential for problems from the substrate.

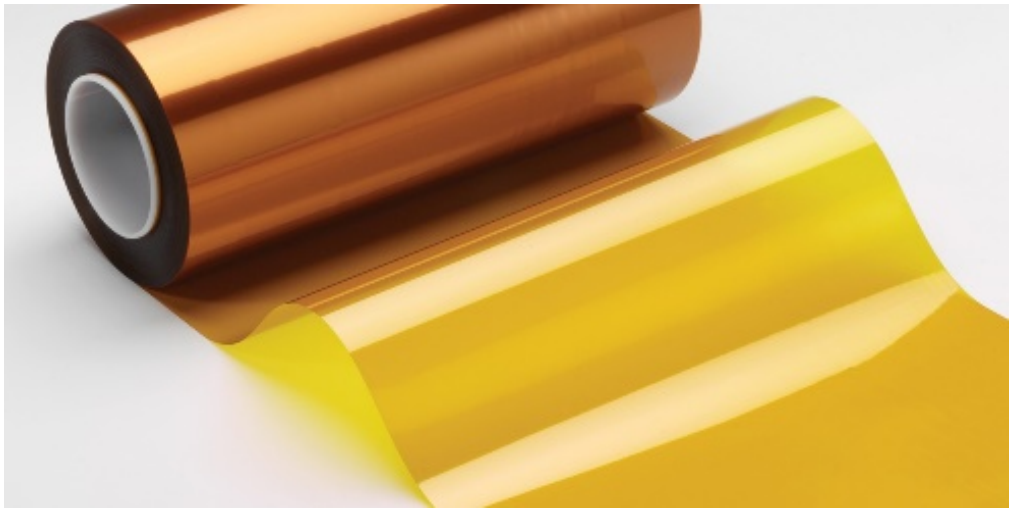

Figure 2.4: A roll of Kapton polymide film. [32]

Due to the high temperature requirements for sintering many silver nanoparticle based inks, most of the projects pursued in Dr. Ray Chen's lab use Kapton as the substrate. Some of the transistor testing was performed on glass slides in order to eliminate the possibility of substrate coupling issues, but once this potential source of error was eliminated development focused exclusively on the Kapton substrate.

REQUIRED PROPERTIES FOR JETTABLE MATERIALS

In order for a solution to be usable by a piezo-electric inkjet printer, there are some very specific properties it must conform to [33], [34]. For a given piezo-electric membrane design, there will be a limit to how much force it can exert on the liquid in the ink cartridge. This enforces a maximum viscosity requirement on the liquid, as high viscosity liquids such as glycerol will require too much force to pull a drop into the piezo-electric chamber. However, if the viscosity is too low, a drop will not form, and instead the liquid will just flow straight out the nozzle, this causes long lines to form, instead of drops being placed at specific locations on the substrate.

The other primary fluid property the ink solution must possess relates to its surface tension[34]. For the same reasons as the viscosity, this must fall in a narrow range. Too high and the piezo-electric material will not be able to provide enough force to break the surface tension at the nozzle/air interface. Too low, and the drop will not properly form, keeping the system from being able to properly place the ink on the substrate with any kind of precision.

When selecting inks, one other property that is essential to examine is the annealing method and temperature. Kapton substrates have a maximum temperature around 500 Celsius depending on the exact type used [31]. This means that while there are materials that could theoretically be deposited using an inkjet printer, many are incompatible with the types of substrates that are typically used. One way to avoid this issue is through the use of high intensity UV curing. Sometimes called "photonic curing," these systems use pulsed UV light to rapidly cure the inks. This curing technique requires inks which are specifically designed to absorb UV spectra light, but otherwise are one of the primary ways in which high speed curing is achieved.[35]

These different properties will by what type of printer and cartridge are used. Some types of print heads use piezo-electric membranes that are stronger than others, which changes the range of both viscosity and surface tension that the system will support. This tends to complicate ink commercialization, as specific solutions tend to work best with specific print systems. Fortunately, viscosity and surface adjustments are usually possible through the addition of solvents and emulsifiers such as glycerol and Triton-X100. [34]

Chapter 3: Material Selection and Ink Development [2]

SILVER CONDUCTIVE INK

Given the emerging nature of the printed electronics technology, it is unsurprising that many different types of conductive inks have emerged to try and fill the needs of researchers and engineers. Costs, chemical properties, and even basic annealing mechanisms vary wildly across the entire range. Of the many various types of conductive materials that have been tried to date, currently the material of choice for most projects needing a conductor is silver, due to its very high conductivity and relatively low annealing point.

Over the course of the printed transistor project, four different silver inks were tested and used in various developmental applications: Novacentrix JS-B40G, UTDots UTDAg40IJ, Paru Co. PG-015, and Electronink RxNA-Ag1012. Each of these inks is pictured in Figure 3.1 below.

[2] Sections of this chapter are pulled from [3], [4], [7], [8], For all of these publications, Peter Mack Grubb was responsible for all preparation and sourcing of materials, printing, and testing of final devices. Ion Gel material was produced in conjunction with Dr. Frisbie from the University of Minnesota. Hybrid dielectric development was accomplished in collaboration with Farzad Mokhtari-Koushyar. Raman spectroscopy was performed with the assistance of Farzad Mokhtari Koushyar and Aref Asghari.

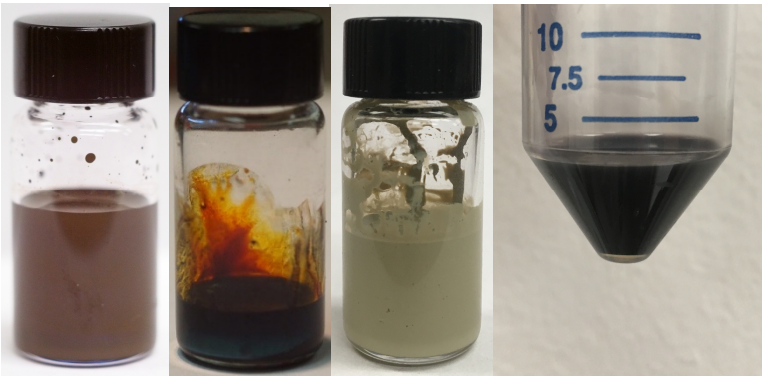

Figure 3.1: The various silver inks used in the project from left to right: Novacentrix JS-B40G, UTDots UTDAg40IJ, Paru Co. PG-015, and Electroninks RxNA-Ag1012.

The UTDots, Novacentrix, and Paru Co. inks all use a very similar mechanism for printing silver. The solution consists of a proprietary solvent combination that meets the requirements of the printer with silver nanoparticles dispersed into it. Silver nanoparticles have a much lower melting point than bulk silver due to the high surface area to volume ratio [36]. When heat is applied to these inks, the solvent evaporates leaving the silver nanoparticles which then melt into a single conductive sheet of silver. This method has been the dominant mechanism for silver printed electronics in recent years [37], and has seen much development by multiple companies in an attempt to commercialize the technology. However, while the three inks are similar in terms of mechanisms, they vary quite a bit in terms of cost, chemical composition, and print quality. In our experience, the Paru Co. ink had the best print results of the three. However, the solvent combination used therein was very prone to clogging the nozzles of the ink cartridges when not in use, rendering the ink far less useful. This forced us to use the Novacentrix cartridge as our day to day printing ink due to its consistency and solid print results. The UTDots ink was the most difficult of the three to print with, but the difficulties had to be worked with as it was

one of the only non-polar inks we were able to consistently source. This became crucial as ink chemistry came into play with both surface effects and inter-ink interactions.

The Electronink product was very different from the other three silver inks we tested. Instead of using a silver nanoparticle solution, the Electronink used a silver salt solution. When heat was applied, the solvents evaporate, and a reaction occurs leaving only the silver on the substrate. This method has great potential for future printing projects, as it has a much lower unit cost than the silver nanoparticles. However, it is currently under development, and thus the ink product was not as consistent batch to batch as we would have liked. While we initially had some very promising results with this ink, it was ultimately abandoned due to reproducibility problems.

PRINTABLE SEMICONDUCTORS

The critical development in the past 15 years that has enabled the development of printed transistors is the emergence of printable semi-conductors. Conductive printing materials were some of the earliest materials developed for use with inkjet printers in an electronics paradigm. However, semiconductors have proven more challenging. CMOS lithography doesn't have an analog for "deposited" semiconductors, as the semiconductor material is usually the basis for the whole device. Thus, the development of new materials was needed.

Three classes of materials have emerged as possibly solving this problem: organic materials, silicon nanoparticles, and more recently carbon nanotubes. Organic materials such as polythiophene or other semiconducting polymers were some of the first printable semiconductors [38]. However, these materials have major limitations with regard to high frequency operation, usually topping out in the low megahertz range with cutting edge technology [39]. The first attempt to find a higher frequency semiconductor used silicon

nanoparticles to try and build something that behaved more like a CMOS device [40]. However, silicon's melting point even in nanoparticle is very high. This meant a binding polymer was required between the silicon nanoparticles. Unfortunately, polymers also have very poor high frequency responses. While researchers were able to get decent mobilities out of these materials, the high frequency response was not adequate.

Because of the limitations of organic and silicon nanoparticle semiconductors, high frequency printed transistors have largely focused on using carbon nanotube (CNT) based solutions for the semiconducting material. Originally CNT based semiconductors were extremely expensive and hard to implement due to the fact that CNTs naturally form in 1/3 semiconducting and 2/3 conducting proportions. However, Nanointegris developed a method to separate the semiconducting CNTs out with a greater than 99.9% purity [41]. This opened the door for the development of CNT based inks. All of these inks operate on basically the same principle. CNTs are dispersed in some kind of solvent with a relatively low evaporation point. The solvent with the dispersed CNTs is then printed on the substrate, and heat is used to evaporate the solvent. What is left is some form of CNT field, similar to the one shown in Figure 3.2.

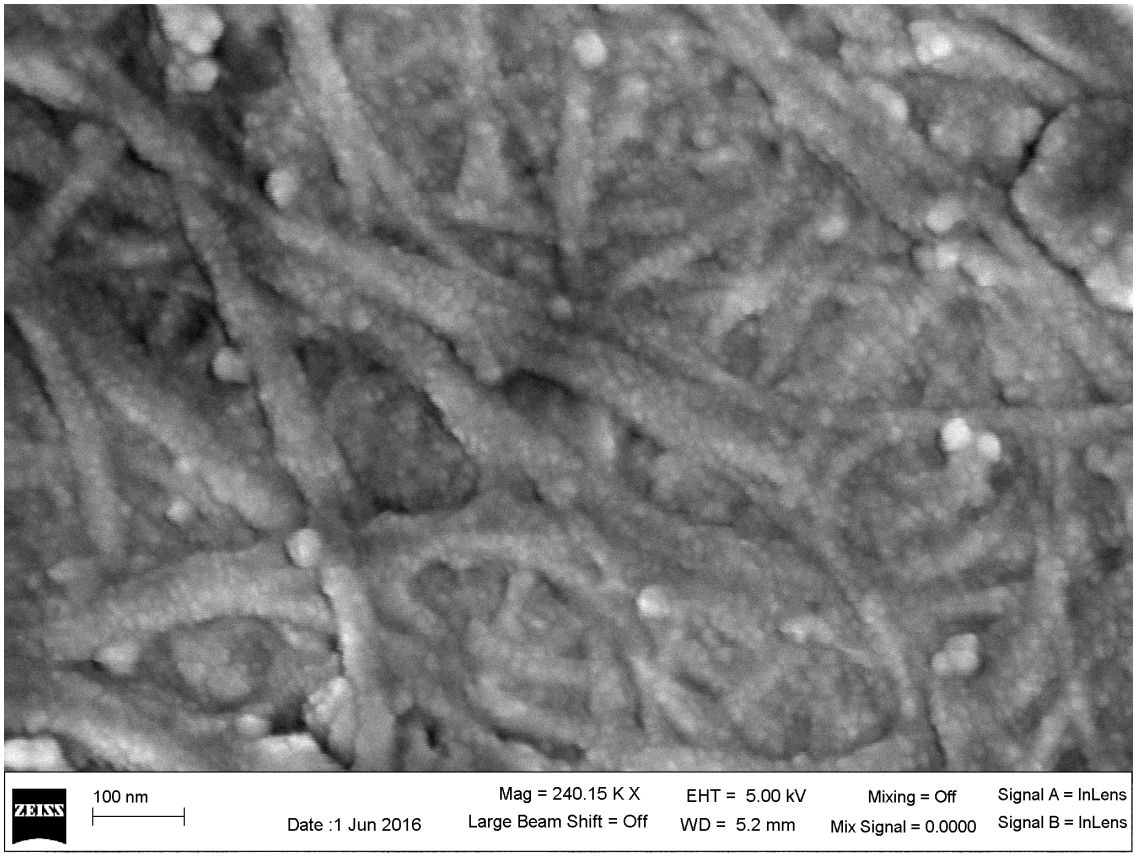

Figure 3.2: Unaligned single walled carbon nanotubes that have been applied using a Dimatix printer. The solvent has been annealed away, though some residue remains.

The primary downside to CNT based semiconducting layers is the fact that it is alignment sensitive. If there is not some path through the CNTs from the source to the drain which forms a continuous line, then no semiconducting effect will be observed. One way to avoid this is via the use of a percolated mesh such as the one shown in Figure 3.2 [42]. At high enough concentrations, a mesh forms such that semiconducting is achieved. Another alternative is self-alignment using dip coating, which has been explored by previous members of Dr. Ray Chen's group [16]. While this method is effective, it is not fully roll to roll compatible, limiting its applications to small scale prototype devices. For

the development of the high speed transistors as a part of this project, a third alternative was developed using electric fields to align the CNTs, which is reported below.

CARBON NANOTUBE INK DEVELOPMENT

One of the key elements in developing high frequency compatible printed thin film transistors (TFTs) has been the development of inexpensive high purity CNTs by Nanointegris Inc. [41]. While the upscaling of these technologies have allowed semiconducting CNTs to be commercially available in purities greater than 99.9%, this does not solve the issue of how to apply these CNTs to a substrate in a precise fashion.

Previously our group developed a CNT inkjet solution using 1-Cyclohexyl-2-pyrrolidone (CHP) [15]. CHP was selected as the solvent due to its relatively low boiling point, ideal viscosity and it polarity. As a polar substance, the CNTs would remain in solution for an extended period of time, giving the ink a good shelf life [43]. However, the CHP was not without its downsides. Firstly, due to its polar nature the CHP could not be applied across multiple inkjet layers. After the first layer of ink was cured, the highly hydrophobic CNTs would push any CHP/CNT solution away from the target site. Given that the CNT concentration was limited to 20% by weight, it was almost impossible to achieve consistent semiconducting layers using this formulation. Additionally, the CHP solution is not compatible with high speed roll to roll printing methodologies. The solvent must be burned away using some sort of thermal curing system [15]. With these negatives in mind, our group worked to formulate a new CNT ink which wouldn't have these negative properties.

For an ink to be compatible with an inkjet deposition system, the two most critical properties are the surface tension and the viscosity of the ink solution. Typical values of 32-42 dynes/cm for surface tension, and 10-12 cps for the viscosity have been recorded as

good targets for an ink in a Fujifilm Dimatix cartridge[34]. While some R2R systems have varying targets for these values, they provide a good benchmark target for developing a new ink.

In addition to these solvent properties, the other key property for this CNT ink would be the absorption spectra. Typically, a high speed R2R system uses some sort of flash lamp system to emit high energy UV and visible light pulses. The ink can then absorb the energy from these flashes, annealing the ink. The development of this CNT ink targeted the Xenon Sinteron-2000 system pictured in Figure 3.3, which features a high intensity pulsed xenon lamp that provides a broadband spectrum from 240 nm to 1000 nm with adjustable pulse energy up to 1500 Joules/pulse [44], which corresponds to UVB up to the Green/Yellow split of the visible light bands.

Figure 3.3: Xenon Sinteron-2000 system used for developing the CNT ink.

One class of solvents with absorption in the right range for usage with the Xenon Sinteron-2000 are the aromatic hydrocarbon liquids including both Xylene and Toluene.

These solvents typically have a strong absorption peak at 400 nm in the UVA range, with a second peak between 575 nm and 750 nm depending on the exact compounds in solution[45]. Consequently, these materials are well suited to absorbing the energy from the Sinteron, allowing them to be evaporated using only the high intensity light pulses.

Of these aromatic hydrocarbons, Xylene is one of the most common. However, its viscosity is only 0.6 cP in a multi isomer blend. This is far too low to have drop formation using a drop on demand printing system. Some sort of thickening agent is needed in order to raise the viscosity of the overall printing solution. The most common thickening agent used in inkjet formulation is glycerin, as it has an extremely high viscosity requiring very little to reach the target viscosity needed. However, glycerin is not miscible in xylene, necessitating the addition of a moderator, in this case methanol, to allow for a stable solution. The last component of the CNT ink is Triton X-100, which is an emulsifier that both keeps the CNTs in the solution and lowers the surface tension to a usable level.

Once the solvents all had been identified, the next step was to identify the proper concentrations. Experimentally, it was determined that a 1:4 ratio of methanol to xylene provided a solution which was miscible with the glycerin. Then, the Refutas equation for viscosity blending was used to determine the amount of glycerin needed to reach the target viscosity[46]. The Triton X-100 concentration was determined based on other ink formulations in the literature [47]. The end result yielded a formula of 0.5% glycerin, 0.1% Triton X-100, 19.4% methanol, and 80% Xylenes. This solvent being jetted by a Fujifilm Dimatix cartridge is shown in Figure 3.4.

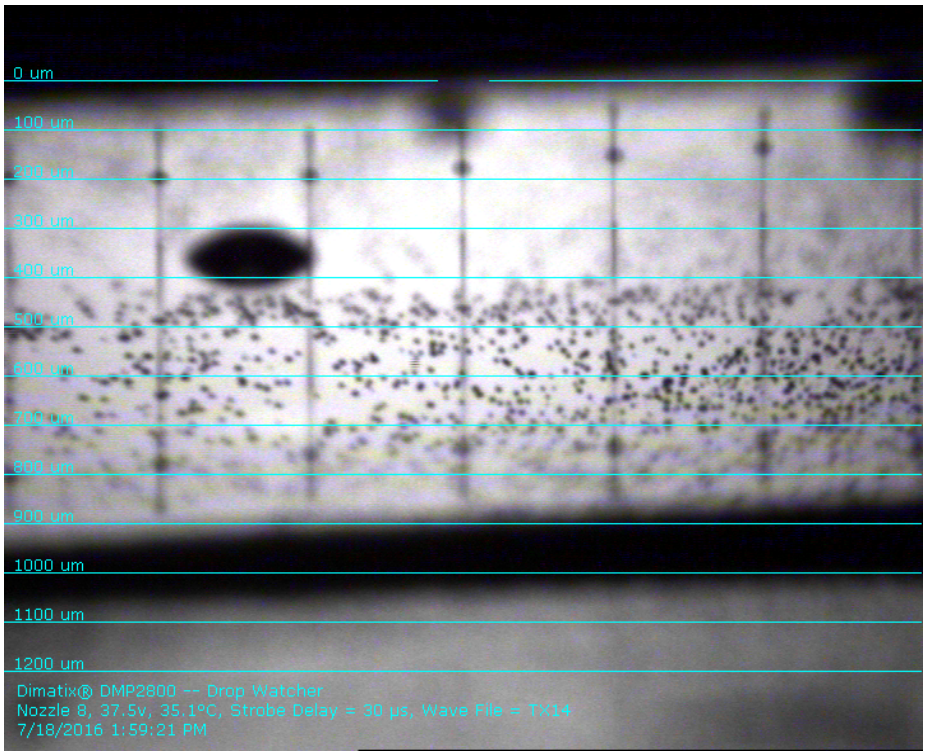

Figure 3.4: Drop watcher view of the new CNT solution on the Dimatix printer. Drops have stability similar to the CHP solution, though markedly better performance once on the substrate.

With the concentrations determined, an IsoNanotubes-s100 CNT thickfilm from Nanointegris was dissolved into the solution at a concentration of 20% by weight. These CNTs are high purity, with no polymer wrapping or other functionalization, and have been sorted to be 99.9% semiconducting CNTs. The resulting solution is shown in Figure 3.5a. This ink solution was then printed in a small patch on a piece of Kapton and glass as shown in Figure 3.5b, which was then placed under the Sinteron. The UV light was then pulsed 12 times at 1.8 kV with a 0.4 second separation between the pulses. This put sufficient energy into the solvent to evaporate the non-CNT components, as shown in Figure 3.5c. An SEM micrograph of the CNT field remaining on the substrate after the curing process is shown in Figure 3.5d.

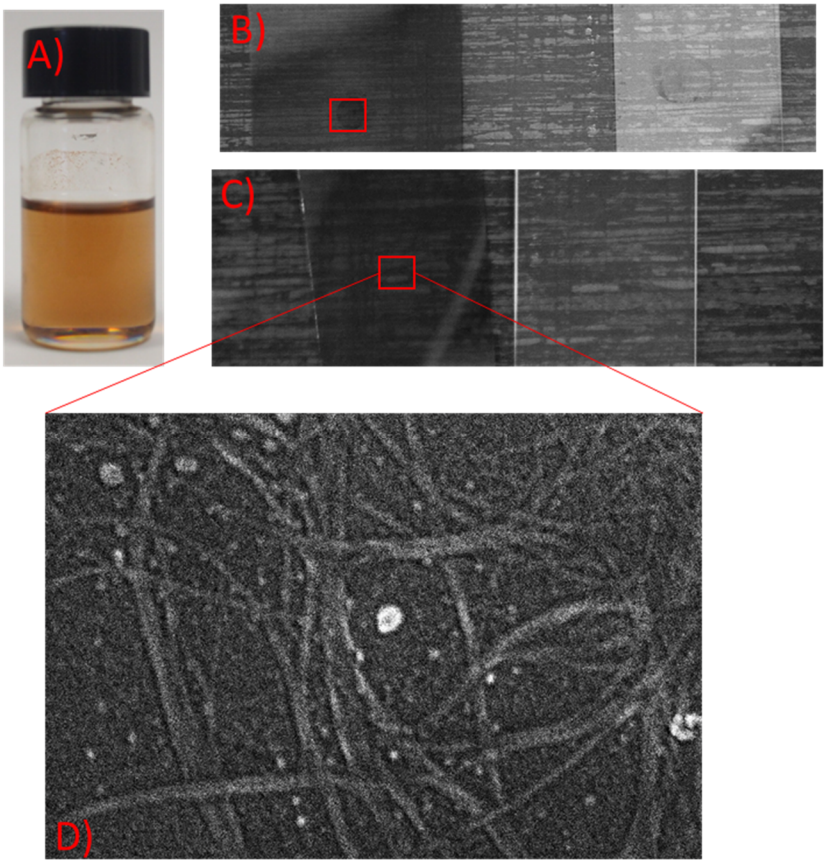

Figure 3.5: A) The CNT Ink Solution, B) Printed solution before curing and C) after curing, D) SEM of the CNT field post curing. No disturbance of the CNT field by the high intensity pulses was observed

In order to assess the purity of the deposited CNT ink, Raman spectroscopy was used. First, as a baseline a reading was taken of the bulk CNT thick film provided by Nanointegris. CNTs were then applied to a Silicon substrate and cured using the Xenon Sinteron, and a reading was taken from the resulting thin film. It is worth noting that readings were attempted on a Kapton thin film, as this is what is typically used for producing R2R transistors. However, the Kapton substrate was too transparent for the Raman apparatus used to gather the data. The resulting data from the two readings is shown in Figure 3.6.

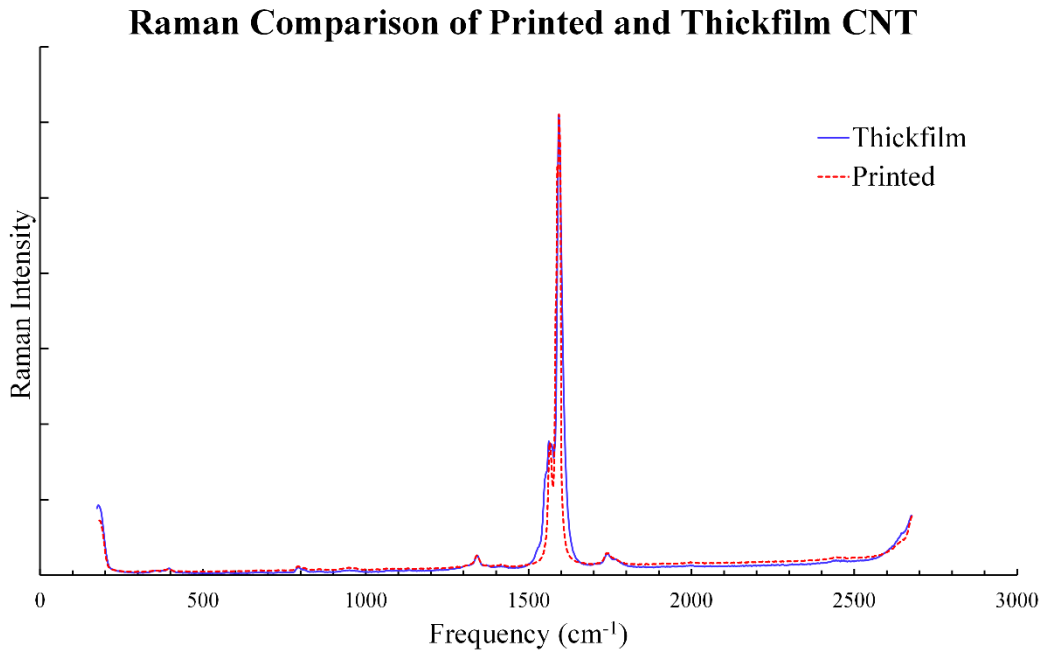

Figure 3.6: Raman spectroscopy of the thickfilm and printed film shows no significant shift in peaks, revealing very little contamination from un-annealed solvents.

The only significant downside of the new solution is that the CNTs do not remain in solution as well as they do in the CHP mixture. This is the downside of most non-aqueous CNT solutions [48]. Much of this is mitigated by the use of Triton X-100, an emulsifier which improves CNT dispersion. For what minimal settling that occurs, a simple hand shaking of the cartridge prior to usage is sufficient to minimize the effects of this issue. Furthermore, an ink recirculation system such as those used in industrial scale applications would also be sufficient to maintain the CNTs in suspension.

DIELECTRIC MATERIALS

One of the primary problems which is causing decreased yield rate with the transistors is the dielectric material used for the gate insulator. Low temperature printable dielectric materials present several unique challenges. The classic gate insulator of silicon dioxide is not really an option do to the high temperatures required to grow it, and the lack

of silicon present in most printed devices [49]. Other modern high-K dielectric materials present their own problems as well, with most materials in this class having annealing temperatures well beyond the limits of Kapton [50]. For example, one common high-K dielectric is ZrO_2, which has an annealing temperature greater than 550 Celsius [51]. This makes most high-K dielectrics, even in nanoparticle form, unusable for flexible electronics. Currently, much research is being done to try and find an elegant solution to this problem. In the course of our research we investigated and tested devices using three classes of printable dielectrics intended for usage as gate insulators including acrylates, ion gel, and a hybrid organic/inorganic material.

The primary class of materials our group has built transistors with in the past are acrylates. These materials typically take the form of photoresists such as AZ5214 and AZ5209. A device using the AZ5214 dielectric is pictured in Figure 3.7. Characteristics include very low dielectric constants on the order of 0.8-2.2 [52], higher viscosity, and good temperature tolerance. While the group has achieved remarkable results using these materials, the yield rate associated with them tends to be very low. With the high viscosity of the materials, particularly AZ5214, printing the material consistently is very difficult. Additionally, the material does not spread very well or very consistently across Kapton. This makes achieving a thin and uniform layer of material difficult. The roughness is visible in the black and white image of a typical deposition in Figure 3.8. Despite these downsides, the material has very good high frequency response, and is not as prone to pin-holing as many dielectric materials, making it a solid baseline for investigating the various dielectric materials under consideration.

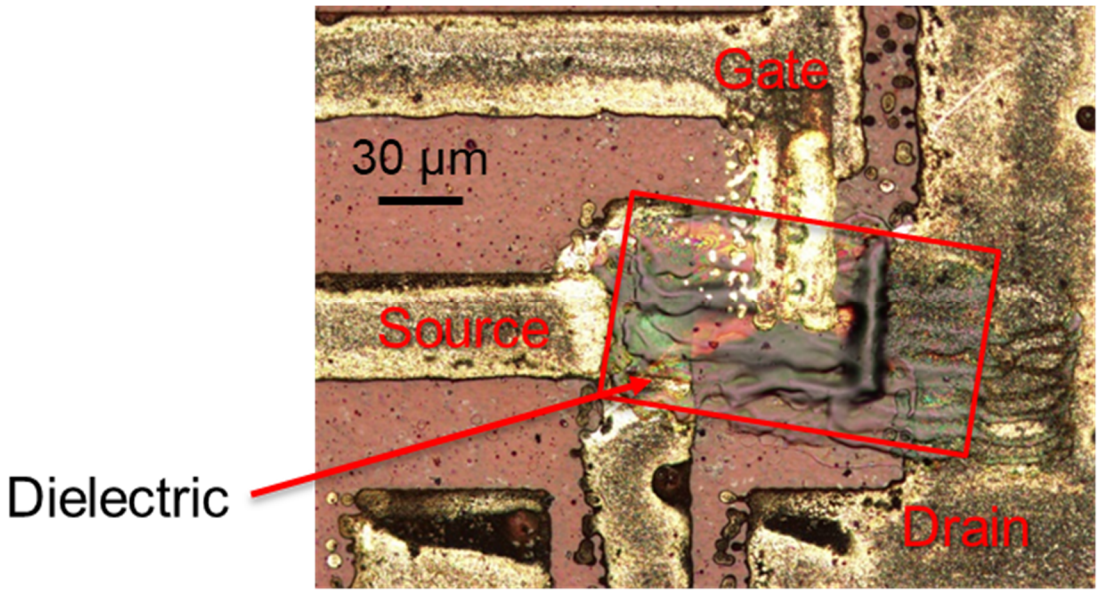

Figure 3.7: A typical AZ5214 thin film transistor. Note the inconsistent thickness.

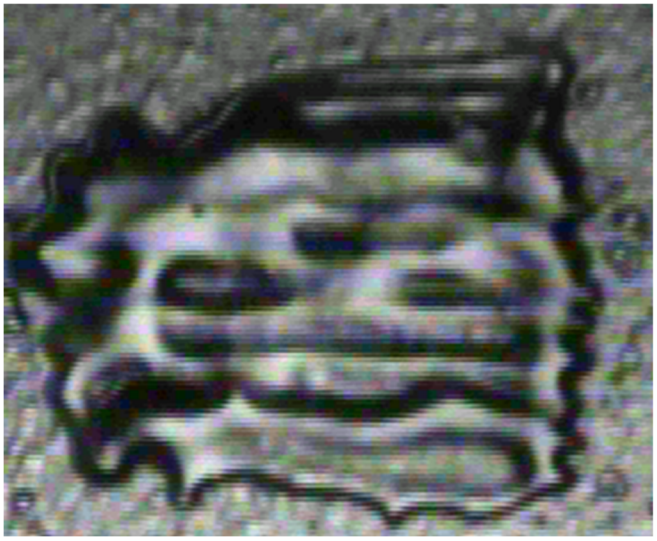

Figure 3.8: Typical AZ5214 deposition. Note the very rough surface with many high and low points despite still being in liquid form. This is due to the high viscosity of the material.

One method we used to boost the yield rate of the acrylate based devices was diluting the photoresist material with propylene glycol monomethyl ether acetate (PGMEA). This solvent is commonly used to control the thickness of photoresists when spin coating on silicon wafers. In the context of printing, it reduces the viscosity of the material, but burns off when the device is heated up. By using a 75% AZ5214/25% PGMEA solution we were able to significantly boost the yield rate of the acrylate based devices with minimal downsides. Additionally, this solution shows promise of being compatible with roll to roll production, whereas pure AZ5214 is too viscous for the Konica Minolta cartridges used in the group's roll to roll system.

While the acrylates have a history of providing high performance devices in our group [17], even with the dilution methodology, yield rates remain stubbornly stuck in the 25-50% range. This is not workable when attempting to build 8x8 phased array devices, so our group has been investigating other alternatives. One dielectric material which has been receiving lots of attention in printed electronics is ion gel. Given ion gel's status as an emerging material, our group consulted with an expert on ion gel devices, Dr. Daniel Frisbie, who provided the support necessary to design and implement devices using these materials. A typical ion gel gate transistor is shown in Figure 3.9.

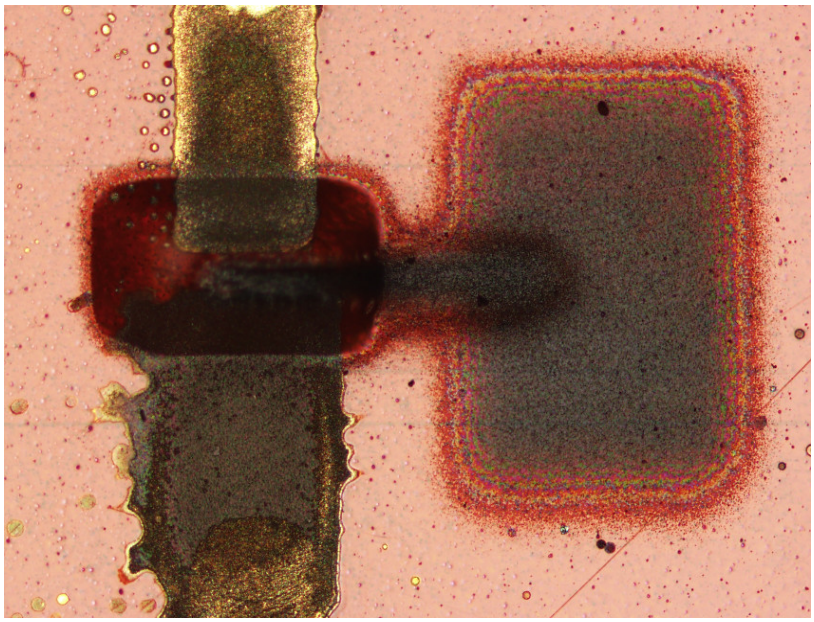

Figure 3.9: A typical ion gel-based transistor with a PEDOT: PSS gate.

Ion gel research grew out of the need for low operating voltage printed electronics while researching printable batteries leads. These requirements can be satisfied by Electrolyte-gated transistors (EGTs)[53], which are a special type of thin film transistor. EGTs with 'ion gel' as the gate dielectric have shown promising characteristic for printed electronics such as electronic ON/OFF current ratio of 106 and gate-drain current of nAmps and more importantly sub-3 volt operating voltages[54]–[56]. Ion gel is a mixture of triblock copolymer and ionic liquid [57]. Despite micron level thickness, ion gel shows specific capacitance in the order 10 $\mu F/cm^2$ which is 10,000 times larger than thin conventional dielectric layer like PMMA, which gives ion gel more printability with current printing methods to relax the alignment requirements [58]. Moreover, ion gel capacitance is constant for thickness range of 2-10 µm, which also eliminates the thickness control as a challenging step in the printing of conventional dielectrics [59].

For ion gel ink, a solution with the mass ratio of 1/9/90 for poly(styrene-*b*-methyl methacrylate- *b* -styrene) (PS-PMMA-PS) /1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)amide [EMI][TFSI]/ethyl acetate was made. The (PS-PMMA-PS) polymer was synthesized by Dr. Hong Chul Moon in the Frisbie/Lodge group. [EMMI][TFSI] was purchased from EMD Chemicals. For the poly(3,4-ethylenedioxythiophene):poly(styrene sulfonate) (PEDOT:PSS) ink, PH1000 was purchased from Heraeus, and 6% volume ethylene glycol was added to the ink to enhance the conductivity. The chemical structures for these inks are shown in Figure 3.10.

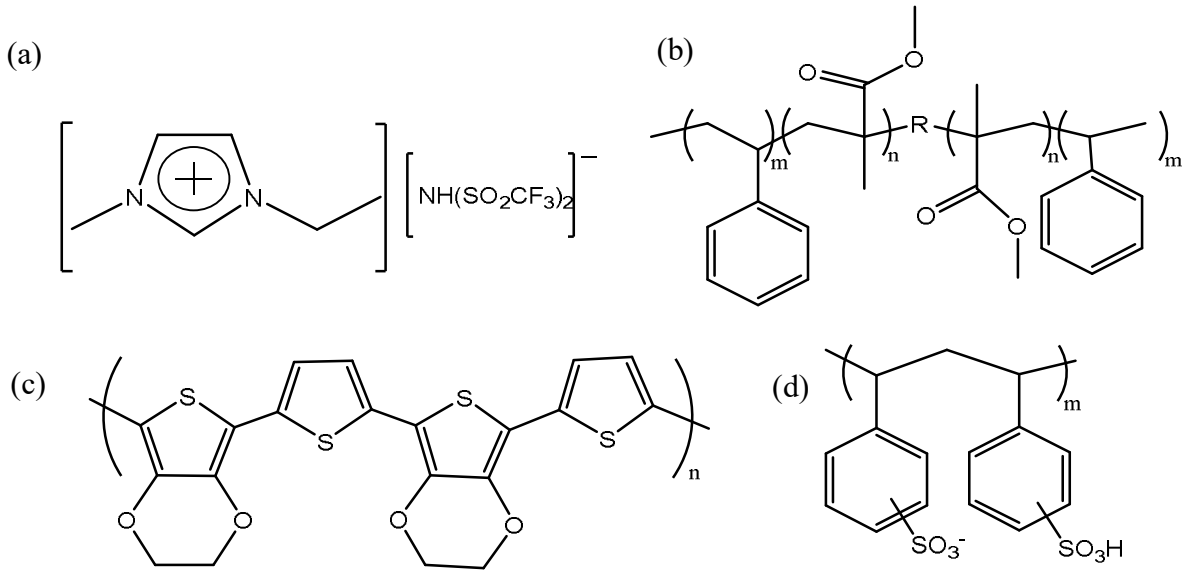

Figure 3.10: Examples of organic dielectric, conductive materials. (a) [EMI][TFSI] Ionic liquid. (b) SMS, PS-PMMA-PS, triblock copolymer (c) PEDOT (d) PSS. The mixture of (a) and (b), ion gel, is used as dielectric. The mixture of (c) and (d) is a well-documented conducting polymer.

While ion gel enabled us to achieve prints with yield rates in excess of 95%, the material has several major disadvantages. Fabrication is non-trivial as it requires the usage of an aerosol-jet printer. Aerosol-jet printing is relatively new printing method for printed

electronics with less viscosity sensitivity than inkjet printers. Aerosol-jet printers are nozzle based methods, in which despite 100 μm sized nozzle, printed high aspect ratio line with width as narrow as 10 μm is accessible [60]. Since our group does not currently possess this equipment, Dr. Frisbie's group performed these prints. Additionally, ion gel lacks the durability of the acrylate gate insulators. Simply wiping a soft cloth across an ion gel device completely destroys the gate layer. This lack of environmental hardiness is exacerbated by the fact that any annealing over 100 Celsius causes the material to evaporate, limiting gate electrodes to very low temperature annealing materials. The most concerning issue with the environmental stability of the ion gel devices is its lack of voltage tolerance. At a voltage greater than 2V or less than -2V, the ion gel permanently deforms, burning the device out. This makes the power supply concerns for a device using these transistors very important.

HIGH VOLTAGE DIELECTROPHORESIS

One of the primary challenges of using carbon nanotubes (CNTs) in a printed electronics setting is the lack of alignment. In CMOS design flows using CNTs, the general method is to grow a series of CNTs, such that there are many groups going from one side of the channel to the other. When using the inkjet deposited CNTs, there is far less control. CNTs tend to spread out from the point where the fluid first contacts the Kapton, forming outward pointing lines, and generally showing minimal directionality in their placement. An example of some unaligned CNTs is shown in Figure 3.11.

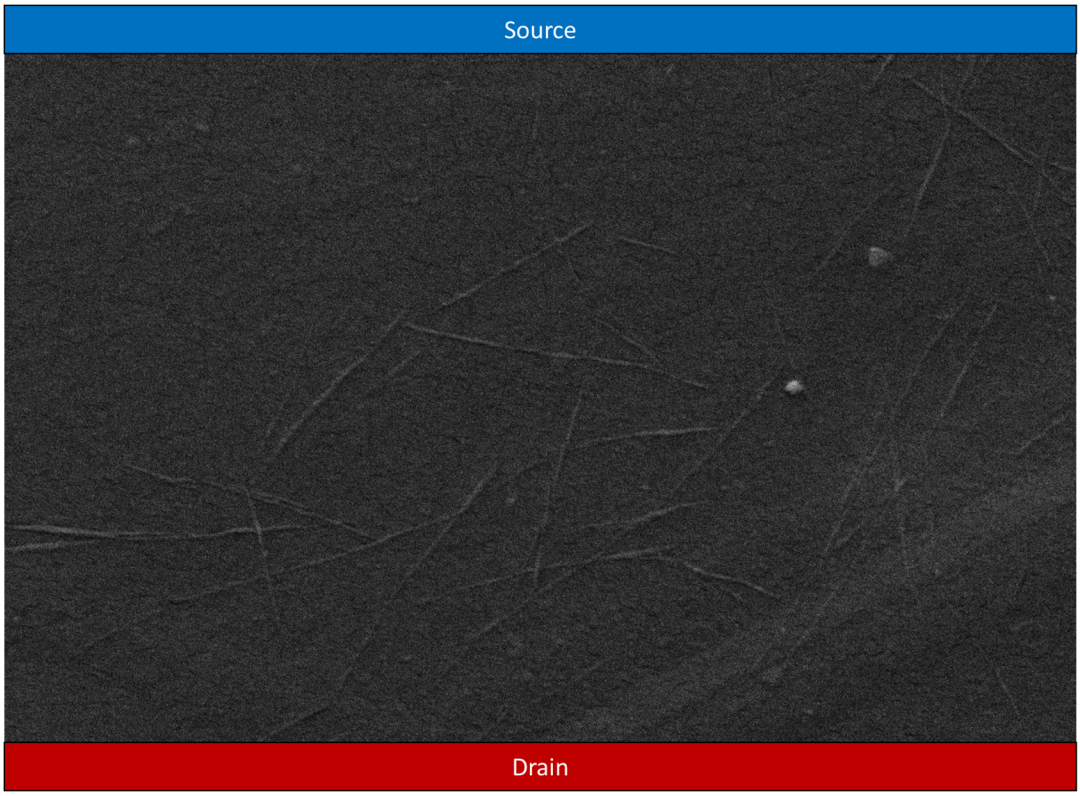

Figure 3.11: SEM image of unaligned CNTs at 77.07kX magnification.

The problem with unaligned CNTs is it requires very high densities of them in order to achieve a semiconducting layer for the transistor. High density leads to other undesirous effects, including very high drain currents and CNT to CNT current induction effects. An ideal CNT layer is almost entirely aligned, with as many CNTs as are needed in order to reach the desired max I_{dsat}.

Thus far in inkjet printing there have been very few attempts to align CNTs. However, in a CMOS setting there have been many methods tried. One which is particularly well suited to inkjet production flows is Dielectrophoresis (DEP). In DEP, the CNT/CHP solution is placed between two electrodes which will eventually form the source

and drain in a transistor setting. An electric field is then applied, which the CNTs align to due to their dipole nature.

In CMOS settings, this method has largely been abandoned. In a clean room setting there are better methods which can be used, though none of these transfer to inkjet printing very well. However, when applied to inkjet printing, DEP leads to much better aligned CNTs. By applying an AC voltage with a frequency on the order of 10 MHz, and a DC bias of approximately 10 Volts, the alignment shown in Figure 3.12 was achieved.

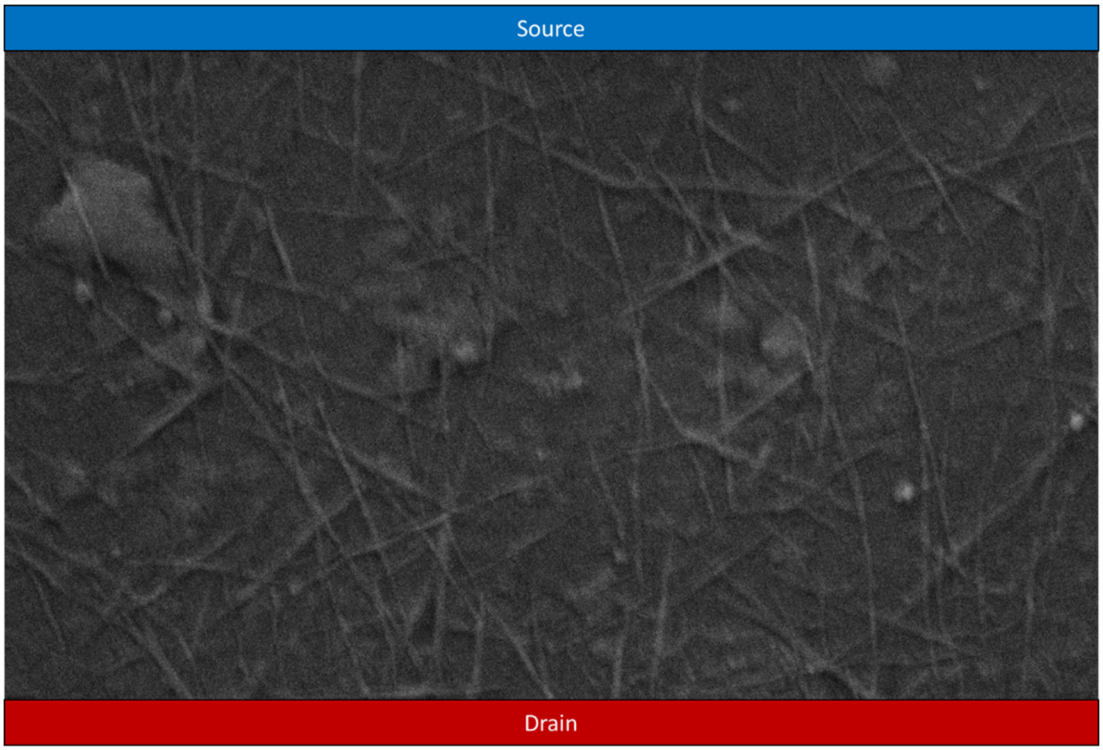

Figure 3.12: SEM image of aligned CNTs at 118.42kX magnification.

While the initial results are very promising, this methodology is not without challenges. Foremost among these is the difficulty in defining how “aligned” a group of CNTs are. While qualitative statements are not too difficult, having a quantitative

definition of alignment is critical. To this end, a model is currently being developed to predict the CNT behavior while undergoing DEP. The other major challenge relates to localized shorts in the CNTs. Even at best purity, 1 in every 1000 CNTs is conducting. This makes the odds that a conducting CNT bridges the gap very high. If this happens without DEP it is a simple matter to apply a ramped current to burn out the conducting CNT. However, if DEP causes a conducting CNT to suddenly bridge the gap between the two electrodes, then it can cause a sudden high current event. This can cause burnouts of the silver and semiconducting CNTs, causing permanent damage to the device being developed. In order to combat this, low current and high voltage is used. The low current prevents the CNTs from burning out, allowing the conducting CNTs to be carefully burned out at a later point in the production cycle.

One important note about DEP is the fact that it is roll to roll compatible. Electric fields may be applied via a roller, allowing alignment as a part of the roll to roll production cycle. This is critical to future development, as there are very few high yield production methods for CNT FETs.

SUBSTRATE SURFACE TREATMENTS

In the course of printing the various materials used for the new CNT ink development, a new methodology for improving the print resolution of various devices was found. Specifically, by coating the print area in a solvent of the opposite polarity and then evaporating it prior to printing the new material, print resolution and smoothness was greatly increased. This is due to the neutralization of surface charges which would normally cause the ink to spread across the substrate. While substrate coating is not a new technique [71], it is usually accomplished via some sort of cured polymer as opposed to a simple wash.

To demonstrate these effects, samples were prepared with Novacentrix JS-B40G silver nanoparticle ink printed on each. This ink is an aqueous ink, so the substrate was coated with Xylene which was then evaporated off. The resulting prints are shown in Figure 3.13. Prior to developing this methodology, the closest parallel lines that could be maintained without reflow causing shorts was 125-150 microns. Using the new method, lines as close as 50-80 microns could be obtained. This allowed for the design of a transistor test fixture which was compatible with both 250 and 500 micron pitch GSG probes, which increases the maximum testable frequency of the device.

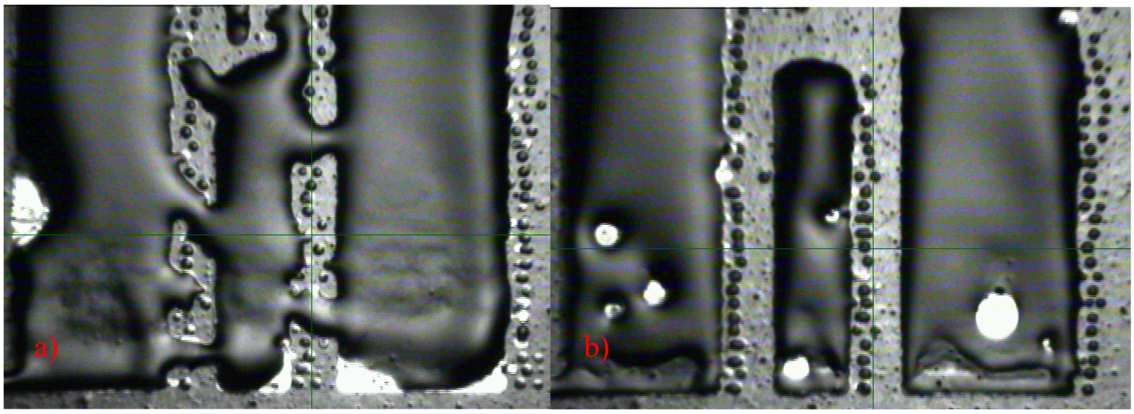

Figure 3.13: a) Novacentrix ink on uncoated Kapton, b) Novacentrix ink on Kapton that has been treated with xylene. Note the smoother surface of the xylene treated sample.

The effect is even more dramatic with the new CNT ink solution. Given the non-aqueous nature of the ink, isopropyl alcohol (IPA) was used as the surface coating which was evaporated off prior to the print. Figure 3.14a shows a print without the coating while Figure 3.14b shows a print with the coating. Of particular note is the much greater concentration of solvent on the substrate. Both contain the same volume, but keeps the solution, and thus the CNTs, concentrated in a much smaller space.

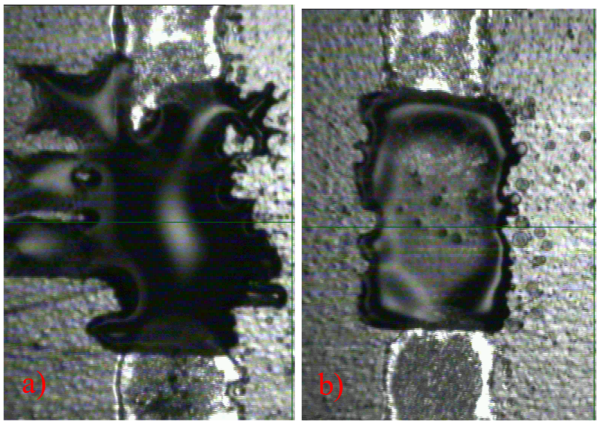

Figure 3.14: a) CNT on uncoated substrate, and b) CNT on IPA coated substrate. Note that the coated sample shows much better control in terms of shape and concentration.

Note that this method is fully roll to roll compatible. By simply running the substrate through a tank similar to what is used in flexographic print systems, the substrate could be coated in the solvent of choice. Given the low boiling point of IPA and Xylene, it could then be evaporated off using a simple heated air gun prior to printing. A diagram of such a system is shown in Figure 3.15.

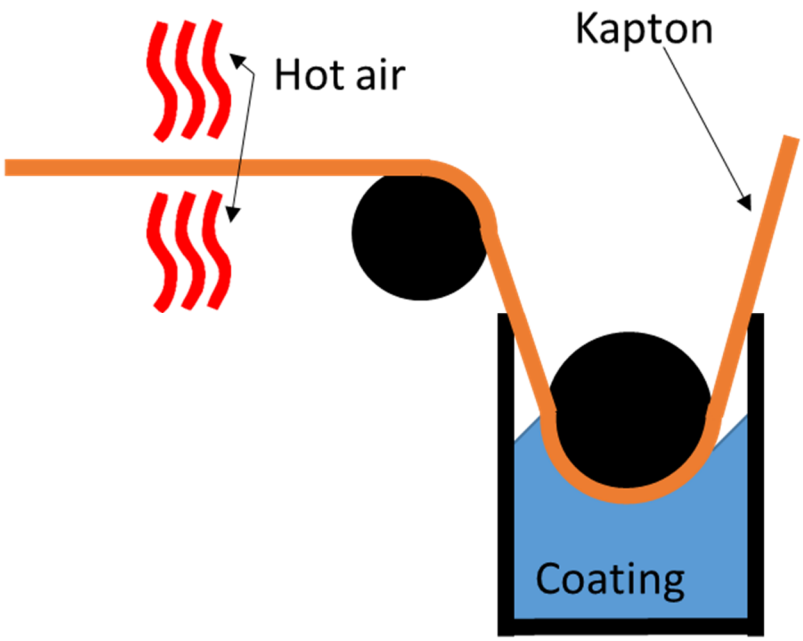

Figure 3.15: Example setup to allow roll to roll substrate coating. The coating could be Xylene, IPA, or some other surface energy neutralizer. Note that additional rollers could be added to flip the substrate if needed.

Chapter 4: High Frequency CNT Transistors [3]

One of the key successes of the research efforts described in this dissertation was the development of a high speed 100% printed CNT Transistor. As a part of the materials development described in the previous chapter, a technique was created which allows for the printing of sub-micron non-conductive gaps between silver electrodes. Using this, it is possible to produce a CNT transistor capable of operating at up to 18.2 GHz.

DEVICE STRUCTURE

The entire fabrication process was completed using a Fujifilm Dimatix DMP-2831[25] printer for deposition. Individual printed material layers were thermally cured in an oven.

The general device structure is shown in Figure 4.1, with 1a showing the device layout and 1b showing the cross section of the transistor. A top gate structure was used in order to protect the SWCNT thin film and provide repeatable printability[42]. Without a protective top layer, the SWCNT thin film can dissolve on contact with environmental contaminants and liquids.

[3]Sections of this chapter are pulled from [1]. Peter Mack Grubb was responsible for all fabrication and electronics printing presented in this publication. Additionally, all device designs originated from Peter Mack Grubb. Most importantly, the sub-micron gapping technique were discovered, tested, and implemented solely by Mr. Grubb.

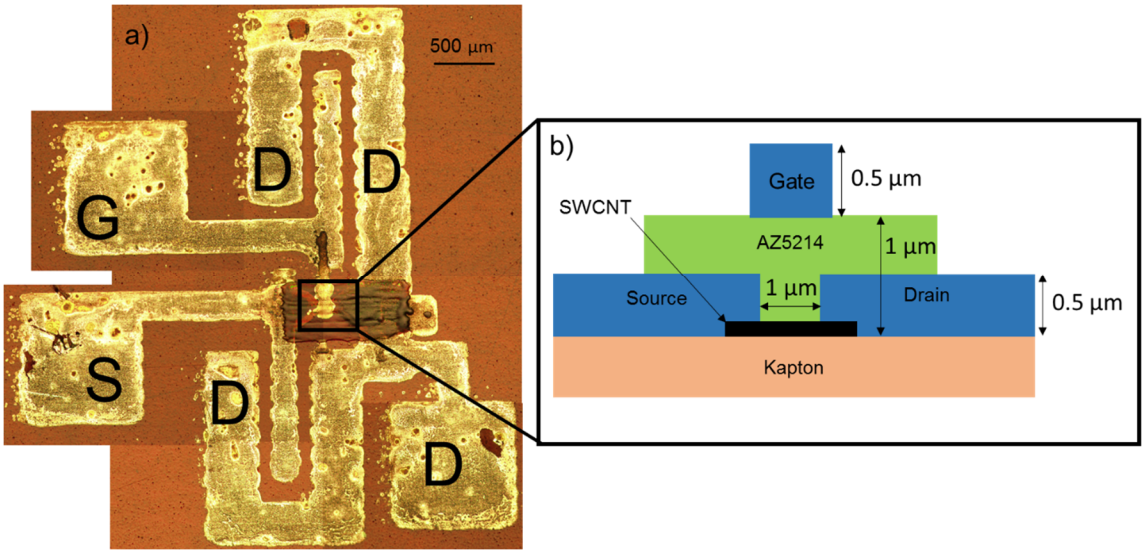

Figure 4.1: a) A composite image of one of the devices produced. The odd structure is designed to allow testing used GSG probes for high frequency testing, while the more conventional pads were used for DC testing. G = Ground, D = Drain, and S = Source. b) A dimensioned cut away of the device structure.

The substrate used was 500HN Kapton. This substrate provides a very high temperature tolerance ranging from –269°C to 400°C[72], allowing for a wide range of compatible inks, while retaining high flexibility. Additionally, these properties make it an ideal substrate for use in aerospace and military applications.

First, SWCNT thin film structures were formed on the substrate using the techniques outlined in subsequent sections. Once the thin film was formed, the source and drain were printed on top, with one terminal using silver nanoparticle ink from Novacentrix Inc (JS-B40G) and the other using non-aqueous silver nanoparticle ink from UTDots Inc (UTDAg40IJ). The opposite polarities of inks cause the generation of a narrow, non-diminishing gap with a finite length. This process is discussed later in this paper. Silver was printed on top of the SWCNT thin film in order to maximize the contact surface area between the SWCNT network and the silver transmission lines. The source and drain were then cured at 200 degrees Celsius. Once this step was completed, a dielectric material

(AZ5214 photoresist from MicroChemicals) was printed over the source, drain, and gap[51]. Finally, a gate was printed on top of the structure using the JS-B40G silver nanoparticle ink from Novacentrix.

The capacitance per unit area for the dielectric material was experimentally determined. Printing usually forms layers of very consistent heights, due to its high degree of control over the quantity of ink deposited in each layer. To find the value for C_{diel}, a simple 100 μm x 100 μm silver patch was printed on top of a 1-micron thick layer of AZ5214. The capacitance across this structure was then measured allowing us to calculate C_{diel} to be ~9.3 nF/m^2. The relatively low capacitance is achieved due to the relatively thick gate dielectric and lower dielectric constant of AZ5214.

SWCNT THIN FILM PRINTING

In the device outlined above the semiconductor consists of a network of single walled carbon nanotubes. Recent efforts for printed transistors have focused on the usage of semiconducting CNTs due to their exceptionally high mobilities[15], [17]. While other printable semiconductors have been used, none have shown the potential for the multiple GHz performance that CNTs have. While other bioFET devices have shown outstanding properties in terms of subthreshold swing and low gate voltage[73], these devices have so far been unable to break into the GHz switching realm, whereas CNT devices have.

Typically, clean room processed SWCNT based transistors use some form of aligned SWCNTs[16]. This provides optimal performance while using the fewest number of CNTs. However, in recent years, the cost of CNTs has dropped to a point that using the minimal number is not necessarily a major concern from a cost standpoint[41]. While aligned thin films do provide significantly better performance[74], [75], unaligned thin

films are much easier to produce. Thus, efforts to ink jet print CNTs have largely focused on unaligned CNT networks [17], [42], [43].

Past efforts to print these CNTs have largely been done using aerosol printer. This process has met with solid results [4], [17], [76], but is not as flexible in terms of applications as ink deposition. Previously, our group formulated a mixture of CHP and SWCNTs which allowed the SWCNTs to be printed using a deposition printer [15]. CHP is ideal from a printing aspect for this application, as it has both a relatively low boiling point of 154°C that is stable at room temperature, and a viscosity well suited to use in the Dimatix printing system[43]. However, while the CHP provides good print performance, subsequent layers must deal with the extreme hydrophobicity of the CNTs themselves. This means that the first layer of solution printed must be the only layer, as the CHP will be pushed away from the print site by the CNTs. To avoid this, the CNT solution described in chapter 3 was developed. CNTs were dispersed via sonication in this proprietary solution at a 20% concentration by weight, leading to a solution like the one shown in Figure 4.2a. This allowed for CNT printing without dealing with the aqueous/non-aqueous interactions of the CHP and CNTs.

Once the solution is deposited on the substrate, the proprietary solution is annealed away via thermal annealing. Figure 4.2b shows an SEM image of a multilayer CNT thin film after the annealing step. The final resistance of the CNT thin film was 200 kΩ, which was in line with past papers using aerosol printing [17]

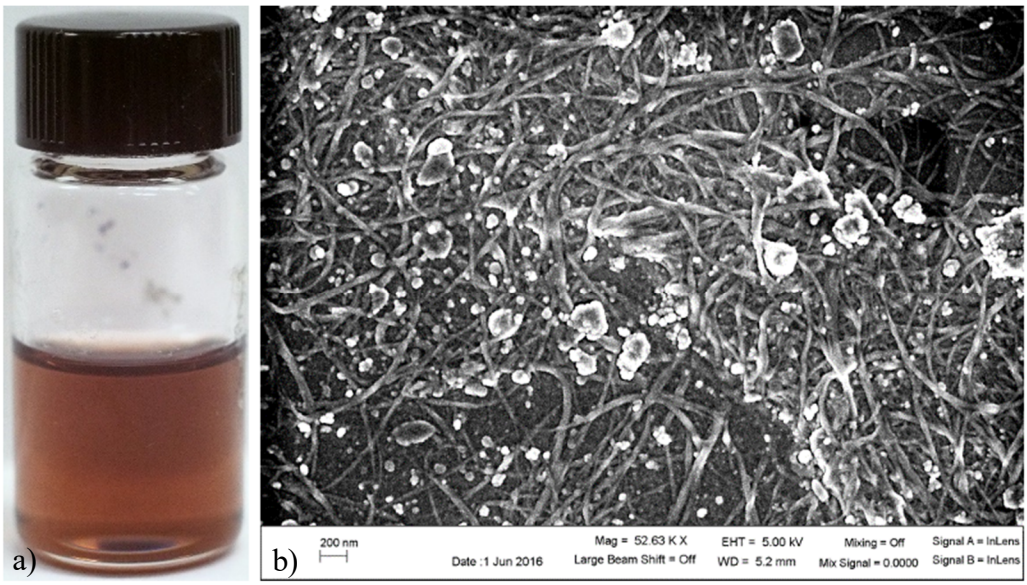

Figure 4.2: a) The CNT solution to be printed for the semiconducting layer. b) An SEM image of the cured CNT solution at 52630X magnification.

CHEMICAL GAPPING PROCESS

One of the primary challenges in fabricating a transistor via any printing methodology is the achievable minimum channel length. Traditionally, inkjet printed electronics achieves this gap between the source and drain by merely not printing a space in a transmission line. In theory this yields a gap where the width is limited by the resolution of the printer. Given that a printer like the Dimatix has a resolution of 10-30 µm depending on drop volume[25], this provides a small gap, but by no means a short channel compared to photolithographic methods in a CMOS foundry[13], [14].

In practice, this gap often has to be much larger. Not only does print position have fairly significant error bars, but this issue is further exacerbated by affinity of inks employed. Thus, if the source and drain are printed using the same ink, and the chemical force is greater than the surface energy of the substrate, the ink will pull across the source and drain, causing closure of the gap and creating a short circuit.

The concept of using surface effects to control gap size is not inherently new[71], [77], [78]. However, past efforts have focused on the usage of some sort of self-aligning monolayer. This potentially places major restrictions on both materials and substrates that could be used. Additionally, the technique has not been ported to a roll to roll technique, limiting its potential for mass production. In order to combat these disadvantages, the technique outlined below focuses instead on creating the chemical effect with multiple wet layers. This allows for the selection of any two inks with opposite chemical properties. For the specific device produced here, conductive silver inks with opposing chemistries were selected due to their easy commercial availability. Both inks form silver thin films when cured. However, one is a hydrophobic, non-aqueous hydrocarbon silver nano-particle solution while the other is a hydrophilic, aqueous silver nanoparticle solution. What this means is that the two inks cannot mix, similar to the way water and oil will separate when poured in the same glass.

By printing the two inks in a single layer side by side, the chemical force would produce the gap as shown in Figure 4.3a. In the printing process, the two ink sections were printed right next to each other with no gap from the printing process. However, the chemical forces between the two inks introduce a micron to sub-micron order gap.

One major advantage of this method over previously listed short channel methods is its flexibility and tunability. In our experiments, Kapton was used with two off-the-shelf inks. However, by using custom formulated silver inks, various solvent combinations could be used to introduce gaps with a specific length. Gap size would theoretically be controlled by the net polarity difference between the chosen solvents. This also allows the technique to be adapted to other substrates that have surface coatings that might affect the polarity of the substrate, and thus the interactions of the inks with it. As far as substrate limitations go, the primary issue would relate to surface roughness. At a certain surface roughness the

ability of the inks to move apart might become impeded. However, this effect was not observed on Kapton, Glass or PET, which covers three of the most common substrates used in printed electronics.

Additionally, unlike most other short channel methods that have been developed for these types of devices, this technique is fully roll to roll compatible, and relies on the usage of inkjet deposition as opposed to gravure[79] or offset methodologies[80, p.]. Inkjet technology does not require the use of any kind of stencil or mask to produce devices, allowing designs to be changed at essentially no cost. This is in essence one of the core promises of inkjet deposition technology, which this technique does not interfere with in any way.

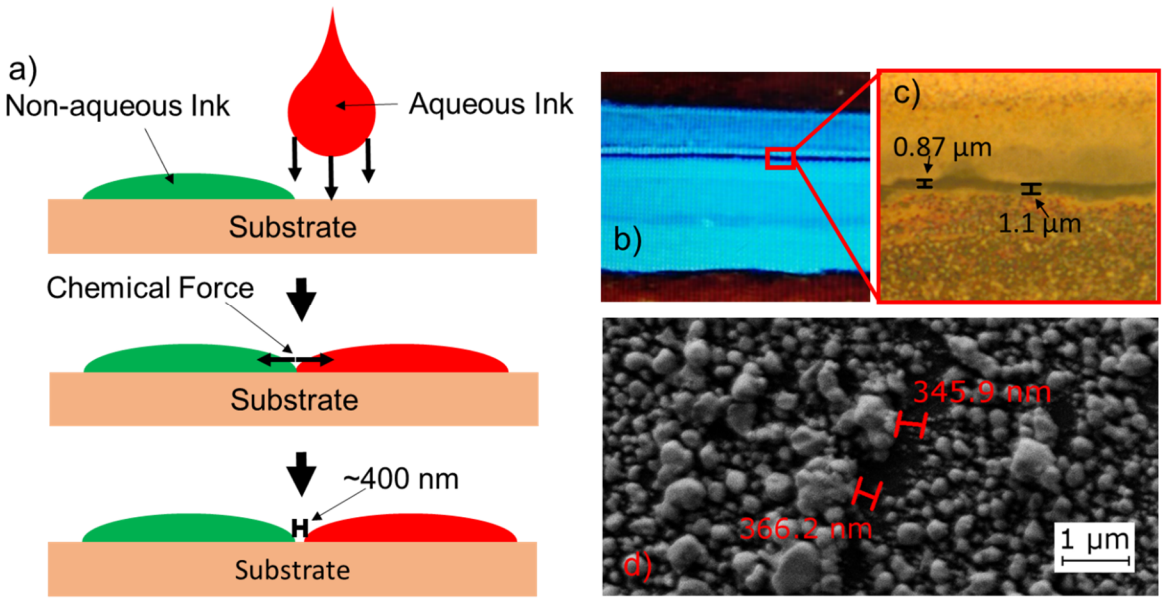

Figure 4.3: a) A diagram of the chemical gapping process. b) An image of one of the printed chemical gaps. c) A measurement of an average gap using an optical microscope. d) An SEM image of the smallest recorded non-conductive gap.

Additionally, this method has the added benefit of being highly reliable. Rather than relying on a mechanical process, this methodology relies on a chemical process which should be consistent as long as the formulation of the inks does not change. Thus, it is possible to print this gap much smaller without having conduction between the two sides of the gap while still maintaining print reliability.

AVERAGE GAP SIZING

In order to characterize the performance of the gapping technique outlined previously, a series of 50 gaps was fabricated using the Dimatix printer in conjunction with the two different inks. Each gap was 1mm long, with a single layer of ink 150-300 microns wide on each side, as shown in Figure 4.3b. The resulting gaps were imaged using an optical microscope and a Zeiss Scanning Electron Microscope to find accurate measurements for each gap. Of the 50 gaps fabricated in this example only a single device was shorted. To further characterize the yield rate, during one transistor fabrication run, 216 gaps were fabricated, of which 10 were shorted. Based on these experiments, this particular combination of inks and substrate has a yield rate greater than 95%. However, it is worth noting that with custom ink tuning without proprietary solvents, a greater yield rate could be achieved.

Across all the optical measurements, a range of 0.5-2 micrometers was observed in gap size, with an average gap size of 1.1 microns and a standard deviation of 0.437 microns. Figure 4.3c shows an optical image of one of these gaps with observed measurements. It is worth noting that the Dimatix printer did have some alignment issues which contributed to the larger gap sizes when printing many simultaneous gaps for developing this average. With a more precise multi-layer printer with better interlayer alignment, more consistent gap sizing could be achieved.

In addition to the repeatability study, a separate set of fabrication was done to determine the minimum gap length that could be achieved using this particular combination of inks. As shown in Figure 4.3d, gap sizes as small as 300 nm were observed using the Zeiss SEM. This was verified via capacitance measurements to ensure that the conduction was occurring all the way out to the edge of the silver deposition.

TRANSISTOR PERFORMANCE

Two different tests were performed on the transistor to determine its capabilities. The first was a simple DC analysis which was completed using an Agilent B1500A transistor analyzer. This analyzer was used to perform both a V_{gs} sweep and a V_{ds} sweep in order to obtain an I_d vs V_g and I_d vs V_d plots. The resulting plots are shown in Figures 4.4a-b and 4.4c-d, respectively. Of particular interest is the on-off ratio, which was found to be on the order of 10^6. This is compared to previous efforts using unaligned printed SWCNT thin films, which achieve 10^2 [14], [17], [76].

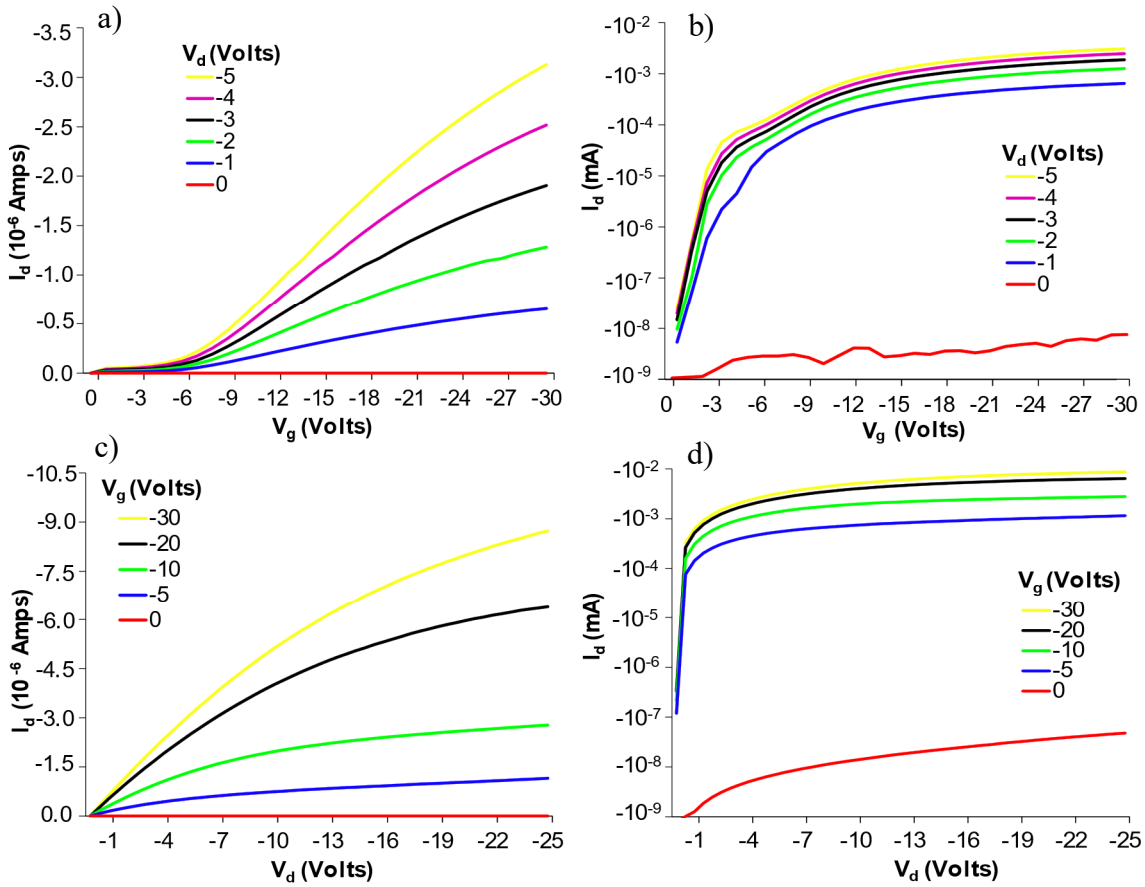

Figure 4.4: DC Test results for the small gap device. a) and b) are Id-Vg plots, with b) using a logarithmic scale for Id to show the on/off ratio. c) and d) are Id-Vd plots, with d) also using a log scale for the same reasons.

Based on the transfer characteristics shown above, the threshold voltage and mobility were calculated. By examining Figure 4.4b, the threshold voltage is found to vary somewhat with V_d as is common for most FET devices. At V_d = -1 V, the threshold voltage is approximately -7 volts, varying up to -11 volts at V_d = -5 V. These relatively high threshold voltages are a product of the acrylate dielectric used to produce these devices. Using an ion gel[4] or hybrid[50] dielectric would potentially decrease this number considerably. Mobility is found using the peak transconductance $G_m = \mu C_{gc} \frac{W}{L} V_{DS}$, where C_{gc} is the gate capacitance. As stated previously, the capacitance of the gate dielectric is

9.3 nF/m^2. Using an optical microscope, the channel area was found to be approximately 10 square microns with dimensions of L = 0.8 microns and W = 12.5 microns, yielding a C_{gc} of 0.093 pF. Using the peak transconductance from V_{DS} = -2V in the linear region, it was found that the effective mobility of the device was approximately 6 cm^2/(V s), well in line with other CNT devices with similar on-off ratios[81].

The second test was to determine the maximum switching frequency of the device. Given that past efforts by the group yielded devices operating up to 5 GHz [17], new techniques were needed to determine the max frequency which should theoretically be higher due to the much shorter channel length. To measure a transistor's maximum frequency via RF tools, the parameter of interest becomes H_{21}, or the small signal gain of the transistor[82], [83]. When the small signal gain is 0, the transistor has reached maximum operating frequency. The H parameter may be derived using the S parameters measured by a network analyzer and the equation $H_{21} = -\frac{S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}}$, where port 1 is the gate and port 2 is the source. S_{11} is then defined as the gate return loss, S_{22} the source return loss, and S_{12} and S_{21} are the power transmitted from the gate to the source and source to the gate respectively. This allows the use of RF equipment that will usually be capable of 5+ GHz measurements, rather than lower speed traditional transistor measurement equipment.

The transistor pictured earlier in Figure 4.1 was measured using this methodology, with the drain tied to the ground plane on a pair of GSG probes and the source and gate serving as the signal lines. The measured transit frequency for the extrinsic device as whole yielded the parameter $f_{t,ext}$. Typically, f_t is significantly larger than $f_{t,ext}$ due to parasitic capacitance and resistive effects. Thus, an experimental dembedded value which actually derives f_t is required. This is accomplished via standard two step dembedding to derive the performance curve for the actual device independent of these parasitic effects[84], [85].

This method essentially consists of measuring the extrinsic device response and then an open and short test structure on the same substrate. With this data, the intrinsic f_t is derived, yielding a de-embedded value for the transistor performance. The intrinsic data set is shown in Figure 4.5. The extrapolated line showed that the transistor was capable of operating at up to 18.21 GHz (at the point when $h_{21} = 0$).

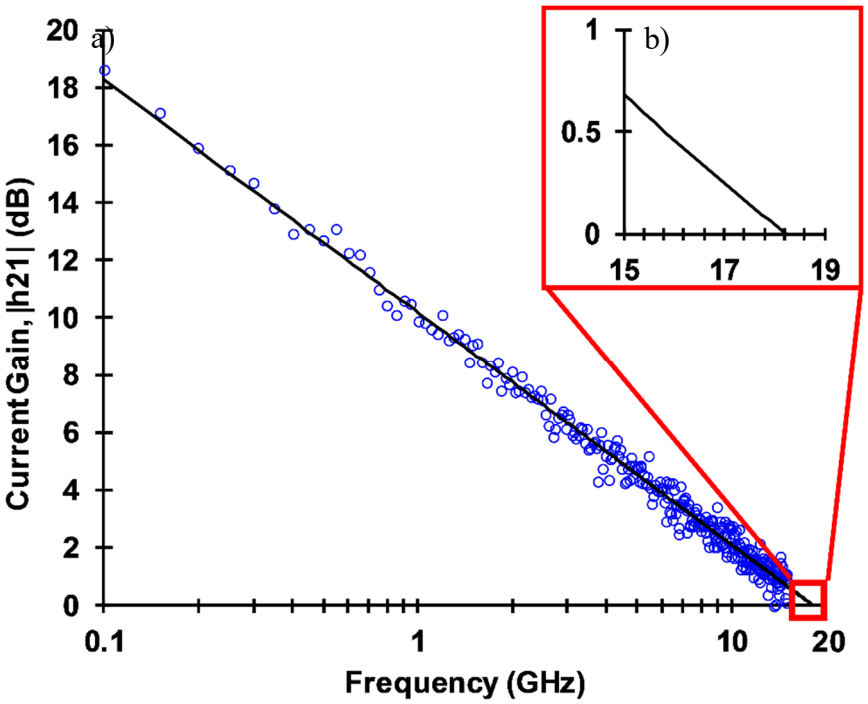

Figure 4.5: The high frequency test results for the device. Note that the signal becomes quite noisy at higher frequencies. The trend line breaks through this somewhat to give us the final value of 18.21 GHz.

To ensure that experimental de-embedded values are reasonable, an analytical estimate needed to be made for the device. For intrinsic results, $f_t = g_m/2\pi C_{gc}$ where g_m is intrinsic transconductance and C_{gc} is the gate capacitance. C_{gc} was calculated above to be 0.093 pF. The parameter g_m can be extracted from the extrinsic transconductance G_m (which is found using the DC curves for the device) via the equation $g_m =$

$\frac{G_m}{1-G_m[R_S+(R_S+R_D)/(G_m/G_{ds})]}$, where G_{ds} is the extrinsic device conductance, and R_s and R_d are the source and drain resistances respectively. Using this equation, g_m was found to be 13.3 mS at the drain bias point used for gathering the high frequency data. When this was substituted to the intrinsic predictor, the analytical result of ~22.76 GHz was found. Compared to our actual measured result, these analytical results show that the device was operating as expected.

These results represent some of the best performance seen in any printed electronics device to date. Through the use of high purity CNTs and novel production methodologies, high frequency switching has been demonstrated this creates the possibility for inkjet printed amplifiers and other high frequency RF devices.

Chapter 5: Production Scale Roll to Roll Compatible Transistors[4]

One critical component for producing systems on flexible substrates is an inkjet printed transistor. Past papers have explored using these roll to roll systems in order to print CNT transistors, typically using a gravure system which employs a lithographically defined stamp to produce the pattern[79], [86]. This method loses one of the main advantages of inkjet printing, in that the stamp must be retooled for each design, whereas R2R drop on demand print heads do not have such a limitation. Moreover, even the few efforts which were able to print transistors using inkjet deposition were forced to use thermal curing due to the nature of the CNT inks used[86], [87]. A typical CNT ink is a high weigh percentage of CNTs dispersed in CHP, which requires a 15 minute cure at 210 C. This negates the high speed capability of R2R, and puts the design out of reach for true production scale electronics.

Using the UV curable CNT ink described in Chapter 3 and a proprietary hybrid dielectric, a high speed R2R compatible transistor was designed and fabricated. This represents the first such device which could be produced using full speed R2R methods, rather than requiring long delays for thermal curing steps.

METHODOLOGY

Many papers have been written about designing CNT thin film transistors for drop on demand printing systems. Typically these papers focus on the usage of small scale printers such as the Dimatix DMP-2800. Part of what makes the Dimatix an attractive prototyping platform is the ability to vary the drop spacing from 15 microns up to 100 microns. This variability allows for the usage of a wide variety materials without

[4] Sections from this chapter were originally published in [3]. Peter Mack Grubb designed, printed, and tested all of the devices described in this section.

complicated design parameters. In contrast, the drop spacing for an R2R system is often fixed. For this design, the Konica KM1024MHB printhead was targeted as the R2R system of choice. This print head has a 35 micron drop spacing in the direction perpendicular to the substrate axis of motion, and a 70 micron drop spacing in the direction parallel, with 1024 nozzles on each print head. Thus, feature sizes needed to be multiples of 35 microns in one direction, and multiples of 70 microns in the other.

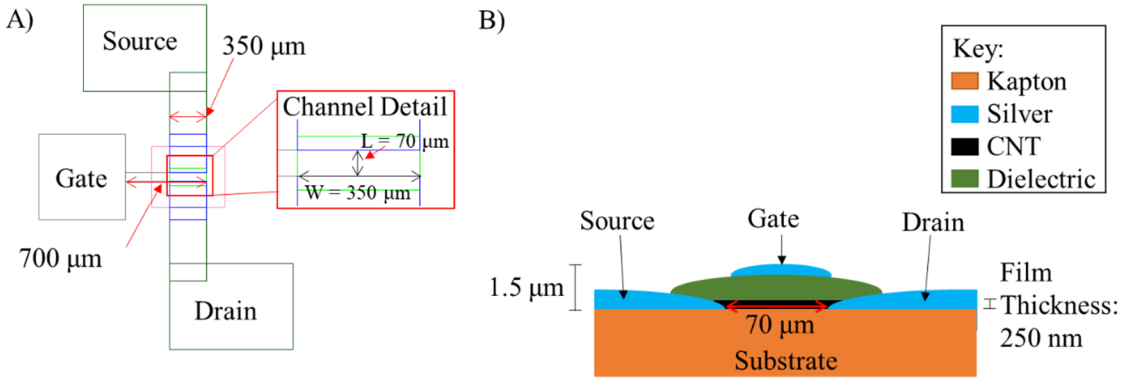

Figure 5.1: A) The layout dimensions are all multiples of 70 microns to allow for easy R2R printing. B) Layers are depicted as sloped surfaces to more accurately reflect the typical shape of a printed material.

With the minimum feature sizes defined, the layout shown in Figure 5.1A was defined. Based on this layout, both top gate and bottom gate structures were tested. Due to the domed nature of the printed dielectric, it was not possible to consistently produce a CNT thin film on top of the dielectric material. The CNTs would invariably reflow off the dielectric, aggregating on the edges of the dielectric layer. Due to this issue, the top gate structure shown in Figure 5.1B was used to construct the devices. The greater adhesion between the silver nanoparticle ink and the dielectric allowed the gate to be accurately placed where needed to produce the device.

Each layer was printed and then cured using the Xenon Sinteron-2000. This required careful coordination of materials, so that a subsequently printed layer would not be burned by a higher cure power on the sintering system. Based on these requirements, Novacentrix JS-B40G was selected for the conductive ink when printing the source and drain and a hybrid SU-8/BaTiO3 nanocomposite was selected for the gate insulator. Due to surface effects of the hybrid dielectric, a UTDots silver nanoparticle ink with better adhesion to SU-8 was used to print the gate. The CNT ink described above was used to create the semiconducting channel. The final device is pictured in Figure 5.2A, where each of the inks can be clearly seen. These devices were arrayed in batches with 22 to a cell as shown in Figure 5.2B.

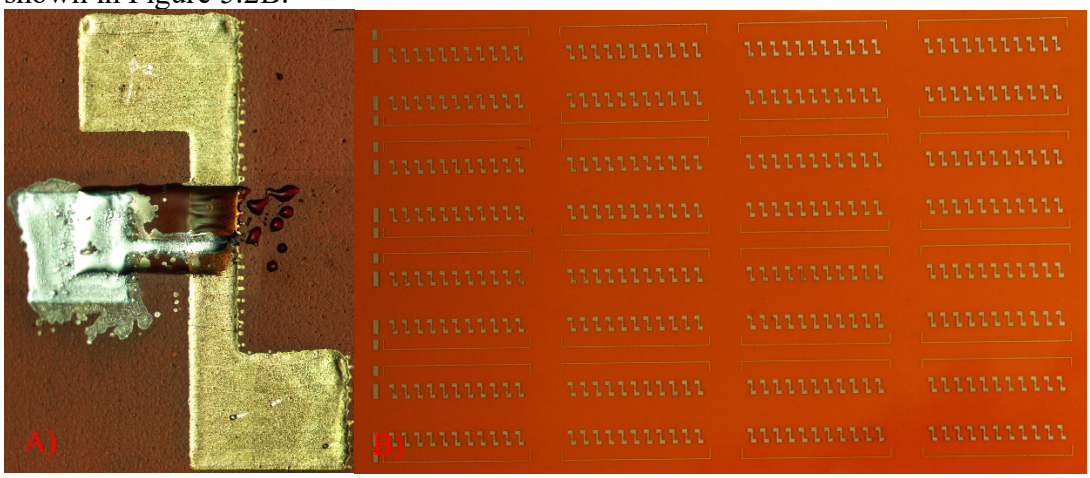

Figure 5.2: A) A composite image of the final device produced. Multiple images were taken and assembled in order to create a higher resolution image. B) An array of transistor devices in production.

RESULTS

The devices were evaluated based on their DC performance. Once produced, the devices were tested using an Agilent B1500A transistor analyzer. Different ranges were tested to find the limits of the thin film transistor before the current melted either the dielectric layer or the substrate. As is typical for printed TFTs, driving voltages for the gate

were quite high due to the relatively thick gate dielectrics required to have contiguous layers without shorts into the CNT semiconducting layer. Of the 352 devices printed for this paper, 142 showed functioning transistor characteristics. However, most of the failures occurred during the dielectric application. Over 90% of the devices had contiguous CNT thin films with resistances on the order of 10 megaohms. Problems with the dielectric layer included both pinholing, and overly thick layers preventing switching. The resulting DC performance curves of a functioning device are shown in Figure 5.3.

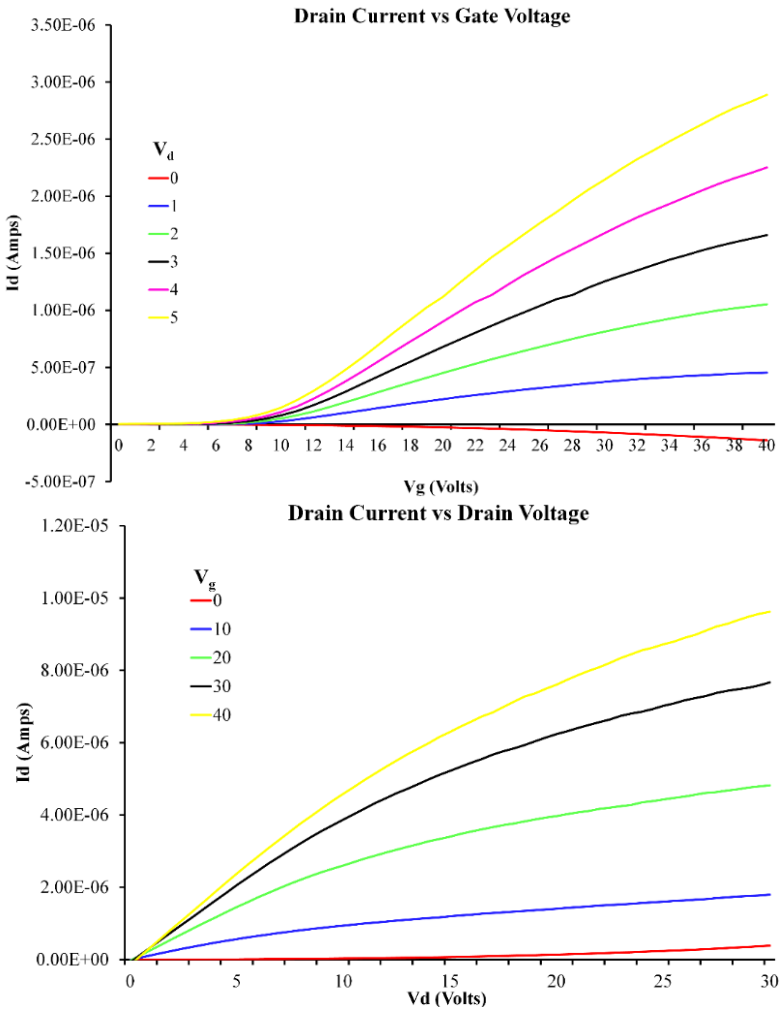

Figure 5.3: The DC performance curves for the R2R compatible transistor design.

In order to better illustrate the On/Off ratio, the subthreshold swing is reproduced using the I_d/V_g plot on a logarithmic scale in Figure 7. The resulting DC curves demonstrate an On/Off ratio of up to 10^4. Additionally, it is worth noting that at 0 volts V_d a small reverse biasing effect was observed at high values for the gate voltage on some devices. This is common in printed TFT devices [76], [88], [89], but was easily overcome even at small source/drain voltage levels. Significant hysteresis was not observed when testing the devices. Hysteresis in printed CNT devices with polymer dielectrics is usually caused by impurities in the deposited CNT thin film or traps formed by voids in the dielectric layer [90]. The wet application of the dielectric over the CNTs minimized the formation of traps at the CNT/dielectric interfaces, and impurities in the deposited film were minimal as shown via the Raman spectroscopy. These properties are all average for a small-scale printed CNT TFT, though they are produced by a device which is compatible with high speed R2R methods.

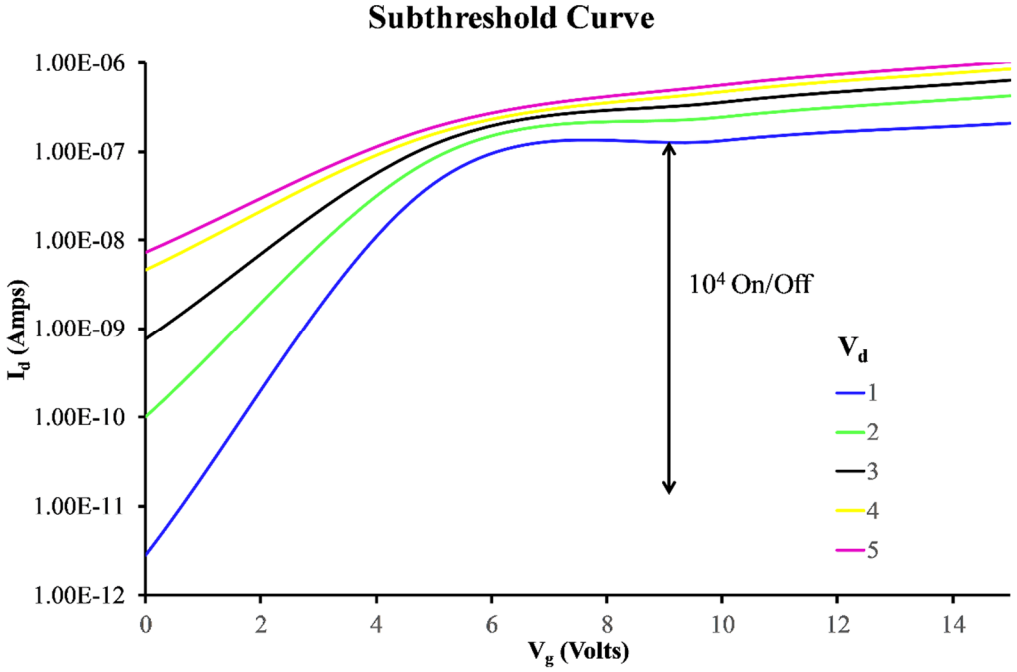

Figure 5.4: The subthreshold curve shows the 10^4 On/Off ratio at V_d = 1 Volt.

DISCUSSION

It is important to consider the context that these transistor devices exist in. The literature is replete with examples of printed high performance transistors ranging from ion gel devices to self-aligned gates [16], [57], [91], [92]. Most of the devices described in these papers have major hurdles relating to potential roll-to-roll applications, usually due to the small minimum feature sizes they require to achieve their significant performance increases. While this device development is important, moving to something that can actually be used in a consumer device requires moving these techniques to production scale technologies such as R2R drop on demand or gravure printing.

The primary area where there has been success in mass producing printed TFTs has been using gravure printing methodologies. The transistor data shown in this paper matches previous On\Off ratios from gravure printing papers[79], [81]. However, it does so without requiring any kind of gravure or stamp to be produced using lithographic means. This means the device can be produced while retaining the high re-configurability inherent to drop on demand systems. The only other reported device that can be produced using high speed gravure printing required the usage of an organic semiconductor due to lacking a UV curable CNT ink[79].

The main advantage of gravure printed devices is the thinner dielectric layers they are able to maintain, and therefore the lower on voltages required to operate the device. For a potential IOT device, this lower on voltage would correspond to significantly lower power usage. This advantage is fundamental to the physics of how the two technologies apply material to the substrate. Future efforts will need to investigate the potential for thinning the gate layer while still maintaining integrity in order to lower the on voltage of the device. These thickness issues along with the yield rates observed in the dielectric application step suggest that the need for improved dielectric materials is significant.

Alternatively, it would be instructive to reformulate the UV curable CNT ink to a gravure printable version. This would allow for a high-speed roll to roll printable device with better performance in low power environments.

The Raman spectroscopy also provides an important data point in terms of the purity of the CNT film that is deposited. While minor shifts are seen throughout the curve, most are not significant enough to show significant variation. The two normalized Raman data sets are over 99.99% correlated, corresponding to a low level of contamination from the solvents used to suspend the CNT ink before applying it to the substrate. By evaporating off all the solvent components, what remains on the substrate is the high purity semiconducting CNT thin film needed for the transistor device. The close correlation between the sample after curing and the reference thickfilm sample shows that the carrier solution does not significantly contaminate the CNT particles. This lack of contamination is critical to preventing the emergence of significant hysteresis in the final device.

Compared to thermal curing, this UV curable CNT ink shows no discernable differences in performance. This was primarily assessed via the performance of the transistor compared to past efforts [76], [88], [89]. Given the Raman spectroscopy results, this was as expected given that most CNT inks aim to minimize impurities in the final thin film. That said, the UV CNT ink does not stay in solution as long as CHP based solutions due to the interactions between the non-polar solvents and the CNTs themselves. This requires sonication or circulation of the ink prior to usage to ensure a uniform solution. Ultimately, no performance impact to the CNTs was measured when using photonic sintering.

Chapter 6: Frequency Scanning Array Antennas[5]

THEORY OF FREQUENCY CONTROLLED PHASED ARRAY ANTENNA

The frequency effects on the beam squint of a phased array antenna are well known and documented in previous literature[93], known primarily as a frequency scanning array. However, there are no examples of building such antennas in a printed electronics type application for which it is uniquely suited. To understand the various effects at play, it is important to first understand the operating principle of a PAA.

PAAs use a network of identical antennas along with a time delay circuit to induce phase differentials between the various antenna patches. This in turn generates a net wave directionality as illustrated in Figure 6.1.

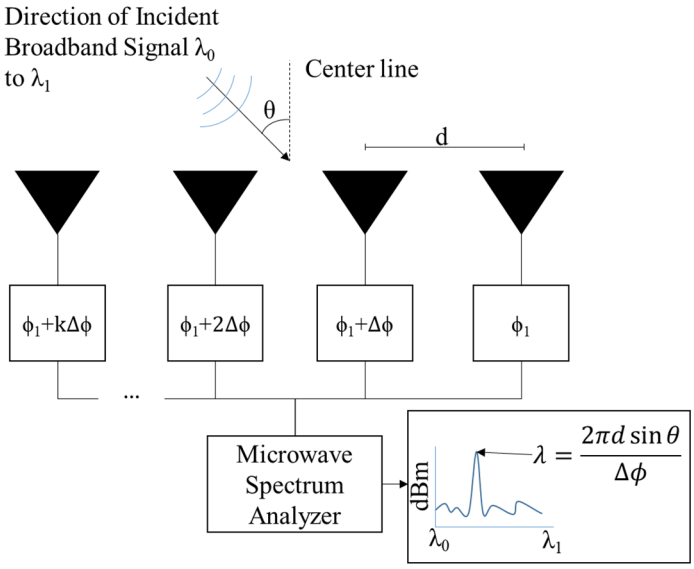

Figure 6.1: Each delay block is some amount n larger than the one before it, with the final delay block being D+kn where k is the number of blocks.

[5] Sections from this chapter were originally published in [2], [5]. Peter Mack Grubb designed the Frequency Scanning Array concept in the context of printed electronics. All simulations, device production, and testing was done by Mr. Grubb. The wideband antenna and power divider were both developed in collaboration with Dr. Li Wentao.

Typically the delay in each block is varied such that the direction of propagation can be controlled. The equation for determining this directionality is derived geometrically from a basic understanding of wave motion, and yields $\Delta\phi = 2\pi\frac{d}{\lambda}sin\,\theta$, where ϕ is the phase shift, d is the distance between the antennas, λ the wavelength and θ the direction of propagation. Most PAA devices achieve shifts in θ by varying ϕ through different delay structures. However, the electrical path of the signal (d/λ) can also be varied with frequency, which in turn is proportional to the phase shift. The usage of metallic delay lines provides a secondary change in ϕ as well. In microstrip transmission lines, phase velocity will vary with frequency [94] which provides a secondary minor source of phase shift as a function of frequency.

These factors are usually negative effects in Phased Array Antenna design, as they cause unwanted variations that are difficult to model. For this design however, these phenomena are exploited in order to create beam steering via the variation of frequency. Such a device is called a Frequency Scanning Array, and is in essence a microwave prism. Due to the lack of switching or other complex elements in the internal antenna structure, such a device is uniquely suited to the limitations inherent in printed electronics devices.

DESIGN VIA SIMULATION

Simulation Setup

Given the complexity of the factors involved in the frequency dependence of the final θ, a simulation was desired to verify the capabilities of the system as a whole. To this end Ansys Electronics Desktop was used to test the individual components and overall system. Of particular interest in the simulations were the reflection coefficient and the far field radiation patterns of the system as a whole.

Unlike some simulations for printed electronics devices, the antenna system was modeled as having a finite thickness. Many simulations use sheet models for the antenna components[95]. However, given the groups previous experience with printed silver[7], [96], [97] the silver depositions were modeled as having a finite thickness of 500nm. This was done to ensure that any extraneous signal phenomena were captured.

This simulation setup was used to gradually work towards an ideal design for frequency shifting. For each component or device, a simulation was run which would capture a full sphere radiation pattern at multiple frequencies. The range of frequencies was selected based upon the S11 performance of the antenna patch being used, yielding a range of interest of 5.0 to 9.0 GHz. For each frequency, the local angles of maximum transmission or "lobes" were extracted and plotted. This yielded steering angle as a function of frequency for the antennas being simulated.

Wide Bandwidth Antenna

The wide bandwidth antenna used in this design is based off an elliptical antenna coming out of a backplane region through a slot, as shown in Figure 6.2. This elliptical design was selected based off of simulated S11 performance. The transitionary curve coming out of the feedline is intended to preserve 50 ohm impedance relative to the input when used on Kapton in a printed application. The continuous ellipses are intended to allow for wideband performance without increasing the complexity of the antenna when it comes to fabrication.

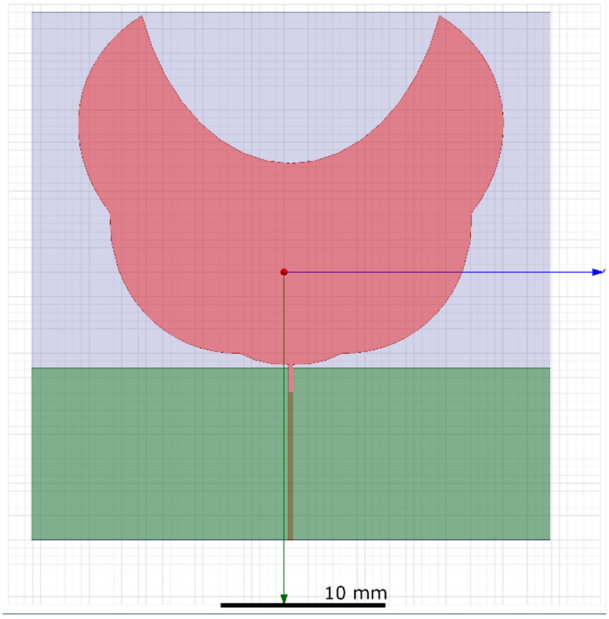

Figure 6.2: The wide bandwidth antenna patch. The green is a silver backplane, and the blue is the simulated Kapton material, while the red is the front antenna element.

This design was developed from other efforts for printed wideband antennas[98]–[101], and then tuned in the Ansys simulation software based on the specific material properties observed in previous efforts by the group at the University of Texas. The resulting design showed good performance from 5.5-9.5 GHz, as shown by the S11 plot in Figure 6.3.

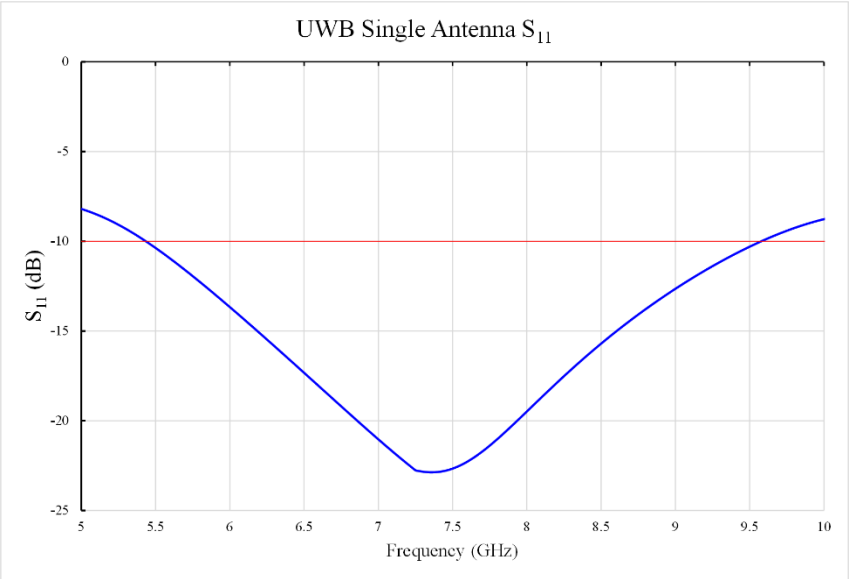

Figure 6.3: The antenna has better than -10 dB S11 performance from 5.5-9.5 GHz.

Power Divider and Fixed Phase Shifter

A power divider was developed to minimize reflection effects and provide a 50 ohm transition into the split. This design runs the signal through a minimally reflecting bend prior to the split, which serves to prevent reflection back to the source and transition the width to something that can be split into two separate 50 ohm lines. Fixed Phase Shifter

The power divider is then connected to a fixed phase shifter. Typically, in a phased array antenna the phase shifter is one of the most critical components, as it is reconfigured to steer the beam. However, in this design the phase shift is fixed. In order to keep fabrication simple, the design is based off of time delay via microstrip delay lines. Essentially, the transmission lines between the various branches of the power divider were extended to create a constant delta L added between each patch. A single cell of this design is shown in Figure 6.4A.

A second phase shifter with a longer path was developed to determine the effect of the constant phase on the frequency steering. Essentially, a delay cell was added to the

original fixed phase shifter, with an appropriate number en route to each patch. A single cell of this design is shown in Figure 6.4B.

While the longer transmission lines cause additional losses and reduce overall antenna performance, it did provide a simple way to quantify the effect of the phase shift differential on the frequency steering factor. Figure 6.5 shows the performance of a 1:4 power splitter using these designs.

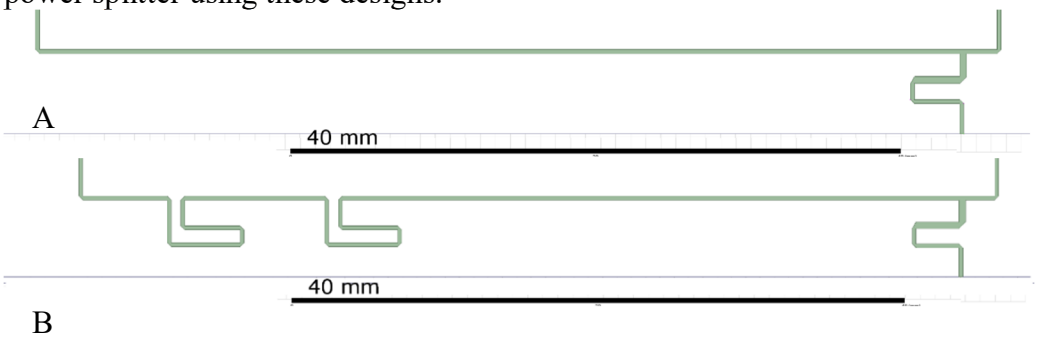

Figure 6.4: The two version of the fixed phase shifter. Lines were kept as straight as possible to minimize loss, with the transitions from the power splitter maintained where possible.

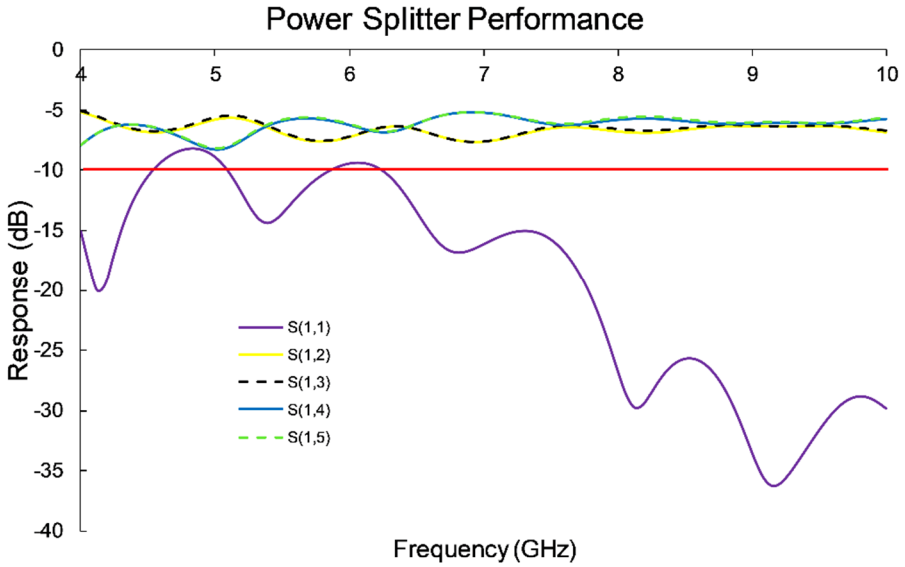

Figure 6.5: S(1,1) performance was consistently below -10dB except at 5 and 6 GHz. Output port performance had some variance which converged at higher frequencies.

System Performance

The various components making up the system were assembled in Ansys into a single contiguous structure and simulated as described earlier. The device structure is shown in Figure 6.6.

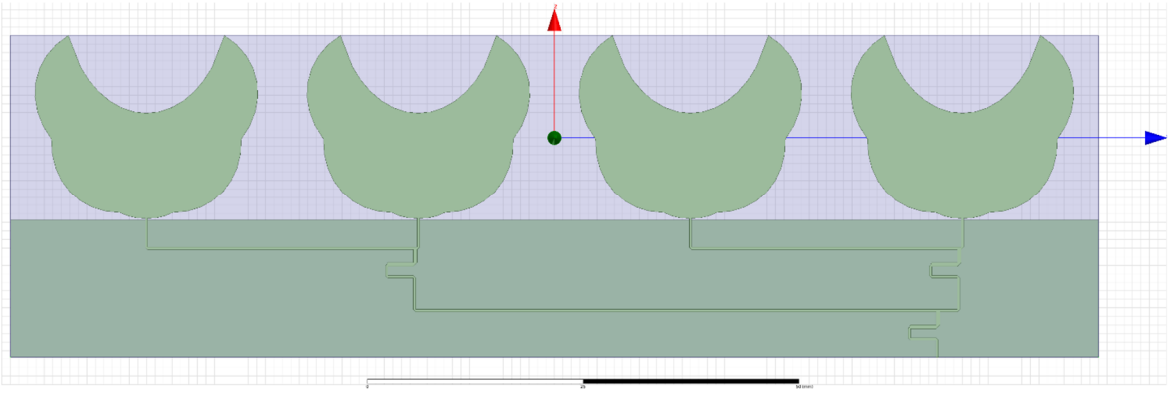

Figure 6.6: The overall system being simulated in Ansys.

The primary parameters of interest for this system are the S11 performance, and the radiation patterns. S11 performance across the best performance range for the antenna patches is shown in Figure 6.7.

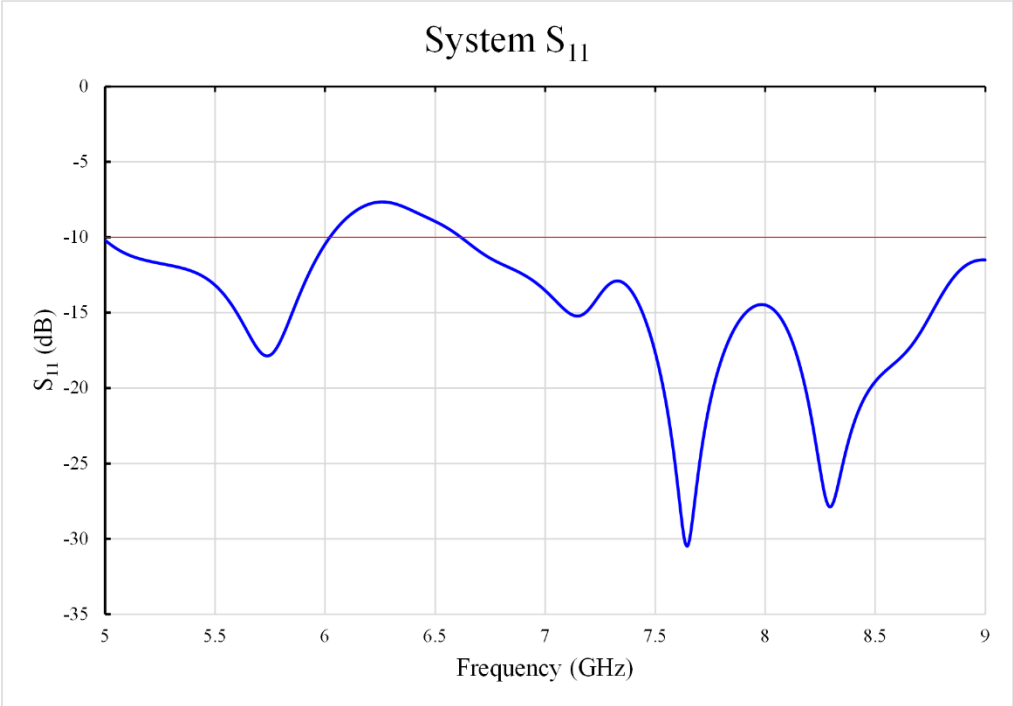

Figure 6.7: Overall system S11 performance.

Compared to the S11 performance of the individual antenna, the PAA network shows less reflectance, but also less consistent performance. This is due to the line losses inherent in having longer transmission line lengths. Due to the physical size of the UWB antennas, the minimum length of the transmission lines was significant. However, on the whole the device showed usable characteristics across the entire range except from 6 – 6.5 GHz.

Radiation Pattern

The radiation pattern was typical for a PAA device, and showed variance as a function of frequency. A typical radiation pattern at 7.5 GHz is shown in Figure 6.8.

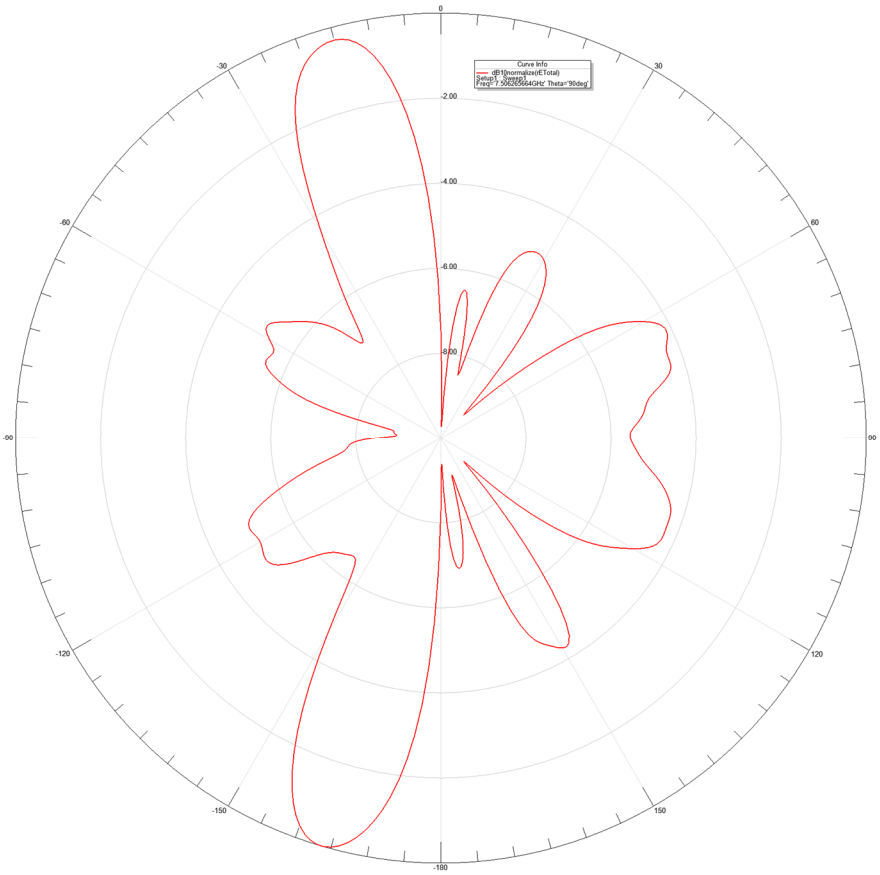

Figure 6.8: A typical radiation pattern for the overall system.

As was expected for such a device, a primary lobe was observed, with side lobes in both the positive and negative directions. Additionally, due to the fact that there is no backplane behind the UWB antenna patches, symmetry between the front and back half of the radiation pattern was also observed.

Frequency Based Beam Steering

For the purposes of defining the beam steering, two pattern features were considered, the primary front lobe between 0 and 30 degrees at 7.5 GHz, and the primary rear lobe between -180 and -150 degrees at 7.5 GHz. These two features at 7.5 GHz and 8.5 GHz are shown in Figure 6.9.

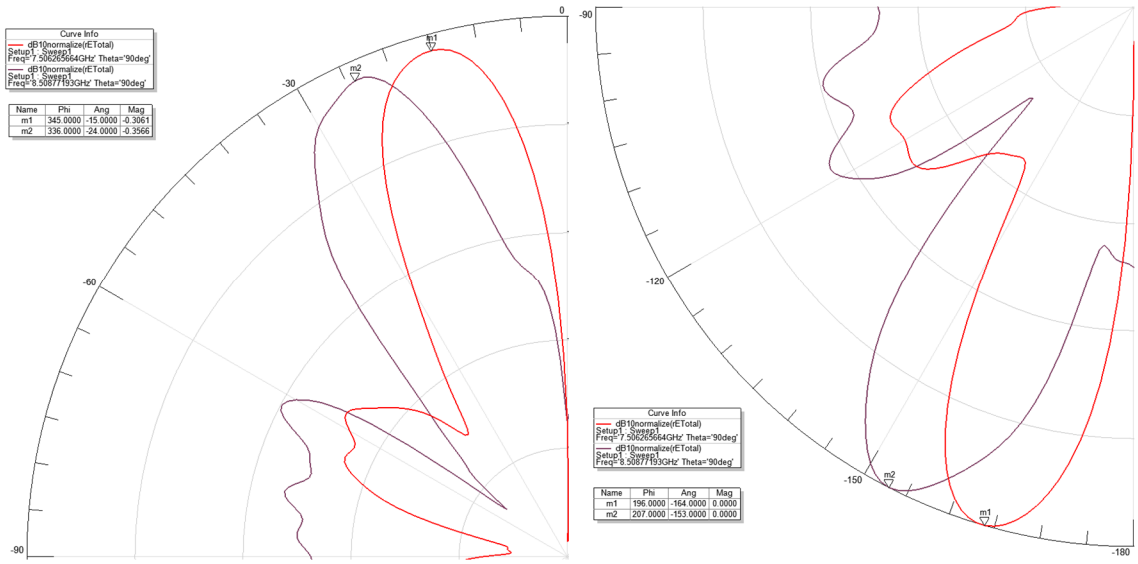

Figure 6.9: On the left, the front left lobe, and on the right the rear left lobe. Both show 11 degrees of variance from 7.5 to 8.5 GHz.

In order to characterize this performance across a range of values, the angle of the maximum at each step of the simulation from 5-9 GHz was considered. Figure 6.10 shows this plot for the front and rear quadrants, along with the trend line.

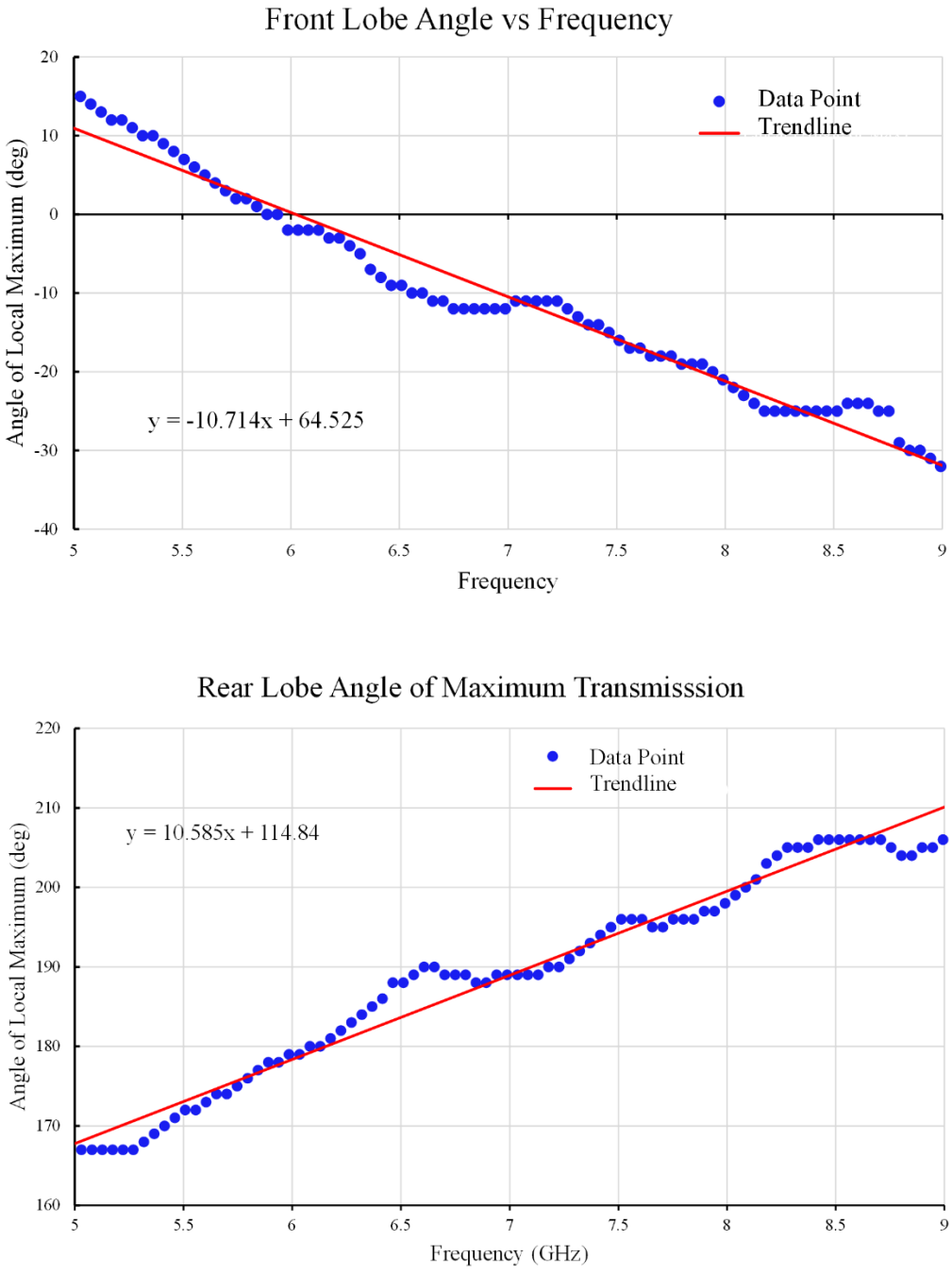

Figure 6.10: Angle of the local maximum as a function of frequency. Note the very small difference in the sloped of the trendlines.

In order to characterize the effects of the phase difference on this phenomenon, the system was also simulated with the longer phase shifter described above. These results are shown in Figure 6.11. Due to the effects of the longer shifter, results below 6 GHz were not consistent enough to be plotted due to a double peak in the region of interest.

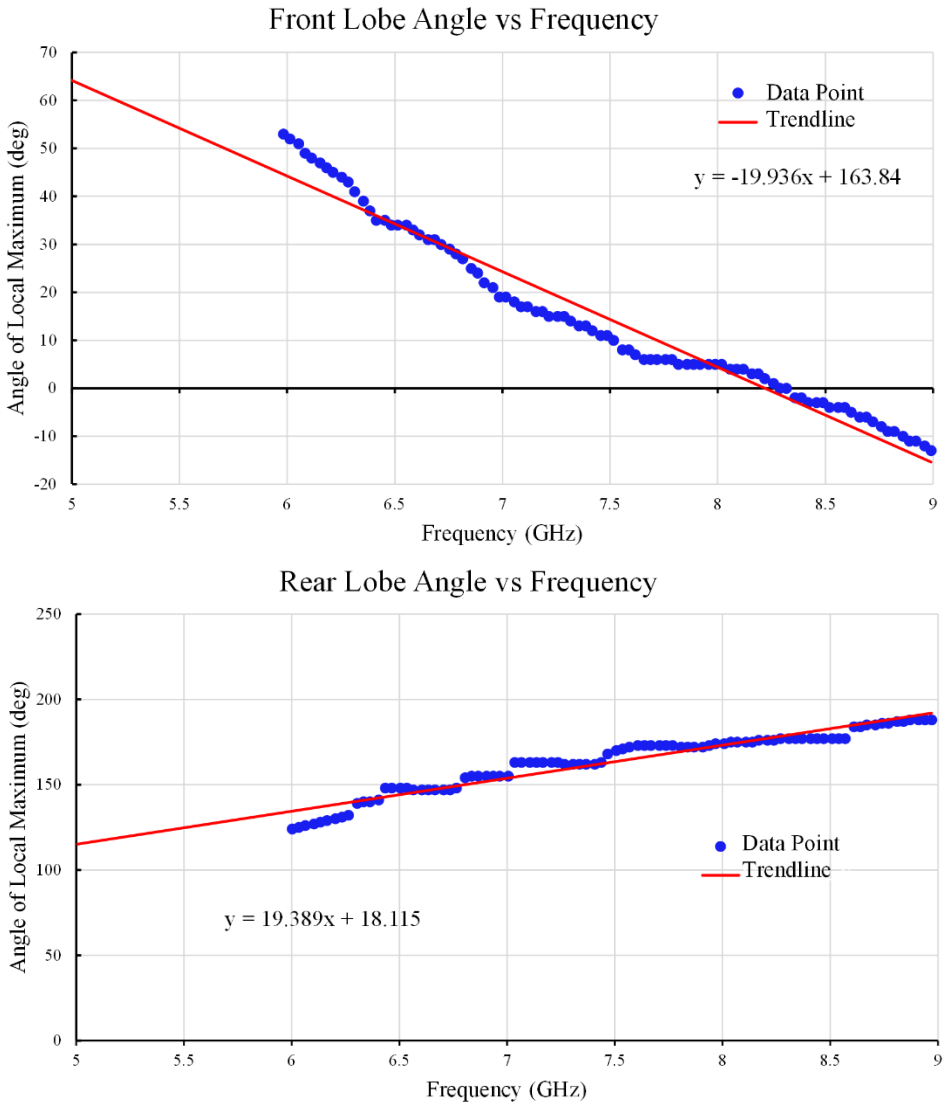

Figure 6.11: Angle of local maximum as a function of frequency for the longer phase shifter. Again, note the similar slopes on the trendline.

From these plots, not only is the beam steering via frequency variation obvious, it is also observable that the steering per unit frequency is a function of the phase difference between the antenna elements. The larger the fixed phase difference, the more rapidly the beam can be steered as the frequency is changed. These conclusions provide the background necessary to design additional devices which exploit these phenomena.

It is worth noting that typically such devices are designed to have 0 degrees or the center at the middle of the frequency range. However, in this case the size of the antenna patches severely limited the potential tunability of the phase shifters in order to achieve the target steering capabilities. Future work will seek to use smaller antenna patches to allow for the creation of a printed array where the center frequency has a 0 degree beam shift.

DEMONSTRATION OF A REAL DEVICE

Printed Device Design

One of the main design challenges regarding building a frequency scanning array on a flexible substrate is the relative thinness of the substrate. Typically substrate thickness is varied to improve properties such as gain or microstrip performance. However, the 5 mil/125 micron Kapton is the thickest option that Dupont currently sells[31]. Additionally, other flexible polymide films have much lower curing temperatures, rendering them incompatible with many silver ink compounds[23]. Consequently, the antenna system must be designed to accommodate the thin substrate being used.

The antenna system consists of three elements: the broadband antenna, the phase shifter network, and the input coupler, an example of which is illustrated in Figure 6.12A. For the input coupler, a simple SMA to microstrip transmission was used to allow for easy connection of various pieces of measurement equipment to the antenna system. The width of the base of the input coupler was determined by the SMA specifications for attaching to

PCBs and similar using off the shelf SMA hardware. To make up for the obvious differences in thickness, epoxy was used to both stabilize and provide a similar dielectric surface. This was then translated into a microstrip transmission line by creating an exponential taper that was mirrored on both the front plane and backplane, providing an impedance matched transition to the microstrip lines throughout the system[102], [103].

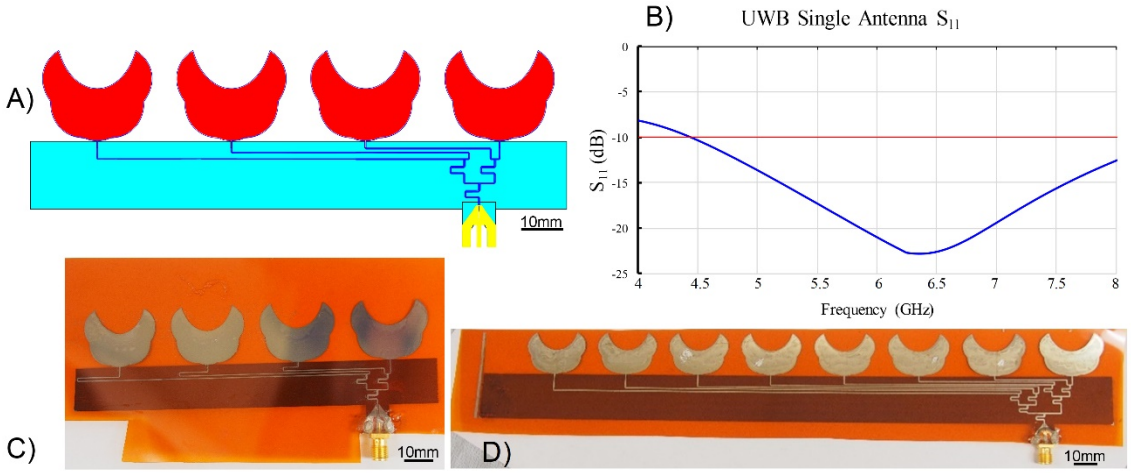

Figure 6.12: A) Red is the antenna patch, dark blue the shifter network, yellow the SMA to microstrip transition, and cyan the backplane. The offset splitters minimize the length of the microstrip lines. B) S11 Performance of a single printed antenna. C) A 1x4 array with an extended phase shifter. D) A 1x8 array with a standard shifter.

The shifter network was more difficult to design, due to the relatively high losses of microstrip lines on thin substrates [104], [105]. A power splitter design was used to maintain 50 Ohm impedance throughout the network, however it was found through simulation that the losses from unbalanced splitters was less than the longer microstrip transition lines [5]. Both the high loss of the microstrip lines and the unbalanced nature of the splitters was previously verified using Ansys simulation software [5].These power splitters, used a gradual increase in width while moving through several corners to prevent sudden changes in impedance. Additionally, the corners were chamfered to control

reflectance within the power splitters. This and the offset provided the fixed phase shifter portion of the system.

The key part of the design which enables the frequency scanning array capability is the broadband antenna patch. Many different broadband antenna patch designs have been demonstrated on printed substrates [99], [106], [107]. For this particular application, a stacked ellipsoid design was selected for its relatively compact size and known performance characteristics [5], [108]. Additionally, this particular antenna could be easily tuned to match the impedance of the shifter network without significant negative effects on the performance of the antenna. The S11 of this antenna is shown in Figure 6.12B.

This design was fabricated in both a 1x4 and a 1x8 element configuration, and with both a shortest path phase shifter network as well as a network with an additional $\Delta\phi$ to increase the steerage per unit frequency. These devices were then tested to obtain far field radiation patterns, as well as performance under flex. Two of the devices fabricated using these methods are shown in Figure 6.12C and D. Both antenna arrays were 22 mm in height, while the 1x4 array was 122 mm in width and the 1x8 array was 250mm in width. With the addition of the shifter and coupler, the total height of system was 45 mm for the 1x4 array and 55 mm for the 1x8 array. The width of the overall system depended on the particular phase shifter network, but was never more than 15mm wider than the array.

Results

Rotational measurements were made using a Microwave Spectrum Analyzer, high frequency signal generator, rotational stage and horn antenna. The FSA being tested was connected to the high frequency generator as a transmitting antenna, while the horn antenna was placed in the far field connected to the microwave spectrum analyser. The frequency of the generator and MSA was then selected, and the rotational stage used to move through

an entire 360 degree rotation recording the various values measured at each degree marker. These results were then collated and plotted.

S11 Results were obtained using an Agilent NS230A Network Analyzer. The antenna was directly connected to the Network analyser output point to minimize system reflectance after calibrating.

Beam steering was demonstrated across multiple devices, with steering per unit frequency varying depending on the number of elements on the array and the length of the phase shifters used. These results are shown in Figure 6.13. Both 1x4 and 1x8 arrays with a shortest path and extended shifter network were tested in order to demonstrate the relationship between the length of the shifter network and the beam steering per unit frequency. Additionally, the two different sizes of arrays were tested to demonstrate the effect of greater elements on the steering phenomenology. Peak directional gain of the 1x4 array was observed at 12 dBi, and the 1x8 array was 15 dBi.

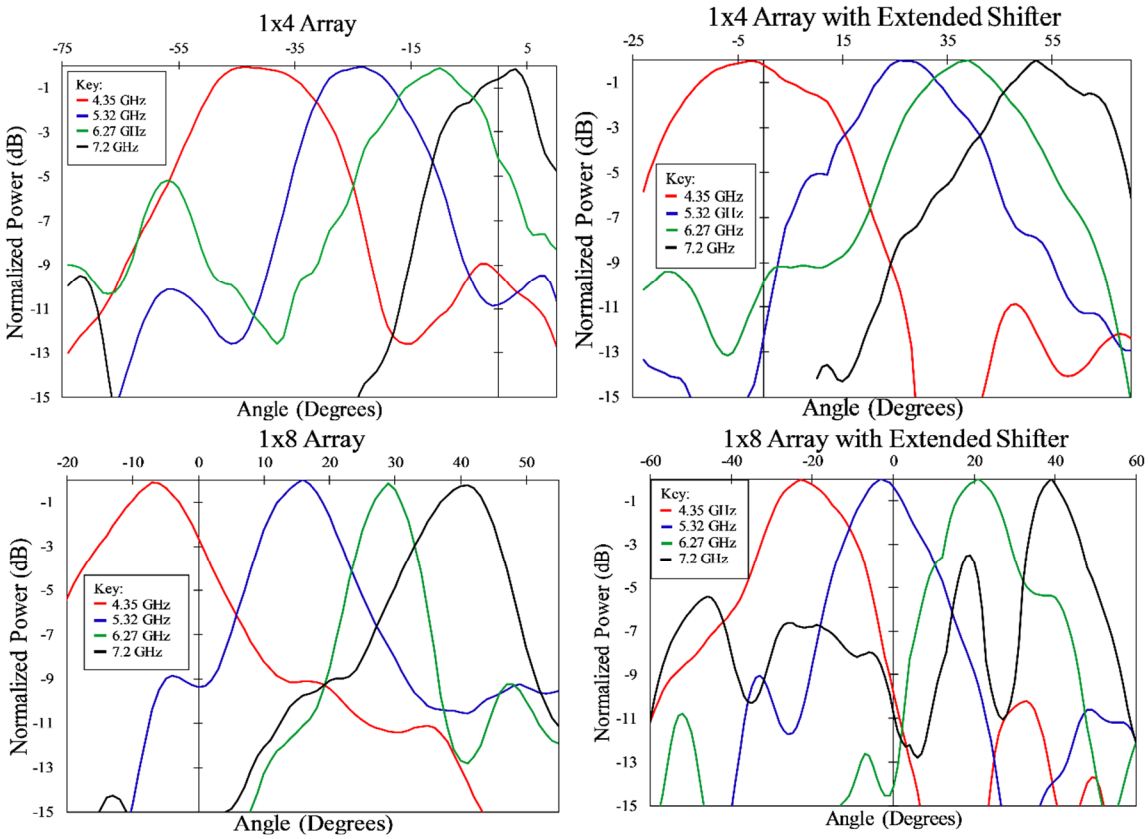

Figure 6.13: Extended shifter networks increase the swing per unit frequency, while the 8 element system exhibits narrower peak power.

It is worth noting that for the physical devices, specific frequencies were tested, whereas for the previous work using simulation was able to do continuous peak capture to show the continuity of the illustrated shifting effect[5]. However, given the limitations of the measurement setup used for evaluating these devices, this was not possible. Consequently, the devices were each tested at a series of key frequencies to demonstrate the beam steering and consistency with the simulated results. Based on the key frequency results and mathematical model of the frequency shifting, it can be concluded that the continuity in steering demonstrated in the simulations is also present in the physical devices.

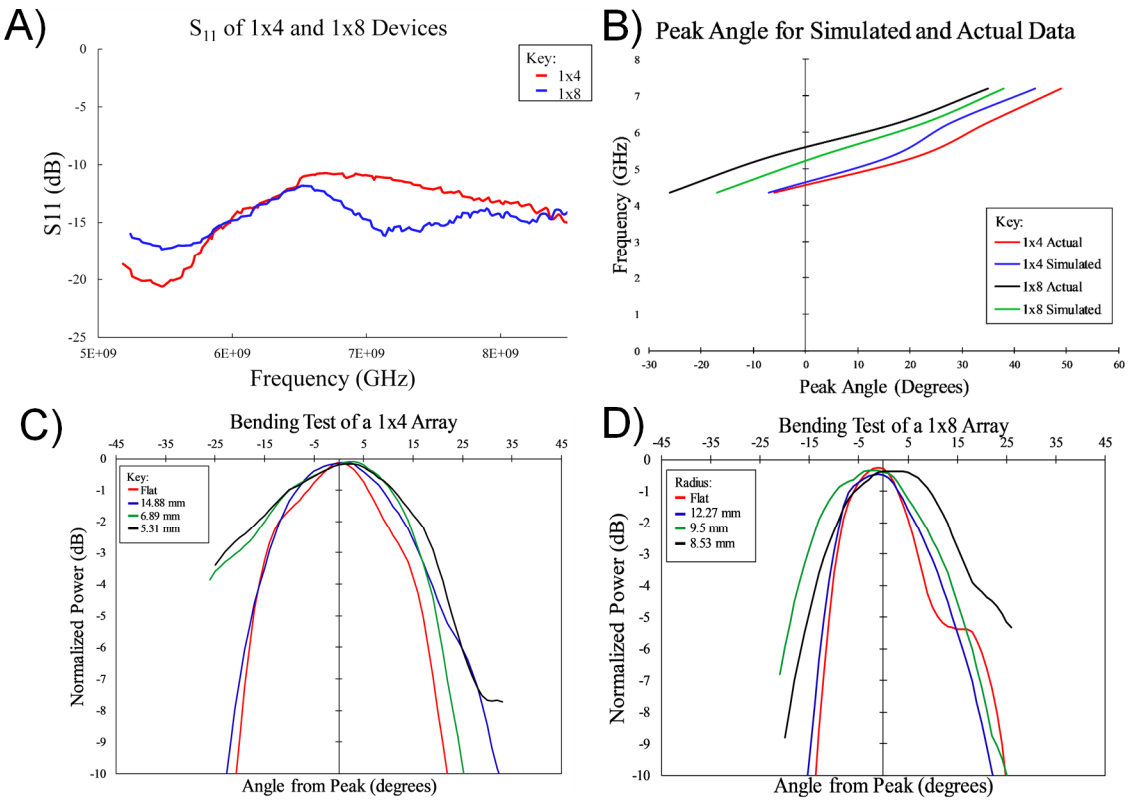

Figure 6.14: A) The S11 of both the 1x4 and 1x8 devices shows less than 10 dB of reflection across the frequencies of interest. B) The 1x4 and 1x8 devices show similar correlation between the actual measured and simulated results. C and D) Both devices exhibited minimal distortion due to bending, but the 1x8 devices were more resilient due to their tighter beam.

S11 results, shown in Figure 6.14A, exhibited less than -10 dB of reflectance across the entire range of interest for both the 1x4 and 1x8 devices. The 1x8 device showed less reflectance from 6.5 to 7.5 GHz, which corresponds to inefficiencies in the longer transmission lines and additional power splitters leading to larger losses. Radiation efficiency at peak transmittivity for the 1x4 devices was observed to be 23%, while the 1x8 devices exhibited similar peak numbers but showed more significant drop off in efficiency as the frequency increased. This caused the development of a much larger side lobe for the

1x8 extended shifter at 7.2 GHz, as the signal strength was lower and the radiation efficiency was also reduced, leading to a much smaller gain relative to the side lobes.

In addition to the rotational measurements, bending tests were also done. Given the potential for flexible electronics devices built using inkjet deposition, it is essential to understand what performance is like under these scenarios. The results of these tests are shown in Figure 6.14 C and D.

Given the minimal loss of performance under bending tests, the Frequency Scanning Array is an ideal type of antenna to be used in situations where both spatial signals and directionality are needed. Many flexible substrate devices exhibit significant losses in performance under bending tests. However, due to the fact that FSA results are assessed from the far field, the bending required to show performance loss is relatively extreme. Combined with the low cost to manufacture, these devices represent an immediate potential application for flexible printed electronics.

DISCUSSION

The first point in interpreting the results is to ensure that they make sense from a physics standpoint. Beyond the equations outlined in this paper, the peak values were compared to previously simulated results [5]. The extended shifters were used for comparison as these are the more interesting devices performance wise, with the results summarized in Figure 6.14B.

Note that both devices show stronger correlation on one end of the range than the other. This is due to differences in the slope or change per unit frequency for the simulated vs actual devices. This difference can be accounted for given the dimensional inaccuracies of the Dimatix system. The simulation is based off the designed dimensions, such as microstrip transmission lines with a width of 285 microns, whereas the actual

results were closer to 310 microns. This can cause significant changes in the S11 performance of several of the components in the system.

There are several different elements in the measured results that warrant further discussion. First and foremost is the basic properties stemming from the steerability as a function of frequency. While this has been demonstrated previously using rigid array antennas [109], these devices have not been built using inkjet deposition technologies. Thus, we must first consider the basic capabilities of the array.

Both the 1x4 and 1x8 arrays exhibit typical array antenna properties and similar levels of gain. The 1x8 arrays have a much narrower -10dB gain angle than the 1x4 devices, which is generally the goal in increasing the number of elements in an array. Changing the number of elements in the array also shifts the center of the angle range encompassed by the 4 different frequencies tested for these antennas. This is product of the shifts in the S11 caused by introducing additional power splitters in the design. Note however that increasing the number of elements does not significantly alter the shift per unit frequency. This implies that higher element count antennas would show similar steering characteristics independent of the element count.

Additionally, increasing the length of the fixed phase shifter path increases the amount of steering exhibited per unit frequency. This is expected based on the equation governing the angle of transmission as a function of frequency. This effect is somewhat independent of the number of elements in the array, as both the 1x4 and 1x8 arrays have a similar total swing in angle. However, while the total swing was similar across frequencies, the distance between the intervening peaks varied. This speaks to the difficulty in designing these types of antenna arrays. The S11 of the patch antenna, power splitter, coupler, and microstrip lines all interact to produce the final signal. This means the simple addition of a power splitter or longer transmission line significantly shifts the center frequency of an

antenna array. Designing to these specifications without the usage of EM software such as Ansys Electromagnetics would be very difficult.

Given the fact that these devices were produced on flexible substrates, it is also important to consider the performance under the bending test. The usage of 5 mil Kapton HN provides excellent tensile performance compared to other polymide films[31], and the usage of a silver/polymer nanocomposite ink further improves lifetime flex performance of the devices as has been demonstrated in other papers[37]. Both the 1x4 and 1x8 devices presented usable performance under bending. However, the 1x8 was more resilient, showing adequate performance through all the tested values. In contrast the 1x4 devices began to degrade significantly around a 10mm radius. This test implies that denser arrays with more elements will be better for flexible electronics applications.

Note that denser arrays with more elements will incur an additional cost in producing these devices, as it will require both additional print time and materials. These negative effects can be combatted through the usage of small area fractal antennas[110] but fundamentally dense arrays will always cost more than their less dense counterparts. Optimization of the cost performance curve should be done on a per application basis, as dense array performance may not be needed in certain applications, while high flex applications may make it a necessity.

MULTI-ANGLE COMMUNICATION CAPABILITIES

One of the more interesting applications available to this particular antenna type is as a multi-angle communication device. Typically, a PAA can only receive or send a signal on one angle at a time[4], [96], [97]. Well-designed antennas will have a phase shifter network which can be reconfigured very quickly, but especially for devices with a high angular resolution, the time between when a given angle is received on may be significant.

For this device, such a lag is not needed. Using a microwave spectrum analyzer, the entire range of frequencies can be monitored for incoming signals. This in turn allows for a large range of angles to be simultaneously listened on. Furthermore, when a signal is received, directional information can be inferred from the frequency it was received on.

This combination is particularly useful for Internet of things (IoT) devices. Suppose we have an IoT device which has a single wide bandwidth antenna patch similar to the one used by the array that is sending data back to the array. As it does so, the directional nature of the array receiving allows the system to make conclusions about the IoT devices location. It can simultaneously receive from multiple devices as illustrated in Figure 6.15.

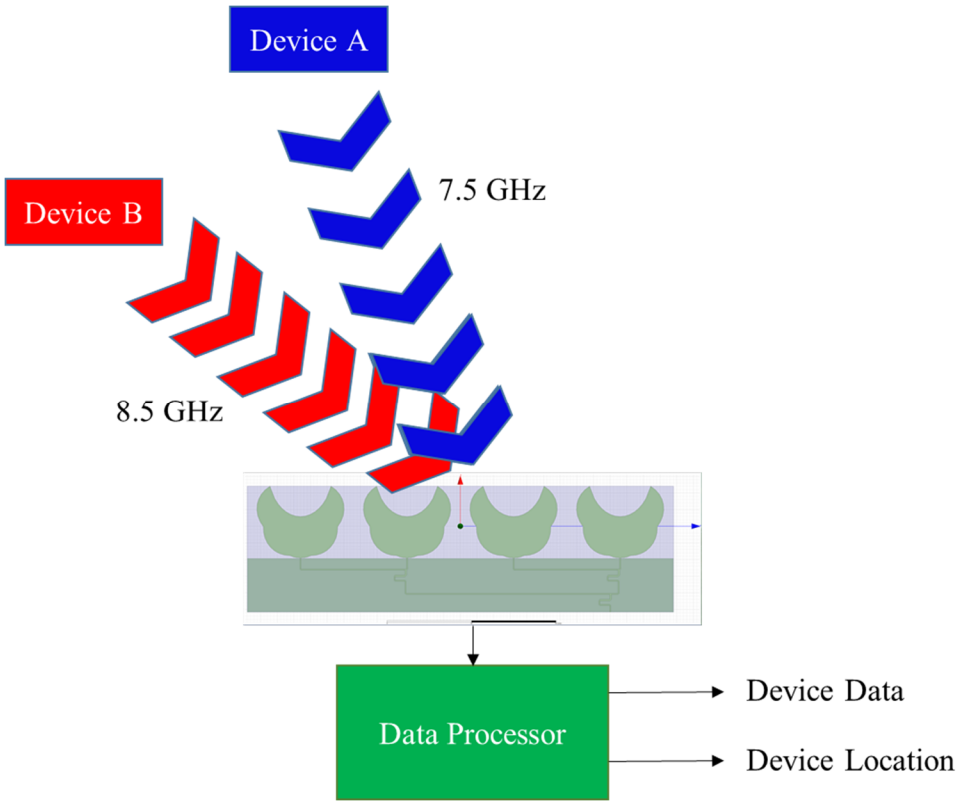

Figure 6.15: An example of the potential for this type of PAA to receive from multiple devices simultaneously.

This ability to receive on two frequencies simultaneously allows for more data intake without loss due to switching. Additionally, it allows for location information to be inferred by the data processor rather than requiring valuable board space on the IoT devices for GPS and other location information.

Chapter 7: Inkjet Printing Enabled Rapid Prototyping and Model Verification Processes[6]

In the last 20 years, additive manufacturing (AM) methodologies have captured the public imagination. 3D filament printing and cellular printing [18], [111], [112] have evoked the idea that the technologies of science fiction are right around the corner. In parallel with these headline grabbing technological developments though, AM has been quietly bringing new ways of device production to several industries, including but not limited to electronics, wearables, sensors, agriculture, security, farming, and medicine[113].

Conventional electronics relies on the use of CMOS technology, which fundamentally focuses on a subtractive process workflow. While this process has matured significantly and scaled in dimensions over the last six decades, thanks to Moore's Law[114], each successive generation has required even more expensive retooling in order to accommodate the new processes. AM has shown the promise to eliminate both the waste of the IC workflow allowing for the usage of more expensive materials, and to allow for new process and design testing without any expensive retooling in low to medium performance applications[115].

Current electronics AM methodologies which are seeing significant development include drop-on-demand and roll-to-roll inkjet printing as discussed previously, as well as screen printing, and aerosol jet printing such as the systems pictured in Figures 7.1a and 7.1b below. Each technology has its own application space and advantages. Drop-on-demand inkjet printing is based off of piezoelectric membrane drop formation used in color

[6] Content from this chapter was originally published in [6]. Peter Mack Grubb created the original concept for the hybrid process and developed the models for the different workflows himself. Dr. Harish Subbaraman assisted with proofreading and honing the models to accurately represent common practices in printed electronics.

inkjet printers[25]. This particular technology is extremely robust, allowing drop-on-demand systems to support a wide variety of materials. Additionally, the printing industry has already mapped out a small-scale to large-scale transition for this technology via the usage of roll to roll (R2R) printing systems. However, of the current printing technologies, the drop-on-demand system has the largest minimum dimension size. Aerosol jet printing grew out of a desire to shrink these minimum dimensions. By using an aerosolized inks with pressure control, the aerosol jet printer has a smaller dimension than the drop-on-demand system[116]. However, the large-scale system for high-rate production of devices is not as well developed. Of the printing technologies, screen printing is most similar to the IC workflow. Screen printing uses a mask to apply the ink, similar to the exposure mask used in lithographic processes. By using a mask, screen printing retains very small dimensions with a relatively high process throughput [53]. However, the usage of masks increases the cost of design changes, negating one of the advantages AM promises for electronics.

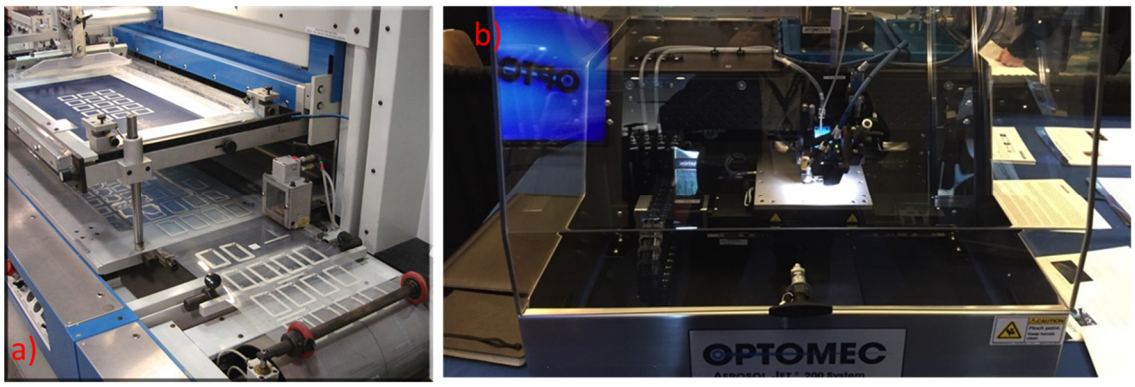

Figure 7.1: a) A typical screen jet printing system[117]. b) An Optomec Aerosol Jet 200 system[118].

Despite the quiet emergence of these new technologies, there has been very little effort to define the processes surrounding using them to produce actual electronics. Part of the power of the IC workflow is the fact that it is extremely well defined and documented, allowing advancements on one part of the process to be quickly integrated with other existing technologies. In this chapter, the current processes typically used in printing labs to produce devices using the three dominant printing technologies will be explored. Then, a potential integrated hybrid printed/IC workflow which maximizes the potential of each technology will be proposed, and examples of how specific devices have been produced using this workflow will be explored. Finally, the potential merits of each of these processes will be discussed forming the basis for future device production using both AM and conventional IC methods.

INKJET PRINTING AS A RAPID PROTOTYPING PROCESS

Given the common background of electronics AM and 3D printing, much of printed electronics follows a very similar rapid prototyping process. Rapid prototyping is characterized as an effort to try and bring some of the workflow elements of the "Agile" process from programming into physical prototyping efforts [119]. Rather than doing extensive simulation to plan a device out, rapid prototyping focuses on taking individual components of a design, quickly producing and testing them, and using the knowledge gained from this to improve the design of the next iteration as illustrated in Figure 7.2.

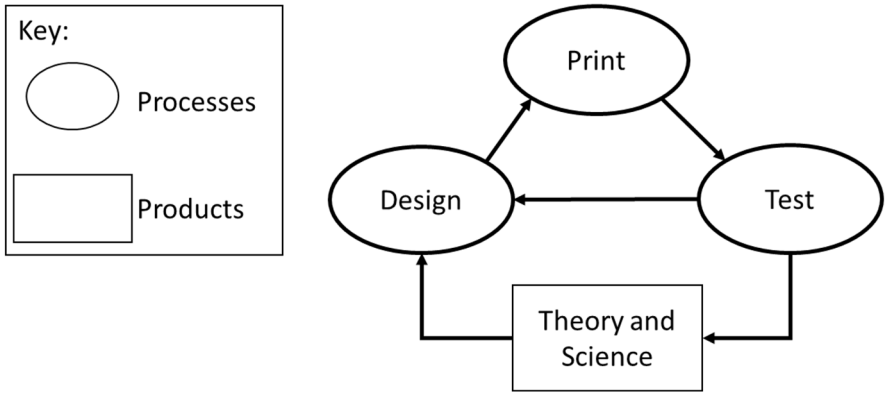

Figure 7.2: An example of the process used for rapid prototyping with electronics additive manufacturing. Each iteration improves the known Theory and Science surrounding the design, in turn improving both this design and future designs.

Compared to a typical process, the rapid prototyping process provides lots of real world test data. This is particularly valuable when building new types of devices which might represent edge cases for existing models. By using a quick production method to move to the test phase early and often, the unique challenges of a particular design can be quickly isolated and resources applied to overcome them.

Additionally, one of the other advantages of a rapid prototyping process is that it provides demonstrable prototypes relatively early in the development process. This can be useful for higher risk projects, as it provides concrete progress at many steps in the project.

The key to making rapid prototyping work is that each step in an iteration needs to be inexpensive enough that an open-ended number of iterations is not cost prohibitive. This is what prevents rapid prototyping from being used with conventional IC workflows or lithographic tools. Masks for lithographic exposures are expensive, and take time to have produced, both of which greatly increase the cost per cycle, making a rapid prototyping approach less appealing. Additionally, printing techniques such as screen printing have similar downsides. The production of each screen has significant costs associated with it,

making a many iteration process expensive. In contrast, both drop-on-demand and aerosol jet printing systems are maskless, with changes in design only requiring changes to a digital pattern file on a computer.

Once a design has been optimized via rapid prototyping, it must be transitioned to a large-scale manufacturing method for production. This is where technology selection becomes critical. For drop-on-demand inkjet, the transition from a small-scale printer to a roll-to-roll (R2R) printer is a well-documented process. Aerosol jet has similar potential to be used in a R2R apparatus, though the technology for it is less mature and more expensive in terms of upfront investment.

The primary problem with a rapid prototyping process is that the pressure for quick iterations and the nature of device testing can often mean that while improvements to a specific design are easy to pull out of testing, larger phenomenological conclusions can be difficult to produce. Simulation environments will often give very detailed readouts of the theoretical behavior of electromagnetic fields or semiconductor materials that are hard to capture using system testing apparatuses. While rapid prototyping can often indicate flaws in the design, identifying the design defect becomes difficult. Thus, setting up experiments to investigate particular aspects of a design is critical, albeit a difficult part of the rapid prototyping process.

CONVENTIONAL IC STYLE WORKFLOWS USING INKJET TECHNIQUES

While rapid prototyping has seen extensive usage in electronics AM, several flexible and printed devices are still primarily produced using conventional simulation-guided development[120], [121]. This is particularly common with complex devices with industry standard simulation environments, such as antennas whose performance can be extensively predicted using tools such as ANSYS Electromagnetics Desktop or COMSOL.

These simulation tools provide quick and straightforward insights into the behavior of the device, thus providing some advantages over rapid prototyping methodology. An example workflow in this vein is illustrated in Figure 7.3.

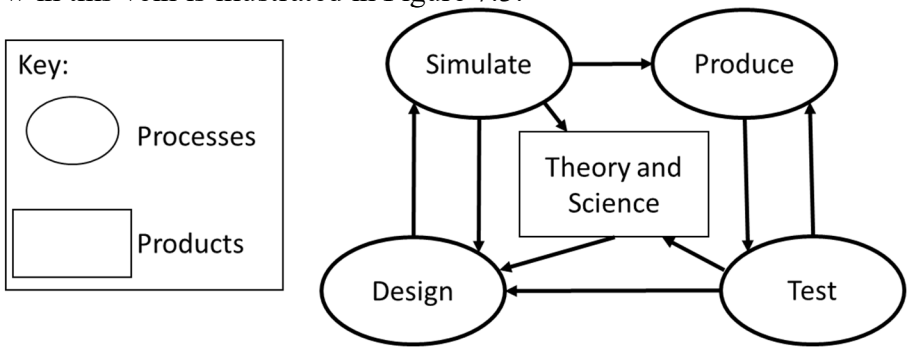

Figure 7.3: An example of an IC style workflow which can be followed using electronics AM methods. While there is an additional step feeding into the Theory and Science gained from the process, fewer iterations are typically done due to its roots in the cost driven IC development process.

Typically, this process is also used when the AM technology is used to bring new capabilities to the table other than the ability to rapid prototyping. For instance, AM methods are often far more compatible with particular types of coatings or with flexible substrates[122], [123]. In these cases, AM production methods enable new types of devices or materials, and consequently usually warrant a more extensive simulation process prior to production to fully understand the effects of these new materials or substrates on the performance of devices.

This type of process also has the advantage of being fully compatible with any of the major electronics AM methods currently on the market. With screen printing, it has the additional advantage of being able to jump straight from a successful prototype to a mass produced device. This high degree of compatibility underlines both the advantage of IC workflows in general, and in using them in the context of electronics AM.

One thing that makes this process very attractive to organizations trying electronics AM for the first time is the fact that it removes the pressure to have the AM apparatuses in house. For rapid prototyping to be successful, the turnaround time from a design to a test needs to be minimized, which usually means having the necessary equipment to produce a device in house. In contrast, without this pressure the AM process can be outsourced to an entity with expertise in that field. This reduces the startup costs associated with exploring an AM technology at the cost of giving up some control over how exactly the process is implemented. This can be critical to justifying the costs necessary to satisfy industry standard safety and lab practices when bringing AM in house.

The tradeoff inherent to using this workflow for AM is that it slows AM production speed in favor of a more deliberate simulation step. While the simulation step provides insight, it does not always reflect the reality of edge cases, leading to additional development cycles. This often reduces the potential positive impact of a move towards an AM production methodology. However, the ability to produce different classes of devices at lower costs still makes this methodology attractive.

HYBRID INTEGRATED PROCESS

Despite the advantages that electronics AM has brought to the various processes it is used in, it has not seen widespread adoption. This is largely due to challenges surrounding yield rates, and the specific types of devices which can be produced using printed electronics, along with the significant differences in feature size and performance metrics. However, the potential advantages that rapid prototyping can generate, especially for low-cost, low-to-medium performance electronic devices, are too significant to be ignored. Thus, it is worthwhile to investigate where an AM methodology could be used to

improve the process typically used for producing electronics regardless of the nature of the final device.

In the context of conventional IC lithography there are two main advantages that can be gleaned from AM devices: the ability to rapidly produce and test prototypes and the ability to apply coatings and other unique materials typically incompatible with IC production equipment. Thus, these are the two elements that should be brought into an IC workflow. An example workflow is shown in Figure 7.4 and explained in detail below.

Most of the typical IC production steps and their associated high costs are moved into a "Development Process" section, which will be addressed momentarily. Before moving to the Development Process, the device must first be designed. The proposed "Design Process" section exploits a rapid prototyping process to rapidly print and test devices. However, instead of merely using these elements to improve the design, as is typical done for a rapid prototyping process, the results of the prints and subsequent tests will be used to both verify the simulation and to develop the trade space associated with the device design. This trade space describes the inherent tradeoffs for the particular device being developed, such as the relationship between area and frequency for an antenna, for example. Using the known theory and science for a particular class of device, along with the verified simulation results and test results, this trade space can be rigorously defined and deeply understood.

Note that none of the steps in the Design Process are expensive both computationally and monetarily. Once the trade space is fully understood, the process moves from design to development. Based on the knowledge developed in the trade space, a refined design for a specific application can be developed. Depending on what is needed for this particular application, either an AM or IC production method can be selected, a pre-production prototype produced and then verified. Ideally, by performing iterations in

the Design Process, iterations in a more expensive Development Process are minimized to keep costs down.

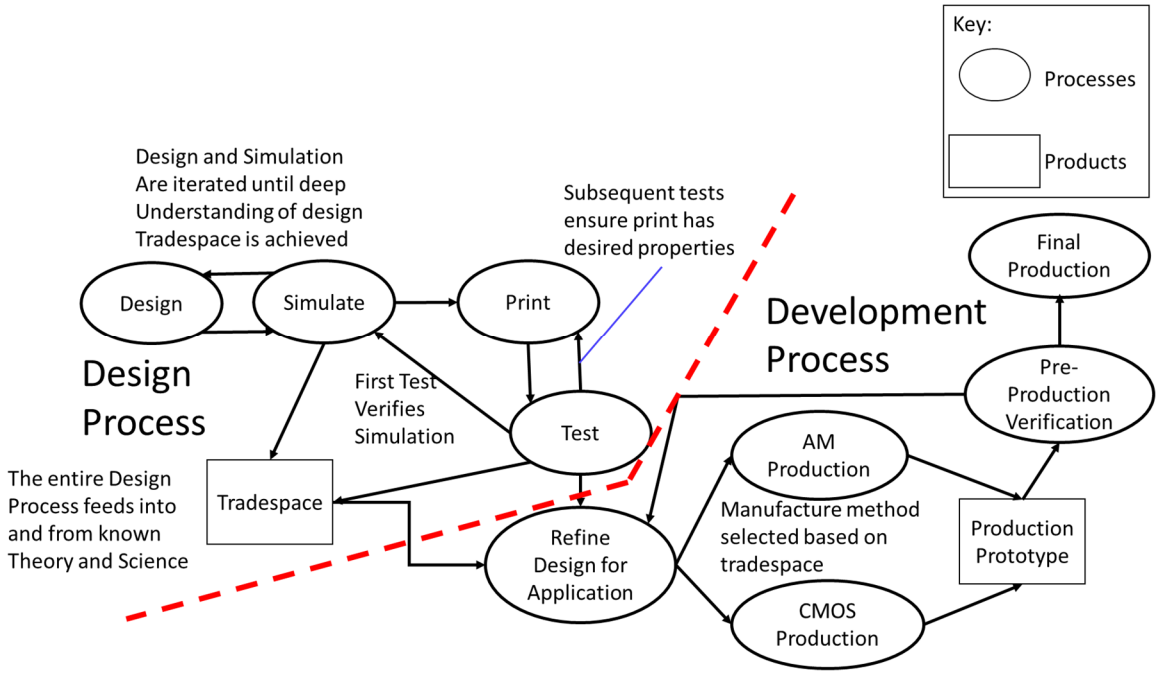

Figure 7.4: The proposed hybrid IC/Printing process. Note that it is split into a design and development process for the purpose of discussion. The Design process is intended to be iterated repeatedly to produce a high quality design, while the Development process is intended to minimize iterations in order to keep costs low.

Note that none of the steps in the Design Process are expensive both computationally and monetarily. Once the trade space is fully understood, the process moves from design to development. Based on the knowledge developed in the trade space, a refined design for a specific application can be developed. Depending on what is needed for this particular application, either an AM or IC production method can be selected, a pre-production prototype produced and then verified. Ideally, by performing iterations in

the Design Process, iterations in a more expensive Development Process are minimized to keep costs down.

This hybrid process will allow for the production of either conventional IC devices or a fully functional flexible electronic system. However, by separating a cheaply iterable Design Process from a more expensive Development Process, specialization in each portion of the process can be achieved. This fits into an existing industry standard of outsourced production facilities, but does so in a manner that allows for the significant advantages associated with rapid prototyping.

Typically, the start-up costs associated with being able to have in-house rapid prototyping of electronics would be prohibitively high. These high start-up costs are what have led to the consolidation of the silicon IC industry as a whole[124]. However, most electronics AM methods have relatively low startup costs compared to the IC industry and, more critically, do not require the maintenance of a clean room. The necessary equipment to add a rapid prototyping capability to an organizations design process is cheap enough that if it reduces the number of iterations using conventional IC production processes, it will easily pay for itself.

EXAMPLES OF ELECTRONICS PRODUCTION USING THE HYBRID PROCESS

To illustrate the potential capabilities of the hybrid production process, two examples of devices that can benefit from this process will be considered. One is a phased array antenna, while the other is a cheap, disposable Internet-Of-Things (IOT) device. Both have been previously printed successfully [4], [125]–[127], and there is a significant body of knowledge surrounding how they can be produced conventionally.

Phased array antennas (PAAs) are a class of devices which have seen significant development using printing technology [15], [121], [125], [128]. An example of a printed

device is shown in Figure 7.5. Of particular interest is the ability to do flexible arrays and sparse arrays without resorting to extremely expensive production methodologies. However, PAAs are complex devices which rely on the interaction of multiple high frequency antennas to produce a desired effect. As such, these devices are vulnerable to edge cases inn simulation environments which can cause difficulties in obtaining the desired performance.

A typical workflow for producing a PAA device involves extensive simulation efforts to refine the device design until the desired characteristics are understood. At this point the design would be sent to a manufacturing entity which would produce samples for testing. Any changes after the first batch of samples would be extremely expensive, with the exact cost depending on size and manufacturing methodology.

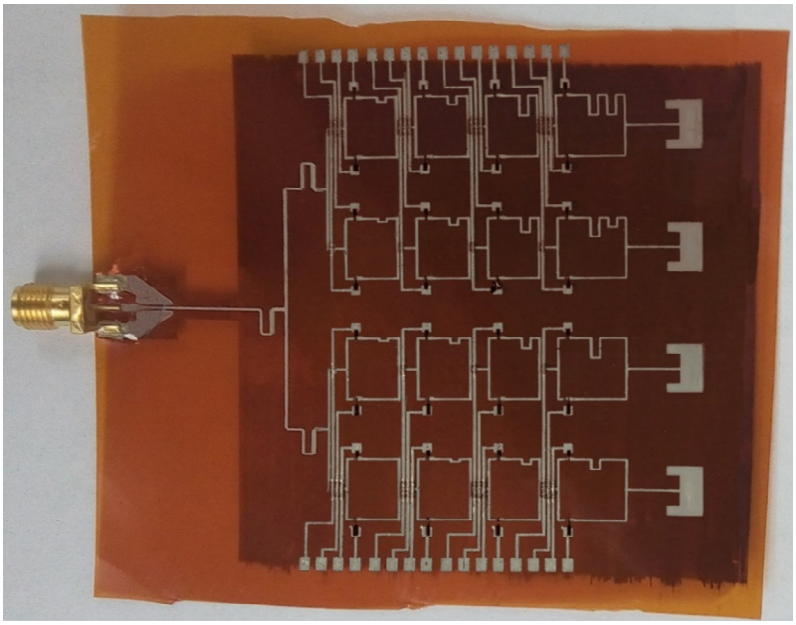

Figure 7.5: A printed 12 GHz phased array antenna device.

To imagine how this device might benefit from the hybrid process, consider a design for the device shown in Figure 50. Initially the device would be designed and simulated using ANSYS Electronics desktop. However, in the printing and testing phase, it is found that the heat curing of the substrate causes the thickness of the Kapton to change, causing a change in the performance of the device. This is then fed back into the model to improve the design, and test other frequencies. Each step of the way, a better understanding of the interaction of the various materials being used is coming together.

Once an optimized prototype like the one pictured in Figure 50 is developed, it is ready to move to application design. In this hypothetical example, the final application requires a flexible substrate, which prioritizes an R2R printing setup. However, given the large amount of ink required to start up an R2R printer, the amount of print runs should be minimized. Since an optimized prototype has already been produced using methods similar to the R2R system, the number of attempts required to produce the same device using an R2R system should be minimal. With a production prototype in hand, the device can then move to full scale production, all while minimizing the costly iterations to get to this point.

A second class of devices worth investigating are cheap disposable IOT devices such as one time use heart rate monitors. The falling costs of production are enabling small devices which may consist simply of an antenna and a sensor on a flexible substrate. Such devices could use gas sensors for methane detection, for example, food storage status recording, personal health monitoring, or other sensing applications. From a user convenience standpoint, the ideal device would be disposable such that a user could use it once and afford to discard it, particularly if the object being monitored is being shipped or otherwise transferred between users.

In a conventional development process, the heart rate sensor would be modeled using some type of physics software if possible, while the circuit would be simulated using

PSPICE or another ASIC design software. There might also be a bench top phase where the physics of the sensor would be verified relative to the theoretical model. However, integration testing would depend on the bench top prototype, which might or might not have tolerances and sensitivity levels similar to the final device. Once integration testing was complete, the device would be sent to a manufacturing entity and produced en masse.

Using the hybrid process, integration testing of the heart rate sensor could proceed from the earliest stages. Using a drop-on-demand system, reasonable facsimiles of the final device could be produced and tested in the design stage, uncovering interactions which would cause performance issues. This would also allow for early assessment of packaging concerns and comfort levels for such a device, which tend to be more critical in health care oriented devices. Once the device design was completed, both a traditional IC based device and a printed version could be produced and compared in terms of both performance and cost/unit. Additionally, alternative packaging possibilities could be explored to design something that best fit the use case. The final product would then select the production methodology based on the exact target application.

By using an AM driven design process, these devices would undergo integration testing at a much earlier phase in the overall production process. This would allow for more use driven testing, and by extension a more user friendly device. Additionally, the potential pitfalls of transitioning from a benchtop apparatus to a compact device are largely avoided.

DISCUSSION

This hybrid process was created as an answer to the lack of OEM printed electronics devices currently being shipped. While there has been substantial interest from several different major electronics production companies[129], for the most part printed devices which could reach a consumer are few and far between.

While the situation is odd by electronics standards, it is very similar to what has happened with 3D filament printers. Despite capturing the public imagination, most of the things actually produced using 3D printing are either very small-scale or highly customized. In the case of the 3D filament printer, its biggest impact has been in the prototyping process, where it allows mechanical prototypes to be rapidly produced and tested. In most cases the consumer can never tell what the role of the 3D printer was in producing their purchase.

Similarly, the proposed hybrid process seeks to outline a niche allowing electronics AM to improve existing electronics production rather than create a specific consumer electronic device using printing. That said, part of the appeal of the process is the fact that it can accommodate large-scale R2R printing. By separating the development and production processes, R2R printing can move into the realm of OEM style outsourced production, making it more cost effective than it currently is.

Most current efforts of R2R printing are done in house requiring design changes from the ground up in order to make design work with them[24], [86]. This is because a specific design rather than an understanding is transitioned from the small-scale printing process to the large. By building a trade space, the hybrid process allows us to feed the particular advantages and disadvantages of a given design into the limitations of a particular manufacturing setup, rather than feeding in a particular design. This creates an end to end approach to design, whereby devices are cheaply optimized for each production methodology.

This brings us to the advantages of the hybrid process. First and foremost, this process keeps costs down by concentrating repeated iterations in a process which has a very low per device cost. This allows knowledge to be developed without incurring significant costs prior to moving to a more production oriented process like IC production.

Additionally, by having the prototype production in house, there is no time lag between device design and prototype production. This removes the 1-4 week lag usually associated with having test devices produced, not to mention the large costs associated with it.

The other advantage comes in the realm of model verification. By creating steps to explicitly verify the model, edge cases of modeling methodologies can be found and assessed. This in turn improves models for future device production, providing an organization an in built advantage for future efforts. Given that differences between models and actual devices can typically cause costly mistakes, this compounding advantage is attractive in both a research and corporate setting.

Electronics additive manufacturing is a discipline rapidly running towards the point where it can have meaningful impact on the methods and processes used in the building of electronics devices. As such, it is important to examine where such processes could have the biggest potential impact. This hybrid process shows how AM systems can be integrated into current electronics workflows to build devices at a lower cost, and much faster than existing methodologies.

Chapter 8: Conclusion

In conclusion, a series of advances to the state of the art of inkjet printing were presented. First, a series of ink innovations were shown, including a non-aqueous UV curable CNT solution. These ink innovations were then leveraged to build several devices using new techniques. One such device was a high performance micro-gapped transistor, which demonstrated speeds of 18.21 GHz. Other devices included a high speed roll to roll compatible transistor with only UV curing, and a frequency scanning array antenna. The experiences of building these devices and inks were then used to present a way to use printed electronics techniques to achieve better results in a traditional IC fabrication strategy.

These advancements cover the gamut of what is involved in creating devices using printed electronics. Thus, this dissertation represents an across the board improvement in available inkjet printed electronics techniques and results. Using the processes and materials described previously, faster, cheaper devices can now be built, as well as new classes of devices such as the frequency scanning array.

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