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A Developed Asymmetric Multilevel Inverter with Lower Number of Components

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ABSTRACT: In this paper, a new configuration for symmetrical and asymmetrical multilevel inverters is proposed. In asymmetric mode, different algorithms are suggested in order to determine the magnitudes of DC voltage sources. The merit of this topology to the conventional symmetric and asymmetric inverters is verified by the provided comparisons. This topology uses a lower number of power electronic devices such as switches, IGBTs, diodes, related gate driver circuits and DC voltage sources. Owing the lower amount of requirements, it has lower total costs and needs less installation area. Also the control strategy has less complexity. The proposed converter can generate all the desired output voltage levels with positive and negative values. To confirm the practicability of the proposed inverter, simulation and experimental results are provided which are in good agreements.

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1- Introduction

Since the initial prototype of multilevel inverter was introduced in early 1980s by Nabae *et al*., there have been intense investigations devoted to the multilevel inverters. Multilevel inverter is considered as an essential device in power conversion process, enabling to generate the desired AC voltage waveform synthesizing several DC voltage sources. In this regard, they have successfully made their own way into the industry and academia as one of the preferred choices of DC/AC power conversion. A multilevel inverter is composed of several power semiconductor switches, diodes and DC voltage sources. A multilevel inverter creates a stepwise voltage that is similar to sinusoidal waveform and it will be much similar as the number of voltage steps increases by an increase in the number of input DC voltage sources. The semi sinusoidal output waveform of multilevel inverters will provide superior characteristics in comparison with 3-level inverters. Some of these characteristics are lower total harmonic distortion, higher power quality, better electromagnetic interface, higher efficiency, lower switching losses, and lower *dv/dt* [1-4]. The output voltage waveform of multilevel inverters can be enhanced by using switching strategies such as PWM and SPWM. Using these kinds of methods will help the output waveform to become more similar to absolute sinusoidal [5, 6]. Power quality issues of the output waveforms such as harmonics spectra are discussed in several international standards like IEEE-929, IEEE-1547 and EN-61000-3-2. Multilevel inverters family consists of three major sections, including; Diode Clamped (DCM), Flying Capacitor (FCM) and Cascaded H-Bridge (CHB) Multilevel inverters. Diode Clamped ones have problems with the inequality of current stresses and voltage unbalancing [7]. Flying capacitor multilevel inverters are less popular in industrial applications, because of their higher switching frequency that is needed to maintain the capacitor voltages' balance and also the requirement of the FC initial voltages [8]. Among various topologies of multilevel inverters, CHB has attracted special attention due to its unique characteristics such as modularity and simplicity of control procedure, nevertheless this topology has its own disadvantages such as the circuit complexity, higher number of isolated DC voltage sources and power switches. Multilevel inverters are divided into two subdivisions from the aspect of DC voltage source value. The first group that uses DC voltage sources with equal values (symmetric topology) and the second group with unequal DC voltage sources (asymmetric topology) that can reach higher number of voltage steps in comparison with symmetric topologies considering the same number of circuit devices, although providing DC voltage sources with different values could make the topologies difficult to be realized. Symmetric topologies have the advantage of simplicity in providing DC voltage sources that may lead to lower implementation costs, but on the other hand these topologies can generate lower number of voltage steps in comparison with the asymmetric ones. Due to the dependency of overall cost, circuit size, reliability and control complexity on the number of DC voltage sources, semiconductor switches and related gate driver circuits of switches, the number of required circuit devices are important in multilevel inverter structures. Nowadays advanced topologies are developed to reduce the high number of components in multilevel inverter. Various cascaded multilevel inverter with different topologies

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have been introduced by now [9-16]. In [9], two different algorithms are proposed to define the magnitudes of DC voltage sources in CHB. Using asymmetrical DC sources can increase the number of output voltage levels. A novel MVSI, has been reported in [10]. This inverter uses bidirectional switches, Each bidirectional switch consists of two IGBTs and two diodes. If these IGBTs are connected as common emitter, then for each bidirectional switch, only one gate driver circuit is needed. The main novelty of this converter is about the reduced number of switches compared to CHB. This improvement causes a reduction on gate drive circuits. But this topology encountered with higher peak inverse value (*PIV*) compared to CHB. The topology presented in [11] uses unidirectional switches. For unidirectional switches the number of gate drivers is equal to the number of switches. Here, the number of switches and gate driver circuits are less than conventional CHB but the total *PIV* is more. The inverter of [12] reduces the requirements for circuit devices. It is known that reducing the number of switches from the conventional inverters imposes an undesired increase in total *PIV* value. With proper connection of power switches to DC voltage sources, this increase can be limited. Comparatively, the *PIV* of [12] is increased to that of [11]. But, it must be mentioned that, since the number of IGBTs, switches and gate driver circuits are reduced significantly, an increase in total *PIV* is acceptable and can be neglected while this increase cannot detract from its values of obtained benefits from reductions. A novel MVSI has been suggested in [13] that reduces the power components compared to CHB resulting higher *PIV.* But its *PIV* is less than those of [10, 12]. The topology presented in [14] is the reconfiguration of [10]. This inverter is well known because of its lower number of semiconductor switches. The *PIV* of this inverter is reduced, compared to that of [10] while this number is more than that of CHB. Recently novel MVSIs have been suggested. The required power devices for these inverters are lower compared to CHB, and these inverters have kept the *PIV* equal to CHB [15, 16]. The main significant improvement done in this paper is proposing a novel configuration for the symmetric and asymmetric multilevel voltage source inverter. This topology is originated from the idea of conventional CHB inverter. In comparison with conventional CHB and the presented CHB based inverters in [9-16], it uses a lower number of circuit devices. Simple control scheme, significant reduction of installation area and total costs due to lower number of circuit requirements are features of this topology. By comparing this topology with prior topologies, perfection of this topology is validated due to minimum number of power switches, IGBTs, power diodes, driver circuits and DC voltage sources. In the rest of this paper, after describing the structure and details of the proposed topology, a full comparison is made between the suggested inverter and other well-known symmetric and asymmetric inverters. Simulation and practical results are provided before presenting the conclusion section.

2- Proposed Configuration

The basic cell of the proposed MVSI in this paper is illustrated in Fig 1(a). Three DC voltage sources and five unidirectional switches are depicted as well. The values of DC voltage sources are equal due to the fact that this cell is symmetric. Each unidirectional switch is made up of an IGBT and an anti-parallel fast recovery diode. Each basic cell can produce three positive and a zero output level. In table 1, possible switching states of the basic suggested cell are presented. Table 1 represents ON state of the switch and zero represents for OFF state of the switch as well. Based on information provided by table 1, the equivalent circuits for *i-th* basic cell of the suggested MVSI are as shown in Fig 1(b)-(e), with flexibility of generating various voltage levels.

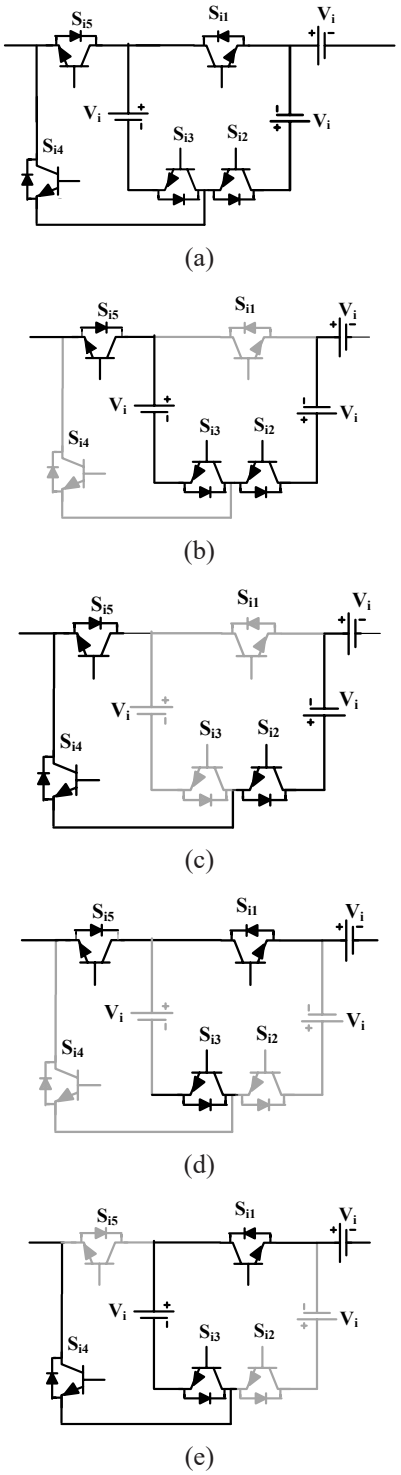


Fig. 1. a) Circuit diagram of the basic cell of proposed MVSI and Equivalent circuits of it for; b) $3V_i$, c) $2V_i$, d) V_i, and e) zero level

Table 1: Various switching states of i-th suggested basic cell

State	S_{i1}	S_{i2}	S_{i3}	S_{i4}	S_{i5}	V_o
1	0	1	1	0	1	$3Vi$
2	0	1	0	1	1	$2Vi$
3	1	0	1	0	1	Vi
4	1	0	1	1	0	0

In Fig. 2 general view of the proposed MVSI is depicted. As shown series connection of *k-basic* cells associated with 2 independent DC voltage sources and related switches formed the proposed inverter. V_{dc} and V_s indicate the mentioned independent DC voltage sources. the Number of DC source determines the value of V_s, and also the number of DC sources is determined by number of output voltage levels, therefore possible values for V_s are $0, V_{dc}$ and $2V_{dc}$ according to number of DC sources. All possible voltage steps with both positive and negative values can be produced by proper using of H_U, H'_U, M, M', H_L and H'_L switches. In the structure of this topology there are *n*-isolated DC voltage sources and these DC voltage sources can be prepared by rectifiers connected to isolated transformers fed from AC voltage, renewable sources like fuel cells, photovoltaic panels or with energy storage devices, like batteries [17]. For instance, if the PV panels are employed as DC voltage sources, they are already equipped with DC/DC converters for voltage level adjustments. Nevertheless, the undesired changes in the DC voltage sources can be compensated by complementary modulation strategies [21, 22]. The implementation of these methods needs the manipulation of the inverters hardware by additional devices and circuits, and makes the control scheme more intricate. Due to the fact that the main purpose of this paper is proposing a novel structure for multilevel inverters, so countervailing differences of DC voltages which can be done by modulation methods, is not taken into consideration. Maximum output voltage is achieved by combining individual DC voltage sources, and in order to calculate the peak amount of output voltage the following equation is taken:

$$V_{o,\max} = \sum_{i=1}^{n} V_i \tag{1}$$

In this equation, n is the number of DC sources, and the number of voltage levels (m) can be calculated by the following equation:

$$m = 2\frac{V_{o,\max}}{V_{dc}} + 1 \tag{2}$$

As mentioned before, the output voltage sets the value of V_s, and to clarify the proposed inverter, it is needed to specify a parameter that is an integer number ($L = 1, 2, 3, \ldots$) and will help develop a relation between m and n as defined in the equations below, where again, m is the number of output levels and n is the number of DC voltage sources.

$$n = \begin{cases} \frac{m-1}{2}; & if\ m = 6L+3 \\ \frac{m-1}{2}; & if\ m = 6L+5 \\ \frac{m-1}{2} - 1; & if\ m = 6L+7 \end{cases} \tag{3}$$

In order to reach a certain number of output voltage levels, the number of cells must be increased on the basis of a proper formula that is between n and k the below equation defines the relation between n and k.

$$k = \begin{cases} \frac{n-1}{3}; & if\ m = 6L+3 \\ \frac{n-2}{3}; & otherwise \end{cases} \tag{4}$$

The relationship between V_s and m is mathematically formulated in the following equation:

$$V_S = \begin{cases} 0 & if\ m = 6L+3 \\ V_{dc} & if\ m = 6L+5 \\ 2V_{dc} & if\ m = 6L+7 \end{cases} \tag{5}$$

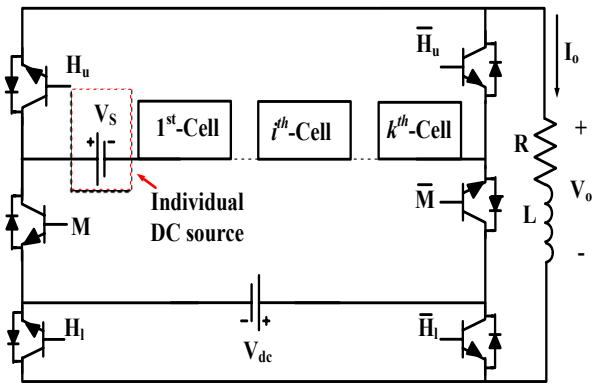


Fig. 2. Proposed MVSI

To have m-levels in output voltage, the required number of DC voltage sources and V_s can be obtained by the given formulas such that to produce 9-levels in output voltage, the number of DC voltage sources is four and then V_s is set to be zero. Also, for $m = 11, 13$, the number of DC voltage sources is calculated to be five, and subsequently V_s is obtained to be $V_s = V_{dc}, 2V_{dc}$, respectively. In the suggested inverter, N_{switch} indicates the number of switches, and it can be calculated as followed:

$$N_{Switch} = \begin{cases} \frac{5n+13}{3}; & if\ m = 6L+3 \\ \frac{5n+8}{3}; & otherwise \end{cases} \tag{6}$$

Moreover, the equation between the number of output levels (m) and the number of switches (N_{switch}) is as follows:

$$N_{Switch} = \begin{cases} \frac{5m+21}{6}; & if\ m = 6L+3 \\ \frac{5m+11}{6}; & if\ m = 6L+5 \\ \frac{5m+1}{6}; & if\ m = 6L+7 \end{cases} \tag{7}$$

Each switch needs a driver circuit to create its switching pulses, so:

$$N_{Driver} = N_{switch} \tag{8}$$

And for calculating the total PIV, these equations can be used:

$$PIV = \sum_{j=1}^{N_{Switch}} PIV_{Switch_j} \quad (9)$$

So, the following formulations are used to calculate the total PIV :

$$PIV^{p.u.} = \begin{cases} \frac{19n}{3} - \frac{7}{3}; & if\ m = 6L+3 \\ \frac{19n}{3} - \frac{14}{3}; & if\ m = 6L+5 \\ \frac{19n}{3} - \frac{2}{3}; & if\ m = 6L+7 \end{cases} \quad (10)$$

In symmetric mode, the relationships between PIV and m are formulated as follows:

$$PIV^{p.u.} = \begin{cases} \frac{19m-33}{6}; & if\ m = 6L+3 \\ \frac{19m-47}{6}; & if\ m = 6L+5 \\ \frac{19m-61}{6}; & if\ m = 6L+7 \end{cases} \quad (11)$$

3- Asymmetric Method

The number and the values of DC voltage sources in multilevel inverters will determine the maximum output voltage amplitude as well as the number of voltage steps. It is obvious that the proposed inverter can be used in both symmetric and asymmetric modes. One way to reach a considerable increase in the number of output levels is to determine the proper magnitude for DC sources, so several algorithms are proposed to calculate the magnitude of DC sources. These proposed algorithms and all their parameters are calculated and shown in Table 2. Regarding the asymmetric mode, DC voltage source values are equal in each cell; however, the magnitudes of DC voltage sources for different cells differ from each other. In the proposed algorithms, a noticeable increase in the number of output voltage steps occurs, without any manipulation on inverters structure. The proposed inverter is called an asymmetric inverter since the magnitudes of DC sources are different from each other in all of the proposed algorithms. Equations indicate that, in addition to the number of output voltage steps, the maximum output voltage of the proposed asymmetric topology is more than symmetric structure that uses the same number of DC sources and switches. In some algorithms defined for asymmetric mode, the proposed inverter can increase the number of output voltage levels by adding two power switches for controlling V_s, Fig. 3 defines the arrangement of these switches surrounding V_s. This reform is essential where the value of V_s is found to be none zero (see algorithms 5 and 6). Otherwise, there is no need to use these switches. Nevertheless, the number of DC sources is pointed by n.

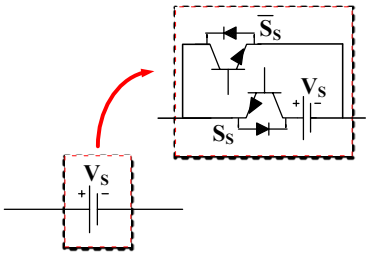


Fig. 3. Required reform to increase the number of outputvoltage steps

A full comparison is provided to analyze the advantages and disadvantages of the proposed algorithms of asymmetric inverter, in this regard, the proposed algorithms are referred to as P_1 to P_6, respectively. The comparisons are made based on the number of output voltage levels. As it is shown in Fig. 4 (a) that compares the number of IGBTs used in different algorithms, the 6th proposed algorithm uses the least number of IGBTs.

As mentioned before, unidirectional switches have the same number of IGBTs with number of switches, power diodes and driver circuits. So, the number of switches, power diodes and driver circuits in the 6th proposed algorithm is less than the other mentioned methods.

Fig. 4 (b) compares the number of DC voltage sources versus the number of levels for the proposed algorithms. It is obvious that the 6th proposed algorithm uses less DC voltage source to generate particular levels.

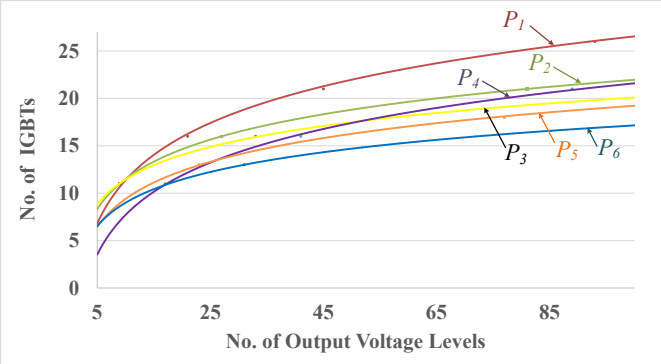


Fig. 4. (a) Number of IGBTs versus number of levels for proposed algorithms

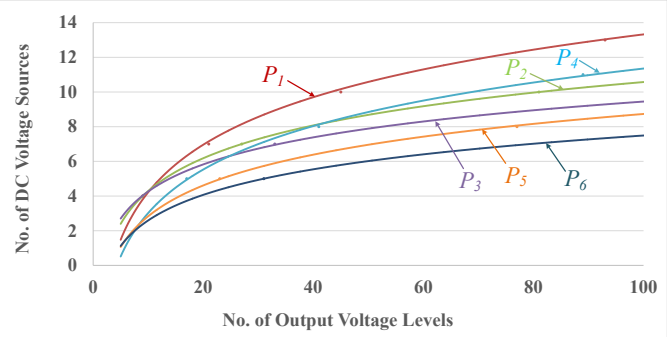


Fig. 4. (b) The number of DC voltage sources versus number of levels for proposed algorithms

The above comparisons show that, the sixth proposed algorithm has better performance than the mentioned solutions.

4- comparison of The Proposed Inverter with other Multilevel Inverters

From several technical points of view mentioned in the above comparisons, it's obvious that multilevel inverters with unequal DC sources (asymmetric inverters) in comparison to the usual symmetric inverters are more efficient. Since the overall costs, circuit size, reliability and control complexity of multilevel voltage source converters are in direct relation with the number of circuit devices used in multilevel converters, including DC voltage sources, power semi-conductor switches and related gate driver circuits of switches, every

Table 2. The proposed algorithms for asymmetrical converter and their related parameters

Proposed algorithms	V_S	*Magnitude of DC voltage sources*	k	N_{Switch}	m	PIV^{pu}
1st proposed algorithm	0	$V_{1,1}=V_{2,1}=V_{3,1}=V_{dc}$ $V_{1,j}=V_{2,j}=V_{3,j}=2^{j-1}V_{dc}$ $j=2,3,...,k$	$\frac{n-1}{3}$	$\frac{5n+13}{3}$	$3\times2^{K+1}-3$	$19\times2^{k}-15$
2nd proposed algorithm	0	$V_{1,1}=V_{2,1}=V_{3,1}=V_{dc}$ $V_{1,j}=V_{2,j}=V_{3,j}=3^{j-1}V_{dc}$ $j=2,3,...,k$	$\frac{n-1}{3}$	$\frac{5n+13}{3}$	3^{K+1}	$\frac{1}{2}[19\times3^{k}-11]$
3rd proposed algorithm	0	$V_{1,1}=V_{2,1}=V_{3,1}=V_{dc}$ $V_{1,j}=V_{2,j}=V_{3,j}=4^{j-1}V_{dc}$ $j=2,3,...,k$	$\frac{n-1}{3}$	$\frac{5n+13}{3}$	$2\times4^{k}+1$	$\frac{1}{3}[19\times4^{k}-7]$
4th proposed algorithm	0	$V_{1,1}=V_{2,1}=V_{3,1}=2V_{dc}$ $V_{1,j}=V_{2,j}=V_{3,j}=2\times4^{j-1}V_{dc}$ $j=2,3,...,k$	$\frac{n-2}{3}$	$\frac{5n+8}{3}$	$3\times2^{K+2}-7$	$19\times2^{k+1}-30$
5th proposed algorithm	1	$V_{1,1}=V_{2,1}=V_{3,1}=3V_{dc}$ $V_{1,j}=V_{2,j}=V_{3,j}=3^{j}V_{dc}$ $j=2,3,...,k$	$\frac{n-2}{3}$	$\frac{5n+14}{3}$	$3^{K+2}-4$	$\frac{1}{2}[57\times3^{k}-37]$
6th proposed algorithm	2	$V_{1,1}=V_{2,1}=V_{3,1}=4V_{dc}$ $V_{1,j}=V_{2,j}=V_{3,j}=4^{j}V_{dc}$ $j=2,3,...,k$	$\frac{n-2}{3}$	$\frac{5n+14}{3}$	$2\times4^{k+1}-1$	$\frac{1}{3}[19\times4^{k+1}-28]$

development done to lower these devices will improve the total acceptability of the multilevel converters. Suppose the case that the output voltage has seventy-seven levels, and the converter uses equal DC sources (symmetric mode).

The number of used DC voltage sources is thirty-eight and 'sixty six' is the number of switches and gate driver circuits. This time suppose that the mentioned output is generated by the asymmetric converter (using 6th proposed algorithm), in this case, the numbers are eight and eighteen, respectively. Making this comparison for all ranges of output levels will lead to the fact that asymmetric multilevel converters need lower number of devices to generate a specific output level in comparison with symmetric converters. In this regard, the proposed asymmetric configuration with its 6th proposed algorithm is applied in comparisons. It is pointed out that all other inverters participated in the comparison study and their different algorithms are shown by $R_1 - R_{10}$ in these comparisons. The conventional symmetric cascaded H-bridge inverter is pointed by R_1. Moreover, two other algorithms for this inverter have been presented in [9]. These algorithms are indicated by R_2 and R_3, respectively. In these algorithms the values of DC links are as $V_1 = V_{dc}, V_{2-\infty} = 2V_{dc}$ and $V_1 = V_{dc}, V_{2-\infty} = 3V_{dc}$, respectively. The other reported symmetric multilevel inverters are indicated by R_4 - R_{10}. The inverter of [11] is presented by R_4, and R_5 is the reported of [14]. The proposed configurations in [15, 16] are indicated by R_6, R_7 respectively. R_8 is the inverter of [10]. R_9 Represents the inverter of [13], finally R_{10} structure was pointed out in [12]. Fig 5 (a) illustrates the number of IGBTs versus number of voltage levels for various MVSI topologies. Since the switches used in this topology are unidirectional switches, then the number of gate drivers is equal to N_{Switch}; However, the topology of R_8 uses several bidirectional switches in its structure. There are two IGBTs in a bidirectional switch, but since these IGBTs are connected in common emitter mode, they have a common gate driver circuit together as well. Fig. 5 (b) shows the number of gate driver circuits versus output voltage levels. By investigating Fig. 5 (a) and 5 (b), it's clear that the proposed topology reduces the number of required power electronic devices, in all possible range of output voltage levels. Therefore, less components result in some reduction in the required installation area and costs. Also, the control scheme gets simpler. The number of required DC voltage sources is another parameter that plays a key role on overall inverter costs. Fig 5 (c) shows the number of DC voltage sources versus output levels in all mentioned inverters, from the comparison studies, it can be said that to realize the same level in the output, the number of required DC voltage sources in the proposed inverter is lower.

Another essential parameter which plays a consequential role on overall inverter expense is voltage ratings of power switches. The voltage rating of the selected power switches is completely dependent on the structure of applied fundamental unit of multilevel inverters. It is known that reducing the number of switches from the conventional inverters imposes an undesired increase in the total PIV value. With proper connection of power switches to DC voltage sources, this increase can be limited. Fig. 5 (d) displays the PIV value of

the mentioned inverters.

Because of the big reduction in circuit equipment in the proposed inverter, a bit increase in its total *PIV* compared to some conventional inverters is acceptable and can be neglected, while a reduction in number of switches, gate driver circuits and DC power supplies are achieved.

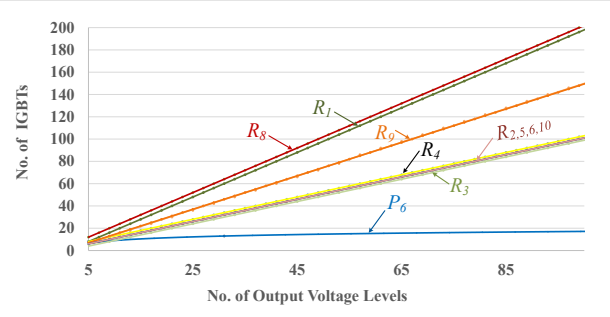


Fig. 5. (a) Number of IGBTs versus number of levels for proposed topology and other mentioned solutions

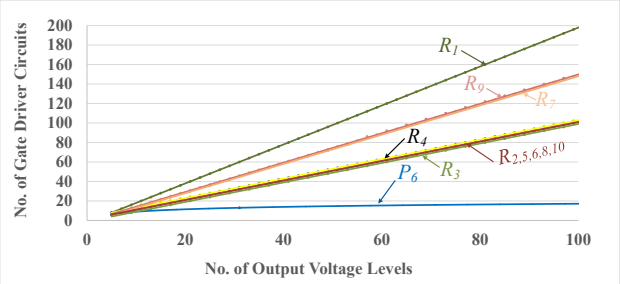


Fig. 5. (b) Number of gate driver circuits versus number of levels for proposed topology and other mentioned solutions

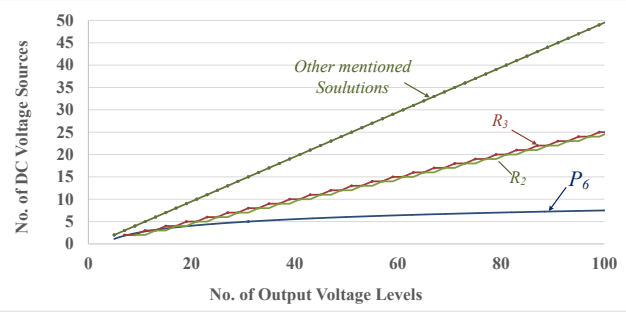


Fig. 5. (c) The number of DC voltage sources versus number of levels for proposed topology and other mentioned solutions

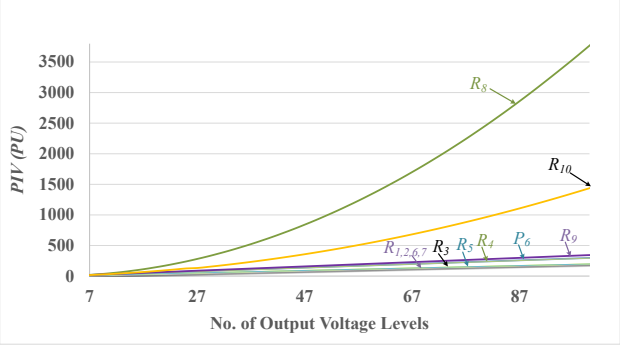


Fig. 5. (d) Total PIV value versus number of levels for proposed topology and other mentioned solutions

5- Simulation and Experimental Results

To determine the practicability of the proposed multilevel inverter, simulation of circuit is inevitably needed. MATLAB/Simulink software is used to simulate the circuit, and to evaluate the performance of the suggested MVSI, experimental results are obtained. Adjustable DC sources in laboratory have been utilized in order to provide the DC voltage links. Table 3 represents the main parameters of proposed circuit.

Table 3. Parameters of implemented inverter

Type of switch	IRF260
Type of MOSFET driver	Hcpl316j
Pulse Generator	AVR mega 32
DC Voltage Sources Magnitudes	$V_{dc} = 5V$
Series R-L Load Parameters	35 Ohm & 36 mH
Fundamental Frequency	50Hz

Since the multilevel inverters are introduced, several switching control strategies have been developed to improve the quality of output power. For instance, fundamental frequency-switching, sinusoidal PWM, selective harmonic elimination (SHE-PWM), space vector PWM (SV-PWM), and others are some of the modulation techniques that are used. The benefit of the fundamental frequency-switching scheme is its low switching frequency [23]. For power converters, the total harmonic distortion (THD) is a popular performance index, which evaluates the quantity of harmonic contents in the output waveform. The THD is defined as follows: The ratio of the sum of the RMS value of the power of all harmonic components to the RMS value of the power of the fundamental frequency component is defined as THD. So the following equation gives the THD value.

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_{o_n}^2}}{V_{o_1}} = \sqrt{\left[\frac{V_{o_{rms}}}{V_{o_1}}\right]^2 - 1} \tag{12}$$

In this equation, n -represents the order of the corresponding harmonic, while the sub-index 1 corresponds to the fundamental frequency. Hence, V_{o_n} and V_{o_1} are the rms of the n order harmonic and fundamental of the output voltage, respectively. Also, $V_{o_{rms}}$ represents the rms magnitudes of the output voltage. In the above relation, the value of V_{o_1} and $V_{o_{rms}}$ can be obtained using the following equations, respectively:

$$V_{o_{rms}} = \frac{2\sqrt{2}}{\pi} V_{dc} \sqrt{\sum_{m=1,3,5,\ldots}^{\infty} \left(\sum_{j=1}^{N_{Level}} \frac{\cos(m\theta_j)}{m}\right)^2} \tag{13}$$

$$V_{o_1} = \sum_{j=1}^{N_{Level}} \frac{2\sqrt{2}}{\pi} V_{dc} \cos(\theta_j) \tag{14}$$

Where, the values of $\theta_1, \theta_2, \ldots \theta_{N_{Level}}$ represent switching angles and are calculated by the methods proposed in [18-20]

$$\theta_j = \sin^{-1}\left(\frac{j-0.5}{N_{Level}}\right) \quad j = 1, 2, 3, \ldots N_{Level} \tag{15}$$

It is clear that the value of THD depends on the number of levels and so, switching angles. It is clear that the objective

of this paper is not THD minimization, and this procedure is only used to generate the output voltage levels. Fig. 6 shows the circuit diagram of the 31-Level multilevel inverter.

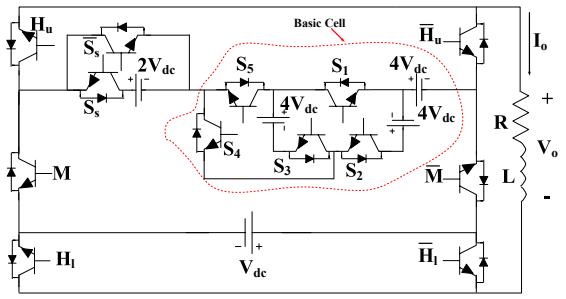
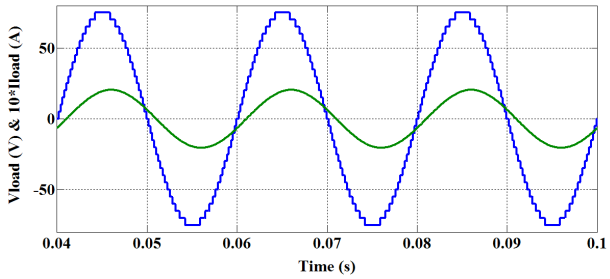


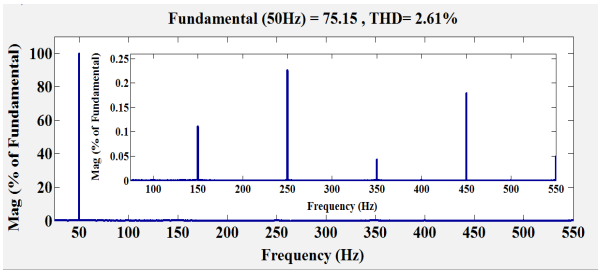
Fig. 6. Circuit diagram of asymmetric 31-Level multilevel inverter

Table 4 illustrates the switching states of the 31-level suggested inverter. The voltage and current waveform of the simulated 31-level inverter are shown in Fig. 7 a. From Fig. 7b, it can be obtained that the output THD for voltage waveform is about 2.61 %, and also the harmonic spectrum is shown in Fig. 7 b.

As it can be seen, all the voltage levels can be generated in the suggested inverter which validates the practicability of the proposed inverter.



(a)



(b)

Fig. 7. a) Voltage and current waveforms and b) harmonics content of voltage of the proposed 31-level inverter

To confirm the feasibility of the suggested multilevel inverter, the measured output voltage and current waveforms of implemented single phase prototype of the asymmetric 31-level proposed inverter are shown in Fig. 8 (b) and (c).

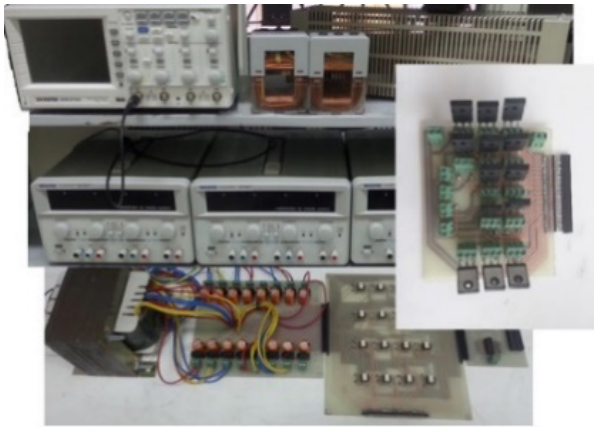
As it can be seen, the provided results confirm that the proposed inverter is able to generate the desired output voltage waveform. These Figs. show good agreements in the simulation and experimental results. The negligible difference between the magnitudes of the simulation and experimental results is due to the voltage drops on switches in the prototype.

Table 4. Switching states of proposed asymmetric 31-level inverter

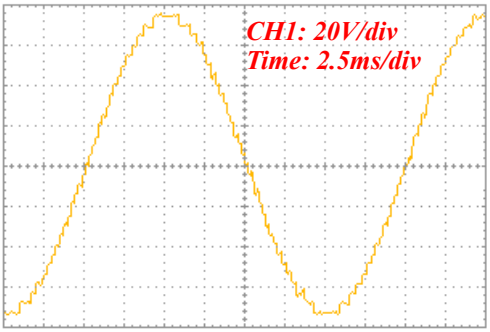
Output Voltage	HL	M	S1	S2	S3	S4	S5	Ss	Hu
$15V_{dc}$	1	0	0	1	1	0	1	1	1
$14V_{dc}$	0	0	0	1	1	0	1	1	1
$13V_{dc}$	1	0	0	1	1	0	1	0	1
$12V_{dc}$	0	0	0	1	1	0	1	0	1
$11V_{dc}$	1	0	0	1	0	1	1	1	1
$10V_{dc}$	0	0	0	1	0	1	1	1	1
$9V_{dc}$	1	0	0	1	0	1	1	0	1
$8V_{dc}$	0	0	0	1	0	1	1	0	1
$7V_{dc}$	1	0	1	0	1	0	1	1	1
$6V_{dc}$	0	0	1	0	1	0	1	1	1
$5V_{dc}$	1	0	1	0	1	0	1	0	1
$4V_{dc}$	0	0	1	0	1	0	1	0	1
$3V_{dc}$	1	0	1	0	1	1	0	1	1
$2V_{dc}$	0	0	1	0	1	1	0	1	1
V_{dc}	1	0	-	-	-	-	-	-	0
0	0	0	-	-	-	-	-	-	0/1 1 - - - - - - 1
$-V_{dc}$	0	1	-	-	-	-	-	-	1
$-2V_{dc}$	1	1	1	0	1	1	0	1	0
$-3V_{dc}$	0	1	1	0	1	1	0	1	0
$-4V_{dc}$	1	1	1	0	1	0	1	0	0
$-5V_{dc}$	0	1	1	0	1	0	1	0	0
$-6V_{dc}$	1	1	1	0	1	0	1	1	0
$-7V_{dc}$	0	1	1	0	1	0	1	1	0
$-8V_{dc}$	1	1	0	1	0	1	1	0	0
$-9V_{dc}$	0	1	0	1	0	1	1	0	0
$-10V_{dc}$	1	1	0	1	0	1	1	1	0
$-11V_{dc}$	0	1	0	1	0	1	1	1	0
$-12V_{dc}$	1	1	0	1	1	0	1	0	0
$-13V_{dc}$	0	1	0	1	1	0	1	0	0
$-14V_{dc}$	1	1	0	1	1	0	1	1	0
$-15V_{dc}$	0	1	0	1	1	0	1	1	0

6- Conclusion

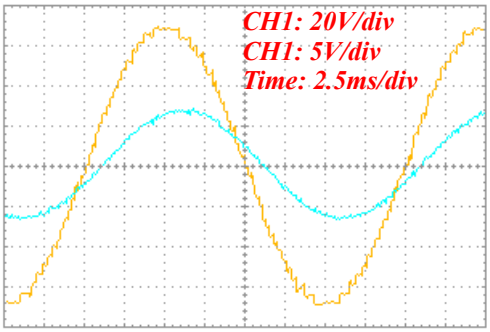
The main purpose of this paper is to propose a new configuration for the symmetric and asymmetric multilevel voltage source inverters. Also, several different algorithms have been proposed in order to calculate the required magnitudes of DC voltage sources for the proposed asymmetric inverter structure. This modular structure reduces the requirements for power semiconductor switches, diodes, IGBTs, gate driver circuits of switches and DC voltage sources in comparison with the previously introduced MLIs. The provided comparison study among suggested inverter, CHB



(a)



(b)



(c)

Fig. 8. a) Visible Hardware of the implemented prototype; and Experimental results of implemented 31-level proposed inverter: b) Output voltage (no load) and c) Output voltage and current (3ohm resistance voltage)

and the recently proposed converters shows the superiority of the proposed inverter over the mentioned topologies. To implement the inverter circuit, the lower number of required devices results in substantial reduction in the total costs and installation area, higher reliability and simpler control scheme. To confirm the practicability of the proposed topology, a prototype of the proposed structure has been implemented. Finally, simulation and experimental results are compared with each other, and the provided comparison shows that the obtained results are in good agreements.

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