Systematic Design of the Lead-lag Network Method for Active Damping in *LCL*-Filter Based Three Phase Converters

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***Abstract*— Three-phase active rectifiers guarantee sinusoidal input currents and unity power factor at the price of a high switching frequency ripple. To adopt an *LCL*-filter, instead of an *L*-filter, allows using reduced values for the inductances and so preserving dynamics. However, stability problems can arise in the current control loop if the present resonance is not properly damped. Passive damping simply adds resistors in series with the *LCL*-filter capacitors. This simplicity is at the expense of increased losses and encumbrances. Active damping modifies the control algorithm to attain stability without using dissipative elements but, sometimes, needing additional sensors. This solution has been addressed in many publications. The lead-lag network method is one of the first reported procedures and continues being in use. However, neither there is a direct tuning procedure (without trial and error) nor its rationale has been explained. Thus, in this paper a straightforward procedure is developed to tune the lead-lag network with the help of software tools. The rationale of this procedure, based on the capacitor current feedback, is elucidated. Stability is studied by means of the root locus analysis in *z*-plane. Selecting the lead-lag network for the maximum damping in the closed-loop poles uses a simple optimization algorithm. The robustness against the grid inductance variation is also analyzed. Simulations and experiments confirm the validity of the proposed design flow.**

***Index Terms*— voltage-source converter, rectifier, Active damping, *LCL*-filter, stability, lead-lag.**

I. Introduction

THREE phase voltage source converters guarantee sinusoidal currents and unity power factor resulting suitable for distributed power generation [1],[2] and smart grid environments [3]. However, this is at the price of a high frequency switching ripple [4]. The use of *L*-filters to limit the harmonic current injection to the grid calls for large and heavy inductors [5]. This may also lead to increased losses due to the large voltage drops and even to a poor dynamic response [5]. In contrast, to adopt *LCL*-filters allow using reduced values for the inductances. However, stability problems can easily arise in the current control loop if the present resonance in the *LCL*-filter is not properly damped.

Passive damping consists of adding resistors in series with the *LCL*-filter capacitors [6]-[8]. The design is simple and no changes needed in the control software. Nonetheless, the damping resistor increases the encumbrances and the losses could claim for forced cooling [6]. Therefore, the efficiency decrease becomes a key point. In addition, the *LCL*-filter effectiveness decreases for increasing damping resistor values [5].

Active damping modifies the control algorithm in order to attain system stability without using dissipative elements [6]. Damping losses are avoided at the expense of increased control complexity and, sometimes, additional sensors. This solution has been addressed in many publications [6]-[27]. Ref. [9] proposes to add a derivative action based on the grid current in the current control loop. Thus, additional current sensors are needed. In [10],[11] the *LCL*-filter capacitor current, which requires new sensors, or equivalently the capacitor voltage derivative is fed back to the converter voltage reference. The same approach is used in [12] but using a lead-lag network instead of the pure derivative. In [13] the capacitor voltages are estimated and delivered to high pass filters. The method of the virtual resistor, proposed in [14], modifies the control algorithm to make the system behave as if there was a damping resistor without physically adding it. This approach requires an additional sensor for each connected virtual resistor [15],[16]. Several strategies are proposed in [17],[18] based on nested loops with the grid current as the most exterior control variable. New sensors are necessary and each nested loop reduces the achievable bandwidth and increases the computation time. An interesting method consists in plugging-in a filter, directly in cascade to the main controller, to damp the unstable dynamics. This approach was initially employed with notch filters tuned by means of genetic algorithms in [19] and later was systematically studied in [20].

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The active damping method of the lead-lag network was initially proposed in [12]. However, it was not explained why to use such a network and how to choose its time constants. In [6] the lead-lag network was tuned to have the maximum lead angle at the resonance frequency. The selection of the maximum lead angle did not take into account the presence of the computational and PWM delays. Conversely, in [21] the lead-lag network is used to compensate the computational and PWM delays in the feed forward of the capacitor voltage but the resonance effects were not considered. Recently the lead-lad network method was used with paralleled grid-connected inverters in photovoltaic plants that are coupled due to grid impedance [22]. An interesting model to describe the totality of the parallel inverters was developed but no new considerations about the lead-lag network tuning were provided. Finally, although the rationale behind the lead-lad network method is intuited to be related with the feedback of the capacitor voltage derivative [23] no explicit derivation has been shown until now.

Hence, although the lead-lag network method is one of the first reported methods of active damping [12] and it is currently dealt in the literature [22],[24], hitherto, there is neither a tuning procedure without resorting to trial and error [25] nor its rationale has been clearly explained. Therefore, the main purpose of this article is to develop a straightforward tuning procedure for the lead-lag network with the help of software tools. In doing this, the rationale of this active damping procedure, based on the capacitor current feedback, is elucidated. This allows obtaining the proper value for the maximum angle of the lead-lag network. The lead-lag network gain is obtained by the use of z-plane root locus design, where the degree of system damping is easily obtainable. The PI controller parameters for the current loops are obtained by means an equivalent model for low frequency. A design flow describing the algorithm for rapid obtaining all the necessary parameters is provided. In addition, an analysis of the robustness against the grid inductance variation is realized.

This paper models first the *LCL*-filter based converter. Next, the tuning procedure of the lead-lag network for active damping is explained. Finally, simulations and experimental results confirm the validity of the proposed design procedures.

II. Modeling And Control Of Three Phase Converter

A. Modeling of the LCL*-filter based converter*

Fig. 1 shows the *LCL*-filter based three-phase converter. In an industrial converter, the current sensors are integrated on the converter side as they are also used for protection [4]. Hence, in this paper the converter current will be sensed [26]. Neglecting the parasitic resistances in all the *LCL*-filter elements, the transfer function relating to the converter voltage, *v*, and the converter current, *i*, is [6]:

$$G_{ud}(s)=\frac{i(s)}{v(s)}=\frac{1}{Ls}\frac{s^2+z_{LC}^2}{s^2+\omega_{res}^2} \tag{1}$$

where $z_{LC}^2=(L_gC_f)^{-1}$ and the resonance frequency is $\omega_{res}^2=(2\pi f_{res})^2=(1+L_g/L)z_{LC}^2$ [6]. The transfer function relating to the grid current, i_g, and the converter voltage, *v*, is [4]:

$$G_{gud}(s)=\frac{i_g(s)}{v(s)}=\frac{1}{Ls}\frac{z_{LC}^2}{s^2+\omega_{res}^2} \tag{2}$$

A slope of 60 dB/decade for $\omega>>\omega_{res}$ in (2) will highly attenuate the grid current harmonics. Thus, the switching frequency should be selected larger than ω_{res} in the *LCL*-filter design stage.

When considering real coils (1) and (2) have finite DC gain equal to the sum of *R* and R_g, the parasitic converter and grid coil resistances respectively.

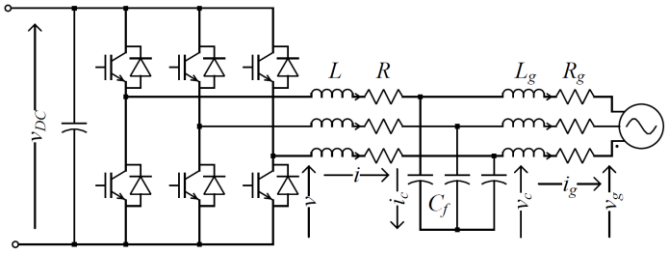

Fig. 1. *LCL*-filter based three-phase converter.

The *LCL*-filter based converter uses the same digital PI controllers for the current loops as the *L*-filter based converter [27]. In doing so, the complexity of the control algorithm is not increased by using an *LCL*-filter. The usual criterion for tuning the PI controllers is the technical optimum [28]. The tuning formulas are given for the *L*-filter plant with transfer function of first order [28]. The transfer function of the *LCL*-filter (1) is linear but has elevated order. Thus, an equivalent model for low frequency of the *LCL*-filter allows using the simple formulas established for the *L*-filter. This can be used because, as will be shown, the *LCL*-filter resonance affects only to the region of frequencies much higher than current control bandwidth.

The Padé approximant [29] can be used to obtain the *LCL*-filter equivalent model for low frequency. The Padé approximant $p_{N,M}(x)$ of a function $f(x)$ consists in a quotient of two polynomials with numerator degree *N* and denominator degree *M*. Taylor series expansion of Padé approximant $p_{N,M}(x)$ equals to Taylor series expansion of $f(x)$ up to degree $M+N$ [29]. The Padé approximant $p_{N,M}(s)$ of (1) with $N=0$ and $M=1$, having into account parasitic coil resistances, is as follows:

$$p_{0,1}(s)=\frac{1}{\left(L+L_g-C_f R_g^2\right)s+\left(R+R_g\right)}=\frac{1}{L_{eq}s+R_{eq}} \approx \frac{1}{\left(L+L_g\right)s+\left(R+R_g\right)} \quad (3)$$

Factor $C_f R_g^2$ in (3) is negligible when compared to $L+L_g$ as R_g is one order of magnitude lower than $\omega_f L_g$, with ω_f the fundamental frequency, and C_f is selected not to decrease power factor more than 5% [5]. This shows that the equivalent model for low frequency is approximately equivalent to eliminate the capacitor branch in the *LCL*-filter as was done in [5].

B. Control of the equivalent model for low-frequency

Converter control is studied using the space vector notation and an average model in the *dq*-frame rotating at grid frequency ω [5]-[6],[30]. Fig. 2 shows the inner and faster loops controlling the *dq*-currents and the outer and slower loop controlling the *DC*-link voltage [4]. The cascaded control structure for the *LCL*-filter based converter is exactly the same as that of the *L*-filter based converter except for the active damping block. The active damping block of Fig. 2 is shown enclosed in the dashed lines and will be explained in the following section.

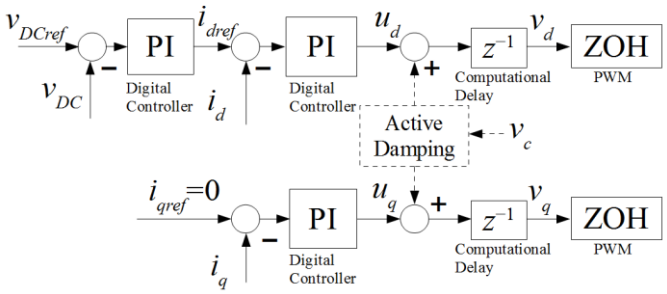

Fig. 2. Block diagram of the digital control for the *LCL*-filter based rectifier (the active damping is shown enclosed in dashed lines).

A digital processor performing all control tasks has the sampled measurements as inputs and the PWM gate pulses as outputs. For control modeling purposes, the PWM modulator can be regarded as a zero order hold (ZOH) [31]. Thus, the control plant will be the ZOH equivalent of the transfer function (1) relating to *v* and *i* considering the parasitic coil resistances.

The parameters for the digital PI controller according to the technical optimum criterion are [28] (damping factor of dominant pole pair ζ_{lf}=0.707 for 4% overshoot):

$$K_p=\frac{L_{eq}}{3T_s} \quad (4)$$

$$T_i=\frac{L_{eq}}{R_{eq}} \quad (5)$$

where T_s is the sampling period. Simple update mode is used i.e. the sampling of all the measurements is done at the beginning of each PWM period and the update of all the outputs (PWM registers) at the ending [28],[32]. Hence, T_s=T_{sw} where T_{sw} is the switching period.

The analysis to obtain (4) and (5) was done in the continuous-time domain by modeling the computational and PWM delays as a first order system with time constant τ=1.5T_s [28]. This approximation is valid because the attained bandwidth (6) is much lower than the sampling frequency:

$$\omega_{bw}=\frac{K_p}{L_{eq}} \quad (6)$$

In order to avoid interference the resonance frequency ω_{res} should be selected larger than ω_{bw} in the *LCL*-filter design stage [5].

The parameters R_{eq} and L_{eq} of the equivalent model for low-frequency are substituted in (4) and (5) for the digital PI controllers of the current loops in the *LCL*-filter based converter. Nevertheless, the additional zeros and poles in (1) can make the system unstable if the proper damping is not applied [5].

The digital PI controller for the *DC*-link voltage is usually adjusted following the symmetrical optimum criterion [28] and taking into account the inner and faster *d*-current control.

III. Active Damping Design

A. Rationale of the procedure

Active damping can be achieved by using a proper feedback state. Thus, the feedback of the current through the *LCL*-filter capacitors yields resonance damping [10]. Fig. 3 illustrates this concept with the negative feedback of the *LCL*-filter capacitor current to the converter voltage reference [10],[33]. Assuming ideal feedback, now the transfer function relating to i_g and voltage *u*, converter current PI controller output, results in:

$$G_{gad}(s)=\frac{i_g(s)}{u(s)}=\frac{1}{Ls}\frac{z_{LC}^2}{s^2+\underbrace{2\left[\frac{k_d}{2L\omega_{res}}\right]}_{damping}\omega_{res}s+\omega_{res}^2} \quad (7)$$

The proportional gain k_d is related to the damping factor ζ_{ad} as follows:

$$\zeta_{ad}=\frac{k_d}{2L\omega_{res}} \quad (8)$$

Unlike the passive damping case, the transfer function (7) does not have a zero that degrades the *LCL*-filter effectiveness [34]. Hence, as was observed in [6], increasing the gain k_d to increase the damping will not incur increasing the grid current ripple. According to (8) the gain k_d will have the same order of magnitude as twice the inverter coil impedance at the resonant frequency $2L\omega_{res}$ since $0<\zeta_{ad}<1$. The transfer function relating to i and u is [34]:

$$G_{ad}(s)=\frac{i(s)}{u(s)}=\frac{1}{Ls}\frac{\left(s^2+z_{LC}^2\right)}{s^2+\underbrace{2\left[\frac{k_d}{2L\omega_{res}}\right]}_{damping}\omega_{res}s+\omega_{res}^2} \tag{9}$$

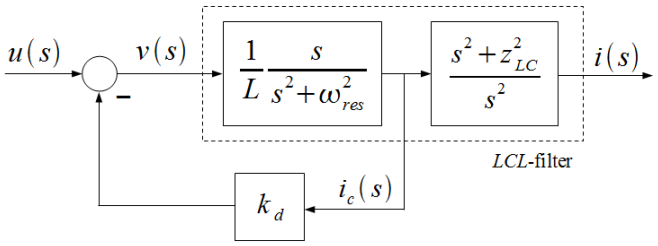

Fig. 3. *LCL*-filter capacitor current feedback to obtain damping.

In order to avoid the use of new current sensors [34]-[35] the *LCL*-filter capacitor current i_c can be estimated from the derivative of the *LCL*-filter capacitor voltage v_c [33], see Fig. 4, as follows:

$$H_d(s)=\frac{i_c}{v_c}=k_dC_fs \tag{10}$$

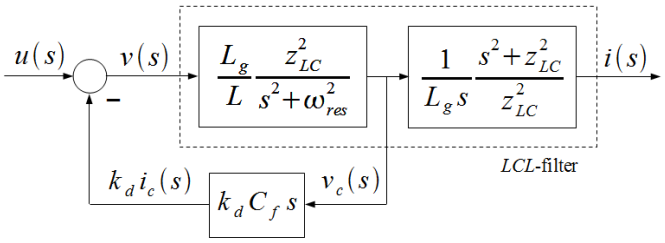

Fig. 4. Feedback of the capacitor voltage derivative to obtain damping in the *LCL*-filter.

B. Minimum gain for stability

Considering the open-loop transfer function of the converter current control in the continuous-time domain:

$$G_{adol}(s)=G_{PI}(s)G_{delays}(s)G_{ad}(s) \tag{11}$$

where $G_{ad}(s)$ is the plant (9), $G_{delays}(s)$ is a pure delay $e^{-1.5T_ss}$ modeling the computational and PWM delays, and finally $G_{PI}(s)$ is the PI controller tuned according to (4) and (5). The frequency that corresponds to −180º phase-shift for the open-loop transfer function is near the resonant frequency [6], [12]. The resonant peak should be below unity (0 dB) [12] for the current control to be stable by achieving a positive gain margin. Thus, the minimum k_{dmin} (considered as a variable parameter) for stability can be obtained by equating the open-loop transfer function to unity (0 dB) at the resonance frequency ($s=j\omega_{res}$):

$$\left|G_{adol}(s)\right|_{s=j\omega_{res}}=\left|G_{PI}(s)G_{delays}(s)G_{ad}(s)\right|_{s=j\omega_{res}}=1 \tag{12}$$

Substituting and solving in (12) and neglecting the smaller terms results in:

$$k_{dmin}=\frac{1}{3}\frac{L_g}{T_s} \tag{13}$$

C. Lead-lag network tuning

A perfect differentiator for the capacitor voltage would amplify the measurement signal noise too much and thus, a lead-lag network should be used instead, see Fig. 5.

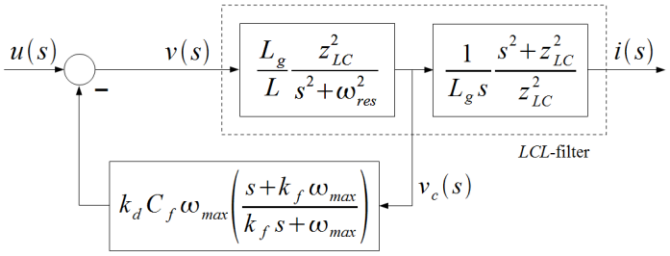

Fig. 5. Feedback of *LCL*-filter capacitor voltage filtered by a lead-lag network to obtain damping.

A proper form for the lead-lag network consists of the following transfer function:

$$H_{ll}(s)=k_dC_f\omega_{max}\left(\frac{s+k_f\omega_{max}}{k_fs+\omega_{max}}\right)\ \text{with}\ k_f=\sqrt{\frac{1-\sin\varphi_{max}}{1+\sin\varphi_{max}}} \tag{14}$$

where $\omega_{max}=2\pi f_{max}$ is the frequency for the maximum phase shift φ_{max} ($|\varphi_{max}|<90^o$), see Fig. 6.

The lead-lag network behaves as a differentiator at frequencies around the resonance frequency, where damping is necessary, by selecting φ_{max} close to 90º and in addition:

$$\omega_{max}=\omega_{res} \tag{15}$$

By doing this, (14) has for $\omega=\omega_{res}$ an amplitude equal to $k_dC\omega_{res}$ a phase close to 90º with zero slope just like in (10). The amplitude slope of (14) for $\omega=\omega_{res}$ is:

$$\left.\frac{d\left|H_{ll}(j\omega)\right|}{d\omega}\right|_{\omega=\omega_{res}}=k_dC_f\left(\frac{1-k_f^2}{1+k_f^2}\right) \tag{16}$$

Eq. (16) is close to the amplitude slope of (10) for $\omega=\omega_{res}$

equal to k_dC_f, see Fig. 6, if k_f<1 ($0<\varphi_{max}<90^o$). Indeed, k_f should be as small as possible (φ_{max} as close to 90º as possible). If k_f>1 ($-90^o<\varphi_{max}<0$) the amplitude slopes of (14) and (10) have different signs for $\omega=\omega_{res}$, see Fig. 6, and the lead-lag network no longer behaves as a differentiator.

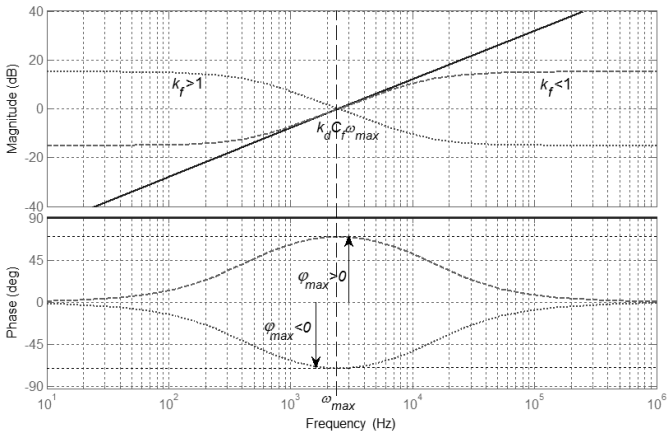

Fig. 6. Bode diagram of the perfect differentiator in (10) and the lead-lag network in (14) for k_f>1 and k_f<1.

The lead-lag network for active damping is implemented in the digital controller, see Fig. 7. The synchronous sampling of the capacitor voltage requires symmetry in the PWM pulse to obtain a ripple free waveform and so simple update mode ($T_s=T_{sw}$) is only used.

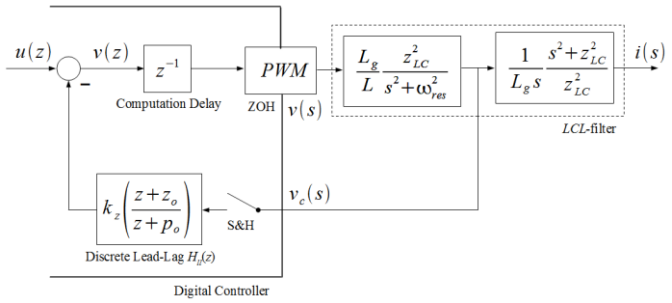

Fig. 7. Implementation of the lead-lag network for active damping in the digital controller.

The digital implementation [36]-[37] incorporates lag phase shifts due to the presence of the computational delay and the PWM. To calculate these lag phase shifts the computational delay is modeled as a pure delay of T_s and the PWM, equivalent to a ZOH, as a pure delay of $0.5T_s$ [28]. This approximation results in adequate accuracy for frequencies much lower than f_s.

The discrete lead-lag network must behave as a perfect differentiator around the resonance frequency. Hence, the phase shift at the resonance frequency must lead 90º once the phase shifts due to the PWM and the computational delays are compensated:

$$90^o=\varphi_{max}-\underbrace{1.5T_s\omega_{res}\frac{360}{2\pi}}_{\text{PWM and computational delays}} \tag{17}$$

In order to preserve the phase and amplitude characteristics at the resonance frequency (14) must be discretisized by using the bilinear transformation (Tustin method) with pre-warping at $\omega=\omega_{res}$ [6], [39]. The discrete equivalent of (14) has the form $k_z(z+z_o)/(z+p_o)$ with k_z a gain, z_o a zero and p_o a pole.

The sampling frequency to get k_f<1, which corresponds to $0<\varphi_{max}<90^o$ (14), is $1.5f_{res}<f_s<2f_{res}$ according to (17). However, the digital control requires the resonance frequency to be lower than the Nyquist frequency so $f_s>2f_{res}$ [39]. If the gain k_d in (14) is selected negative, a phase lag of 180º must be added in (17). This results in k_f<1, $0<\varphi_{max}<90^o$ (14), for $3f_{res}<f_s<6f_{res}$ (17), which fulfills the previous condition $f_s>2f_{res}$. A negative gain k_d in (14) is coherent with the original formulation of the lead-lag method [12], which used positive feedback of the capacitor voltage filtered by the lead-lag network. The switching frequency f_{sw} should be selected as low as possible to reduce the switching losses [38]. As $f_{sw}=f_s$ then f_s should be selected as close to $3f_{res}$ as possible. It is not possible to make $f_s=3f_{res}$ as this corresponds to $\varphi_{max}=90^o$ and (14) would result in a pure derivative. A practical upper limit is $\varphi_{max}=80^o$ [6], corresponding to $f_s=3.2f_{res}$ (17). In addition, there is a lower limit $\varphi_{max}=70^o$, corresponding to $f_s=3.4f_{res}$ (17), to make (16) close (>90%) to the perfect differentiator slope. Hence, the frequency ratio should be selected in the following range:

$$\frac{f_s}{f_{res}}\approx 3.2\div 3.4 \tag{18}$$

The approximation for the computational and PWM delays used in (17) is valid for the ratios according to (18). Indeed, the achieved bandwidth for the current control according to (6) for the ratio (18) is approximately $f_{bw}\approx f_{res}/5$. Hence, the resonance does not affect very much to the current control that can be safely tuned using the equivalent model for low frequency.

Root locus analysis in the *z*-plane, considering the discrete nature of the employed digital control, is used to select the gain k_d that results in an adequate damping of the closed-loop poles. The gain k_d cannot be arbitrarily increased to get a very high damping as the system becomes unstable [6].

D. Equivalent model for low-frequency

At low and high frequencies where damping is not necessary, $\omega<<k_f\omega_{max}$ and $\omega>>\omega_{max}/k_f$, (14) behaves as a constant, $H_{llDC}=k_dC_f\omega_{max}k_f$ and $k_dC_f\omega_{max}/k_f$ respectively, feeding back the capacitor voltage to the converter voltage reference [10]. This behavior is analogous to use a properly sized coil and capacitor in parallel to the damping resistor. The current bypasses the damping resistor at extreme frequencies

where the passive damping is not necessary [35], [38].

The equivalent model for low frequency of the *LCL*-filter including the lead-lag network by using the Padé approximant results in:

$$L_{eq} = L + L_g\left(1 + H_{lIDC}\right) - C_f R_g^2\left(1 + H_{lIDC}\right) + \frac{R_g H_{lIDC}}{\omega_{res}}\left(\frac{1}{k_f} - k_f\right) \quad (19)$$

$$\approx L + L_g\left(1 + H_{lIDC}\right)$$

$$R_{eq} = R + R_g\left(1 + H_{lIDC}\right) \quad (20)$$

The equivalent resistance and inductance from (19) and (20) are to be substituted in (4) and (5) for the digital PI controller of the converter current.

E. Overshoot reduction

The gain K_p in (4) was selected only having into account the equivalent model for low frequency. The high frequency behavior of the *LCL*-filter and the equivalent notch filter produces higher overshoot to the step input than the expected 4% [6]. Half K_p in (4) would make the closed-loop dominant poles critically damped (ζ_{lf}=1) and the only present overshoot would be due to the high frequency dynamics. So if overshoot is not acceptable K_p should be reduced, but not as much as halving (4), until obtaining acceptable overshoot. Nevertheless, this solution would be at the expense of reducing the overall bandwidth according to (6).

F. Design flow

Fig. 8 shows the step-by-step procedure for the active damping design of the *LCL*-filter based rectifier.

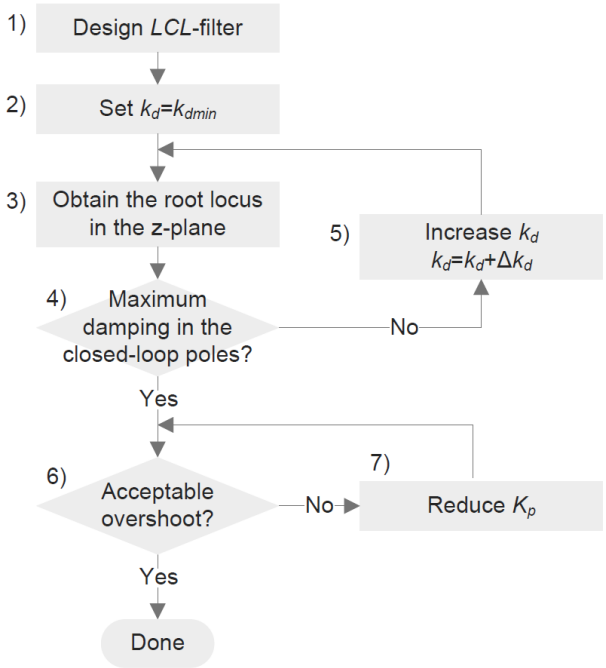

Fig. 8. Design flow for the active damping design of the *LCL*-filter based rectifier.

For the step 1) the guidelines proposed in [4],[5] can be used. The switching frequency is selected according to (18). The gain k_d with the poles entering in the unit circle of the root locus (minimum value for stability) will be near k_{dmin} (13), initial value of the step 2). Several times (9) can be used as the maximum k_d. The digital PI controllers are tuned according to (4),(5) by using the equivalent model for low frequency (19),(20). In the steps 3), 4) and 5) the gain k_d is progressively increased until obtaining the optimum value corresponding to the maximum damping of the closed-loop poles.

The maximum value is detected by observing a reduction in the damping for an increase in the gain k_d. This simple optimization algorithm is known as hill-climbing [40]. The increment length for the step 5) is initially selected according to (8) $\Delta k_d = 2L\omega_{res}\Delta\zeta_{ad}$ by considering increments in $\Delta\zeta_{ad}$=1%. A shorter increment $\Delta\zeta_{ad}$ can be selected for greater accuracy at the expense of a larger computation period. These steps are automated by using a scripting language for numerical calculations such as Matlab [29],[39].

IV. Simulation Results

Simulation models have been built using Matlab and Simulink. The *LCL*-filter data are from [5] complying step 1) in the proposed design flows: L_g=5 mH, L=3 mH, and C_f=2.2 μF so f_{res}=2478 Hz. Parasitic coil resistances are chosen to be one order of magnitude less than the coil impedance at fundamental frequency. The converter data are: rated power P_{nom}=4.1 kW, V_{nom}=380 V (rms phase-to-phase), fundamental frequency f_f=50 Hz, *DC*-link voltage V_{DC}=700 V, *DC*-link current I_{DC}=5.5 A (simulated as a simple *DC*-link load resistor), and *DC*-link capacitor C_{DC}=500 μF. Current control loops were equipped with anti-windup mechanisms. The adopted PWM modulation strategy is SVM. A digital *dq*-PLL [32] is used for AC voltage synchronization. Voltage sensors are located across the *LCL*-filter capacitor branch for active damping. Simple update mode is used so T_s=T_{sw}. The simulations are ideal without any non-linear effect (ideal switches, no dead time, no coil saturation and perfect sinusoidal grid voltage).

Active damping according to the proposed design flow is as follows:

Step 1) the *LCL*-filter data were selected from the reference [5]. The selected switching frequency is 8 kHz according to (18), this corresponds to φ_{max}=77.3º according to (14).

Step 2) the optimization algorithm starts for k_d=k_{dmin}. The estimation (13) for the minimum k_d to achieve stability is quite accurate for higher frequencies. This was expected since deducing (13) was based on assuming high switching frequencies. For f_{sw}=8 kHz the calculated minimum gain results k_{dmin}=13.35 and by substituting in (13) k_{dmin}=13.35 Fig. 9 shows the root locus in *z*-plane of the converter current control for increasing gains k_d. It can be seen that the closed-loop poles enter into the unit circle, approximately for k_{dmin}>13.3 according to (13) resulting in stability. The

dominant pole pair follows the lines of constant damping factor ζ_{lf}=0.707 by considering the Padé approximant for the equivalent model according to (19) and (20).

Steps 3), 4) and 5) the gain k_d is progressively increased until obtaining the maximum damping in the closed-loop poles for k_d =27, corresponding to ζ_{cl}>0.15. The optimization algorithm stops at reaching the optimum k_d =27. Notwithstanding, Fig. 9 shows how the system starts to change its dynamics for k_d>27 and tends again to be unstable. Closed-loop poles leave the unit circle for k_d>46 and the system becomes unstable.

Step 6) and 7) the resulting overshoot is 13.5%, more than the expected 4% if not allowable K_p should be reduced. Halving the proportional gain K_p reduces the overshoot to zero. Decreasing the gain to 85% K_p reduces the overshoot to below 4% at the expense of decreasing the bandwidth according to (6).

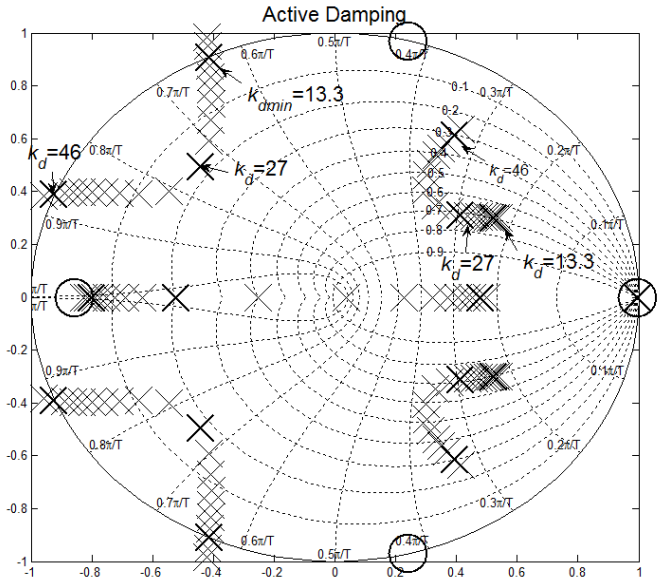

Fig. 9. Closed-loop poles in the *z*-plane of the converter current control by varying k_d for the active damping case.

Grid currents obtained from simulation for k_d=27 resulted in very clean waveforms with THD=0.6%. Fig. 10 shows the root locus in *z*-plane of the converter current control by varying the grid inductance due to variations in the line impedance. The real grid impedance L_{grid} varies between 50-150% of the considered inductance value L_g. It can be seen that increasing values of the real grid inductance result increasing damping of the closed-loop poles and vice versa. This was expected from (8) as the achieved damping factor for the calculated k_d increases as the resonance frequency decreases and vice versa.

It can also be seen that for decrements in the real grid inductance L_{greal}=55%L_g with $\Delta\omega_{res}$=14%ω_{res} the system enters instability but for increments L_{greal}=155%L_g with only $\Delta\omega_{res}$=–7%ω_{res} the system remains stable. This is because the *LCL*-filter is designed to have L_g/L>1 [4] so elevated increments in the grid inductance are necessary to significantly reduce the resonance frequency (negative $\Delta\omega_{res}$). Indeed, as the resonance frequency separates from the considered one for (14), the lead-lag network detaches from its behavior as differentiator and the active damping loses its efficacy. Thus, the active damping procedure is more sensitive to decrements in the real grid inductance and in case of uncertainty; it would be advisable to underestimate L_g. Finally, the PI controllers will result in higher overshoots (less damping of the dominant poles) for the decreasing values of the real grid inductance and vice versa.

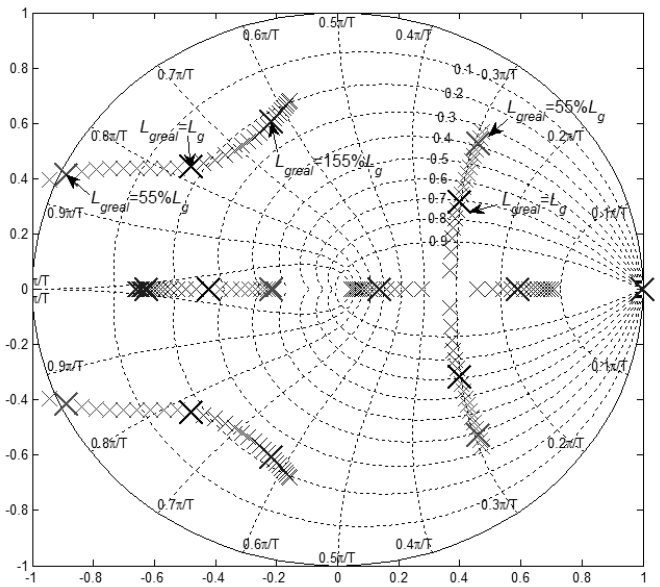

Fig. 10. Closed-loop poles in the *z*-plane of the converter current control by varying the grid inductance for the active damping case.

V. Experimental Results

One of the advantages of Simulink is the capability to generate code for the implantation (DSP [41] or FPGA [42]) directly from the block diagrams [43]. This feature eliminates the tedious and error prone task of hand coding the control algorithm. However, the proposed procedures use the standard nested structure of Fig. 2 for the rectifier control [32] and so all the already available code can be reutilized. Therefore, the only necessary new code is for active damping block of Fig. 2. Due to its superior numerical properties, it is recommended to use the direct form II transposed structure [44] to implement the discrete lead-lag network. The code for the discrete lead-lag networks is incorporated to the PWM interrupt service routine [32] and so its execution is scheduled in the same slot [45] as the current control loop.

The experimental setup, see Fig. 11, consists of a 2.2 kW Danfoss FC302 converter connected to the grid through an isolation transformer and supplied by Delta Elektronika power supplies. The setup parameters are shown in Table I.

The resonance frequency is f_{res}=2385 Hz and the maximum angle is φ_{max}=71º according to (14). The maximum damping for closed-loop poles results in k_d=13. The measured waveforms for *LCL*-filter capacitor voltage and grid current

upon the connection of the lead-lag network are shown in Fig. 12. Thus, the experiment confirms the stability and correctness of the proposed tuning procedure.

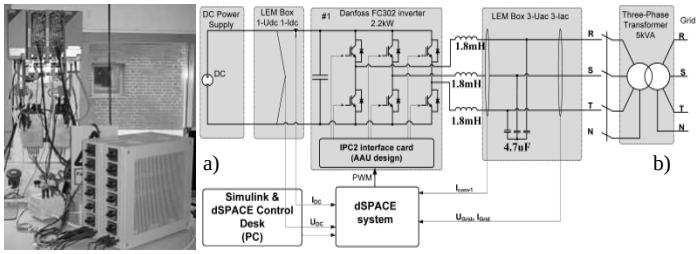

Fig. 11. The laboratory setup: a) photo of setup; b) hardware wiring diagram.

TABLE I. PARAMETERS OF THE EXPERIMENTAL SET-UP.

Parameter	Value
Inductance of converter side coil L	1.8 mH
Capacitance of capacitor C_f	4.7 μF
Inductance of grid side coil L_g	2 mH
Switching (sampling) frequency	8 kHz
DC voltage	650 V
Active power	2 kW
Reactive power	0 VAr

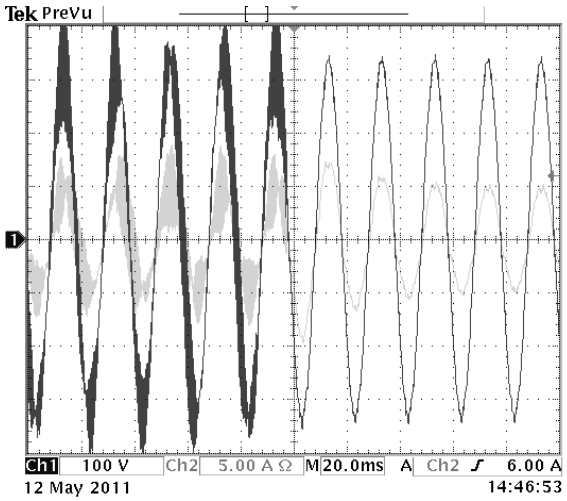

Fig. 12. Measured capacitor voltage (100 V/div) and grid current (5 A/div) upon the connection of the lead-lag network.

VI. CONCLUSION

This paper is intended as a guide to systematic design of the lead-lag network method for active damping in *LCL*-filter based three phase converters. The capacitor current feedback to voltage references constitutes the rationale of the method. This allows explaining the parameter tuning by means of unsophisticated linear techniques. Root locus analysis in z-plane is necessary to assess stability in selecting the lead-lag network gain. A simple optimization algorithm is used to select lead-lag network corresponding to the maximum damping in the closed-loop poles. Simulation and experiments confirm the validity of the proposed design flow. Hence, the parameters of the lead-lag network method for active damping are calculated without recurring to trial-and-error iterations. This procedure is limited to simple update mode with the narrow range for the switching frequency. Future research should study the underlying notch nature of the lead-lag network method to tune the notch filter directly inserted in the controller path.

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