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Investigation on Metal–Oxide Graphene Field-Effect Transistors With Clamped Geometries

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ABSTRACT In this work, we report on the design, fabrication and characterization of Metal-Oxide Graphene Field-effect Transistors (MOGFETs) exploiting novel clamped gate geometries aimed at enhancing the device transconductance. The fabricated devices employ clamped metal contacts also for source and drain, as well as an optimized graphene meandered pattern for source contacting, in order to reduce parasitic resistance. Our experimental results demonstrate that MOGFETs with the proposed structure show improved high frequency performance, in terms of maximum available gain and transition frequency values, as a consequence of the higher equivalent transconductance obtained.

INDEX TERMS Graphene, metal-oxide graphene field-effect transistors (MOGFETs), microwave transistors, clamped geometries, meandered graphene contacts.

I. INTRODUCTION

The ever increasing performance requirements in high-frequency electronics have pushed Silicon-based Field Effect Transistors (SiFETs) technology to scale down geometries to the limit [1], [2]. However, this aspect has produced serious drawbacks, known as short channel effects [3]. To avoid such issues, different techniques have been adopted, e.g., reducing the gate oxide thickness, lowering the source/drain junction depth, increasing the channel doping [4], [5]. In particular, promising results have been achieved in this research field, especially thanks to the design and fabrication of double gate device structures [6], [7]. The same approach could also be adopted in the fabrication of novel transistors employing new nanomaterials. Due to the high charge carrier mobility, huge current density and low contact

resistance [8]–[10], graphene has been adopted for various fields of application such as optoelectronics [11]–[14] and high-frequency electronics [15]–[17]. Large area growth of graphene by chemical vapor deposition (CVD) has been achieved [18], with quality comparable to that of exfoliated flakes [19] and suitable for wafer-scale integration [20]. Concerning graphene high-frequency electronics, Metal Oxide-Graphene Field-Effect Transistors (MOGFETs) have already demonstrated excellent performance in RF/Microwave regime [15], [21]–[27]. Also graphene transistors with double gate have already been studied readily in several research works (e.g., [25], [28]–[31]). In our previous works, we carried out an in-depth statistical study of Metal-oxide Graphene Field-effect Transistors (MOGFETs) aimed at experimentally evaluating

the dependence of microwave parameters on the devices dimensions [32] and on the dielectrics employed as gate layer [33]. We also investigated the possibility of employing MOGFETs specifically designed for microwave applications to sense infrared radiation [34]. In this work, we instead focus on the design, fabrication and characterization of MOGFETs with clamped-gate structures. In detail, we have designed and fabricated MOGFETs with clamped local gate structures aimed to obtain, for a given gate dielectric thickness, a more efficient channel modulation and a higher transconductance. The proposed structure also presents a clamped geometry for both source-drain contacts [35] and an optimized graphene meandered pattern for source contacting [36] to decrease parasitic resistance. A comparative study has been carried out showing the increase of high-frequency performance of MOGFETs employing our structure with respect to single-gate devices having the same channel length and width and the same oxide thickness.

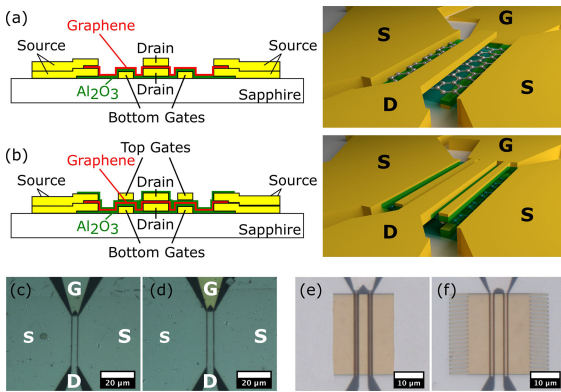


FIGURE 1. Cross-section and tridimensional sketch of single-gate (a) and clamped-gate MOGFET (b). Optical micrographs of single-gate (c) and clamped-gate (d) fabricated devices. Optical micrographs of the PMMA mask for the (e) not meandered and for the (f) meandered graphene.

II. DEVICES FABRICATION

The clamped geometries have been designed to improve MOGFETs performance increasing the device transconductance (g_m) without significantly influencing gate leakage, output conductance and reactive parasitic elements. Two different geometries have been used with the same gate length (500 nm) and channel length (850 nm): the first one (Fig. 1a) consists of a MOGFET with a single back gate, while the second one shows a clamped gate (Fig. 1b). To obtain better DC and RF performance, both structures were fabricated using double source/drain contacts [35]. In order to reduce parasitic resistances [37]–[39], meandered graphene contacts [36] devices have been fabricated following the technological steps illustrated in Fig. 1, and then compared with the standard ones. First, the dual-finger back-gate has been patterned on a sapphire substrate [40], [41] by e-beam lithography followed by the evaporation of Ti/Au bilayer ($\sim 5/20$ nm) and lift-off in acetone. A 8 nm thick Al_2O_3

film has been directly grown via atomic layer deposition at 90°C as dielectric layer. After the deposition of bottom contacts (Ti/Au $\sim 5/20$ nm), a CVD-grown graphene film has been transferred and etched into rectangular or meandered pattern by Reactive Ion etching (RIE).

Source/drain top electrodes have been patterned onto Graphene sheet via e-beam lithography step followed by a Ti/Au ($\sim 5/25$ nm) deposition. Subsequently, the devices have been covered locally by a second layer of Al_2O_3 (~ 8 nm). In order to fabricate the clamped gate ones, the dual-finger top-gate has been patterned on Al_2O_3 by e-beam lithography, followed by the evaporation of a Ti/Au bilayer ($\sim 5/20$ nm) and lift-off in acetone.

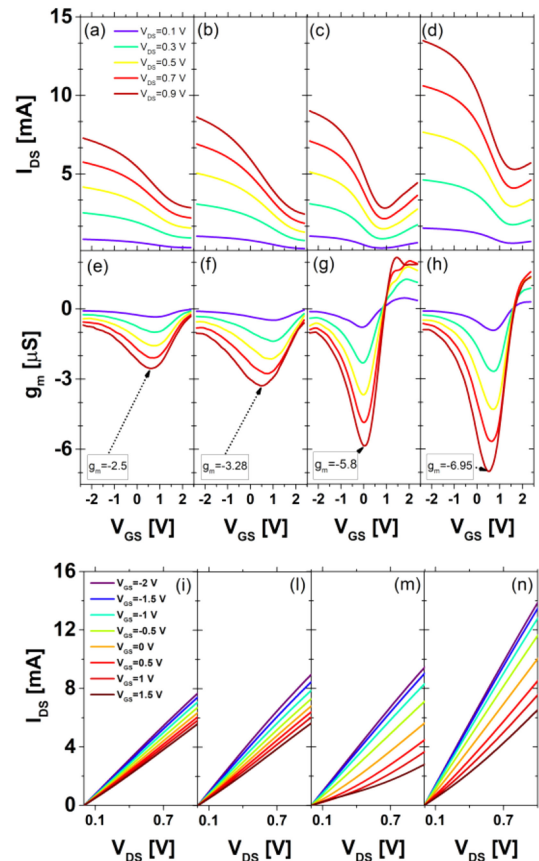


FIGURE 2. Graphs of I_{DS} vs V_{GS} and g_m vs V_{GS} as a function of V_{DS} for: (a, e) single-gate device with not meandered graphene source contacts, (b, f) clamped-gate device with not meandered graphene source contacts, (c, g) single-gate device with meandered graphene source contacts, (d, h) clamped-gate device with meandered graphene source contacts. Graphs of I_{DS} vs V_{DS} with V_{GS} as a parameter for: (i) single-gate device with not meandered graphene source contacts, (l) clamped-gate device with not meandered graphene source contacts, (m) single-gate device with meandered graphene source contacts, (n) clamped-gate device with meandered graphene source contacts.

III. RESULTS AND DISCUSSION

Our MOGFETs have been characterized in the DC regime (Fig. 2). The four types of devices have been compared in terms of drain current I_{DS} (Fig. 2 a-d) and of transconductance (Fig. 2 e-h) vs the gate voltage V_{GS} at varying drain voltages V_{DS} . As reported, for devices with the same gate

and channel length both the ON-OFF ratio and the static g_m increase in case of meandered graphene devices, being this trend even more pronounced in clamped-gate structures, as expected. Measurements of I_{DS} versus V_{DS} at varying V_{GS} (Fig. 2 i-n) demonstrate that clamped-gate devices present a broader spread in the I_{DS} - V_{DS} curves at increasing V_{GS} if compared to single-gate ones. At a given bias voltage, also the meandered devices present a larger I_{DS} than the not-meandered ones, probably due to the lower contact resistance between source and channel. Our characterization has been aimed at evaluating the maximum obtainable performance for RF applications. For this reason, we have explored the ranges of V_{GS} and V_{DS} in order to find the highest value of g_m . Note that the output characteristics in Fig. 2 do not show signs of soft current-saturation (contrarily to what reported, e.g., in [42]) within the studied operating ranges, as high doping has been avoided, since MOGFETs for RF applications need to not work in the saturation region.

Once verified that devices with meandered graphene exhibit better properties in terms of static g_m , we focused only on the meandered devices for the subsequent RF/microwave characterization and modeling.

For each device, the intervals of V_{GS} and V_{DS} with the highest value of g_m have been identified, and then scattering parameters have been measured in the [50 MHz-20 GHz] frequency range using a Cascade Summit 9000 wafer-probe station and an HP8510C Vector Network Analyzer. A standard de-embedding procedure has been applied to extract the intrinsic transit frequency of the transistor [43]. De-embedded S-parameters, short circuit current gain and maximum available gain have been calculated biasing the transistors at the operating points with the maximum transconductance (i.e., $V_{GS} = 2$ V, $V_{DS} = 1.5$ V for a single gate device; $V_{GS} = 1.4$ V, $V_{DS} = 1.5$ V for the clamped gate device), shown in Fig. 3.

The extensive characterization campaign performed permits us to claim that MOGFETs with clamped-gate exhibit better performance in terms of gain, cut-off frequency (f_T) and maximum oscillation frequency (f_{max}). In detail, f_T increased by a factor of 1.22 (from 4.83 GHz to 5.92 GHz), while f_{MAX} , increased by a factor of 2.19 (from 2.03 GHz to 4.65 GHz).

To more deeply investigate the differences between the fabricated single-gate and clamped-gate MOGFETs, the small-signal equivalent circuits of the intrinsic devices have been identified fitting measured data through computer-aided techniques. As shown in Fig. 4, a good quality fitting has been achieved.

The equivalent circuit topology adopted for the intrinsic MOGFET modeling is illustrated (Fig. 4 (a) and (b)), which includes not only the main transconductance (g_m) and the output resistance (R_{ds}), but also the parasitic access resistances (gate, R_g , source, R_s , and drain R_d) and the coupling capacitances between gate-source (C_{gs}) and gate-drain (C_{dg}). The measured vs simulated values of $|h_{21}|_{dB}$ are compared for both the intrinsic and extrinsic devices of single-gate and

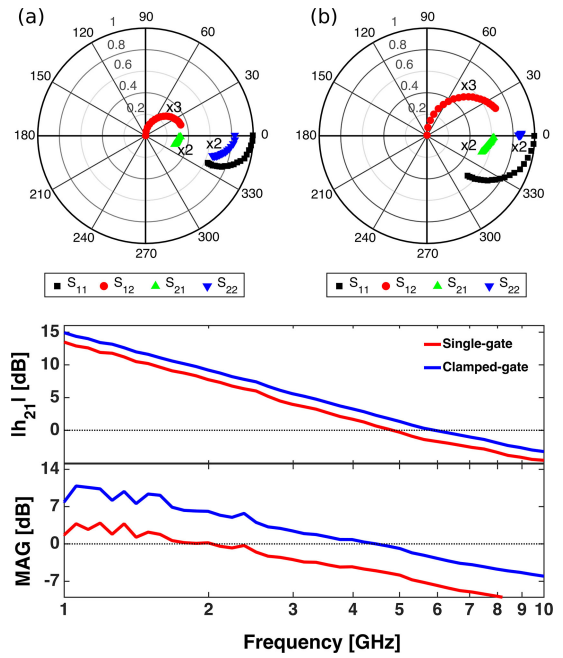


FIGURE 3. Polar plot of the S-parameters of single-gate device (a) and clamped-gate device (b). The frequency range is from 50 MHz to 20 GHz. Comparison of measured $|h_{21}|_{dB}$, MAG_{dB} , as a function of frequency for a single-gate device (red curves) and clamped-gate one (blue curves).

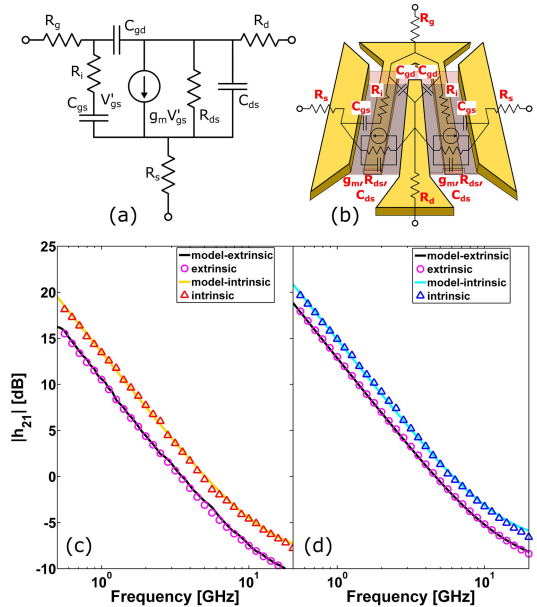


FIGURE 4. (a, b) Small-signal equivalent circuits. Measured and simulated curves of $|h_{21}|_{dB}$ for both intrinsic and extrinsic devices of (c) single-gate and (d) clamped-gate MOGFETs.

clamped-gate types are shown in Fig. 4(c) and Fig. 4(d), respectively. The equivalent circuit parameter values identified for the devices with S-parameters and gains shown in Fig. 3 are reported in Table 1.

From the reported model parameter values, it can be observed that the main variation between single-gate and clamped-gate devices is associated to the increase of the

TABLE 1. Model parameter values for both single and clamped-gate devices.

Model parameter	Single-gate device	Clamped-gate device
R_g [Ω]	128.3	63
$R_{s,d}$ [Ω]	0.6	0.9
R_d [Ω]	36.4	22.9
R_i [Ω]	0.03	0.9
R_{ds} [Ω]	84.4	103.1
g_m [mS]	-3.1	-5.2
$C_{gs} = C_{gd}$ [fF]	41	64
C_{gs} [fF]	15.3	9

transconductance (from 3.1 to 5.2 mS) and to the decrease of the gate resistance (from 128.3 to 63 Ω), as expected by virtue of the improved gating mechanism and of the double metal-layer structure of the clamped-gate configuration. The former result is also consistent with the DC characterization above reported. Since the other circuit parameters exhibit only small variations, the model confirms the improvement in the gain and frequency response expected from the new design and verified by the measurements.

IV. CONCLUSION AND FUTURE WORKS

In conclusion, two technological improvements in the structure of MOGFETs have been proposed and experimentally verified to increase devices high-frequency performance. The first one consists in the adoption of meandered graphene source contacts, in order to reduce contact resistances. The second one is associated to the use of a clamped-gate structure to increase the device transconductance. Both these improvements have been confirmed by the MOGFET prototypes, which have been fabricated on a sapphire substrate by using CVD graphene in a standard planar technology. The proposed approach, combined with state-of-the-art graphene, could accelerate the widespread adoption of MOGFETs as active devices for microwave telecommunication applications.

REFERENCES

- [1] W.-Y. Lu and Y. Taur, "On the scaling limit of ultrathin SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 1137–1141, May 2006.
- [2] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H.-S. P. Wong, "Device scaling limits of Si MOSFETs and their application dependencies," *Proc. IEEE*, vol. 89, no. 3, pp. 259–288, Mar. 2001.
- [3] S. Veeraraghavan and J. G. Fossum, "Short-channel effects in SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 36, no. 3, pp. 522–528, Mar. 1989.
- [4] B. Yu *et al.*, "FinFET scaling to 10 nm gate length," in *Dig. Int. Electron Devices Meeting*, 2002, pp. 251–254.
- [5] A. Chaudhry and M. J. Kumar, "Controlling short-channel effects in deep-submicron SOI MOSFETs for improved reliability: A review," *IEEE Trans. Device Mater. Rel.*, vol. 4, no. 1, pp. 99–109, Mar. 2004.
- [6] R. S. Shenoy and K. C. Saraswat, "Optimization of extrinsic source/drain resistance in ultrathin body double-gate FETs," *IEEE Trans. Nanotechnol.*, vol. 2, no. 4, pp. 265–270, Dec. 2003.
- [7] K. W. Guarini *et al.*, "Triple-self-aligned, planar double-gate MOSFETs: Devices and circuits," in *Int. Electron Devices Meeting Tech. Dig. (IEDM)*, 2001, pp. 1–4.
- [8] K. S. Novoselov, "Electric field effect in atomically thin carbon films," *Science*, vol. 306, no. 5696, pp. 666–669, Oct. 2004.
- [9] A. K. Geim and K. S. Novoselov, "The rise of graphene," *Nat. Mater.*, vol. 6, no. 3, pp. 183–191, 2007.
- [10] A. C. Ferrari *et al.*, "Science and technology roadmap for graphene, related two-dimensional crystals, and hybrid systems," *Nanoscale*, vol. 7, no. 11, pp. 4598–4810, 2014.
- [11] M. A. Giambra *et al.*, "High-speed double layer graphene electro-absorption modulator on SOI waveguide," *Opt. Exp.*, vol. 27, no. 15, pp. 20145–20155, 2019.
- [12] T. Cassese *et al.*, "Capacitive actuation and switching of add-drop graphene-silicon micro-ring filters," *Photon. Res.*, vol. 5, no. 6, pp. 762–766, 2017.
- [13] M. Romagnoli *et al.*, "Graphene-based integrated photonics for next-generation datacom and telecom," *Nat. Rev. Mater.*, vol. 3, no. 10, pp. 392–414, Oct. 2018.
- [14] J. E. Muench *et al.*, "Waveguide-integrated, plasmonic enhanced graphene photodetectors," *arXiv preprint, arXiv:1905.04639*, 2019.
- [15] F. Schwierz, "Graphene transistors: Status, prospects, and problems," *Proc. IEEE*, vol. 101, no. 7, pp. 1567–1584, Jul. 2013.
- [16] Y.-M. Lin, K. A. Jenkins, A. Valdes-Garcia, J. P. Small, D. B. Farmer, and P. Avouris, "Operation of graphene transistors at gigahertz frequencies," *Nano Lett.*, vol. 9, no. 1, pp. 422–426, Jan. 2009.
- [17] X. Du, I. Skachko, A. Barker, and E. Y. Andrei, "Approaching ballistic transport in suspended graphene," *Nat. Nanotechnol.*, vol. 3, no. 8, pp. 491–495, Aug. 2008.
- [18] X. Li *et al.*, "Large-area synthesis of high-quality and uniform graphene films on copper foils," *Science*, vol. 324, no. 5932, pp. 1312–1314, Jun. 2009.
- [19] L. Banszerus *et al.*, "Ultrahigh-mobility graphene devices from chemical vapor deposition on reusable copper," vol. 1, no. 6, pp. 1–7, Jul. 2015.
- [20] V. Miseikis *et al.*, "Deterministic patterned growth of high-mobility large-crystal graphene: A path towards wafer scale integration," *2D Mater.*, vol. 4, no. 2, Jan. 2017, Art. no. 021004.
- [21] Y. Wu *et al.*, "State-of-the-art graphene high-frequency electronics," *Nano Lett.*, vol. 12, no. 6, pp. 3062–3067, Jun. 2012.
- [22] M. Donnelly, D. Mao, J. Park, and G. Xu, "Graphene field-effect transistors: The road to bioelectronics," *J. Phys. D Appl. Phys.*, vol. 51, no. 49, 2018, Art. no. 493001.
- [23] J. Tian, A. Katsounaros, D. Smith, and Y. Hao, "Graphene field-effect transistor model with improved carrier mobility analysis," *IEEE Trans. Electron Devices*, vol. 62, no. 10, pp. 3433–3440, Oct. 2015.
- [24] M. C. Lemme, T. J. Echtermeyer, M. Baus, and H. Kurz, "A graphene field-effect device," *IEEE Electron Device Lett.*, vol. 28, no. 4, pp. 282–284, Apr. 2007.
- [25] M. C. Lemme *et al.*, "Mobility in graphene double gate field effect transistors," *Solid-State Electron.*, vol. 52, no. 4, pp. 514–518, 2008.
- [26] T. Thingujam, D. Chettri, K. J. Singh, M. Kumar, T. J. Singh, and S. K. Sarkar, "Study and design of graphene field effect transistor for RF performance," in *Proc. Int. Conf. Inventive Commun. Comput. Technol. (ICICCT)*, 2017, pp. 308–312.
- [27] F. Schwierz, "Graphene transistors," *Nat. Nanotechnol.*, vol. 5, no. 7, pp. 487–496, Jul. 2010.
- [28] B.-W. Hwang, H.-I. Yeom, D. Kim, C.-K. Kim, D. Lee, and Y.-K. Choi, "Enhanced transconductance in a double-gate graphene field-effect transistor," *Solid-State Electron.*, vol. 141, pp. 65–68, Mar. 2018.
- [29] Y.-M. Lin, H.-Y. Chiu, K. A. Jenkins, D. B. Farmer, P. Avouris, and A. Valdes-Garcia, "Dual-gate graphene FETs with f_T of 50 GHz," *IEEE Electron Device Lett.*, vol. 31, no. 1, pp. 68–70, Jan. 2010.
- [30] S. Kim *et al.*, "Realization of a high mobility dual-gated graphene field-effect transistor with Al_2O_3 dielectric," *Appl. Phys. Lett.*, vol. 94, no. 6, 2009, Art. no. 062107.
- [31] J. Yan and M. S. Fuhrer, "Charge transport in dual gated bilayer graphene with corbino geometry," *Nano Lett.*, vol. 10, no. 11, pp. 4521–4525, Nov. 2010.
- [32] M. A. Giambra *et al.*, "Layout influence on microwave performance of graphene field effect transistors," *Electron. Lett.*, vol. 54, no. 16, pp. 984–986, Aug. 2018.
- [33] M. A. Giambra *et al.*, "Graphene field-effect transistors employing different thin oxide films: A comparative study," *ACS Omega*, vol. 4, no. 1, pp. 2256–2260, Jan. 2019.

- [34] A. Benfante *et al.*, "Employing microwave graphene field effect transistors for infrared radiation detection," *IEEE Photon. J.*, vol. 10, no. 2, Apr. 2018, Art. no. 6801407.
- [35] A. D. Franklin, S.-J. Han, A. A. Bol, and V. Perebeinos, "Double contacts for improved performance of graphene transistors," *IEEE Electron Device Lett.*, vol. 33, no. 1, pp. 17–19, Jan. 2012.
- [36] J. T. Smith, A. D. Franklin, D. B. Farmer, and C. D. Dimitrakopoulos, "Reducing contact resistance in graphene devices through contact area patterning," *ACS Nano*, vol. 7, no. 4, pp. 3661–3667, 2013.
- [37] F. Xia, V. Perebeinos, Y.-M. Lin, Y. Wu, and P. Avouris, "The origins and limits of metal-graphene junction resistance," *Nat. Nanotechnol.*, vol. 6, no. 3, pp. 179–184, 2011.
- [38] A. Venugopal, L. Colombo, and E. M. Vogel, "Contact resistance in few and multilayer graphene devices," *Appl. Phys. Lett.*, vol. 96, no. 1, 2010, Art. no. 013512.
- [39] S. Russo, M. F. Craciun, M. Yamamoto, A. F. Morpurgo, and S. Tarucha, "Contact resistance in graphene-based devices," *Physica E Low Dimensional Syst. Nanostruct.*, vol. 42, no. 4, pp. 677–679, 2010.
- [40] E. Pallecchi, C. Benz, A. C. Betz, H. V. Lo, B. Plaçais, and R. Danneau, "Graphene microwave transistors on sapphire substrates," *Appl. Phys. Lett.*, vol. 99, no. 11, 2011, Art. no. 113502.
- [41] C. Benz *et al.*, "Graphene on boron nitride microwave transistors driven by graphene nanoribbon back-gates," *Appl. Phys. Lett.*, vol. 102, no. 3, 2013, Art. no. 033505.
- [42] I. Meric, M. Y. Han, A. F. Young, B. Ozyilmaz, P. Kim, and K. L. Shepard, "Current saturation in zero-bandgap, top-gated graphene field-effect transistors," *Nat. Nanotechnol.*, vol. 3, no. 11, pp. 654–659, Nov. 2008.
- [43] M. C. A. M. Koolen, J. A. M. Geelen, and M. P. J. G. Versleijen, "An improved de-embedding technique for on-wafer high-frequency characterization," in *Proc. Bipolar Circuits Technol. Meeting*, 1991, pp. 188–191.