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Power Quality Services Provided by Virtually Synchronous FACTS

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Abstract: The variable and unpredictable behavior of renewable energies impacts the performance of power systems negatively, threatening their stability and hindering their efficient operation. Flexible ac transmission systems (FACTS) devices are able to emulate the connection of parallel and series impedances in the transmission system, which improves the regulation of power systems with a high share of renewables, avoiding congestions, enhancing their response in front of contingencies and, in summary, increasing their utilization and reliability. Proper control of voltage and current under distorted and unbalanced transient grid conditions is one of the most critical issues in the control of FACTS devices to emulate such apparent impedances. This paper describes how the synchronous power controller (SPC) can be used to implement virtually synchronous FACTS. It presents the SPC functionalities, emphasizing in particular the importance of virtual admittance emulation by FACTS devices in order to control transient unbalanced currents during faults and attenuate harmonics. Finally, the results demonstrate the effectiveness of SPC-based FACTS devices in improving power quality of electrical networks. This is a result of their contribution to voltage balancing at point of connection during asymmetrical faults and the improvement of grid voltage quality by controlling harmonics flow.

Keywords: FACTS; virtual synchronous machine; synchronous power controller; power quality; harmonics

1. Introduction

The continuously increasing penetration of renewable energies (REN), particularly wind and PV generation, is gradually reducing the conventional synchronous generation share from the energy mix. As a result, the overall power system performance degrades, since REN plants do not perform as conventional synchronous generation in terms of regulation and grid support [1]. Hence, the grid codes require modern REN plants to integrate certain grid-interactive functionalities in order to make their response compatible with the natural behavior of the electrical grid in case of grid events [2,3]. In this regard, the power converters used in modern REN plants need additional functionalities, specifically, to provide voltage and frequency support during faults by remaining connected to the grid, known as low-voltage ride-through (LVRT), and to inject instantaneous reactive power. Even so, these functionalities improve the interaction of REN power plants with the electrical grid only at the point of common coupling (PCC). Therefore, other mechanisms are necessary for improving power system performance in the area level. These mechanisms should address issues related to congestion, contingencies, oscillations, inefficiencies and instabilities resulting from the inherent intermittence and lack of inertia of REN power plants. In this regard, flexible ac transmission systems (FACTS) have demonstrated to be an effective approach that enhances controllability and increases utilization of power systems.

2. FACTS Based on Virtually Synchronous Power Converters

The FACTS concept was introduced in the late 1980s [4] and since then the relevant technologies have experienced significant advancements, both in hardware components and control methods. FACTS and High-voltage dc (HVDC) systems possess fundamental differences with respect to their operating principle. However, both are presented together as active solutions based on high-power electronics to enhance regulation and flexibility of transmission systems, and thereby to increase the capacity of power systems [5].

Depending on their configuration and application, different types of FATCS devices are described in the literature [6–8]. In general, they can be classified into two main categories, namely, series-connected and shunt-connected FACTS devices. The series-connected FACTS are installed between two buses of the power system by connecting them in series with a transmission line. Therefore, by regulating the voltage provided through the series-connected FACTS, it is possible to modify the apparent impedance of the power line; in other words, to increase/reduce its capacity and to regulate the power flow in the system. Moreover, proper control of the output voltage from the series-connected FACTS allows the improvement of the systems response against voltage distortions or sudden events, such as grid faults. The thyristor controlled series capacitor (TCSC) [9], the static synchronous series compensator (SSSC) [10], the dynamic voltage restorer (DVR) [11], and the fault current limiter (FCL) [12], among others, can be mentioned as the most popular series-connected FACTS. The shunt-connected FACTS are usually implemented through power converters that are able to control the current injected into a given bus of the system. Through appropriate controllers, the current injected in the grid can be formed by positive- and negative-sequence components at the fundamental frequency as well as harmonic components. This not only makes possible to control the magnitude of the voltage at the bus where the shunt-connected FACTS is connected, but also to compensate for unbalances and distortion. Commonly used shunt-connected FACTS devices are the static synchronous compensator (STATCOM) [13], the static var compensator (SVC) [14], the thyristor controlled reactor (TCR) [15], the thyristor switched capacitor [16], and the shunt active filter (SAF) [17]. The combination of series- and shunt-connected FACTS gives rise to cost-effective devices, which combine features from both FACTS categories. The unified power flow controller (UPFC) [18], the convertible static compensator (CSC) [19] and the unified power quality conditioner (UPQC) [20] are examples of such hybrid FACTS devices.

The majority of existing shunt-connected FACTS devices are based on detecting characteristic parameters of the grid voltage, i.e., amplitude, frequency and phase-angle, and, accordingly, to inject an appropriate current for emulating a given shunt-connected impedance. Series-connected FATCS follow the same rational where the power converter imposes a given voltage in series with the line to emulate a series-connected impedance. Nevertheless, in both cases a synchronization system, such as the well-known phase-locked loop (PLL) [21], is used to detect the grid voltage parameters. However, the conventional PLL does not perform properly under unbalanced and distorted conditions. This necessitates the use of other sophisticated implementations that can accurately detect the grid components even during these demanding operating conditions [22]. Note that the PLL is a non-linear system with a particular dynamic response, which strongly affects the grid-connected power converters response. This is particularly significant during grid faults and transients that can even give rise to hazardous interactions with other controllers in the grid.

For this reason, a new approach to design power converters controllers was proposed around one decade ago. Specifically, this approach demands the equations that define the operation of a synchronous machine to be integrated in the power converter controller [23]. It is worth mentioning that a synchronous machine can synchronize with the electrical grid or even regulate its operation without using a PLL. Recently, the aforementioned approach has materialized in several implementations. For instance, the synchronous power controller (SPC) [24] that has exhibited good performance in both HVDC [25,26] and FACTS systems [27,28] under generic operating conditions.

In this paper, we present the SPC operating principle and set of equations. Special attention is given to the configuration of its virtual output admittance to improve the power quality of the

electrical grid when it is affected by harmonics and transient balance and unbalanced faults. Finally, we demonstrate the effectiveness of the SPC when used within the power converter controller of a shunt-connected FACTS device through validation by both simulations and experiments.

3. Synchronous Power Controller

The SPC has been widely used to enable electronics power converter to behave as a synchronous machine [29–32], being an interesting control solution to implement virtually synchronous FACTS. In contrast to PLL-based conventional control schemes, the SPC relies on a power balancing mechanism to maintain its synchronism with the electrical grid. As illustrated in Figure 1, where a generic dc source has been connected at the power converter dc-bus, the SPC consists of a power controller, a virtual admittance emulator, and a current controller. For the stable operation of the power converter, the parameters of these control blocks should be tuned properly. Due to the fact that these control loops have different bandwidth, they can be separately tuned to meet stability requirements as well as to conform to grid codes. Practically, the current control loop, the virtual admittance loop and the power control loop have very different bandwidth and settling time; therefore, they are decoupled and can be tuned separately.

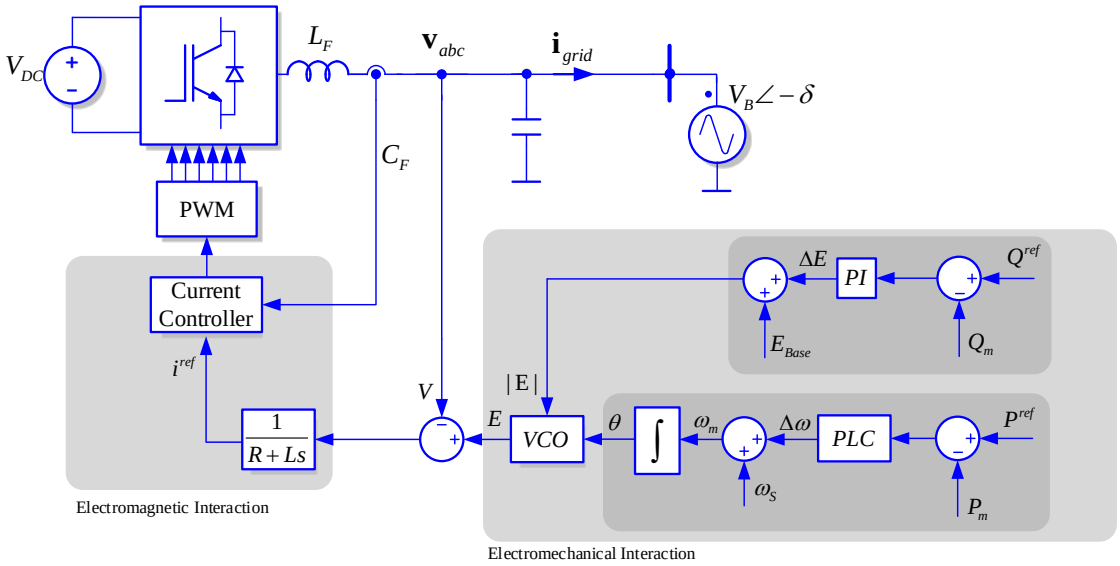


Figure 1. Block diagram of a synchronous power controller (SPC)-based flexible ac transmission systems (FACTS) power converter.

The current controller is the most inner loop of the SPC. The main requirements for this controller are to track the current reference generated by the virtual admittance block and to tolerate the inherently resonant characteristic of the LCL filter. To properly tune the current controller, the LCL filter is modeled on the stationary reference frame as follows:

$$\begin{bmatrix} \dot{i}_c(t) \\ \dot{v}_f(t) \\ \dot{i}_g(t) \end{bmatrix} = \begin{bmatrix} -\frac{R_c}{L_c} & -\frac{1}{L_c} & 0 \\ \frac{1}{C_f} & -\frac{R_c R_f}{L_c} & -\frac{R_f}{L_g+L_{th}} - \frac{R_f}{L_c} & R_f\frac{R_g+R_{th}}{L_g+L_{th}} - \frac{1}{C_f} \\ 0 & \frac{1}{L_g+L_{th}} & -\frac{R_g+R_{th}}{L_g+L_{th}} \end{bmatrix} \begin{bmatrix} i_c(t) \\ v_f(t) \\ i_g(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_c} \\ \frac{R_f}{L_c} \\ 0 \end{bmatrix} v_c(t) + \begin{bmatrix} 0 \\ \frac{R_f}{L_g+L_{th}} \\ -\frac{1}{L_g+L_{th}} \end{bmatrix} v_{th}(t) \quad (1)$$

where i_c, v_f and i_g denote converter-side current, capacitor voltage and grid-side current, respectively, R_c, R_f and R_g represent filter resistances, L_c and L_g represent filter inductances, and R_{th}, L_{th} and v_{th} are

the grid equivalent parameters which can be calculated from the grid short-circuit ratio (SCR) and the quality factor ($q = X/R$) ratio as:

$$R_{th} = \frac{V^2}{SCR \cdot P_n \sqrt{1+q^2}} \text{ and } L_{th} = \frac{V^2 q}{SCR \cdot P_n \cdot \omega_g \sqrt{1+q^2}} \tag{2}$$

The LCL filter model can be concisely expressed as:

$$\dot{\mathbf{x}}_{lclc}(t) = \mathbf{A}_{lclc}\mathbf{x}_{lclc}(t) + \mathbf{B}_{lclc}u(t) + \mathbf{G}_{lclc}w(t) \tag{3}$$

$$y_{lcl}(t) = \mathbf{C}_{lcl}\mathbf{x}_{lclc}(t) \tag{4}$$

where $\mathbf{C}_{lcl} = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix}$ is the output matrix.

Taking into account the digital implementation of the current controller, the filter model is discretized as:

$$\mathbf{x}_{lcl}(k+1) = \mathbf{A}_{lcl}\mathbf{x}_{lcl}(k) + \mathbf{B}_{lcl}u(k) + \mathbf{G}_{lcl}w(k) \tag{5}$$

$$y_{lcl}(k) = \mathbf{C}_{lcl}\mathbf{x}_{lcl}(k) \tag{6}$$

The delay originated by the digital implementation can also be considered in the controller design by the dummy variable x_d as follows:

$$\underbrace{\begin{bmatrix} \mathbf{x}_{lcl}(k+1) \\ x_d(k+1) \end{bmatrix}}_{\mathbf{x}_{in}(k+1)} = \underbrace{\begin{bmatrix} \mathbf{A}_{lcl} & \mathbf{B}_{lcl} \\ 0 & 0 \end{bmatrix}}_{\mathbf{A}_{in}} \underbrace{\begin{bmatrix} x_{lcl}(k) \\ x_d(k) \end{bmatrix}}_{\mathbf{x}_{in}(k)} + \underbrace{\begin{bmatrix} 0 \\ 1 \end{bmatrix}}_{\mathbf{B}_{in}} u(k) + \underbrace{\begin{bmatrix} \mathbf{G}_{lcl} \\ 0 \end{bmatrix}}_{\mathbf{G}_{in}} w(k) \tag{7}$$

$$y_{in}(k) = \underbrace{\begin{bmatrix} C_{lcl} & 0 \end{bmatrix}}_{C_{in}} \underbrace{\begin{bmatrix} x_{lcl}(k) \\ x_d(k) \end{bmatrix}}_{x_{in}(k)} \tag{8}$$

To asymptotically track the reference current, the internal model principle is employed to model a proportional resonant (PR) as:

$$\dot{\mathbf{x}}_{prc}(t) = \underbrace{\begin{bmatrix} 0 & 1 \\ -\omega_g^2 & 0 \end{bmatrix}}_{\mathbf{A}_{prc}} \mathbf{x}_{prc}(t) + \underbrace{\begin{bmatrix} 1 \\ 0 \end{bmatrix}}_{\mathbf{B}_{prc}} e_i(t) \tag{9}$$

where w_g denotes fundamental grid frequency, and $e_i = i^* - i_g$ represents tracking error with i^* being reference current. The controller model can also be discretized as:

$$\mathbf{x}_{pr}(k+1) = \mathbf{A}_{pr}\mathbf{x}_{pr}(k) + \mathbf{B}_{pr}e_i(k) \tag{10}$$

The inverter model and the current controller model can be augmented as:

$$\begin{bmatrix} x_{in}(k+1) \\ \mathbf{x}_{pr}(k+1) \end{bmatrix} = \begin{bmatrix} \mathbf{A}_{in} & 0 \\ -\mathbf{B}_{pr}\mathbf{C} & \mathbf{A} \end{bmatrix} \begin{bmatrix} x_{in}(k) \\ \mathbf{x}_{pr}(k) \end{bmatrix} + \begin{bmatrix} \mathbf{B}_{in} \\ 0 \end{bmatrix} u(k) + \begin{bmatrix} \mathbf{B}_d \\ 0 \end{bmatrix} w(k) + \begin{bmatrix} 0 \\ \mathbf{B}_{pr} \end{bmatrix} r(k) \tag{11}$$

or:

$$\mathbf{x}(k+1) = \mathbf{A}\mathbf{x}(k) + \mathbf{B}u(k) + \mathbf{B}_d w(k) + \mathbf{B}_r r(k) \tag{12}$$

Asymptotic tracking of current controller can be achieved by stabilizing the augmented system in (12) using the following feedback controller:

$$u(k) = \mathbf{K}\mathbf{x}(k) \tag{13}$$

The feedback controller can be optimally calculated by minimizing the following quadratic cost function:

$$J_\infty = \sum_{k=0}^{\infty} \left\{ \mathbf{x}^T(k)\mathbf{Q}\mathbf{x}(k) + u^T(k)Ru(k) \right\} \tag{14}$$

where $\mathbf{Q}$ and R are tunable parameters to adjust performance of the current controller. It is worth noting that the choice of $\mathbf{Q}$ and R is based on the relative importance of system states and control signals, which is not always a straightforward process. To simplify the selection of $\mathbf{Q}$ and R, one may select R as an identity matrix i.e., $R = 1$ and $\mathbf{Q}$ as $\mathbf{Q} = \rho\mathbf{I}$. Then, ρ can be altered to achieve a desired response. For instance, the higher the value of ρ, the faster the transient response and smaller the stability margin.

The virtual impedance shown in Figure 2 is usually chosen according to voltage support requirement by the grid codes. The state space equation for the virtual impedance can be given as:

$$\dot{i}_g^*(t) = -\frac{R_v}{L_v} i_g^*(t) + \frac{1}{L_v} e(t) - \frac{1}{L_v} v_g(t) \tag{15}$$

where R_v is the virtual resistance, L_v is the virtual inductance, i_g^* is the reference current for current controller, and e is the reference voltage coming from power control loop.

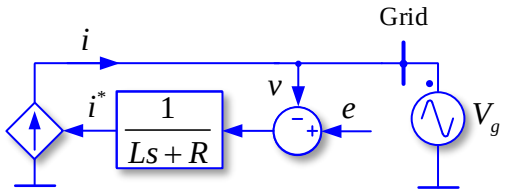


Figure 2. Simplified model of a current-controlled grid-connected power converter with virtual admittance.

The power controllers consisting of an active power and a reactive power controller are the main elements of the SPC scheme. The active power controller is based on the electromechanical swing equation to synchronize the power converter with the electrical grid. The transfer function of swing equation is given by:

$$\omega_{spc} = \frac{1}{\omega_s(Js + D)}(P_m - P_e) + \omega_s \tag{16}$$

where P_m and P_e are the mechanical and the electrical power, respectively, ω_{spc} and ω_s are the SPC and synchronous angular speed, respectively, J is the virtual polar moment of inertia and D is the damping factor.

The reactive power controller is based on a proportional integral (PI) controller defined as follows:

$$E = \frac{k_p s + k_i}{s}(Q_m - Q_e) + E_r \tag{17}$$

where E is the amplitude reference for the virtual electromotive force (emf) voltage of the virtually synchronous FACTS, E_r is a feed-forward reference for such emf voltage and k_p and k_i are the proportional and the integral gains of the controller.

To simplify the analysis of the power controller loop, the dynamics of inner control loop are neglected and replaced by static gains. To calculate these gains, the powers exchanged between the SPC-based virtually synchronous FACTS and the electrical grid can be written as:

$$P_e = \frac{EV}{Z}\cos(\phi - \delta) - \frac{V^2}{Z}\cos(\phi) \tag{18}$$

$$Q_e = \frac{EV}{Z}\sin(\phi - \delta) - \frac{V^2}{Z}\sin(\phi) \tag{19}$$

where $Z = \sqrt{R_v^2 + X_v^2}$ is the magnitude of the virtual impedance, ϕ is the phase-angle of such an impedance, V denotes the rms value of the grid line voltage, E the rms value of the virtual emf and δ is the grid load angle, i.e., the angle between E and V phasors.

The above equations can be rewritten for small-signal analysis as:

$$P_{e0} + \Delta P_e = \frac{(E_0 + \Delta E)V}{Z}(\cos\phi\cos(\delta_0 + \Delta\delta) + \sin\phi\sin(\delta_0 + \Delta\delta)) - \frac{V^2}{Z}\cos(\phi) \tag{20}$$

$$Q_{e0} + \Delta Q_e = \frac{(E_0 + \Delta E)V}{Z}(\sin\phi\cos(\delta_0 + \Delta\delta) - \cos\phi\sin(\delta_0 + \Delta\delta)) - \frac{V^2}{Z}\sin(\phi) \tag{21}$$

In steady-state, when synchronism takes place, $\delta_0 = 0$, and also $\Delta\delta \approx 0$, then $\cos(\Delta\delta) \approx 1$ and $\sin(\Delta\delta) \approx \Delta\delta$. Therefore:

$$P_{e0} + \Delta P_e = \frac{E_0 V\cos(\phi)}{Z} - \frac{V^2\cos(\phi)}{Z} + \frac{E_0 V\sin(\phi)}{Z}\Delta\delta + \frac{V\cos(\phi)}{Z}\Delta E + \frac{V\sin(\phi)}{Z}\Delta E\Delta\delta \tag{22}$$

$$Q_e + \Delta Q_e = \frac{E_0 V\sin(\phi)}{Z} - \frac{V^2\sin(\phi)}{Z} - \frac{E_0 V\cos(\phi)}{Z}\Delta\delta + \frac{V\sin(\phi)}{Z}\Delta E - \frac{V\cos(\phi)}{Z}\Delta E\Delta\delta \tag{23}$$

Omitting the zero- and second-order terms, the small-signal component of the electrical power can be written as:

$$\Delta P_e = \frac{E_0 V\sin(\phi)}{Z}\Delta\delta + \frac{V\cos(\phi)}{Z}\Delta E \tag{24}$$

$$\Delta Q_e = -\frac{E_0 V\cos(\phi)}{Z}\Delta\delta + \frac{V\sin(\phi)}{Z}\Delta E \tag{25}$$

From Equations (16), (17), (24) and (25), the state-space representation of the power control loop is given by:

$$\begin{bmatrix} \Delta\dot{\omega}_{spc} \\ \Delta\dot{\delta} \\ \Delta\dot{Q}_e \end{bmatrix} = \begin{bmatrix} -\frac{D}{J} & \frac{k_p k_{p2} k_{q1} - k_p k_{p1} k_{q2} - k_{p1}}{(k_p k_{q2}+1)\omega_g} & \frac{k_i k_p k_{p2} k_{q2} - k_i k_p k_{q2} - k_i}{(k_p k_{q2}+1)\omega_g} \\ 1 & 0 & 0 \\ 0 & -\frac{k_{q1}}{k_p k_{q2}+1} & -\frac{k_i k_{q2}}{k_p k_{q2}+1} \end{bmatrix} \begin{bmatrix} \Delta\omega_{spc} \\ \Delta\delta \\ \Delta Q_e \end{bmatrix} + \begin{bmatrix} \frac{1}{\omega_g} & -\frac{k_p k_{p2}}{(k_p k_{q2}+1)\omega_g} \\ 0 & 0 \\ 0 & 1 - \frac{k_p k_{p2}}{k_p k_{q2}+1} \end{bmatrix} \begin{bmatrix} \Delta P_m \\ \Delta Q_m \end{bmatrix} \tag{26}$$

$$\begin{bmatrix} \Delta P_e \\ \Delta Q_e \end{bmatrix} = \begin{bmatrix} 0 & k_{p1} - \frac{k_p k_{p2} k_{q1}}{k_p k_{q2}+1} & k_i - \frac{k_i k_p k_{p2} k_{q2}}{k_p k_{q2}+1} \\ 0 & \frac{k_{q1}}{k_p k_{q2}+1} & \frac{k_i k_{q2}}{k_p k_{q2}+1} \end{bmatrix} \begin{bmatrix} \Delta\omega_{spc} \\ \Delta\delta \\ \Delta Q_e \end{bmatrix} + \begin{bmatrix} 0 & \frac{k_p k_{p2}}{k_p k_{q2}+1} \\ 0 & \frac{k_p k_{q2}}{k_p k_{q2}+1} \end{bmatrix} \begin{bmatrix} \Delta P_m \\ \Delta Q_m \end{bmatrix} \tag{27}$$

where $k_{p1} = \frac{E_0 V\sin(\phi)}{Z}$, $k_{p2} = \frac{V\cos(\phi)}{Z}$, $k_{q1} = \frac{E_0 V\cos(\phi)}{Z}$, $k_{q2} = \frac{V\sin(\phi)}{Z}$, and δ is the grid load angle, as previously defined.

Due to the fact that the three control loops have very different bandwidths, their dynamics are nearly decoupled. Thus, these control loops can be designed separately. The stability of the current control loop can be ensured by choosing a proper value of ρ. Since the current control loop is stable, the voltage control loop is also stable, as the virtual admittance is in a form of a low-pass filter. The same analogy is applied to the power control loop.

Even though the dc-bus voltage level of SPC-based FACTS is naturally regulated thanks to the inherent power balance-based principle of the SPC controller, the dc-bus voltage level might experience dramatic changes due to unexpected events, such as line trips. To prevent the dc-bus voltage of SPC-based FACTS from surpassing safe operational limits, the control loop shown in Figure 3 is added to the SPC schema already shown in Figure 1. This protection loop has two PI controllers devoted to directly change the phase-angle of the virtual emf of the SPC, and thereby its output power, to keep the dc-bus voltage level within given limits. In this way, the protection range for the dc-bus voltage can be adjusted by just setting the $v_{\mathrm{lim}}{}^{\mathrm{min}}$ and $v_{\mathrm{lim}}{}^{\mathrm{max}}$ parameters. In addition, a saturation block is added at the output of each PI controller to ensure the protection loop only acts in case the dc-bus voltage level is out of the safe operational range, and to limit the maximum power reference in case of activation. This control loop has a very fast response, since it directly changes the phase-angle of the virtual emf, being its dynamics set by the parameter k_{phase}.

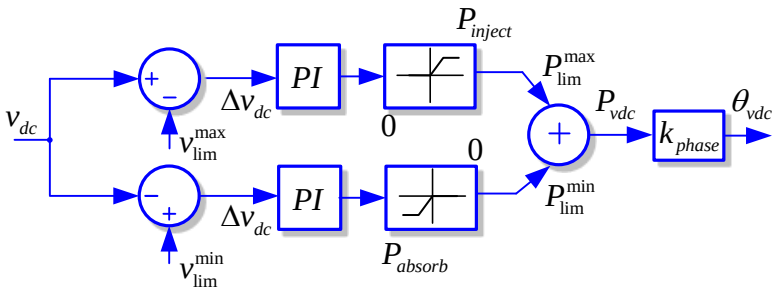


Figure 3. Proportional integral (PI) strategy for dc voltage protection.

4. Simulation Results

The setup structure for the simulation results is presented in Figure 4. It is composed by a 100 kVA power converter, a harmonic load and a voltage sag generator. The devices will be connected and disconnected from the PCC during the different simulation tests. In a first simulation case, voltage support results under balanced and unbalanced voltage dips will be presented, where the harmonic load is not connected to the PCC, thus not generating any harmonic disturbances in the grid voltage. In a second simulation case, the voltage sag generator will be disconnected from the system, and the harmonic load will be connected. This load will consume harmonic current which will distort the grid voltage.

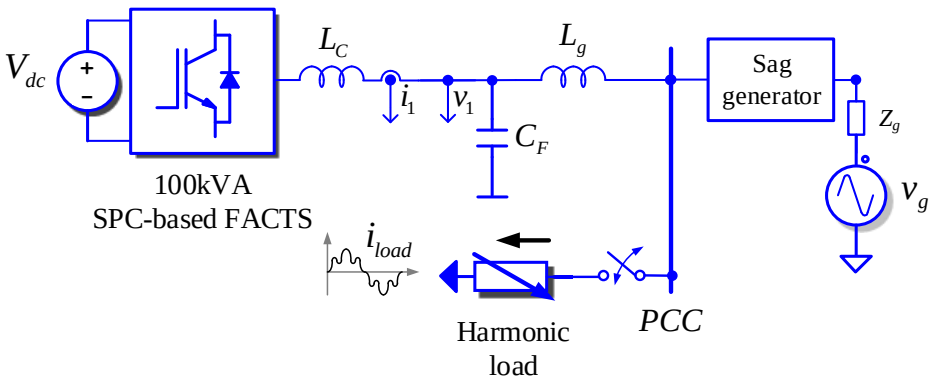


Figure 4. Simulation results setup. PCC: point of common coupling.

The parameters of the 100 kVA power converter and the grid connection are presented in Table 1, which specifies the inductance parameters of the grid and the voltage sag generator.

Table 1. Of the SPC-based FACTS power converter, the voltage sag generator and the grid.

Inverter Parameters	
Total output power	100 kVA
Filter Parameters	
Converter Inductor	777 µH
Grid Inductor	294 µH
Damping resistor	0.5 ohm
Capacitor	66 µF
Voltage sag Gen. Inductance	400 µH
Grid Parameters	
Grid Inductor	400 Uh
Grid Resistor	0.152 ohm

In the upcoming subsections, the balanced and unbalanced low voltage ride through (LVRT) simulation results are presented, as well as the harmonic compensation results during harmonic distortions at the grid voltage.

4.1. Balanced LVRT

To simulate the performance of an actual voltage sag generator, which is composed by inductors and contactors changing their connection, the voltage sag has two voltage steps during the connection and disconnection of contactors. Figure 5 presents the voltage dip generated at the PCC of the SPC-based FACTS connected to the grid. On the left side, Figure 5a presents the voltage dip at the PCC without the interaction of the SPC-based FACTS. It is possible to see how the voltage drops to zero at the PCC when the SPC-based FACTS does not support the grid voltage. On the right side, Figure 5b presents the voltage dip at the PCC when the SPC-based FACTS interacts with the electrical grid by injecting reactive currents during the voltage disturbance. In this case, once the voltage dip is detected by the control system, the power converter starts injecting reactive currents thanks to the effect of the virtual admittance controller. This allows the power converter to support the grid voltage during voltage sags. The third plot in Figure 5b shows the injected current in the synchronous reference frame, evidencing the injection of reactive current i_q during the voltage sag. Once the grid fault is released, the power converter stops injecting reactive current to the grid, and returns to the steady state operation set-point.

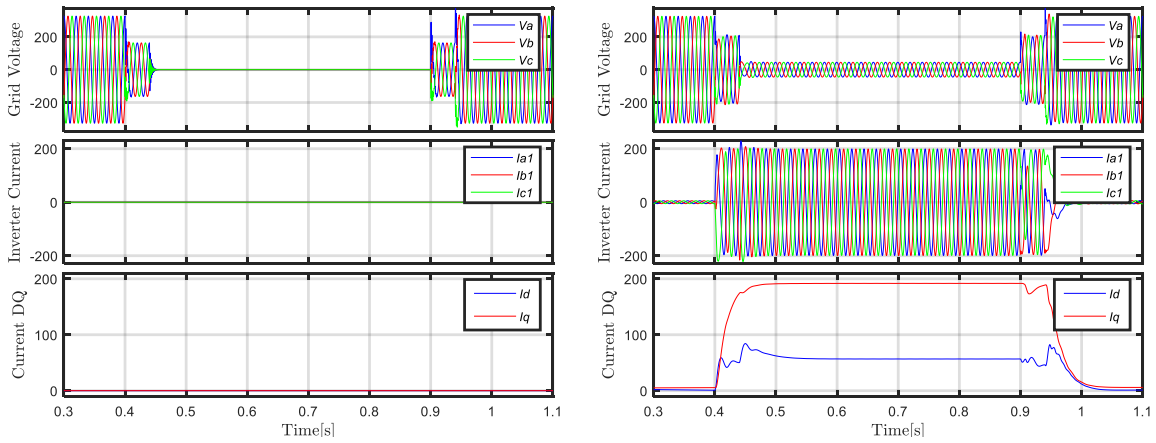
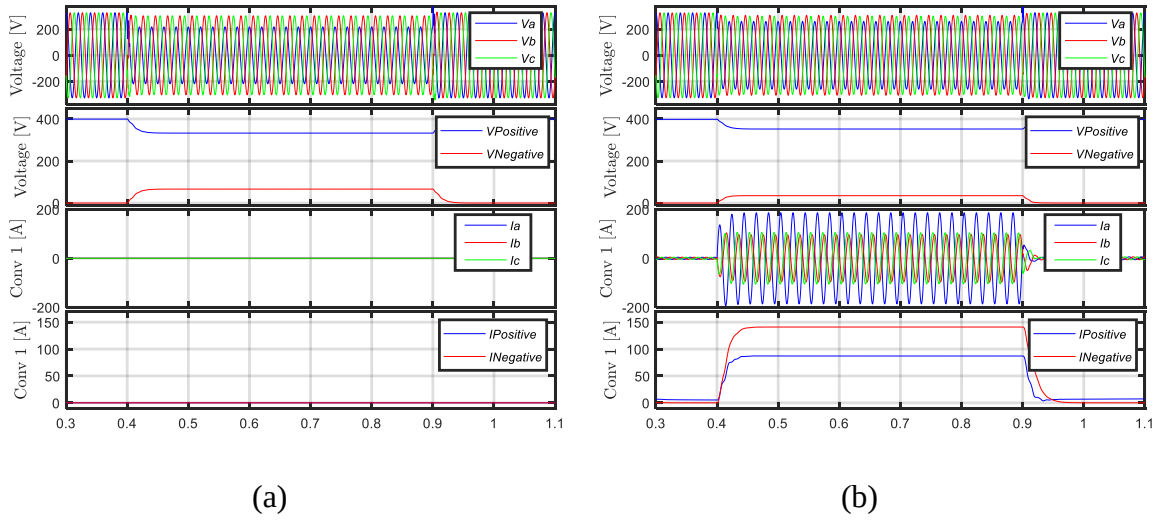


Figure 5. Balanced low-voltage ride-through (LVRT) test. Voltage sag to 0% of the voltage (**a**) LVRT without SPC-based FACTS compensation. (**b**) LVRT with the compensating current injected by the SPC-based FACTS.

4.2. Unbalanced LVRT

The unbalanced voltage sag is one of the most common voltage disturbances affecting the grid voltage, as it appears when one or two phases of the grid are faulted. This perturbation generates negative-sequence voltages along the grid, which can be observed as unbalanced voltages at the PCC. Figure 6 presents an unbalanced voltage dip at the PCC. On the left, Figure 6a presents the PCC voltage when the SPC-based FACTS does not provide any support to the grid voltage. In this case, the negative-sequence component of the gird voltage reached 70 V. Figure 6b displays the PCC voltage when the SPC-based FACTS supports the grid voltage in front of unbalances. In this case, the SPC-based FACTS injects negative-sequence currents to keep the grid voltage balanced. Comparing Figure 6a and Figure 6b, it is possible to appreciate that there is a significant reduction of the negative-sequence component of the grid voltage, which is reflected in reducing the imbalance degree among phases at the PCC.



(a) (b)

Figure 6. Unbalanced LVRT test. (**a**) LVRT without SPC-based FACTS. (**b**) LVRT with the compensating current injected by the SPC-based FACTS.

4.3. Harmonic Compensation

Harmonics can be generated by a large amount of systems, commonly the ones using power converters to process power. Systems such as diode rectifiers, charging systems or even computers produce harmonics that flow through the grid and distort the grid voltage. In addition to hazardous grid resonances, such distorted voltages can damage to the equipment connected to the grid. By enabling several parallel virtual admittances in a SPC-based FACTS, it is possible to control harmonics flow and to minimize their impact on the grid. Figure 7 presents the PCC voltage resulting from the connection of a harmonic load to the grid, and the effect of the SPC-based FACTS in conditioning such a voltage. Figure 7a displays the PCC voltage waveform resulted from the connection of a harmonic load. The amplitude for the 5th and the 7th voltage harmonic arises to 14 V and 16 V, respectively. Once the harmonic admittances of the SPC-based FACTS are enabled, the power converter starts injecting compensating currents. Figure 7b, shows the compensating currents injected by the SPC-based FACTS and how they dramatically reduce the grid voltage distortion. A comparison between Figure 7a and Figure 7b shows the significant reduction of 5th and 7th harmonic components of the grid voltage.

The simulation results shown in this section have demonstrated how SPC-based FACTS can improve the power quality of the electrical grid in front of voltage transients and distortions. In the following section, some experimental results are presented to validate such simulation results. In this manner, the same tests shown in simulation are now conducted in the lab by using real equipment.

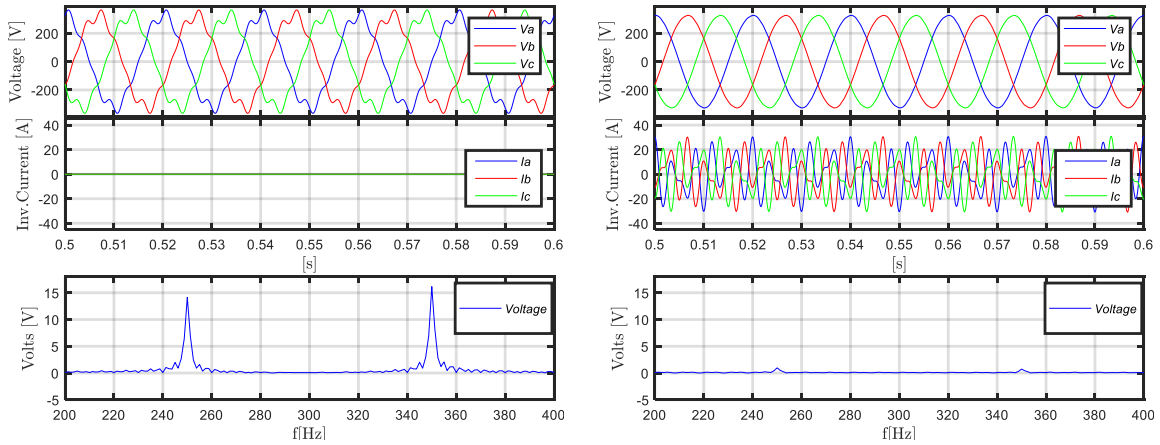


Figure 7. Harmonic control simulation result. (**a**) Harmonic load without SPC-based FACTS compensation. (**b**) Harmonic load with SPC-based FACTS injecting harmonic current to the PCC.

5. Experimental Results

The experimental setup used for obtaining experimental results consists of two 100 kVA power converters connected to the PCC, a dc-voltage generator, a voltage sag generator and a harmonic load to absorb harmonic currents from the grid, as shown in Figure 8.

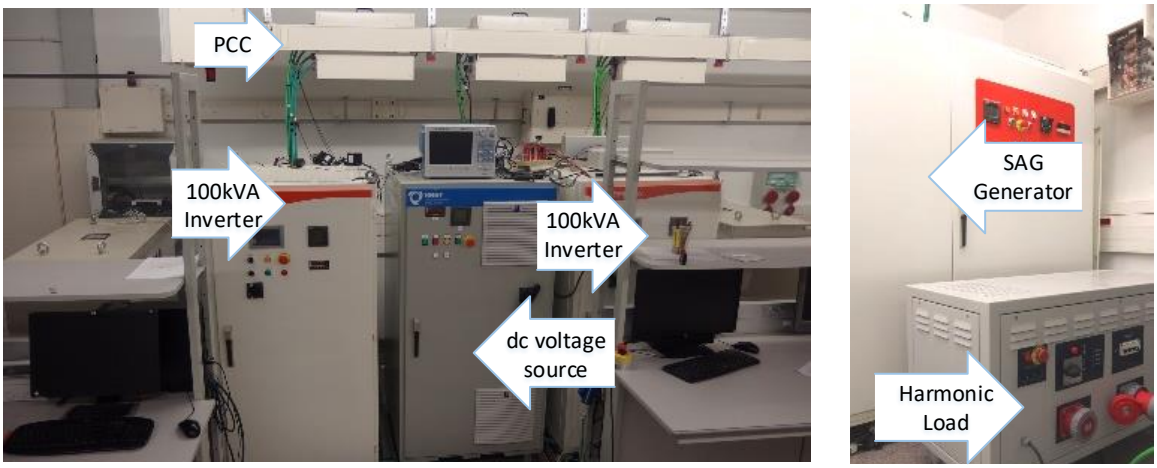


Figure 8. Experimental setup.

By following the sequence as in simulations, the first test to be conducted will deal with the grid support provided by the SPC-based FACTS when a balanced voltage sags happens in the grid, i.e., when the three phases of the grid are affected equally by the voltage sag. In a second test, the response of the SPC-based FACTS in front of unbalanced voltage sags will be shown. After that, the impact of the SPC-based FACTS when conditioning a distorted grid voltage due to harmonic currents will be evaluated experimentally. These test will show how the SPC-based FACTS perfectly withstand voltage transients and distortions, inject reactive currents and harmonics to improve the quality of the voltage waveform.

5.1. Balance LVRT

In this experiment, voltage sags are generated through a voltage sag generator, which consists of several inductances and tap switches to generate different voltage levels at the PCC. In the case of a

balanced voltage sag, the three phases decease the voltage amplitude to a certain value during the sag time. In this experiment, the SPC-based FACTS will inject reactive current to restore the voltage level at the PCC. Figure 9 presents the scheme of the experimental setup used for this experiment.

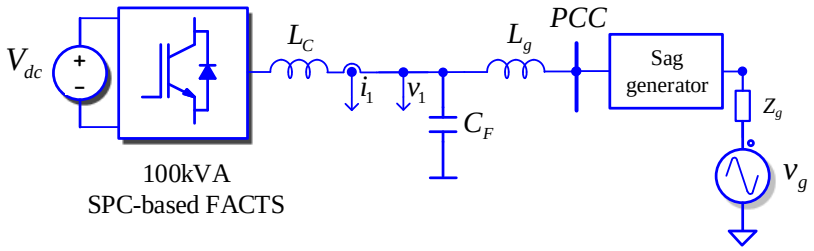


Figure 9. Scheme of the SPC-based FACTS connected to the grid for the balance LVRT test.

As shown in simulations, the SPC-based FACTS presents an inherit capability to inject reactive current in the electrical grid during voltage sags thanks to the effect of the virtual admittance. Once the virtual admittance controller detects a significant difference between the measured gird voltage, $v_1(t)$, and the virtual emf, $e(t)$, it generates an instantaneous reference current to counteract such a difference by injecting reactive current into the electrical grid. Figure 10a shows the beginning of the voltage sag. During this transient, the SPC-based FACTS detects the grid voltage reduction at the PCC and start increasing the reactive current injected into the grid. Later, once the voltage sag is released, the SPC-based FACTS stops providing reactive current and returns to its regular state. Figure 10b presents the end of the voltage sag, when the SPC-based FACTS returns to steady-state operation set-point.

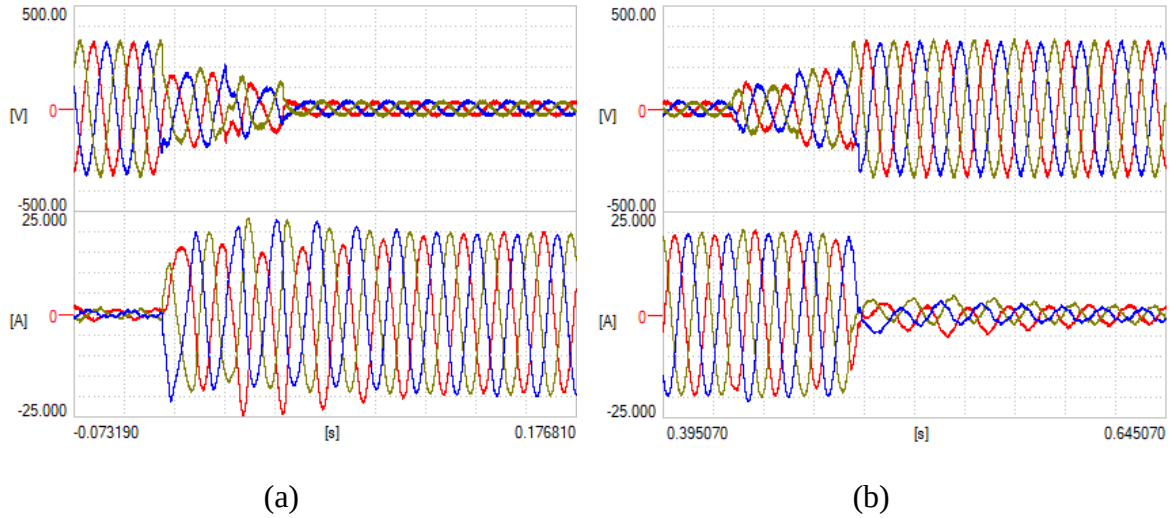


Figure 10. Response of the SPC-based FACTS to a balanced sag. Voltage sag to 0% (**a**) Beginning of the voltage sag. (**b**) End of the voltage sag.

Analyzed the system on the synchronous reference frame, it can be appreciated how the SPC-based FACTS inject reactive current i_q during the grid fault to contribute to restore the voltage at the PCC. In Figure 11, the dq current components i_{dq} are plotted. It can be appreciated in this figure how the current i_q is triggered at t = 2.18 s, when the voltage sag is detected by the SPC-based FACTS controller. The system remains injecting reactive current to the grid until the voltage sag is cleared at t = 2.7 s. Once the voltage dip is cleared, the current i_q goes to zero.

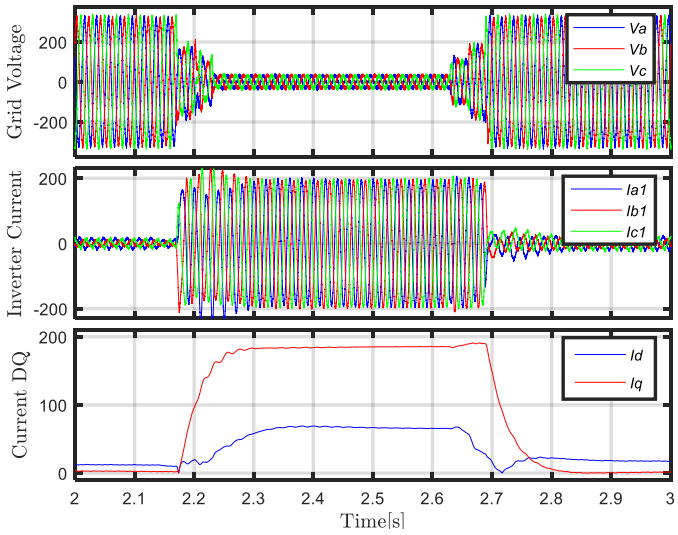


Figure 11. SPC-based FACTS dq currents during a balanced LVRT test.

5.2. Unbalanced LVRT

Single-phase and phase-to-phase faults generate unbalanced voltages, which gives rise to negative-sequences components in the grid voltage, which affects negatively to all the connected elements. The control algorithm of the SPC-based FACTS is able to detect the negative-sequence component of the grid voltage and provides a negative-sequence reference current aimed to restore the unbalanced grid voltage. This response in front of unbalanced voltage sags due to the action of the virtual admittance controller, which, after calculating the negative-sequence component of the grid voltage, sets such a voltage component as an input for a virtual admittance block, which generates a negative-sequence reference current addressed to reduce the negative-sequence component of the gird voltage at the PCC. Figure 12 shows the scheme of the setup used for conducting the unbalanced LVRT test. In this case, two SPC-based FACTS are connected to the PCC, which will experience the unbalanced voltage sag created through the sag generator. During the fault, the SPC-based FACTS will inject reactive currents to contribute to balance the grid voltage. Additionally, both SPC-based FACTS will share the amount of negative sequence current injected into the grid as a function of the parameters set for the virtual admittance in each SPC-based FACTS.

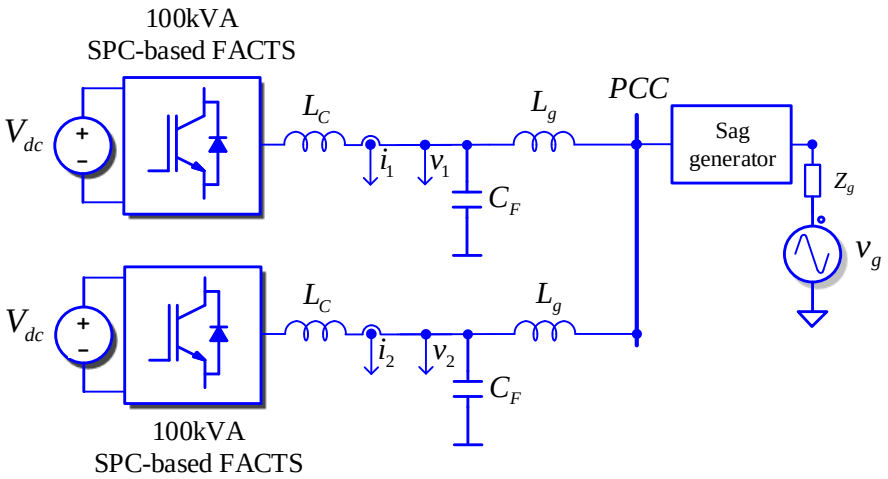
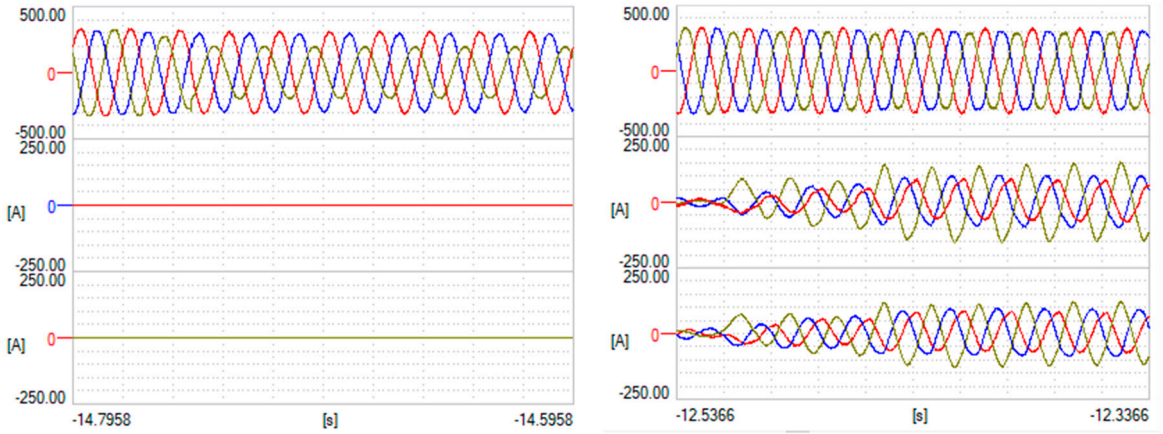


Figure 12. Electrical schematic for two SPC-based FACTS affected by an unbalanced voltage sag.

In this experiment, a voltage sag generator is used to generate the unbalanced grid voltage. In a first test, the SPC-based FACTS does not inject any reactive current into the grid when the unbalanced

sag happens. Plots for this test are shown in Figure 13a, where unbalanced voltages can be seen at the PCC when the SPC-based FACTS do not provide any support. In Figure 13b, the two SPC-based FACTS are enabled to provide support to the electrical grid. In this test, once the sag is detected by the virtual admittance controller, the SPC-based FACTS starts injecting negative-sequence current into the grid in order contribute to balance the grid voltage at the PCC.



(**a**) (**b**)

Figure 13. Response of the SPC-based FACTS to an unbalanced sag. (**a**) Unbalanced voltage sag without SPC-based FACTS (**b**) Two SPC-based FACTS inject reactive current to balance the gird voltage at the PCC.

The positive- and negative-sequence components of the voltage and current resulting from this experiment can be analyzed to assess the support provided to the electrical grid by the SPC-based FACTS. Figure 14a presents the voltage sag components when no reactive current is injected by the SPC-based FACTS. In this case, the positive-sequence component of the grid voltage decreases to 81% of its rated value, whereas the amplitude for the negative-sequence component grows until 20% of the rated grid voltage. As shown Figure 14b, once the SPC-based FACTS controllers are enabled to compensate unbalanced grid voltages, the positive-sequence component of the grid voltage at the PCC during the unbalanced sag decreases to the 92% of its rated value, while the negative-sequence component of the unbalanced voltage at the PCC just increases to the 5% of the rated grid voltage. Those effects can be seen in the difference between the sinusoidal waveforms from Figure 14. In this experiment, both SPC-based FACTS inject the same amount of reactive current since both of them set the same values for the virtual impedance used for processing the negative-sequence component of the PCC voltage.

5.3. Harmonic Compensation

The SPC-based FACTS can integrate multiple virtual admittances, each of them tuned to a given frequency, which can generate compensating currents addressed to the minimize distortion of the grid voltage at the PCC. To do that, the frequency components of the grid voltage should be measured, e.g., using band-pass filters tuned to the frequencies of interest, and provided as inputs to corresponding harmonic admittances in order to generate the compensating harmonic currents to be injected into the grid.

In this experiment, a non-linear load connected to the PCC, which will generate some harmonic components at the PCC voltage. The admittance controller of the SPC-based FACTS is enabled to detect such a voltage distortion at the PCC, and to inject compensating currents to attenuate the distortion of the grid voltage at the PCC. Figure 15 presents the setup used in this experiment, where a harmonic load is connected to the PCC in parallel to the SPC-based FATCS. Additionally, a 400 μH line inductance has been added to increase distortion at the PCC voltage.

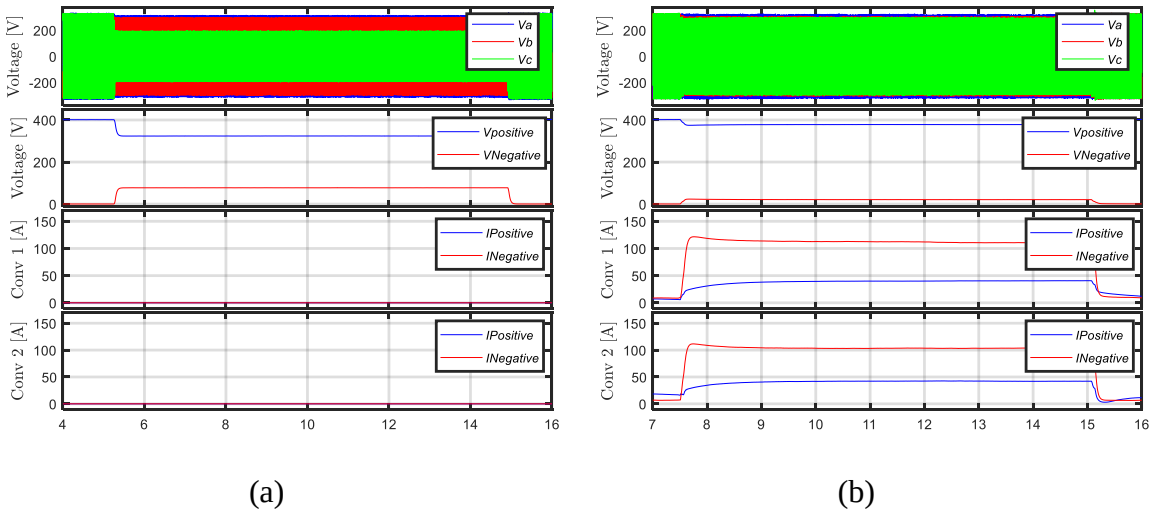


Figure 14. Response of the SPC-based FACTS to an unbalanced voltage sag. (**a**) Positive- and negative-sequence components of the PCC voltage and current when the SPC-based FACTS is disabled. (**b**) Positive- and negative-sequence components of the PCC voltage and current when the SPC-based FACTS is enabled.

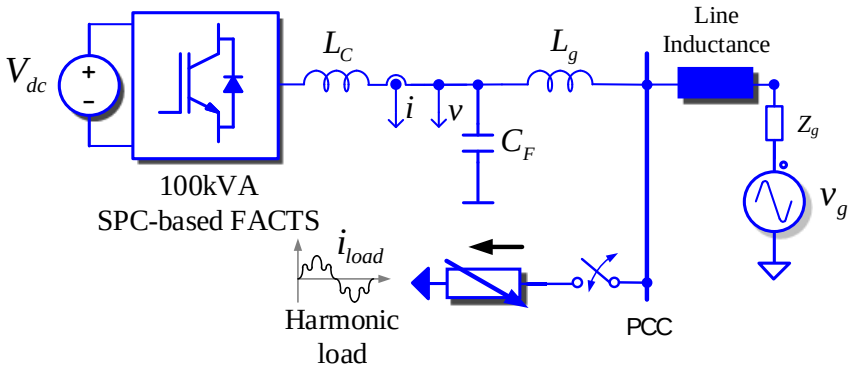


Figure 15. Electrical schematic for harmonic compensation control test.

In this experiment, a non-linear load is connected, giving rise to a notable amount of 5th and 7th harmonic in the current absorbed form the electrical grid. The SPC-based FACTS is able to detect the harmonic components at the PCC voltage, e.g., using multiple band-pass filters, and to inject proper currents reduce the voltage distortion at the PCC. Figure 16, from top to bottom, shows the grid voltage at the PCC, the current injected by the SPC-based FATCS and the current absorbed by the non-linear load. As appreciated in this figure, the current injected by the SPC-based FACTS compensates the one demanded by the load and the quality of the voltage at the PCC is improved. This is evidenced when the SPC-based FACTS is disabled at $t = -0.73$ s. From that time on, the harmonic load currents flow through the line impedance, instead through the SPC-based FACTS, which notably increases the grid voltage distortion.

A more detailed analysis of the grid voltage, paying special attention to the 5th and 7th harmonic components, allows assessing the effectiveness of the SPC-based FACTS in improving power quality. Figure 17a,b show the PCC voltage spectrum in case the SPC-based is disabled and enabled, respectively. As Figure 17a shows, when the harmonics control of the SPC-based FACTS is disabled, the grid voltage at the PCC presents remarkable levels for the 5th and 7th harmonic components, namely, 12 V and 7 V, respectively. However, once the harmonics compensation function is enabled in the SPC-based FATCS, the quality of the PCC voltage improves significantly. In such a case, Figure 17b shows how

the amplitude levels for the 5th and 7th harmonic components has been reduced to 6 V and 2.5 V, respectively, which can be also appreciated on the sinusoidal waveform shape.

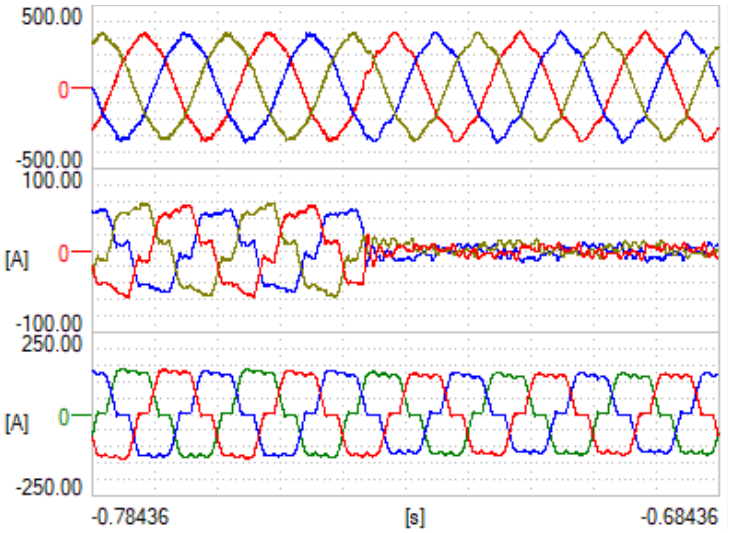


Figure 16. Grid voltage distortion reduction by the SPC-based FATCS.

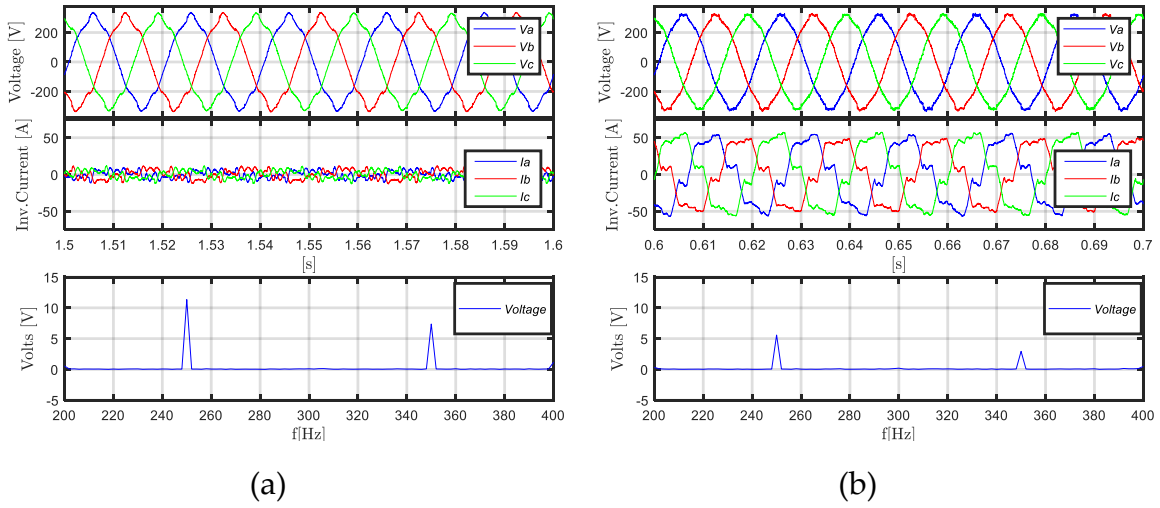


Figure 17. Effect of the SPC-based FACTS in grid voltage reduction (**a**) Harmonics compensation disabled. (**b**) Harmonics compensation enabled.

6. Conclusions

This paper has presented the application of the synchronous power controller (SPC) to FACTS with the aim of improving power quality in electrical grids. This paper has conducted an overview on FACTS devices and has highlighted that the virtual synchronous power has gained notable popularity among engineers and researchers in the last years to interface power converters to ac synchronous electrical grid. The control scheme and the main equations governing the SPC, which are essential to implement simulation models and analyses, have been presented in the paper. Based on such models, the paper has presented some simulations results addressed to evaluate the performance of a SPC-based FACTS when improving power quality in the electrical grid. In such an evaluation, the positive impact of the SPC-based FACTS to improve the grid voltage quality during balanced and unbalanced voltage sags, as well as in case of current harmonics flowing along the grid, has been illustrated by representative simulations. Moreover, such simulation results have been validated through experiments in the lab, obtaining satisfactory results. As a conclusion, this paper has presented

the SPC formulation and has evidenced the interest of the SPC-based FACTS for improving power quality in electrical grids.

7. Patents

The Synchronous Power Controller technology is protected by the following patents:

- WO 2012/117131 A1. "Synchronous controller for a generating system based on static power converters", Priority date: 18/02/2011 Licensed by: Abengoa Solar NT, S.A.
- WO 2012/117132 A1 "Controller of the electro-mechanical characteristic of a static power converter", Priority date: 18/02/2011 Licensed by: Abengoa Solar NT, S.A.
- WO 2012/117133 A1 "Virtual admittance controller for a static power converter", Priority date: 18/02/2011 Licensed by: Abengoa Solar NT, S.A.

Author Contributions: G.N.B. conducted an overview of FACTS systems. N.-B.L. developed the SPC's formulation and simulation models. A.T. conducted simulations and lab experiments. P.R. provided conceptual and technical support as the inventor of the SPC. All the co-authors contributed to writing and reviewing the paper. Conceptualization, P.R., A.T. and N.-B.L.; methodology, A.T. and N.-B.L.; software, N.-B.L. and G.N.B.; validation, A.T. and P.R.; formal analysis, A.T. and N.-B.L.; investigation, N.-B.L. and P.R.; resources, A.T.; data curation, G.N.B.; writing—original draft preparation, A.T. and N.-B.L.; writing—review and editing, G.N.B. and P.R.; visualization, G.N.B.; supervision, P.R.; project administration, P.R.; funding acquisition, P.R.

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Conflicts of Interest: The authors declare no conflict of interest.

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