Reliability Study of Thin-Oxide Zero-Ionization, Zero-Swing FET 1T-DRAM Memory Cell

Santiago Navarro, Carlos Navarro, Carlos Marquez, Norberto Salazar, Philippe Galy, Sorin Cristoloveanu and Francisco Gamiz

***Abstract*—Experimental time-dependent dielectric breakdown and ON voltage reliability of advanced FD-SOI Z^2-FET memory cells are characterized for the first time. The front-gate stress time is shown to significantly modulate the ON voltage, hence the memory window. The Weibull slope, β, indicating the device variability to breakdown and the time to soft breakdown, α, present different trends depending on the cell geometry. This fact highlights the trade-off between variability and reliability to account for in Z^2-FET designs.**

***Index Terms*—Z^2-FET, FD-SOI, PIN, DRAM, Reliability, Time Dependent Dielectric Breakdown, Weibull, Capacitor-less.**

I. Introduction

MODERN VLSI process is based upon aggresive dimension scaling and ultra low power consumption strategies. Several deteriorating effects arise from these approaches, being the electric field that the gate oxide supports one of the most important. Over the last CMOS technology generations this oxide field has increased by several MV/cm [1]. This implies a higher gate leakage current and oxide reliability issues which may even render a device unusable.

The Zero Subthreshold Swing and Zero Impact Ionization FET (Z^2-FET) [2] behaves as a 1-transistor DRAM (1T-DRAM) memory cell aimed to replace traditional 1-transistor, 1-capacitor DRAM cells due to its potentially smaller footprint and enhanced current ratio [3]. Unlike most other 1T-DRAM cells [4]–[6], the Z^2-FET operation is not based on any degrading mechanism such as band-to-band tunneling or impact ionization, being outstanding in terms of reliability. Z^2-FET reliability analysis is of primary importance when millions of memory cells are integrated within the same circuit and a cell failure could lead to data corruption. In this work, the Z^2-FET operation at high temperature is initially analyzed and reliability measurements are then carried out: i) the Z^2-FET ON voltage and ON current are measured after front-gate bias stress; ii) the front-gate time-dependent dielectric breakdown (TDDB) is characterized extracting both the Weibull slope, β, and time-to-breakdown, α, for Z^2-FET devices featuring different dimensions. The back-interface reliability is not as relevant for memory operation since the buried-oxide (BOX, Fig. 1) thickness is approximately 25 nm, thus the vertical electric field is much weaker than at the front-gate oxide. Note that the common back-gate voltage is fixed to -1 V or even less negative (closer to 0 V) [7].

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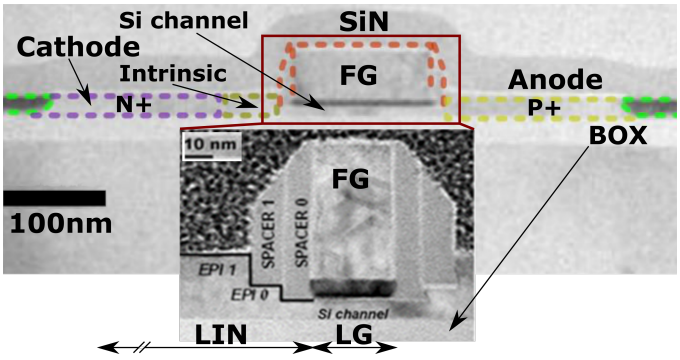

Fig. 1. Cross-section TEM image illustrating the Z^2-FET structure. The inset shows a closer gate-stack picture of a different Z^2-FET featuring distinct geometry. t_{Epi0} + $t_{Epi1} \simeq 15\ nm$, $t_{Si} \simeq 7\ nm$, $t_{BOX} \simeq 25\ nm$.

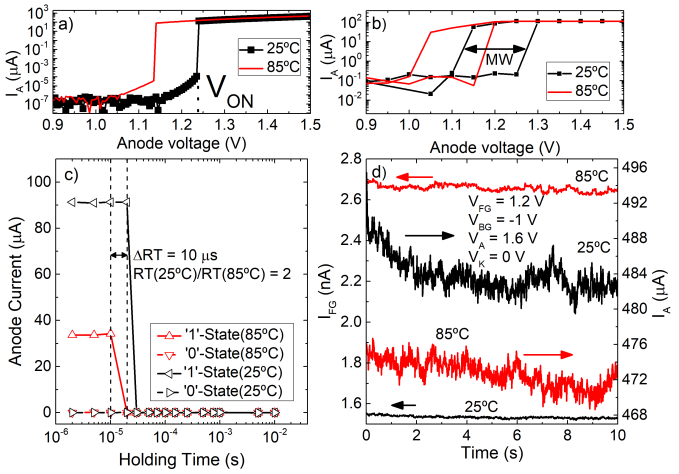

Fig. 2. a) I_A-V_A sweep indicating the point where V_A is equal to V_{ON} for room temperature (25ºC) and 85ºC. b) MW shift to lower voltage as temperature increases. c) RT for both temperatures indicating the time penalty and '1'-state instability under mentioned conditions. d) Front-gate tunnel SILC: initially the SILC decreases until it stabilizes. V_{FG} = 1.2 V, V_{BG} = -1 V and V_K = 0 V in all experiments unless otherwise noted. W = 1000 nm, L_G = 200 nm, L_{IN} = 200 nm.

II. Characterization Setup

Devices under test have been fabricated by ST-Microelectronics [8]. Advanced 28 nm node FD-SOI Z^2-FETs featuring a metal Silicide/Poly/TiN/HfO_2/SiO_2 gate stack with approximately 3.1 nm of thickness (EOT $\simeq$ 1.5 nm) are studied. No oxide corner rounding, enhancing the

electric field, has been observed based on lithography mask simulations. The Z^2-FET cell resembles a conventional PIN diode, Fig. 1, in which the intrinsic region is partially covered by a front gate (FG), defining the gated and ungated intrinsic regions whose lengths are L_G and L_{IN}, respectively. The FG is adjacent to the forward-biased anode (A) contact, while the cathode (K) contact lies at the other side. A bottom back gate (BG) covers the whole PIN structure. Thanks to complementary top and back gate bias ($V_{FG} > 0\ V$ & $V_{BG} < 0\ V$) a virtual NPNP structure is emulated: the gated region and the cathode behave as N-type and the ungated region and the anode as P-type semiconductors. Two distinct current levels (I_1 and I_0, associated to each logic state) are achieved based on the stored charge under the gate. The Z^2-FET operation as memory cell can be found in [7], [9].

III. Results

A. Memory parameter dependence on temperature

Fig. 2a demonstrates the typical Z^2-FET operation exhibiting the characteristic sharp current switch. The ON voltage (V_{ON}, defined as the anode bias at which the current onset arises [10], Fig. 2a) is reduced by increasing the temperature as previously reported [11] due to carrier energy increase, which enables them to surmount the potential barriers from cathode and anode to channel. A similar shift to lower anode bias is observed for the memory window (MW, defined as the V_{ON} difference between the '1' and '0'-programmed state), Fig. 2b. Nor the memory window or the current margin (I_1-I_0) are affected by the high operation temperature. A lower V_{ON} is useful for power consumption reduction with no current level penalty. Nevertheless, the retention time (RT, the time a certain logic state is held) is reduced to 10 μs when the temperature increases to 85°C (Fig. 2c), as occurs for most DRAM cells [12]. The front-gate tunnel leakage current is primary responsible of the RT penalty together with Shockley-Read-Hall (SRH) recombination [13] and trapping/detrapping events. Fig. 2d shows a gate-leakage current increase of about 50% when the temperature is increased.

B. V_{ON} & I_{ON} evolution under stress conditions

The Z^2-FET device is stressed by applying a constant voltage stress (CVS) at the front gate (V_{FG_ST} = 1.5 V) for a fixed time. V_{FG_ST} is set to exceed the operating bias intended for 1T-DRAM usage while V_A is set to 1.6 V to ensure the device is not in OFF state. V_{ON} is monitored by pulsing the anode voltage (increasing the pulse height by 25 mV every cycle and maintaining the same V_{FG}) immediately after stressing to avoid relaxation. Fig. 3a-b show the transient anode current I_A at room and high temperatures for different stress times. The sudden current onset indicates the minimum V_A to overcome the energy barriers, i.e. V_{ON}. At room temperature I_A sharply rises at the same point (the second shown pulse in Fig. 3a) for all stress times, proving it is independent of stress conditions.

In contrast, at 85°C (Fig. 3b) the Z^2-FET triggering arises earlier for shorter stress times. The longer the stress time, the larger the V_{ON} shift. Variations of 50 mV or even larger

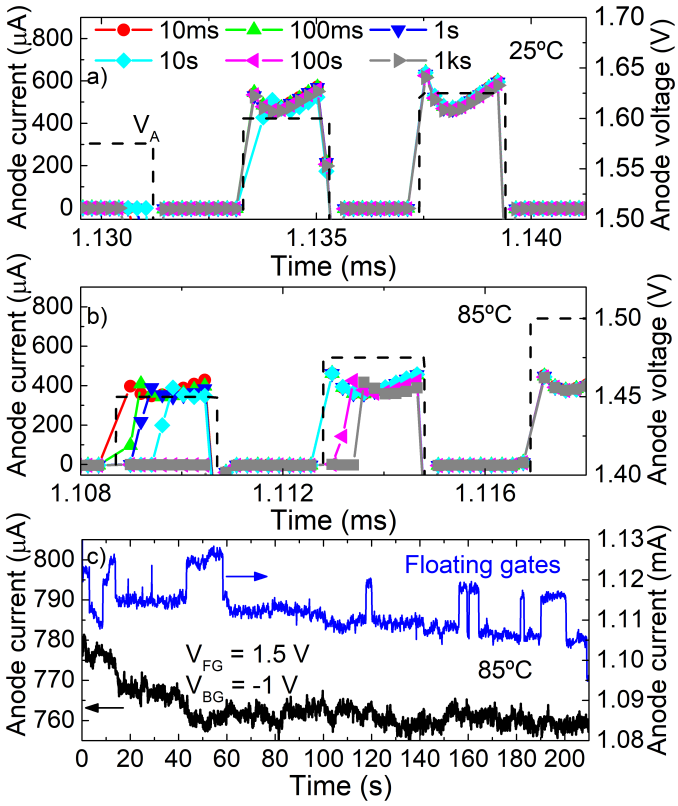

Fig. 3. V_{ON} evolution at a) room and b) high temperature for different stress times. Distinct time scales have been used for a) and b) since V_{ON} changes as a function of temperature. c) I_{ON} with (upper curve) and without (lower curve) floating gates at 85°C. V_{FG} = 1.5 V, V_{BG} = -1 V, V_A = 1.6 V. W = 1000 nm, L_G = 150 nm, L_{IN} = 200 nm.

are observed for stress times longer than 10 s, after which the V_{ON} increase seems to saturate, Fig. 3b. Both the V_{ON} independence at room temperature and the V_{ON} increase at high temperature with the stress time trends have the same origin: at room temperature the electron reservoir under the front gate is not depleted even with the longest stress time. On the contrary, at 85°C, the longer the stress, the more electrons tunnel through the front gate increasing V_{ON}.

The lower curve in Fig. 3c shows the on-the-fly current, namely I_{ON} when $V_A > V_{ON}$, as a function of the stress time for the same V_A and V_{FG_ST} values as mentioned above. The initial decay indicates bias temperature instability (BTI) degradation by two possible mechanisms [14]: i) interface states, acceptor-like presumably, are created by charged H ions as predicted by the Reaction & Difussion model [15] in which carriers are trapped; ii) possitive oxide charge (screening the V_{FG}-V_{BG} induced electric field) is built up as a consequence of charge interaction among oxide species [14]. BTI scenario is verified by repeating the experiment with both gates left floating, Fig. 3c upper curve. As observed the current does not present any BTI degradation and only reveals typical random telegraph noise (RTN) fluctuations. A higher current level is measured when the gates are floating due to the absence of gate-induced energy barriers blocking carrier injection.

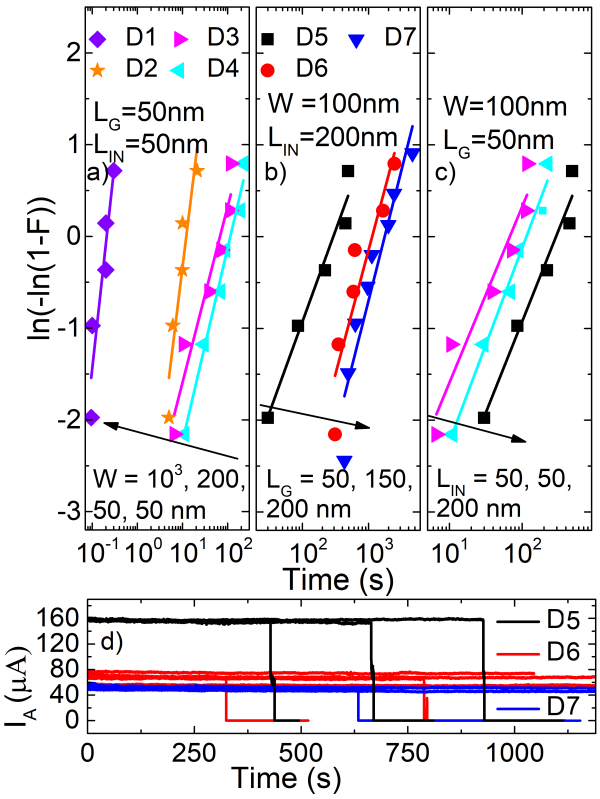

Fig. 4. Weibull plot of the soft t_{BD} as a function of a) the width b) L_G c) L_{IN}. a) Illustrates a high Weibull β for W = 1 and W = 0.2 μm and a medium slope factor for W = 100 nm. b) β slightly increases as the gate length is made larger. c) β slopes are almost parallel. d) anode current, I_A, for D5 (160 μA), D6 (75 μA) and D7 (55 μA). V_{FG} = 3 V, V_A = 1.5 V, V_{BG} = 0 V, t_{OX} = 3.1 nm.

C. Front-gate Time Dependent Dielectric Breakdown

The cell dimensions of devices employed in this work are reported in Table I. The Z^2-FET TDDB was measured at high temperature (85^oC, typical in DRAM cells) and high front-gate voltage (3 V) to cause operation failure at reasonable times for all Z^2-FET geometries. As indicated in [16], constant voltage stress is more appropriate than constant current stress for ultra-thin oxides due to the ballistic interaction of electrons with the dielectric. The random nature of oxide breakdown is generally described by the Weibull distribution [17] $F(t) = 1 - exp(-(t/\alpha)^{\beta})$ where F is the cumulative distribution function (CDF) representing the cumulative fraction of breakdown/wornout devices, t is the stress time, α is the characteristic life and β is the Weibull slope.

Measurements report an initial decrease of stress-induced leakage current (SILC) (Fig. 2d shows the same trend for a different bias) when increasing the stress time which suggests that electrons are trapped in the dielectric [18]. After some time, the SILC becomes constant, which is key for 1T-DRAM memory cells since it is related to the retention time. Fig. 4 represents the Weibull cumulative distribution as a function of the time to soft breakdown (t_{BD}), obtained by varying one cell dimension parameter at a time. t_{BD} is measured when an instantaneous current increase of 5% occurs after the front-gate current has settled down.

Fig. 4a shows the dependence of the Weibull parameters on the cell width (note that D3 and D4 feature the same dimensions). As expected t_{BD} increases in narrow devices since the dielectric area is smaller, in accordance with the percolation model [17]. The wider cells (D1, D2) feature higher β than their W = 100 nm counterparts, see Table 1. A trade-off arises then between the breakdown variability, β (the higher the less deviation among devices), and the time to breakdown, α (the longer the more robust), preventing the optimization of both parameters simultaneously. According to the cell-based model [19], the reduction of β with the device width scaling suggests either a greater lattice constant or a lower defect generation rate. Fig. 4b illustrates the dependence on L_G, where all curves exhibit similar slopes. Interestingly, t_{BD} increases as L_G is made longer (i.e. more dielectric area). The reason is the higher anode current measured for shorter L_G cells (Fig. 4d, D5 anode current, doubles that of D6 and D7). The larger the anode current, the more degradation the dielectric suffers (as happened when V_{ON} is reduced, not shown). Fig. 4c depicts the impact of L_{IN} where the Weibull slopes are almost parallel suggesting similar variability to breakdown: the intrinsic region does not significantly impact the oxide properties.

TABLE I
DIMENSIONS(nm) AND OBTAINED WEIBULL $\beta(-)$ AND $\alpha(s)$ OF REPORTED DEVICES IN THIS WORK.

Dev.	D1	D2	D3	D4	D5	D6	D7
W	1000	200	100	100	100	100	100
L_G	50	50	50	50	50	150	200
L_{IN}	50	50	50	50	200	200	200
β	1.95	1.74	0.92	0.83	0.86	1.17	1.24
α	0.21	12.2	68.7	117.5	290.7	1130.7	1752.4

IV. CONCLUSION

The Z^2-FET ON voltage, memory window, and retention time have been experimentally studied at 85^oC. V_{ON} is insensitive to the applied front-gate stress at room temperature, while at 85^oC a 50 mV increase is observed for stress times longer than 10 s. The ON current is affected by BTI degradation and RTN fluctuations produced by interface and oxide trapping effects. The TDDB analysis shows lower breakdown variability for wider cells but shortest time to breakdown evidencing a trade-off between reliability and variability. The time to breakdown is also shown to be more affected by the lateral electric field than by the dielectric area. The reported results highlight the design strategy towards more robust Z^2-FET memory matrices in terms of footprint and reliability.

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