Investigation of Thin Gate-Stack Z^2-FET Devices as Capacitor-less Memory Cells

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***Abstract*—Thin-oxide Z^2-FET cells operating as capacitor-less DRAM devices are experimentally demonstrated. Both the retention time and memory window demonstrate the feasibility of implementing this cell in advanced 28 nm node FDSOI technology. Nevertheless a performance drop and higher variability with respect to thicker oxide Z^2-FET cells are observed.**

I. Introduction

The traditional 1 transistor – 1 capacitor (1T-1C) DRAM memory cell is approaching its scaling limit [1]. The capacitor can no longer follow the transistor scaling trend since a minimum and technology-independent capacitance is required to guarantee correct memory cell operation [2]. Capacitor-less memory cell architectures, formed solely by one transistor, are a promissing solution for future electronics.

Capacitor-less memory cells are based on the SOI-FET floating body effect [3] by which charge can be stored in the body of the transistor, modulating the threshold voltage and exhibiting distinct drain currents. The body of the memory cell is then fully depleted from or accumulated with carriers to obtain two distinct current levels corresponding to the complementary logic states.

In order to further increase the DRAM integration density limiting the fabrication costs, key aspects for embedded applications, novel capacitor-less cells [4], such as the the MSDRAM [5], the A2RAM [6], [7] or the Z^2-FET [8] have been proposed. All these cells meet most of the stringent next generation DRAM requirements: work under low voltage, present low power consumption, exhibit long retention times and are scalable. Among all this 1T-DRAM cell candidates, the Z^2-FET stands out for its performance and feasible integration with the standard fabrication process in ultra-thin body structures [9]–[11].

Recently it was demonstrated the operation of a fully operational 2x2 Z^2-FET matrix [12] successfully probing simultaneous word programming and reading. In this work, characterization results of 1T-DRAM Z^2-FET cells on 28 nm FDSOI [13] with ultra-thin gate oxide are reported. The measured devices were chosen to characterize both the width (W) and the gate length (L_G) dependence on the cell operation with a fixed ungated length ($L_{IN} = 200\ nm$), as shown in Table I. Section II explains the Z^2-FET structure and operation as memory cell and the sharp current switch mechamism. The 1T-DRAM operation is experimentally verified in Section III. Section IV and V illustrate the memory window and retention time respectively to quantify the memory cell performance. Finally, Section VI is devoted to the variability characterization of some of these cells.

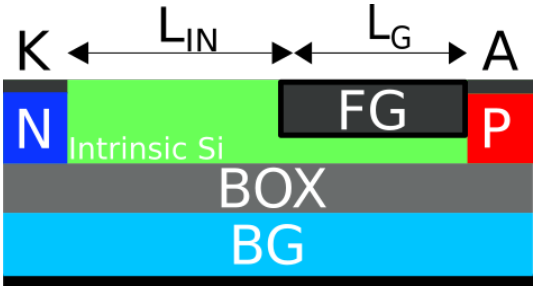

Fig. 1. Z^2-FET DRAM cell parameters: EOT $\approx$ 1.5 nm, $t_{Si} \approx$ 7 nm, $t_{Epi} \approx$ 15 nm (ungated epitaxy thickness) and $t_{BOX} \approx$ 25 nm. $N_{body} \approx 10^{16} cm^{-3}$, $N_{BG} > 10^{18} cm^{-3}$ and $N_{A/K} > 10^{21} cm^{-3}$.

TABLE I
Dimensions of the reported Z^2-FET devices.

Device	L_G(nm)	L_{IN}(nm)	W(μm)
D1	200	200	1
D2	200	200	0.4
D3	200	200	0.1
D4	150	200	1
D5	100	200	1
D6	80	200	1

II. Device structure and operation

A. Device structure

The Z^2-FET DRAM cell basic structure is depicted in Fig. 1. It is similar to a conventional PIN diode in which the intrinsic region is partially covered by a front gate (FG); below the whole device, a highly-doped ground-plane (GP) acting as back gate (BG) is implemented.

The Z^2-FET cells were characterized both at simulation and experimental level. Synopsys Sentaurus [14] software was used to properly confirm the device principles of operation. A

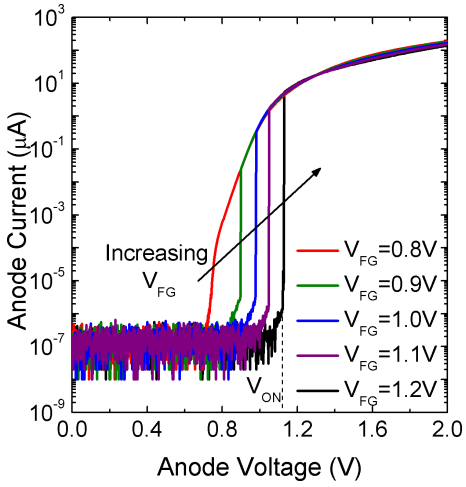

Fig. 2. DC $I_A(V_A)$ sweeps for various V_{FG} for D3. V_{BG} = -1 V, V_K = 0 V. Vertical dashed line illustrates V_{ON} for V_{FG} = 1.2 V. Fabrication parameters are shown in Fig. 1.

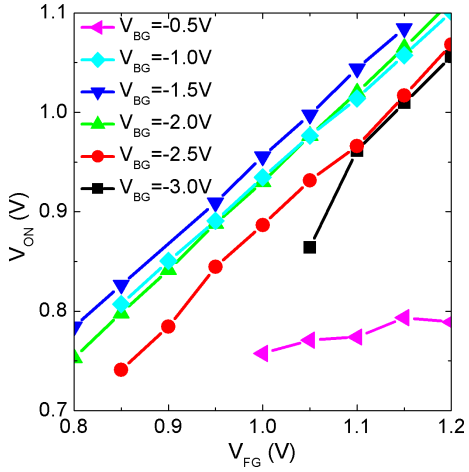

Fig. 3. V_{ON} dependence on the front-gate voltage for several back-gate voltages for D3.

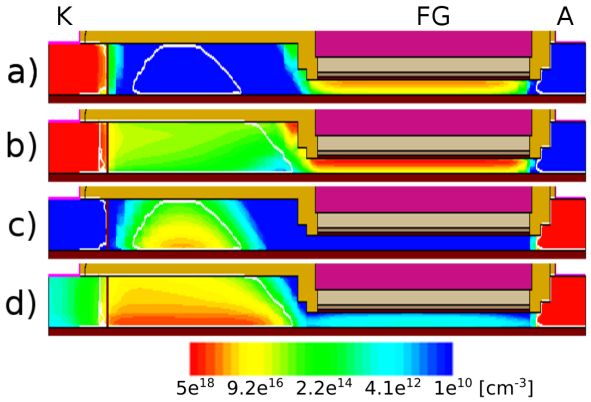

Fig. 4. Carrier concentration reflecting both logic states. Electrons after the a) W_0 and b) W_1 operations. Holes after the c) W_0 and d) W_1 operations.

2D structure following the architecture shown in Fig. 1 was built. The parameters and models accounted include: room temperature (300K), Fermi-Dirac statistics, Shockley-Read-Hall (SRH) generation/recombination, band-to-band tunneling, density gradient and distinct mobility models (field saturation, normal field and thin-layer). The experimental characterization was performed by using the following setup: a semiautomatic Suss-Microtec probe station along with a dedicated Keysight B1500 semiconductor analyzer. Since the cell operation requires fast and accurate timing patterns, B1530 WGFMUs (Waveform Generator/Fast Measurement Unit) were used. Care was taken to minimize the parasitics of the setup to optimize the cell characterization.

B. Device operation

As opposed to conventional diodes, a complementary gate biasing scheme ($V_{FG} > 0$ V and $V_{BG} < 0$ V) is employed to induce high vertical energy barriers and block the current flow in forward mode. Only when the anode voltage (V_A) is high, carriers start to diffuse and, at $V_A = V_{ON}$, the Z^2-FET abruptly recovers the diode behavior. Experimental DC $I_A(V_A)$ curves, probing the typical Z^2-FET sharp current switch, are obtained by applying a sufficiently slow anode ramp signal. This is illustrated in Fig. 2 for D3, (all other devices follow the same trend, not shown). As also happens for thick insulators Z^2-FET cells [8], [9], V_{ON} increases when the front-gate bias is made more positive: holes requires more energy to overcome the anode-body injection barrier. Conversely, when the back gate is made more negative V_{ON} decreases because the front-gate induced potential becomes smaller, Fig. 3. Notice that for close to zero back-gate voltages the back-gate induced energy barrier of D3 barely blocks carriers, so the device does not present a sharp current switch and V_{ON} cannot be defined. The same effect is found when V_{BG} approaches -3 V: the back-gate induced electric field prevails over the front-gate, lowering the barrier along the silicon film and preventing carriers from being blocked. These two effects combine enabling the definition of a maximum V_{ON} for a given V_{FG}.

The energy barrier control, defining the current level and thus the DRAM logic states, is achieved by altering the inner body carrier concentration under the gate: '0'-state corresponds to a very low electron concentration (Fig. 4a) whereas the '1'-state reflects high population (Fig. 4b).

The stored charge is programmed (W) by: forward biasing the diode (V_{FG} = 0 V and $V_A = V_{AW} > 0$ V), which introduces carriers (W_1), or by capacitive coupling (V_{FG} = 0 V and V_A = 0 V) which evacuates them (W_0). State reading, R, is accomplished by simply pulsing the anode terminal ($V_A > 0$ V) to V_{AR}. During holding operations, available body carriers are retained thanks to the gate-induced potential wells ($V_{FG} > 0$ V and $V_{BG} < 0$ V). Exhaustive information regarding the Z^2-FET cell as 1T-DRAM can be found in [9], [11].

C. Sharp current switch

When the mentioned complementary gate biasing scheme is employed and the anode voltage is low enough ($V_A < V_{ON}$),

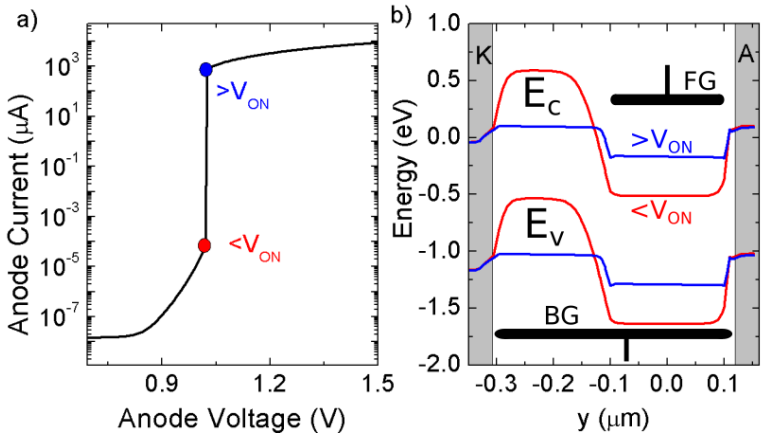

Fig. 5. a) Simulated $I_A(V_A)$ plot showing the typical Z^2-FET sharp switching characteristic at $V_A = V_{ON}$. b) Horizontal Z^2-FET energy bands diagram demonstrating the barrier collapses at $V_A = V_{ON}$. At $V_A < V_{ON}$ two induced potential wells effectively prevent carriers from flowing through the cell, while at $V_A > V_{ON}$ both potential wells are collapsed and the device recovers the PIN diode behavior.

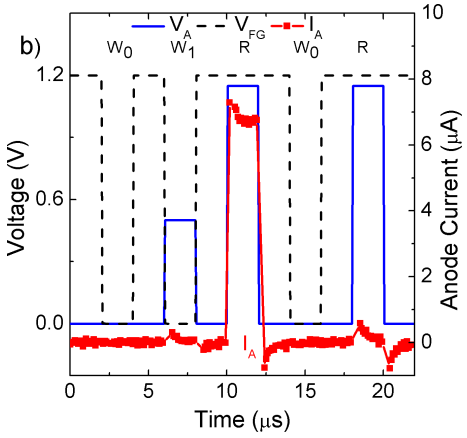

Fig. 6. Transient anode readout current for a $W_0{-}W_1{-}R{-}W_0{-}R$ sequence demonstrating valid DRAM operation. $t_{r/f} = 50\ ns$ (rise/fall times) with $t_w = 2\ \mu s$ (pulse width) for D3. The same behavior is observed for all reported devices in Table I.

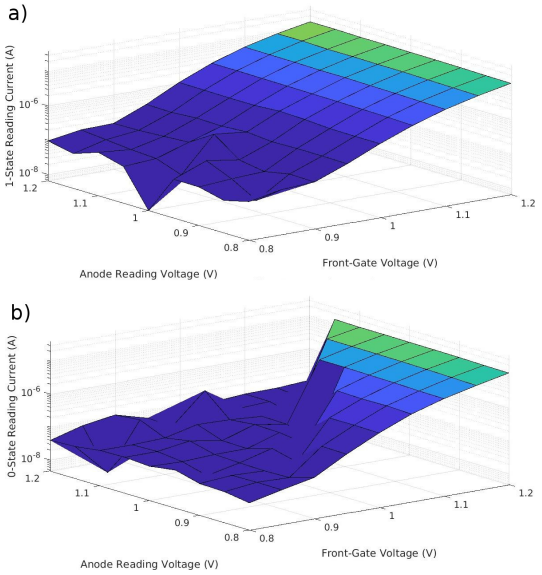

Fig. 7. a) '1' and b) '0'-state reading current for V_{AR} = 1 V as a function of front-gate and anode reading voltages.

carriers cannot overcome the anode/cathode -body barrier (red curve in Fig. 5b), so a negligible anode current is observed, Fig. 5a. As the anode voltage is increased, holes acquiere enough energy to surmount the anode-body barrier and start diffusing into the body. Since the body-cathode barrier is not changed, holes will be accumulated in the back-gate induced well along the intrinsic (ungated) region increasing the electrostatic potential. This reduces the body-cathode barrier and allows electrons to diffuse into the cell, accumulating in the front-gate induced well. The diffused electrons lower the front-gate well potential and therefore the anode-body injection barrier. This in turn, triggers a positive feedbak mechanism by which more carriers flow into the cell until barriers are collapsed (blue curve in Fig. 5b) and the abrupt current switch is suddenly observed. At this point (V_{ON}), the anode current is magnified by several orders of magnitude and the cell recovers the conventinal PIN diode bevavior, Fig. 5a. Thanks to this abrupt change the current ratio, defined as the current relation between both logic states when reading, is boosted with respect to other cells [5], [7], improving the Z^2-FET cell performance.

III. DRAM VALIDATION

To verify the Z^2-FET DRAM operation, both logic states need to be written and then read back. Since the cell transient response depends on the accumulated carriers on the body, electrons are evacuated before the W_1 operation or accumulated before the W_0 operation to ensure the worst scenario. The $W_0 - W_1 - R - W_0 - R$ pattern is applied to the cell (Fig. 6) where the timing conditions were optimized to reduce the leakage current and RC parasitic discharges in the setup.

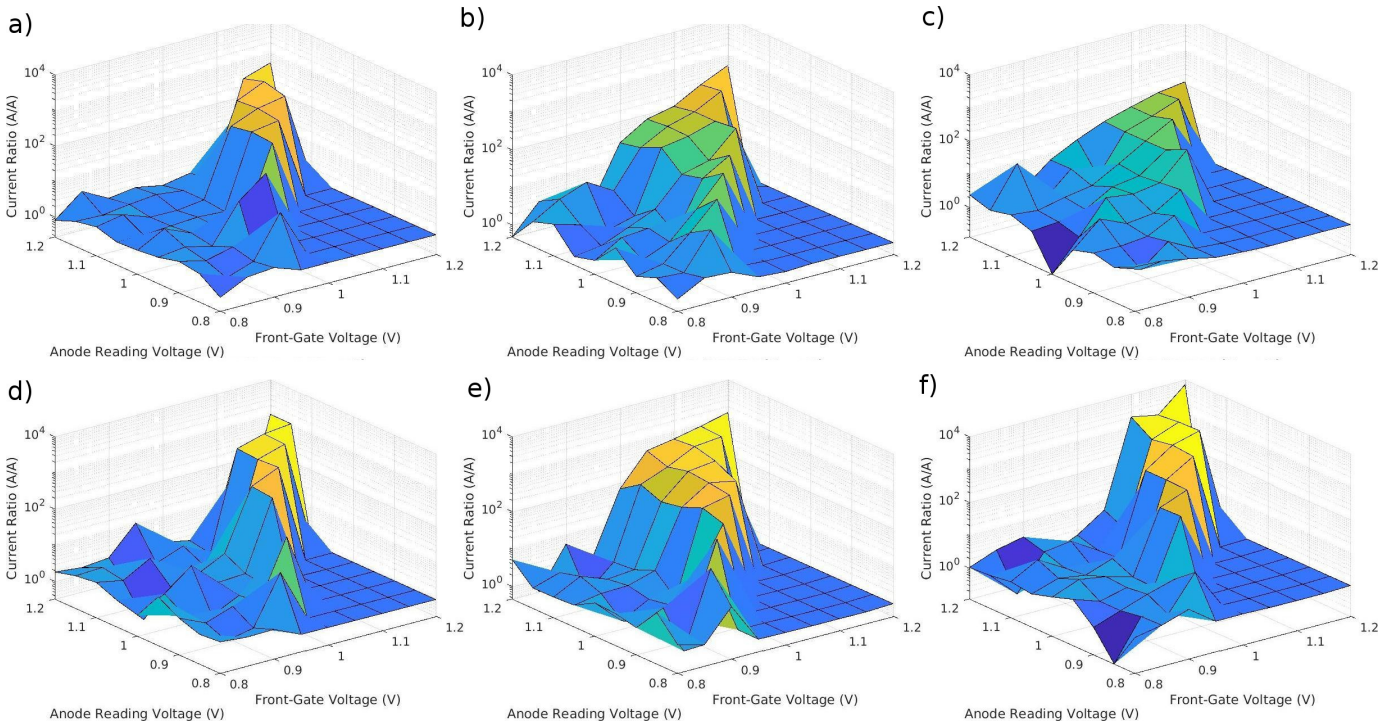

Fig. 8. Current ratio between logic states '1' and '0' as a function of V_{FG} and V_A. V_K (cathode) = 0 V and V_{BG} = -1 V for a) D1 b) D2 c) D3 (corresponds to the ratio of Fig. 7a to 7b) d) D4 e) D5 f) D6.

Since the operation of this cell depends on several parameters (V_{FG}, V_{BG}, V_{AW}, V_{AR}, ...), initial transient measurements are aimed to optimize the performance, i.e. the current ratio (I_1/I_0). The following bias points were initially tested for all devices: V_{FG} ranged from 0.8 to 1.2 V whereas V_A started at 0.5 to 1.2 V. The cell anode current readout is shown in Fig. 6 for D3 (other devices present similar behavior, not shown). The current ratio is high (with $I_1/I_0 \approx 44$) and the memory behavior is correct: two distinct readout current levels are achieved according to the last programmed state (W_0 or W_1). Note that the V_A bias can be smaller for writing than for reading, enabling substantial power saving. From all the transient results, the surface plots illustrated in Fig. 7 can be built. They represent the anode current for both logic states, I_1 and I_0, as a function of V_{FG} and V_{AR} for a fixed V_{BG} = -1 V for D3. It is worth noting that the D3 (W=0.1 μm) logic '1'-state anode current readout does not present an abrupt current switch as other wider cells, as D1 (W=1 μm), do (not shown). The absence of abrupt switching for D3 might be related, on the one hand, to a more effective electron injection (while W_1 at low V_A = 0.5 V): less carriers are required to collapse the energy barrier. On the other hand, width channel effects and especially, variability, may affect the barrier potential profiles. Fig. 8 depicts the I_1/I_0 current ratio for all reported devices. We can observe a functional region of biasing values ($V_A \leq V_{FG}$) from which the final biasing point was selected. This biasing point, Table II, was chosen to optimize the I_1/I_0 current ratio, but other policies such as minimum power consumption or supply voltages are easy to implement examining the cell transient responses.

TABLE II
BIASING CONDITIONS FOR TRANSIENT OPERATION. PULSES FEATURE $t_{r/f} = 50\ ns$ (RISE/FALL TIMES) WITH $t_w = 2\ \mu s$ (PULSE WIDTH).

Z²-FET Cell	W_0	W_1	R	H
Anode	0	0.5	1.15	0
Cathode	0	0	0	0
Front gate	0	0	1.2	1.2
Back gate	-1	-1	-1	-1

IV. MEMORY WINDOW

The memory window indicates the range of anode voltages in which the cell exhibits memory effect for a given timing and gate bias conditions. It is defined as the V_{ON} difference between the two logic states, so the larger it is the more robust the memory cell is against anode reading voltage variability. The memory window is extracted by monitoring the anode current level for different anode reading pulse voltages, see inset in Fig. 9a. The delay between the write and read operations is limited to 2 μs (close to the equipment limitations) in order to evaluate the best possible memory window. In real applications DRAMs are operated much faster so the memory window is expected to improve drastically. Fig. 9 depicts the experimental DRAM Z^2-FET memory window for all reported devices with the dashed line being the anode reading voltage used in Fig. 6.

Comparing the results by width (D_1, D_2 and D_3), the narrower the cell width is, the wider the memory window

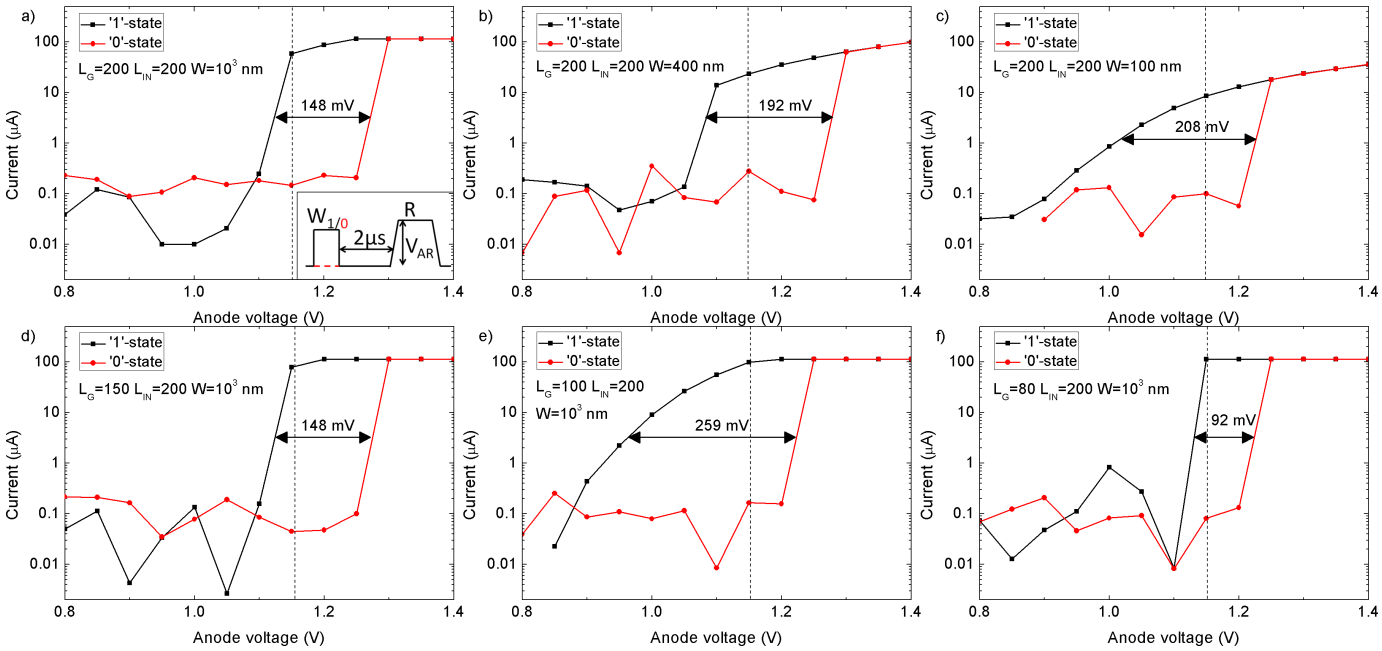

Fig. 9. Extracted memory window for reading pulses with $t_r = t_f = 50\ ns$ and $t_w = 2\ \mu$s for a) D1 b) D2 c) D3 d) D4 e) D5 f) D6. Dashed line corresponds to anode reading bias in Fig. 6.

seems to be, as was anticipated in the I_1/I_0 current ratio plots. This may be attributed to the logic '1'-state anode current not triggering, as explained in the previous section. Conversely, since the I_1 current is lower for thinner devices but the I_0 keeps almost constant, the current ratio across the memory window is poorer when the width is shortened. Comparing by gated length (D_1, D_4, D_5 and D_6), D_1 and D_4 exhibit a very similar memory window, whereas for D_6 it is much thinner.

V. Retention Time

The retention time is characterized with several $W_{1/0}$-H-R bias patterns, as illustrated in the inset of Fig. 10a. The holding (H) time is gradually increased from 20 μs to 70 ms, to monitor if the previously programmed state ($W_{1/0}$) is still available afterward. Consistent retention times are only reported for D_1, D_2 and D_3, Fig. 10, since for the remaining devices a different V_{AR} is required, thus a fair comparison is not possible. In contrast with other 1T-DRAM cells [5], [7] where the retention is enhanced when enlarging the width, the Z^2-FET retention seems to follow the opposite trend: it increases as the cell width is made narrower, obtaining times from 20 to 200 μs, Fig. 10. Due to the limited retention times observed, this unnatural trend might be an artifact originated by the strong variability these cells present (see following section). Indeed, previous Z^2-FET work featuring much wider cells yield much longer retention times, above tens of ms [8]. However, in such studies the cells featured a thicker top dielectric which might be also responsible for the retention

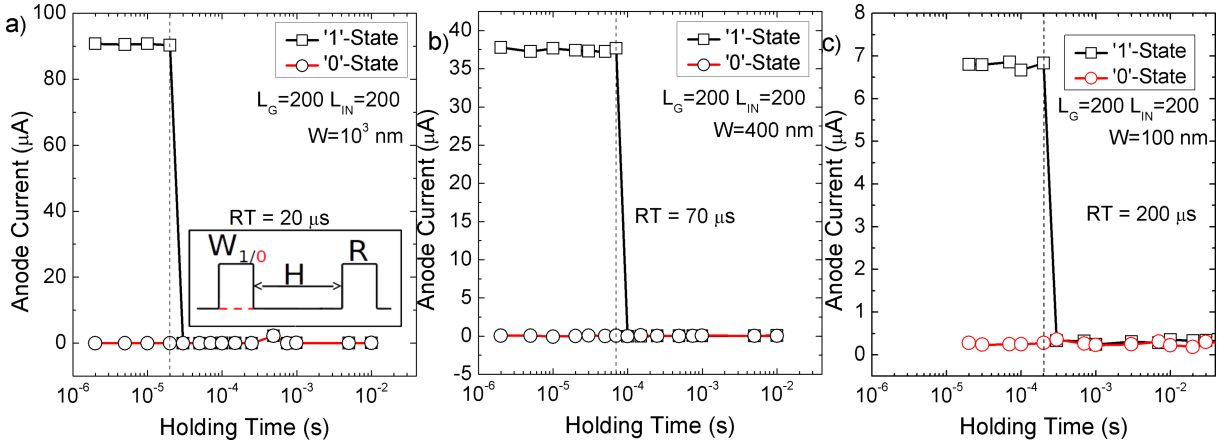

Fig. 10. Retention time (RT) for a) D1 b) D2 c) D3 with V_{AR} = 1.15 V. V_{FG}=1.2V, V_K = 0V and V_{BG} = -1V.

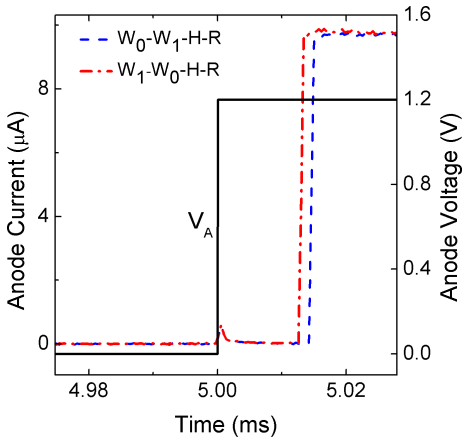

Fig. 11. Anode current readout in between the holding (H) and reading (R) (R triggered by the V_A voltage step) operations. Anode current levels are almost equal for both patterns, indicating the stored '1' and '0'-states are lost during the H and continuous R respectively.

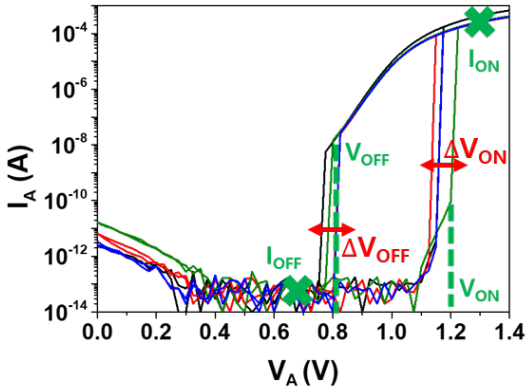

Fig. 12. Several examples of I_A-V_A characteristics of the Z^2-FETs in the wafer showing hysteresis at V_{FG} = 1.2 V. Four parameters (V_{ON}, V_{OFF}, I_{ON} and I_{OFF}) are extracted for variability analysis.

time enhancement. Further investigation is required. Notice also that, unexpectedly [8], [9], the stable state during holding seems to be the '0'-state (logic '1' falls toward the '0'). However, for continuous reading, the Z^2-FET cell always ends up driving the high-current '1'-state. Both facts can be observed in Fig. 11: after the holding time, the readout current corresponds inconditionally to the '0'-state (default value while holding). Later on, the anode current switches to the '1'-state (default state while continuous reading) in both cases. This surprising result, not observed in Z^2-FET with thicker gate dielectrics [8], is thought to be a consequence of the thinner oxide: the increased vertical electric field reinforces the energy barriers preventing the current flow ('0'-state). Additional recombination and/or evacuation mechanisms, e.g. direct gate tunneling, might also affect the memory operation. Nonetheless, during reading, the carrier injection can easily counteract any carrier gate leakage or recombination finally leading to the '1'-state.

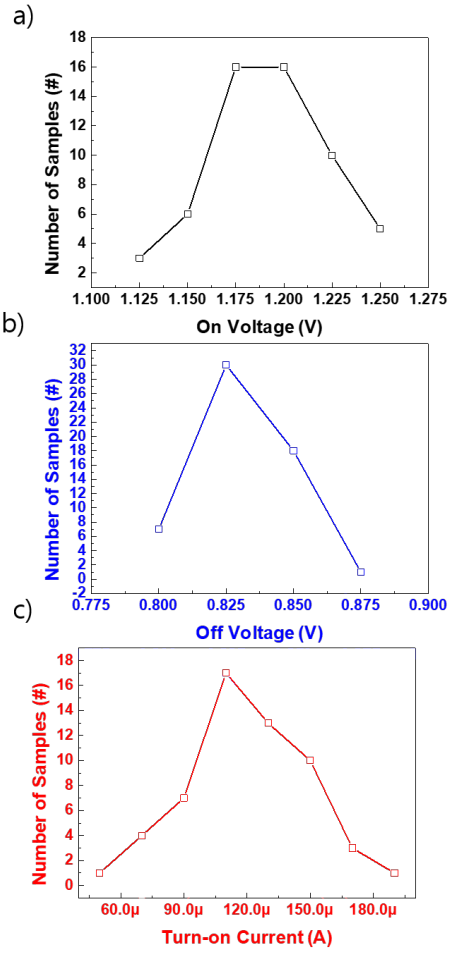

Fig. 13. Statistical distributions of a) ON voltage, b) OFF voltage and c) turn-on current for 56 Z^2-FETs. L_{IN} = L_G = 200 nm and W = 1 μm. V_{BG} = -1 V, V_{FG} = 1.2 V and V_K = 0 V.

VI. DC VARIABILITY

Statistical measurements of some Z^2-FET devices were performed to assess the wafer-level variability. A set of 56 devices were studied for the wafer-level variability at V_{FG} = 1.2 V. The test is based on the DC characteristics which provide the key parameters to be used in the memory operation measurement as shown in Fig. 12. Devices with L_G=L_{IN}=200 nm, W=1 and 0.1 μm are chosen and compared to evaluate the variability. Fig. 13 and 14 show the spreading of Z^2-FET parameters: a) ON voltage, b) OFF voltage and c) turn-on current. For the wider devices (Fig. 13), turn-on voltages (V_{ON}) range from 1.125 V to 1.250 V (ΔV_{ON} = 0.125 V) and turn-off voltages (V_{OFF}) from 0.8 V to 0.875 V (ΔV_{OFF} = 0.075 V). The turn-on currents vary from 50 to 190 μA. However, variability is severely degraded for narrow devices as shown in Fig. 14. Notice that the V_{ON} voltages range from 0.95 V to 1.3 V and V_{OFF} range from 0.75 V to 0.9 V. Similarly, the turn-on currents vary from 1 to 20 μA although the turn-off currents remain low. This variability makes the optimization of the biasing conditions in transient mode for the memory

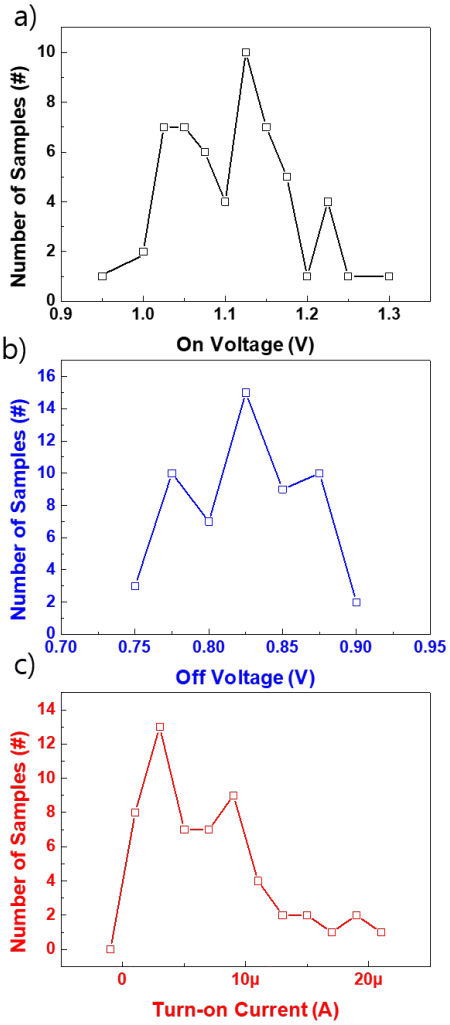

Fig. 14. Statistical distributions of a) ON voltage, b) OFF voltage and c) turn-on current for 56 Z^2-FETs. L_{IN} = L_G = 200 nm and W = 100 nm. V_{BG} = -1 V, V_{FG} = 1.2 V and V_K = 0 V.

performance difficult. Among the possible contributions to the increasing variability in narrow Z^2-FET cells, two sources can be highlighted: a larger relative width deviations from the layout mask design and the interface density of states (D_{it}) induced by the lateral shallow trench isolation (STI).

VII. Conclusion

Advanced narrow Z^2-FET memory cells with ultrathin gate oxide have been experimentally characterized. Retention times and memory windows have been determined for the first time. The memory operation is successfully demonstrated despite a performance drop with respect to previous results, due to increased variability, vertical electric field and gate leakage.

Acknowledgment

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References

[1] Semiconductor Industry Association, "International Technology Roadmap for Semiconductors (ITRS)", 2015.

[2] D. James, "Recent innovations in DRAM manufacturing", 2010 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (ASMC), San Francisco, CA, 2010, pp. 264-269. DOI: 10.1109/ASMC.2010.5551462

[3] J.-P. Colinge, "Silicon-On-Insulator Technology: Materials of VLSI", *Springer US,*, 2004. DOI: 10.1007/978-1-4419-9106-5

[4] S. Okhonin, M. Nagoga, J. M. Sallese, and P. Fazan, "A SOI capacitor-less 1T-DRAM concept", in 2001 IEEE International SOI Conference. Proceedings, Oct 2001, pp. 153–154. DOI: 10.1109/SOIC.2001.958032

[5] M. Bawedin, S. Cristoloveanu, and D. Flandre, "A Capacitorless 1T-DRAM on SOI Based on Dynamic Coupling and Double-Gate Operation", IEEE Electron Device Letters, vol. 29, no. 7, pp. 795–798, July 2008. DOI: 10.1109/LED.2008.2000601

[6] N. Rodriguez, C. Navarro, F. Gamiz, F. Andrieu, O. Faynot and S. Cristoloveanu, "Experimental Demonstration of Capacitorless A2RAM Cells on Silicon-on-Insulator", in IEEE Electron Device Letters, vol. 33, no. 12, pp. 1717-1719, Dec. 2012. DOI: 10.1109/LED.2012.2221074

[7] N. Rodriguez, F. Gamiz, C. Navarro, C. Marquez, F. Andrieu, O. Faynot, and S. Cristoloveanu, "Experimental developments of A2RAM memory cells on SOI and bulk substrates", Solid-State Electronics, vol. 103, pp. 7–14, jan 2015. DOI: 10.1016/j.sse.2014.09.001

[8] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "A compact capacitor-less high-speed DRAM using field effect-controlled charge

[9] C. Navarro, J. Lacord, M. S. Parihar, F. Adamu-Lema, M. Duan, N. Rodriguez, B. Cheng, H. E. Dirani, J. C. Barbe, P. Fonteneau, M. Bawedin, C. Millar, P. Galy, C. L. Royer, S. Karg, P. Wells, Y. T. Kim, A. Asenov, S. Cristoloveanu, and F. Gamiz, "Extended Analysis of the Z2-FET: Operation as Capacitorless eDRAM", IEEE Transactions on Electron Devices, vol. 64, no. 11, pp. 4486–4491, Nov 2017. DOI: 10.1109/TED.2017.2751141

[10] C. Navarro, M. Duan, M.S. Parihar, F. Adamu-Lema, S. Coseman, J. Lacord, K.H. Lee, C. Sampedro, B. Cheng, H. El Dirani, J.C. Barbe, P. Fonteneau, S.I. Kim, S. Cristoloveanu, M. Bawedin, C. Millar, P. Galy, C. Le Royer, S. Karg, H. Riel, P. Wells, Y.-T. Kim, A. Asenov and F. Gamiz, "Z^2-FET as Capacitor-Less eDRAM Cell For High-Density Integration", IEEE Transactions on Electron Devices, vol. 64, no. 12, pp. 4904-4909, Dec. 2017. DOI: 10.1109/TED.2017.2759308

[11] S. Cristoloveanu, K.H. Lee, M.S. Parihar, H. El Dirani, J. Lacord, S. Martinie, C. Le Royer, J.-Ch. Barbe, X. Mescot, P. Fonteneau, Ph. Galy, F. Gamiz, C. Navarro, B. Cheng, M. Duan, F. Adamu-Lema, A. Asenov, Y. Taur, Y. Xu, Y-T. Kim, J. Wan, M. Bawedin, "A review of the Z2-FET 1T-DRAM memory: Operation mechanisms and key parameters", Solid-State Electronics, 2017, ISSN 0038-1101, DOI:10.1016/j.sse.2017.11.012.

[12] S. Navarro, C. Navarro, C. Marquez, H. El Dirani, P. Galy, M. Bawedin, A. Pickering, S. Cristoloveanu, F. Gamiz, "Experimental Demonstration of Operational Z2-FET Memory Matrix", in IEEE Electron Device Letters, vol. 39, no. 5, pp. 660-663, May 2018. DOI: 10.1109/LED.2018.2819801 regeneration", IEEE Electron Device Letters, vol. 33, no. 2, pp. 179–181, 2012. DOI: 10.1109/LED.2011.2176908

[13] N. Planes, O. Weber, V. Barral, S. Haendler, D. Noblet, D. Croain, M. Bocat, P. O. Sassoulas, X. Federspiel, A. Cros, A. Bajolet, E. Richard, B. Dumont, P. Perreau, D. Petit, D. Golanski, C. Fenouillet-Branger, N. Guillot, M. Rafik, V. Huard, S. Puget, X. Montagner, M. A. Jaud, O. Rozeau, O. Saxod, F. Wacquant, F. Monsieur, D. Barge, L. Pinzelli, M. Mellier, F. Boeuf, F. Arnaud, and M. Haond, "28nm FDSOI technology platform for high-speed low-voltage digital applications", in 2012 Symposium on VLSI Technology (VLSIT). IEEE, 2012, pp. 133–134. DOI: 10.1109/VLSIT.2012.6242497

[14] Synopsys Inc. Sentaurus Device User Guide, version J-2014.09, 2014.