A Low-Power Low-Supply MOS-Only Subthreshold Voltage Reference for Wide Temperature Range

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Abstract. *A Sub-1V, MOS-only Voltage Reference Circuit (VRC) has been proposed with the utmost of transistors working as subthreshold region for low-supply and low-power applications. A supply-insensitive current is passed to Active Load Circuit (ALC) for supply and temperature independence at the output reference voltage. It has four current mirrors connected in a closed loop configuration to generate a supply-independent current which is passed through the ALC resulting supply and temperature insensitive output reference voltage. The ALC has a combination of two subthreshold NMOS transistors having different threshold voltages. The presented VRC is simulated using standard 90 nm CMOS model for 0.25-1 V supply voltage range. The simulation result gives minimum operating voltage required as 0.25 V for which all transistors work in their respective region of operation. For the supply range of 0.25-1 V, the obtained mean voltage reference is 100.4 mV with the line regulation of 0.186 mV/V. The Temperature Coefficient (TC) of 51 ppm/° C is achieved for a wide temperature range of -50 to 135 °C with the given minimal operating supply voltage. The power dissipation for minimal supply voltage at room temperature is 33 nW. The proposed VRC exhibits a high PSRR of -52.5 dB at 100 Hz and -29 dB at 1 MHz.*

Keywords

Current mirror, low-power, low-voltage, sub-1V circuit, subthreshold MOS.

1. Introduction

The reference voltage generator circuits are the vital block of analog as well as the mixed analog System on Chip (SoC). These are used virtually in every digital and analog system to generate a biasing voltage insensitive to temperature, supply voltage, and process parameters. For the need of ultra-low-power and low-voltage applications like portable multimedia devices and compact medical devices, the use of BJTs for conventional bandgap references is restricted as it cannot satisfy the demand of low-power, as well as compact area requirements of today's need of technology as it has bulky size and higher bandgap voltage i.e. in the range of around 1.2 [1]. This demand of low-voltage and low-power applications is fulfilled by a Sub-1V VRCs with most of the MOS transistors of the designed circuit operating in the subthreshold region.

Many of the recent studies for generating reference voltage and current focus on the subthreshold region operation of MOSFET devices and the VRCs employing MOSFETs operating in the subthreshold region have emerged as the core research area for low-voltage and low-power applications [2] and [3]. The previously designed VRCs employing resistors and BJTs [4], [5], [6], [7], [8], [9], [10], [11] and [12] has larger area occupation, power dissipation, and need high supply. Then, the CMOS VRCs employing the subthreshold operating MOS transistors using resistors as in [13], [14], [15] and [16] employed for low-power circuits. Now, the new circuits without using resistors and BJTs are proposed in [17], [18], [19], [20], [21], [22], [23] and [24]. Another resistorless VRC is proposed in [25], which has used two different types of transistors as High V_{TH} (HVT) and Standard V_{TH} (SVT) for generating the supply-independent current. Here HVT works in the subthreshold region and other transistors work in the sat-

uration region. This circuit has supply voltage range of 0.9 V to 4 V and has supply current of 40 nA at 0.9 V supply. It gives reference voltage of 670 mV. Another CMOS subthreshold VRC for low-voltage and low-power without resistor and BJT is presented in [21]. It has used a bulk driven technique to generate the supply independent current where most of the transistors are working in the subthreshold region. It reduces power by using bulk driven technique and the subthreshold MOS operation. It has PSRR of −44 dB at 100 Hz and line regulation of 1.7 mV/V. In [27], a resistorless VRC is implemented using BJTs for better power supply noise attenuation and low TC. Its output voltage is a combination of CTAT, threshold voltage and PTAT voltage. All its transistors are working in strong inversion region hence it has high working voltage with power dissipation in around microwatts. The above discussion concludes that most of the reported circuits operate at high supply voltage and have higher power dissipation. They also have high power supply noise effect at the output.

The presented work is a circuital modification to the work presented in [21] to overcome the performance parameters especially in terms of PSRR and Line Regulation. The proposed work is a Sub-1V, Looped Current Mirror Voltage Reference (LCMVR) using MOS-only transistors operating in the subthreshold region for a very low-supply voltage of only 0.25 V resulting in low output generated current, hence reduced power dissipation. The looped current mirror network provides extra transconductance and output resistance terms for improving PSRR than [21] and [26]. The proposed LCMVR provides a current of 131.8 nA with 0.25 V supply voltage at room temperature. This current is fed through the ALC to have temperature independence of output voltage. The obtained output voltage is 100.4 mV with the TC of 51 ppm/°C at 0.25 V supply.

The remaining contents of this paper are organized in the following sections. Section 2. explains the basic operating principle of the proposed LCMVR. The mathematical analysis for the CGC and the ALC of the proposed LCMVR is given in Sec. 3. Section 4. explains the design consideration of the proposed VRC. The analysis of simulation results and its comparison with the recent works for low-power application is discussed in Sec. 5. The conclusion of the paper is given in Sec. 6.

2. Operating Principle

There are different ways to design a VRC and one of the ways is by using the subthreshold operation mode of transistors. The basic operating principle is shown in Fig. 1, where utmost of the transistors are operating in the subthreshold region. All the transistors of the proposed core circuit are having SVT except M5 as HVT. The HVT transistor shown in Fig. 1 is represented by a thicker line for gate region. The HVT transistor is body biased with V_{GS6} to reduce the effect of temperature variation on the output voltage. A supply-independent current is mirrored to ALC having transistors M2-M6 operating in the subthreshold region. The NMOS transistor operating in the subthreshold region has a current in relation to an exponential function of drain to source voltage, V_{DS} and gate to source voltage, V_{GS} which is given by [26] as:

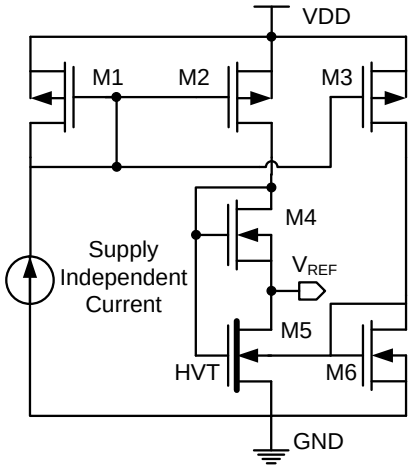

Fig. 1: Basic operating principle of proposed VRC.

$$I_{sub} = I_o \left(\frac{W}{L}\right) \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) \left[1 - \exp(-\tfrac{V_{DS}}{V_T})\right], \quad (1)$$

where $I_o = \mu C_{ox} (\eta - 1) V_T^2$, V_{TH} is the threshold voltage of the MOS, μ is the mobility of the carrier, C_{ox} is the gate-oxide capacitance per unit area, W/L is the aspect ratio, η is the subthreshold slope parameter and V_T is the thermal voltage. For $V_{DS} \gg V_T$, the current I_{sub} is nearly independent of V_{DS} and given as:

$$I_{sub} = I_o \left(\frac{W}{L}\right) \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right). \quad (2)$$

From Fig. 1, the V_{REF} obtained as the difference of gate to source voltages of M4 and M5 as:

$$V_{REF} = V_{GS5} - V_{GS4}. \quad (3)$$

Further, the temperature compensation is obtained by selecting required aspect ratio for transistors M4, M5, and M6 obtained by the condition when

$$\frac{\partial V_{REF}}{\partial T} = 0. \quad (4)$$

This gives a voltage reference, V_{REF} as invariant as possible to both supply voltage as well as the temperature variations.

3. Circuit Description

The proposed VRC consists of start-up circuit, supply independent Current Generator Circuit (CGC) followed by an ALC is shown in Fig. 2. The start-up circuit is used to bias different transistors in their respective mode of operation avoiding undesirable zero current mode. The CGC uses transistors numbered from M1 to M9, where all the transistors operating in the subthreshold region except two transistors M2 and M9, operating in saturation and moderate inversion, deep-triode region, respectively. This CGC produces a nano-ampere current which is almost insensitive to the supply voltage variations. This current is passed through the ALC which consists of transistors numbered from M10 to M14 to generate a temperature insensitive output reference voltage, V_{REF}. The following sections will explain the operation in details.

3.1. Current Generator Circuit

To obtain a nano-ampere supply current reference, the looped current mirrors are used along with bulk-driven transistors without any resistance, as shown in Fig. 2. This CGC delivers a current as insensitive as possible to power supply variations, as shown in Fig. 11. The concept of the looped current mirror is employed by using four current mirrors used to bootstrap the output current I_8 to the I_7 branch to give a supply independent output current. Here, V_{DD} independent current will circulate around the loop, sustaining similar nature of current in left and right branches as I_7 and I_8 indefinitely. This loop of the current mirror reduces the effect of supply voltage variation on the generated current; hence the output reference voltage has better PSRR and better line regulation than [21].

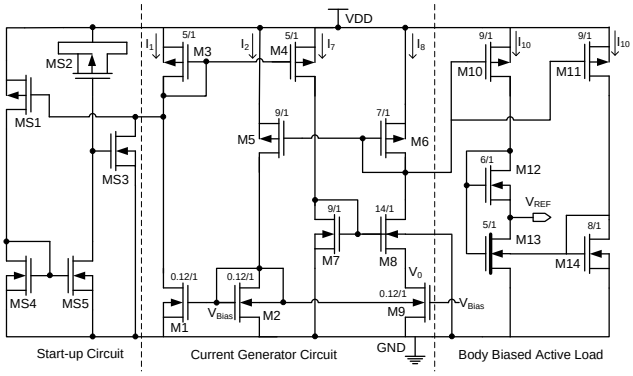

Fig. 2: Schematic of the Core circuit of proposed LCMVR.

The core components of the current generation circuit include the transistors M1, M2, M7, M8 and M9 defining the value of generated nano-ampere current, I_8. The transistors M3 and M4 provide equal current to transistors M1 and M7 and transistors M5 and M6 copy the current of transistor M8 to transistor M2 in the ratio of K_5/K_6. The transistors M2 and M9 are biased to work in saturation and moderate inversion, deep-triode region of MOS, respectively. The saturation current of MOS is given by

$$I_{sat} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}), \quad (5)$$

where λ is the channel length modulation constant.

The transistors M2, M8 and M9 are having the effect of body biasing on its threshold voltage. The expression of the threshold voltage for body effect is given by [23] as:

$$\begin{aligned} V_{TH} &= V_{TH0} + \gamma\left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F}\right) \\ &\approx V_{TH0} + (\eta - 1)V_{SB}, \end{aligned} \quad (6)$$

where Φ_F is the Fermi potential, V_{TH0} is the threshold voltage with no body bias, V_{SB} is the source to body voltage, and γ is the body effect coefficient of the MOSFET.

The transistor M9 biased in the deep-triode region works as a MOS resistor and its resistance is given by

$$R_9 = \frac{1}{\mu_n C_{ox} K_9 (V_{GS9} - V_{TH9})}. \quad (7)$$

From Fig. 2, it is observed that

$$V_{GS7} = V_{GS8} + V_o. \quad (8)$$

As M7 and M8 are working in the subthreshold region, then from Eq. (2) and Eq. (8), we get the expression of V_o as:

$$V_o = V_{TH7} - V_{TH8} + \eta V_T \ln\left(\frac{K_8}{K_7}.\frac{I_7}{I_8}\right), \quad (9)$$

where I_7 and I_8 are the currents of transistor M7 and M8, respectively. The current ratio is given by used current mirrors:

$$\frac{I_7}{I_8} \approx \frac{K_5}{K_6}. \quad (10)$$

From Eq. (6), Eq. (9) and Eq. (10), we get the following expression for V_o as

$$V_o \approx V_T \ln\frac{K_5 K_8}{K_6 K_7}. \quad (11)$$

From Eq. (7) and Eq. (11), we get

$$I_8 = \frac{V_o}{R_9} = \mu_n C_{ox} K_9 \left(V_{GS9} - V_{TH9}\right) V_T \ln\left(\frac{K_5 K_8}{K_6 K_7}\right). \quad (12)$$

Considering the biasing conditions of transistors M2 and M9 and neglecting the channel length modulation ($\lambda = 0$), following is observed:

$$V_{GS9} - V_{TH9} = V_{GS2} - V_{TH2} = \sqrt{\frac{2I_2}{\mu C_{ox} K_2}} = \sqrt{\frac{2K_5 I_8}{\mu C_{ox} K_6 K_2}}. \quad (13)$$

By substituting the value of $(V_{GS9} - V_{TH9})$ in Eq. (12) and simplifying, we get

$$I_8 = 2\mu_n C_{ox} V_T^2 \frac{K_5 K_9^2}{K_6 K_2} \left[\ln\left(\frac{K_5 K_8}{K_6 K_7}\right)\right]^2. \quad (14)$$

The current expression obtained by Eq. (14) is insensitive to the supply voltage. Further, this supply independent current is fed to the ALC transistors operating in the subthreshold region for temperature compensation.

3.2. Active Load Circuit

The ALC has transistors numbered from M10 to M14, operating in the subthreshold region. The supply independent current, I_8 is injected to ALC via PMOS current mirror consisting transistors M6, M10, and M11. In Fig. 2, the gate to source voltage difference of transistor M12 and M13 gives expression of V_{REF} which is given by using Eq. (2) and Eq. (3) as:

$$V_{REF} = V_{TH13}^* - V_{TH12} + \eta V_T \ln\left(\frac{K_{12}}{K_{13}}\right), \quad (15)$$

where V_{TH13}^* is body biased threshold voltage of M13 which is given by Eq. (2) and Eq. (6) as:

$$V_{TH13}^* = V_{TH013} - (\eta - 1)V_{TH0} - \eta(\eta - 1)V_T \ln\left(\frac{K_{11} I_8}{I_o K_6 K_{14}}\right), \quad (16)$$

where V_{TH013} is zero body biased threshold voltage of HVT transistor M13 and V_{TH0} is zero body biased threshold voltage of SVT transistors.

Finally, the output reference voltage, V_{REF} from Eq. (15) and Eq. (16) is given as:

$$V_{REF} = \eta V_T \ln\left(\frac{K_{12}}{K_{13}}\right) - \eta V_{TH0} + V_{TH013} - \eta(\eta - 1)V_T \ln\left(\frac{K_{11} I_8}{K_6 K_{14} I_o}\right). \quad (17)$$

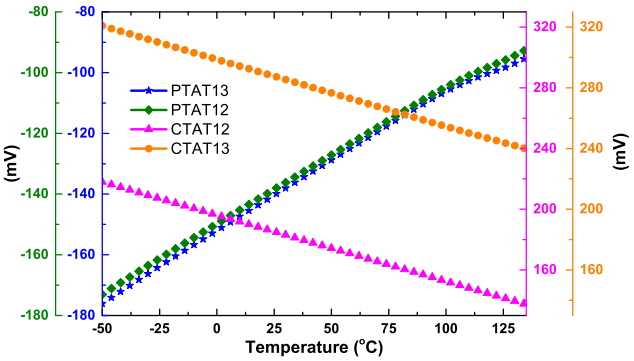

Fig. 3: The variation of CTAT and PTAT voltage w.r.t. temperature.

The first two terms of Eq. (17) represent a PTAT voltage and the last two terms represent a CTAT voltage. The combination of these PTAT and CTAT voltage gives an output voltage independent of temperature variations. By adjusting the transistor dimensions of Eq. (17), a temperature and supply independent output reference voltage is obtained. From Eq. (2), the V_{GS} of transistors operating in the subthreshold region consists of CTAT threshold voltage and PTAT thermal voltage. The variation of CTAT and PTAT components of V_{GS12} and V_{GS13} is shown in Fig. 3. From Eq. (3), the subtraction of these two V_{GS} voltages of M12 and M13 result in a temperature independent output reference voltage.

3.3. Start-Up Circuit

The start-up circuit consists of transistors numbered from MS1 to MS5, and is shown in Fig. 2. It is similar to the one proposed in [21] but differ in the way start-up transistors are connected to lower the gate voltage of PMOS transistor M3. Here, transistor MS2 is made to work as a capacitor used to turn off the transistor MS3 when core circuit of proposed LCMVR is working in normal mode to save the further power dissipation by start-up circuit components. When the power supply voltage is turned ON, it charges the MOS-capacitor MS2 to high, turning MS3 ON. This will lower the gate of M3 to start the looped CGC and the whole reference circuit, and subsequently, MS1 starts conducting using current mirror consisting of MS4 and MS5. Consequently, MS2 is discharged to a lower voltage resulting MS3 turns OFF, separating start-up circuit from the core part of the circuit for power saving.

3.4. PSRR Analysis

The PSRR (Power Supply Rejection Ratio) is analyzed using a small-signal model of the proposed LCMVR. Figure 4 shows the small-signal equivalent of the out-

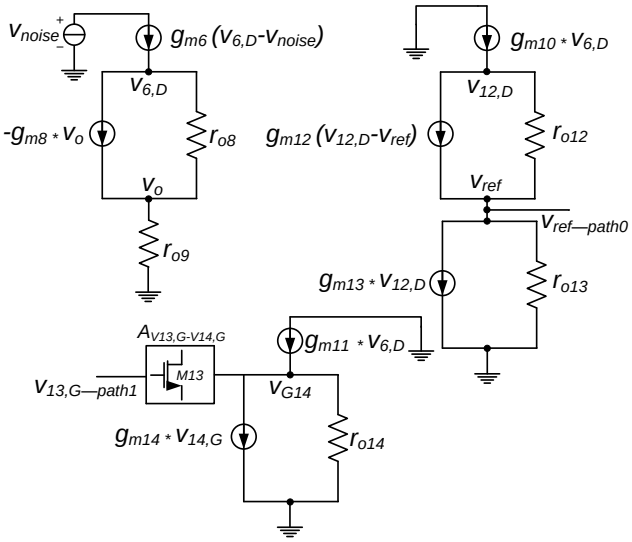

Fig. 4: Small-signal equivalent of output branch of CGC and ALC for *path*0 and *path*1 of the proposed LCMVR circuit.

put branch of the CGC and ALC. Here, output resistance, r_o and transconductance, g_m of the subthreshold transistors using Eq. (1) is given as

$$r_o = 1/\frac{\delta I_D}{\delta V_{DS}} \approx \frac{V_T}{I_D}\exp\frac{V_{DS}}{V_T}, \tag{18}$$

$$g_m = \frac{\delta I_D}{\delta V_{GS}} \approx \frac{I_D}{\eta V_T}. \tag{19}$$

Here, the noise effect is considered in CGC. This noise effect is contributed to the output reference voltage through current mirrors in the ALC. The noise effect from M6 of CGC to ALC via current mirror M10 and M11 is taken as *path*0 and *path*1 respectively. Considering the *path*0, following equations can be derived from Fig. 4 using KVL and KCL as:

$$v_o = r_{09}g_{m6}(v_{6,D} - v_{noise}), \tag{20}$$

$$v_{6,D} - v_o = r_{o8}g_{m6}(v_{6,D} - v_{noise}) + r_{o8}g_{m8}v_o, \tag{21}$$

$$v_{12,D} - v_{ref} = r_{o12}g_{m10}v_{6,D} - r_{o12}g_{m12}(v_{12,D} - v_{ref}), \tag{22}$$

$$g_{m13}v_{12,D} + \frac{v_{ref}}{r_{o13}} = g_{m10}v_{6,D}. \tag{23}$$

From Eq. (20) and Eq. (21), we get the value of $v_{6,D}$ as:

$$v_{6,D} = \frac{r_{o8}g_{m6}(1 + r_{o9}g_{m8})}{r_{o8}g_{m6}(1 + r_{o9}g_{m8}) - 1} \times v_{noise} = C_1 \times v_{noise}, \tag{24}$$

$$\text{where} \quad C_1 = \frac{r_{o8}g_{m6}(1 + r_{o9}g_{m8})}{r_{o8}g_{m6}(1 + r_{o9}g_{m8}) - 1}.$$

From Eq. (22) and Eq. (24), we get the value of $v_{12,D}$ as:

$$v_{12,D} = \frac{v_{ref}(1 + r_{o12}g_{m12}) + r_{o12}g_{m10}C_1v_{noise}}{1 + r_{o12}g_{m12}}. \tag{25}$$

From Eq. (23), Eq. (24), and Eq. (25), the expression for noise contribution to v_{ref} by *path*0 is given as:

$$v_{ref-path0} = \frac{g_{m10}}{g_{m12}g_{m13}}(g_{m12} - g_{m13})C_1v_{noise}. \tag{26}$$

Considering the *path*1, following equation can be derived from Fig. 4 using KVL as:

$$v_{14,D} = r_{o14}[g_{m11}v_{6,D} - g_{m14}v_{14,G}]. \tag{27}$$

The noise effect on body biased threshold voltage of M13 can be observed by Eq. (6) as:

$$\Delta V_{TH13} \approx -(\eta - 1)\Delta V_{bias} = -(\eta - 1)\Delta v_{GS14}. \tag{28}$$

This noise effect from *path*1 on body biased V_{TH} directly affects the V_{GS13}. Consecutively, this change in the threshold voltage changes the output reference voltage. Thus, the voltage gain is given as:

$$A_{v_{13,G}-v_{14,G}} = -(\eta - 1). \tag{29}$$

Then, from Eq. (24), Eq. (27), and Eq. (29) the expression for noise content in V_{REF} by *path*1 is given as

$$v_{v_{13,G}-path1} = -(\eta - 1)\frac{g_{m11}}{g_{m14}} \times C_1 \times v_{noise}. \tag{30}$$

It can be observed that Eq. (26) and Eq. (30) are of opposite nature resulting in reduced noise content at the output. Thus, adding Eq. (26) and Eq. (30) gives a reduced total noise content at the output reference voltage in terms of r_o and g_m of different transistors. By adjusting the terms present in Eq. (26) and Eq. (30), the noise content of output reference voltage can be reduced with improved PSRR of the proposed LCMVR.

4. Design Consideration

4.1. Transistor Biasing

The CGC comprises of transistors M2, M3, M6 and M7 in diode-connected mode resulting in most of the supply voltage drop on the other transistors connected in these branches *i.e.* M1, M4, M5, M8 and M9. The V_{TH} of M2 and M9 is found to be 121 mV and the V_{TH} of M1 is 137 mV then the V_{GS} of these transistors are made to 124 mV to make sure M2 is biased

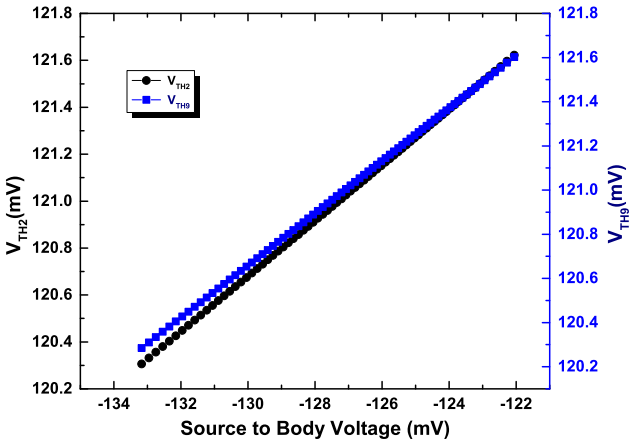

Fig. 5: The variation of V_{TH2} and V_{TH9} of proposed LCMVR for variation in source to body voltage.

in saturation, M9 is biased in deep triode region, and M1 is biased in the subthreshold region. Further, it can be noted that the condition for deep-triode region operation of M9 is $V_{DS} << 2V_{dsat}$, which is satisfied with $V_{DS9} = 26$ mV and $V_{dsat9} = 57$ mV. When I-V characteristic is plotted for M9, it gives a linear relation verifying the voltage-dependent resistor nature of M9.

Here, it can be noted that since each diode-connected device is nursed by a current mirror then the output current will be independent of the supply voltage. The branches I_1 and I_2 are used to provide a biasing for deep-triode region transistor M9 working as a resistor and also it provides more parameters to control the PSRR and output noise.

4.2. Minimum Supply Current

The current consumption is mainly due to the transistor M2 and M9, where M2 is operating in saturation region, and M9 is operating in the deep-triode region. The dimensions of transistor M2 and M9 are selected as the minimum possible value of W_{min}/L_{max} to reduce the circuit current consumption. The current in M2 can be given as:

$$I_2 = \frac{K_5}{K_6} I_8. \tag{31}$$

Further, I_2 is reduced by reducing the ratio K_5K_8/K_6K_7 to minimum possible such that the PSRR should maximize which is decided by the high conductance of the transistor M8. Also, the transistor M1 is minimal sized to reduce the feedback current to M7 resulting in the lower supply current. The dimensions of all transistors of proposed LCMVR, in Width (µm)/Length (µm) format for respective MOSFET is shown in Fig. 2. Here, higher transistor length is taken to minimize the channel length modulation effect.

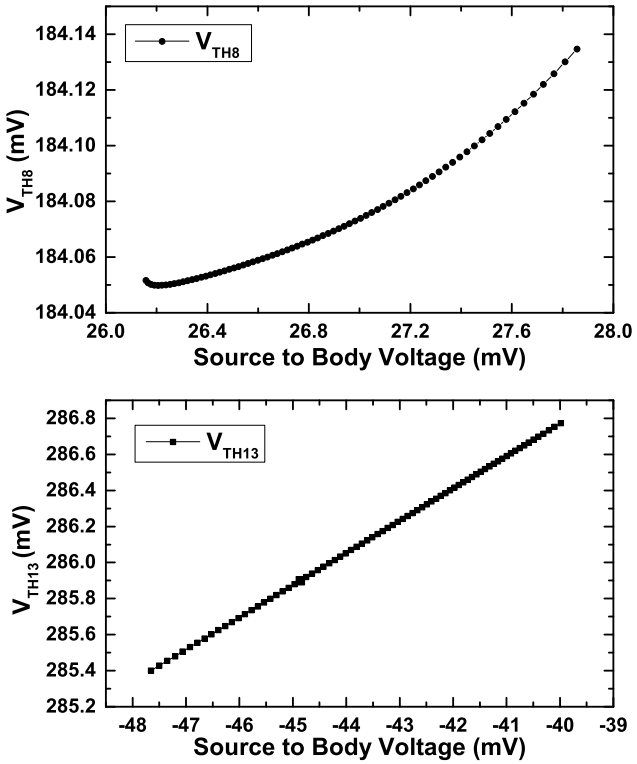

Fig. 6: The variation of V_{TH8} and V_{TH13} of proposed LCMVR for variation in source to body voltage.

4.3. Body Biased Transistors

The proposed LCMVR uses body biased transistors operating in their respective mode of operation. The analysis of the threshold voltage of these body biased transistors is shown in Fig. 5 and Fig. 6. This indicates very less variation of the threshold voltage of different body biased transistors with respect of source to body voltage variation for complete operating range of supply voltage from 0.25 V to 1 V. Further, it is observed that these body biased transistors have very low i_{bs}, i_{bd}, and i_{bulk} in order of pico or femto amperes. Therefore, it is concluded that there is no latch-up or bulk diode forward bias due to these body biased transistors.

5. Simulation Results

5.1. Simulation Framework

The proposed Sub-1V, subthreshold MOS-only LCMVR is implemented in 90 nm CMOS technology. The minimum supply voltage of 0.25 V is used for circuit simulations. Cadence Virtuoso EDA tool with SPECTRE simulator is used for simulation purposes. The variability analysis is done using Monte Carlo analysis for 0.25 V supply voltage at

room temperature. The line regulation is given by $\Delta V_{REF}/\Delta V_{DD}$ in mV/V and the TC is expressed as $\Delta V_{REF} \times 10^6/(\Delta T \times Average\ V_{REF})$ in ppm/°C. Figure 7 shows the extracted layout of the proposed LCMVR having an active area of 0.000268 mm^2.

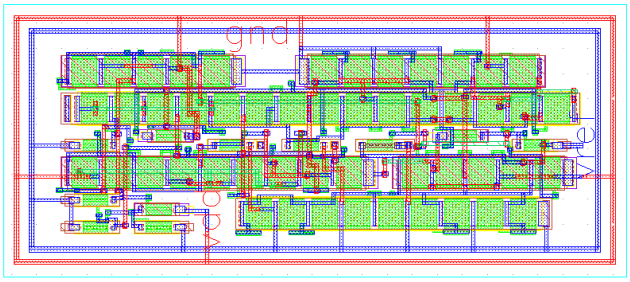

Fig. 7: The extracted layout of the proposed LCMVR with a length of 24.86 µm and width of 10.81 µm as active area.

5.2. Result Analysis

In Fig. 8, the output voltage, V_{REF} is shown for the variation of the supply voltage at different corners. It can be observed that for all the process corners, the output V_{REF} is almost constant for the supply voltage larger than around 0.25 V. Therefore, the minimum possible supply for proposed LCMVR is 0.25 V for which all the transistors work in their respective region of operation. The average output reference voltage and line regulation obtained for 0.25 to 1 V supply variation for room temperature is 100.4 mV and 0.186 mV/V, respectively. This low LR is possible due to looped current mirror configuration used for supply independent current represented by Eq. (17). The worst case value of line regulation is 4m V/V when the circuit is operated at FS corner. When V_{DD} is taken up to 1.4 V, the line regulation is 1.46 mV/V.

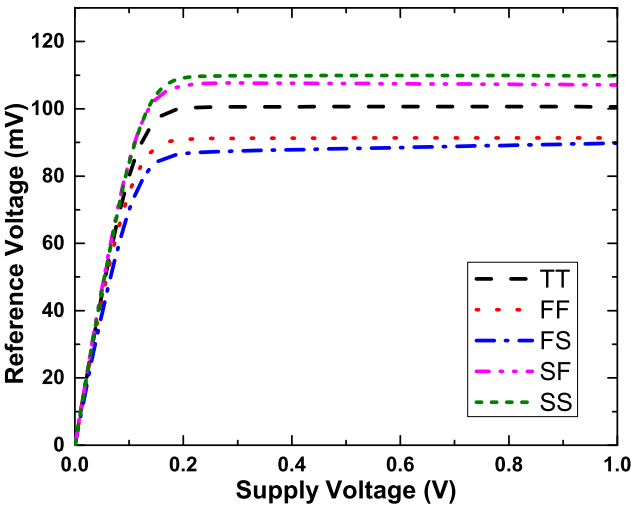

Fig. 8: V_{REF} vs V_{DD} of proposed LCMVR at different process corners.

In Fig. 8, when NMOS is fast, the V_{REF} is lower than typical value as the difference of threshold voltage of M12 and M13 is less due to the lower threshold voltage of HVT and SVT transistors for the fast corner. Similarly, for the slow corner of NMOS, the V_{REF} is higher than typical value. When PMOS is fast, V_{TH10} is low hence V_{DS10} is low. But $V_{DS10} + V_{GS13}$ is constant to V_{DD}, so V_{GS13} is high resulting V_{REF} higher. Similarly, when PMOS is slow, the V_{REF} is lower than when PMOS is fast.

Figure 9 shows the variation of output voltage, V_{REF} with respect to change in temperature from −50 to 135 °C for four different power supply variations between 0.25 to 1 V. For a temperature ranging from −50 to 135 °C, the variation of V_{REF} is best at 0.25 V supply than other supply ranges. The value of V_{REF} is around 100.4 mV for all the supply ranges near room temperature. Because of the threshold voltage terms in the output reference voltage, there is a slight change in V_{REF} for temperature other than room temperature for different supply variations. At 0.25 V supply, the minimum and maximum value of V_{REF} is 99.7 mV and 100.65 mV, respectively, giving a TC of around 51 ppm/°C. The worst case value of TC is observed at 1 V supply, giving TC of around 240 ppm/°C. Figure 10 shows the variation of V_{REF} with temperature at different process corners. The V_{REF} is almost constant for all corners except at FS and SF corners. The worst case TC is around 450 ppm/°C and 250 ppm/°C at FS and SF corners respectively.

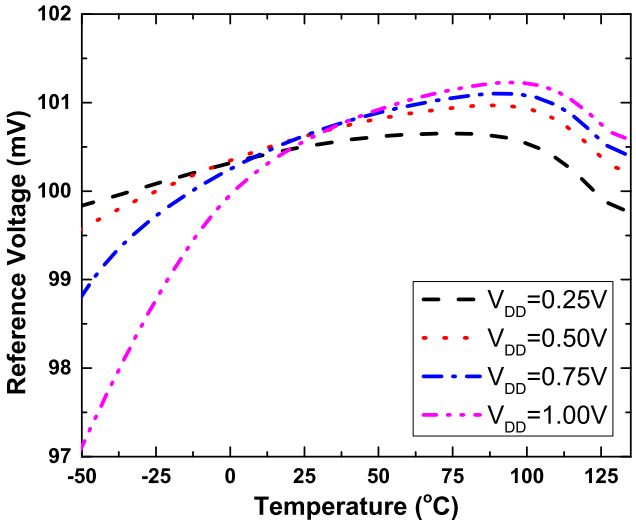

Fig. 9: V_{REF} vs Temperature of proposed LCMVR at the different supply voltage.

Figure 11 shows the variation of supply current at different V_{DD} for different process corners. It shows less variation w.r.t. V_{DD} but slight variation for process corners. The supply current of 131.8 nA is recorded for 0.25 V supply at 27 °C for typical corner. This gives the minimum power dissipation of around

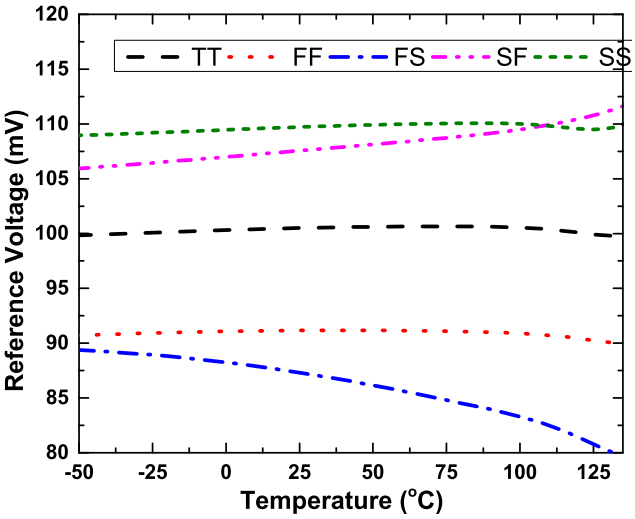

Fig. 10: V_{REF} vs Temperature of proposed LCMVR for different process corners.

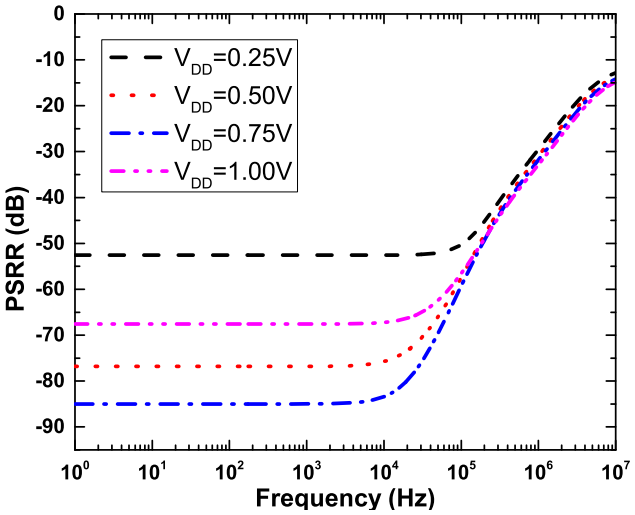

Fig. 12: PSRR of the proposed LCMVR at different power supplies for frequency varying from 1 Hz to 10 MHz at room temperature.

33 nW. When V_{DD} is increased beyond 1 V up to 1.4 V, the variation of supply current is large, so V_{DD} is taken up to 1 V only. The maximum and minimum value of supply current is 273 nA and 55 nA at FF and SS corners, respectively, for 0.25 V supply. The worst case value of supply current at TT corner is around 183 nA at 1 V. Similarly, the worst case power dissipation is around 68.25 nW at 0.25 V supply for FF corner.

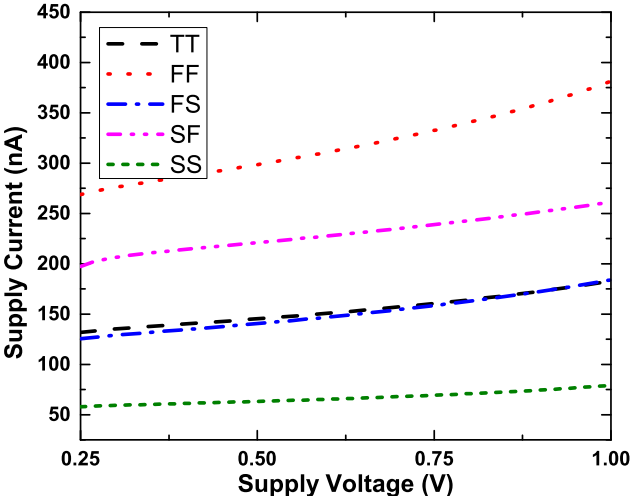

Fig. 11: Supply Current vs V_{DD} of proposed LCMVR at different process corners.

Figure 12 shows the PSRR of the proposed LCMVR obtained by simulating the proposed circuit for 1 V of AC magnitude in AC analysis with frequency ranging from 1 Hz to 10 MHz for different supply variations. The PSRR of the proposed LCMVR circuit is around −52.5 dB at 100 Hz and −29 dB at 1 MHz for 0.25 V supply at room temperature. The maximum and minimum value of PSRR for positive supply voltage is obtained at 0.75 V and 0.25 V, respectively. For 0.25 V supply at room temperature, the PSRR is best at FF corner and worst at FS corner valued −54 dB and −44 dB, respectively. At FF corner, the conductivity of transistors is high, resulting in higher PSRR.

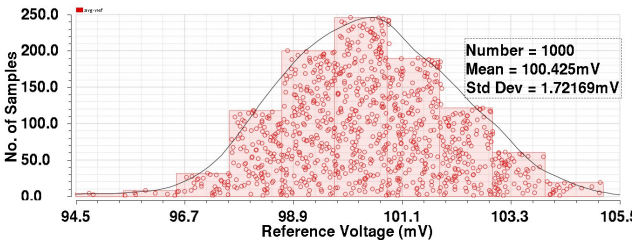

Fig. 13: Histogram of output reference voltage, V_{REF} for 1000 samples with V_{DD}=0.25 V at room temperature using Monte Carlo simulation for typical corner.

Tab. 1: Monte Carlo simulation Results of V_{REF} for 1000 samples with V_{DD}=0.25 V at room temperature for different corners.

V_{REF}(mV)	FF	FS	TT	SF	SS
Minimum	86.24	71.28	95.49	101.9	104.7
Maximum	94.95	94.74	104.3	111.8	113.5
Mean (μ)	91.17	87.31	100.4	107.4	109.6
SD (σ)	1.72	4.23	1.74	1.95	1.77

The sensitivity of the output reference voltage, V_{REF}, is evaluated using a 1000 point Monte Carlo simulation by considering the mismatch and process variations in all the transistors of the proposed circuit. The histogram of V_{REF} after Monte Carlo simulation with V_{DD} = 0.25 V at room temperature is shown in Fig. 13 for typical process corner. This results in a mean value of 100.425 mV and the standard deviation, (σ) of 1.72 mV. Also, the complete result of Monte Carlo simulation for different corners is compiled in Tab. 1. Figure 14 shows the histogram of V_{REF} for

Monte Carlo simulation with the varying temperature at V_{DD} = 0.25 V for typical corner. It results in a mean of 100.176 mV and σ of 1.68 mV, which is comparable to results obtained in Fig. 13. This shows that the LCMVR is less dependent on mismatch and process variation effects.

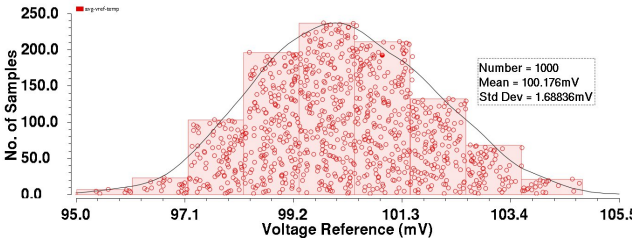

Fig. 14: Histogram of output reference voltage, V_{REF} for 1000 samples with temperature varying from -50 to 135 °C at V_{DD}=0.25 V using Monte Carlo simulation for typical corner.

Figure 15 shows the output noise spectral density of the output reference voltage without using any filtering capacitor from 0.1 Hz to 1 MHz. The root mean square (rms) value of output reference voltage noise integrated from 0.1 Hz to 10 Hz is 15.73 µV. The output noise at 10 Hz and 100 Hz is around 2.11 µV/$\sqrt{\text{Hz}}$ and 0.942 µ =V/$\sqrt{\text{Hz}}$, respectively. From the noise analysis of the circuit, it is noted that the flicker noise of transistors M12 and M13 are the dominant noise sources for the frequency ranging from 0.1 Hz to 550 Hz, while the thermal noise of transistors M12 and M13 are the dominant noise sources for the frequency ranging from 550 Hz to 1 MHz.

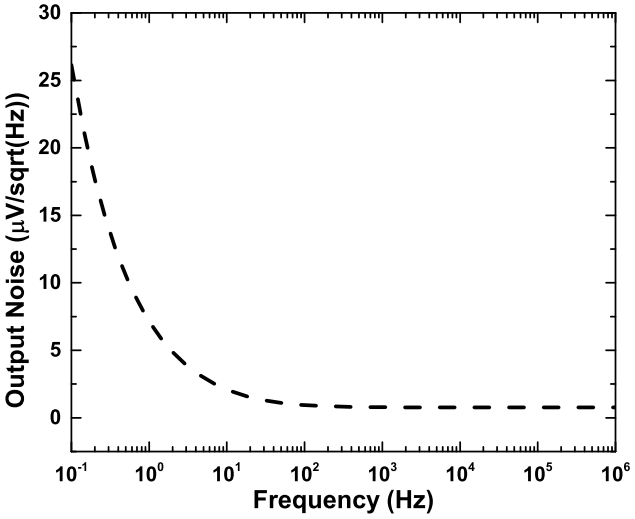

Fig. 15: Output noise spectral density (in µV/$\sqrt{\text{Hz}}$) of proposed LCMVR for frequency ranging from 0.1 Hz to 1 MHz.

The analysis of start-up circuit for setting the stable operating mode of the proposed VRC is performed by transient analysis, applying a pulse input voltage as input supply with a rise time of 1 µs for TT, SS, SF, FS, and FF process corners at room temperature. After around 2 µs, the output reference voltage, V_{REF} is settled as constant and the core reference circuit is said, working in normal mode. Figure 16 shows the transient analysis of proposed LCMVR for different process corners with pulse supply voltage.

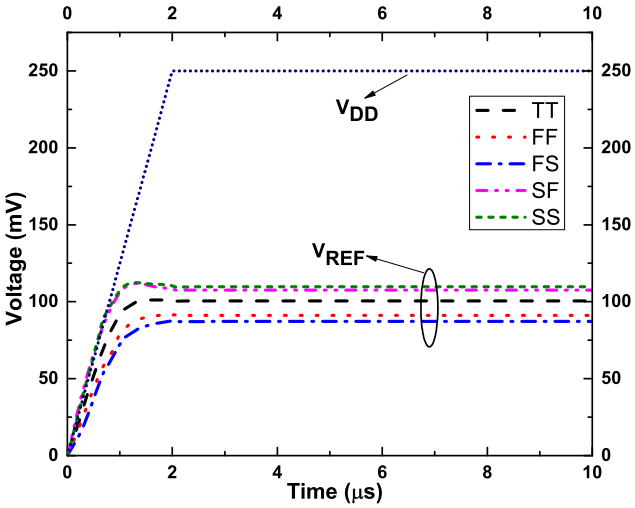

Fig. 16: Transient analysis of proposed LCMVR for different process corners with pulse supply voltage.

Finally, Tab. 2 shows the comparative analysis of proposed LCMVR and VRC of [21] for the same MOS technology environment. From the results shown in Tab. 2, it is concluded that the proposed LCMVR has better performance in terms of PSRR, and LR than work reported in [21].

Tab. 2: Comparative analysis of proposed LCMVR and VRC of [21] for similar technology environment.

Parameters	Proposed	[21]
Technology	90 nm	90 nm
Supply Voltage (V)	0.25–1	0.25–1
V_{REF} (mV)	100.4	41.8
Temperature (°C)	−50–135	−40–100
TC (ppm/°C)	51	127.55
Line Regulation (mV/V)	0.186	6.66
PSRR@100Hz (dB)	−52.5	−32
Output Noise (µV/$\sqrt{\text{Hz}}$)	2.11@10 Hz	1.93@10 Hz

Table 3 sums up the comparative performance of the proposed LCMVR and the recent reported low-power subthreshold VRCs. For a fair comparison with different technology simulations, Figure of Merit (FOM) is defined in [15] as:

$$FOM = \frac{PSRR@100Hz}{TC \times Area \times Supply\ Current}. \qquad (32)$$

It can be observed that the proposed LCMVR needs very low supply voltage compared to all of the reported work. It dissipates very low power than [7], [9], [27], and [28] and has comparable power consumption as

Tab. 3: Comparative performance of the proposed LCMVR circuit with the recent literatures.

Parameters	**Proposed**	**[15]**[a]	**[19]**[a]	**[22]**[a]	**[29]**[a]	**[9]**[b]	**[11]**[b]	**[17]**[b]	**[27]**[b]
Technology	90 nm	180 nm	90 nm	28 nm	180 nm	130 nm	65 nm	180 nm	180 nm
Temperature (°C)	−50–135	−40–120	0–85	−15–80	−20–80	−40–85	−40–125	−40–130	−20–80
Supply Voltage (V)	0.25–1	1.4–2	0.85–1.65	0.85–4.1	0.6	1–3.3	1.08–1.32	0.4	1.35–1.8
V_{REF} (mV)	100.4	650	281	252	441	598	500	212.4	630
TC (ppm/°C)	51	82	125	218.8	25	47	75*	84.5	14.1
PSRR (dB)@100 Hz	−52.5	−70	−48*	−34*	−44	−44	−54	−40	−75.7@dc
LR (mV/V)	0.186	3.33*	0.65*	6.46*	29.5*	1.13*	NA	NA	0.298
Supply Current (µA) @V_{DD}	0.1318 @0.25 V	0.05 @1.4 V*	14.13 @0.85 V*	1.56 @4.1 V*	0.051 @0.6 V	1 @1 V	140 @1.32 V*	0.48 @0.4 V*	0.88 @1.8 V
Die Area (mm^2)	0.000268	0.035	NA	NA	0.00715	0.02	0.04	0.09	0.015
Noise (µV/$\sqrt{Hz}$)	2.11@10 Hz	NA	NA	3.08@10 Hz	NA	NA	1.17@100 Hz	NA	NA
FOM	29143	487	NA	NA	4826	47	0.128	11	406.7

[a] Simulated Values, [b] Measured Values, * Calculated from given data and graph

[25], [26], and [29]. It has high PSRR value among most of the reported literature except [7], [10], [14], and [15] where [10] uses pre-regulator technique and [14] uses an extra capacitor to enhance PSRR. The proposed LCMVR has best line regulation among all reported works. The TC of the proposed LCMVR is comparable to [9] and better than [5], [15], [17], [19], and [22]. It has the smallest active area compared to all the reported work in this paper. Its output noise performance is better than [11], [17], [22], and [30]. Overall this work has comparable TC, power dissipation, high PSRR and best line regulation and FOM to the recent works in the subthreshold VRC designs.

6. Conclusion

A Sub-1V, subthreshold reference is realized in standard 90 nm CMOS technology for low-voltage and low-power applications with the utmost of the transistors working in the subthreshold region. Supply independent current is generated by a looped current mirror, which is allowed to pass through an ALC to generate the voltage reference. The circuit operates with 33 nW power dissipation, 131.8 nA supply current with 0.25 V supply voltage at 27 °C. The obtained reference voltage is 100.4 mV with the line sensitivity of 0.186 mV/V. A temperature coefficient of 51 ppm/°C is achieved at room temperature. The proposed LCMVR exhibits a PSRR of −52.5 dB at 100 Hz. It also has a very small active area of 0.000268 mm^2.

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