A high-efficiency and compact charge pump with charge recycling scheme and finger boost capacitor

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Abstract. A 16-phase 8-branch charge pump with finger boost capacitor is proposed to increase the power efficiency. Compared with the standard capacitor, the finger capacitor can significantly reduce the parasitic capacitance. The proposed four-stage charge pump with finger capacitor can achieve 14.2 V output voltage from a 3 V power supply. The finger capacitor can increase the power efficiency of the charge pump to 60.5% and save chip area as well.

1 Introduction

In the last decade the wearable and portable electronic device market has shown an explosive increase. The electronic device size and the battery autonomy are two important evaluation factors for consumers. In the electronic devices the DC-DC converter is a necessary module to bridge the voltage difference between the battery supply and the requirements of other functional modules. The capacitive DC-DC converter and the inductor-based DC-DC boost converter are two popular topologies to step up the DC voltages. The inductor-based DC-DC converter normally has relatively high efficiency and can supply more power, but it also needs a bulky external inductor which needs more space and is not suitable for the tightly compact devices. In contrast, the capacitive DC-DC converter has the advantage that it can be integrated in monolithic chips and significantly save space. The Dickson charge pump (CP) is an extensively used capacitive converter [1] and a 4-stage Dickson CP is shown in Fig. 1. Compared with the inductor-based converter, a Dickson CP always experiences relatively low efficiency which is attributed to the parasitic capacitance (C_P) of the flying boost capacitor (C). In each clock period, the parasitic capacitance always needs to be charged and discharged, thereby causing power losses, but it doesn't make any useful contribution to the CP operation. As the energy stored in the battery is limited, it is necessary to design a
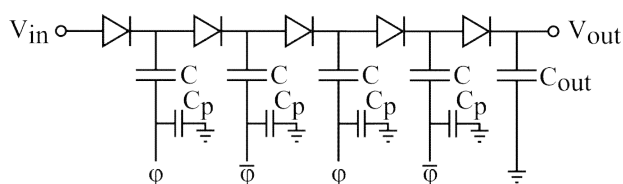
CP with high efficiency and low power consumption in order to extend the electronic device's battery autonomy.

One way to minimize the effect of parasitic capacitance is the charge recycling method. This method can save 50 % of the power consumption attributed to the parasitic capacitance. In our previous work [2], a 16-phase 8-branch CP is introduced which is also based on the charge recycling concept but has an advanced charge recycling strategy. This new CP has 7 intermediate voltage levels during the charge recycling process which can save 87 % of the power consumption related to the parasitic capacitance. Apart from the charge recycling method, another straightforward way to boost the power efficiency is by decreasing the parasitic capacitance of the boost capacitor itself. In this work we use the top metal layers to design several finger structure capacitors. The ratio of parasitic capacitance to the nominal capacitance of finger capacitors with different configurations is investigated and compared with standard capacitors in the CMOS technology library. Finally the finger capacitor is used in the 16-phase 8-branch CP which can significantly increase the power efficiency compared with the CP using the standard capacitors.

2 Circuit Implementation

2.1 16-phase 8-branch CP

Charge recycling is a useful method to improve the power efficiency and it has been demonstrated in several papers [3, 4]. In our previous work the concept of charge recycling was extended and implemented in a 16-phase 8-branch CP, yielding an improved power efficiency as reported in [2]. Fig. 2 (a) shows one stage of the 16-phase 8-branch CP, where the bottom plates of the boost capacitors C_1-C_8 are connected by a transmission gate (TG) matrix (as shown in Fig. 2 (b)) to implement the

Fig. 1 4-stage Dickson charge pump
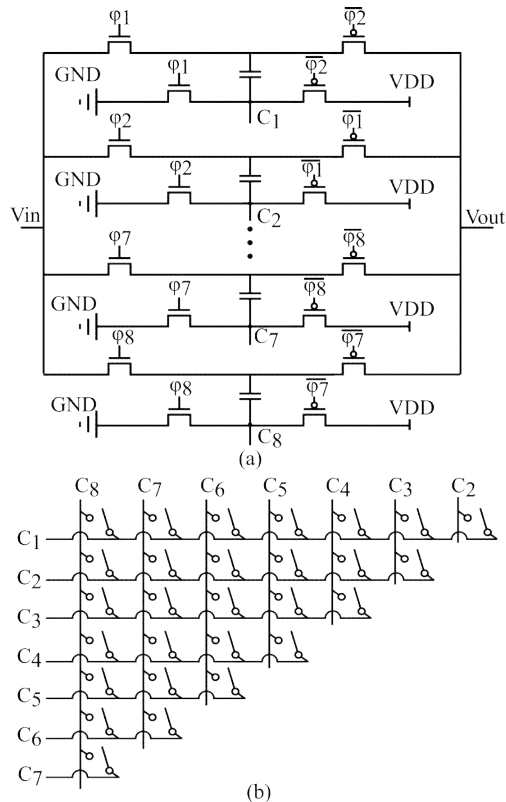
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Fig. 2 (a) One stage of the 16-phase 8-branch CP structure (b) TG matrix

charge recycling strategy. Fig. 3 shows the waveform of the boost capacitor's bottom plate C_1 in one stage and the charge recycling procedure. The principle of charge recycling in this 16-phase 8-branch CP is that instead of charging the bottom plate of boost capacitor C_1 directly from GND to VDD, it will first be properly shorted by the transmission gate matrix to the bottom plate of other boost capacitors, in such a way that a 9-level triangular waveform is obtained. This strategy can significantly decrease the power dissipation due to parasitic capacitance and hence increase the power efficiency, as well as decrease the output voltage ripple.

2.2 The structure of the finger capacitors

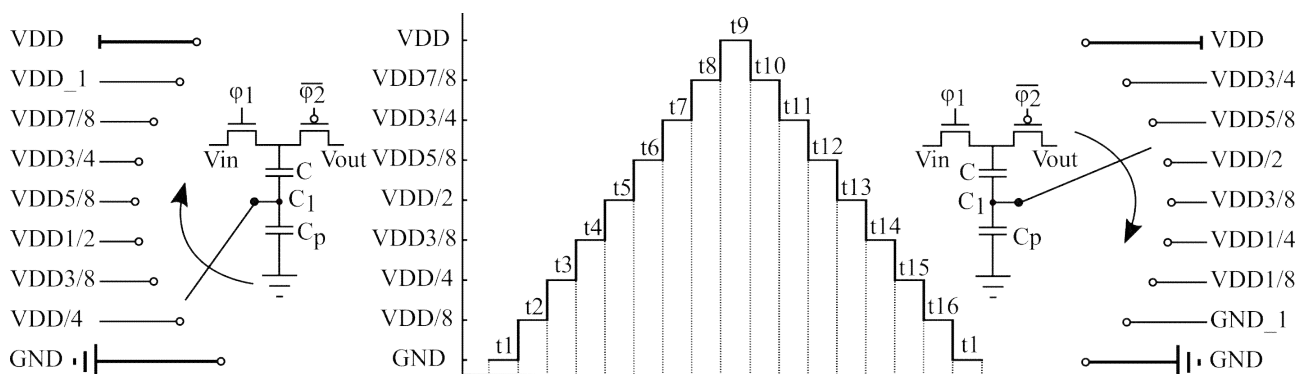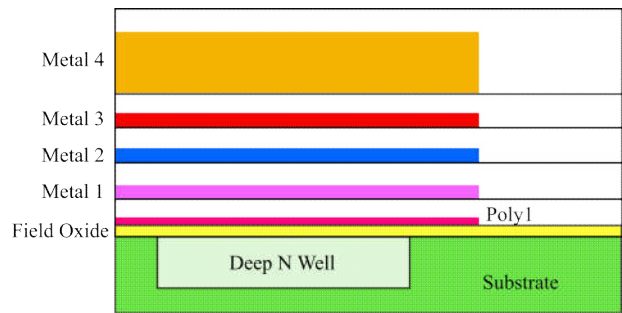In the monolithic CP design, a big challenge is that the

Fig. 4 Cross-sectional view of all the used layers in H35 CMOS technology

expected output voltage of the CP is normally higher than the voltage tolerance of a standard CMOS technology. Therefore a high-voltage (HV) CMOS technology should be used in the CP design. The 0.35 μm H35 CMOS IC technology of Austria MicroSystems (AMS) is a typical high-voltage CMOS technology and the cross-sectional view of the relevant layers in this technology is shown in Fig. 4. There are three standard types of capacitors in this technology and they are the CPOLY (Poly 1 - Poly 2), CPM (Poly 1- Metal 1 - Metal 2 - Metal 3) and CWPM (Deep N Well - Poly 1 - Metal 1 - Metal 2 - Metal 3) capacitors respectively. The CPOLY capacitor has the highest nominal capacitance but its maximum operation voltage is only 5.5 V, which is too low to work as boost capacitor. For the CPM and CWPM capacitors, their maximum operation voltages are 120 V and 70 V respectively, which is high enough for most portable electronic devices. But these two types of capacitors both experience a high ratio of parasitic capacitance to nominal capacitance. For a CPM capacitor with an area of 115 μm * 115 μm for example, the parasitic capacitance and nominal capacitance are 1.597 pF and 1.7 pF respectively, the ratio being as high as 94 %. One way to solve this problem is that we only use the several metal layers on the top side to design the capacitor, so the parasitic capacitance can be significantly reduced. If we use the layers Metal 2 till Metal 4 to design a 115 μm * 115 μm flat metal capacitor (CM), Metal 2 and Metal 4 being

Fig. 3 16-phase 8-branch CP boost capacitor's bottom plate waveform
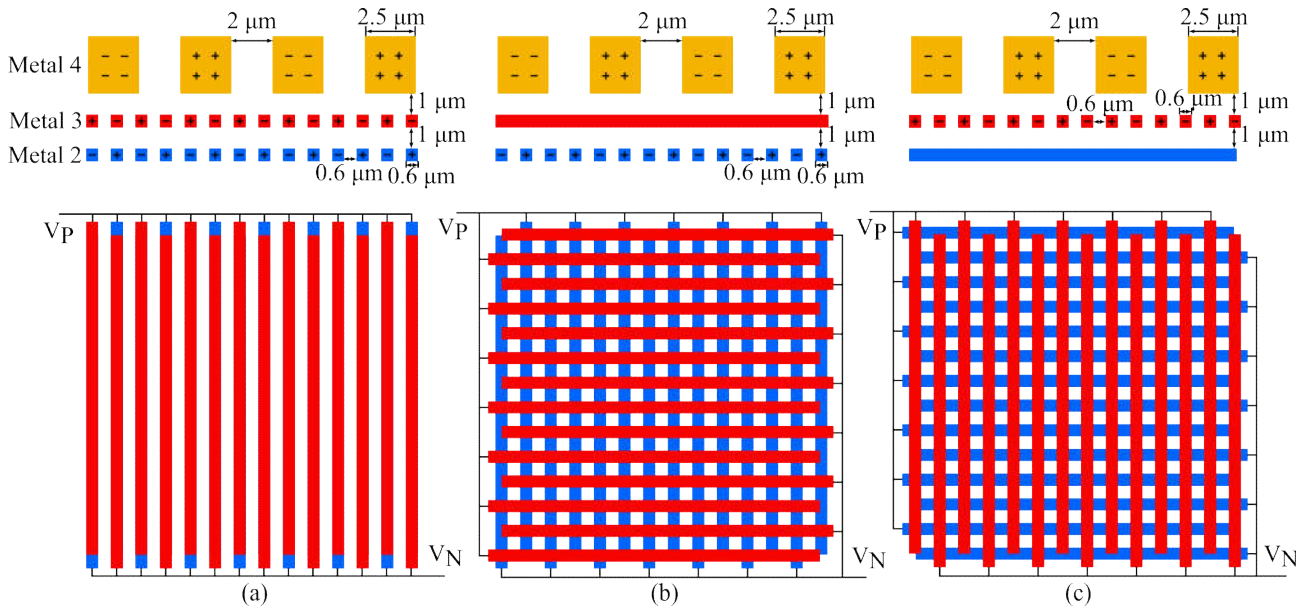
Fig. 5 The finger capacitors with different configurations

Table 1. The capacitance of different capacitor types (115 μm * 115 μm)

Capacitor	Nominal Capacitance [pF]	Parasitic Capacitance [pF]	Ratio of Parasitic to Nominal Capacitance [%]
CPOLY	11.4	1.588	13.9
CPM	1.7	1.597	94.0
CWPM	3.3	N/A	N/A
CM	0.979	0.185	18.9
CFM_a	1.962	0.093	4.74
CFM_b	1.887	0.093	4.93
CFM_c	1.893	0.093	4.91

interconnected as one plate of the capacitor and Metal 3 serving as the other plate, the ratio of parasitic to nominal capacitance is reduced to 18.9 %. However, the nominal capacitance is only 0.979 pF, as shown in Table 1. In order to achieve at the same time the highest possible nominal capacitance, we designed the finger structure capacitors (CFM) by using the Metal 2 to Metal 4 layers with different configurations. The CFM capacitors' structures are shown in Fig. 5 and the corresponding nominal and parasitic capacitance values are shown in Table 1. The CFM capacitors have a reasonable nominal capacitance and very little parasitic capacitance, with the CFM_a capacitor having the lowest ratio of parasitic to nominal capacitance of only 4.74 % between one plate and the substrate.

2.3 Control circuit

Fig. 6 shows the on-chip control circuit of this 16-phase 8-branch CP. The frequency of this control circuit is determined by the voltage V_C which is connected to the gate of p-type MOSFET P_1. V_C controls the drain current of P_1, which drives the unity-gain current mirror $N_1 + N_2$, resulting in a ring oscillator bias current equal to the current through P_1. The ring oscillator is comprised of 17
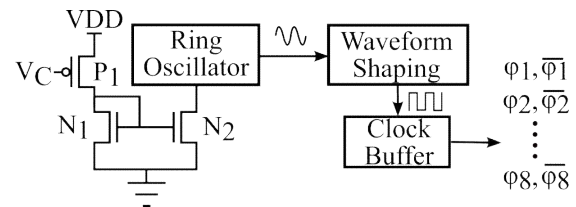

Fig. 6 The schematic of the control circuit

inverters and the frequency can sweep from 0 to 9.32 MHz by varying the control voltage V_C. The signal from the oscillator then passes through the waveform shaping and clock buffer circuits to become the expected clock signals φ_1, $\overline{\varphi_1}$, φ_2, $\overline{\varphi_2}$ .... φ_8, $\overline{\varphi_8}$ to control the 16-phase 8-branch CP.

3 Simulation Results

The performance of a 16-phase 8-branch CP with CFM_a, CM or CPM boost capacitors is simulated by using a 0.35 μm CMOS technology. These three types of capacitors exhibit a ratio of parasitic to nominal capacitance of 4.74 %, 18.9 % and 94 % respectively, as already stated in Table 1. The layout of these three capacitors is shown in Fig. 7. They are all square and their side lengths are 116 μm, 165 μm and 125 μm respectively in order to obtain the same nominal capacitance of 2 pF for all boost capacitor types, which is essential to allow a fair comparison of the CP performance. The supply voltage VDD is 3 V and the clock frequency is set to 4 MHz. All the CPs have four stages which are connected in series. The first stage's node Vin is connected to VDD and a 20 pF load capacitor is attached to the output node of the fourth stage.
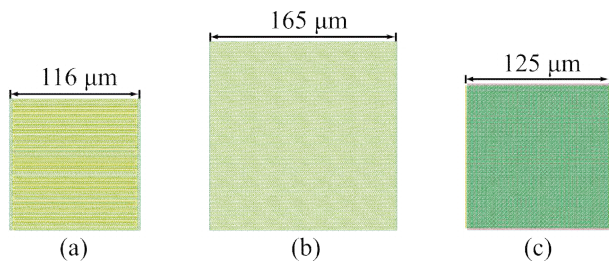
Fig. 7 The layout of (a) CFM_a, (b) CM and (c) CPM capacitors

The output voltage of the three CP circuits with different boost capacitors at different output currents is plotted in Fig. 8. For all these three CPs, the output voltage decreases equally fast when the output current increases. At zero-load condition, the CPs with CM and CFM_a capacitors have a similar output voltage of 14.2 V, while the output voltage for the CP with CPM capacitor is a little lower, about 13.8 V.

Fig. 9 shows the power efficiency of the three CP circuits with different boost capacitors at different output current. In the efficiency calculation, the power dissipation in the control circuit and all CP transistors is taken into account. The maximum efficiency of the CP with CPM boost capacitor is only 36.2 % at 70 µA current load. In contrast, at the same current load the power efficiency of the CP with CFM_a and CM capacitors is 57.2 % and 55.4 % respectively. The maximum efficiency of the CP with CFM_a and CM
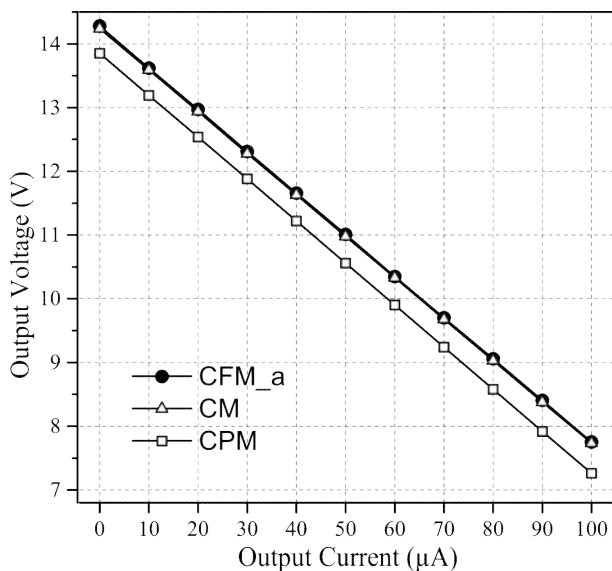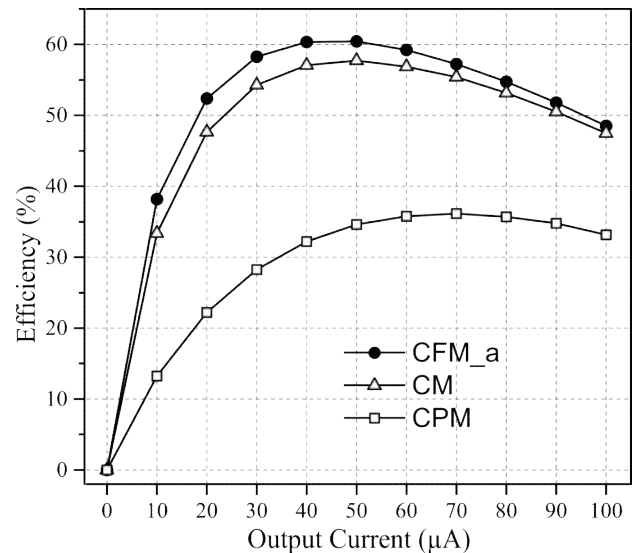

Fig. 9 Efficiency at different current load

capacitors is 60.5 % and 57.8 % respectively. It is worth mentioning that the CP with CFM_a boost capacitor not only has the maximum efficiency but also has the minimum chip area because for the same nominal capacitance of 2 pF the CFM_a capacitor has the minimum size of 116 µm * 116 µm.

4 Conclusion

In this work a 16-phase 8-branch CP with finger boost capacitor is proposed. By using the finger capacitor, the ratio of parasitic capacitance to nominal capacitance of the boost capacitor can be significantly reduced to only 4.74 %, compared to 94 % for a standard poly-metal sandwich capacitor. By combining the charge recycling method and the finger capacitor, the output voltage of the proposed four-stage CP can reach 14.2 V from a 3 V power supply and the maximum efficiency is 60.5 %.

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Fig. 8 Output voltage at different current load