

Trends in R&D in TSV Technology for 3D LSI Packaging

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1 Introduction

Small, high-speed, and multi-functional computers and other electronic devices have been enabled by high integration technologies that have come to reality by the miniaturization through the LSI process scaling which uses a very fine pattern. However, an upper limit in the progress of such miniaturization has come into sight. The miniaturization will be technologically limited due to the increase of leak current which generates heat in transistors, and signal delay time caused by wiring. 3D packaging technology is one of the technologies that are expected to make a breakthrough such miniaturization on a 2D surface, which will enable high density integration that does not depend on miniaturization on 2D surfaces. By stacking LSI chips, which would conventionally be set out on a plane, it will be possible to produce LSI components, with the same functionality as that of the components produced by conventional methods, and with a smaller footprint.

The 3D packaging key technologies are electrical packaging technology, which means that it is vital to connect the stacked chips electrically. Conventional

3D packaging technology uses wire bonding with fine metal lead wires. Recently, novel technologies have been developed to replace wire bonding. For example, wireless connection for data communication, which will reduce the space needed for wiring, has been proposed.^[1-4] Another example is through-silicon via packaging technology^[5-7] (hereinafter, referred to as TSV technology), which uses through-holes in silicon substrate for electrical connection. By using TSVs, it is possible to save the space that would be necessary for bonding wires and to make wiring lengths shorter. TSV technology is moving further ahead of other novel 3D packaging technologies mentioned above towards the production of commercially viable LSI components.^[8,9]

In this article, TSV technology is introduced as one of the 3D packaging technologies. At the same time, as well as discussing the features of TSV technology, the technological challenges for attaining commercial viability are introduced. Finally, the R&D organizations or the consortiums both in Japan and in other countries, which have been working to tackle these challenges, will be introduced.

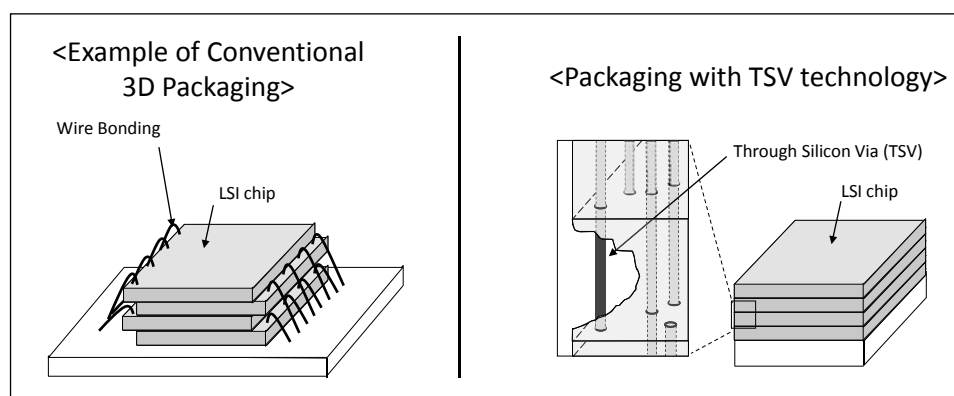


Figure 1 : Comparison of Conventional 3D Packaging and Packaging with TSV technology

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2 | What is Through Silicon Via (TSV) Technology?

2-1 TSV technology for 3D LSI Packaging

3D LSI Packaging, which is expected to improve packaging density, has conventionally been accomplished by connecting chips electrically with wire bonding. TSV technology, one of the advanced 3D packaging technologies, is expected to improve packaging density compared with that using wire bonding.(Figure 2)

By using TSV technology, circuits in the stacked LSI chips are interconnected (Figure 1) by electrical connection through vias (TSVs) so that those chips can be integrated into an LSI component. TSV technology has attracted attention as alternative advanced technologies to replace the conventional process scaling of LSI. Furthermore, TSV technology is expected to be technologies to enable multi-functional LSIs, because of their capability to integrate heterogeneous LSI chips and/or MEMS in a single package.

Japan has led the world in the research and development in TSV technology for 3D high-density packaging since the Association of Super-Advanced Electronics Technologies (ASET) started the packaging technology research projects supported by MITI (now METI) in 1998 and kicked off its activities

as the R&D center of TSV technology for high density packaging.^[10] In the industrial sector, in 2007, Toshiba Corp. succeeded in reducing the volume of a mobile phone camera module by 64% by applying a TSV technology (Toshiba called it TCV, Through Silicon Chip, at that time) for the first time in the world,^[8] and attracted attention from all over the world. Elpida Memory, Inc. announced that it had developed a DRAM of eight stacked LSI chips that had an eight times larger memory capacity than conventional ones.^[9]

Although a lot of commercially available products using TSV technology have been announced, they were all merely examples of limited applications of the technology, where only miniaturization and high-density integration, from among various advantages of TSV technology, were achieved. On the contrary, current R&D activities worldwide are focused on the more advanced and more sophisticated applications of TSV technology which use the full range of the advantages of TSV technology, and an innovation in chip design methods also becomes a research target.

2-2 Two directions of TSV technology

The miniaturization and high-density integration methods of LSI are generally classified into two categories. The method in the first category is an implementation method called SiP (System in package) and the method in the second category is one of the LSI design methodologies called SoC (System

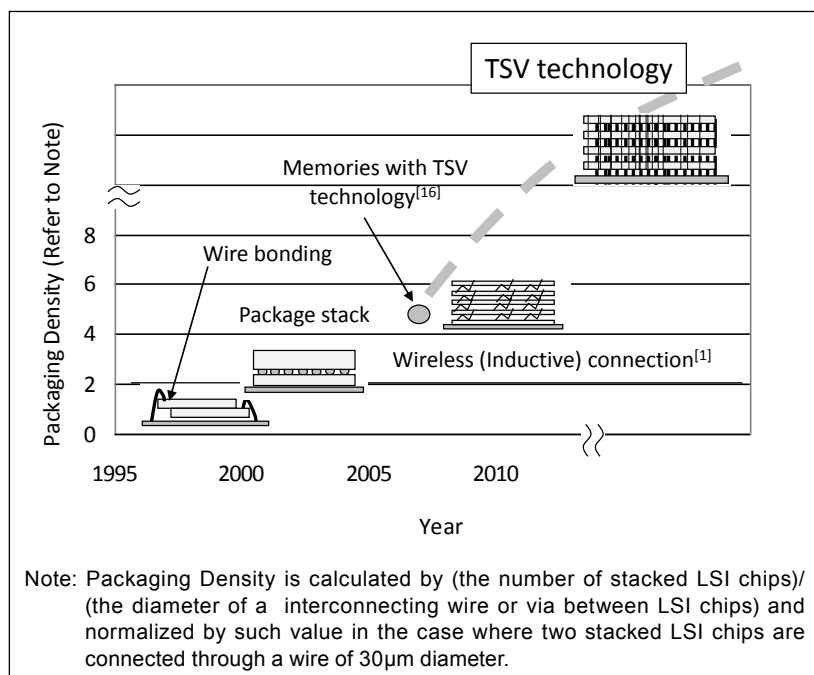


Figure 2 : Transition of 3D packaging

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on a chip). In SiP, individually manufactured LSI chips are integrated and combined into a package with ports for outer connections to form a single device. In SoC, a chip is designed in such a way that logic circuits which contain functional circuit blocks are realized in an single LSI chip. TSV technology has been developed to be applied in both categories that are said as both directions. Below, TSV technology is introduced in detail along the lines of the two directions referred to above, namely SiP and SoC:

(1) TSV technology as an extension of SiP

Basically, in SiP, LSI chips are interconnected electrically by metal wires. SiP technologies have been frequently applied to 3D packaging for digital cameras and mobile phones in order to miniaturize them by integrating chips with high-density. Fig 3 illustrates TSV technology as a next technology of SiP. As illustrated, heterogeneous LSI chips, adjacently placed or stacked, are interconnected electrically through an interposer (an interconnecting substrate for connecting between LSI chips) by wire bonding to be completed as an LSI component (upper-left of Fig 3). By contrast, in TSV technology, heterogeneous LSI chips are stacked and electrically interconnected through vias, not through wire bonding. The camera modules and the stacked memories referred to in 2.1 are examples of the expansion of SiP. Such extended methods of SiP are expected to be applied to the integration of various types of LSI chips on a chip (heterogeneous LSI) or to the packaging of LSI chips and/or MEMS together in a single package.

(2) TSV technology as a conceptual leap from SoC

Figure 4 illustrates how the SoC method originally used for a 2D design changes into for a 3D design method and how it can be applied to 3D packaging. It is a kind of conceptual leap. The conceptual leap occurs as follows: first, dividing a logic circuit composed on a 2D surface into multiple sub logic circuit chips; second, laying them out on multiple chips (silicon substrate); and finally, stacking the chips perpendicularly. TSV technology enables implementation of the same functionality on a smaller footprint. Therefore, as in the case of miniaturization or high-density integration, TSV technology is similarly effective in the scaling of LSI. Although commercially viable examples are not yet to be seen, high-density integrated logic LSIs will be considered

to be one of the embodiments thereof.

2-3 Advantages of TSV

The advantages of applying TSV technology in comparison with conventional methods are as follows:

(1) Small size and high density

As illustrated in Figure 3 and Figure 4, TSV technology enables the miniaturizing of LSI components. Although SiP has been used for stacking, SiP requires excessive spaces outside the LSIs for wire bonding. In contrast, TSV is more effective for miniaturization because TSV requires no such spaces. As for a “conceptual leap from SoC,” TSV technology can be used for the perpendicular construction of LSIs in a 3D space, not on a 2D surface, and require a footprint at a fraction of that of a conventional LSI. On the other hand, as for high density integration, it has been reported that TSV technology can potentially be used effectively for stacking processor cores in a CPU composed of multi cores to realize a highly parallel processor LSI.

(2) High speed signal propagation and processing

As illustrated in Figure 3 and Figure 4, TSV technology can reduce the total wiring length, compared with 2D implementation. Shorter wiring lengths will lead to higher speeds in signal propagation and a reduction of mutual coupling which causes signal delays, and will finally result in high-speed data transmission. In addition, by using TSV technology, it is possible to increase the design flexibility, to reduce the wiring length and, finally, to increase the processing speed, by stacking and interconnecting LSI chips which transmit and receive data frequently. It has been reported that numerical simulations showed an increase of processing speeds up by 44% in comparison with the case of conventional LSI, by applying ideas such as those referred to above to increase the transmission speed between the processor and the memory in a supercomputer LSI.^[11]

(3) Low power consumption

Electrical resistance causes heating. Further, since parasitic capacitance increases due to the length and the number of wires, charge/discharge current increases, then increasing current also causes heating. TSV technology, which can reduce the wiring length, enables the elimination of such heating and, as a

result, reduces power consumption by cutting out power losses due to wiring resistance or parasitic capacitance. Furthermore, the shorter circuit length results in reducing the number of repeaters (signal reshaping components) while at the same time reducing the power required by such repeaters needed for compensating the decay and delay of signals. A simulation on the supercomputer LSI referred to in (2), showed that a power saving of up to 14% can be estimated.^[11]

(4) Many input-output terminals

TSV technology also provides many input-output

terminals. In a conventional SiP implementation, wire bondings are located at the edges of an LSI chip. Therefore, the input-output terminals have to be placed along the edges of an LSI chip. In contrast, in implementations using TSV technology, there is no such limitation on the placement of input-output terminals in an LSI. This capability of being able to place input-output terminals in arbitrary positions in an LSI chip without limitation leads to an increase in the number of interconnections (Figure 1), and also to an increase in the flexibility of circuit layout. Moreover, it is possible to explosively increase the number of parallel data transmission lines between

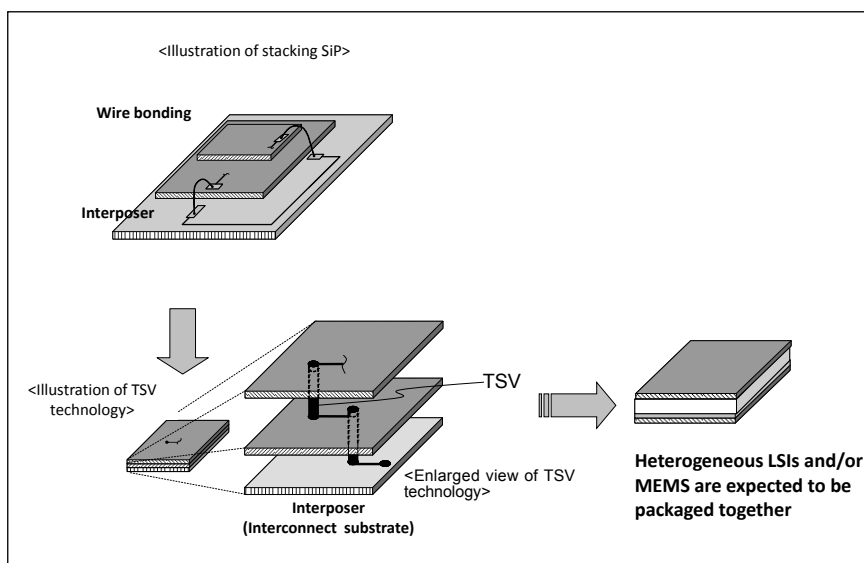


Figure 3 : TSV technology as an extension of SiP

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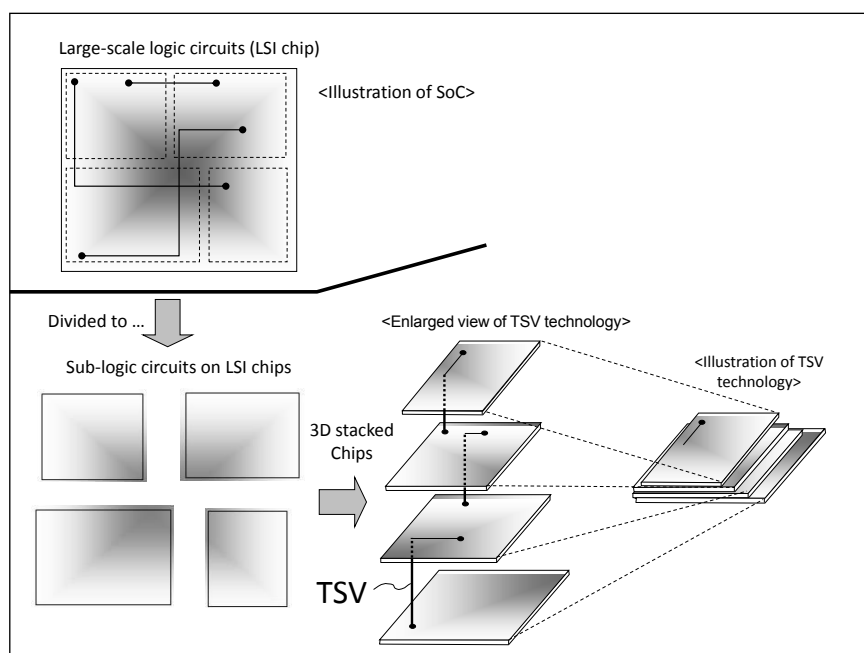


Figure 4 : TSV technology as a conceptual leap from SoC

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LSI chips and, as a result, to increase the data transmission speed, because of a number of input-output terminals.

(5) Multi-functionality and high performance

SiP technologies have been used to implement multi-functionality, and can enhance much more by using TSV technology enable to provide a number of input-output terminals. Then, more LSI chips can be implemented in a single package. For example, a high-resolution and high-speed image processor with the processing power of 10,000 frames per second can be constructed in a single package by integrating a large number of memory chips, a large number of high-speed processors and a large number of image sensors, working in parallel through a large number of input-output terminals produced by TSV technology.^[12] This is an example of utilizing the advantages of integration and the high-speed capability of TSV technology. In such a way, TSV technology is expected to contribute to obtaining high-performance that would be difficult using conventional technologies.

2-4 TSV Application Targets

The requirements for TSVs differ from LSI to LSI, for instance, miniaturized LSIs require small-diameter TSVs and LSIs with large-scale circuits require a large number of TSVs.

Figure 5 shows various groups of LSIs, categorized by type or usage, in relation to the required TSV diameter and the required number of TSVs, where the

horizontal axis represents the required diameter and the vertical axis represents the number.

As showed in Figure 5, the CMOS camera module, which has already been marketed, uses a small number of TSVs with a large diameter. The stacked-die memory, which has been announced, compared with the CMOS camera module referred to above, uses a larger number of TSVs with a smaller diameter. However the number of TSVs is still only around several thousands. Compared with those two earlier examples, Logic LSI components, expected to be developed in future, will require several tens of thousands of TSVs with a much smaller diameter. If the TSV's diameter is 1µm, up-to one million TSVs can be formed into a 1mm square. However, LSI components may use a variety of TSVs with different diameters on a single chip. For example, Logic LSIs will use small-diameter TSVs for signal transmission and, at the same time, for power supply, they will require large-diameter TSVs due to a large current capacity. Moreover, heterogeneous LSIs which contain different types of LSI chips integrated into one component, and MEMS consolidated LSI components will require a larger variety of TSVs with different diameters.

Therefore, the technical difficulty of forming TSVs differs largely from application to application, and thus it is not easy to discuss TSV technology in a uniform way.

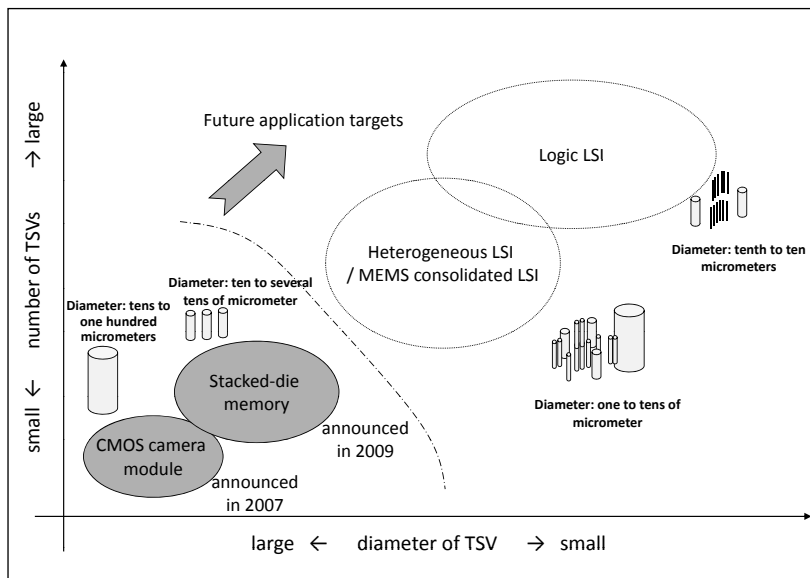


Figure 5 : Map of TSV applied components in relation with TSV diameter and number

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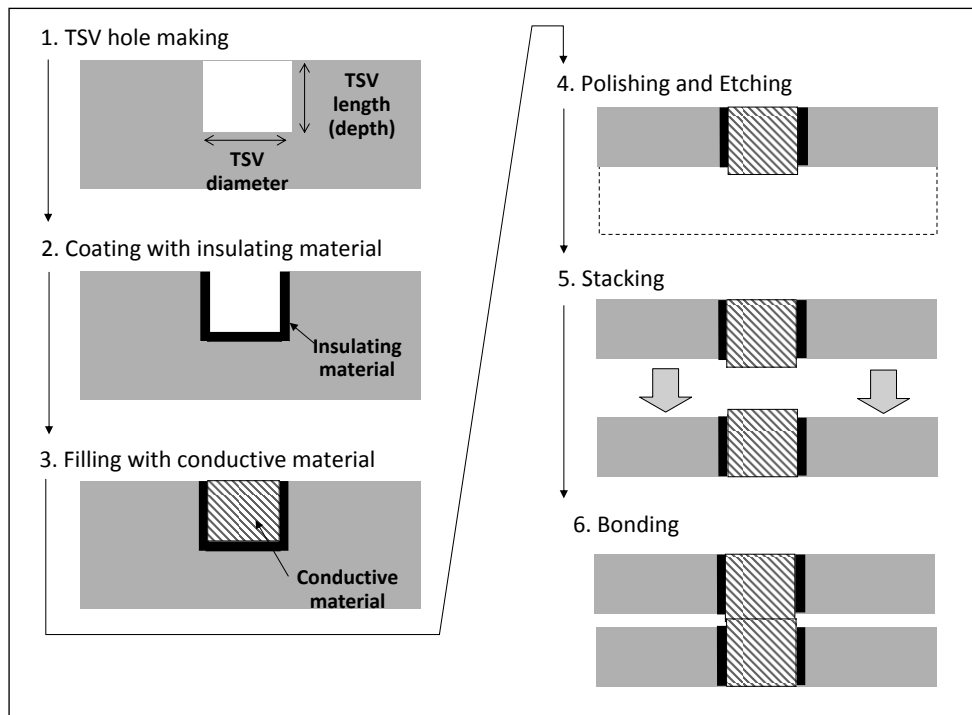


Figure 6 : TSV fabrication Process, illustrated in cross-section

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2-5 Fabrication Process of TSV

The TSV fabrication process consists of TSV forming process, chip stacking process and TSV bonding process.

First, a hole is made on a silicon substrate (Figure 6, 1). Then, the inside of the hole is coated with insulating material for preventing electrical conduction between the TSV and the substrate (Figure 6, 2). Next, the hole is filled with conductive material (Figure 6, 3) to become a via. Then, for the interconnection of TSVs, the bottom of the substrate, which is on the opposite side of the hole, is polished and etched to make it thinner in order to expose the TSV (Figure 6, 4). Finally, two LSI chips are stacked (Figure 6, 5) in such a way that the TSVs are bonded with each other, and a circuit connection through TSVs is established (Figure 6, 6).

3 Challenges in R&D in TSV

3-1 Primary Challenges in Fabrication

(1) TSV hole Forming

The first challenge in the fabrication process is to create a TSV hole on a silicon chip. TSVs require deep holes with a small diameter.

The aspect ratio of a TSV (TSV length / TSV diameter) reaches to several times to several ten times

in the ratio. Making such a high aspect ratio hole is a significant technical challenge. Furthermore, as the aspect ratio rises, the difficulty in fabrication increases and the time taken for fabrication grows longer. How to choose the fabrication process, how to apply the process, and how to determine the diameter and length of the TSV are researched through experiment or trial and error.

As for “making holes,” two processes are well known; the first is called the “Bosch Process,”^[13] which is a “deep-etching process,” originally developed for MEMS fabrication; and the other is called the “non-Bosch Process,” which simply means that “it is not included in the category of the Bosch Process.” The Bosch process, developed by Robert Bosch GmbH in Germany, begins with digging a shallow hole by Reactive Ion Etching (RIE). The hole is then coated with insulating material, and dug again. By repeating the process described above, a deep perpendicular hole is formed. RIE is a digging process where a specimen to be etched is placed in a chamber filled with reactive gas (etching gas), given electric potential, and exposed with ions or radicals to be hollowed.^[14] On the other hand, in the non-Bosch process, a deep hole is formed by a sophisticatedly controlled anisotropic etching process and does not require the in-process insulation material coating which is required in the Bosch process.

The holes formed by the processes mentioned above are then coated with insulation material and filled with conductive material. The selection of the conductive material depends on the TSV forming process. How to choose the conductive material is left to section (4). The next section (2) will illustrate the polishing and etching processes.

(2) Polishing and etching

A silicon substrate is polished thinly to a thickness of several tens to several hundreds of micrometers in order to shorten the time required for TSV forming by shortening the length of TSV holes. This is done because TSV forming processes are very time consuming. Next, the substrate is etched thinly to expose a TSV. Also, the substrate polishing is an effective way to obtain a higher packaging density in a stacking direction and to produce thin LSI components. During polishing processes, silicon substrates suffer from mechanical stresses, therefore it is necessary to protect the substrate by supporting it with, for example, a glass carrier. Of course, the supporting glass carrier must be removed after completion of the polishing. A lot of effort has gone into research on how to choose the adhesive for bonding the glass carrier and how to remove it after polishing, as well as into other problems such as how to determine the process sequence or how to remove the dust brought about by polishing.

(3) Connecting

As for connecting TSVs, there are three methods called “Wafer to Wafer,” “Die to Wafer” and “Die to Die.” In “Wafer to Wafer,” silicon wafers are bonded to each other before LSI chip dicing, in “Die to Wafer,” chips diced-out of wafers are bonded to wafers, and in “Die to Die,” diced-out chips are bonded to each other. The process technologies for all three methods, which have both drawbacks and advantages as regards difficulties or costs, are targets for research. For example, in Wafer-to-Wafer, 300 mm wafer discs are bonded to each other in such a way that each of several thousands to several tens of thousands of TSVs with a 1 μ m diameter on a wafer disc is precisely interconnected to each TSV on the other wafer chip. It is easy to understand that a very high precision alignment is required. There are two methods for stacking TSVs: the “Face to Face” method and “Face to Back.” In “Face to Face,” circuits formed

on an LSI are stacked face-to-face to the circuits on the other LSI. In “Face to Back,” LSIs are stacked in such a way that the faces are in the same direction. Different technologies are required for each method with different directions of stacking, and so, different aspects of research and development are necessary.

(4) TSV formation timing

TSV forming methods are categorized into three groups according to when in the process the TSVs are formed. These three methods are described in detail along with the generalized manufacturing process of LSI^[15] illustrated in Figure 7. The first is called “vias first,” where TSVs are formed on a silicon substrate before circuits are built. The second is “vias middle” where TSVs are formed after circuit building and before wiring among circuits. In some cases vias middle is categorized as vias first. The final one is “vias last” where TSVs are formed after wiring. In some cases, TSVs are formed after stacking LSI chips. Such a case, although also called vias last, is positioned on the Assembly and Testing process in Figure 7.

These three processes, which have different timings for each TSV formation, require different TSV-filling conductive materials. In vias first or vias middle, polysilicon is used, because, in those processes, heat-resistance or process-compatibility is required. In vias last, requirements for materials are not so severe, and Cu (copper), W (tungsten), or Al (aluminum) is used.^[16] The material for the filler needs to have high electrical conductivity, however polysilicon has high electrical resistance. On the other hand Cu or Al has low resistance. In addition, Ni (nickel) has been tried as a replacement for polysilicon which has not been used favorably.

As for the TSV formation, the best process timing has not yet been found and still is a research target.

3-2 Challenges in Significant Related Technologies with growing Difficulties

For applying TSV technology successfully, more complicated and sophisticated technologies are necessary than are required in conventional LSI manufacturing. Such technical challenges in the significant related technologies are described below:

(1) Testing

As for an LSI component composed by using TSV technology with several stacked LSI chips and/or

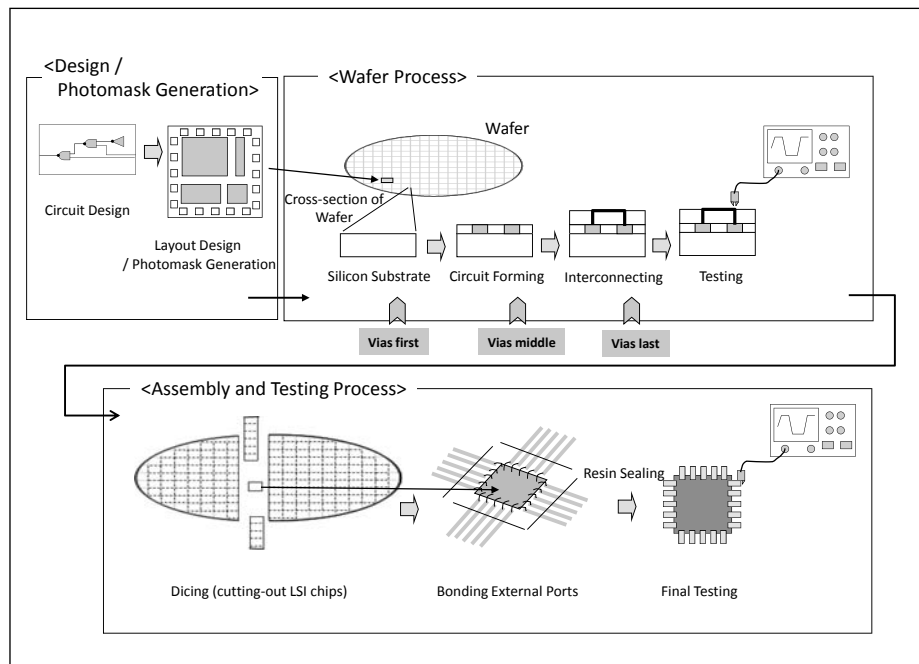


Figure 7 : Timing of TSV formation in the generalized manufacturing process of LSI

Prepared by the STFC based on Reference^[15]

several stacked MEMSs, some test ports that would be necessary for the diagnostic test of LSI chips and MEMSs placed on inner layers may be hidden inside the component and not accessible from the outside. Such LSIs or MEMSs can be tested only through ports exposed outside the component. Therefore, more complicated test items and longer testing times are required because access from the outside is limited. To remove such inexpediencies, much more effort will have to be put into researching, for example, effective test programs with fewer test items and high-speed data gathering capabilities, or into analysis methods. If an LSI component fails a test, it means that a large number of LSI chips and MEMS are discarded, resulting in a great loss. Therefore, the verification tests of an LSI component become much more critical than for conventional LSIs.

(2) Heat design and heat dissipation

Generally, when LSIs are in operation they generate heat, and the generated heat raises the operating ambient temperature. When operated at a high temperature, LSIs lose their reliability. Therefore, heat design and heat dissipation are critical for ensuring reliability. For stacked chips, the heat design for chips on the inner layers is more difficult. In addition, when non-uniform heat is generated by an LSI chip, it causes mechanical stresses due to differences in heat expansion, leads to excessive force in TSV connection, and finally results in reliability degradation. To solve

heat problems, ideas have been proposed such as forming dummy TSVs, with a view to making positive use of their heat conductivity for heat dispersion and heat dissipation.^[17]

A more sophisticated heat design will be required for multiple stacking LSIs which generate much more heat. ASET, the research consortium referred to earlier, has reported experiments^[5] where cooling water runs along the surface of LSI chips, as one of the water-cooling trials for high-end LSI components. IBM Corp. has reportedly started a research project for novel, their original, cooling technologies using a liquid coolant.

To solve heat problems, in addition to heat simulations in layout design or structural analysis which take care of mechanical distortions by heat, research and development efforts will have to be put into the codesign method which consolidates electrical design, heat design and structural design.^[12]

(3) Analysis of Signal and Power Integrity

LSI components integrated by using TSV technology contain electrodes for perpendicular interconnections, which conventional LSIs do not have. The physical characteristics of various materials related to the interconnection electrodes, such as conductive material in TSVs, insulator material surrounding TSV and silicon substrate through which TSVs are made, have to be taken into consideration when electrical and electromagnetic characteristics are

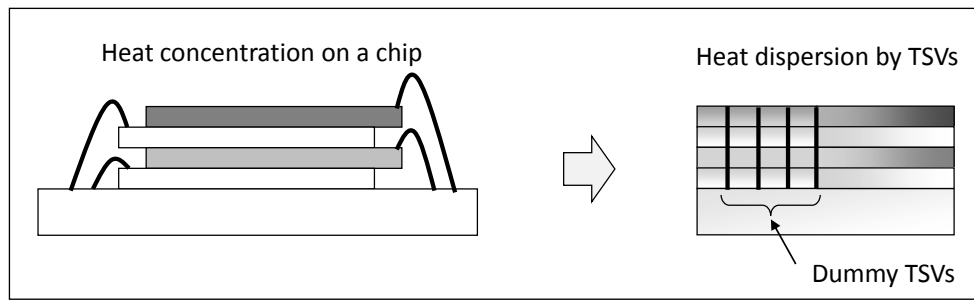


Figure 8 : Heat dispersion through TSVs

Prepared by the STFC

determined, because they are the critical factors that determine signal transmission quality. At the same time, research and development efforts are required on simulation models or model of computation of TSVs for analyzing SI (Signal Integrity). In order to build such simulation models, the ability to link circuit simulators with electromagnetic field simulators will be indispensable.

At the same time, it is important to make effective use of the know-how stored in conventional LSI design. For such practical use of conventional know-how, it will be necessary to apply the design methodology of a “what-if analysis,” where the design process proceeds through a “parameter-change analysis” based on hypothesis and assumption. High-speed simulators will be indispensable for such what-if analysis.

On the other hand, high PI (Power Integrity) is necessary for the stable operation of LSIs. High PI means that a circuit has a low voltage drop in a DC component and also has a low voltage fluctuation in an AC component.

Voltage drop in a DC component is basically determined by the diameter of TSV and DC resistance to conductive material that fills the TSV. It means that the diameter and the DC resistance are the critical factors. Similarly, capacitance and inductance are the critical factors of AC fluctuation. Capacitors can be effectively used for suppressing high-frequency voltage fluctuation. To use capacitors effectively, it is necessary to place them as close to the LSI chip as possible. Even embedding capacitors in the chip or in the interposer may be necessary in some cases. Therefore, capacitor embedding technology may be required.

(4) EMC: Electromagnetic Compatibility

In some cases, electromagnetic interference affecting the stable LSI operation may occur due

to electromagnetic coupling between unconnected circuits. In TSV applied LSIs, electromagnetic interference between circuits is not negligible because circuits are placed closely within a short distance of tens of micro meters to circuits on other LSI chips, or TSVs are placed close to each other by several micro meters, and at the same time electric signals of various voltages and frequencies congest on an LSI chip as a result of packaging multiple LSI chips and/or MEMS. Generally, it is effective, in order to suppress electromagnetic interference, to place the reference potential (ground) of a large area close to the circuits and to give it a stable potential. However, in a TSV applied LSI, it is difficult to place the common ground of all the circuits because the circuits are multiple stacked.

In addition, research and development for electromagnetic noise emission control is also important. In some cases, such electromagnetic interference may adversely affect the operation of other outside instruments and devices. Therefore, the upper-limit of an allowable emission of electromagnetic noise from electronic devices has been determined by international standards, and additionally in Japan such emissions are restricted.^[18] Countermeasures for electromagnetic noise emission will be more complicated for LSI components of a larger scale and with more functions as a result of the adoption of TSV technology.

So, such simulation technologies as used for SI or PI design will be critical.

3-3 Challenges in TSV design

The LSI manufacturing process is roughly divided into three processes; design process, wafer process and assembly and testing process (Figure 7). The design process, or the first process, is also divided into system design, logic design, layout design and test design. In recent years, an option of the

manufacturing process has also been regarded as a part of design process, because design and manufacturing are closely inter-related. The design technology is a technology to design marketable products with optimizing all the manufacturing processes under electrical or mechanical constraints or conditions. The design technology will be realized by using design support software tools such as EDA (Electronic Design Automation) tools based on design concept (architecture). Two essential points in the design process when TSV technology is applied are as follows;

(1) TSV specific Design Challenges

As referred to in 2-3, 3D packaging using TSV technology could expand design flexibility to a large extent. That is the performance of LSI components may, possibly, depend largely on the performance of the design. For example, the layout design of LSI chips or LSI components will be changed drastically by the adoption of TSV technology. Generally, in layout design, circuit components are placed and routed between them, and, as a result of the design, photomask data to be used in the LSI chip manufacturing process are generated. In the case of LSI components with large-scale circuits, TSV locations have to be determined in such a way that the total circuit length is minimized. To accomplish such layout design, a new design methodology and also a new EDA tool supporting the design process will have to be developed.

In addition, TSV technology enables direct circuit interconnections between LSI chips, and eliminates I/O interface circuit connection on a pad which is indispensable for implementation by SiP technologies to accomplish the connection. However, those interface circuits have the role of waveform shaping. So, in TSV design, there is a requirement for such waveform shaping to be taken into consideration. Furthermore, new dedicated design tools may be required to design efficiency for a better design.

(2) TSV Design Technologies for Competitiveness

Generally speaking, the core technologies of TSV technology are based on mastery of the manufacturing equipment for TSV formation. However, the best combination of those core technologies has yet to be found. So, in production of the LSI with TSV technology, each semiconductor maker chooses

the appropriate technologies from among the core technologies and combines them to obtain the advantage by using own methods in order to maintain its competitive edge by utilizing its know-how on parameter setting and so on. For the development of the LSI with TSV technology, each semiconductor maker determines the overall component-design by taking into consideration all constraints such as manufacturability, market adoptability, product reliability and cost. Among the critical technical factors listed in the previous section, the most critical factor is “cost.” Miniaturizing, high density integration and multi-functionality have already been achieved in SiP by using wire bonding. So, in LSI components designed by TSV technology, the most critical factor compared with that of SiP is cost. Device engineers estimate that the allowable rise in cost caused by the adoption of TSV technology will be about 200 US dollars per one 300 mm wafer. However, future target has been set at 50 US dollars in one view,^[19] and a Japanese venture company has announced a key technology that is expected to attain that target.^[20] To keep on absorbing such new technologies and customizing them to create their own products will lead to better strategies for maintaining competitiveness.

4 | Worldwide Research Organization on TSV technology

Research and development is being undertaken all over the world to solve the challenges referred to in chapter 3. Table 1 lists major public research organizations worldwide which are working on research and development in TSV technology, such as semiconductor design and processes or nano-scale fabrication. In this chapter, research and development projects aiming at the production of market adoptable products are introduced, focusing on their distinctiveness or originality.

4-1 SEMATECH (Semiconductor Manufacturing Technology Institute), US

SEMATECH in the US launched the TSV development program “3D Interconnect” in March 2007. Since then, they have been inviting participants to cooperate in the program. They say that the cooperation will be fostered in the “area of basic, precompetitive R&D.” This means that

Table 1 : Major Public Research Organizations worldwide

Organization	Location
SEMATECH (Semiconductor Manufacturing Technology Institute)	US
Georgia Institute of Technology	US
Massachusetts Institute of Technology	US
Rensselaer Polytechnic Institute	US
RTI International	Offices around the world (established in US)
University of Arkansas	US
MIT Lincoln Laboratory	US
IMEC (Interuniversity Microelectronics Center)	Belgium
CEA-Leti (Electronics and Information Technology Laboratory of the French Atomic Energy Commission)	France
Fraunhofer Institute for Reliability and Microintegration	Germany
IME (Institute of Microelectronics)	Singapore
ITRI (Industrial Technology Research Institute)	Taiwan
ASET (Association of Super-Advanced Electronics Technology)	Japan
Tohoku University	Japan

Prepared by the STFC based on the Reference^[5]

participants will cooperate in an area where they are not competing with the others. The distinctive points regarding SEMATECH are described below:^[21,22]

(1) Variety of Participants

Various companies from all over the world are participating, including semiconductor dealers, chip makers, materials suppliers, assembling and packaging companies, design laboratories, test laboratories and test equipment makers, from every sector of the semiconductor industry.

(2) Practical Approach

They are addressing the challenges in TSV technology development in a practical way such as:

- {1} Building a consensus in the semiconductor industry on 3D packaging methods, manufacturing processes, supportive tools and so on,
- {2} Accumulating practical knowledge, such as the cost of each manufacturing process or other product specific information,
- {3} Developing a practical and applicable manufacturing method,
- {4} Building a roadmap and making efforts toward standardization.

(3) Other Features

SEMATECH allows the participants to use its new manufacturing technologies. It works on incentives to invite participants. In addition to this program,

SEMATECH has a close relationship with Tokyo Electron Ltd.,^[23,24] which is an LSI manufacturing equipment maker, and they have worked together in the development of the etching equipment for TSV forming. Such close relationships and strong alliances with semiconductor manufacturing equipment makers have enhanced SEMATECH's technological development capability in the semiconductor manufacturing process, especially in as regards the "wafer process" in Figure 7. Furthermore, in the wafer process area, SEMATECH has been undertaking collaborative research with universities such as CNSE (College of Nanoscale Science and Engineering).

4-2 IMEC (Interuniversity Microelectronic Center), Belgium

In 2004, Belgium-based IMEC started research and development in basic TSV technology, and has boosted its activities since it launched a specific project for 3D packaging by using a cooperation scheme called IIAP (IMEC Industrial Affiliation Program) in 2006. This project aims to develop 3D packaging technologies, and also undertakes penetrating research into design problems. The characteristics of the project are as follows:^[25,26]

(1) Variety of Participants

The project has alliance partners from all over the world, including IDMs (integrated device manufacturers: semiconductor maker which design, manufacture and sell, semiconductor products),

packaging companies, fabless/fab-lite semiconductor makers, EDA tool providers, manufacturing equipment makers and materials suppliers.

(2) Innovative Approach

The project focuses on 3D interconnections of circuits between different layers, and covers almost all levels of interconnection, ranging from a LSI package to an LSI chip. At the same time, it seeks industry-relevant, cost-effective and innovative solutions. It currently aims at determining the application areas for critical design problems where system level 3D interconnections are applicable, and also proposing the design methodologies for such interconnections. It has shown a roadmap of TSV technology, on which they have announced, as one of their goals, LSI circuit interconnections using TSVs with a precision of 0.1µm diameter. This project’s activities in this area can be said to be an example of the “conceptual leap from SoC” referred to in 2-2.

(3) Other Features

IMEC has accepted EDA tool providers as cooperation partners. IMEC’s approach differs from that of SEMATECH on that point. On the other hand, IMEC has been undertaking original and advanced research in addition to the project, and, as well as SEMATECH, has an accumulation of excellent world-class knowledge. Furthermore, IMEC has allowed its members to use the world-class advanced manufacturing equipment installed in IMEC, and it has been attracting participants.

4-3 EMC-3D (Semiconductor 3D Equipment and Materials Consortium), EU, US and Korea

EMC-3D, a cross-border project between the EU, US and Korea, was started in 2007 when CEA-Leti, France, announced its participation in the project. EMC-3D aims to undertake TSV technology development for 3D chip stacking and MEMS consolidation. The distinctive points of the project are described below.^[27]

(1) Worldwide participants

EMC-3D is an international consortium of which members are materials suppliers and manufacturing equipment manufacturers from the EU, US and Korea. In addition, universities and R&D divisions of major semiconductor makers have participated as partners.

(2) Sharing R&D Approach

The members have their own R&D themes in their fields of expertise, and have R&D responsibilities on sub-divided themes in TSV technology such as TSV forming, wafer polishing, and LSI chip stacking and packaging. Their common shared objective is to develop practical and low-cost TSV technology to gain market adoption and to make trial production frequently.

(3) Other features

It is noteworthy that, as for semiconductor makers, it is the R&D divisions of such organizations that have participated in the work not their manufacturing division. Furthermore, government research organizations dedicated to basic research, such as the Fraunhofer Institute, Germany, and CEA-Leti, France, are also involved. Therefore, EMC-3D seems to have targeted the area of basic and precompetitive R&D, as well as SEMATECH. Reportedly, EMC-3D was established to compete with ASET, Japan. So, EMC-3D is a consortium in which major private corporations and organizations worldwide, except for Japan, have participated.

4-4 Association of Super-Advanced Electronics Technology, Japan

For the first time anywhere in the world, the ASET started R&D activities of TSV technology in 1999 as a consortium project. Now, another project is working on practical and market adoptive R&D projects. Those projects are managed under the unified theme of “3D-Integration Technology (Dream Chip Project).”

(1) Participants pursuing Practical Technologies

Electronic equipment makers, semiconductor makers, materials suppliers, manufacturing equipment makers and a packaging company from across the entire industry which is seeking practical technologies are participating. In addition, universities and the National Institute of Advanced Industrial Science and Technology^[12] (AIST) have participated.

(2) Approach for Practical Application Oriented Research

Activities have been carried out as contract research of the New Energy and Industrial Technology Development Organization (NEDO) on themes relating to the industrial application of TSV

technology, such as circuit simulation, electromagnetic simulation, SI and PI using interposers, testing, heat design, polishing and trial production of LSI components using TSV technology.^[12,28]

(3) Other features

As for semiconductor manufacturing equipment makers, the companies that have expertise in testing are also participants in addition to the TSV forming equipment makers. This is one of the unique features of the ASET. The development of almost all the essential technologies in the TSV fabrication processes have been completed, and the major current research targets are concentrating on the significant related technologies referred to in 3-2.

5 Conclusions

TSV technology has attracted attention as high-density integration technologies replacing miniaturization through the LSI process scaling. At the same time, TSV technology is expected to be applied in the production of multi-functional LSIs through their capabilities in integrating multiple heterogeneous LSI chips and/or MEMSs.

R&D efforts in US are concentrated on essential technologies and the application of TSV technology; in EU, in addition to the essential technologies, new EDA tools are under development and the practical application of TSV technology is being pursued along the long-range landscape of technology application; EU, US and Korea associated research consortium,

while continuing R&D in essential technologies, is focusing on trial production using TSV technology; and in Japan, under the ASET consortium, R&D efforts are being put into practical applications including significant related technologies. Each of these international research projects has its own concepts and is unique, and it seems that Japan is working most closely to the “production.”

Although the application of TSV technology brings a lot of advantages such as high-speeds, low power consumption, multi-functionality or high performance in addition to miniaturizing and high density integration, there are still a lot of technical challenges to be tackled. A variety of technical challenges ranging from design and TSV forming to significant related technologies will need to be tackled. To overcome such challenges, much research is being carried out all over the world and across borders. The majority of this research is generally based on “global alliances”, which should attract attention as a keyword in the development of cutting-edge LSI technology.

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