

科学技術・学術政策研究所
講演録—297

SEMATECH における研究とイノベーション戦略

米 SEMATECH 副所長

Raj Jammy

2013 年 12 月

文部科学省 科学技術・学術政策研究所

科学技術動向研究センター

本講演録は、2013年3月15日に文部科学省科学技術政策研究所で行われた、SEMATECH 副所長 Raj Jammy 氏の講演会の内容を、講演者の了承のもとに当研究所においてとりまとめたものである。また、本講演録の内容は、講演の記録として講演者の見解を掲載しており、当研究所の公式の見解を示すものではないことに留意されたい。

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本講演録の引用を行う際には、出典を明記願います。

科学技術政策研究所講演会

- 演題：** 「SEMATECH における研究とイノベーション戦略」
講師： Raj Jammy (SEMATECH 副所長)
コメント： 鳥海 明 (東京大学教授)
日時： 2013年3月15日(金) 15時00分～17時00分
場所： 新霞が関ビル LB階 201D号室 科学技術政策研究所会議室
言語： 英語 (質疑応答は日本語でも可能)

講演趣旨：

1987年に米国で発足した官民共同による半導体製造技術組合 SEMATECH (SEmiconductor MAanufacturing TECHnology)は、米国の半導体産業の競争力回復に成功を収めた。その後は、米国以外の半導体会社も加わり、国際的な半導体研究の拠点になっている。現在も、紫外線露光による微細化プロセスや3次元配線などの先端的な研究で、世界の半導体研究をリードし続けている。そして米国におけるナノテクノロジー産学官連携拠点である Albany Nano Tech Complex においても中核機関としての地位を確立しており、コンソーシアムマネジメントの観点からも重要な存在となっている。

このような官民共同のコンソーシアムを大きな成功に導く秘訣は何か、そしてそのマネジメントや組織はどうあるべきかを、マネージャーの立場からお話を伺う。

講師経歴：

SEMATECH の材料および技術融合担当副所長。特に、革新的スケールで技術を融合する研究の責任者を務める。過去4年間、フロントエンド・プロセッサ部の部長を務めた。

IBM 社の半導体研究開発センター (East Fishkill, NY) で、デープトレンチ DRAM のフロントエンド技術の開発に従事した後、DRAM 開発組織の熱プロセスと表面処理グループの責任者となる。2002年に、ワトソン研究センター (Yorktown Heights, NY) に転勤、high-k 誘電材料ゲートの開発責任者となる。

米国ノースウェスタン大学で博士号を取得し、50件以上の特許の取得と150件以上の論文発表および講演の実績を持つ。

(本講演後、4月より Intermolecular Inc. 半導体グループ担当副社長)

講演内容

SEMATECH における研究とイノベーション戦略

Raj Jammy (SEMATECH 副所長)

【司会者】 それでは、定刻になりましたので、科学技術政策研究所所内講演会を開催させていただきますと思います。本日は、お忙しい中をお集まりいただき、ありがとうございます。司会進行をさせていただきます市口と申します。お手元に資料が3枚ありますが、もし足りない方がおられましたらご挙手をお願いします。

本日は、世界的な半導体研究の拠点であります SEMATECH の Jammy 副所長をお招きして、ご講演をして頂くことになっています。本来なら、この講演会の講演趣旨と講師の方のご経歴をご紹介しますが、お手元にお配りしております案内状に記載しておりますので、詳細はそちらを読んでいただくことにして、説明は省略させていただきます。

時間配分は、Jammy 先生のご講演が約 60 分、それに続いて東京大学の鳥海先生のコメントを約 10 分間いただくことになっております。その後 30 分ほど質疑応答、あと残り 20 分ほどを名刺交換のために時間を残しておきたいと思っています。

それでは、早速、講演をお願いいたします。


【Jammy】 Thank you very much, Ichiguchi-san. Good afternoon, everybody. Thank you for joining me here today. It is my pleasure to be here at your office, NISTEP. I also want to thank Ichiguchi-san and Kamiyama-san and Chuma-sensei for the invitation to come to Japan and to present some of our works, how we collaborate at SEMATECH and why collaboration is critical in our opinion. And to me the discussion that we have today is more around how future of research and development must be done and how it is necessary to be done, as we go into many complex situations in the coming years. This is probably example of semiconductor technology, but the same example can be applied in many other fields.

To take this discussion off, I would like to go through semiconductor industry, how the industry has grown and what scaling is all about, and I also talk a little bit about



Fig. 1

the industry's current trends and some gaps between the R&D costs and revenue in the semiconductor industry. That may give you an idea of why a collaborative organization like SEMATECH makes sense, how SEMATECH was established and what is the impact of that. What are the major transitions that are taking place in the industry?



Contents 目次

- Growth of semiconductor industry and scaling
半導体産業と微細化の成長率
- Technology and industry trends – and gaps
テクノロジーと産業動向、そのギャップ
- Rising cost of R&D and SEMATECH context
増加し続けるR&D費用とSEMATECHの背景
- History of SEMATECH, collaboration model and impact
SEMATECHの歩み：協業モデルと影響力
- Major technology transitions in semiconductor industry
半導体産業における主要なテクノロジーの推移
- Consortia success factors and Summary
コンソーシアムの成功の要因とまとめ

13 March 2013

Fig. 2

The semiconductor industry

is continuously going through changes and transitions. It is important to look at that change and transition today. And of course, Toriumi-sensei is a big part of some of these changes in the industry; some of his research directly impacts many of the things that I'm going to talk about today.

At the end of this presentation, I would like to highlight some of the discussion topics that we go through as a summary point. What I would like to do is to talk about what makes a consortium successful, why a consortium can be successful and what is necessary for that.

Now, through all this presentation, please stop me if I am speaking too fast. I speak very fast, so please stop me and tell me to slow down.



Contents 目次

- Growth of semiconductor industry and scaling
半導体産業と微細化の成長率

13 March 2013

Fig. 3

So, let's start with the first topic: semiconductor industry growth (Fig. 3). In the semiconductor industry, we have what is called a virtuous cycle (Fig. 4). We call it virtuous because we innovate, and that innovation leads to new technology, and that new technology obviously is giving us lower cost and more functionality. Once we have a virtuous cycle, we have more applications, business increases, and then obviously revenue is going up. So once there is more revenue, again we invest it back in R&D, and more ideas, more innovation, and we continue. This is how we have been doing for a

long time. Although this is called a virtuous cycle, this may be a dangerous cycle in one way. The danger comes because the need for R&D and the cost of R&D are continuously increasing. Unless the application space is expanding faster, you would not gain an advantage from the virtuous cycle. You will see that during the presentation.

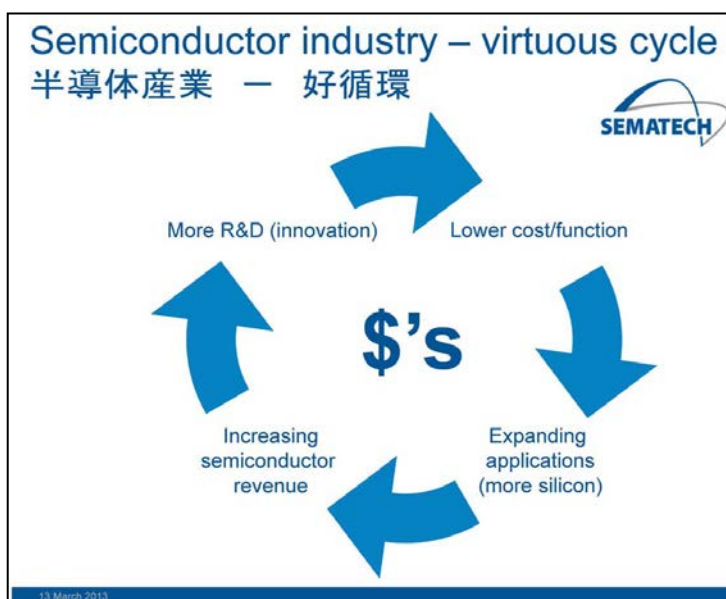


Fig. 4

No person in the semiconductor industry can do a presentation without talking about Gordon Moore. I am from the semiconductor industry, so I have to tell you about Moore's Law (Fig. 5). I am sure that many of you are familiar with Moore's Law, so I do not have to spend too much time here. Just I want to make one very important point: Moore's Law is neither a technology law nor a scientific law. It is purely economics. When

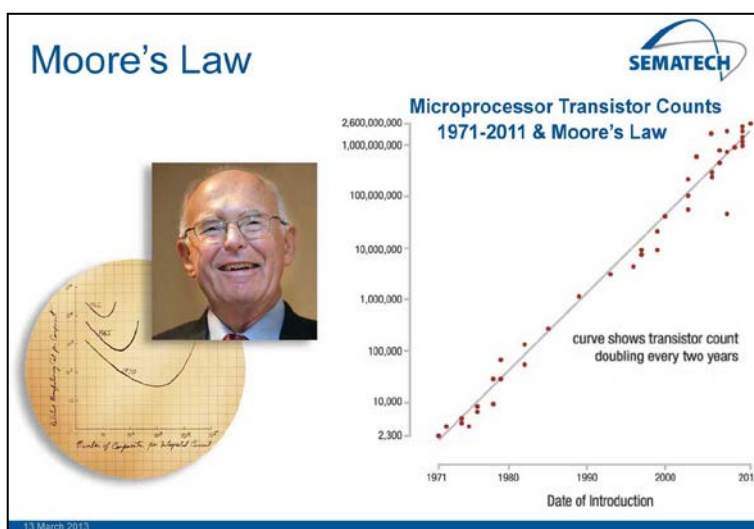


Fig. 5

the number of transistors is doubled, the designers can put more circuits on the same chip. More circuits mean more functionality. Therefore, the customers and consumers are happy that the next-generation cell-phone can do more work and the next-generation laptop can be faster. At the end, that is literally what has been happening.

Right here, I want to say "If we can get this kind of functional improvement by other methods, it is also good." I think the industry is going in that direction. I was talking to Kamiyama-san a little before, and both of us believe that conventional scaling

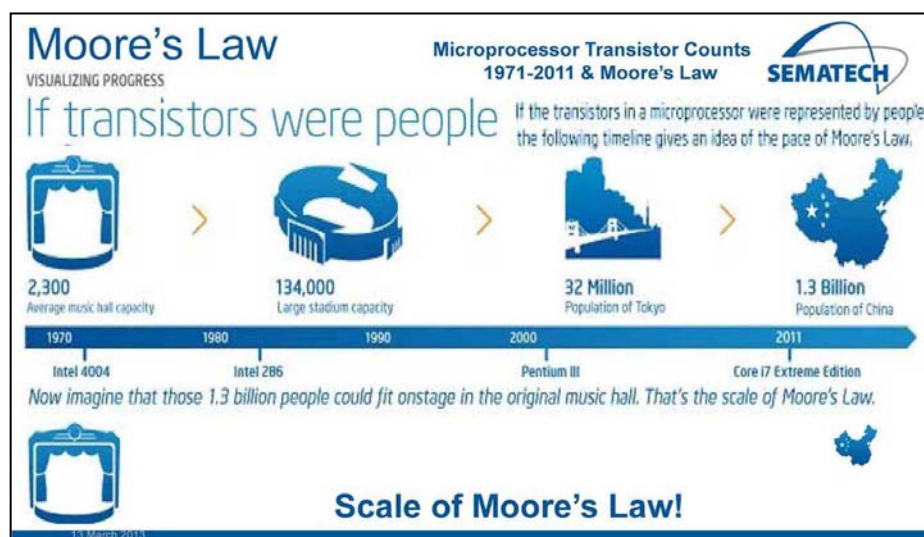


Fig. 6

approaches may not be necessary. Some of the ideas that are being looked at today might be more appropriate for future generations. If we select materials that are pioneered by various groups, a lot of non-lithography techniques might be the direction that we should look into. We will come back and talk about that subsequently.

For those of us in the room here who might want to get an idea of what kind of semiconductor technologies and how the scaling happened, Fig. 6 might be of an interesting chart. In 1970s, when the Intel's first chip 4004 was introduced, the number of transistors was about 2,300. That means it is like an auditorium or a hall. In mid-1980s, when Intel 286 was introduced, the capacity in terms of transistors was about 134,000 just like a stadium. By the time when Pentium III was introduced, the number of transistors went up to 32 million, which is like the population of Tokyo. Now, we have 1.3 billion transistors, and some of the chips that are being made today are close to 2 billion transistors. The number of 1.3 billion is equaling to the population of China. If transistors were people, this is how you would see them. You can imagine the size of these data.

What is interesting is that actual chip size has not changed. I think this is probably the most important thing in the industry. The chip size has to remain the same as back in 1970s. In reality, what we have is the population of China on a chip. That is really the scaling power that we are all working on today.

Now, another very important factor within the Moore's Law is that we are getting lower and lower cost. Figure 7 shows the cost per transistor and per frequency. The frequency is a typical measure for performance improvement, in general. So far, that is how the industry has been looking at it. From that perspective, there is a significant reduction in terms of cost as being scaled. You have not only been able to put more

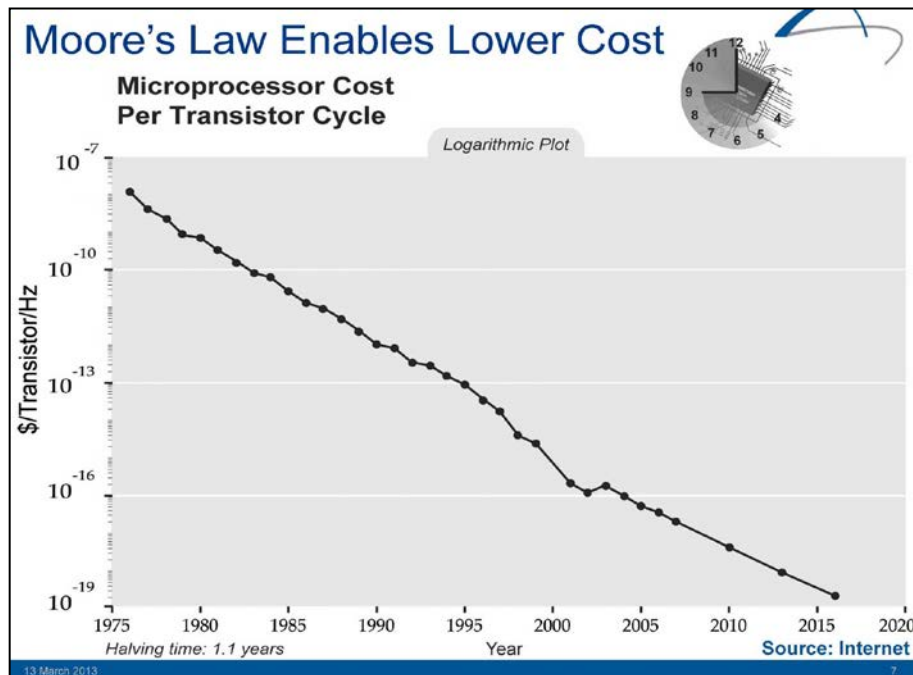


Fig. 7

transistors in a chip by making them smaller, but also you have been able to reduce the cost per transistor as well at the same time.

Contents 目次
 SEMATECH
 • Technology and industry trends – and gaps
 テクノロジーと産業動向、そのギャップ
 13 March 2013

Fig. 8

Now, let's start looking at technology trends and industry trends and where are the gaps (Fig. 8). The big driver was a personal computer in 1990s, and PC was a big thing (Fig. 9). Everything was made for PC and everything was geared around PC. In 2000s, it was on Internet. The computer was important, but how fast the computer was able to get the Internet information was more important than the computer itself. Today, it is more about smart technologies. By smart, it is not just a technology being smart; it is more about how the technology interacts with us. It

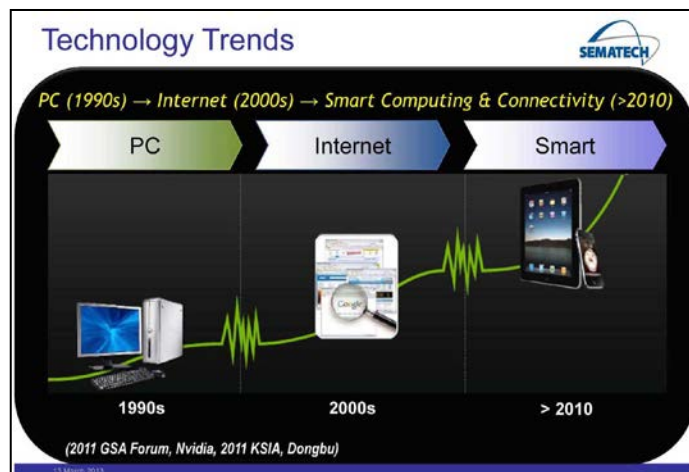


Fig. 9

may be more about people than about the technology itself. What is required to be smart is very important.

In the past, we had display technology, computing technology, communication, storage, sensing, and all separate technologies. Today, it is not the case; they are all integrated. We have functional integration in



Fig. 10

these technologies. If we look into how this is doing, we are putting all these technologies together so that we have a higher level of functional integration, and we can access information wherever we want, whenever we want, and whatever information we want. We may access the entire collection from Library of Congress or the entire scientific database may be available in our pockets. That is the direction we are headed. This is an important change we are seeing right now.

This trend is also related to some other changes that are coming in mobile computing platforms and mobile communicating platforms (Fig. 11). Mobile communications and mobile computing are coming together. At the same time, the growth rate for mobile communication platform is very fast (see Fig. 11). In fact, the demand is so much higher for communication chip that the supply cannot match. It is expected to be the same way for the next few years. It is also important that these computing platforms always have a communication part attached to them. That is why these two are coming together. Similarly, behind

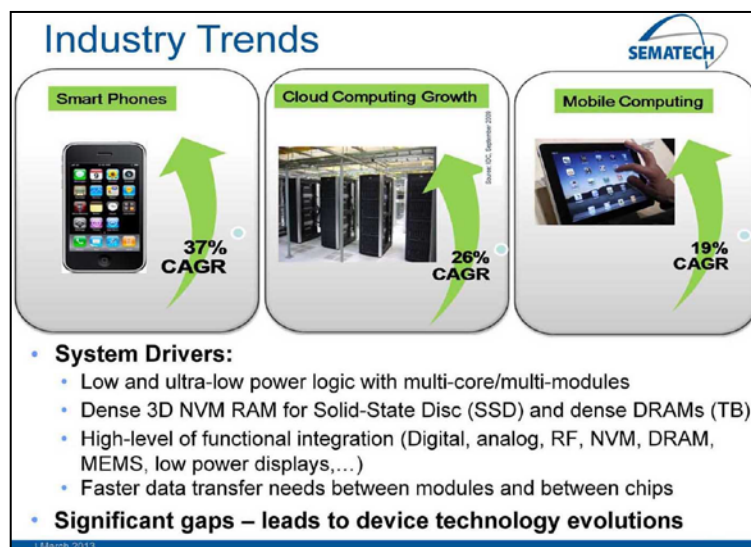


Fig. 11

every cell-phone, there are cellular technologies. This means that cellular technology is also growing very rapidly.

Now, the new technologies' needs are very different. In case of communication technologies, main important thing is low and ultra-low power technologies. You need ultra-low power devices and cell-phones. Even cloud computers also need low power technology because the number or the size they have to deal with is so huge that they need a power plant right by the side of a server station. It will be expensive. In fact, Google started their server station by Columbia River in Oregon State only because there was a power plant right next to it. They need that much of energy just to run a server station today. Therefore, the low power is very important.

Second important thing is memory technology. Dense memory is another absolute need. We all create a lot of information on a daily basis. All the information is not just created, but it is also stored. In some cases, the information may be multiplied many times and saved. For example, university degrees, health records, benefits, and financial reports are kept in different locations multiple times. If we are going to store such information for the entire lifetime or if people create one's own information, we have to think about how to save it. How much memory each person would have on the planet? We have 7 billion people today, and from today standard, each person may consume 10 terabytes of information through the entire life. Information of seven billion times 10 terabytes are a huge load of memory.

We talked about function integration in the previous part (see Fig. 10), and it means more companies are coming together. There is a large problem when we use the fast logic and high-density memory: How fast do we send information from the logic to memory? And how fast do we take it from memory storage and send it to the logic when we need it? The communication channel becomes a very important piece. Namely, the fast data transfer between the modules or between the chips is a very important thing.

All these things have significant gaps. This is what the industry wants, but I do not think that it is possible today. We need some new revolutionary changes in the device technology. I will come back to that later, but I want you to hold that in your mind.

Now, I would like to show you how ITRS, the International Technology Roadmap for Semiconductors, is treating the same thing (see Fig. 12). One direction is, of course, the Moore's Law direction, and the other one is functional diversification of more than Moore's Law or beyond Moore-based technologies.

Now, in this situation of course, one can continue to scale; that is one possibility. But, there is another possibility where you can continue to add more functional components on the same chip. This is called “system on a chip” or “system in a package.” I will talk about that piece. Adding different components on

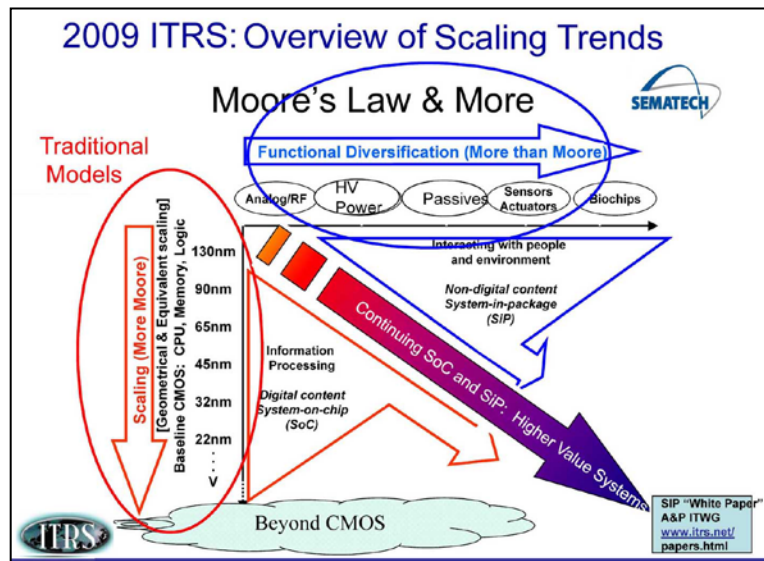


Fig. 12

one chip has a big advantage because it means that we get more scaling indirectly. It is equivalent to the ordinal scaling that was done with dimension shrinking. Thus, higher value systems using “system on a chip” or using “system in a package” is a new direction the entire industry is going.

I talked about gaps and about changes, and those changes are here (Fig. 13). The device evolutions or technology evolutions are listed up in Fig. 13. There are very important things in three categories. The first category is that most devices are going

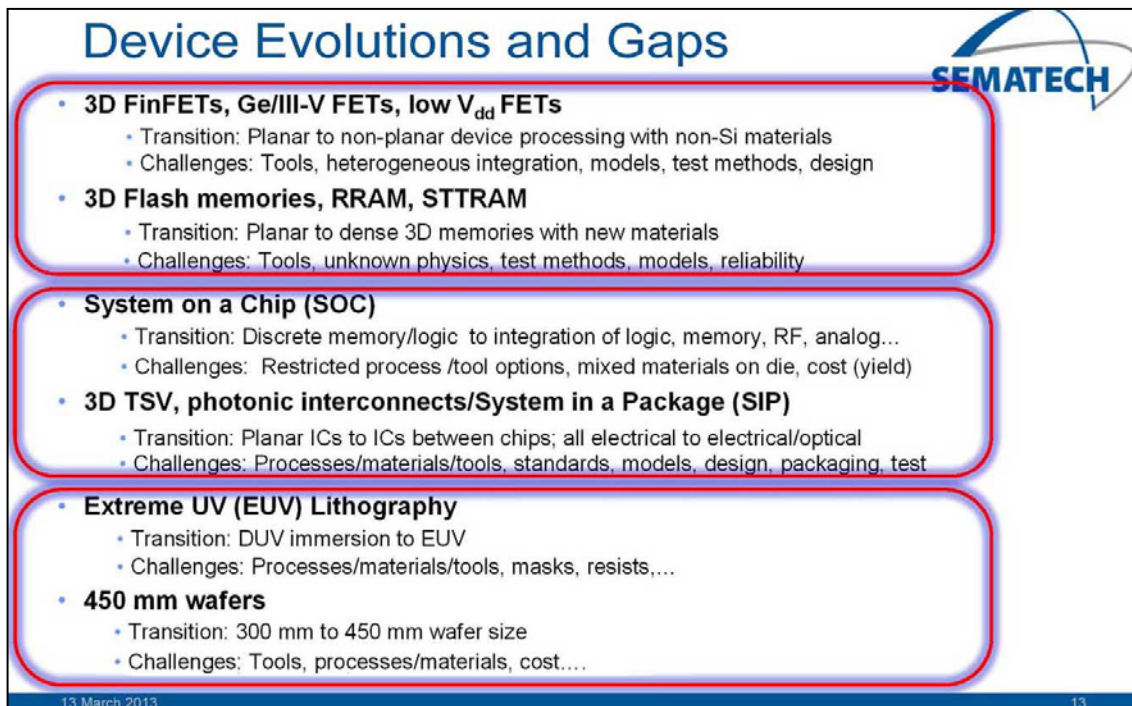


Fig. 13

towards 3-dimensional devices. We are no longer making devices on a flat surface, but we are making 3-dimensional structures. Scaling itself is going to take advantage of 3-dimensional structures now. Next important piece is that a lot of new non-silicon materials are coming out both for logic and for memory.

We need electrons in a memory device in order to store a piece of information. The current memory technologies, however, do not store enough electrons. We have about 10 electrons in each memory cell. The 10 electrons are not good enough statistically to ensure that we can come back and access the information after one year. That is a big issue. Another important part is low power. Because of low power or ultra-low power technologies, we may not use CMOS, but we may use something different technology. It is another important change that is coming up.

The next changes that we should be looking into are the System-On-a-Chip and System-In-a-Package, which we talked earlier. These two are also significant changes because we are putting different components on the same die. You have the same size of die, but you have a lot more functionality coming from the die. Thus, System-On-a-Chip and System-In-a-Package are new important trends.

The last one is an equipment-based change. You need the right two sets of infrastructure. Extreme UV is one area, which is extremely difficult, and there are a lot of works going on in that direction. The other is wafer size; there is a transition from 300 mm to 450 mm diameter.

Each of these things has a huge amount of works and resources that are necessary to make these changes happen. What is interesting to me is that the industry is pursuing all these changes at the same time today. In the past, even if you did one of them, it was a large change. But we are all working hard to cause all of these changes at the same time. That is the big challenge.



Fig. 14

Now, let me talk about the cost of R&D and what is happening in the cost of R&D. Before that, I would like to mention a little bit of the history of the industry itself. The semiconductor industry started in the United States, Silicon Valley area, 50 years ago (see Fig. 12). It was Bell Lab. that invented the first transistor. A lot of the semiconductor industry started in the Silicon Valley area, and this industry is continuing to grow faster than the GDP of the United States. The semiconductor industry is needed economically. If there is not this industry, the economy will collapse

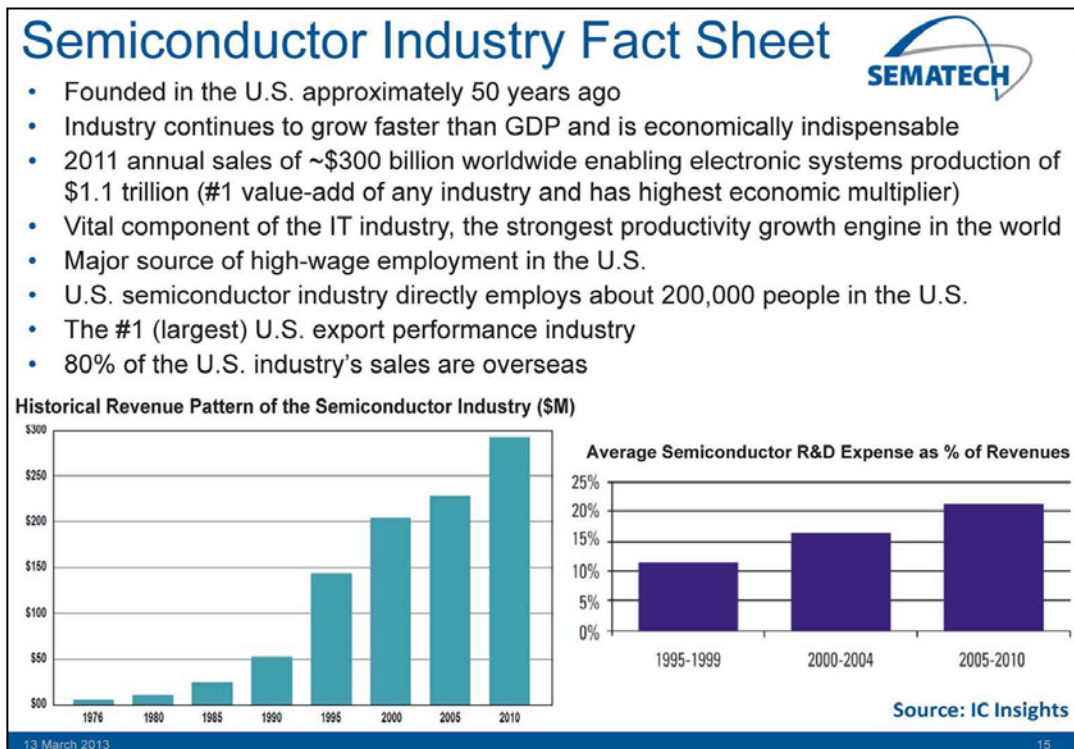


Fig. 15

in many countries.

The annual sale in 2011 was \$300 billion worldwide. That \$300 billion allows for making systems that are valued at \$1.1 trillion, and allows for a huge employment potential. These are very large numbers because they also have an economic multiplier factor. Every high-technology job creates 5 to 10 other jobs. Thus, the economic multiplier factor is very high in this industry. Because the semiconductor industry is a very vital component of IT, it is a growth engine for the world. In the U.S., the semiconductor industry has the largest employer with high wages. There are about 200,000 people employed in this industry in U.S. alone. Now, it is the number-one export performance industry for U.S. along with jet engines and aircraft. Eighty percent of the U.S. industry sales are outside the United States. Thus, a lot of exports come from this.

The worldwide revenue is continuing to increase. The interesting fact to me is that the ratio of R&D expense to the revenue is also going up. Very few industries can claim that they will spend 20% of their revenue for R&D. It is a necessity at the same time in the semiconductor industry.

This is probably a sign of the future and how things are going to be looked at, not only in this industry but other industries as well, biotechnology and medical technology and so on. Why is this happening? One reason why this was inevitable to happen in many industries in the past is that the industry was vertically integrated. For example,

IBM, from which I came, used to make its own systems. They had their own design house where they had design teams. They had packaging and assembly plants. They also kept internally developed chip technology such as

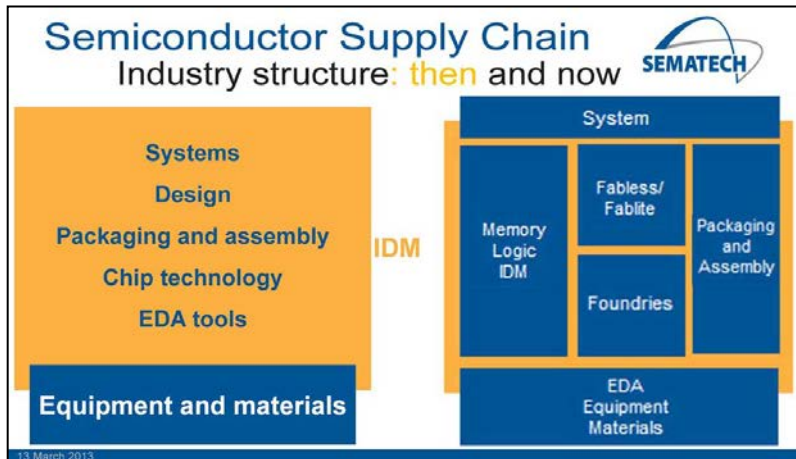


Fig. 16

process technology. They also made their own software tools for verification and design layout. Of course, they did not buy the equipment and materials from outside. That was before.

Today, the industry is fragmented (see Fig. 16). Since mid-90s, the industry splits up into several segments. Many companies decided to become fables. In fact, some newly started companies were purely design-driven and fables. They contracted manufacturing to a foundry. Memory, logic, and IDMs (Integrated Device Manufacturer) essentially became a small separate segment. Packaging and assembly became a separate segment. EDA (Electronic Design Automation), equipment, and materials became another segment with suppliers clearly being distinguished there.

Now, at the top is the system house. The companies that make systems are the ones

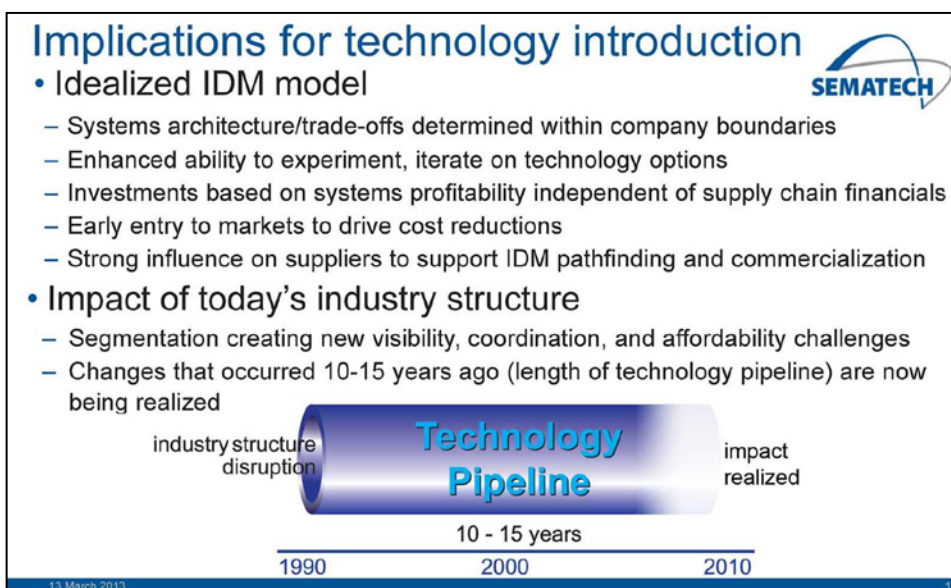


Fig. 17

that control the profits in the industry today. They do not necessarily need to spend as much money for R&D as I have shown. R&D burden is continuously getting pushed down. This is a very important change that has taken place.

Another important issue is how long it takes for a new concept to become a manufacturable idea. It takes at least ten years. Many concepts that we are using today have been looked at for almost 10 to 20 years by the universities, by research labs, or by national labs. It took a long time before they became production-worthy. There is a very long technology pipeline (see Fig. 17). It needs a long time and a lot of resources for that to happen.

Again, if each company is spending money on their own technology development in this fashion, you can imagine how much money is going to be spent in the whole industry. That is exactly what the problem is today. The semiconductor industry revenue is growing, but it is flattening out (Fig. 18). However, the total R&D cost, as a part of that revenue, is also growing. The gap, which is essentially the profit that companies make, is shrinking and reducing rapidly. That is a dangerous sign. Every company is forced to spend money on R&D multiple times. This is what needs to be addressed.

The revenue itself of the semiconductor industry is growing for a long period. However, the revenue is becoming flat although there is a variation on the equipment side. The equipment is crucial for the semiconductor manufacturing. In fact, you cannot make chips without the right equipment.

Japan is very strong in the equipment industry. Today, the equipment industry and material supply industry are very strong in the U.S. and Japan. That is very important because we may not have to make the chips like we used to make. If the equipment

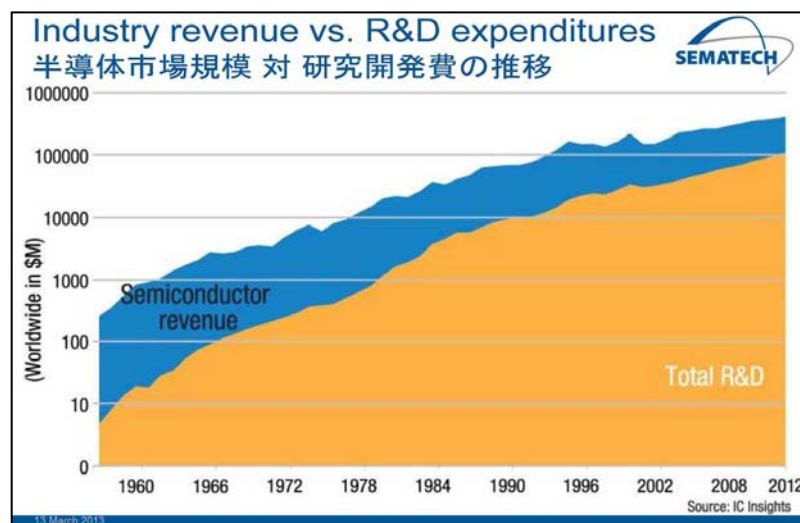


Fig.18

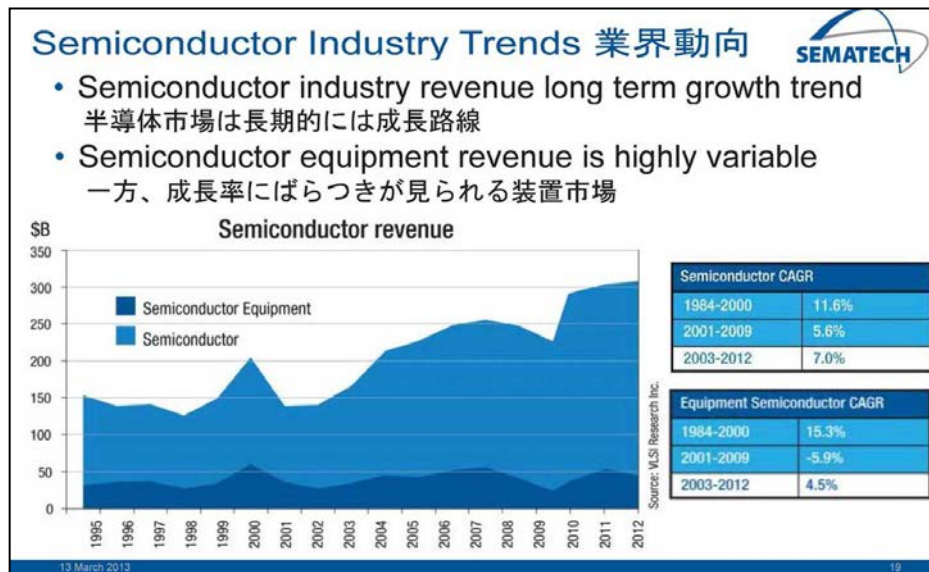


Fig. 19

industry makes better equipment, it is a very controlling factor. That is a very important issue. Now, at the same time, the revenues of equipment industry are very flat (Fig 19). I will talk subsequently about how we make better equipment. I am going to come back to this topic.

Another important trend is the significant consolidation. The top-five OEMs (Original Equipment Manufactures) are supplying up to 60% of the market (Fig. 20).

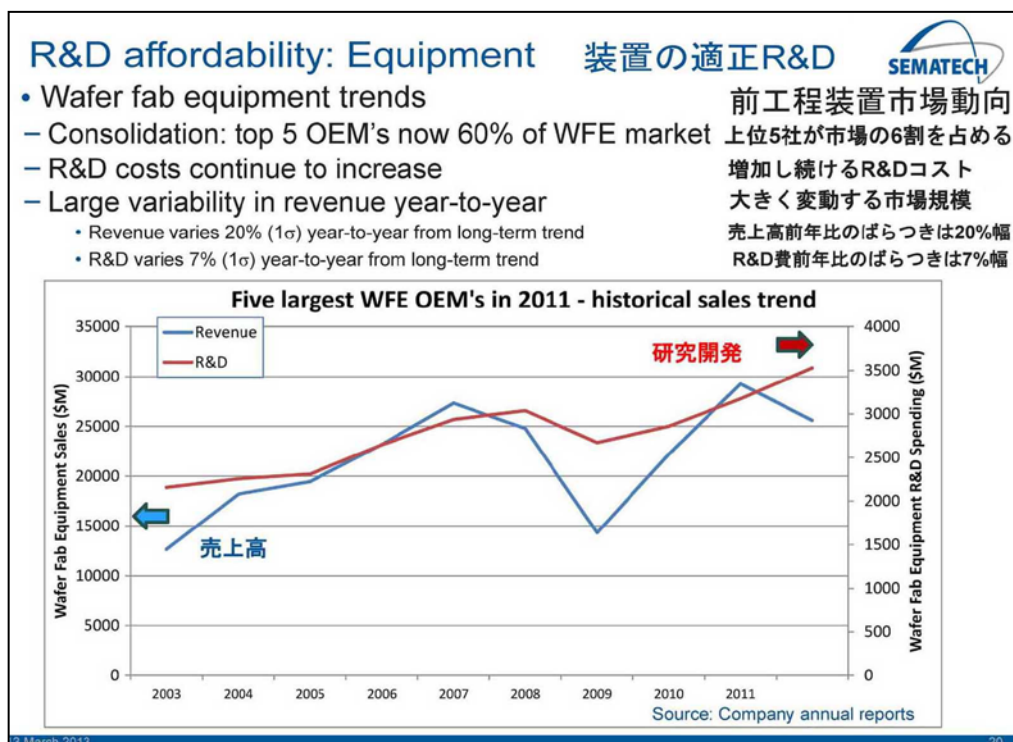


Fig. 20

There are five chip-making companies and also there are five equipment-making companies. Namely, the five equipment-making companies are supplying to the five chip-making companies for a \$300 billion. Therefore, the risk becomes higher than ever before.

Losing some chance from a chip-making company may drive equipment companies out of business. That is a big risk factor. You can see some of these risk factors in the large year-to-year variability of revenue shown in Fig. 20, but their R&D cost has to keep up without that kind of variability. The shock is very high in the industry.

The same thing happens to the equipment sub-system (Fig. 21). When equipment companies make equipment, they need the pumps, robotics, and all kinds of sub-components that go into the equipment. The sales variability is even higher for such subsystem supplier as shown in Fig. 21. They are much more reactive; their R&D budget shakes and goes up and down almost in step with what the industry needs. This is a problem because the technology is so high-end that we need the sub-components to be much higher quality than before. If we have low quality sub-components in today's fab, we would lose billions of dollars quickly. We have to be very careful about that.

Here, I would like to say that technologies drive our success in the industry (Fig. 22). So, how do we bring a new technology from a lab to fab? To do that, a comprehensive and industry-wide collaboration is important. The challenges are global because the industry is also global. In fact, problems cut across companies many times. To find a

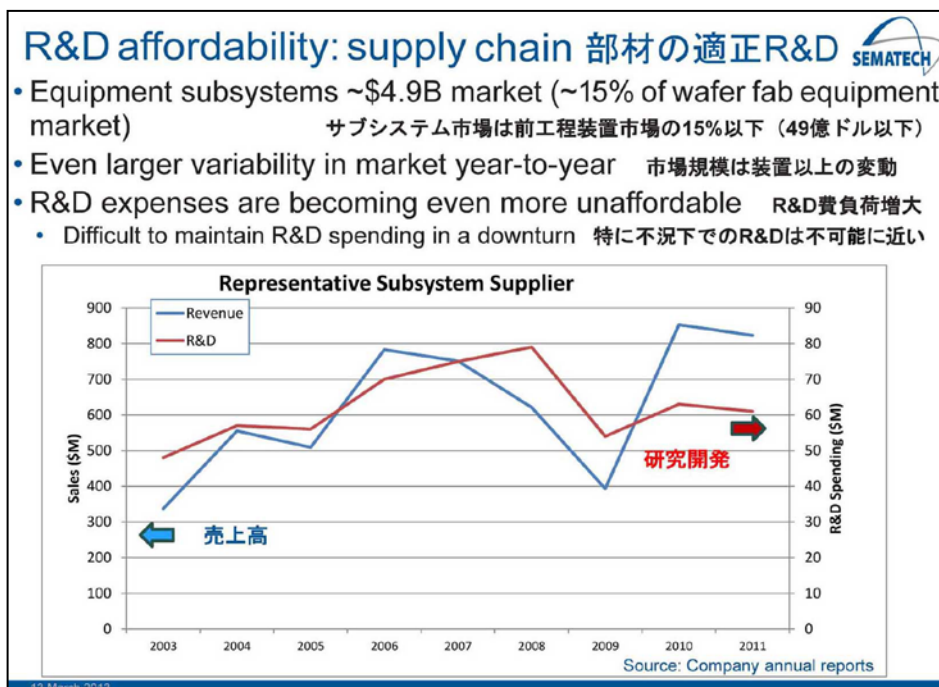


Fig. 21

new technology, you need to align the material supplier and new equipment company. Consequently, the supply chain has to be completely aligned. Eventually, they have to supply to these large companies in a very high volume. If there is no supply chain alignment across the globe, it may be difficult to manufacture.

Too many challenges to solve alone
 協業での取り組みが必要とされる課題解決 SEMATECH

- Success in semiconductors is driven by technology innovation and advances in manufacturing
 半導体事業の成功を導く、「技術革新」と「先端生産技術」
- Success depends on comprehensive industry-wide collaboration 成功の秘訣は「業界の協業」
 - Challenges are global, and cut across industry ecosystem
 - Solutions require significant investment, leveraged funding

SIA SRC Semiconductor Research Corporation SEMATECH semi
 EIDEC imec GSA ITRI Industrial Technology Research Institute ITRS

13 March 2013

Fig. 22

The significant investment is also necessary for these things to be successful. Therefore, there are many consortia in the industry today. Some of them are the large-sized consortia that are working. There are a few consortia in Japan, but I choose EIDEC (EUVL Infrastructure Development Center) specifically because it is developing very important future technologies by getting a lot of contributions from many companies.

Contents 目次 SEMATECH

- History of SEMATECH, collaboration model and impact
 SEMATECHの歩み: 協業モデルと影響力

13 March 2013

Fig. 23

Now, let me talk about SEMATECH itself. The need for high technology and the need for collaborative work brought SEMATECH to life. SEMATECH was established in 1987 by the government of the United States, both the defense department and the House Science & Technology Committee (see Fig. 24). They got together and put \$100 million per year. The industry also started putting \$100 million per year. That was the original budget for SEMATECH. It is, of course, a non-profitable consortium, and was supposed to be an experiment for five years. Today, it is 26 years old; we just finished our 25th year anniversary.

It is interesting to me that in Washington D.C, today, whenever there is a crisis in any industry, the government wants to start a SEMATECH for that industry. When we had a problem in the auto industry in Detroit in 2008, the government of the United States said, “We should start a SEMATECH for the auto industry.” It was a problem with battery technology, and the government said, “We should start SEMATECH for the battery industry.” For the solar industry, they had a similar concept.

I would emphasize that SEMATECH is a very successful model. The government likes this kind of model and thinks that many industries can benefit from that model. Personally, however, I do not believe that the same model can be applied across all industries. They have to have the right situation for it to be successful. I will talk about that subsequently, but that is my opinion.

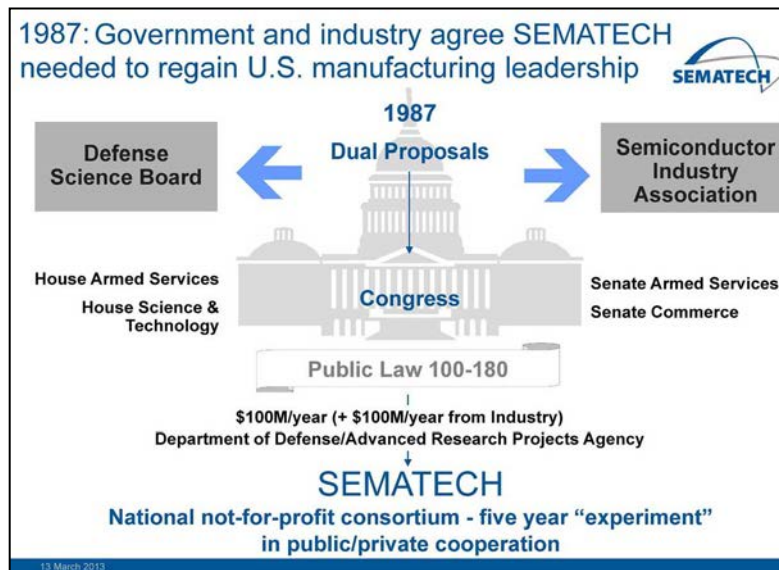


Fig. 24

Once SEMATECH was established, there was a definite impact. We saw that the industry in the U.S., which was declining, started picking up and it improved to a leadership position (Fig. 25). One of the focus areas at SEMATECH was how we improved the equipment quality and reliability in order to boost the device yield. That was the focal theme when SEMATECH was established. We saw that it had an impact and the benefit came out.

Since then, SEMATECH moved on from the initial position of serving the U.S. industry to the next position very quickly; it became a part of the international community because the U.S. government, as well as the member companies of SEMATECH, realized that this problem is not local to the United State. This problem is global. We have to work together with many companies in many other countries.

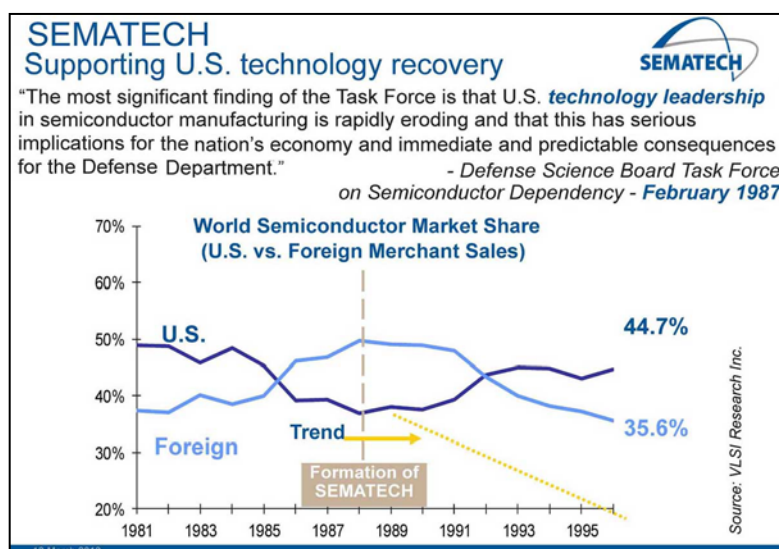


Fig. 25

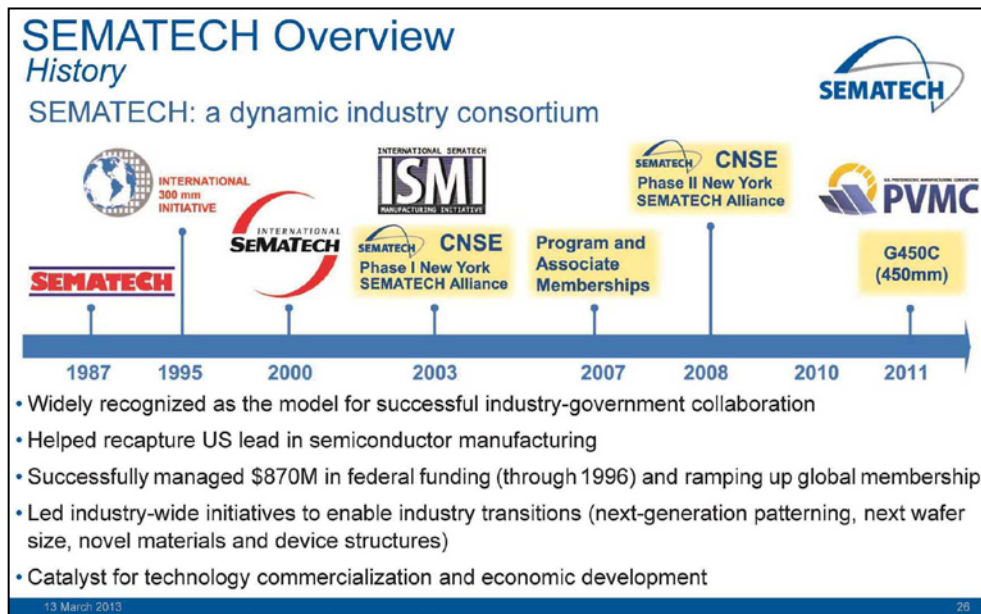


Fig. 26

The first step was the transition to 300mm wafer size. The wafers were 200mm diameter before that, and the industry was considering to switch to 300mm. They used that as an opportunity to form the “International 300mm Initiative,” which was the first international consortium (Fig. 26). From that time, SEMATECH became permanently international SEMATECH.

Then we started looking at different opportunities. One main opportunity, which we were pursuing, is our relationship with the State of New York and the College of Nanoscale Science and Engineering (CNSE) in the State University of New York (see Figs. 26). That is our partner.

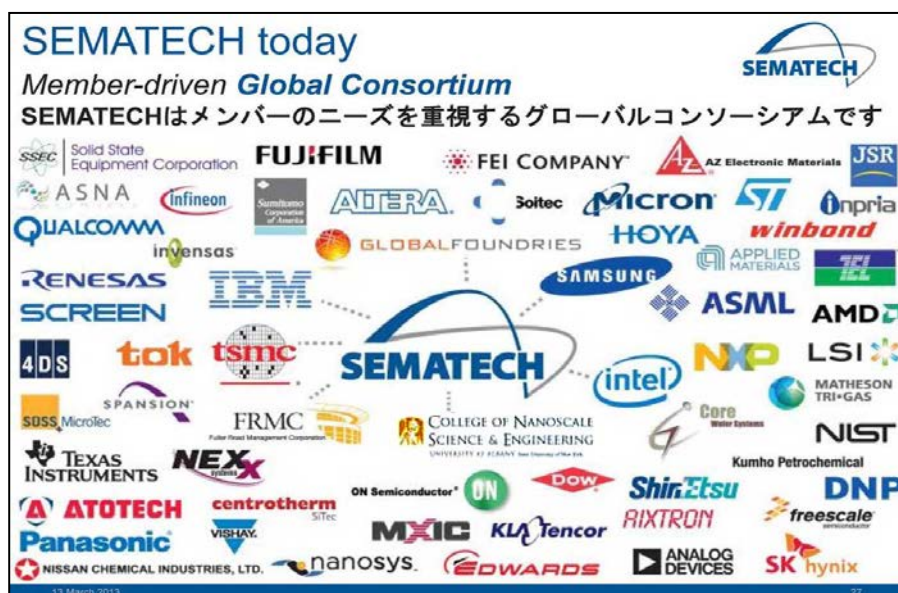


Fig. 27

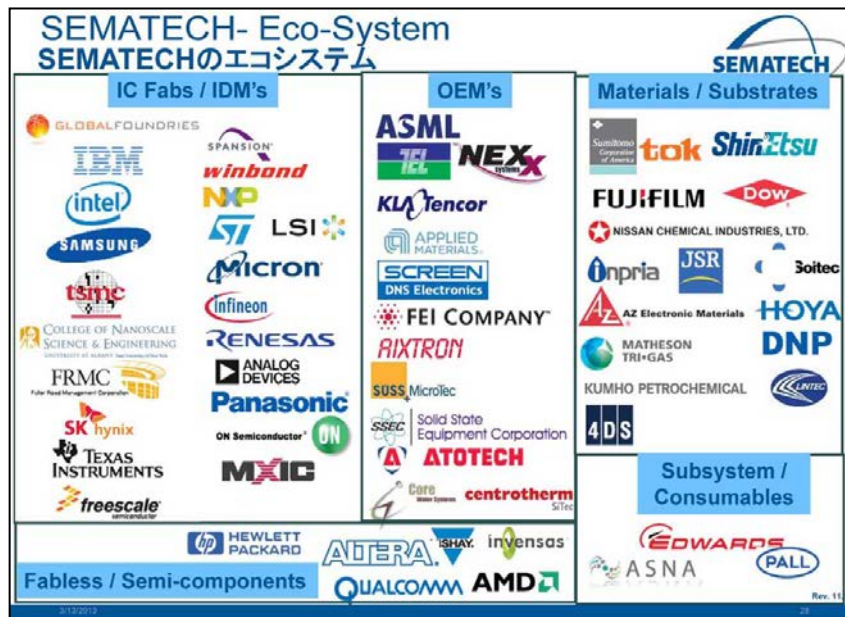


Fig. 28

There are two important partnerships that we have right now. The U.S. Department of Energy asked us to work on photovoltaics to improve the manufacturability. So we started the photovoltaic manufacturing consortium (PVMC) with the U.S. Department of Energy. There is also a work going on in 450 mm wafer size transition; G450C. Now, this whole SEMATECH model, a catalyst for the industry to develop technology, has been recognized as being quite successful.

Thus, SEMATECH is a global consortium today (Fig. 27). Originally, we had only the chip-making companies, but we have now more members from the entire industry even though the chip-making companies are the core members.

We have people from the SEMATECH Ecosystem (Fig. 28), which consists of IC fabs such as IBM, original equipment manufacturers (OEMs) or equipment suppliers, and materials and substrates suppliers. We have subsystem or consumable suppliers, fabless companies, and semi-component companies as well, who become a part of this consortium. It is very important that the entire Ecosystem comes into play together at the same time. It is necessary to have everybody's opinion because somebody else may impact the person who uses it at the end. We see that such examples are increasing.

The other important thing is that SEMATECH has a strong worldwide network among chipmakers, suppliers, universities, and government agencies including the State of New York (Fig. 29). Although the State of New York is a very important partner for us, we also have relationships with many government agencies around the world, and we have the facilities and research activities there. We work with research labs not only in the United States but also in other countries. The partnership with suppliers is

also very close and dense. More than 60 universities are also in our partnership today. We continue to expand the relationship with universities because it is important for us to develop new ideas and new research projects.

If we summarize this, I should say that SEMATECH Ecosystem is a good example of very strong partnerships among industry, academia and government (Fig. 30). Some of the universities and national labs are listed here.

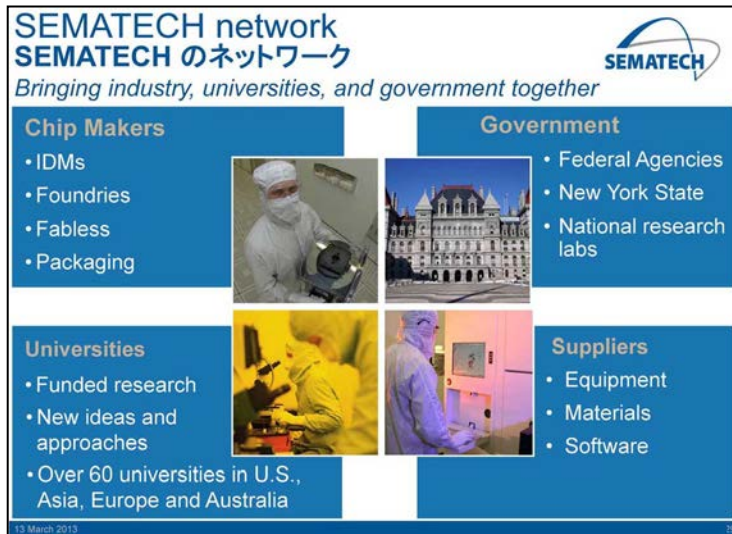


Fig. 29

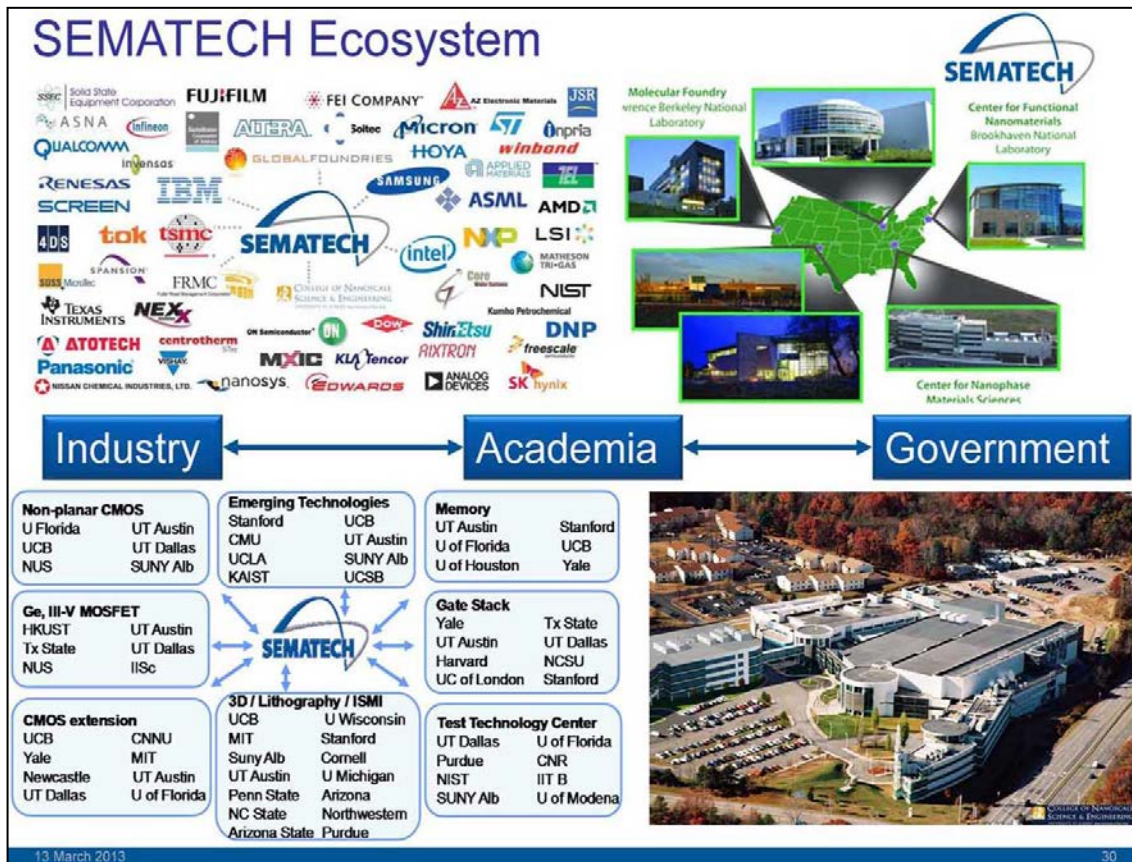


Fig. 30

Let me show you where SEMATECH was started first. In 1987, SEMATECH was started in Austin. Figure 31 is a 200mm facility. It has been sold and now it is a private facility of R&D foundry that runs over there. Of course, we continue to maintain a small presence in this facility, but most of our activities are in New York

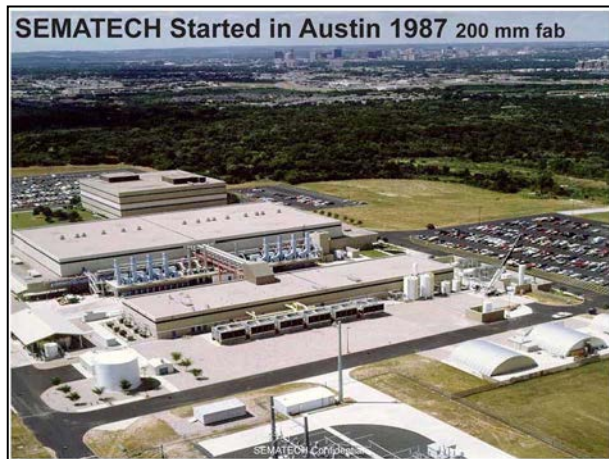


Fig. 31

In New York, there is a 300 mm fabrication facility that the State of New York has built. It was necessary for us to move because we had an opportunity to make the transition to 300 mm in this core facility by ourselves (see Fig. 32). Otherwise, we could spend almost a few hundred million dollars to convert the fab to 300 mm. We were able to collaborate with other companies like IBM and the State of New York, and were able to use this facility. Thus, SEMATECH, IBM and the State of New York collaborated together to get this facility going. Today, the same office building is shared by all of us: The entire second floor is for SEMATECH, the third floor is for IBM and partners, and the fourth floor is for the university faculty.

Subsequent to the original fab, we constructed the additional fab, NanoFab 300

SEMATECH Locations - Albany

Current CNSE facilities and key site partners

NanoFab 300 South
\$75M, 150K ft²
32K Cleanroom
Completed: 3/04

NanoFab 300 North
\$200M, 228K ft²
35K Cleanroom
Completed: 12/05

NanoFab 300 Central
\$100M, 100K ft²
15K Cleanroom
Completed: 1/09

NanoFab 200
\$35M, 70K ft²
4K Cleanroom
Completed: 6/97

NanoFab 300 East
\$100M, 250K ft²
Completed: 3/09

SEMATECH

SEMATECH & CNSE Partnership Roles

University

COLLEGE OF NANOSCALE SCIENCE & ENGINEERING
UNIVERSITY AT ALBANY State University of New York

Industry

Suppliers

- ◆ 800,000 sq. ft. of cutting-edge facilities, with 85,000 sq. ft. of 300mm cleanrooms with a planned expansion to 1,250,000 sq. ft. 105,000 sq. ft. of 300 and 450mm cleanrooms
- ◆ More than 250 industry partners including electronics, energy, defense & biohealth
- ◆ Over \$12B investments and over 2,600 R&D jobs currently on site (projected increase to 3500 R&D jobs by 2013)

13 March 2013 32

Fig. 32

North, which has a 300 mm cleanroom, and the total area is about 228,000 square feet. When we were constructing this fab, we ran out of space because there were too many tools for many programs at that point. We needed to construct an extension fab of 300 mm right by the side of that. Today, in fact, all three fabs are full, and there is no room to put a new tool. If we want to bring a new tool here, we have to throw something out.

When we started the 450 mm program and the EUV (Extreme Ultraviolet Lithography) program, we realized that a new facility was needed. So we needed a new building right across the street. Figure 32 is an old picture, and this new building is almost done. The total square footage available on the site today is 800,000 square feet of office space, not counting the new building. We will be adding even more space when the new building is fully functional.

There are 2,600 R&D jobs on the site today. The total investment is about \$12 billion in this facility, from industry, government and others. What is also important is there are more than 250 industry partners working on this site. Now, we have many companies working with us (see Figs. 27 and 28). We also have the equipment suppliers who have established room capabilities there. That is a very important component of how this place is working today.

President Obama visited us to inaugurate the new building last year (Fig. 33), and we were all quite inspired by having President Obama there. The new building is up and running now.

I want to switch my topics and talk about SEMATECH's program (Fig. 34). What does SEMATECH do? What do they focus on? Do they research? Do they develop something? Do they manufacture something? Those are questions that you may have.

We do not research because a basic research is not interesting for us. We do not manufacture anything because it is left to companies. What we do is the technology development. We do work a little bit with universities and national labs, so that there is applied research that is being done, and so that we understand what are the new components coming out of



Fig. 33

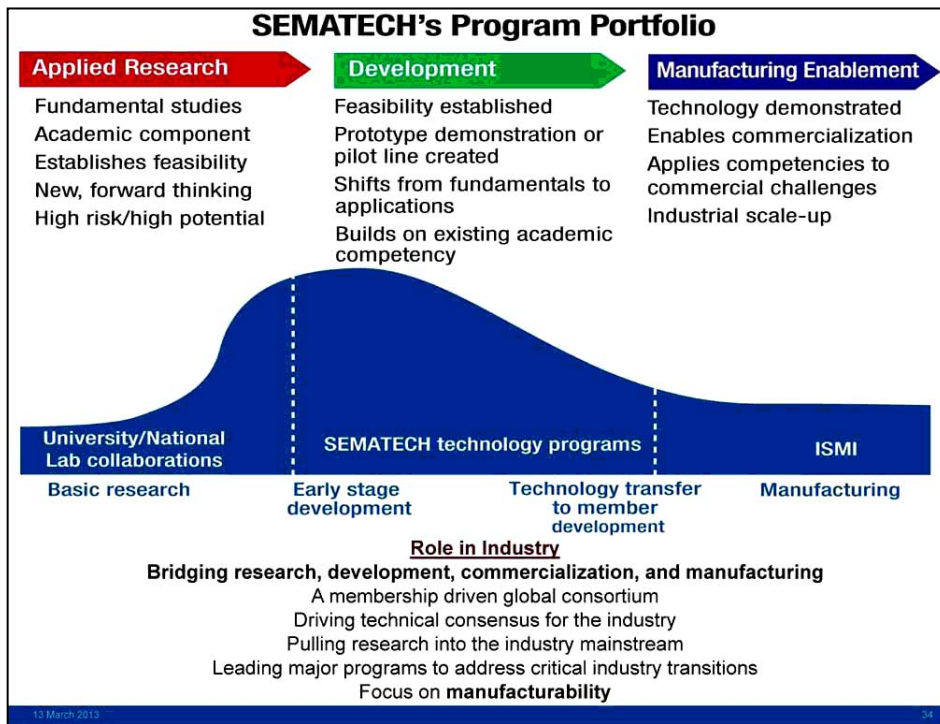


Fig. 34

universities and what are the promising new ideas. How do we take that idea from a lab and make it manufacturing-worthy? How do we take it to a fab?

If we have a new technology, can we just directly manufacture it? Maybe we cannot. Do we have the right equipment? Do we have a good understanding of what kind of materials are needed? What kind of precursor is appropriate first? Do we have the right model? We want to understand liability, and we want to understand failure mechanism in these materials. There is a lot of work that happens at SEMATECH.

There are fundamental works such as basic physics and engineering. They are, however, common works, and all the member companies need the works anyway. They can do the works by themselves with spending a lot of money, or they can come to SEMATECH and share resources. Once they do that, then they can bring it back to their own company and become competitive. That is where we focus. A technology has been manufactured, and then we go there and say, “How do we make it more efficient? Is the equipment consuming too much electricity? Is this process consuming too much water? Is there an environmental or a safety issue with these chemistries or these precursors? How can we address those things?” Those are important issues as well. Those kinds of things are tackled by one of our groups called ISMI.

This is the comprehensive set of activities that we have (Fig. 34.). It is very important that we are membership-driven; we do not conduct these projects just by ourselves, but we get direction from the industry. They tell us, “We need this. How we

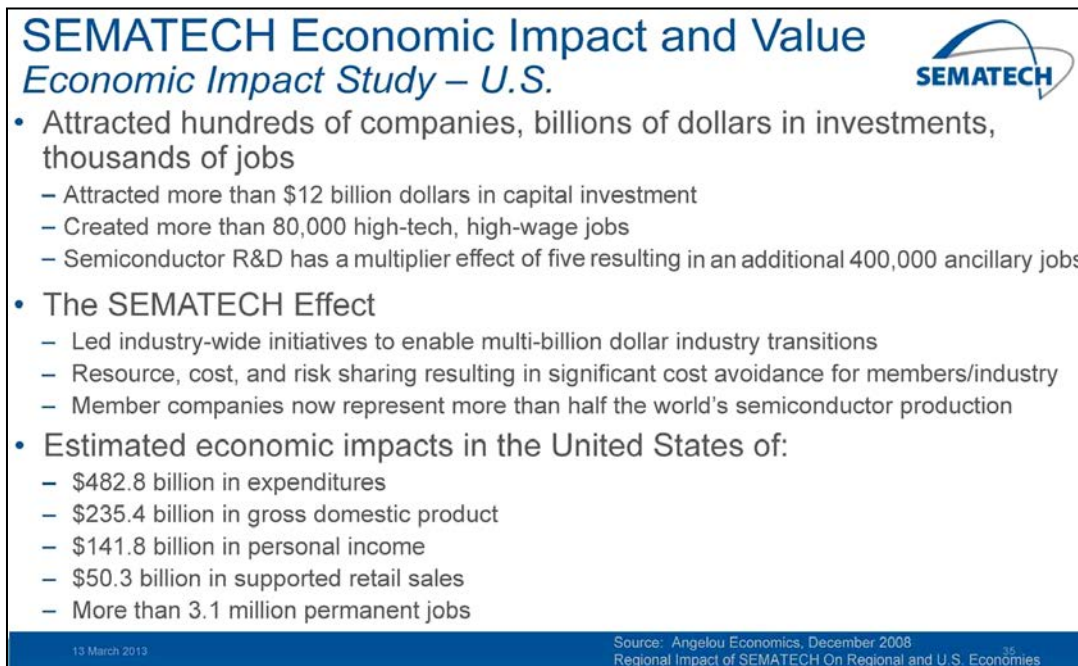


Fig. 35

are going to put this together?” Thus, we work with them to define problems and milestones, and develop the technology. We also get consensus from the industry so that there is a common standard and common benchmarking. It is very important for us to make sure that the problems are critical so that companies cannot solve themselves. If the company can solve them alone, there is no point in wasting our resources there.

The economic impact of SEMATECH is quite large (see Fig. 35). The economic impact study was done by AngelouEconomics, an independent economic development consulting firm, in December, 2008. At that time, huge numbers were derived as a benefit because of the establishment of this consortium; \$482 billion in expenditure, \$235 billion in GDP, and \$141 billion increase in personal income. These are very impressive numbers. It started in Texas that was cowboy country before 1987. It was dependent on oil and ranching. That was the economy in Texas. Today the high-technology industry is the largest employer in the State of Texas. There is a proof which tells why this kind of consortium is valuable.

Let me summarize here as shown in Fig. 36. A trend in the industry is consolidation. Both device makers and supply chain have significant consolidation. The cost of R&D is rising; very few funders can invest. The problem in the supply chain is an insufficient early feedback from the device makers. Infrastructure affordability is very expensive. A material supplier needs to have the equipment, and also needs to have the best structures that are electrically testable. Where do they get that? They are neither a chip maker nor an equipment maker. Hence, infrastructure access is very important, and the

business model may be broken because of this. The R&D burden is pushed down because the cost is high for the smaller companies. Therefore, a compelling collaborative model is necessary, and it is also important to show a clear pathway to 450 mm activity.

Trends 業界の動向 SEMATECH

- Consolidation – device makers, supply chain
デバイスメーカーならびにサプライチェーンの統合化
- Rising R&D costs with fewer funders
増加するR&D費用と減少する出資者
- Supply chain challenges サプライチェーンの課題
 - Insufficient early feedback 不十分な早期フィードバック
 - Affordable infrastructure リーズナブルな費用のインフラ
 - Broken business models 衰弱したビジネスモデル
 - Greater share of the R&D burden R&D負荷の増加
- Increasing need/pressure to collaborate
協業の必要性の増加
- A growing and compelling collaborative model in Albany and clear pathway to 450mm activities
NY州アルバニーにおける成長し説得力のある協業モデルと450mm移行への明確な経路

13 March 2013

Fig. 36

Contents 目次 SEMATECH

- Major technology transitions in semiconductor industry
半導体産業における主要なテクノロジーの推移

13 March 2013

Fig. 37

Now, let me quickly go through some of the technology transitions and why this is important (Fig. 38). Especially, I want to share with you the magnitude of the problem

Major manufacturing technology transitions SEMATECH				
Wafer Size				
200mm	→	300mm	→	450mm
One company		Consortium of chipmakers and collaboration with other consortia		Consortium of chipmakers and enhanced supplier role
Devices				
SiON	→	Strain	→	High-k
Consortia initiated and IDM led		IDM led		Collaboration across consortia (FEP Research Center) and IDM led
				FinFETs or Ge/III-V channels or ETSOI or... IDM led and collaborative innovation
Interconnect				
Cu	→	Low-k	→	3D
IDM led		IDM led and collaboration across consortia		Collaborative innovation across entire supply chain
Lithography				
248 nm	→	193 nm	→	Immersion
IDM led		Consortia initiated and IDM led		IDM & supplier with consortium support
				Double Pat → EUV IDM led Supplier leadership +EUV/EMI consortium across supply chain

13 March 2013 38

Fig. 38

we are trying to deal with as we try to make these changes. In terms of wafer size, I talked about 450mm transition. In terms of device, we experienced the change in high-k and changes to FinFETs, germanium device and other new types of devices. Interconnects are going towards 3-dimension

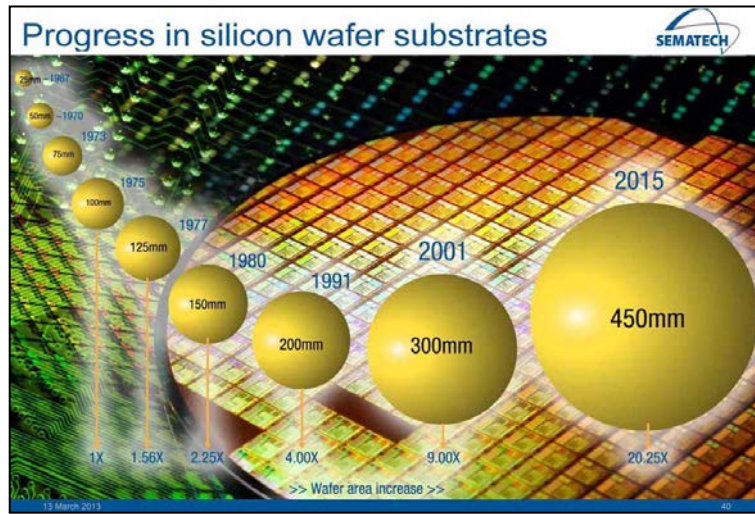


Fig. 39

connections. Lithography is going towards EUV (extreme ultraviolet). Many new changes are coming and are continuously happening.

Of course, SEMATECH has been in the middle of all these changes over the years. Our organization structure is based on those kinds of changes. Today, we have a lithography group, an interconnect group, materials and emerging technologies group, and a manufacturing group. These four groups correspond to what you see in Fig. 38. As we do some of this work, we keep a focus on what is coming in the future, but not what the industry can do today. I will explain that in a short.

From the perspective of a wafer size, we are going to 450 mm. The wafer size will become 450 mm hopefully in the next 3 to 5 years because the industry goes in that direction. The main reason for going from 100 mm to 450 mm wafer is the area advantage that reaches about 20 times (Fig. 39). You can get chips roughly 20 times more in a single process. Thus, the productivity goes up and the cost per chip should come down quite dramatically. This is the big advantage here.

I summarize the programs in SEMATECH that has been done (Fig. 40).

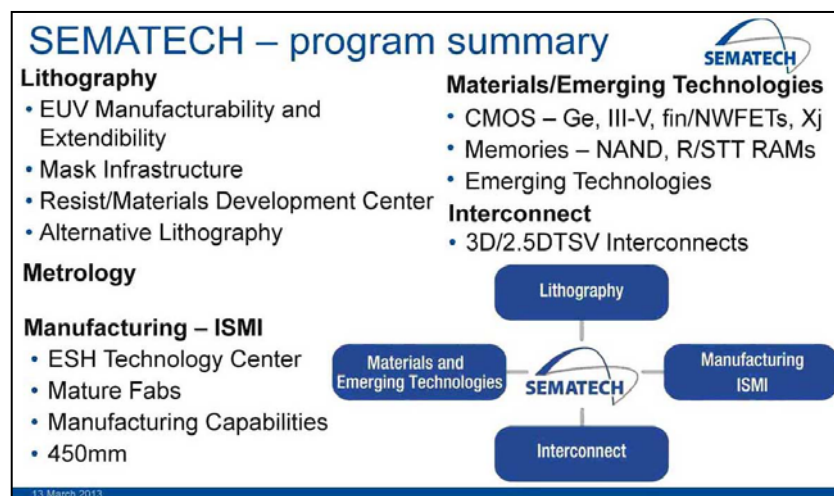


Fig. 40

Since 2007, they have been working in this area shown in Fig. 41. They have found early design and prototypes. They have made a new type of FOUPs (Front Opening Unified Pods) for carrier transport and wafer transport. They have also interoperability test bed. They have looked at many issues, and that is very useful for the industry, although it is not enough.

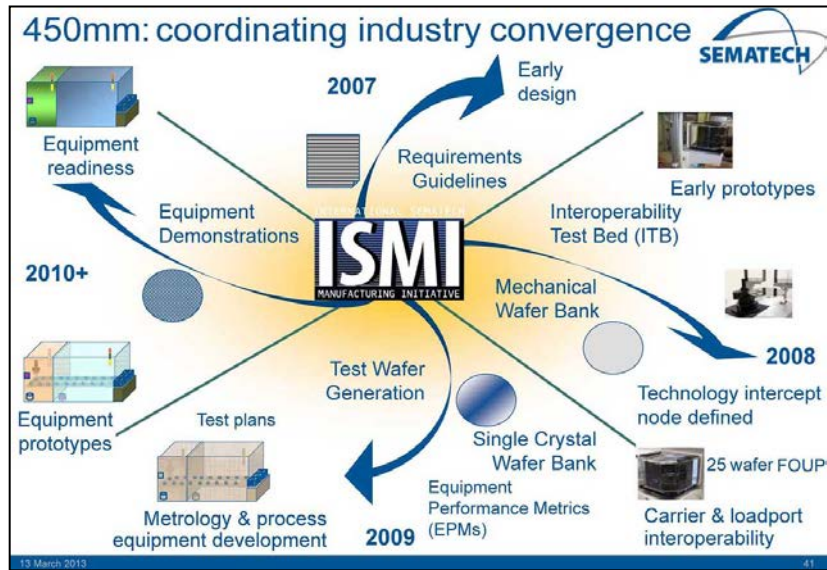


Fig. 41

Because it was not enough, there was a big gap (Fig. 42). We told the industry, “Now you need to take this information and put it into a new consortium where you have to put more resources to build that consortium. What you really need is a new fab with 450 mm.”

That takes a billion dollars at least, but SEMATECH does not have the budget. It is the industry’s job to do that at this point. That is exactly what they are doing in G450C (the Global 450mm consortium—see Fig. 43). That was started by the governor of New York as shown in the photo. You can see all the company heads are sitting here in the second photo. Heads of Intel, Samsung, IBM, Global Foundries, TSMC and other companies are there.

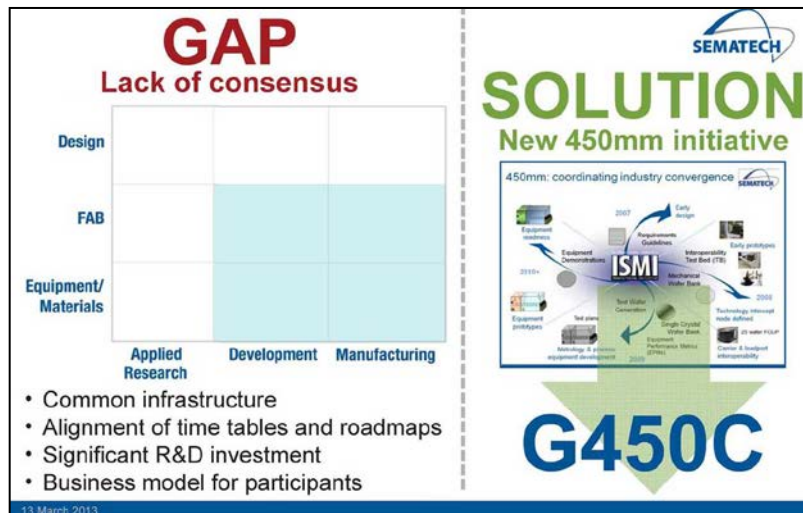


Fig. 42

The Global 450mm Consortium (G450C) SEMATECH

New York based consortium

- The announcement made September 27, 2011 at Governor Cuomo's economic development conference, was a major economic-development deal for the state – projects to boost NYS economy
- The agreement consists of two projects, totaling \$4.4B, featuring the five industry players (IBM, Intel, TSMC, Samsung, Global Foundries) who will be making substantial cash investments
- Consortium is funded to collaboratively work with suppliers to develop 450mm equipment

G450C objectives: preparing for pilot line introduction

- Test wafer operations will continue and expand as resources accelerate support of supplier development and equipment demonstrations
- Focus on scale up - minimize changes not related to wafer size to reduce risk and cost
- Demonstrate a full 450 mm tool set (~ 50 tool types)




Fig. 43

The next big challenge is lithography (Fig. 44). Lithography scaling has been continuously pushing down in terms of wavelength. Today the goal is a 13.5 nm wavelength. To make that happen, we have to do many things together.

I will show you what that is. What I want you to keep in mind is that these changes

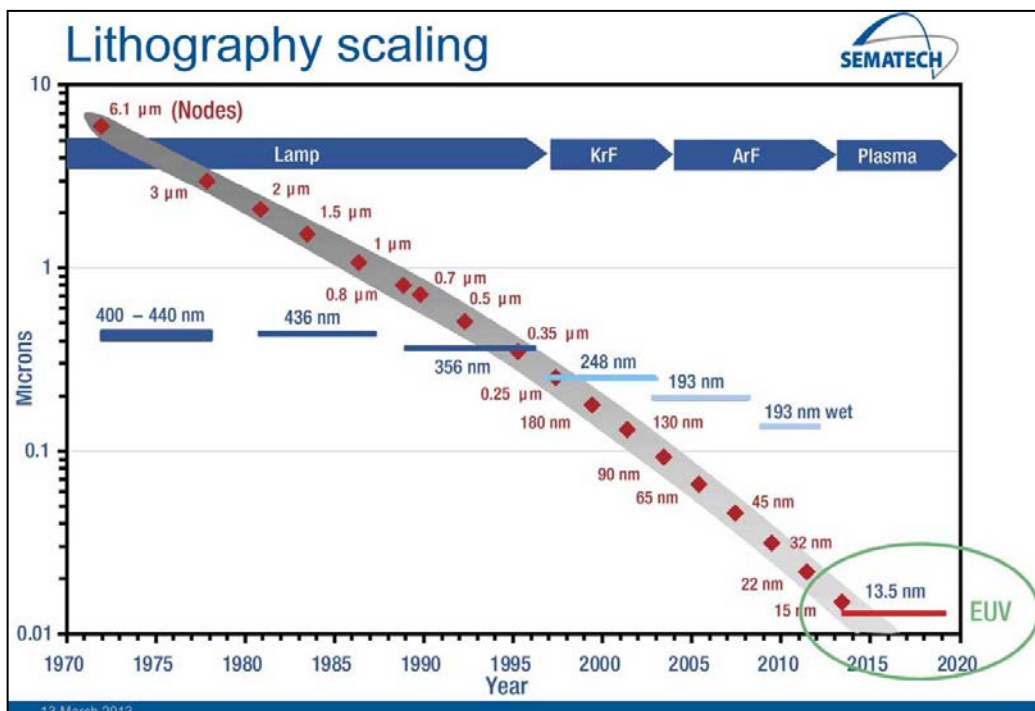


Fig. 44

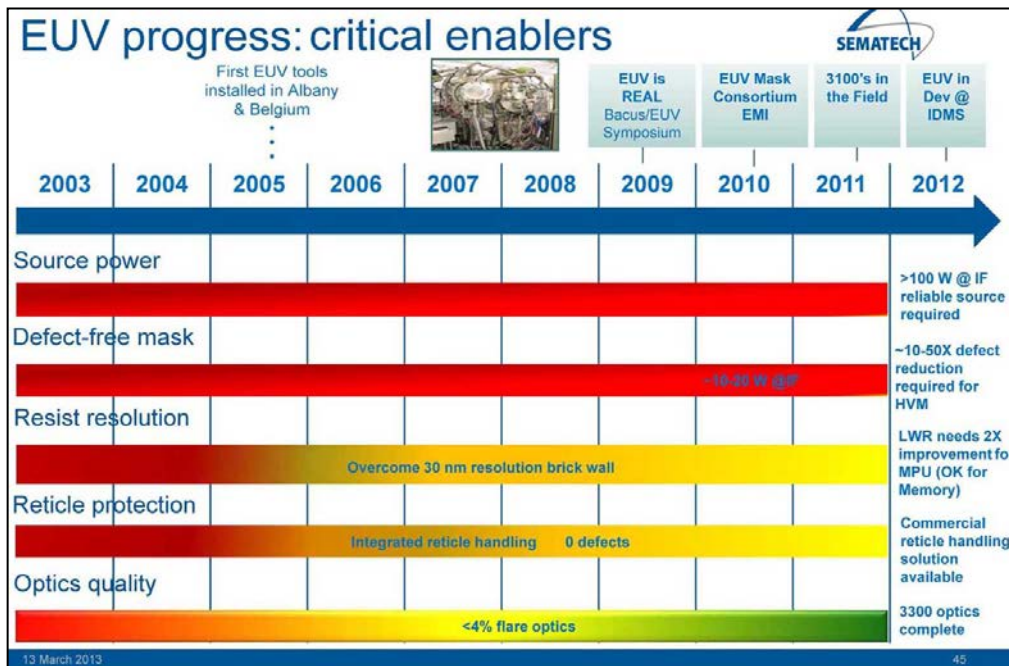


Fig. 45

are very difficult but evolutionary. If you think about the physics, it is a very natural progress. In terms of readiness, however, the technology is not completely ready (Fig. 45). The resist resolution, the reticle protection, and the optics quality have improved quite a bit. It is probably ready for manufacturing in these three aspects, but the source power is very poor; therefore, the throughput is low. The mask capability is also not very good (see Fig. 45), and we cannot make defect-free masks today. Even if we have an EUV tool, we cannot use it still because the mask technology has to improve. There is a

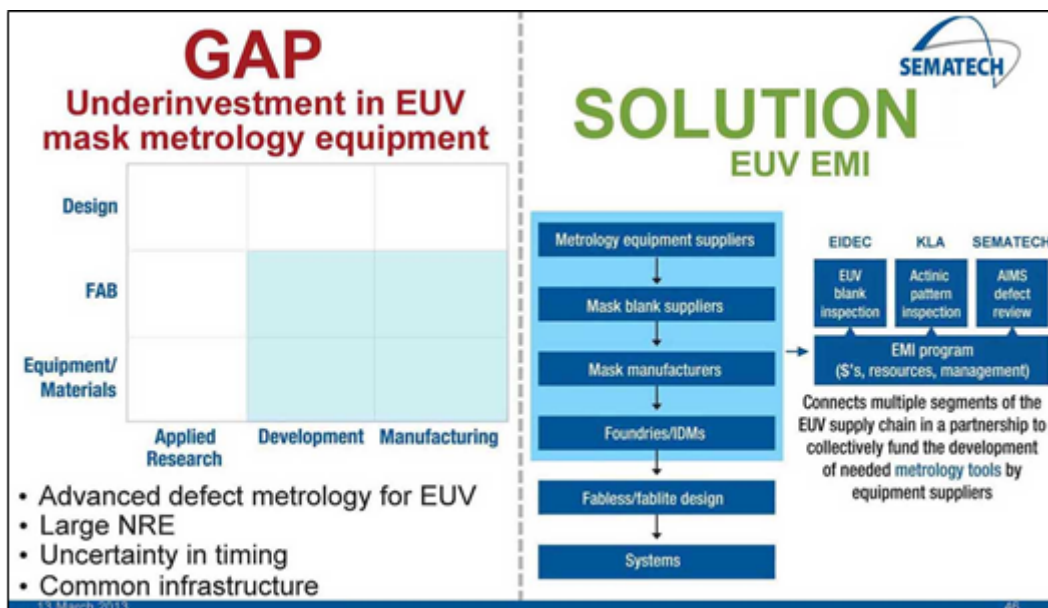


Fig. 46

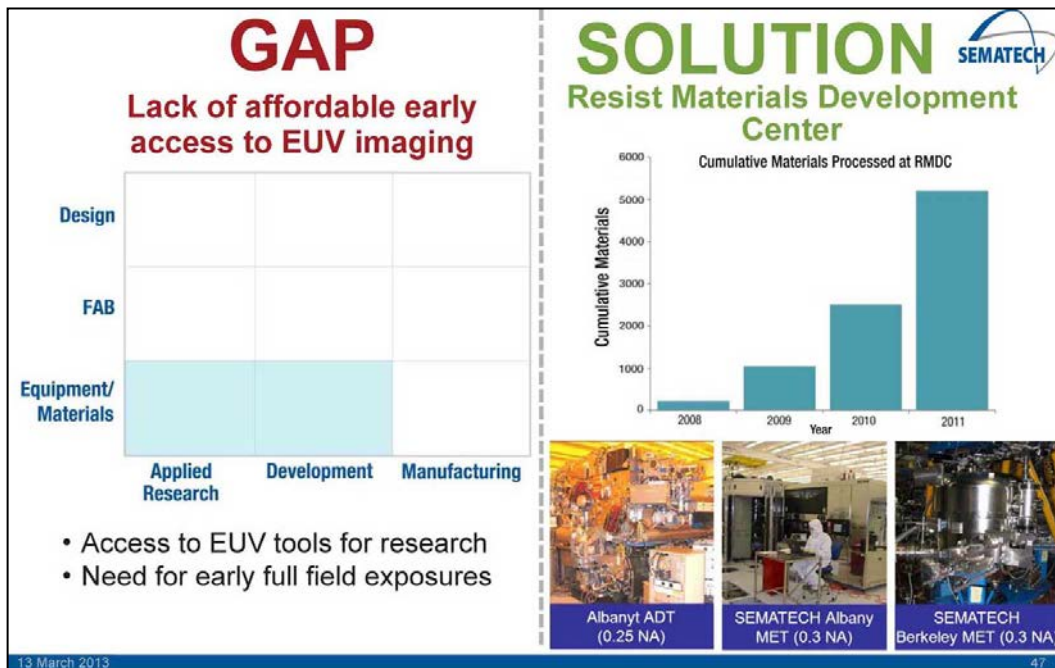


Fig. 47

lot of work that needs to be done in this area.

There is a big gap here (Fig. 46). That is why we started a group called EUV EMI that focused on mask inspection technology (see right side in Fig. 46). The resist technology has also a problem (Fig. 47). If you want to do lithography, you need to have the right-quality resist. The problem for resist suppliers is that they cannot access the EUV equipment. It is very expensive and costs more than \$120 million. Rather than having the equipment to buy it, we put the equipment together in Albany; both a large

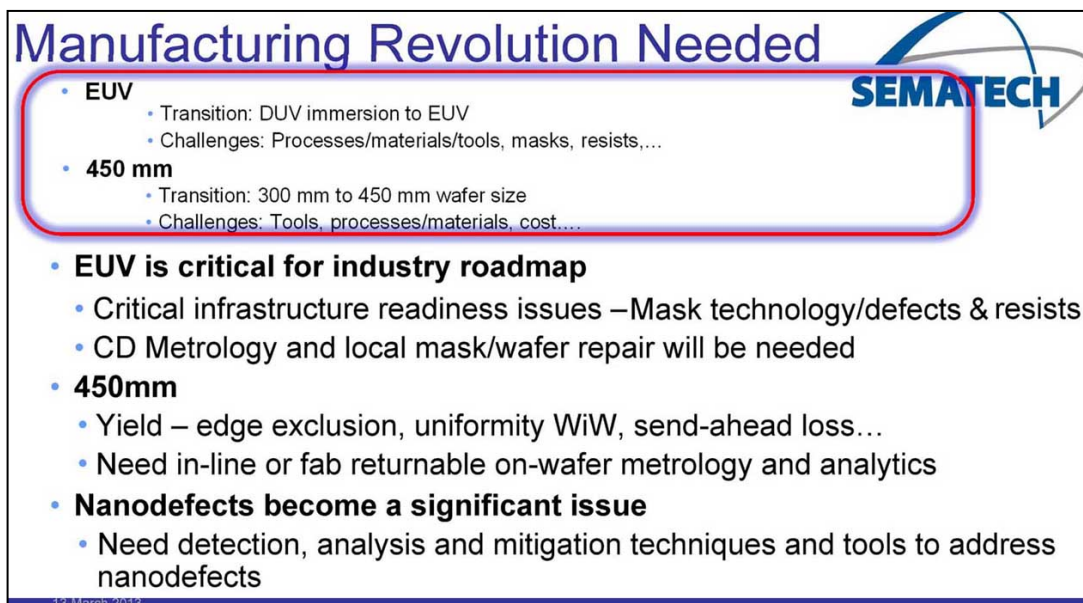


Fig. 48

exposure tool and small micro-exposure tools. We allow them to come and work with us so that they can take advantage of this and develop the resist formation.

EUV and 450 mm are the two technologies I just talked about (Fig. 48). I want to say that these two technology changes are very evolutionary; it is a very natural change. This is what we do. To manufacture these technologies, however, we need a revolutionary approach because they are difficult in terms of new physics and cost. We have to take a completely different approach.

Let us move on to the devices (Fig. 49). We have a lot of activities in both memory and logic devices, focused on advanced materials. We also have activities focused on advanced structures such as Fin-FETs, nanowire FETs, and quantum FETs. This is very common; many companies do that, too. Although some of these structures will be used at least two generations ahead, we also keep focus on what might be coming in the future. We have focused also on Graphene, NEMS-based devices, and tunneling transistors (see Fig. 49). This is important to us because some of these technologies, which are called “beyond CMOS”, quickly start moving into CMOS technology area, examples being nanowire FETs or Fin-FETs. The industry has to watch when that transition takes place and we need to drive it in the industry.

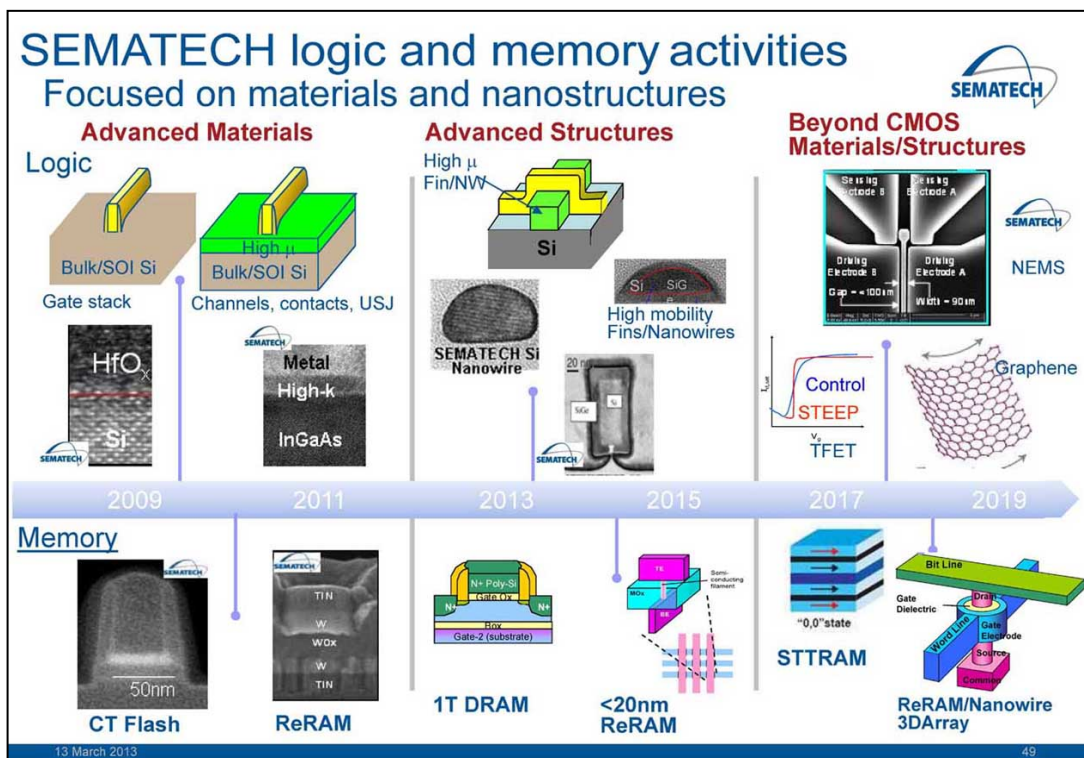


Fig. 49



Fig. 50

There is a large change that is coming up. As we make this change from planar device to non-planar Fin-FET-like devices, there is quite a big challenge. Intel introduced these technologies two years ago (Fig. 50), and the entire industry is trying to make the same change.

Some roadmaps for the industry today are firmly 3-dimensional (Fig. 51). On the roadmap, we see also that we are going towards germanium CMOS. In the germanium

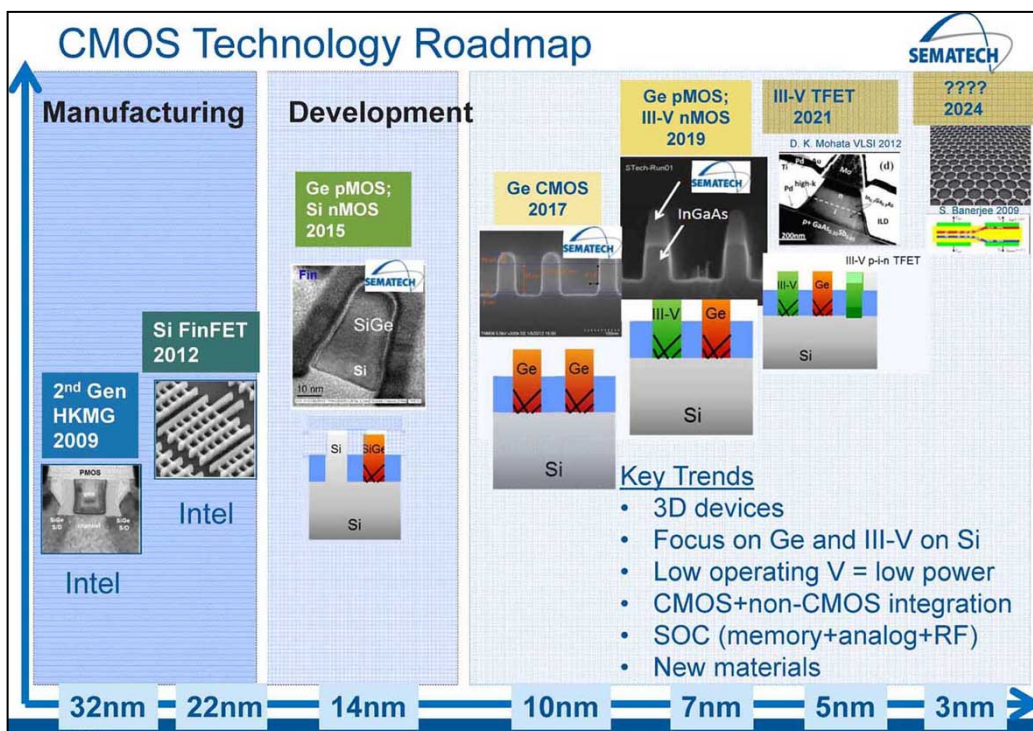


Fig. 51

CMOS works, there are a lot of excellent works that have been done by Prof. Toriumi and his team. We are hoping that the industry will actually introduce germanium CMOS within the next two years or so after a 3-dimensional device Fin-FET. Subsequent to that, the III-V device will come probably along with the germanium device. That will be another Fin-like device like III-V TFET. If we go beyond that, we believe that we have to have a new type of device like a quantum tunneling transistor or 2-dimensional graphene device.

A quite big change will be coming up in the next 10 or 15 years. This change has to be managed carefully because we need to understand exactly where the applications are and what the trends are. If we just take Fin-FETs, there are many different Fin structures that we can make at SEMATECH. Every option of structures has pros and cons, and it may not necessarily be the right structure for a particular device. In the case of nanowires, we can make stack nanowires and put all kinds of structures there. However, each structure has many issues. Thus, we will have advantages and disadvantages.

Even in memory technology, the memory has become 3-dimensional today, and Toshiba has pioneered the biggest memory. A three-dimension is a very important concept because the industry can scale at the small cost without scaling physical dimension by lithography for the first time. The small cost scaling is the direction the entire industry will be going in the near future.

The other important part is new materials. New materials are rapidly introduced into these technologies. However, I think there is a big gap. We do not have the right

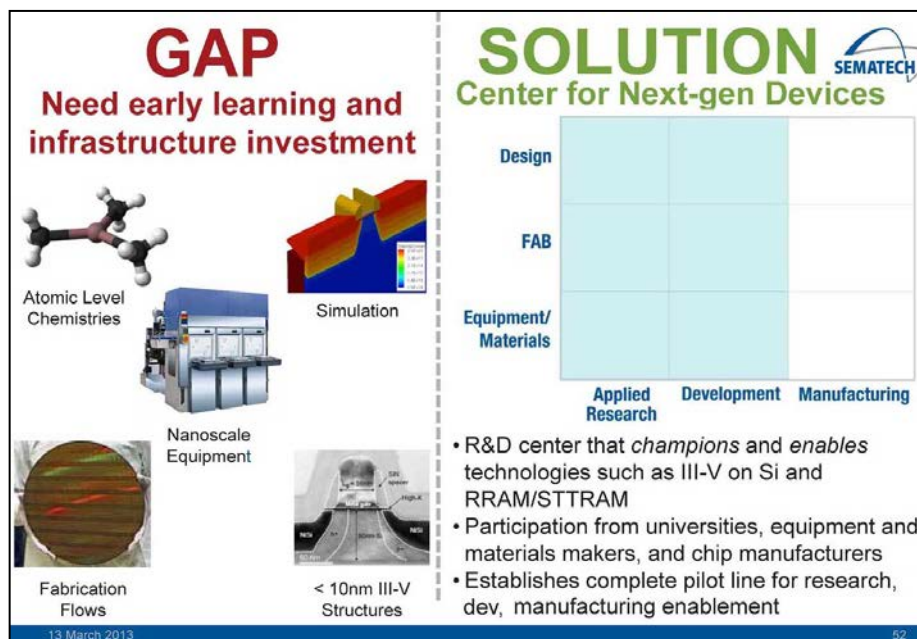



Fig. 52

Manufacturing Revolutions Needed



- **3D FinFETs, Ge/III-V FETs, low V_{dd} FETs**
 - Transition: Planar to non-planar device processing with non-Si materials
 - Challenges: Tools, heterogeneous integration, models, test methods, design
- **3D Flash memories, RRAM, STTRAM**
 - Transition: Planar to dense 3D memories with new materials
 - Challenges: Tools, unknown physics, test methods, models, reliability
- **Semiconductor world is 3D!**
 - Need new process technologies suitable for 3D manufacturing
 - Need new in-line metrology techniques for 3D devices
 - Selective processing (ALD, CVD, RIE, clean, CMP) techniques
 - New patterning techniques?
- **Materials...new materials...and more new materials – all on Si wafer**
 - Low thermal budget, low damage & local processing methods are needed
 - Cross contamination/interactions, ESH issues
 - Supply chain alignment
- **Cost of taking a technology from lab to fab is critical**


13 March 2013

Fig. 53

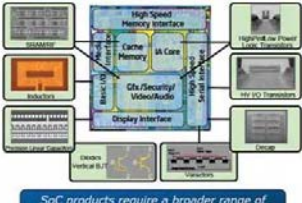
materials, and we do not know how to make these materials. All these materials have to be put on top of silicon at present (Fig. 53). We cannot use other material independently.

We have a center that has focused on all these areas of the next-generation devices (Fig. 52). Again, the challenge here is that a revolutionary manufacturing technology is necessary to make a new type of memory, a new type of Fin-FET, a nanowire FET, a III-V material FET, or a germanium FET (Fig. 53). We do not have the well-suited tools today. We need to bring many new technologies in ALD, CVD, and RIE, understanding

Technology Trends: New Drivers



System-on-Chip Building Blocks

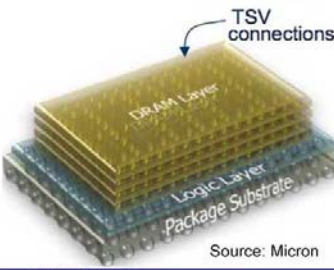


SoC products require a broader range of device types than mainstream CPU products

Source: Intel

System-on-a-Chip (SOC)

- Enables low power, low form factor solutions
- Minimal performance compromise
- Integrate MPU/GPU with analog, RF, NV memory
- High performance
- Cost to scale?



Source: Micron

System-in-a-Package (SiP)

- Enables low power, low form factor solutions
- Minimal performance compromise
- Integrate MPU/GPU with analog, RF, memory
- High bandwidth
- Cost effective to scale?

13 March 2013

Fig. 54

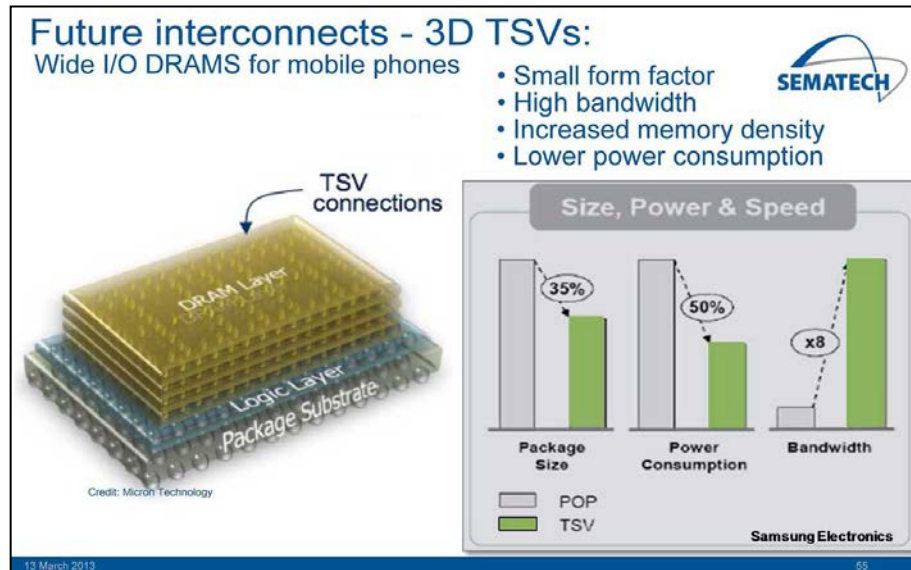


Fig. 55

the physics behind them. We do not have these technologies. Ideas are revolutionary, but we need to put resources to make the revolutionary manufacturing possible.

The last area of new technology trends is System-on-a-Chip (SOC) as shown in Fig. 54. The other important part is System-in-a-Package (SIP), where we are stacking memory and logic chips together. Stacking memory and logic chips enable high bandwidth (or high speed) and low power (Fig. 55). It is also a very cost-effective solution. In this technology, Samsung has been working very hard. They have shown that, if we stack the chips together, we can get a 35% improvement in package size and 50% improvement in power consumption. The memory bandwidth or speed goes up by 800%. It is a significant improvement in bandwidth, which is important for many systems today.

A lot of attention for 3D interconnection is received by the industry. We are working in this area as well, but there is also a big gap there because many things are immature in that area (Fig. 56).

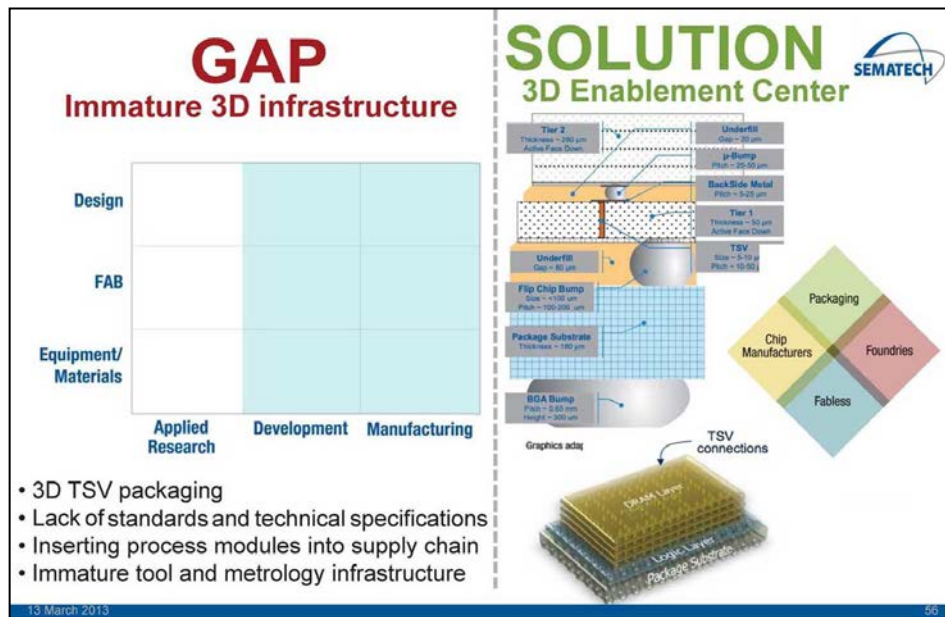


Fig. 56

Standards for 3D technology are very important (Fig. 57). We are trying to help all the companies that have an interest in this technology, and try to establish standards. Those who define the standards are the people who would also define the technology tomorrow. This is a very important activity.

Of course, all this leads to more heterogeneous integration systems as shown in Fig. 58 down the road, but I do not want to spend time on that. Again, here is the problem

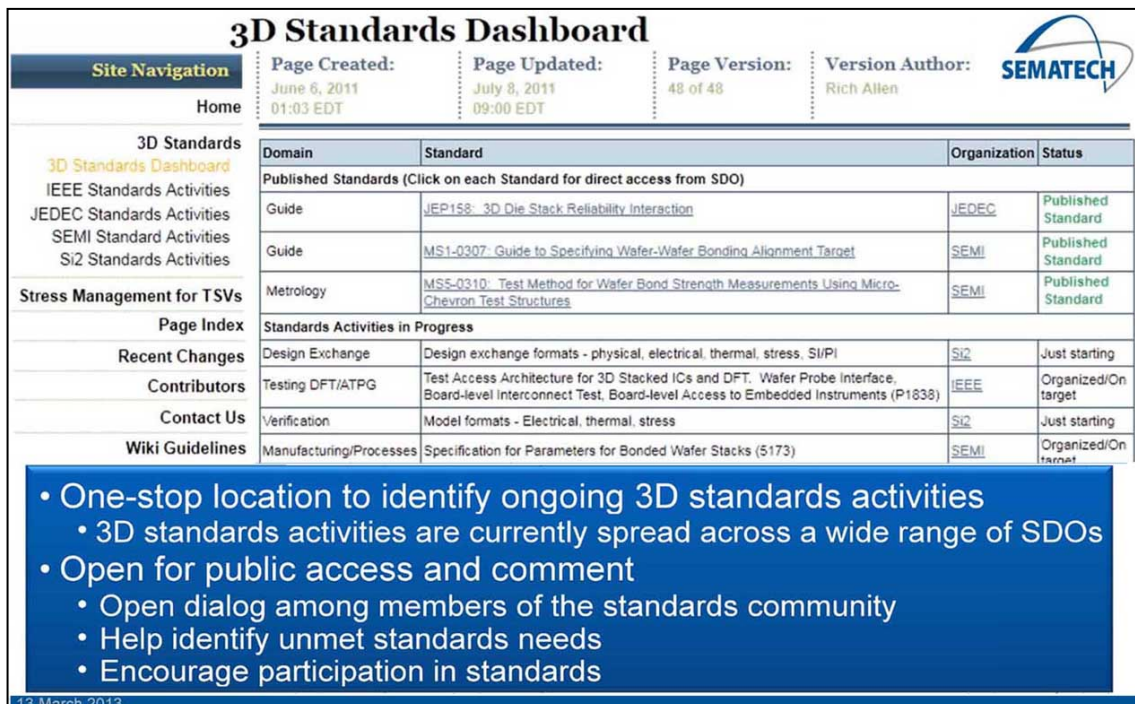


Fig. 57

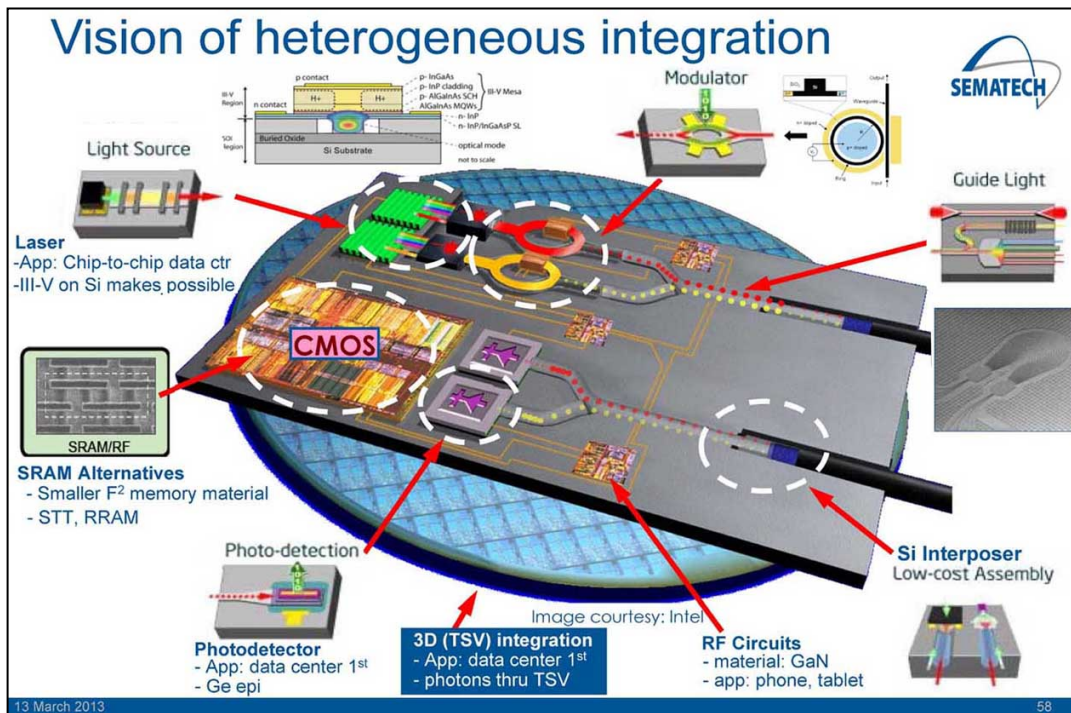


Fig. 58

(Fig. 59). We need revolutionary changes to make these technologies happen. A lot of researches are necessary in each of these areas for them to be successfully manufactured. We are not at the stage.

One new area that is also coming up quickly is the 10 nm size device (Fig. 60). The


Manufacturing Revolutions Needed

- **System on a Chip (SOC)**
 - Transition: Discrete memory/logic to integration of logic, memory, RF, analog...
 - Challenges: Restricted process /tool options, mixed materials on die, cost (yield)
- **3D TSV, reduced Cu/low-k levels, photonic interconnects/System in a Package (SIP)**
 - Transition: Planar ICs to ICs between chips; all electrical to electrical/optical
 - Challenges: Processes/materials/tools, standards, models, design, packaging, test
- **2.5D/3D interconnects are “equivalent scaling” solution**
 - For 3D IC – Thin wafer/die, thermal, stress and test are key issues
 - For 2.5D – cost/sq mm of interposer is critical metric
 - Many new materials need to be developed/engineered
- **BEOL fab process or Assembly/Test Packaging house?**
 - All process costs will need to come down for wider implementation
 - Need simple EDA tools for thermo-mechanical, signal integrity, 3D vs 2.5D, hot spot analysis and other options evaluation
 - Standards, interfaces and supply chain alignment
- **Cost is critical – early planning is a must**
 - SOC and SIP require early design-process-integration interlock

13 March 2013

Fig. 59

device that we make today is a 20 nm size. The problem is that defect detection is only possible for 20 or 30 nm at best. How do we find a defect smaller than 10 nm? We cannot see such a nano-defect that causes a heavy damage on the 10 nm size device. Thus, the economic model of the industry would fail if you do not know how to do that (Fig. 61).



E Nanodefacts

E

E P

T O Z

L P E D

P E C F D

E D F C Z P

F E L O P Z D

D E F P O T E C


L E F O D P C T

F D P L N C E O

- Device sizes are rapidly approaching 10nm and so are “killer” defects
- The defect sources are increasingly equipment sub-components and materials
- Finding those defects requires improved infrastructure for defect detection, root cause identification and solution verification





13 March 2013 60

Fig. 60



Nanodefacts

“Standard” o-ring “New” o-ring

Carbon

100nm

Silicon

20nm

Fails

Much worse

- Goal: No defects >10nm
- Standard approach identified deposition defects that were traced to vacuum system gate valve o-rings
 - Standard material sheds carbon defects >100nm
- Supplier “solution” increased the defect count with 20-40nm silicon nanoparticles
- Gaps:
 - Insufficient defect detection
 - Ability to link sub-component to new application conditions

13 March 2013

Fig. 61

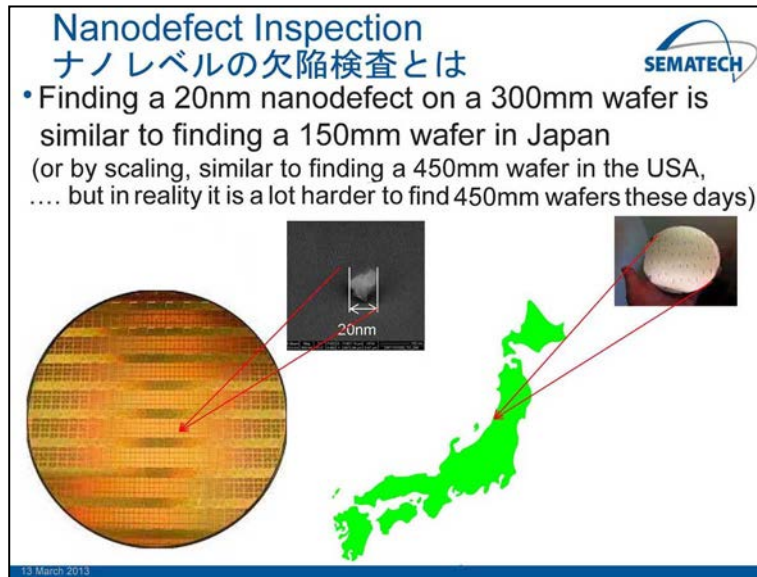


Fig. 62

If we want to find a 20 nm defect on a 300 mm wafer, it is like finding 150 mm wafer in the entire country of Japan (see Fig. 62). If we go into the space and then ask someone, “Tell me where the 150 mm wafer is kept in Japan,” it becomes extremely challenging. We need to do something in this area. One example of this is our vacuum chamber. We saw a lot of carbon-based 100 nm particles on the wafer when we were using a standard O-ring (Figs. 61 and 63). We went to the O-ring supplier and told them, “We have a problem. Can you fix it?” They said “Okay. No problem,” and came back to give us a new silicon O-ring. But we found that there were many 20-40 nm silicon

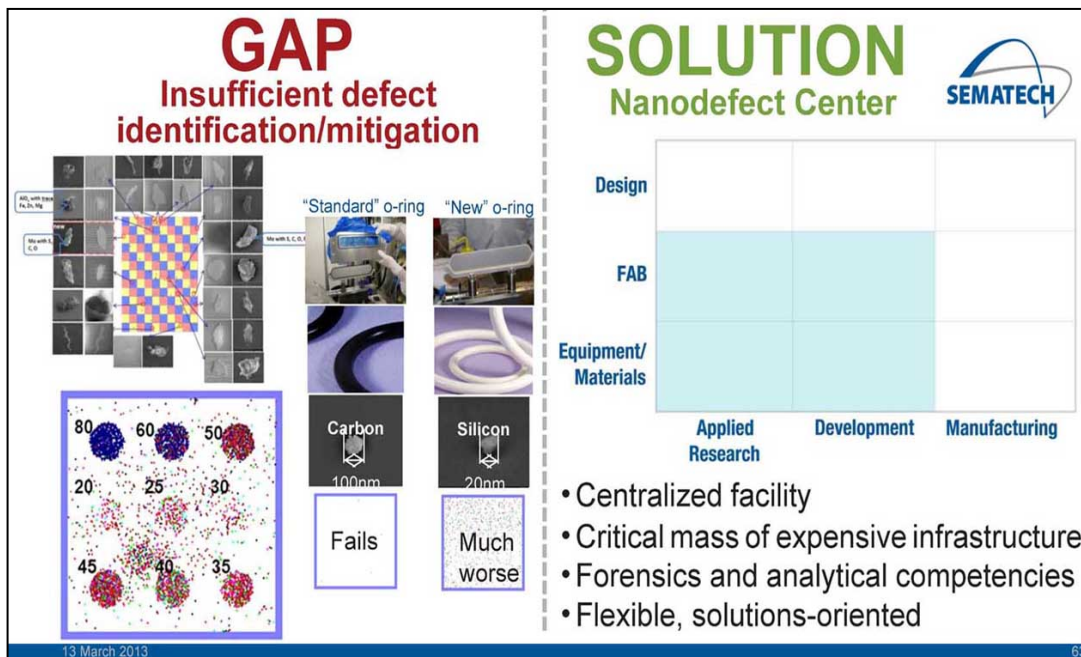


Fig. 63

Improving manufacturing productivity through SEMATECH ISMI



- Addressing the manufacturing needs and requirements of both leading-edge and mature/mainstream fabs, through tailored opportunities for benchmarking and shared learning
- Developing new environment, safety, and health technologies for resource conservation and manufacturing sustainability
- Coordinating with the industry to drive early standards, guidelines, and infrastructure for a cost-effective transition to the next wafer size



Councils and Forums



Mature Fabs



Manufacturing Capabilities



ESH Technology



Metrology Technology



450mm Transition

13 March 2013


Fig. 64

particles. 100 nm particles have gone but there are many 20 nm particles (Fig. 63).

A decrease of nano-defect is important. We need to understand how to fix this problem. The problem may not be the tool itself but may be in the subcomponents although we have not worried about this. If we make a 90 nm device, this may not matter that much. But this is a crucial issue when we start making 20 nm devices.

There are ESH (environment, safety, and health) implications (see Figs. 64 and 65) in manufacturing issues and metrology techniques. A whole range of issues is being

Environment, Safety and Health ESH Technology Center



- **Global Legislation and Regulatory Strategies**
 - Greenhouse gases / emissions estimation
 - Emerging chemical / material regulations
- **Resource Conservation Initiatives**
 - Fab/Tool energy use and analysis
 - Supplier interactions / roadmap development
- **Technology Assessment Initiatives**
 - New process materials evaluations and assessment
 - Nanomaterial exposure / Toxicity evaluation
 - Occupational health and safety





13 March 2013 65

Fig. 65

looked into on the manufacturing side.

One important thing at SEMATECH is the interaction between suppliers and integrated device manufacturers (IDM). It happens that one IDM interacts with many suppliers, and they communicate with each other (see Fig. 66). This is multiplied many times. Suppliers get different inputs from each of IDM. The inputs may be neither consistent nor standard because each IDM will have different priorities. There is only limited information shared among suppliers. This causes a lot of confusion in the industry. Suppliers cannot understand where they should invest for the future, if Intel, IBM and Samsung tell them different things.

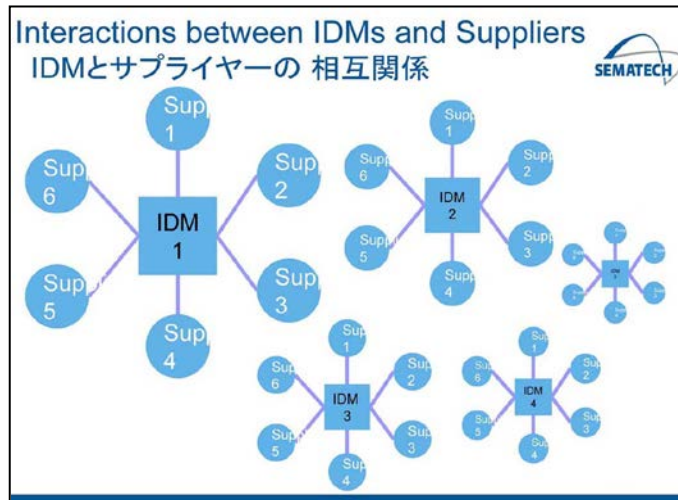


Fig. 66

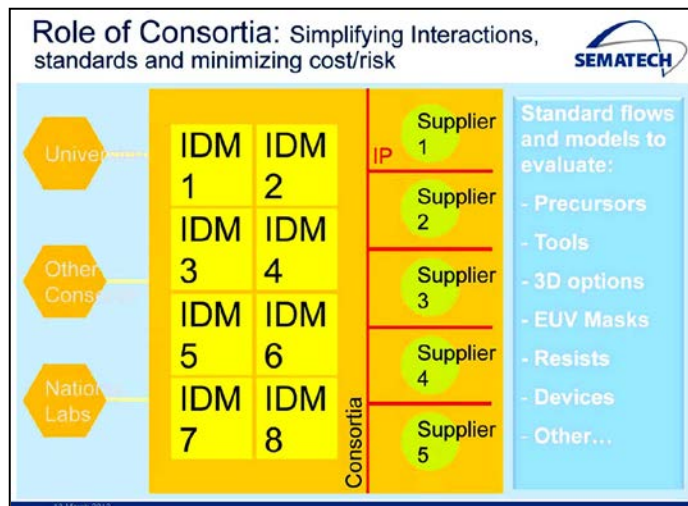


Fig. 67

The consortium-like model is very useful because all of them sit together and discuss about what a problem is and what will be needed (Fig. 67). If suppliers focus on the area of specialty, they will get a better answer. All of them can save money and everybody benefits on that.

If they need, they can bring it to universities or national labs to work with them. They can also bring it to other consortiums to collaborate. This is a model that is very efficient, and we have used this in many areas. I believe this kind of structure is absolutely needed in order to develop all the new technologies that I showed you. I want to emphasize that these consortiums are not limited to any specific country, specific region or specific industry. It is global. We have to work globally, and we are doing that in the semiconductor field.



Fig. 68


In the last few minutes, let me summarize the success factors of the consortium (Fig. 69). If you look at the consortium itself, the success factors are its industry-led model and the clear mission. What are we doing in the consortium? That is a very important factor. Another important factor is the leadership that comes from the industry. The industry should say, “I need this technology. I want to do this. It is the important problem to solve.” The industry should also recognize that it is not a tomorrow’s problem, but it has to be long-term. A tomorrow’s problem is the proprietary problem that they have to solve internally: product development is not a consortium activity but a confidential activity. Our task has to be done in a longer-range fashion. It is the way that we can save cost. It is also important to include the entire eco-system. It cannot be just for chipmakers nor equipment and material suppliers; it has to be a broad-based ecosystem-driven activity.

It should be noted we cannot always this consortium model to other industries. The industry has to be mature and has to have enough revenue to support the consortium. If the industry is very small for some new technology that might be coming up, it does not



Fig. 69

Summary - contd



- Trend of increasing R&D spending in the semiconductor industry is continuing R&D費用の急増
- Affordability of R&D spending in the semiconductor supply chain is becoming increasingly more difficult
装置・材料・部材メーカーのR&D負荷は適正範囲を超過
- Collaboration, particularly in partnerships for access to expensive facilities, is a critical tool for enabling affordable R&D
高価な施設を協業でアクセス可能にし、適正なR&D費実現
- Future device manufacturing requires a revolution in manufacturing tools and methods
- Success of SEMATECH's model is because
 - (i) it is industry driven (ii) it has evolved with industry
 - (iii) it has adapted to change and (iv) it is global

13 March 2013

Fig. 70

make sense to have a consortium.

I feel also that it is very beneficial to drive everybody to come together and form a consortium if there is a crisis in that industry; otherwise there is a less incentive for companies to decide that they sit together and work with other companies. A crisis is the necessary factor in some ways. It is also important for both government and industry funds to be working together.

Engagement of all the participating members is very important. They need to engage actively with the consortium because what they are doing is for the industry and for member companies. Another extremely crucial factor is agility. They should respond agilely to any changes that may be happening in the industry. If we start a project today, it may not make sense six months later. We should stop the project and look at the new activity that is necessary, rather than trying to continue the project with wasting our time and money.

Partnerships have to be global, and the business of \$300 billion is global. Without the global partnership, we cannot come across the right ideas. If partnerships are not global, you do not get the right material quality, the right equipment quality, and the latest technology that is necessary. Eventually, the customers are also global. We need to be able to provide solutions in a global fashion, and that is the reason why partnerships should be global.

Now, I want to extend the summary here (Fig. 70). I have shown that the cost of R&D and the affordability of R&D are going up dramatically. The collaboration is the only answer to that. In particular, a global collaboration enables affordable R&D so that they can continue to keep pace with the development cycle of the technology.

As I have shown, ideas of future device manufacturing are evolutionary, but the manufacturing solutions have to be revolutionary. It is a very challenging situation that the industry faces today. We have to have new tools and new methods. In fact, some physics of that is not understood. It is crucial for us to make the physics clear so that the revolution is going to take place. We cannot introduce all the changes at the same time, and they have to come in one by one.

If I look at SEMATECH itself, the next issue is why SEMATECH has been successful. One of the success factors is the industry-driven consortium; it has evolved with the industry. We tried to change the structure of SEMATECH when the industry changed. Thus, we also adapted to change. When we started, we were doing equipment analysis. Subsequent to that, we need to develop technologies such as low-k technology, copper technology, and high-k nanowire technology. When we were required to do something different, we went and did that. Very quickly, we became a global partnership consortium rather than focusing only on the United States businesses. This is another important factor that made it successful and worldwide adaptable.

I am going to stop my presentation with this summary. I want to thank you for your attention.



Fig. 71

コメント

鳥海 明（東京大学教授）

【司会者】 Thank you very much. 続きまして、鳥海先生からのコメントをお願いしたいと思います。

【鳥海】 東京大学の鳥海と申します。よろしくお願ひします。SEMATECH そのものへのコメントということではなく、SEMATECH を含めて、半導体の R&D 全般について、大学の立場と産業界の立場ということで、お話をさせていただきます。

半導体に携わったほとんどの方は、Fig. 72 に示した年表は良く知っていて、そうでない人はあまりご存じないと思います。先程の SEMATECH の創設が 1987 年というのは、この図にも書いてある通りです。それに先立ち、SIA (Semiconductor Industry Association) ができたのが 1977 年で、SRC (Semiconductor Research Corporation) が 1982 年に出来ています。日本では、成功したとの評価が高い「超 LSI 技術研究組合」が、1976 年から 1980 年まで実動しました。SIA による NTRS (National Technology Roadmap for Semiconductors) というロードマップが出て、その後、1998 に世界の同様な組織と共同で ITRS (International Technology Roadmap for Semiconductors) という国際ロードマップが出て、これが今も続いています。

1984 年に imec (the Interuniversity Microelectronics Centre) ができて、今も世界の最先端技術開発の中心の 1 つです。1985 年に始まった CIS (Center for Integrated Systems) というのはスタンフォード大学工学部にあつて、MTL (Microsystems Technology Laboratories) というのは MIT の School of Engineering にあります。私は、1989~1990 年に、MTL に行つており、ちょうど『メード・イン・アメリカ』という本が出た頃です。

日米関係で言えば、1986 年に半導体協定が結ばれて、私もその時には半導体メーカーに在籍していましたが、外国製の半導体を買うということになっていました。その後、SIRIJ (Semiconductor Industry Research Institute Japan)、つまり(社)半導体産業研究所ができ

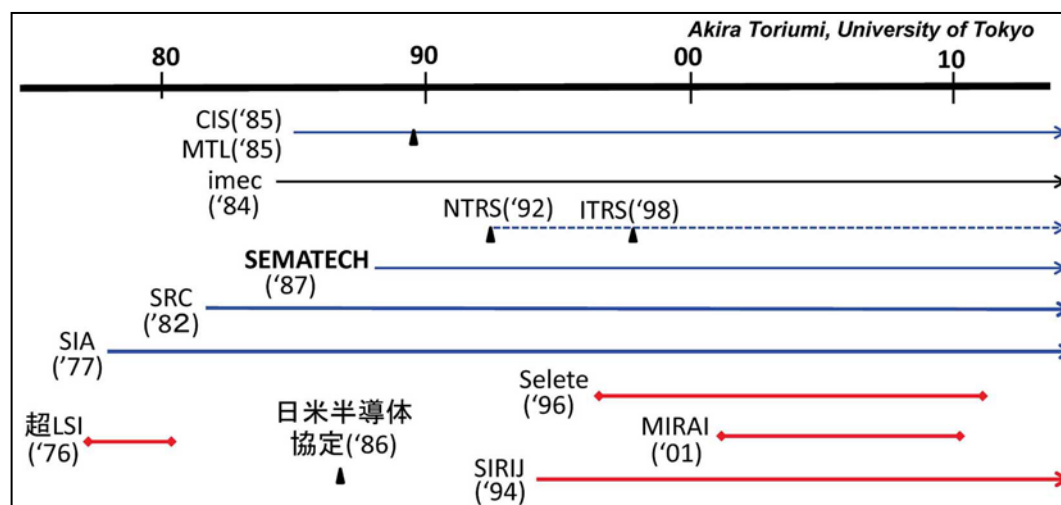


Fig. 72

ました。また、Selete (=株)半導体先端テクノロジーズ)や MIRAI (=次世代半導体材料・プロセス基盤プロジェクト)もできました。

ここで特徴的なのは、2点あると思います。よく言われるのは、「More than Moore」が叫ばれる一方で、半導体でもシリコンに関するプロジェクトがほとんど終わっているということです。SIRIJは続いてはいるのですが、ハード的なものは既に終わっています。そういう状況の中での SEMATECH であり、imec であるということです。

IEEE のデバイス関係の大きな国際学会 IEDM (International Electron Device Meeting) で、インテルからの招待講演者が「More than Moore」や「More Moore」を議論した時に、「インテルにはムーアが沢山(=more Moore)いる」と冗談をいっていました。確かに、インテルには創業者の Robert Noyce さんと Gordon Moore さんに始まって Andrew Grove に続きさらに多くの優秀な人がいるのは事実です。

SEMATECH や imec がどう意識しているかは別にして、私が感じるのは、SEMATECH は、最初は manufacturing technology というところから入って行って、imec は、例えばクリーニングテクノロジーといった、要素技術から入っています (Fig. 73)。imec の近くにはルーベン大学という大学がありますが、最初は大学ベースの非常にファンダメンタルなところから入ってきています。ところが、最近の imec の活動は、プロセスや要素技術だけでなく、manufacturing というところまで向かってきています (Fig. 73)。

SEMATECH の活動は、manufacturing だけではなく、process や device technology へと広がっています。これは、先ほど Jammy さんの話にあった通りです。Science や physics までには行かないけれども、knowledge という領域に入ってきているということです。

SEMATECH と imec の両者ともがフレキシブルに動いているということが特徴だと思います。私自身は、日本のプロジェクトの中の MIRAI というのに入っていました。開発を目的とするプロジェクトであって、機関ではないですから、5年なり10年で開発を終えると終了するプロジェクトです。私自身はメタルゲート high-k を研究していました。ところが、SEMATECH では、先ほどの

Jammy さんの話にもあったように、high-k の開発が終わった後には、また新しい開発へと展開しています。これと同じようなことは imec でもやっていて、要素技術の開発を終えれば、それを使ってデバイスをつくっています。

最後のどこで勝負するかというのは、SEMATECH も imec もそして我々もそう大きな違いはないと思います。大きく違うのは勝負

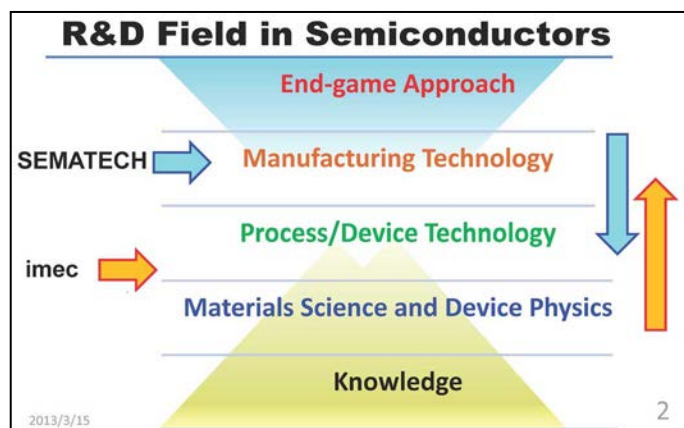


Fig. 73

の仕方であって、我々が単発であるのに対して、SEMATECH や imec では特定の技術やデバイスに拘らないフレキシビリティを持っていることだと思います。このフレキシビリティというのはとても大事で、お金を出している人がどれくらいの自由度を与えることができるかということにもなります。そのシステムの違いが大きいと考えています。

大学にいと、physics は要らないと言われても困るわけです。そこをやらないと大学にならないので、physics をやらざるを得ない。しかし、シリコンの研究を大学でやろうとすると、「シリコンは十分に研究したのもういいだろう。今更どうして？」と言われてしまいます。でも本当に十分に研究し尽くしたのかは誰にも分からない。基礎研究というのはいつもそういう言い方をして研究を続けますが、それでは説得力に欠けることも分かっています。シリコンは研究し尽くしたという言われ方をされますが、決してそうではないということを強く感じます。

誤解をしないで頂きたいのですが、Jammy さんの話にゲルマニウムだとか III-V 族の GaAs が出ていましたが、それはシリコンの延長線上にそういう材料があるということです。だからシリコンを含めてそういう材料も研究しないといけない。そういう研究が我が国では欠けていると感じます。

1982 年に設立された SRC (Semiconductor Research Corporation) の 30 周年のセレブレーションが最近ありました。その時の資料の 1 枚が Fig. 74 です。SRC が設立された 1982 年頃は、日本の半導体が世界を席卷していた時期です。アメリカの半導体メーカーは、マーケットシェアを落として、国の資金も出ず、シリコンの研究も下降線をたどる。そして学生も少なくなり、結果として、パイプラインのところで才能が枯渇するということが起きていました。この様な状況を克服するために SRC ができたわけです。今の日本を見みると、1982 年頃のアメリカに非常に近いのではないかと思います。

半導体の研究開発のアクティビティを示す時には、様々な示し方があります。例えば、

IEDM (IEEE International Electron Device Meeting) や ISSCC (International Solid-State Circuits Conference) の発表件数を示すのが一般的ですが、ここではあえて応用物理学会の発表件数を示しました(Fig. 75)。今、私が応用物理学会に関係していることもあってこれを持ってきました。興味深いのは、

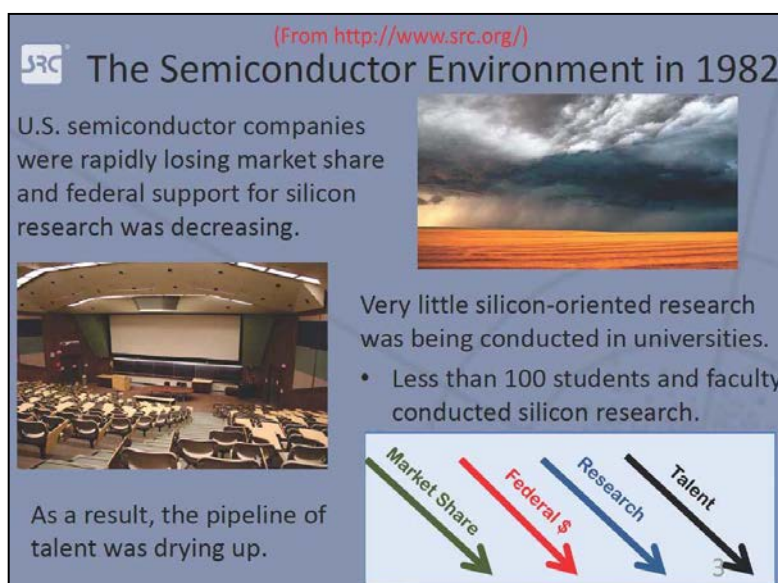


Fig. 74

産業界からの発表が、1993年をピークに落ち始めて、1997年には大学からの発表数と逆転しています。2010年には、産業界からの発表数はさらに落ちています。先ほど言った様にコンソーシアムが増えたので、2003年には官の発表数が少し増えています。しかし、産業界からの発表数の激減は続いています。

その理由については、様々なところで議論されています。学会発表を重視しなくなったとか、いろ

いろと議論されています。しかしそうではなくて、結局のところ、企業の研究開発のアクティビティの低下の実態を表しているのだらうと思います。

大学での研究は、何とか頑張っていますが、やはり低落傾向に入りつつあります。応用物理学会の中では、シリコンや半導体はもう大セッションではなくなっています。今は、有機材料やスピントロニクス関連の方が、発表件数として圧倒的に多くなっています。それが良いとか悪いとかということではなくて、こういう現実の中で、シリコン産業がほんとうにこのままで良いのだらうかということを感じます。

SEMATECH の様な研究開発組織が日本にとって良いのかどうか分かりませんが、会社に対して、利益の出ないだめなものを頑張れと言ってもしょうがないわけで、そこをどうするかというのが一番問われています。学生にすると、世界で負けているのに、どうしてそんなところに就職しないといけないのかという感じになります。半導体を研究していた学生も、半導体メーカーでないとどこに就職したいという希望を持つようになります。資金力も、瞬発力も、スピードもない企業では、研究はやらせてもらえない。そこをどう乗り越えるかというのが、我々の問題なののだらうと思います。

3月5日に広島大学でワークショップがあつて、これが結構充実していました(Fig. 76)。インテルでシニアフェローの Mark Bohr さんや絶縁膜関係で有名な T.P. Ma エール大学教授、スタンフォード大学の教授で配線や heterogeneous integration で有名な Krishna Saraswat 氏が講演をしました。このランチセッションのオーガナイズをやりましたが、これから先シリコンをどうしていくのかという話が出ていました。皆さんがやはり同様に悩んでいるわけです。

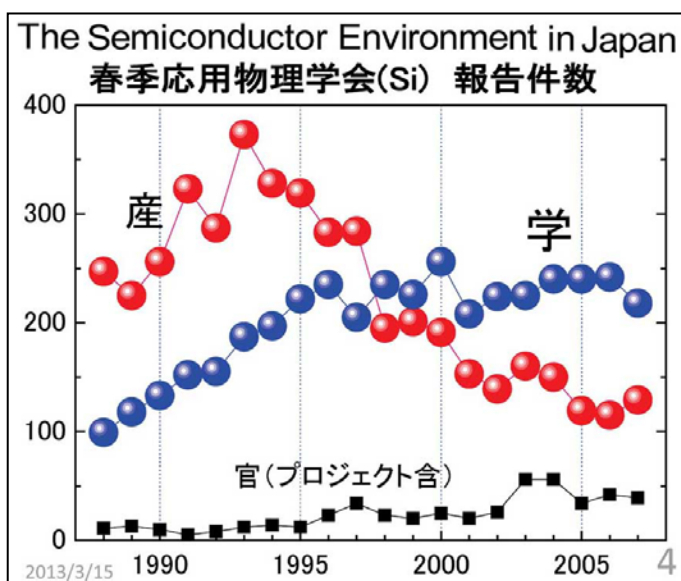


Fig. 75

現在も続いている典型例の1つに、スタンフォードの CIS があります。1985年のオリジナルスポンサーは、当時のそうそうたる会社の多くがスポンサーになっていました。今でもこれと同じくらいの数の会社がスポンサーになっています。インテル、IBM、テキサス・インスツルメントは、今でもサポートしている会社です。Saraswat 先生には、「スポンサーとパートナーとはどこが違うのか」という質問をしました。スポンサーとパートナーでは、金の出し方が違うのですかという質問です。Saraswat 先生によれば、最も大きな違いは、パートナーの場合は、スタンフォード大学と会社の1対1対応であり相互のリンクである、ということでした。

日本の大学を見ていると、スポンサーはあり得てもパートナーに相当するシステムはあまり存在しません。キャノン、NEC、ルネサス、東芝といった日本の大きな半導体メーカーが日本の大学をサポートしないで、何故スタンフォードには大金を払ってでも人を送り込むのだろうというのが私の素朴な疑問でした。そこで重要なことは、パートナーであるがゆえの human link と knowledge link だったのです。つまり、CIS の人だけではなく、様々な会社の人が来ている。そこから来るナレッジのリンクというのはとても大きいということです。もう一つはヒューマン・リンクです。つまり、例えば NEC から来た人の隣には IBM から来た人がいる。そういう人と人の繋がりができます。その繋がりが日本の大学には欠けています。そこが日本の大学とは違うところだと思います。

Jammy さんの講演でも SEMATECH はグローバルでインターナショナルだという話が出ていました。SEMATECH の本当の意味を理解すれば、私たちは何をしなければいけないのかを理解できると思います。

これは私の個人的な気持ちを述べた最後のスライドです(Fig. 77)。日本の役所や大学の偉い方は、imec 詣や SEMATECH 詣でがとても好きです。imec や SEMATECH を見てくると、何か研究開発の仕組みがわかったような気になります。しかし、そこを見ても本当の解は見えないです。私も、imec にも SEMATECH にも何回か行っていますし、技術としては参考になります。しかし、そこでなぜ上手くいっているのかということは、それだけでは見えてきません。先ほどの Jammy さんの話の中に出てきた様に、本当の意味や目的が

広島大学 ナノデバイス・バイオ融合科学研究所
国際ナノデバイステクノロジー ワークショップ 2013
 International Workshop on Nanodevice Technologies 2013

日時 平成25年3月5日(火)
 場所 広島大学 学生会館レセプションホール (東広島キャンパス)
 参加費 無料 (Webにて事前登録受付中)

プログラム

10:00-10:30 オープニング

10:30-11:15 基調講演 Tso-Ping Ma (エール大学 教授)
 「ナノデバイスプロセスの研究と教育」

11:15-12:00 基調講演 Krishna Saraswat (スタンフォード大学 教授)
 「集積回路デバイスプロセスの研究と教育」

12:00-14:00 昼食

14:00-14:45 基調講演 Mark Bohr (インテル シニアフェロー)
 「モビリティ時代のテクノロジー・シーキング」

14:45-15:15 招待講演 Donhee Ham (ハーバード大学 教授)
 「プラズマモニック回路とメタマテリアル」

15:15-15:45 招待講演 秀 道広 (広島大学 教授)
 「表面プラズモン共鳴を用いた生きている細胞の解析」

15:45-16:15 招待講演 池田 丈 (広島大学 助教)
 「シリコン積層タンパク質によるバイオエレクトロニクス」

16:30-17:30 総合討論
 「シリコン系デバイスプロセス研究の課題」
 オーガナイズ 島海 明 (東京大学 教授)
 パネリスト Tso-Ping Ma (エール大学 教授)
 Krishna Saraswat (スタンフォード大学 教授)
 Mark Bohr (インテル シニアフェロー)

17:30-18:30 ポスターセッション
 18:30-20:00 懇親会 (有料) ※講演は英語で行われます

主催 広島大学 ナノデバイス・バイオ融合科学研究所
 協賛 米国電気化学会 (ECS) 日本支部
 IEEE 固体電子回路協会 (SSOS) 日本支部
 IEEE 固体電子回路協会 (SSOS) 関西支部
 広島大学大学院理工学系 ナノデバイス・バイオ融合科学研究所
 中国材料学会 固体電子学分会 中国協会
 電子情報通信学会 中国支部、情報処理学会 中国支部、電子学会
 中国支部、国際電気伝導体工学センター (ITARC)、株式会社
 半導体工学研究センター (STARC)

参加登録 (無料、先着順、お席に限りがあります)
<http://www.RNBS.hiroshima-u.ac.jp/>

【問い合わせ先】
 広島大学ナノデバイス・バイオ融合科学研究所
 国際ナノデバイステクノロジー ワークショップ 事務局
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 電話: 082-424-3265
 Web: <http://www.RNBS.hiroshima-u.ac.jp/nwt2013.html>

Fig. 76

どこにあるかということ、私たちはあまり見ていないからです。Jammy さんのお話に出てきた以外にも、様々な意図があるのだと思います。

ルーベンの田舎町に imec をつくってどうして成功できると考えたのか。ニューヨーク

州の州都と言っても田舎町に過ぎないオールバニにどうして SEMATECH をつくったのか。単純に科学技術の話だけではなく、雇用や税金の問題など、様々な要因が複合していると思います。私は技術の側からしか見ていませんが、そういう様々な要因を理解して次のステップに行かないといけないと思います。

私は、日本がもう一度出直すためには、個人的には、鎖国か完全グローバル化かのどちらかの極端なことをやる必要があると思っています。鎖国というのは現実的ではありませんが、何とかの開発のためのプロジェクトという様な中途半端なコンソーシアムをつくらないで、その中では英語を公用語とするセンターをつくって、海外から人を呼び込む完全グローバル化が必要だろうと思います。

別に産学連携に拘る必要はありませんが、Jammy さんが仰ったように、リーダーはインダストリーから出ることが望ましいと思います。その方が industry-driven の serendipity が発揮できると思うからです。次世代の産業のタネを探す努力をしないと、日本でうまくいくモデルはできないというのが、私自身が SEMATECH から学んだことです。また、imec の人とお話をして、技術がすごいという思いもありますけど、それ以上に、その進め方に大きな違いがあるという感じを私自身は強く持っています。

そういうことで、私のコメントにかえさせていただきたいと思います。

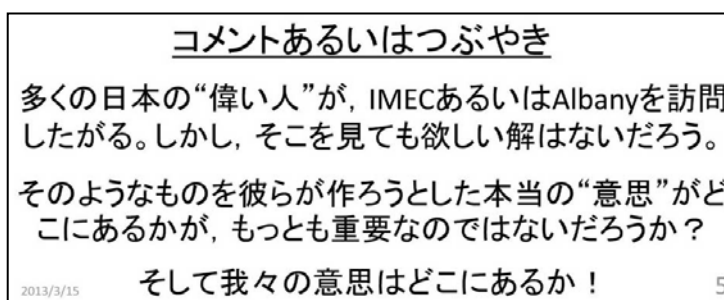


Fig. 77

質 疑 応 答

【司会者】 どうもありがとうございました。これから質疑応答に移りたいと思います。講演録作成のために録音はさせて頂いておりますが、講演録自体には個人名は記載されませんので、どうぞご安心してご質問、ご討議をお願いいたします。ご討議は英語でも日本語でも構いません。最初に、所属、ご氏名をおっしゃってからご質問をお願いいたします。ご質問、討論のある方、どうぞ挙手をお願いします。日本語でも構いませんので。

【司会者】 直ぐにはご質問が出ないようですので、私から少し口火を切らせて頂きます。実は、私は電機メーカーから出向していて、入社当時はシリコンの量子細線の研究をしていました。それは、会社が半導体デバイスを作っていたからできていた研究ですが、その生産がルネサスエレクトロニクス（当時はルネサステクノロジー）やエルピーダメモリへ移ってしまうと、半導体の研究、特にシリコンの研究は、社内的に難しくなりました。そういうことを考えると、企業からの発表が非常に少なくなってきた時期というのは、私の経験ともよく非常に一致しています。

ということで、ご質問をお受けしますのでよろしくをお願いします。英語でも日本語でも構いませんので挙手をお願いします。

【質問者 1】 SEMATECH には企業が多く入っているということですが、知財関係、特に特許の管理はどのように行っておられるのでしょうか。

【Jammy】 It is a very good question. The core member companies of SEMATECH are chip-making companies, and they all share the patents. Everybody gets license to the patents. When we work with equipment suppliers or material suppliers, the patents are only shared between SEMATECH and that company. The core members also get a license to that because they have to give the license anyway when the equipment manufacturers sell the tool to the chip-makers. It is very easy for them to share that effort.

【司会者】 他にご質問、お聞きになりたいことがあれば、どうぞ遠慮なく。コメントについてもよろしくお願いします。

【質問者 2】 鳥海先生の最後の「コメントあるいはつぶやき」のところで、実際自分も同じようなことを言われて、非常に寂しいと言われてきたことを覚えています。当事者として、耳が痛いところです。文部科学省の立場として、今何をしないといけないのかを考えていて、もし、鳥海先生にもう少し具体的なご提案があるようであればアドバイスをお願いしたいと思います。文部科学省としてやれること、あるいはやるべきことが多々あると思いますので、そういった観点でアドバイスを頂ければと思います。

【鳥海】 大きいことや小さいこと、いろいろありますが、わかりやすい言い方をすると、

TIA-nano (つくばイノベーションアリーナ・ナノテクノロジー拠点) には、私も少しは関わっていますが、どこが責任を持ってどう成功させるかということはありません。大学、産総研、NIMS という素晴らしいところがあって、それで上手くいかなかったら、他にそういうことができることはありません。話としては良いのですが、現実的に動くときの施策がとても弱いと思います。人を増やさないと動かないし、研究者一人で何もかもやれというのは無理です。一方で、産総研、NIMS は、別の問題を抱えていると思います。大学の立場から言うと、日本でも上手い仕組みができないかと思っています。これが1点です。

先程、最後に申し上げた、鎖国か完全グローバル化ということですが。シリコンに関して、完全グローバル化のセンターをどこかにつくるという夢は、私はまだ捨て切れていません。技術を外に出さない訳ではないので、完全鎖国でも構わないですが、これからは多分難しいと思います。もう完璧に、国境をなくした完全なグローバル化が必要です。

TIA のような組織をうまく成功させないといけないのですが、皆で潰しているように見えないでもない訳です。細かいことは他にもあるのですが、大きなところではそういうことです。

【司会者】 今のお答えに関連しての質問ですが、逆に、なぜ「超 LSI 技術研究組合」が上手くいったのでしょうか？おそらく SEMATECH が発足した本当の理由は超 LSI 技術研究組合の成功に刺激されたからだろうと思っています。

【鳥海】 私は 83 年に入社した時には、超 LSI 技術研究組合は終わっていて、本当のところはよく分からないのですが、上司や先輩によると、「追いつけ」というところが大きかったようです。それと、装置というところに特化したところも大きかったと思います。

【司会者】 「追いつけ」というところが大きかったのでしょうか。

【鳥海】 そう言われています。但し、それだけではないと思います。あれだけの会社が集まって、しかも身銭を切るというところがないとなかなか成功しません。私の上司は超 LSI 技術研究組合で電子線露光をやっていましたが、そういう技術がその後の日本に繋がっています。そういう意味でも、全体の士気が高かったと言えます。

逆に、私たちが関わった MIRAI プロジェクトや Selete は、世間では負けプロジェクトのように言われています。私は、決してそうではないと思っていますが。ターゲットを絞ったプロジェクトは、そのターゲットだけを成功させるという硬直化の弊害が大きいと思います。先程の Jammy さんの話にもあったように、やり始めた後のフレキシビリティが重要だと思います。そのフレキシビリティあつてかつ完全グローバル化をすれば、良い形でアジアでの拠点ができるのではないかと思います。

【司会者】 ありがとうございます。他にご質問のある方、挙手をお願いいたします。

【質問者 3】 I do not come from the semiconductor industry, but my question may be

very general. In the last section, you mentioned that the leadership from the industry was a key for the success. Could you tell me the actual example of how the industry shows the leadership for success? Toriumi-sensei has mentioned that the flexibility of the project is a key for the success. Could you explain keys for the success again?

【Jammy】 Thank you for very good questions. In terms of the leadership, I can take EUV (extreme ultraviolet) lithography technology. Lithography is a key step that we have to do for patterning silicon wafers. We use it now, but many companies did not know whether EUV was going to be successful or not. What I really appreciate is that some companies in our consortium have focused intensively on it. They knew that it might not be successful and that it might not go into commercial production. At the same time, however, they had to make sure that it would work or not.

One of the large contributions that the consortium can make is to find out what does not work. You do not always get a final solution. For every final solution, there may be 10 solutions that do not work. If all those 10 solutions are pursued by everybody, they will waste a lot of money. So, that is a very important contribution.

The industrial companies, such as Intel, IBM and others, are showing a lot of leadership at SEMATECH. They are really focusing resources. They are putting people into SEMATECH and trying to push the technology forward. Because they want to know if a new technology is going to work or not, that kind of engagement is necessary. It is the leadership that I mean. Same thing happened when we did high-k metal gate. A similar technological leadership was there even when we were trying to do some of the work on Fin-FETs. There were a lot of direct connections and interactions with their leading internal researchers who do the work.

Does it answer your question about the leadership?

【質問者 3】 Yes, thank you. You seem to take a risk to identify the very aggressive area.

【Jammy】 Right. High risk, high reward. When I say leadership in consortia, it does not mean that the consortium is very successful. We want them to sit at a table and discuss the problems; for instance, “I would like to have a 250 ml bottle. I would like to make the shape of the bottle like this because I want to pack the bottle in this fashion and because customers can hold it easily.” That kind of engagement is important. It is the leadership that I was talking about.

Your second question is about flexibility. In terms of flexibility, I think it is what Toriumi-sensei has referred to. Imagine that we are making a bottle. We may find that another company has actually invented the same bottle, or market wants the smaller bottle than that we are going to make. In that case, we should be flexible to change the plan to meet market needs. We have to do that quickly. We cannot wait, and should say,

“I started this design, but I stop it immediately.” Thus, we would wrack this project and start another project. If it is too late, the market has already gone. That flexibility is necessary for us to be in line with the market needs.

In the case of SEMATECH, we started working on equipment evaluation in order to improve the equipment quality. That was our first focus in 1987. Around 1995, the whole focus of SEMATECH changed into the development of process technology such as low-k material, copper technology, and even some SOI-based substrate development. These were all given to SEMATECH, and we had to have such flexibility. Around 2000, It became clear that we needed to focus on the high-value added technologies such as high-k metal gate and silicon nitride. Many new processes that have been used in the industry were developed at SEMATECH.

As the industry changed, we also changed. Our projects changed, and even the composition of the membership also changed. Only chip-makers were members initially, but now, we include equipment makers as members. We changed the structure so that we can share intellectual property that you were asking before. We are very careful to include their intellectual property.

We have also brought in fabless companies as members. We are right now bringing component makers too. We have many companies sit at the table for discussion. In fact, it is also very important.

【質問者 4】 A business is the annual process through the market. How do you choose the next research area?

【Jammy】 The input of the next research area comes from our members. We meet with members three times a year at the technical level, at the strategic level and at the executive board level. All of actions get done there. The financial details are discussed at the executive board level.

At the same time, our team at SEMATECH goes out and talks not only to many intelligent faculty members but also to many people in the industry who are making equipments. We are making an idea as follows: “I think we need to do this, or we need to develop this. This is going to be a problem in five years from now. If we want to fix this problem within five years, what do we need to do now? How do we set up a plan?” That is the thinking we do. Then, we go to our member companies and show our results to them. We tell them why we need to do the project. In many cases, our members say, “That is good, but it is not necessary to do the project now. We can wait for the university to finish it.” In that case, we start the project at a low level. If we do not do that, we are not ready when the industry needs it. Thus, we have to think very carefully.

We work with the industry to make sure that we are doing what the industry wants, but we also have to apply our own judgment as a consortium to do the right thing so that we are able to use the technology whenever it is necessary.

【質問者 4】 Thank you so much.

【Jammy】 You are welcome.

【司会者】 他にご質問があれば、お受けします。

【質問者 5】 Thank you very much for your impressive presentation. If my understanding is correct, most of your presentation is about “More Moore,” and you mentioned “Beyond CMOS” a little. I am very interested in the future plan or strategy for “More than Moore” such as bio-electronics for instance. How does SEMATECH have the activity in that direction?

【Jammy】 That is also a very good question. Thank you. I did not tell you everything because I had only one hour. I think we have activities in “More than Moore.” As shown in Fig. 12, I do not believe that there is a barrier between “More Moore” and “More than Moore.” I thought before that there was a certain barrier between them. I think now that the barrier is pointless. Some of “More than Moore” technologies have been developed at SEMATECH. Thus, we have activities.

About five years ago, we started the technology development in one of these areas. We call it an emerging technology. Our idea is how we shape the technology. For example, MEMS (Micro-Electro-Mechanical-System) is one of these technologies. However, we are not interested in MEMS because everybody is doing that. We focus on nanoscale electromechanical switches and their systems. How can we put the nanoscale system on a CMOS? Is there a benefit if we do that? Is there a potential advantage? Is there a performance improvement? Are there new applications that can become available? Which industry is going to be a customer? Is it really plausible or not? Those are questions that we ask.

There was a question on gallium nitride, “How can we make use of materials like gallium nitride?” Of course, the industry is now using gallium nitride. What should SEMATECH do? Why does SEMATECH waste time and money for gallium nitride? At that point, it became obvious to us that doing gallium nitride is not good. However, we introduced gallium nitride on the large-scale silicon device. It is quite useful if we can put gallium nitride devices in CMOS-controlled circuitry at the same time. We can make power devices, laser, and other photonic devices. We can do different things with similar ideas.

Thus, we have many “More than Moore” technologies at SEMATECH. We are very

cautious in how we approach those technologies because the member companies who pay our bills today are strongly silicon-driven companies. If I give them an impression that I am doing something completely new, the immediate reaction would be “Why?” It is a very natural reaction, but they soon recognize it to be important. They came back and said, “You are correct. You are doing the right thing.” In any case, we have to be able to justify what we are doing. “Do we have a real advantage?” It is a long answer for a short question.

【質問者 5】 Thank you very much.

【司会者】 時間が来たようですので、所内講演会はここで一旦クローズさせて頂きたいと思います。この後 20 分ほど、名刺交換と個人的なご質問のために時間をとっておりますので、もしご質問のある方はその時にご質問をお願いします。

最後に、講演して頂いた Jammy さんとコメントを頂いた鳥海先生に拍手でお礼を申し上げます。（拍手）

— 了 —