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DESIGN OF NEW HIGH SPEED MULTI OUTPUT CARRY LOOK-AHEAD ADDERS

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Abstract

The carry look-ahead adders are designed till now by using standard 4 bit Manchester carry chain. Due to its limited carry chain length, the carries of the adders are computed using 4 bit carry chain. This leads to slow down the operation. A high speed 8 bit (MCC) adder in multi output domino CMOS logic is designed in this thesis. Due to its limited carry chain length this high speed MCC uses 2 separate 4-bit MCC. The 2 MCC namely odd carry chain and even carry chain are computed in parallel to increase the speed of the operation. This technique has been applied for the design of 8 bit adders in multi output domino logic and the simulation results are verified. Results prove that 8 bit MCC produces less delay compared to conventional 4 bit delay. The reduced delay realizes better speed compared to the conventional designs. The existing design and the previous designs are designed and simulated using Mentor Graphics. The delay of these designs is compared with 8 bit input and with 50 nm technology file. Implementation results reveal that the high speed comparator has delay of 37.47% less compared to the conventional designs used for comparison when operated at 50 MHz.

Keywords*:* delay; speed; carrier chain length

1. INTRODUCTION

Addition is the most commonly used arithmetic operation and also the speed limiting element to make faster VLSI processors. As the demand of higher performance grows, there is continuing need to improve the performance of arithmetic units and to increase their functionality. High speed adder architectures include the carry look ahead adders, carry skip adders, carry select adders, conditional sum adders, and combination of these structures. High speed adders based on the CLA principle remain dominant, since the carry delay can be improved by calculating each stage in parallel. The CLA algorithm was first introduced by Weinberger and several variants have been developed.

2. OBJECTIVE OF THE WORK

To design a high speed and efficient 8 Bit Manchester Carry Chain Adders suitable for VLSI processor applications.

To increase the speed of the operation by operation the carry chain by using two independent carry chain in parallel and thus reduces the delay of the operation.

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2.1 High Speed Multi Output 8 Bit MCC Domino Logic

Domino logic to implement carry propagate and carry generate signal in carry look ahead adders was proposed by Uyemura [6]. The high speed adder architecture includes the carry look ahead adders, carry skip adders, carry select adders and combination of these blocks. The Manchester carry chain is the most common domino CLA adder architecture with the regular, fast and simple structure adequate for in VLSI. The recursive properties of the carries in MCC have enabled the development of multi output domino gates, which have shown area-speed improvements with respect to single-output gates. The carry look ahead block mainly consists of carry implementation propagate and carry generate signal blocks.

2.2 Generate Signal Implemented in Domino Logic

The generate signal implemented in domino logic is shown in Figure 1. It consists of two inputs namely a_i and b_i and has one output g_i. The two inputs are connected in series thus perform AND operation. The operation of the circuit is controlled by clock signal. The circuit will possesses generally two state precharge state and evaluation state. If the clock signal goes to value '0', then the circuit will enter into precharge state and pmos will get connected to ground and output will maintain the value of 0. If the clock makes the transition from 0 to 1 then the circuit will enter into evaluation state and the output depends on the input value. Since generate signal possess AND operation if both input are maintained at 1, 1 then the output g_i will be maintained at 1 else the output value will be maintained at 0 i.e g_i=0

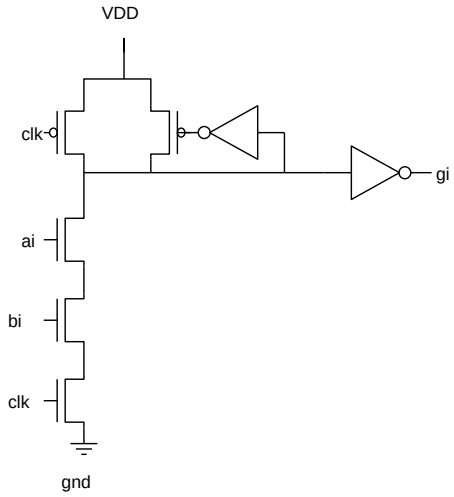

Figure: 1 Schematic Diagram of Generate Signal Implemented in Domino Logic

2.3 Propagate (XOR) Signal

The propagate signal implemented in domino logic is shown in Figure 2. Here the propagate signal is implemented in XOR operation. The propagate circuit is controlled by clock signal. If clk goes to '0', then the circuit will enter into precharge state and the output remains in 0 value. If clk value is 1, then the output value depends on input value. Since this propagate signal is XOR operation based if both the inputs are different then output pi will maintain the value 1 else pi will have value 0**.**

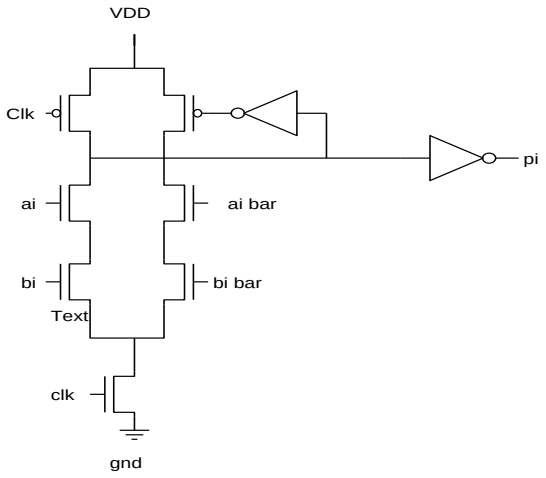

Figure: 2 Schematic Diagram of Propagate XOR Signal

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2.4 Propagate (OR) Signal

The propagate signal implemented in domino logic is shown in Figure 3. It consists of two inputs a_i and b_i and consists of one output signal t_i. Here the propagate signal is implemented in OR operation. The propagate circuit is controlled by clock signal. If clk goes to '0', then the circuit will enter into precharge state and the output remains in 0 value. If clk value is 1, then the output value depends on input value. Since this propagate signal is OR operation based if any one of the inputs is 1, then output pi will maintain the value 1 else pi will have value 0.

3. CONVENTIONAL 4 BIT MCC

In the conventional 4 bit MCC the CLA length is limited to 4 in order to cut down of number of series-connected transistors. Figure 3 shows the conventional implementation of the 4 bit carry chain using multi output domino CMOS logic. Let A = a_{n-1} a_{n-2} ……. a_1 a_0 and B = b_{n-2} b_{n-1} b_1 b_0 represent two

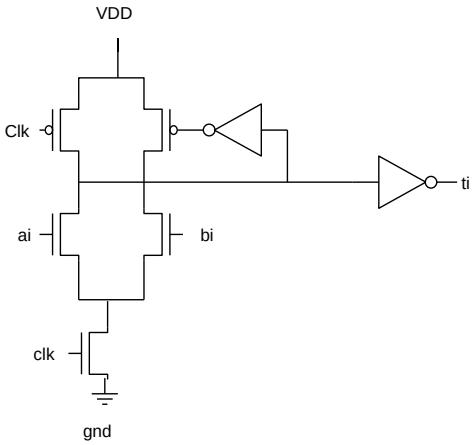

Figure: 3 Schematic Diagram of Propagate OR Signal Implemented in Domino Logic

binary numbers to be added and S = s_{n-2} s_{n-1} …… s_1,s_0 be their sum. In binary addition, the computation of the carry signal is based on the following equations

$$C_i = g_i + z_i \,.\, c_{i-1}$$

Where, $g_i = a_i \,.\, b_i$ Z_i are carry generate and carry propagate terms.

For the case of adders it is given by

$$Z_i = a_i + b_i$$

And the sum bits of adders are defined as

$$S_i = p_i \text{ exclusive } c_{i-1}$$

This conventional circuit consists of 4 bit two inputs namely p_0, p_1, p_2, p_3 and g_0, g_1, g_2, g_3. The operation of the circuit is controlled by clock signal. The input values are get from pi and gi values of the domino propagate and generate output values. If clock equals to '0', the circuit will enter into precharge state and no output will be obtained. If clock value is '1', then the output will depend on the input values. The inputs of propagate and generate signals from pi and gi will possesses and the corresponding output carry signals namely c_0, c_1, c_2, c_3. The circuit of conventional 4 bit MCC implemented in domino is shown in Figure 4.

4. A HIGH SPEED 8 BIT MCC MULTI OUTPUT DOMINO LOGIC

MCC adders can be efficiently be designed in CMOS logic. Due to technological constrains, the length of their carry chains is limited to 4 bits. However, these 4 bit adder blocks are used extensively in the design of wider adders. In the following, the design of an 8 bit adder module which is composed of two independent carry chains. These chains have the same length as the 4 bit MCC adders. The use of the 8 bit adder as a basic block, instead of 4 bit MCC adder, can lead to high speed adder implementations.

The derived here carry equations are similar to those for Ling carries equation. The derived carry equations allow the even carries to be computed separately of the odd ones. This separation allows the implementation of the carries by two independent 4 bit carry chains; one chain computes the even carries, while the other chain computes the odd carries.

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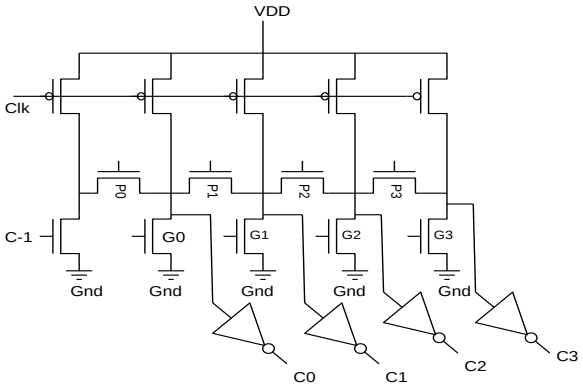

Figure: 4 Schematic Diagram of Conventional 4 bit MCC

4.1 Even Carry Computation

This carry chain gets computed when input value has even values. Say i= 0,2,4,6. For the even input values say p_0, p_2, p_4, p_6 and g_0, g_2, g_4, g_6 the corresponding intermediate even carries say h_0, h_2, h_4, h_6 is obtained. The input values of propagate and generate signals are obtained from p_i and g_i respectively.

The even carries can be analytically given by

$$H_2 = g_2 + p_2g_0$$

$$H_4 = g_4 + p_4g_2 + p_4p_2g_0$$

$$H_6 = g_6 + p_6g_4 + p_6p_4g_2 + p_6p_4p_2g_0.$$

The circuit of even carry computation is shown in Figure 5

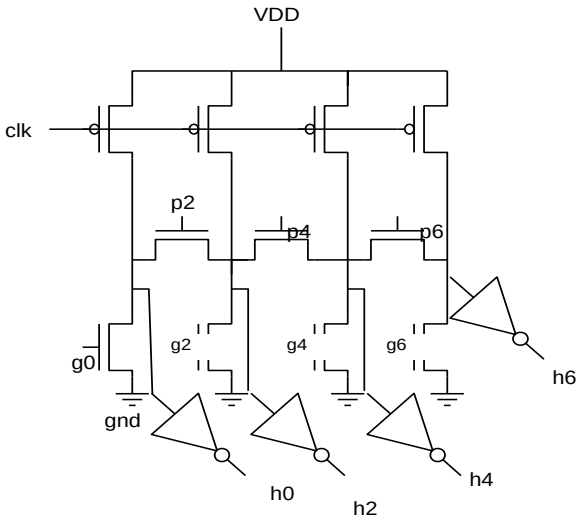

Figure: 5 Schematic Diagram of Even Carry Chain

4.2 Odd Carry Computation

This carry chain gets computed when input value has odd values. Say i= 1,3,5,7. For the odd input values say p_1, p_3, p_5, p_7 and g_1, g_3, g_5, g_7 the corresponding intermediate odd carries say h_1, h_3, h_5, h_7 is obtained. The input values of propagate and generate signals are obtained from p_i and g_i respectively.

The odd carries can be analytically given by

$$H_1 = g_1 + p_i \,.\, c_{i-1}$$

$$H_3 = g_3 + p_3g_1 + p_3p_1c_{-1}$$

$$H_5 = g_5 + p_5g_3 + p_5p_3g_1 + p_5p_3p_1g_0.$$

$$H_7 = g_7 + p_7g_5 + p_7p_5g_3 + p_7p_5p_3g_1 + p_7p_5p_3p_1c_{-1.}$$

The circuit of even carry computation is shown in Figure 6

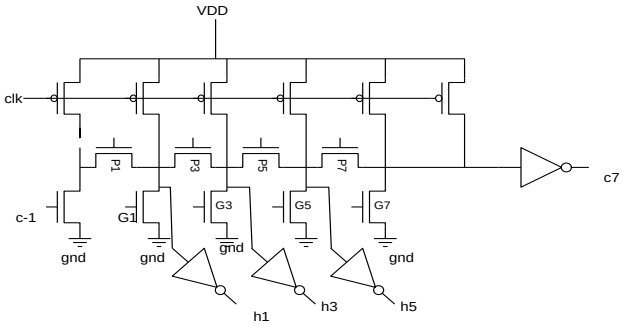

Figure: 6 Schematic Diagram of Odd Carry Chain

4.3 Domino Logic Implementation of Carry Signals

The domino logic circuit implementation for carry signals consists of two signals namely carry generate signal and carry propagate signals respectively. The implementation of generate and propagate signals using domino logic is shown in Figure 7.

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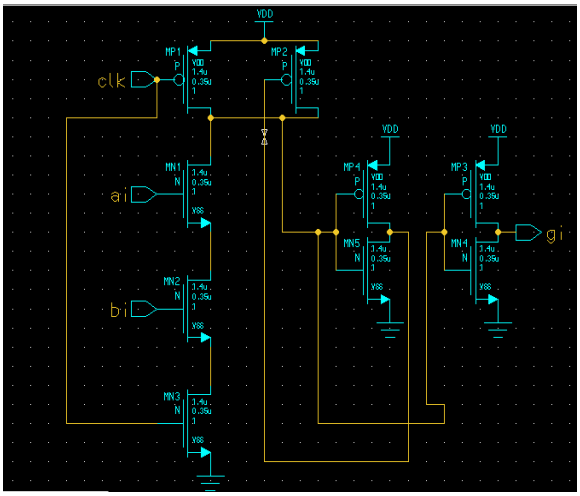

Figure: 7 Circuit of Domino Generate Signal

5. CONCLUSION

A high speed and an efficient 8 bit Manchester Carry Chain implemented in domino CMOS logic is suitable for Carry Look-Ahead Adders in processor applications is discussed in this project. This circuit is designed and simulated using MENTOR-GRAPHICS software. This design realizes better improvement in reducing the delay by introducing parallelism concept in carry chains. As a result, the 2 separate carry chains namely odd carry chain and even carry chain work in parallel thus increases speed of operation by reducing the delay considerably compared with 4 bit MCC. Hence this 8 bit carry chain is more efficient and can operate at low supply voltages with high speed, thus making this carry chain suitable for most of the high speed processor applications. This high speed Manchester Carry Cain is found to have a delay of 37.47 - ps less compared to conventional 4 bit MCC delay which is 49.75- ps. Even though the delay of 8 bit MCC gets reduced, number of transistors gets increased in the high speed 8 bit Manchester Carry Chain. As a further work reducing the area of this chain and further reducing the delay by analyzing this design in submicron technology and implementing it in a variable bits like 16 bit, 32 bit Manchester Carry Chain in multi output domino CMOS logic can be considered.

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A Brief Author Biography

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