International Journal of Research and Innovation in Engineering Technology
Volume: 01 Issue: 01
ISSN: 2394 – 4854
Pages: 25 – 32

IJRIET

DESIGN OF AN ENERGY-EFFICIENT CONSTANT DELAY LOGIC FOR LOW POWER APPLICATIONS

N.Akilandeswari[1], R.Vijayabhasker[2]
[1]*PG scholar, Department of Electronics and Communication Engineering*
[2]*Assistant professor, Department of Electronics and Communication Engineering*
Anna University Regional Centre, Coimbatore
Academic Campus, Jothipuram, Coimbatore- 641 047, India.
[1]*akilaece.12@gmail.com*

Abstract

An Energy Efficient Constant Delay Logic (EE-CDL) is proposed in this thesis to reduce the power consumption for low power applications. The EE-CDL is well suited to arithmetic circuits where the critical path is made of a large cascade of inverting gates. It has a unique characteristic where the output is pre-evaluated before the inputs from the preceding stage are ready. The proposed logic style requires low power when compared to the existing CDL. The proposed circuit is designed and using 90-nm, CMOS technology file with supply voltage 1.2V. An inverter is designed using energy efficient feedthrough logic and simulated in MicroWind. The simulation result shows that the proposed logic reduces the power consumption by 88%, 83% and 56% when compared with FTL, Low Power FTL (LP-FTL) and Constant Delay Logic (CDL) respectively. The problem of requirement of inverter as in dynamic logic is completely eliminated in the proposed logic.

Keywords: Constant Delay Logic (CDL), Critical path, Pre-evaluated, Constant delay.

1. INTRODUCTION

Energy efficiency is one of the most required features for modern electronic systems designed for high-performance and portable applications. In one hand, the ever increasing market segment of portable electronic devices demands the availability of low-power building blocks that enable the implementation of long-lasting battery-operated systems.The invention of the dynamic logic in the 80s is one of the answers to this request as it allows designers to implement high performance circuit block, i.e., Arithmetic Logic Unit (ALU), at an operating frequency that traditional static and pass transistor CMOS logic styles are difficult to achieve. However, the performance enhancement comes with several costs, including reduced noise margin, charge-sharing noise, and higher power dissipation due to higher data activity. Because of dynamic logic's limitations and diminished speed reward, a slowly rising need has emerged in the past decade to explore new logic style that goes beyond dynamic logic.

To improve the performance of dynamic logic circuit in terms of speed and power, new logic family called

feedthrough logic was proposed in [5], where FTL concept is extended for the design of low power and high performance arithmetic circuits. This logic works on domino concept along with the important feature that output is partially evaluated before all the inputs are valid. This feature results in very fast evaluation in computational block. In this project, the proposed design of a low power FTL circuit that further improves the power consumption of FTL.

In [5], Navarro-Botello, et al., proposed the design of low power high performance arithmetic circuits using the feedthrough logic concept. Two modes of operation namely reset mode and evaluation mode are introduced instead of pre-charge and evaluation modes in dynamic logic. In this paper, the design of a FTL adder and compare its features with a corresponding adder in standard CMOS. When implemented in a 0.13*nm* CMOS technology process, a low power FTL based 40-bit Ripple Carry Adder (RCA) performs the standard CMOS by 2.6 times in terms of propagation time delay, while maintaining the same figure of Merit and improving the energy consumption per MHz rating by about 31%.

In [9], Shashank parashar, Chaudhry Indra kumar, proposed a new class of logic family for Dynamic CMOS technology based on the feedthrough evaluation concept to increase its noise immunity. In case of FTL its speed is very good but noise immunity is poor. In this work, a new design approach is implemented using FTL concept for high performance dynamic CMOS logic with high noise immunity. A 2 input AND gate has been designed using the improved FTL technique. Further a comparison analysis has been carried out by realizing and simulating the logic circuits in 180*nm* technology at supply voltage of 1.8V. At 180*nm* technology the ANTE & Energy normalized ANTE of proposed technique improved by 2.24X & 2.57X over conventional FTL and power dissipation is reduced by 32% over conventional FTL technique. For the proposed technique, performance improvement has been achieved at the cost of area overhead and higher leakage power dissipation but the overall power dissipation is less. The proposed technique improves dynamic circuit noise immunity with area penalty. Thus this technique can be a better choice for low power and high noise immune applications and can be tailored for the high-speed or low power circuits with long logic depth, such as high-performance Ripple Carry Adder (RCAs) for high noise immunity.

2. EXISTING FTL TECHNIQUES

2.1 Feedthrough Logic (FTL LOGIC)

FTL logic [Figure 1(b)],in CMOS technology was first introduced in [4] and [5]. Its basic operation is as follows: when CLK is high, the predischarge period begins and Out is pulled down to GND through M2. When CLK becomes low, M1 is on, M2 is off, and the gate enters the evaluation period. If inputs (IN) are logic "1," Out enters the contention mode where M1 and transistors in the NMOS PDN are conducting current simultaneously. If PDN is off, then the output quickly rises to logic "1." In this case, FTL's critical path is always a single PMOS transistor. In summary, the main advantages of FTL gate are:

- It only requires NMOS transistor logic expression
- The critical path is constant regardless of the logic expression
- The output is pre-evaluated before the inputs from the preceding stage is ready

Despite its performance advantage, FTL suffers from reduced noise margin, excess direct path current, and nonzero nominal low output voltage, which are all caused by the contention between M1 and NMOS PDN during the evaluation period. Furthermore, cascading multiple FTL stages together to perform complicated logic evaluations is not practical.

Consider a chain of inverters implemented in FTL cascaded together and driven by the same clock. When CLK is low, M1 of every stage turns on, and the output of every stage begins to rise. This will result in false logic evaluations at even numbered stages since initially there is no contention between M1 and NMOS PDN because all inputs to NMOS transistors are reset to logic "0" during the reset period.

ISSN: 2394 – 4854
Pages: 25 – 32

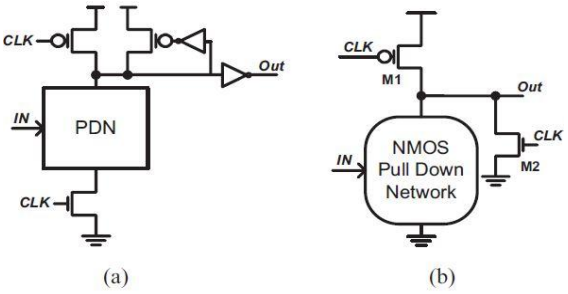

Figure: 1 (a) Dynamic Domino Logic and **(b)** FTL**.**

2.2 Dynamic FeedThrough Logic (DFTL)

In order to mitigate the afore mentioned problems, a dynamic feedthrough logic (DFTL) style (Figure 2) where FTL logic is used in conjunction with dynamic logic implemented by Chuang et al., (2009) [2]. The output of FTL logic does not drive another FTL stage directly. Instead, a dynamic logic is inserted between two FTL stages to act as a buffer while performing logic operation (the concept is similar to compound domino logic). When multiple DFTL stages are cascaded together, transistor M2 in the subsequent stage is no longer required. This is because during the predischarge period (CLK is high), the inputs to the NMOS PDN which come from the dynamic gates of the preceding stage are always charged to logic "1" because the dynamic gates are in the precharge period (driven by CLK'). DFTL eliminates the problem of false logic evaluation associated with cascaded FTL because the inputs to FTL's NMOS PDN are always at logic "1" when first entering the evaluation period. Therefore, FTL gates first enter the contention mode and conditionally make a low to high transition depending on the inputs during the evaluation period.

A global timing window technique was also proposed to reduce the power consumption. However, this caused the output of the FTL stage to be floated when both the window and NMOS PDN are off during the evaluation period. Therefore, a keeper is required at the output of every FTL stage, which increases the layout complexity and reduces the performance advantage. The width of this global window determines the FTL's functionality, since an insufficient window width will cause the FTL to evaluate incorrectly.

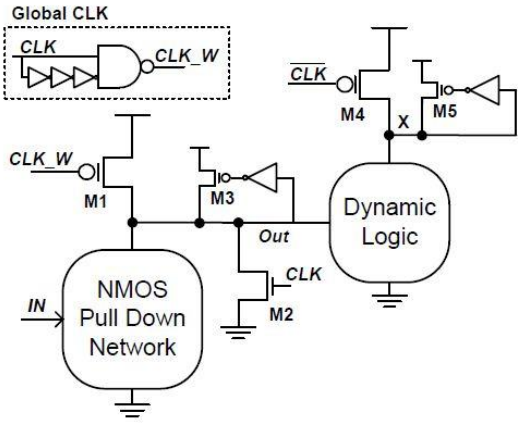

Figure: 2 Dynamic FeedThrough Logic (DFTL)

It is then extremely important to ensure that the width is sufficiently long to ensure proper logic evaluation of all FTL logic gates under temperature, process and load variation. This is clearly not the most optimized design since the output capacitance of every FTL logic can vary significantly, depending on the interconnect wire length and the next stage load. The keeper (M5 in Figure 2) at the output of every dynamic stage also needs to be sized up to maintain sufficient noise margin because of the inevitable glitch caused by the contention in the previous FTL stage. The outputs of both FTL and dynamic logic are heavily influenced by the load and interconnect parasitic capacitance (similar to the problem of dynamic logic' output in compound domino logic).

This raises a reliability problem in a design with many signals lying out in parallel, as the crosstalk of one signal can potentially flip the state of other signals and results in false logic evaluation. Clearly, while DFTL alleviates some of FTL logic's problems, it still requires further work to make this logic style practical.

2.3 Low Power FeedThrough Logic (LP-FTL)

The low power FTL circuit is shown in Figure 3 was implemented by Sauvagya Ranjan Sahoo, Kamala Kanta Mahapatra (2012) [6]. This circuit reduces VOL by using one additional PMOS transistor M_{P2} in series with M_{P1}. The operation of this circuit is similar to that of FTL. During reset phase i.e. when CLK = 1, output node is pulled to ground (GND)

ISSN: 2394 – 4854
Pages: 25 – 32

through M_r. During evaluation phase output node charges through M_{p1} and M_{p2}. When CLK goes low (evaluation phase) M_r is turned off and the output node conditionally evaluates to logic high (VOH) or low (VOL) depending upon input to NMOS block. If the NMOS block evaluates to high then output node pulled toward VDD i.e. VOH =VDD, otherwise it remain at logic low i.e. VOL. Since M_{p1} and M_{p2} are in series the voltage at drain of M_{P1} is less than VDD. During evaluation due to ratio logic the output node pulled to logic low voltage i.e. VOL which is less than the VOL of existing FTL. This reduction in VOL causes significant reduction in dynamic power consumption but due to the insertion of PMOS transistor M_{p2} propagation delay of the LP-FTL increases.

The propagation delay of FTL circuit can be improved by using an NMOS transistor as shown in Figure 4. In order to improve the speed of proposed LP-FTL structure the reset transistor Mr is connected to VDD/2 as shown in Figure 4. The operation of this circuit is as follows, when CLK =1, the output node (OUT) will charges to the threshold voltage VTH.
During evaluation phase according to input value the output node only makes partial transition from VTH to VOH or VOL. Since during evaluation phase the output node (OUT) only makes partial transitions, this improves propagation delay.

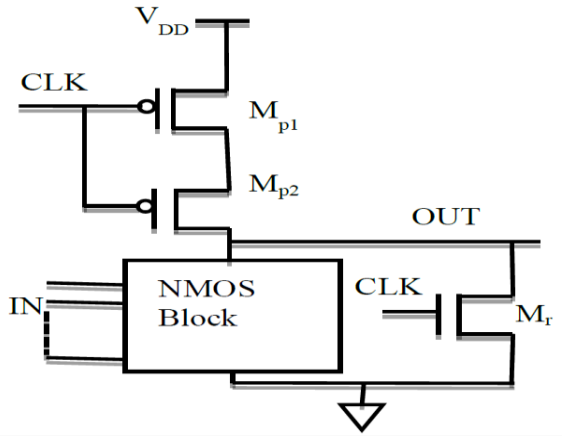

Figure: 3 Low Power Feedthrough Logic (LP-FTL).

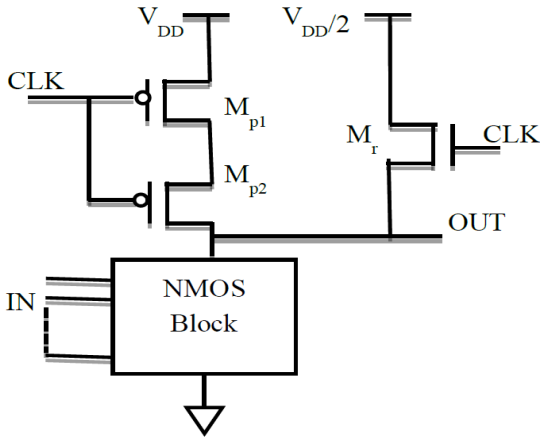

Figure: 4 High Speed LP-FTL

2.4 Modified Feedthrough Logic (MFTL)

The proposed modified circuit is shown in Figure 5 implemented by Sauvagya Ranjan Sahoo, Kamala Kanta Mahapatra (2009) [8] . It consists of an additional PMOS transistor (Tp2) in series with T_{pl}. Since T_{pl} and T_{p2} are connected in series the source voltage of transistor T_{p2} is less than that of VDD. Due to ratio logic VOL reduces as compared to FTL. This reduction in VOL helps in reducing the dynamic power consumption. In order to improve the speed, one or more additional parallel NMOS transistors in the reset block are connected in series with Tn1. The gates of these NMOS transistors are connected to the inputs which having important role in pulling down the output during evaluation phase. These parallel NMOS transistors in the reset block pull output node (OUT) to ground or leave it unchanged during reset phase (when φ=1) depending upon inputs (IN).

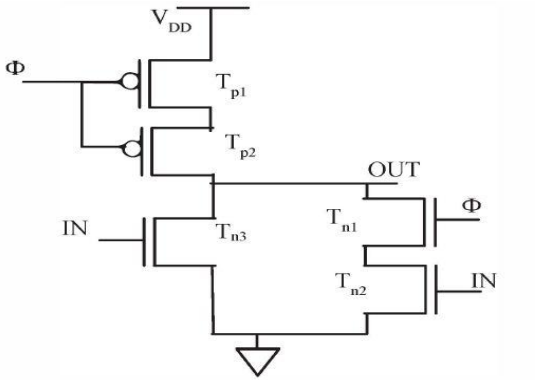

Figure: 5 Modified FeedThrough Logic (MFTL)

ISSN: 2394 – 4854
Pages: 25 – 32

During evaluation phase (when φ=0) according to inputs to the NMOS block OUT node is evaluated to VOH or VOL. The reset block consist one additional NMOS transistor (T_{n2}) in series with T_{n1}. The gate of T_{n2} is connected to the input (IN). During reset phase (φ=1), if IN=1 then node OUT is pull down to ground else node OUT is isolated from ground. During evaluation phase (φ=0), if IN=O node OUT is evaluated to VOH through T_{pl} and T_{p2}, else node OUT pull down to VOL.

2.5 Constant Delay Logic (CDL)

To mitigate the contention problems, CD logic is implemented by Chuang et al.,(2013) [1] with a schematic shown in Figure 6. Timing block (TB) creates an adjustable window period to reduce the static power dissipation. When CLK is high, CD logic pre discharges both X and Y to GND. When CLK is low, CD logic enters the evaluation period and three scenarios can take place: namely, the contention, C–Q delay and D–Q delay modes.

The contention mode happens when CLK is low while IN remains at logic "1". In this case, X is at a nonzero voltage level which causes Out to experience a temporary glitch. The duration of this glitch is determined by the local window width, which is determined by the delay between CLK and CLK_d. When CLK_d becomes high, and if X remains low, then Y rises to logic "1", and turns off M1. Thus the contention period is over, and the temporary glitch at Out is eliminated.

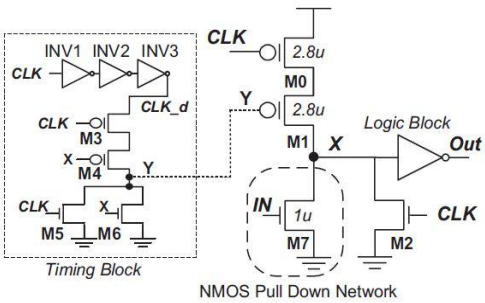

Figure: 6 CD Logic

C–Q delay mode takes places when IN make a transition from high to low before CLK becomes low. When CLK becomes low, X rises to logic "1" and Y remains at logic "0" for the entire evaluation cycle. D–Q delay mode utilizes the pre-evaluated characteristic of CD logic to enable high-performance operations.

In this mode, CLK falls from high to low before IN transit, hence X initially rises to a nonzero voltage level. As soon as IN become logic "0", while Y is still low, then X quickly rises to logic "1". Figure 6 shows the timing waveform of required signals and nodes. If CLK_d rises slightly slower than X, then Y will initially rise (thus slightly turns off M1) but eventually settle back to logic "0". CD logic can still perform the correct logic operation in this case, however, its performance is degraded because of M1's reduced current drivability.

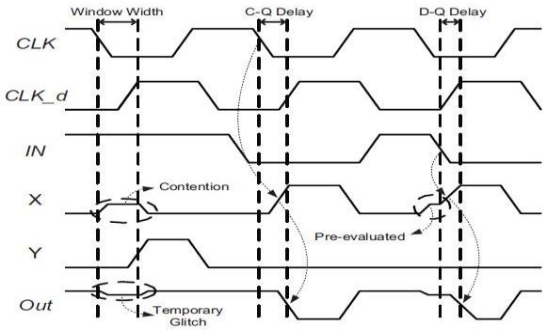

Figure: 7 Timing Diagram of CDL

3. PROPOSED ENERGY-EFFICIENT CONSTANT DELAY LOGIC

An energy efficient constant delay logic (EE-CDL) is proposed in this project to reduce the power consumption for low power applications. The EE-CDL is well suited to arithmetic circuits where the critical path is made of a large cascade of inverting gates. It has a unique characteristic where the output is pre-evaluated before the inputs from the preceding stage are ready. The EE-CDL circuit reduces the power consumption by control the PMOS PUN by feedback technique.

3.1 EE-CDL Schematic Diagram

The proposed EE-CDL circuit is shown in Figure 3.8. This circuit consists of additional PMOS pull up transistor (T3) in series with T1. The T3 transistor is

ISSN: 2394 – 4854
Pages: 25 – 32

controlled by the drain signal of T2 transistor. The inverted clock signal is given to source of T2. The output signal is taken to control gate terminal of T2. T4 transistor is connected to reset the node X, when CLK is high. T6 transistor is used to reset the output terminal. The single bit input signal is given to pull down NMOS transistor T5.

3.2 EE-CDL Operation

There are two modes of operation in EE-CDL circuit namely, reset mode and evaluation mode. When CLK is high, both X and OUT predischarges to GND. Thus the output of EE-CDL circuit is always at logic "0" when CLK is high. So it is called as reset mode. When CLK is low, circuit enters the evaluation mode and the contention mode take place. In the contention mode, CLK is low while input (IN) at logic "1". In this case, both PUN and PDN will simultaneously conduct, which causes a temporary glitch at output node. This will create direct path exist between power supply and ground.

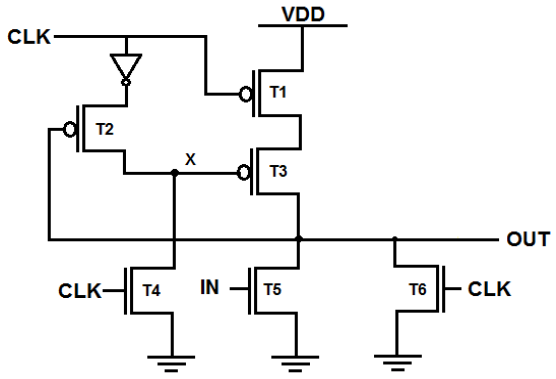

Figure: 8 Schematic Diagram of EE-CDL

The power dissipation occurs due to this short circuit current is known as short circuit power dissipation. This effect can be reducing by EE-CDL circuit. The output node become a non zero voltage level at this mode. This voltage level is used to turn on the transistor T2 by feedback method. The high level inverted clock signal pass through T2 and disables the T3 transistor. Thus the direct path is disabled till the entire contention period and the glitches also eliminated.

3.3 EE-CDL Characteristics

a. EE-CDL versus pseudo-NMOS

Both pseudo-NMOS and EE-CDL are rationed circuits which rely on the correct PMOS to NMOS strength ratio to perform correct logic operations. PMOS transistor width is often selected to be about double the strength of the NMOS PDN as a compromise between noise margin and speed in pseudo-NMOS. On the other hand, EE-CDL always discharges X to GND when CLK is high. So PMOS clock transistors in EE-CDL can be upsized larger to provide more speedup, as long as the output glitch is maintained at an acceptable level.

All logic transistors have a 1-µm effective NMOS width and the PMOS transistors width is 2-µm. The transistor sizing is optimized primary for delay, because the main objective of this section is to explore EE-CDL performance advantage. The clock and data frequencies are set to 1 GHz.

b. Power consumption

EE-CDL always consumes power when it enters the evaluation period. During the evaluation period, EE-CDL always dissipates power via either dynamic power dissipation (OUT is discharged to GND) or direct path current (contention mode). While EE-CDL requires more area compare to static and dynamic, EE-CDL is still an attractive choice in a high-performance full-custom design because very less power consumption without sacrifice speed advantage of FTL.

3.4 *Simulation Result For Power Analysis of 1-Bit Inverter*

A 1-bit inverter is implemented in various logic styles using MICROWIND tool. The various parameters such as power, delay and area are calculated.

The power consumed in FTL is given as 244µW with delay of 5ps. The area required for 1-bit FTL inverter is 31.7µm².

In LP-FTL is given as , which is comparitevely having low power than FTL.Thus the power consumed here is given as174µW with delay of 6ps.

ISSN: 2394 – 4854
Pages: 25 – 32

The area required for 1-bit LP-FTL inverter is 56.7µm² using 90nm technology.

In MFTL is given as , which is comparitevely having low power than LP-FTL.Thus the power consumed here is given as 173µW with delay of 5ps. The area required for 1-bit MFTL inverter is 67.3µm² using 90nm technology.

In CDL is given as , which is comparitevely having low power than MFTL.Thus the power consumed here is given as 64.013µW with delay of 11ps. The area required for 1-bit CDL inverter is 139.5µm² using 90nm technology.

The simulated signal of inverter with power and delay parameters is shown in Figure 9.

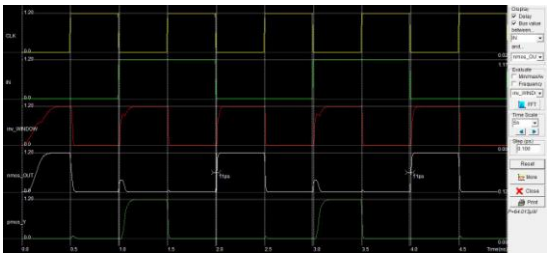

Figure: 9 EE-CDL inverter signal with power and delay

The power consumed in EE-CDL is given as , which is comparitevely having low power than CDL.Thus the power consumed here is given as 28.621µW with delay of 8ps. The area required for 1-bit CDL inverter is 93.4µm² using 90nm technology. The timing block is completely eliminated which is in CDL technique. So the overall area is reduced when compare to CDL.

A. POWER DELAY PRODUCT

Power Delay Product is defined as the amount of energy spent in the system. The power-delay product (PDP) was calculated by following equation:

PDP = Maximum Delay * Average Power (1)

The Power delay product is the figure of merit with energy efficiency of a logic gate or logic family. This power delay product is also known as the switching energy. It is the product of the power consumption and times the input-output delay or the duration of switching even. It measures the energy consumed per switching.

B. IMPLEMENTATION RESULT OF 1-BIT INVERTER IN DIFFERENT LOGICS

Logic Style	Area (µm²)	Power (µW)	Delay (ps)	Power Delay Product(PDP) (fJ)
FTL	31.7	244	5	1.220
LP-FTL	56.7	174	6	1.044
MFTL	67.3	173	5	0.865
CDL	139.5	64.013	11	0.704
EE-CDL	93.4	28.621	8	0.228

Table: 1 Implementation Result for 1-bit Inverter using Different Logic

The table 1 describes about the implementation result of 1-bitinverter in different logics, here the EE-CDL technique consumes low power, less area, less delay and a reduced power delay product (PDP).

4. CONCLUSION

A new energy efficient feedthrough logic was proposed in this project to reduce short circuit power dissipation in contention mode. The pre-evaluated feature of EE-CDL makes it particularly suitable in a circuit block where performance is the primary concern. The proposed logic style requires low power when compare to the existing feedthrough logic.

The proposed circuit is simulated and a comparison analysis has been carried out using 90 nm, 1.2V CMOS process technology. An inverter is designed by FTL techniques and the simulation result in MicroWind environment shows that the proposed logic reduces the power consumption by 88%, 83% and 56% over FTL, LP-FTL and CDL, respectively. The simulation result confirms that at same frequency of operation the power delay product of proposed

circuits is much better than that of existing FTL structure.

References

[1] Chuang.P, Li.D, and Sachdev.M, "Constant delay logic style," IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol.21, No.3,March 2013.

[2] Chuang.P, Li.D, and Sachdev.M, "Design of a 64-bit low-energy high performance adder using dynamic feed through logic," in Proc. IEEE Int. Circuits Syst. Symp., May 2009, pp. 3038–3041.

[3] Deepika Gupta, Nitin Tiwari and R. K. Sarin,"Analysis of Modified Feed-Through Logic with Improved Power Delay Product,"International Journal of Computer Applications (0975 – 8887) Volume 69– No.5, May 2013.

[4] Navarro-Botello.V, Montiel-Nelson.J.A, and Nooshabadi.S, "Analysis of high-performance fast feedthrough logic families in CMOS," IEEETrans. Circuits Syst. II, Exp. Briefs, vol. 54, no. 6, pp. 489–493, Jun.2007.

[5] Navarro-Botello.V, Montiel-Nelson.J.A, and Nooshabadi.S, "Low power arithmetic circuit in feedthrough dynamic CMOS logic," in Proc. IEEE Int. 49th Midw. Symp. Circuits Syst., Aug. 2006.

[6] Sauvagya Ranjan Sahoo, Kamala Kanta Mahapatra,"Design of Low Power and High Speed Ripple Carry Adder Using Modified Feedthrough Logic", in 2012 International Conference on Communications, Devices and Intelligent Systems (CODIS),2012.

[7] Sauvagya Ranjan Sahoo1, Kamala Kanta Mahapatra,"Noise Tolerant Circuit Techniques For High Performance Feedthrough Logic", International Conference on Emerging Trends in Science, Engineering and Technology, 2012.

[8] Sauvagya Ranjan Sahoo, Kamala Kanta Mahapatra,"Performance Analysis of Modified Feedthrough Logic for Low Power ,"in IEEE -International conference on advances in engineering, science and management, 2012.

[9] Shashank parashar, Chaudhry Indra kumar,"An Efficient Design Technique for High Performance Dynamic Feedthrough Logic with Enhanced Noise Tolerance,"IEEE Computer Society Annual Symposium on VLSI, 2011.

[10] M. Aguirre-Hernandez and M. Linares-Aranda, "CMOS CMOS Full-adders for energy-efficient arithmetic applications," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 99, pp. 1–5, Apr. 2010.

[11] K. H. Chong, L. McMurchie, and C. Sechen, "A 64 b adder using selfcalibrating differential output prediction logic," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, Feb. 2006, pp. 1745–1754.

[12] L. McMurchie, S. Kio, G. Yee, T. Thorp, and C. Sechen, "Output prediction logic: A high-performance CMOS design technique," in *Proc. Comput. Des. Int. Conf.*, Austin, TX, 2000, pp. 247–254.